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Nanoscale Electronic Devices

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

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in

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by

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ABSTRACT OF THE DISSERTATION

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Continuous downscaling in microelectronics has pushed conventional CMOS technology to its physical limits, while Moore's Law has correctly predicted the trend for decades, each step forward is accompanied with unprecedented technological difficulties and near-exponential increase in cost. At the same time, however, demands for low-power, low-cost and high-speed devices have never diminished, instead, even more stringent requirements have been imposed on device performances. It is therefore crucial to explore alternative materials and device architectures in order to alleviate the pressure caused by downscaling. To this end, we investigated two different approaches: (1) InSb nanowire based field effect transistors (NWFETs) and (2) single walled carbon nanotube (SWCNT) – peptide nucleic acid (PNA) –SWCNT conjugate.

Two types of InSb nanowires were synthesized by template-assisted electrochemistry and chemical vapor deposition (CVD) respectively. In both cases, NWFETs were fabricated by electron beam lithography (EBL) and crystallinity was confirmed by transmission electron microscopy (TEM) and selected area diffraction (SAD) patterns. For electrochemistry nanowire, ambipolar conduction was observed with strong p-type conduction, the effect of thermal annealing on the conductivity was analyzed, a NWFET model that took into consideration the underlapped region in top-gated NWFET was proposed. Hole mobility in the channel was calculated to be 292.84 $cm^2V^{-1}s^{-1}$ with a density of $1.5\times10^{17}/cm^3$. For CVD nanowire, the diameter was below 40nm with an average of 20nm. Vapor-liquid-solid (VLS) process was speculated to be the mechanism responsible for nanowire growth. The efficient gate control was manifested by high I_{ON}/I_{OFF} ratio which was on the order of 10^6 and a small inverse subthreshold slope (<200 mV/decade). Scale analysis was used to successfully account for disparities observed among a number of sample devices. N-type conduction was found in all NWFETs with electron mobility between 110 $cm^2\cdot V^{-1}\cdot s^{-1}$ and 169 $cm^2\cdot V^{-1}\cdot s^{-1}$.

In the approach of SWCNT-PNA-SWCNT conjugate, we chemically functionalized single walled carbon nanotubes to synthesize the conjugate and characterized its electrical properties. Negative differential resistance (NDR) was observed consistently at different temperatures and the mechanism was explained through the energy band diagram in which NDR effect was caused by misalignment between Fermi energy level at

the source and resonance states in the potential well. The consistent NDR effect shows possible application for microelectronic devices.

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Chapter 1 Introduction

Last century has witnessed a breathtaking progress in microelectronics led by CMOS technology. The continuous drive for better functionality and higher operation speed is best manifested by Moore's Law[1], which predicts that the number of transistors on a chip doubles every 18 months. While Moore's Law has proven to be correct for the past several decades, the ultimate physical limit and increasingly severe short channel effects cannot be ignored.

To prevent Moore's Law from hitting the wall, more stringent requirements have been put on different aspects of current technologies so as to achieve extremely small feature sizes, however, each step of recent improvement was accompanied with near-exponential increase in cost[2], which therefore forces scientists and engineers to seek alternatives to cross the financial as well as technical barrier. Different new materials and device architectures have been brought up in the endeavor to alleviate the pressure caused by downscaling while still achieving improved performances, among which are FinFET structure[3], high-K dielectric technology[4], strained silicon technology[5] etc. However, all of these technologies are still lithographically based top-down approach that suffers from above mentioned disadvantages.

Nanotechnology, which deals with structures sized 100nm or smaller, is not just the technological continuation of downscaling, rather, it exemplifies the concept of self-assemble capability in nanostructure, which means that material structure could organize

itself in a way that is independent of lithography-based top-down process, as a result, could achieve unprecedented integration density. Also, due to quantum effects, nanostructures with novel optical, electrical or mechanical properties have been demonstrated. To utilize nanostructures as building elements for microelectronics, these novel properties deserve full exploitation and have thus drawn great research attention in recent years.

My PhD work consists of studies of electrical properties in two nanostructures: semiconductor (InSb) nanowires, carbon nanotubes-molecular conjugates. The thesis is organized as follow: chapter one gives overall introduction and discusses downscaling trend in microelectronic devices; chapter two discusses synthesis of semiconductor nanowires, fabrication of nanowires based field effect transistor (NWFET) and electrical characterization of NWFET; chapter three discusses synthesis and energy band formation in single walled carbon nanotube (SWCNT) – PNA - SWCNT conjugate and explains the measured electrical properties especially negative differential resistance (NDR) effect based on resonant tunneling diode (RTD) model; chapter four concludes this work.

Chapter 2 Nanowire Based Field Effect Transistor

2.1 Introduction

Semiconductor nanowire based field effect transistor has drawn great attentions since its inception. As an example of 1D material system, nanowire holds unique physical properties due to quantum confinement effects[6]. Also due to the low dimensional nature, nanowires tend to have a large surface to volume ratio especially in free standing case, which puts it in a better position comparing to conventional devices for applications such as gas[7, 8] and bio-molecule sensors[8].

Different types of NWFETs have been experimentally implemented by different research groups: Cui Y. et al had first studied electrical transport properties in single crystal, n-type and p-type Si nanowire prepared by laser catalytic growth[9] [10] and had found the transconductance and carrier mobility in Si NWFET to be better than that in state-of-the-art planar silicon devices[11]. Huang Y. et al pushed nanowire work further by assembling crossed nanowire p-n junctions and configured these nanowire transistors into logic gate structures with OR, AND and NOR functionalities[12]. Wang D. et al had synthesized Ge nanowires by low-temperature chemical vapor deposition method and fabricated top-gated Ge NWFET with high-k HfO_2 as gate dielectric with which they obtained hole mobility of 600cm^2/Vs[13]; Fan Z. et al had synthesized single-crystal ZnO nanowires using vapor trapping chemical vapor deposition method and explored oxygen sensing properties through ZnO NWFET in which the oxygen detection sensitivity could be modulated by the gate voltage[14] while Wang X. et al demonstrated a piezoelectric

field effect transistor (PE-FET) that utilized semiconducting and piezoelectric dual properties of ZnO. The source to drain current in PE-FET is controlled by bending of nanowire and the mechanism was speculated to be associated with carrier trapping effect and the creation of charge depletion zone under elastic deformation[15]. Since typical nanowire transistor has a horizontal layout with either backgate or topgate geometry, the typical effort required to align and integrate nanowire components to high density planar circuit remains an obstacle for widespread application, Goldberger J. et al demonstrated direct vertical integration of Si nanowire into surrounding gate field effect transistor without the need of post-growth assembly processes[16]. The achieved electronic properties were comparable to other horizontal NWFETs, however, the advantages of vertical assembly was compromised by large contact resistance and difficulties in direct controlling the gate of any single nanowire etc. Heterostructure nanowire based devices had also been studied. Xiang J. et al had demonstrated that Si/Ge core-shell NWFET outperform state-of-the-art MOSFET three to four times in terms of scaled transconductance and was comparable to carbon nanotube based FET in terms of intrinsic switch delay CV/I. The advantage of Si/Ge core-shell structure came from the 500meV valence band offset which served as a confinement potential to the hole-gas[17]. Dayeh S. et al had synthesized InAs nanowire through CVD process and developed a model which took into consideration ungated nanowire regions and contact resistance that allowed more accurate estimation of nanowire characteristics. The InAs NWFET demonstrated the highest electron mobility (6580 $cm^2V^{-1}s^{-1}$) among all reported values for NWFETs[18].

There has been, however, few research on InSb nanowire based devices [19, 20], especially on NWFET[21]. Motivation also comes from the fact that InSb as a direct bandgap semiconductor material holds the largest electron mobility among all semiconductors, therefore, a systematic and detailed study on InSb NWFET is of vital importance.

2.1.1. Mechanism of MOSFET

The essential functionality of a transistor is switching, which means the conduction of charge carrier is controlled by another signal. The schematic of a typical metal oxide semiconductor field effect transistor (MOSFET) is shown in figure 1.

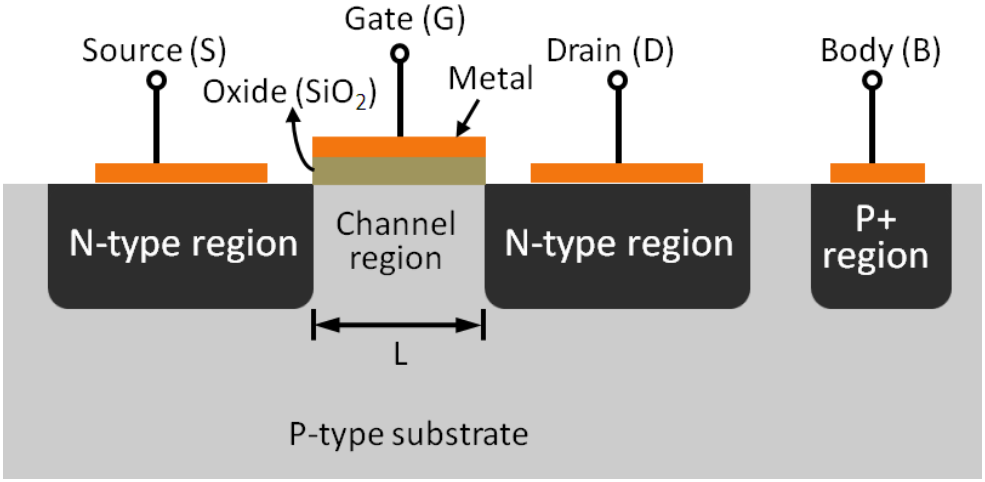

Figure 1 Cross-section view of N-type MOSFET.

Key parameters of a MOSFET are: I_{ON} (conduction current), I_{OFF} (leakage current), g_m (transconductance), noise, breakdown voltage etc. A typical I-V curve of N-type MOSFET is shown in figure 2.

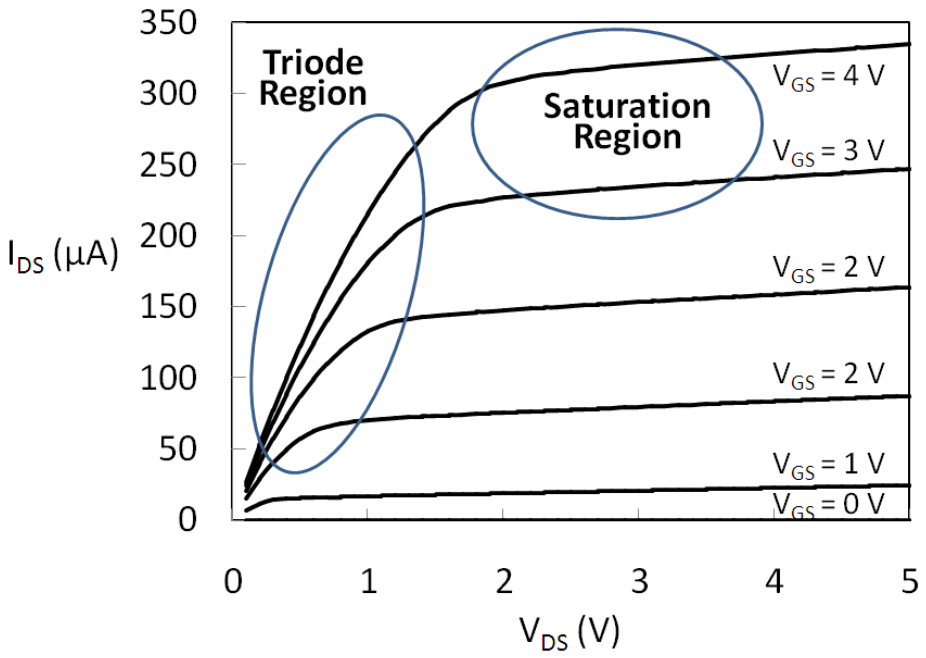

Figure 2 I-V curve of N-type MOSFET

Depending on gate-to-source voltage, the operation of a MOSFET is divided to three regions: cut-off region, in which gate-to-source voltage is smaller than threshold voltage and no carriers exist in the channel; triode region, in which channel carriers exist throughout the channel and saturation region, in which carriers exist in the channel but are pinched in the vicinity of drain region. In most cases, MOSFET is biased to work in the saturation region where current is solely a function of gate-to-source voltage.

2.1.2. Scaling and Short Channel Effects

The primary reason for MOSFET downscaling is that cost per device is reduced with smaller chip size; another reason is that the transistor is able to run faster with smaller channel length, as unit gain frequency of a MOSFET is determined by

$$f_T = \frac{3}{4\pi}\frac{\mu(V_{GS} - V_t)}{L^2}$$

in which μ is the carrier mobility in the channel (electron for N-type MOSFET, hole for P-type MOSFET), V_t is the threshold voltage of the transistor.

In ideal case, device scaling in MOSFET is as follow:

Dimension: t_{OX}, L, W, X_j	1/S
Substrate Doping: N_A	S
Supply Voltage: V	1/S
Oxide Capacitance: WL/t_{OX}	1/S

Table 1 Scaling rules in MOSFET

MOSFET parameters change as follows:

Current

$$I_{DS} = \mu C_{OX}\frac{W}{L}\frac{(V_{GS} - V_t)^2}{2} \propto 1 \times S \times \frac{1/S}{1/S} \times (1/S)^2 = \frac{1}{S}$$

Total gate capacitance

$$C = \varepsilon\frac{WL}{t_{ox}} \propto \frac{S \times S}{S} = S$$

Group delay

$$\tau = \frac{CV}{I} \propto \frac{1/S \times 1/S}{1/S} = \frac{1}{S}$$

Power dissipation

$$P = IV \propto \frac{1}{S} \times \frac{1}{S} = \frac{1}{S^2}$$

Power-Delay product

$$P \times \tau = IV \times \frac{CV}{I} \propto \frac{1}{S^2} \times \frac{1}{S} = \frac{1}{S^3}$$

However, the benefit of MOSFET scaling is compromised in reality due to short channel effects (SCEs) that become more and more severe as downscaling continues.

(1). Channel-length modulation. As indicated in figure 2, current increases as V_{DS} increases at saturation region, leading to a finite output resistance. This effect can be modeled by adding a channel length modulation factor λ into the expression of channel current.

(2). Drain-induced-barrier-lowering (DIBL), in which case the potential barrier exists between source and channel under weak inversion is lowered by drain voltage, leading to an increased drain current that is not just a function of gate voltage, but also drain to source voltage. This effect can be modeled as:

$$V_T = V_{T0} - \Delta V_{T0}$$

where

$$\Delta V_{T0} = \frac{1}{C_{OX}} \sqrt{2q\varepsilon_{Si} N_A |2\phi_F|} \cdot \frac{x_j}{2L} [\left(\sqrt{1 + \frac{2x_{dS}}{x_j}} - 1 \right) + (\sqrt{1 + \frac{2x_{dD}}{x_j}} - 1)]$$

in which ΔV_{T0} is proportional to $\frac{x_j}{L}$ and therefore increases with shorter channel lengths and with increasing V_{DS}.

(3) Sub-threshold conduction. As indicated in figure 3, MOSFET also conducts current at voltages below the threshold voltage and the drain current under this condition depends exponentially on V_{DS}

$$I_{DS} = I_S e^{\frac{V_{GS}}{\frac{nkT}{q}}} \left(1 - e^{-\frac{V_{DS}}{\frac{kT}{q}}}\right)(1 + \lambda V_{DS})$$

The screening length

$$\lambda = \sqrt{\left(\frac{\varepsilon_0 \varepsilon_{NW}}{\varepsilon_{OX}}\right) d_{NW} d_{OX}}$$

provides a measure of how effectively the gate potential ϕ_{gs} modulates the surface potential ϕ_f.[22] When channel length L is comparable or smaller than screening length, short channel effects dominate.

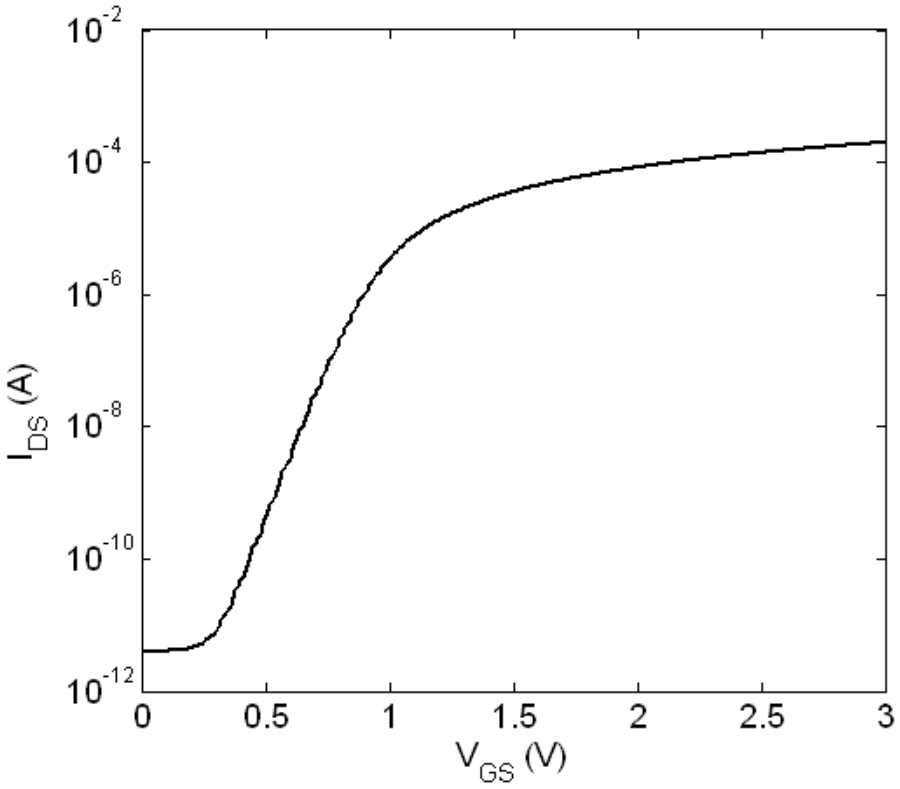

Figure 3 $I_{DS} - V_{GS}$ of MOSFET

All these detrimental effects can only become worse as downscaling of MOSFET continues. At the same time, the demand for better functionality and higher operation speed has never stopped; better functionality often translates into more complex circuits and requires circuit with higher density. To meet the seemingly contradictory requirements, alternatives materials systems or circuit architectures need to be exploited.

2.1.3. Nanowire FET

Nanowire refers to the type of structures with diameter under 100nm, in which charge carriers are confined to move in only one dimension, as a result, it has discrete energy bands and presents unique electrical[23-25], mechanical[15, 26-33] and optical[34-40] properties. As physical limits of downscaling in conventional CMOS techniques are approached, more and more research attentions are given to nanowire based field effect transistor (NWFET)

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A schematic of NWFET is presented in figure 4.

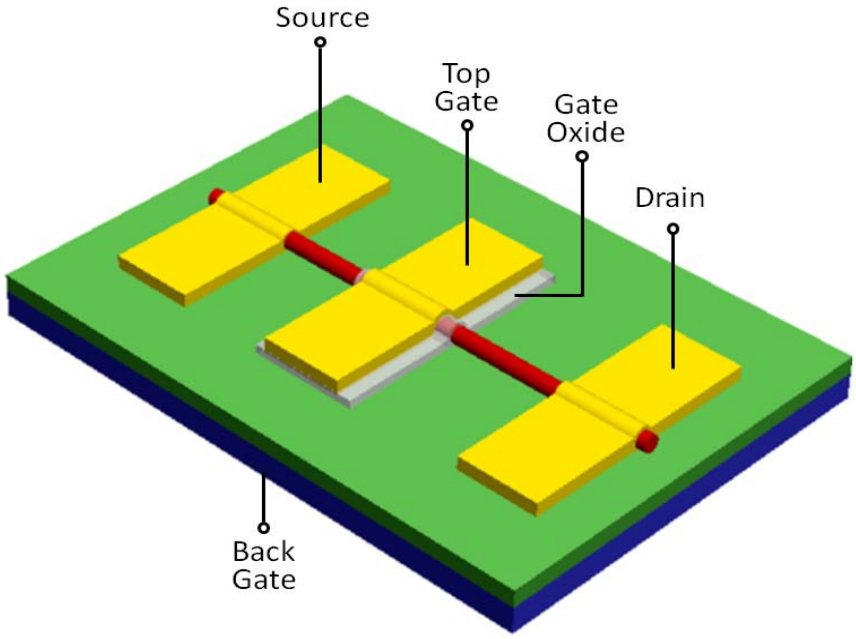


Figure 4 Schematic of nanowire field effect transistor (NWFET)

The structure of NWFET is similar to MOSFET in terms of terminals (source, drain, top gate and back gate). The carriers in the channel are controlled by applied gate voltage which shifts up or down energy bands through field effect as illustrated in figure 5.

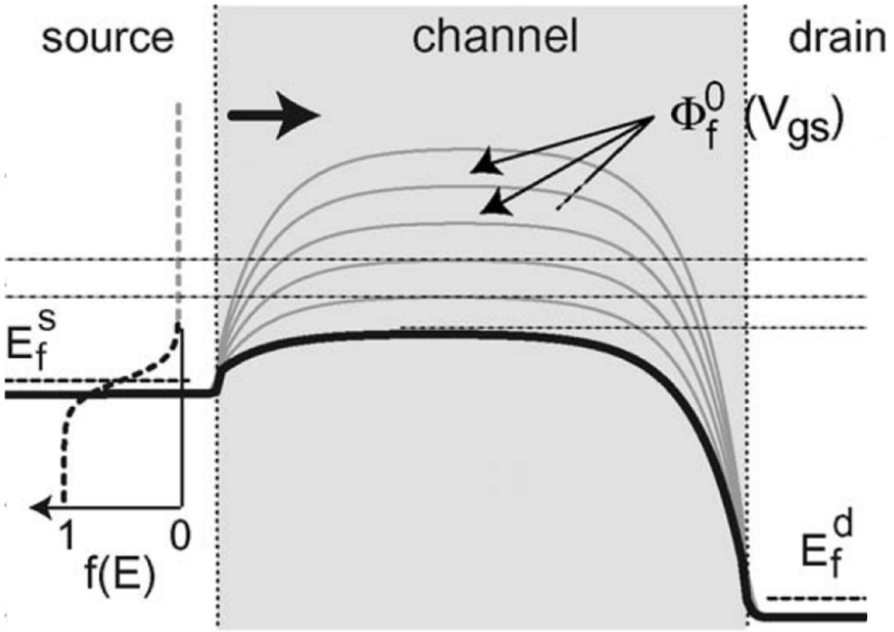


Figure 5 Energy bands diagram in field effect transistor

In 1-D case, the density of state (DOS) is

$$\rho_{DOS}^{1D}(E) = \frac{1}{\pi\hbar}\sqrt{\frac{m^*}{2(E-E_0)}}$$

The probability for energy level E to be occupied by electron at temperature T is given by Fermi function

$$f(E) = \frac{1}{e^{(E-E_f)/kT}+1}$$

The surface potential $\Phi_f(x)$ is in the FET channel is described by 1-D Poisson equation in the following form:

$$\frac{\partial^2 \Phi_f(x)}{\partial x^2} - \frac{\Phi_f(x) - \Phi_{gs} - \Phi_{bi}}{\lambda^2} = -\frac{e\rho(x)}{\varepsilon_0 \varepsilon_{NW}}$$

where Φ_{gs} and Φ_{bi} are the gate and built-in potentials respectively, ρ is carrier density, therefore, the charge density in NWFET channel is

$$n = \sum_{\upsilon} g_{\upsilon} \int_{E_{\upsilon}^n}^{\infty} \frac{D_{\upsilon}^n(E)}{2} [f(E - E_s) + f(E - E_d)] dE$$

where E_{υ}^n is the conduction minimum for the nth subband, $D_{\upsilon}^n(E)$ is the density of state, g_{υ} is the valley degeneracy at υ valley.

With the 1D density of state as stated above, the total charge in the nanowire channel can be found as [41]

$$Q_{NW} = \frac{q\sqrt{2k_B T}}{2\pi\hbar} \sum_n \sum_{\upsilon} g_{\upsilon} \sqrt{m_d^{\upsilon}} \{ \int_0^{\infty} \frac{E^{-1/2} dE}{1 + e^{\left[\frac{E + E_{\upsilon}^n - q\psi_s}{k_B T}\right]}} + \int_0^{\infty} \frac{E^{-1/2} dE}{1 + e^{\left[\frac{E + E_{\upsilon}^n - q(\psi_s - V_{ds})}{k_B T}\right]}} \}$$

Where m_d^{υ} is effective mass, k_B is Boltzman constant, T is absolute temperature, and q is electronic charge. To get transfer properties of NWFET, transport mechanism needs to be determined. There are mainly two transport mechanisms: ballistic transport and drift-diffusion transport.

In ballistic transport, electrons do not experience any scattering while moving through the medium, their trajectories change only when hitting the inner boundary. Ballistic transport is an ideal scenario in general. However, if the mean free path (MFP) of

electron in a particular medium is longer than the dimension of the medium in the direction of transport, ballistic transport can be approximated.

By means of the Landauer approach[42], channel current in ballistic transport can be expressed as

$$I = \frac{q}{\pi\hbar}\sum_{v}\sum_{n} g_v[\int (f_S(E) - f_D(E)) \cdot T(E) dE]$$

The quantity $\frac{q}{\pi\hbar}$ is the current carried per occupied subband per unit energy, T(E) is the transmission probability, which is unit when $E > \Phi_f^0$ (maximum of potential barrier in the channel), when $E < \Phi_f^0$ channel current can be expressed as

$$I = \frac{q}{\pi\hbar}\sum_{v}\sum_{n} g_v \ln[\frac{1 + e^{\frac{E_{FS} - \Phi_f^0}{kT}}}{1 + e^{\frac{E_{FD} - \Phi_f^0}{kT}}}]$$

In real devices scattering is not negligible and hence, ballistic transport model does not accurately predict current in these devices, in which case, drift and diffusion becomes two dominating, yet competing factors, drift is movement of charge due to electric fields, and diffusion is the flow of charges due to density gradients. The carrier mobility is defined as

$$v_{N,P} = \mu_{N,P} E$$

N and *P* refer to electrons and holes respectively. As electric field increases, the average carrier velocity and the average carrier energy increase. However, for every semiconductor material, there exists a point when further increase in electric field does not increase the average carrier velocity any more, which is called velocity saturation.

The reason for velocity saturation is that interaction between high energy electron and crystal lattice becomes much stronger at higher electric fields, and extra energy is then transformed to emitted phonons. To model this effect, field dependent mobility is introduced and defined as

$$\mu = \frac{\mu_0}{1 + \frac{\mu_0}{v_{sat} L_{eff}} V_{DS}}$$

drift-diffusion current can then be obtained as

$$I_{DS} = \frac{\mu}{L_{eff}} \int_0^{V_{DS}} Q_{NW}(V_{GS}, V_{DS}) dV$$

2.2 CVD Based InSb Nanowire FET (NWFET)

2.2.1 Synthesis and Characterization of InSb Nanowire

InSb is a direct bandgap semiconductor material with an extremely small bandgap of 0.17eV[43]. Its electron mobility is as high as 78,000cm^2/ (V·s)[44] and carrier ballistic length is as long as 0.7um at 300K, which is the longest among a variety of semiconductor materials. Such high electron mobility makes it an attractive candidate for high speed electronic devices, to date, Intel and QinetQ have developed quantum well field effect transistor with operating speed as high as 305 GHz at gate length of 85nm[45]. In these devices, transistor was fabricated on semi-insulating GaAs substrate and InSb region is “sandwiched” by high bandgap $Al_yIn_{1-y}Sb$ layers, to serve as buffer to accommodate lattice mismatch. The demonstrated device showed 50% higher intrinsic switching frequency and 10 times reduction in DC power compared to Si MOSFET.

While the quest for high speed electronic devices has never slowed down, reports on InSb nanowire remain scarce, which is the main incentive for this work.

Different nanowire synthesis methods have been proposed over the years.[24, 46-54] Among them two most popular ones are chemical vapor deposition (CVD) assisted method and electrochemistry assisted method.

Chemical vapor deposition is conventionally used to deposit high quality thin film of materials. The use of CVD process for the synthesis of semiconductor nanowire was an accidental discovery[55, 56] and had developed into a general strategy.

The procedure of nanowire synthesis is illustrated in figure 6 and can be summarized into following steps:

(1). Cleaning of InSb substrate with surface orientation in (001) direction.

(2). A thin film of gold with thickness of 1nm is deposited onto the substrate through electron-beam evaporation.

(3). Gold coated InSb substrate is then placed inside CVD furnace and heated at 400℃ for 15 min, during which period thin film of gold deforms to metal clusters at sparse locations, and particles of Au-In-Sb alloy are formed with an average diameter of 5-10 nm.

(4). A small quartz well is filled with InSb power and placed in the middle section of the CVD furnace, annealed InSb substrate is then placed next to the quartz well

at the downstream side. The exact positions of both are critical as a result of the temperature gradient inside the furnace; the condition of the synthesis is tuned such that when the temperature at InSb power spot is 550℃, the temperature at annealed substrate is 400℃. The furnace is then heated for 1 hour during which time, Argon and Hydrogen gas are fed into the furnace at a rate of 100 sccm, resulting InSb nanowire with an average length of 10-20um.

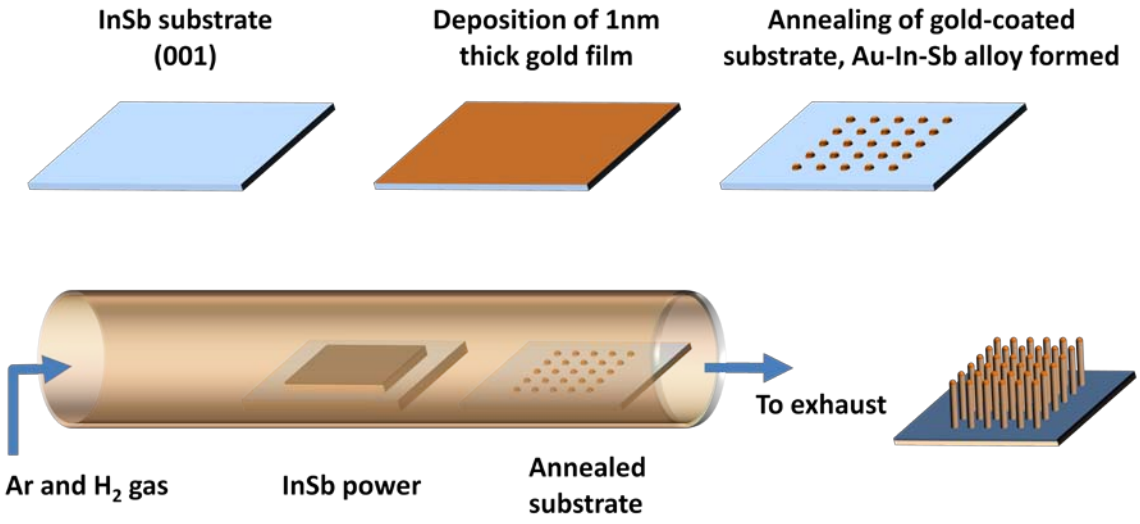


Figure 6 Procedures of chemical vapor deposition (CVD) assisted nanowire synthesis

The growth of InSb nanowire follows vapor-liquid-solid (VLS) mechanism as illustrated in Fig 7. The starting point of the process is Au-In-Sb alloy which is formed after the coated substrate is annealed, as the annealed substrate and InSb power are heated up, InSb power vaporize and is then carried downstream by Argon and Hydrogen gas, the vaporized InSb is then adsorbed by the alloy. As more and more InSb gas was adsorbed, the alloy reaches its supersaturation point and nucleates at its interface from the substrate.

The gold particle is “pushed up” as a result of nucleation, and leads the continual 1-D growth of nanowire.

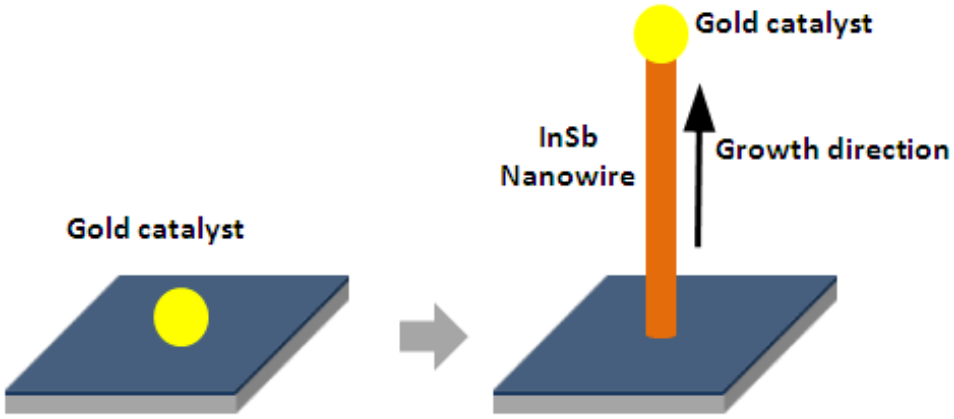


Figure 7 mechanism of gold catalyst assisted nanowire growth

A number of factors determine the quality of synthesized nanowires, such as temperature, pressure, thickness of deposited gold film etc. While optimizing the growth condition is largely a try-and-error process, a few key principles can be followed.

(1). Thickness of gold film determines the size of gold seeds, thicker films tend to form bigger metal clusters and as a result lead to nanowires with larger diameters.

(2). Optimal growth temperature exists in terms of the shape of nanowire. At too low a temperature, gold seeds do not fully melt which impede the adsorption process while at too high a temperature, nanowires tend to grow at multiple angles from one gold seed, and more often renders “bushy” nanowires. The choice of growth temperature also depends on the melting point of the catalyst seed and that of the semiconductor material[57].

(3). Gas pressure controls the growth of nanowire in a sense that the flux of gas precursor to the liquid Au surface is proportional to the gas pressure. However, in steady state the growth rate is determined by the rate for adsorption and crystallization.

The crystallinity of synthesized nanowire can be confirmed by HRTEM images shown below:

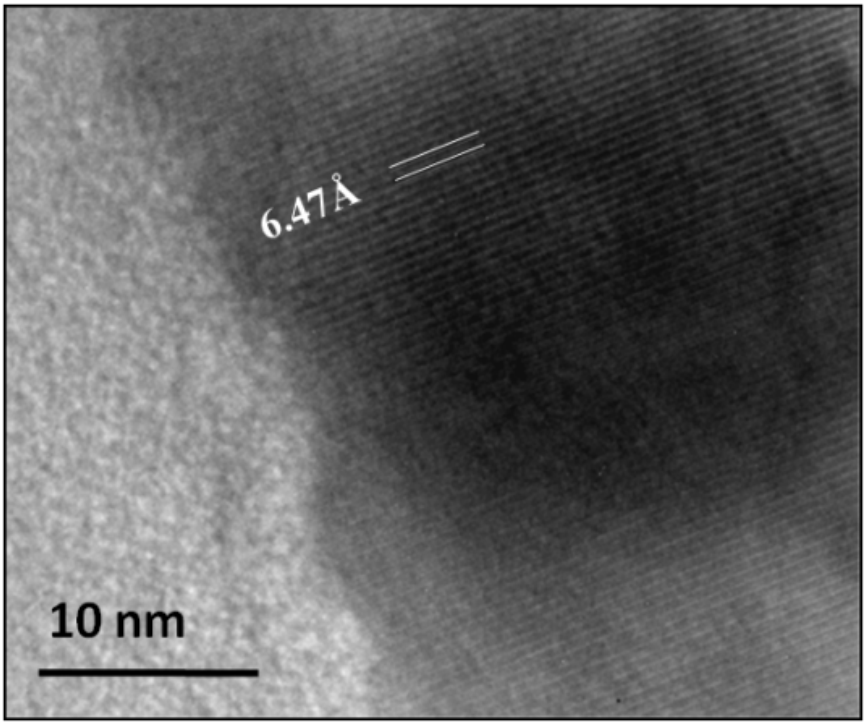


Figure 8 Image from high resolution transmission electron microscopy (HRTEM) of InSb crystal lattice shows lattice constant of 6.47 angstrom.

Selected area diffraction (SAD) pattern also demonstrated single crystallinity of synthesized nanowire.

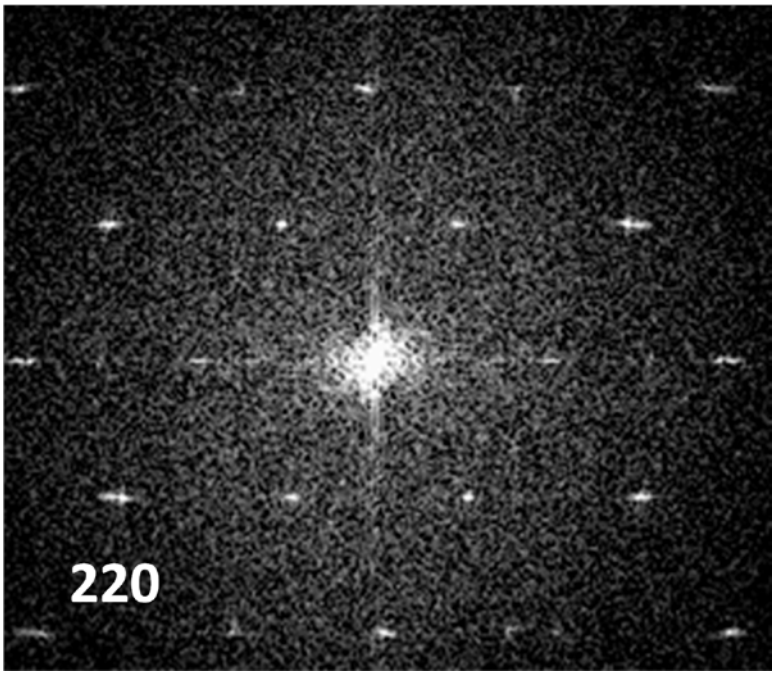


Figure 9 Selected area diffraction (SAD) pattern of InSb nanowire.

2.2.2 Fabrication of NWFET

InSb nanowires are stick to the substrate after synthesis, so the first step is to sonicate nanowires off the substrate and is done by immersing the substrate in isopropyl alcohol (IPA) for 1 min, the amount of IPA determines the density of final nanowire solution. The solution is then dip-coated onto Si/SiO_2 substrate with pre-drawn alignment marks. These alignment marks will be used for locating single nanowire during electron beam lithography (EBL). The dip-coated substrate is then blow dried and baked for 10 min to free the surface with any water molecules. The substrate is then spin-coated with bi-layer process sequentially MMA and PMMA (polymethyl methacrylate), the reason the bi-layer process is that MMA has a smaller molecular weight and higher solubility than PMMA, and hence when a pattern is exposed, hollow regions underneath the brinks of

the remaining structure is also created, which makes it possible to get isolated metal patterns and keeps them from being stripped off by adjacent undesired metal layers.

The above procedures of spin coating can be summarized as follow:

(1). Bake the NW-coated substrate at 180℃ for 10 minutes.

(2). Spin coating of MMA onto the substrate at 3800 rpm for 45 seconds, which results in a layer of 250nm in thickness, then baked at 180℃ for 15 minutes, followed by spin coating of PMMA at 4000 rpm for 45 seconds, which results in a thickness of 300nm and then post bake for 10 minutes.

Note that e-beam resists as well as photoresist are carcinogenic chemicals therefore spin coating has to be carried out under vacuum hood.

Electron beam lithography is then used to open windows on e-beam resist coated substrate. The multiple steps for e-beam lithography are summarized as below:

(1). Dip a few droplet of silver paste on a corner of the coated substrate and place it inside SEM chamber.

(2). Adjust SEM image and focus on any silver particles.

(3). Adjust working distance of electron beam and height of sample stage so that the working distance is 6mm when image is focused at which time the focal point of electron beam is on the surface of the substrate.

(4). Turn on electron beam blanker and turn on NPGS electron beam control system.

(5). Set parameters such as beam current, area dose, line dose and measured beam current, run NPGS program and exposed selected area according to pre-drawn pattern. (Since a

larger aperture allows more electrons to expose the substrate, and large beam current result, which could greatly reduce the exposure time. Larger apertures such as 60um or 120um are used when drawing large patterns such as major contact lines or bonding pads) (6). After exposure, turn off NPGS system and switch back to SEM control, turn off electron beam gun and purge the chamber with Nitrogen gas and take out sample.

The next step is to develop the exposed area, steps are summarized as below:

(1). Clean and blow dry three 50ml beakers.

(2). Developer used here is MIBK/IPA solution, with volume ratio of MIBK to IPA 1:3. Fill three beakers with MIBK/IPA, isopropyl and water respectively.

(3). Use self-closed tweezer to hold the chip and dip it into MIBK/IPA solution for 80 seconds, and immediately dip it into isopropyl for 2 minutes, then rinse it with isopropyl for 30 seconds, rinse it with DI water for 30 seconds, blow dry with nitrogen gas.

More often than not, above develop process cannot fully dissolve the exposed e-beam resist, which leaves spots or tiny areas of residues which will adversely affect the quality of lithography. As a result, descumming is used to further clean up developed regions in the substrate. In our case, inductively coupled plasma (ICP) system is used for descumming, the steps for ICP process can be summarized as follows:

(1). Purge the ICP chamber three times and open it.

(2). Glue the chip onto a six inch wafer and load it inside the ICP chamber

(3). Set oxygen flow rate to 100sccm and power to 500 W, set the duration time to 12 seconds to have residues thoroughly cleaned.

The next step is metal deposition. In this work, it is carried out by electron beam evaporator, the procedures of metal deposition is as follow:

(1). Check the cover glass is clean.

(2). Check availability of desired metal source.

(3). Check whether detector's crystal life is over 80, if not, replace it with a new one.

(4). Check whether all power sources are ready.

(5). Keep descummed chip on six inch wafer and place the wafer inside the ebeam evaporator chamber facing down.

(6). Close the chamber and start pumping till the pressure is below $2 \cdot 10^{-6}$ torr.

(7). Set desired metal source, film thickness, deposition rate. In this work, Titanium and Gold are used as metal contacts, with thickness of 10nm and 80nm respectively. The deposition rate determines quality of the metal film, so it's desirable to set it to a smaller value, in our case, deposition rate is set to be 0.1 Å/second.

(8). When deposition is finished, wait till the chamber cools down before taking out the sample. Note that most metals are easily oxidized at high temperature in the air, which reduces their conductivities.

Lift-off is used to remove unwanted metal pieces and the procedures are:

(1). Dip the metal coated chip in acetone for five to ten minutes, PMMA/MMA dissolve in acetone and as a result, metal pieces on top of them are left free.

(2). If deposited metals at the edge of the chip are hard to remove, and therefore a gentle shaking or even one to two seconds of sonication is necessary to strip off the metal pieces, also important in lift-off is that chip should never be taken out of acetone solution before unwanted metal pieces are completely removed.

A SEM image of fabricated NWFET is shown in figure 10.

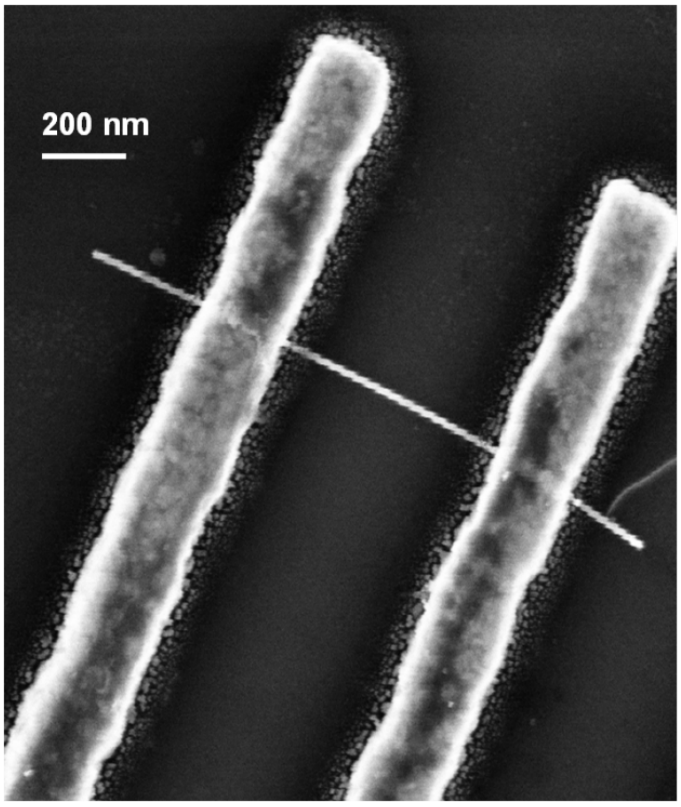


Figure 10 SEM image of fabricated InSb NWFET

2.2.3 Electrical Characterization and Result Analysis

Characteristic parameters of a NWFET are carrier mobility, sub-threshold slope, I_{ON}/I_{OFF} ratio and carrier density. Transfer curve $I_{DS} - V_{GS}$ is the starting point of this analysis. Measurement of $I_{DS} - V_{GS}$ is carried out with a testing schematic shown in figure 11.

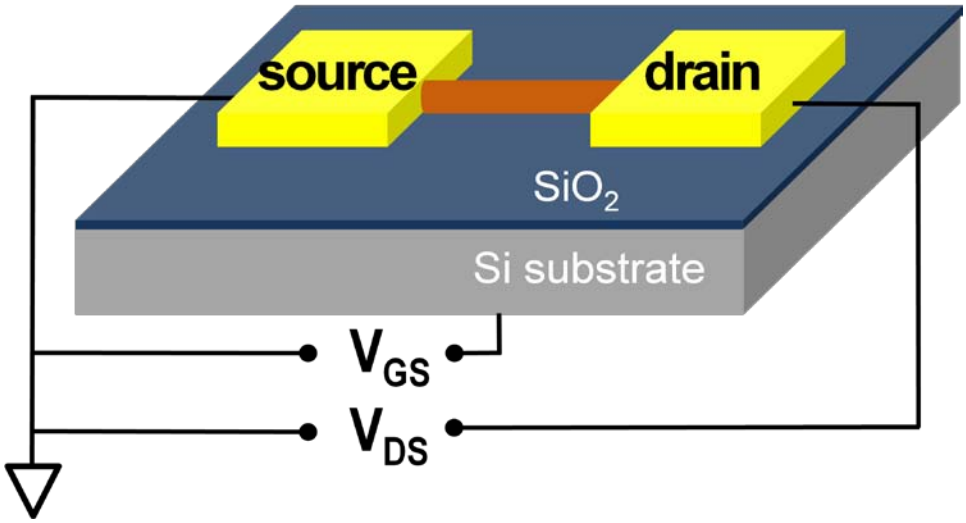


Figure 11 schematic of testing setup for NWFET

Metal-semiconductor contact plays a vital rule in the performance of NWFET and could lead to pervasive problems. In practice, naturally-grown oxide layer on the surface of semiconductor nanowire, though very thin, could insulates the metal contact from the nanowire channel, under which case, the tiny current flow is dominated by tunneling electrons though the energy barrier and the overall performance becomes completely unpredictable.

An example of NWFET with rectified current flow is shown in figure 12.

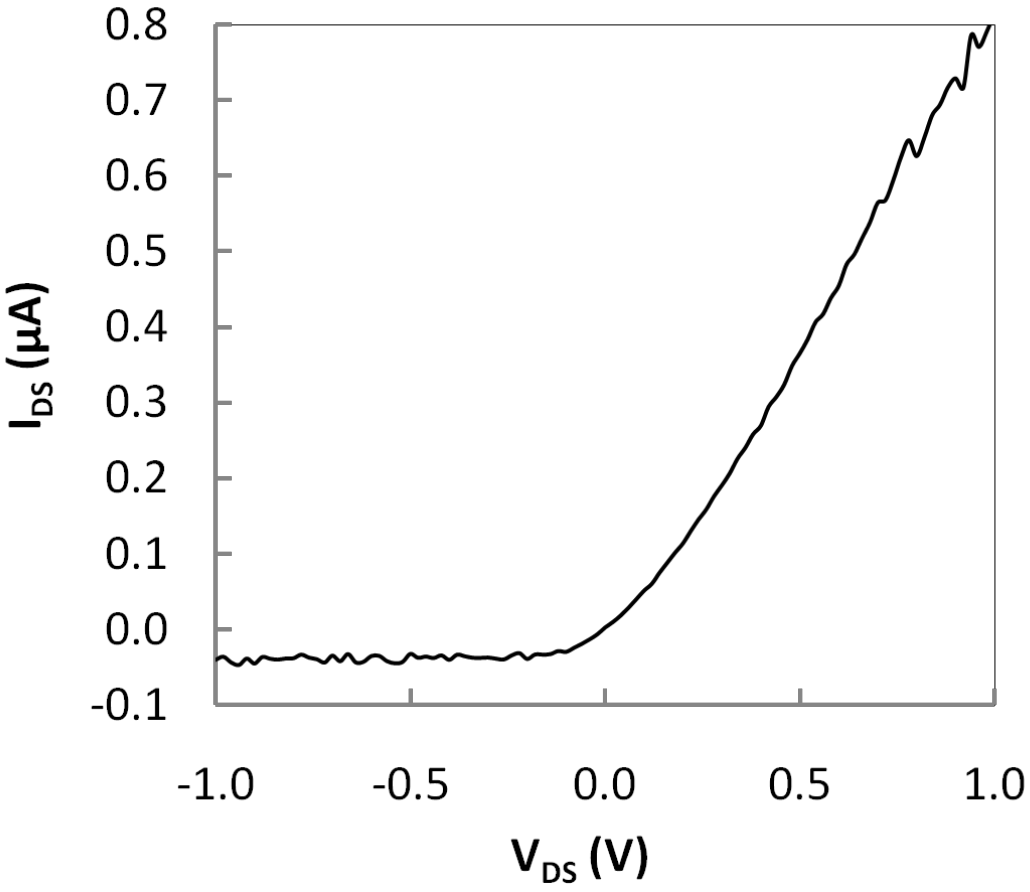


Figure 12 I-V characteristic of an NWFET without any post-lithography treatment. Diode like behavior is clearly observed as current ramps up with increasing positive supply voltage V_{DS} and clamped at a relative constant value under reverse bias.

Different models have been proposed to explain the rectifying I-V behavior [58-62] in which the contact between semiconductor nanowire and metal is modeled either as parallelly connected resistor and diode or a simple diode. Also, depending on whether rectifying effects occurs at both positive and negative supply or just one way, the NWFET is modeled to have diode on both ends or single-sided. For example, for the above observed result, to extract the barrier height and information as such, only one diode should be included in the circuit model.

To get a better understanding of electrical behavior of a metal-semiconductor contact, we need to look at bandstructure. Since the metal contact is directly deposited onto semiconductor nanowire, two types of contacts could be formed namely Ohmic contact and Schottky barrier, and it is of important to make sure that the contact is always Ohmic instead of Schottky barrier for obvious reasons: first, Schottky barrier rectifies current flow depends on the barrier height, work function and a number of parameters which results in nonlinear I-V behavior; second, Schottky barrier height is a function of temperature, which leads to temperature-dependent electrical characteristics. The formation of Schottky barrier and energy band diagram of a metal and semiconductor contact is shown below:

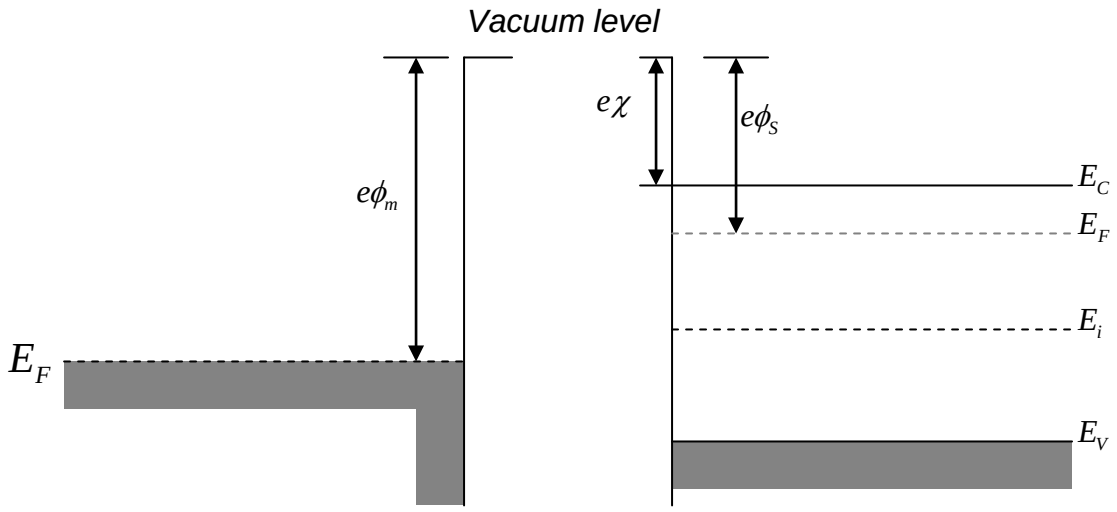


Figure 13 Energy band diagram of a metal and semiconductor before contact

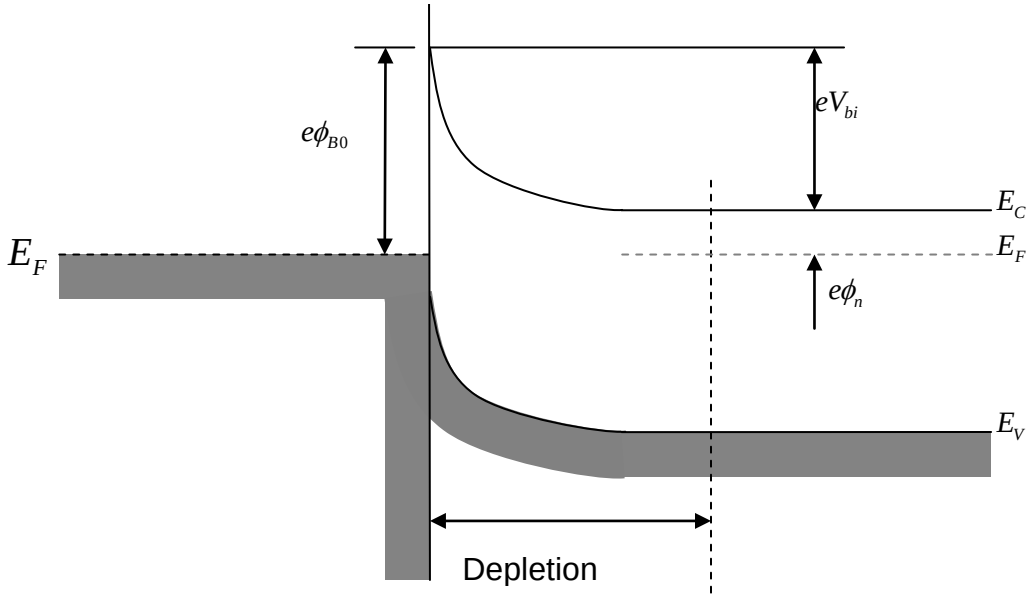


Figure 14 Ideal energy band diagram of a metal-n-semiconductor junction for $\phi_m > \phi_s$

Before contact, the Fermi energy level in the semiconductor is higher than that in the metal and when a contact is formed. Since the Fermi energy level should be constant through the system in thermal equilibrium, electrons from the semiconductor will flow to metal leaving positively charged donor atoms in the semiconductor, creating a space charge region and because of space charge region, a built-in potential barrier is formed at the interface from semiconductor side which is called Schottky barrier.

When the system is under reverse bias, the built-in potential seen by electrons in semiconductor side increases, and it is difficult for electrons to transfer to metal. When the system is under forward bias, the built-in potential decreases and electrons can easily move from semiconductor to into the metal due to the lowered barrier.

The rectifying effect of metal-semiconductor junction on current can be illustrated below:

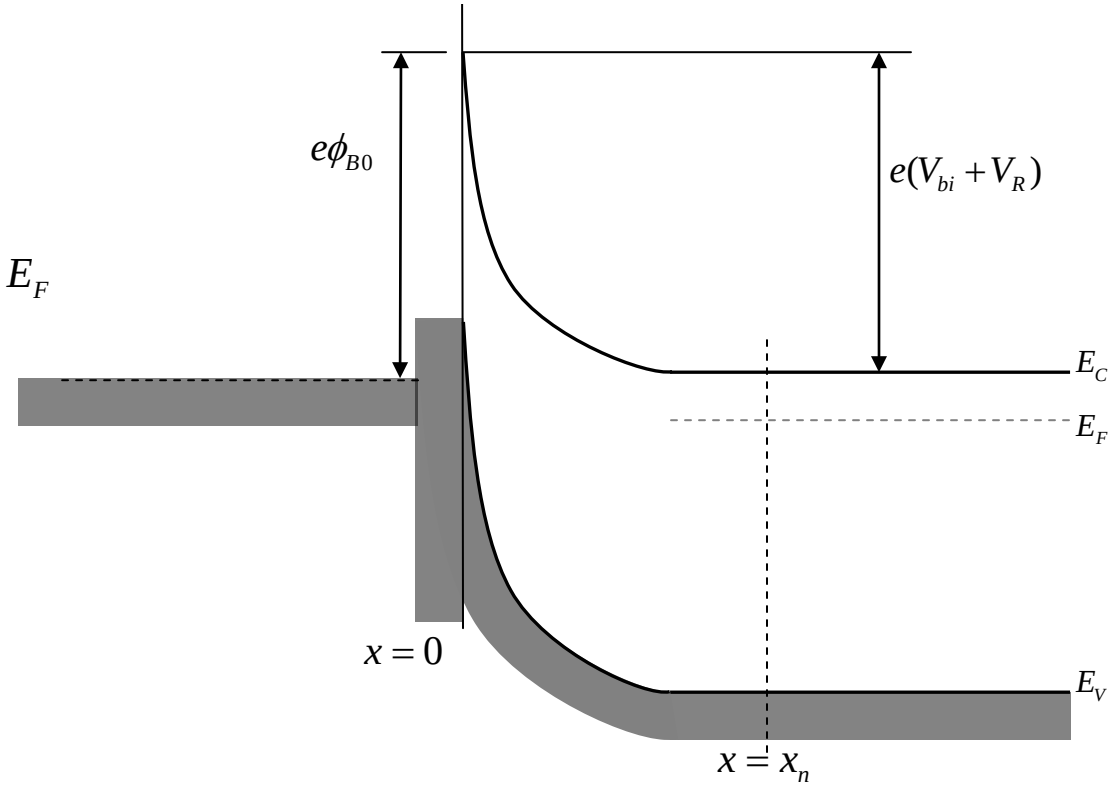


Figure 15 Metal-Semiconductor junction under reverse bias

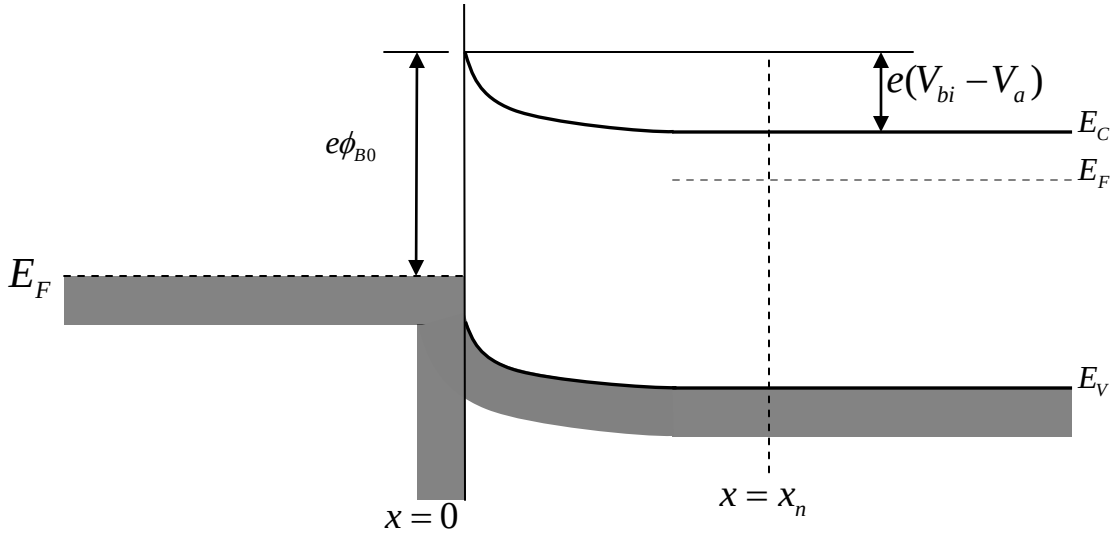


Figure 16 Metal-Semiconductor junction under forward bias.

Another important issue in the discussion of metal-semiconductor contact is surface states. State refers to energy levels that electrons or holes with a specific wave vector k could stay and are normally studied through bandstructure which is based on infinitely repeating crystal lattice structures. At the surface or metal-semiconductor interface, interface traps states exist which lead to detrimental effects of nanowire FET due to slow charging and discharging[63].

Therefore, post-lithography treatment is necessary to avoid possible formation of Schottky diode. The naturally grown oxide layer is difficult to estimate due to a large number of unknown variables such as environment temperature, material type etc. Two types of oxide removal solutions have been reported and experimented in this work: hydrofluoric acid (HF) and ammonium sulfide $(NH_4)_2S$ [64]. While HF has proved to be

effective for silicon dioxide and silicon nitride, our results showed that even buffered HF worked in a drastic manner and had a potential of damaging the nanowire material. Ammonium sulfide $(NH_4)_2S$ and ammonium polysulfide $(NH_4)_2S_X$ removes oxide layer of III-V material through a passivation process. The advantage is that it is a self-terminating process which keeps the solution from continuing etching the channel material.

The transfer curve was obtained by fixing V_{DS} at 1V and sweeping backgate voltage V_{GS}, both voltage sweeping and current monitoring functions were done by Agilent 4155. A set of samples with different channel lengths were prepared, and the results are compared so as to reach a general correlation among channel length, nanowire diameter, subthreshold slope, mobility and carrier density.

The transfer properties $I_{DS} - V_{GS}$ of all six samples are shown in figure 17.

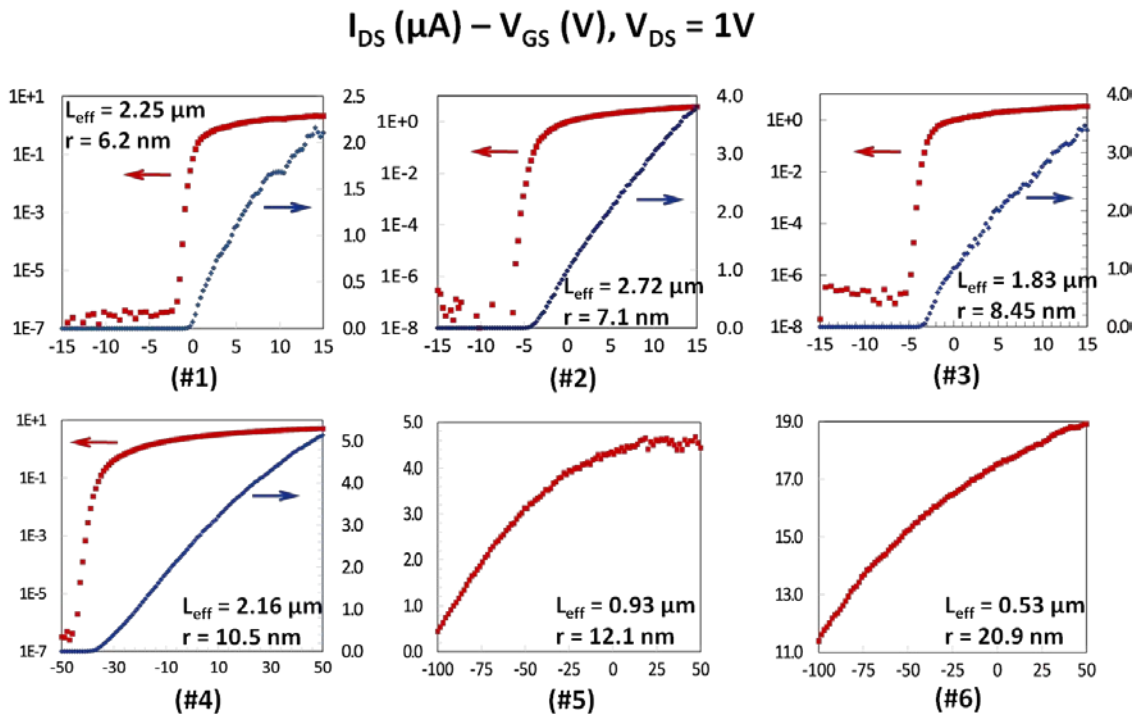


Figure 17 I_{DS} (μA) – V_{GS} (V) of six nanowire FETs. Clear ON and OFF regions were observed in first four samples in contrast to the last two samples. The ON/OFF current ratio were on the order of 10^6 averagely; the lowest inverse sub-threshold slope obtained from sample No.2 was 81.6mV which is close to the ideal value of 60mV determined "Boltzmann tyranny".

To extract the mobility of in the channel of NW, Drude model was used in which carrier mobility is expressed as

$$\mu = \frac{\partial I_{DS}}{\partial V_{GS}} \frac{L_{eff}^2}{C_{GS} V_{DS}}$$

To have a fair comparison of carrier mobilities, unified benchmarks need to be applied in terms of the value of V_{GS} where $\frac{\partial I_{DS}}{\partial V_{GS}}$ is taken, value of I_{ON} and I_{OFF}, etc. Here, we adopt benchmarks as set out by R. Chau,[65] in which maximum value of $\frac{\partial I_{DS}}{\partial V_{GS}}$ is taken as $\frac{\partial I_{DS}}{\partial V_{GS}}$ in above equation, and I_{ON}, I_{OFF} are taken when V_{GS}=V_{DS} and 0V respectively. Gate

capacitance is directly related to the calculation of carrier mobility however direct measurement of it is not easy considering the irregular shape of the gate structure. Ideally, the capacitance from an infinitely large plate to a cylinder shape object is expressed as

$$\mathrm{C} = 2\pi\varepsilon L_G / \ln\left[\left(t_{OX} + a + \sqrt{(t_{OX}+a)^2 - a^2}\right)/\mathrm{a}\right]$$

In which L_G is the gate length, ε is the insulator dielectric constant, t_{OX} is the thickness of gate insulator, and a is the nanowire radius, however, it is reported that capacitance calculated by above equation is underestimated by 10-14%[18], which means our reported carrier mobility is conservative.

The expression of carrier density is based on

$$\mathrm{R} = \frac{\mathrm{V_{DS}}}{\mathrm{I_{DS}}} = \rho\frac{\mathrm{L}}{\mathrm{S}}$$

$$\rho = \frac{1}{\sigma}$$

$$\sigma = \mathrm{nq\mu}$$

in which S is the area of the nanowire cross-section Therefore, carrier density can be expressed as

$$\mathrm{n} = \frac{I_{DS}}{V_{DS}}\frac{4}{q\mu}\frac{L_{eff}}{\pi d^2}$$

The summarized NWFET parameters and properties are as below:

	μ ($cm^2V^{-1}s^{-1}$)	n (cm^{-3})	S (mV/dec)	I_{ON}/I_{OFF}	r_{NW} (nm)	L_{eff} (um)	λ (um)	L_{eff}/λ
#1	169.92	$1.36\cdot10^{19}$	92	$1.3\cdot10^{6}$	6.20	2.25	0.124	13.4
#2	114.40	$1.29\cdot10^{19}$	192	$2.7\cdot10^{6}$	7.10	1.72	0.133	13.0
#3	169.28	$5.13\cdot10^{18}$	81.6	$3.5\cdot10^{6}$	8.45	1.83	0.145	12.6
#4	62.90	$1.71\cdot10^{19}$	336	$4.6\cdot10^{6}$	10.50	2.16	0.162	18.1
#5	27.23	$2.06\cdot10^{19}$			12.10	0.94	0.174	5.4
#6	15.15	$2.15\cdot10^{19}$			20.90	0.53	0.228	2.3

Table 2 Summarized characteristics of six InSb NWFET samples including electron mobility, electron density, inverse sub-threshold slope, I_{ON}/I_{OFF} ratio, nanowire radius, effective channel length, screening length, ratio of channel length over screening length.

Inverse subthreshold slope S is defined as

$$S = \ln(10)\left(\frac{\partial I_{DS}}{\partial V_{GS}}\frac{1}{I_{DS}}\right)^{-1}$$

Inverse subthreshold slope is used to describe the transition property of a transistor. At subthreshold region, electron follows Boltzmann distribution and current through the channel is proportional to $\exp\left(\frac{qV_G}{k_BT}\right)$ where k_B is Boltzmann constant and T is temperature. Simple algebra could show that

$$\frac{I_2}{I_1} = e^{\frac{q\Delta V_G}{k_BT}}$$

Therefore, V_G must change by $\frac{K_BT}{q}\ln10=60mV$ to have current changed by a factor of ten. This value 60mV per decade provides a limit of subthreshold slope, therefore, by comparing inverse subthreshold slope S to this value, we could get a sense of how close the transition property of NWFET is to ideal case. The importance of a large sub-threshold slope is three folded: first, it increases the device speed by reducing the threshold voltage; secondly, it increases the dynamic range of a device by allowing

smaller minimum operation gate voltage; lastly, it reduces the switching energy by reducing required supply voltage.

Based on the calculated inverse subthreshold slope, the best value we have obtained is about 3 to 4 times larger than the ideal limit, which is better comparing to conventional CMOS FET devices. The superior performance comes from the intrinsic cylindrical half-wrap-around shape of the gate dielectric structure of NWFET.

A comparison of the calculated carrier mobility with other materials is shown in table 3 as below:

	Carrier type	Mobility ($cm^2V^{-1}s^{-1}$)	N ($cm^{-3)}$	I_{ON}/I_{OFF}
Si[11]	Hole	560	-	10^4
Ge[13]	Hole	600	$3\cdot10^{18}$	10^3
ZnO[66]	Electron	~3	$5\cdot10^{17}$	125
InAs[18]	Electron	~6200	$10^{17} – 10^{18}$	2 - 100
InSb	Electron	~43	$\sim3\cdot10^{19}$	$\sim3\cdot10^6$
GaN[23]	Electron	650	$10^{18} – 10^{19}$	-

Table 3 Carrier mobility, density, I_{ON}/I_{OFF} current ratios in NWFETs.

Interestingly enough, although a high I_{ON}/I_{OFF} current ratio is achieved, the carrier mobility is orders of magnitude lower than that in bulk form, and carrier density is the highest among a variety of NWFETs. To understand the mechanism from solid state perspective, we turn to band structure of InSb is as shown in figure 18.

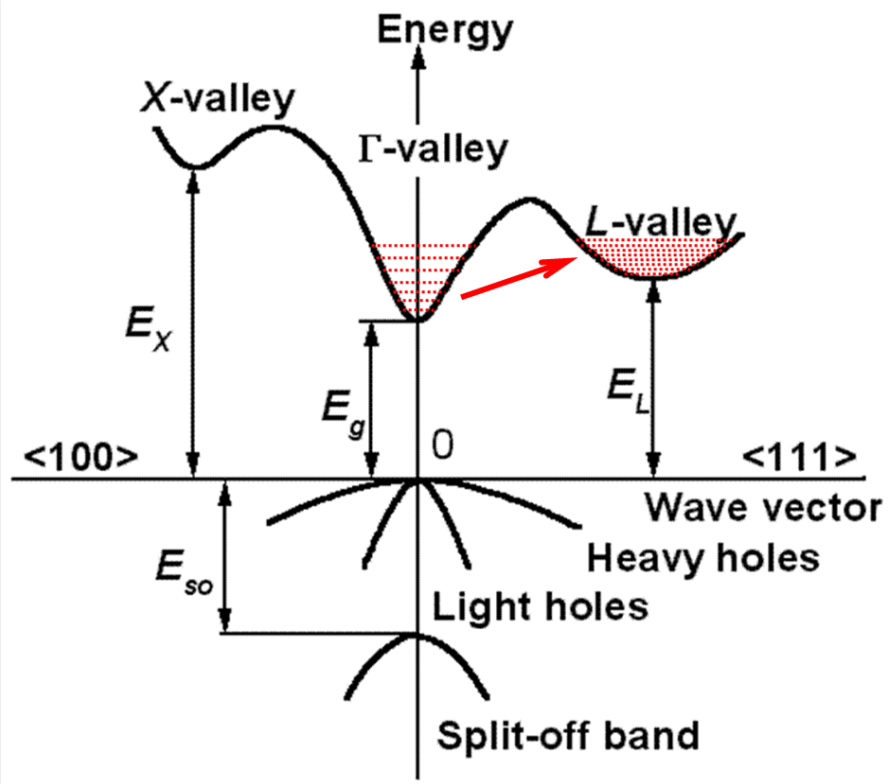


Figure 18 Band structure and effective electron mass of InSb. The small effective mass at Γ valley leads to small density of state (DOS) and highly discrete energy levels, as a result, electrons are popped to L-valley under strong electric field. The effective mass at L-valley however, is almost two orders of magnitude as high as that in Γ valley, which means the majority of electrons are with a high effective mass, therefore, lower the overall carrier mobility.

		Effective mass: m*
InSb	Γ	$0.014m_e$
	L_4	$1.261\ m_e$
	X_1	$0.175\ m_e$
	X_2	$0.440\ m_e$

Table 4 InSb electron effective mass at different critical point in the band structures, X_1 and X_2 refer to two degree of degeneracy. m_e is the mass of electron. One observation is that effective mass at L valley is orders of magnitude higher than that in Γ valley, which is a major reason for the measured mobility.

InSb is direct bandgap material with an extremely small bandgap of 0.17eV, the high carrier mobility comes from its low effective mass in the Γ valley based on equation

$$\mu = \frac{e\tau}{m^*}$$

However, the density of state in 1-D case is expressed as

$$\rho_{DOS}^{1D}(E) = \frac{1}{\pi\hbar}\sqrt{\frac{m^*}{2(E - E_0)}}$$

in which E_0 is the minimum energy in the conduction band.

Despite high carrier mobility at Γ valley, the density of state at Γ valley is low, and quantized energy levels rise up rapidly, both of which come from small effect mass m* that reduces the inversion charge at Γ valley and moves most carriers to the heavy L valley, and hence reduces the drive current. [67] From electrical characterization perspective, it is impossible to decouple the current contributed from carriers at Γ valley from that at L valley. Therefore, the overall current is compromised by majority carriers that stay at L valley.

Also noticed from figure 17 is that all devices have distinct ON and OFF states except device No. 5 and No. 6. Scale analysis is used to account for the disparities. Intuitively, a long nanowire channel is less vulnerable to drain induced barrier lowering (DIBL) effect since the tail of potential barrier does extend to drain region. As mentioned in section 2.1, screening length provides a good measure of how effective gate voltage modulates surface potential in the channel[68] and further the current conduction in the NWFET.

Therefore, comparison is made between effective gate length and screening length as in table 5, the result confirms with the theory: devices No. 1 to No.4 are with larger L_{eff}/λ and are easier to be switched ON or OFF, devices No.5 and No.6 on the other hand, have a relatively smaller L_{eff}/λ therefore no clear distinctions between ON and OFF states were found. Scale analysis reveals that in CVD NWFET systems, if L_{eff}/λ is larger than 12, a good gate control can be guaranteed and if L_{eff}/λ is smaller than 5, no distinct ON/OFF region can be found; for devices with L_{eff}/λ between 5 and 12, more experiments are needed.

	I_{ON}/I_{OFF}	r_{NW} (nm)	L_{eff} (um)	λ (um)	L_{eff}/λ
#1	$1.3 \cdot 10^6$	6.20	2.25	0.124	13.4
#2	$2.7 \cdot 10^6$	7.10	1.72	0.133	13.0
#3	$3.5 \cdot 10^6$	8.45	1.83	0.145	12.6
#4	$4.6 \cdot 10^6$	10.50	2.16	0.162	18.1
#5		12.10	0.94	0.174	5.4
#6		20.90	0.53	0.228	2.3

Table 5 I_{ON}/I_{OFF} ratio, Screening length and effective channel length in all NWFETs.

Also, all NWFETs demonstrated strong n-type polarity as against commonly observed ambipolar conduction type, the reason for it is unclear at this moment and further analysis is needed.

2.2.4 Conclusion

InSb nanowire based on chemical vapor deposition (CVD) process was synthesized through a vapor-liquid-solid (VLS) mechanism. The crystalline nature of synthesized nanowires was confirmed by HRTEM and SAD pattern. The carrier mobility was

calculated by Drude model and lower-than-expected carrier mobility was explained based on the bandstructure, in which low density of state at Γ valley (low effective mass, high mobility) and high density of state at L valley (high effective mass and low mobility) combined to lead to the overall lower carrier mobility. The high I_{ON}/I_{OFF} current ratio, low OFF state current indicated lower leakage current, manifesting the advantage of Ω - shape gate control, and even better gate control thus can be expected from wrap-around-gate NWFETs, making NWFETs a potential candidate for low power digital devices. The close to ideal inverse subthreshold slope allows for larger dynamic range of input signal at gate which also indicates the efficient gate control. Short channel effect (drain induced barrier lowering) is studied and a comparison between screening length and channel length in all samples are made which are in accordance with the generalized physical meaning of screening length.

2.3 Electrochemistry based NWFET

2.3.1 Introduction

Electrochemistry is the study of reactions in which charged particles (ions or electrons) cross the interface between two phases of matter, typically a metallic phase (the electrode) and a conductive solution (the electrolyte). Electrochemistry process produces an unbalance in the electric charges of the electrode and the solution, and much of the importance of electrochemistry lies in how these potential differences can be related to the thermodynamics and kinetics of electrode reactions.

Electrodeposition (or equivalently electroplating) is the process of producing a layer of metal or metal oxides on a surface by the action of electric current. The coating is usually conducted by introducing negative charges onto the object to be coated and immersing the object into a solution which contains a salt of the metal to be deposited. The metallic ions of salt carry positive charges and are reduce to metallic form when they reach the negatively charged object.

The thickness of the electrodeposited layer is determined by the time of plating, therefore, the longer the object is placed in the operating plating bath, the thicker resulted electroplated layer will be.

The use of electrochemistry for synthesizing nanowire was accomplished with the assist of template film and had drawn great research attentions [69-80] due to the obvious advantages: firstly, it is simple comparing to chemical vapor deposition based method in that requirements such as high temperature, specific gas flow are not required. Secondly, it is of low cost, the experiment setup contains a cell, a potentialstat, electrodes and target chemical solutions. Lastly it allows for better process controls in that nanowire diameter is directly controlled by the pore size of the template, and nanowire length is capped by the thickness of the template. Routkevitch D. et al were the first to develop this method[71] in which anodic aluminum oxide (AAO) film was used as a template in which the deposition of semiconductor nanowire was restricted to the direction that was

normal to the substrate. The significance of this work was that the developed technique was generalizable as a means of fabricating nanowire of a wide range of semiconductors.

2.3.2 Synthesis and Characterization of Electrochemistry based InSb Nanowire

A schematic of the synthesis method is shown in figure 19.

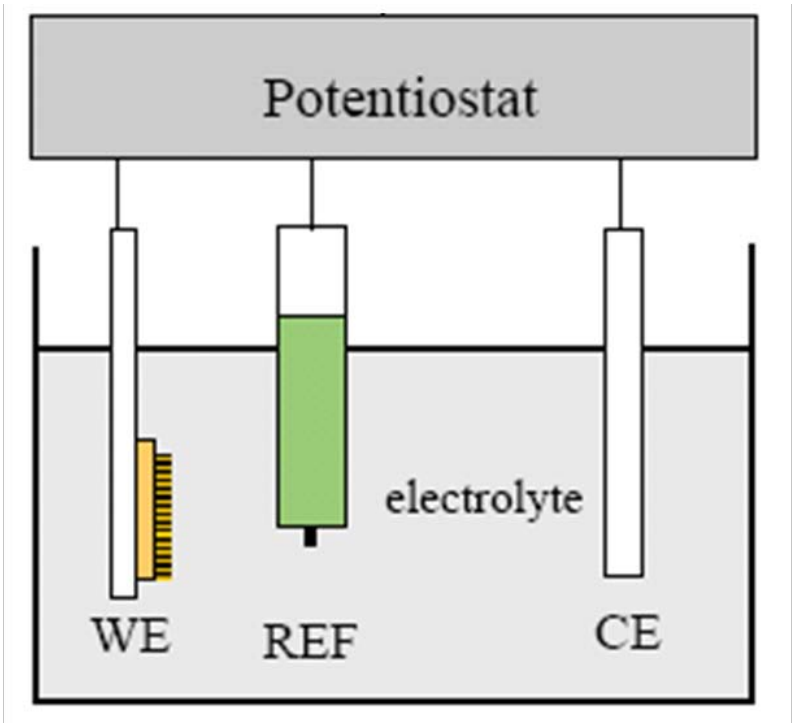


Figure 19 Schematic of electrochemistry based nanowire synthesis system.

The potentiostat has three outputs: working electrode, reference electrode and counter electrode. The growth process is controlled completely by computer through Potentiostat and the output voltage is applied between working electrode and reference electrode.

A brief synthesis process is as follow:

(1). Preparation of template. Anodic aluminum oxide (AAO) template (from Whatman) is used as the synthesis platform, and comes in three types with different pore diameters. Shown in figure 20 is a cross section view of the template.

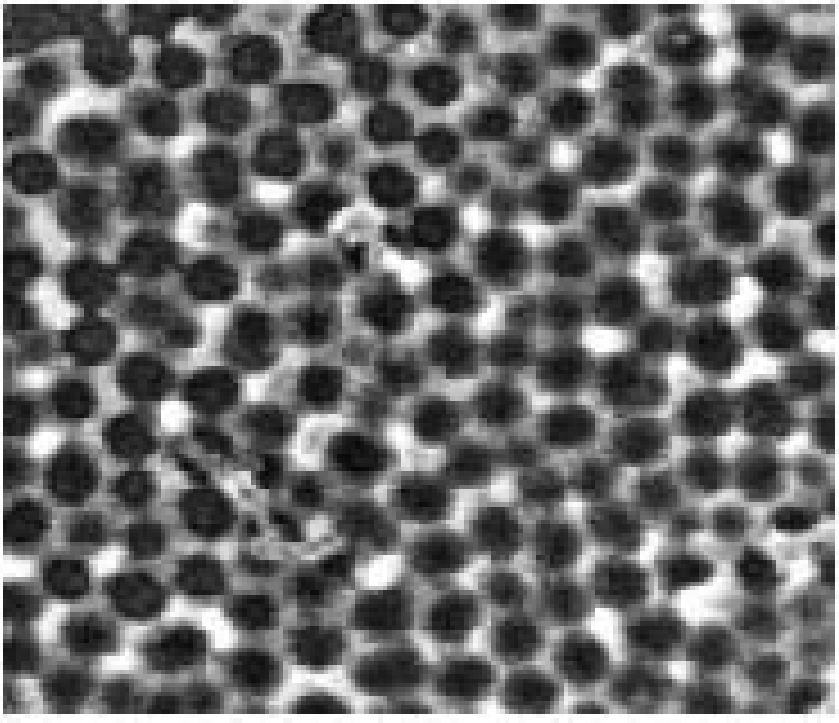


Figure 20 Cross-section view of AAO membrane.

(2). The AAO membrane is then coated on one side with copper film by sputtering for 5 min. The other side of the copper film is coated with nonconductive paste to make sure the only exposed areas of the working electrode are inside the pore so that nanowires can grow inside the template.

(3). DC voltage is then applied to working electrode and desired material in solution form is then deposited onto the working electrode through electrochemical reaction, which results in growth of nanowires inside the pores as schematically shown in figure 21:

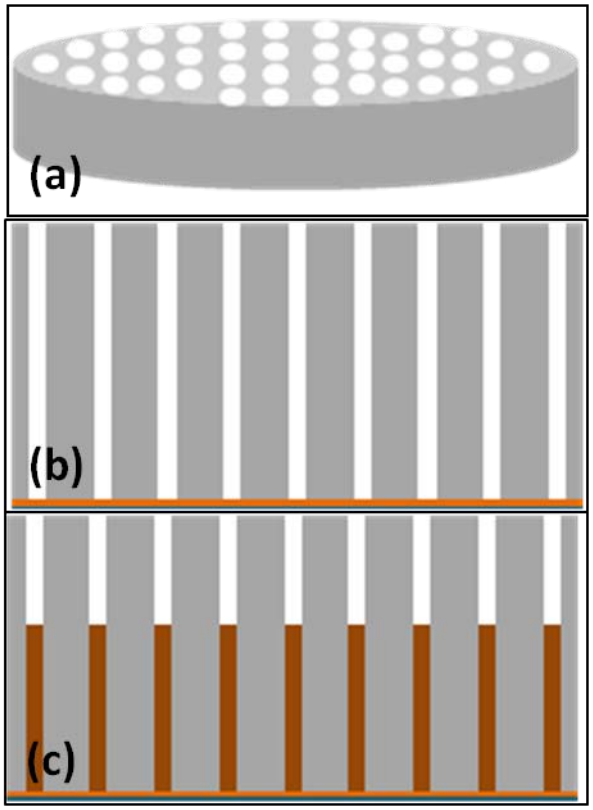


Figure 21 Schematic description of the electrochemistry based synthesis. (a) Electrochemistry process starts with bare anodic aluminum oxide (AAO) membrane with pore size selectable among 50nm, 75nm and 200nm. The thickness of the membrane is around 10um which sets the maximum length of the nanowires. (b) Cross-section view of the AAO membrane after depositing of a layer of serving as working electrode which is then covered by another layer of nonconductive paste to expose working electrode exclusively to the pores inside the membrane. (c) Cross-section view of nanowire growing inside the pore under applied voltage at the working electrode.

(4). Nanowires are obtained after dissolving the template and the backside copper cover, and these nanowires are suspended in solution and it takes three to four times centrifuge to remove the impurities.

SEM pictures of nanowires are shown in figure 22. The advantage of electrochemistry based synthesis method is demonstrated by orderly bundled uniform nanowires.

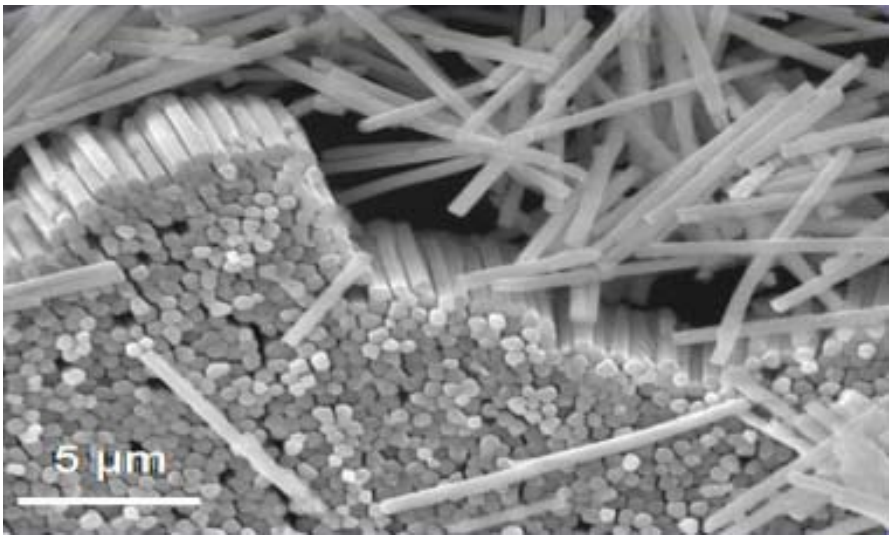


Figure 22 Electrochemistry based InSb Nanowires.

Electrochemistry based synthesis appears to be a pure deposition process with which the crystallinity of nanowire has been in question, however, it is discovered that under certain circumstances, single crystal nanowires can be obtained. There are several major techniques to confirm the crystallinity as well as crystal structures. Transmission electron microscope (TEM) is a widely used one, in which a thin piece of target material is used as specimen and collimated high energy electrons passes through the sample to generate sample images, on the contrary to SEM in which reflected electrons are used to image a sample. Because of this, TEM can be used to reveal crystal lattice directly; a high resolution TEM image of InSb nanowire is shown in figure 23.

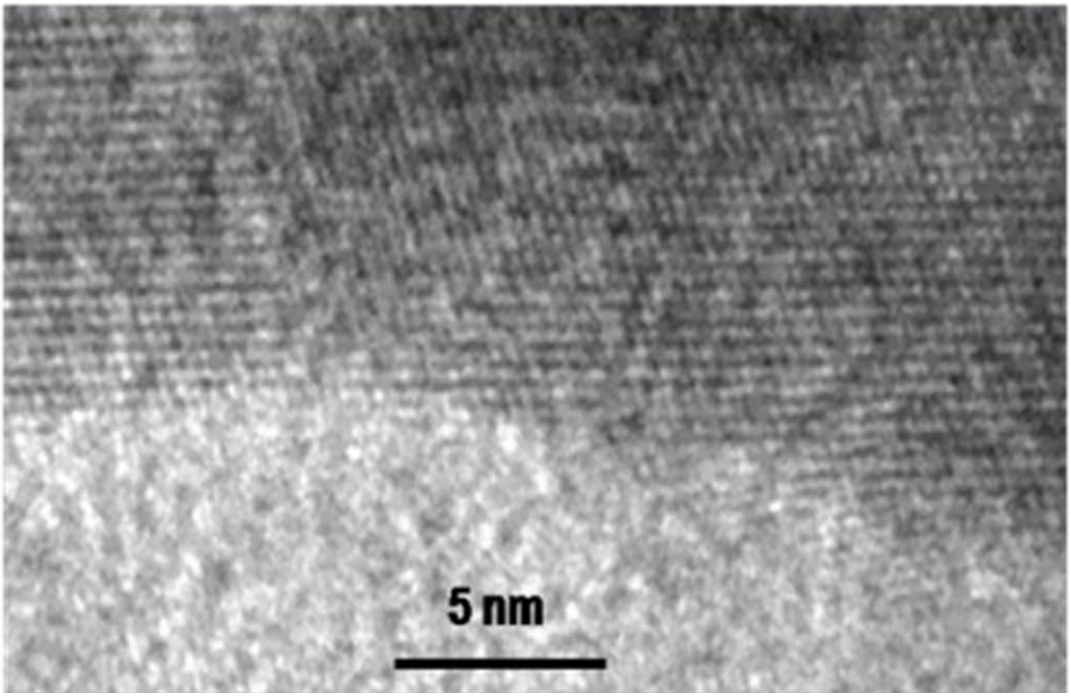


Figure 23 High resolution transmission electron microscopy (HRTEM) image of synthesized nanowire. The crystallinity is confirmed by the periodically arrayed atoms. The brighter clustered area refers to the native oxide grown spontaneously on the surface of the nanowire.

The periodically arrayed bright dots are InSb crystal lattice from which lattice constant can be calculated. The relatively blurry area refers to the oxide layer formed on the surface of nanowire. While TEM images do confirm crystallinity of certain regions of the nanowire, the whole nanowire cannot be guaranteed to be single crystal due to the randomness nature of the synthesis technique and the inevitable impurities generated during the process, these difficulties add up uncertainties in the extracted parameters of nanowire based electronics. We speculate a large percentage of the synthesized nanowire is polycrystal, if not single crystal in which case the material is composed of different crystallite with varying sizes and orientations. The disadvantages of polycrystal material

originate from the grain boundaries at the interface of different crystal segments when it comes to conductivity of polycrystal material. Due to the sudden change of crystal lattice in terms of lattice orientation and lattice constant, the flow of charged carriers under applied voltage experience scattering caused by the grain boundaries, which reduces carrier mobility, therefore the measured mobility could provide a lower bound of mobility in InSb nanowire.

Another technique to check the crystallinity is using selected area diffraction (SAD) pattern. SAD is a technique also based on transmission electron microscope (TEM). To get image under TEM, a thin piece of sample is required which is often prepared by mechanical milling using focused ion beam. The sample is then subjected to high energy electron beams inside TEM chamber. Since electron beams have wave-particle duality, a wavelength can be defined to a beam of electrons based on equation

$$\lambda = \frac{h}{P}$$

in which λ is the wavelength of electrons, P is electron momentum, and h is Planck constant. The applied voltage is high so that electrons are also of high energy and high momentum, and as a result extremely small wavelength. The wavelength of electron beam is comparable to the lattice constant so that targeted material works as diffraction gating to the electrons.

In selected area diffraction, a diffraction pattern is obtained under electron illumination. An aperture in the image plane is used to select the diffracted region of the sample, and

SAD pattern is a projection of the reciprocal lattice, with lattice reflections showing sharp diffraction spots. The pattern of spots reveals the crystallinity of the selected area of material and there are mainly three different types of SAD patterns: (a) ring patterns, (b) spot patterns and (c) Kikuchi patterns.

Ring patterns reflect grains of polycrystalline materials and consist of a strong directly transmitted spot and rings of diffracted intensity. For a given beam direction particles with spacing of d that satisfies Bragg's law will be oriented randomly and produce cones of intensities in reciprocal space. An example of SAD pattern of polycrystalline material is shown below:

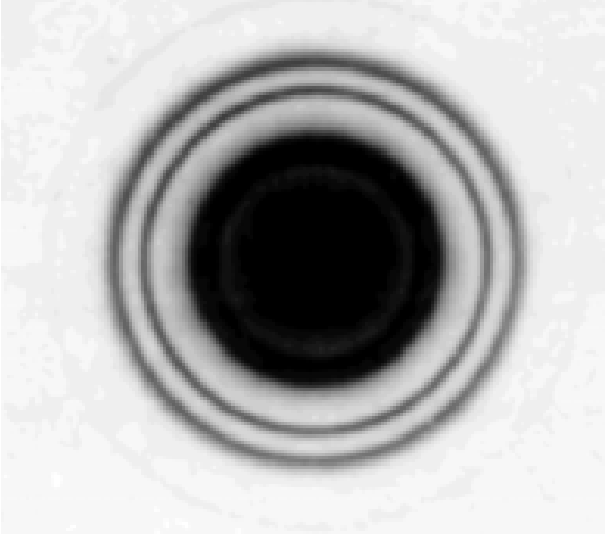


Figure 24 SAD pattern corresponds to polycrystalline material

Spot patterns correspond to magnified images of planar sections through the reciprocal lattice normal to the incident beam direction and consist of regular two dimensional

arrays of regularly situated spots related by two common vectors of translation. A sample spot pattern is shown below:

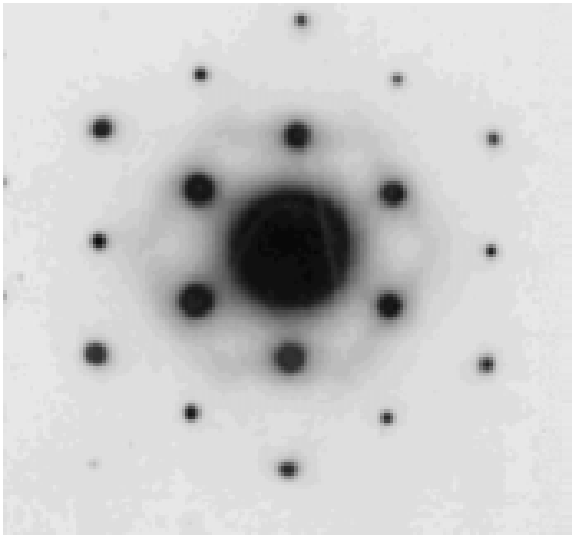


Figure 25 Spot SAD pattern indicates single crystallinity and reveals general indices of the spot.

Kikuchi patterns occurs in single crystal regions which are sufficiently thick and have low bright and dark lines separated by a distance proportional to the spacing of the planes.

The SAD image of synthesized InSb nanowire is shown below:

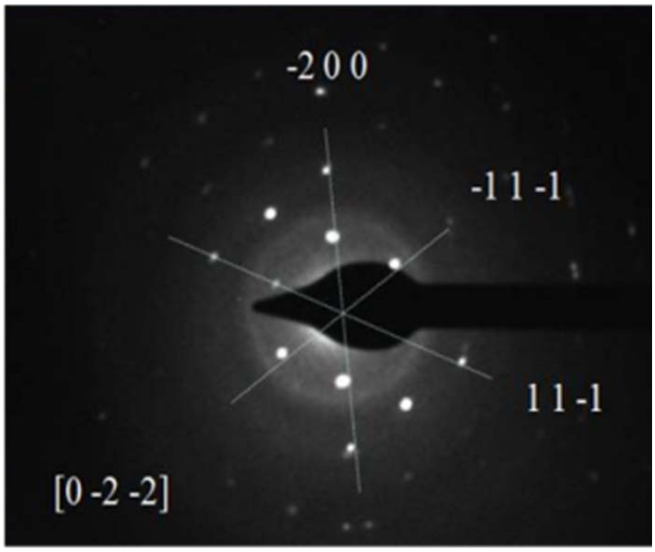


Figure 26 SAD pattern of synthesized InSb nanowire with spot pattern indicating single crystallinity

To further check the crystallographic structure of synthesized InSb nanowire, X-ray diffraction (XRD) is used. XRD is a powerful and widely used technique that is capable of measuring the average spacing between layers or rows of atoms; determining the orientation of a single crystal or grain; finding the crystal structure of an unknown material and measuring the size, shape and internal stress of small crystalline regions.

The mechanism of XRD is based on Bragg's law which is simply put as

$$n\lambda = 2dsin\theta$$

in which n is an integer, λ is the wavelength of the incident X-ray, d is the distance between atomic layers in a specific direction, and θ is the angle of incident X-ray beam. X-ray wave interference is direct evidence for the periodic atomic structure of crystals postulated for centuries.

Bragg's law can be derived as illustrated below:

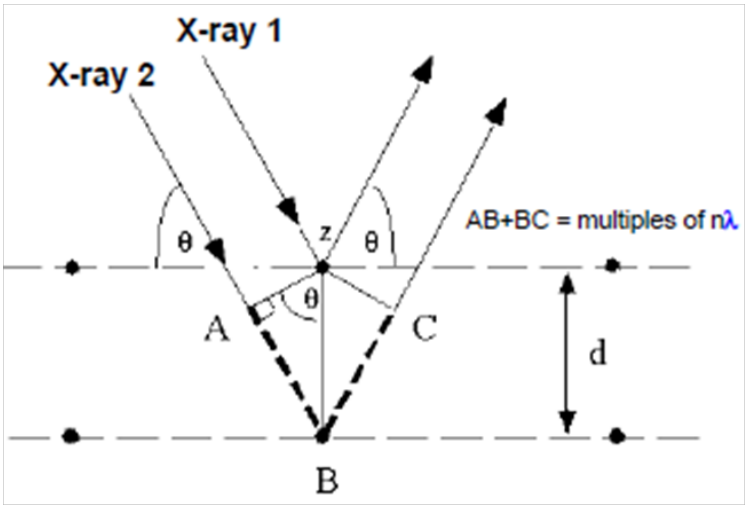


Figure 27 Schematic illustration of Bragg's Law

As can be seen from the schematic, incident X-rays have constructive interference only when the extra distance X-ray2 traveled through is integer times of the wavelength, that is, $n\lambda = AB + BC$ and $AB = BC = d\sin\theta$, and therefore, when coming out of the crystal, both rays are of the same phase when the condition $n\lambda = 2d\sin\theta$ is satisfied. When X rays strike a crystal and diffracts into many specific directions, angles and intensities of these diffracted beams can be observed, from which the arrangement of atoms within a crystal can be extracted.

The XRD system used in the experiment is Bruker AXS system, nanowire in solution form are first mixed with acetone, and painted onto the platinum stage for measurement. During the measurement the X-Ray source tube and the detector both move up on an arc such that they are both at the same angle with respect to the sample.

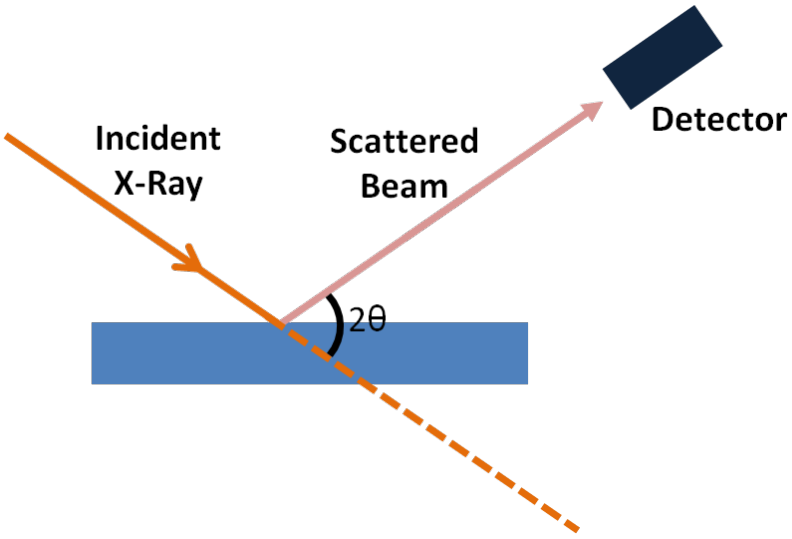


Figure 28 Schematic of XRD measurement setup

The diffraction peaks are signatures of different material structures that can be identified by checking the similarity between these signatures and the XRD diffraction database. The crystallinity regions give sharp narrow diffraction peaks and the amorphous component gives a very broad peak. The ratio between these intensities can be used to calculate the level of crystallinity in the material. The obtained XRD pattern is shown in figure below:

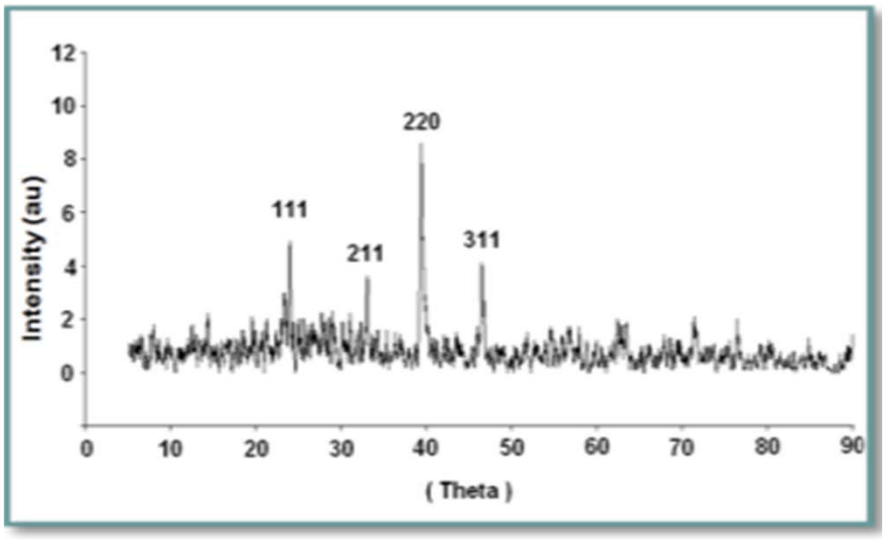


Figure 29 XRD signature of synthesized InSb nanowires, sharp peaks are observed which are the indication of a high level crystallinity in the specimen.

2.3.3 Fabrication of top-Gated NWFET

The next step is to make NWFET. The procedures are the same as for CVD nanowires except that top gate is also made this time to allow for another degree of control over the carrier conduction in the channel. Atomic layer deposition (ALD) used to grow the top gate dielectric material. ALD is a thin film deposition technique that is similar to CVD process, the operation of ALD is based on four consecutive steps that works in a repeating manner: (1). Exposure of the first precursor. (2) Purge the reaction chamber to remove the non-reacted precursors and gaseous reaction by-product. (3) Exposure of the second precursor or another treatment to activate the surface again for the reaction of the first precursor. (4) Purge the reaction chamber.

ALD system has a several advantages over CVD process: (1) the thickness of deposited dielectric material can be precisely, almost “digitally”, controlled at atomic level; (2) self-limiting deposition process results in excellent uniformity over the entire substrate area. (3) Low defect, pinhole density and low deposition temperature. The shortcoming of ALD process is that it’s a slow process; however, for use in microelectronics area, top gate dielectric usually is very thin, normally under 20 nanometers therefore, the slowness does not appear to be a contingent problem in our case.

A second time ebeam lithography is used to place another layer of metal contact just onto the gate. The fabricated NWFET is shown in figure 30.

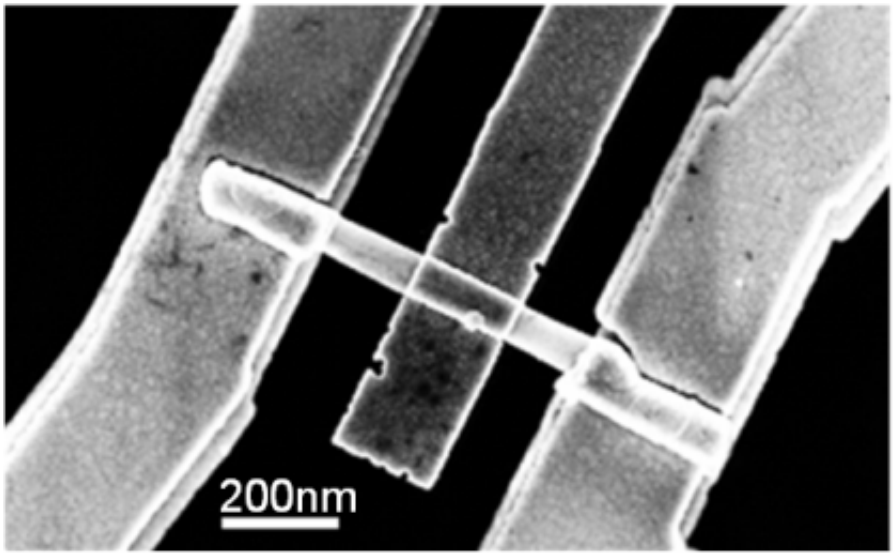


Figure 30 InSb NWFET with top gate.

Gate dielectric materials are chosen based on several factors: (1) it should have as large a dielectric constant as possible. Since gate capacitance can be expressed as

$$C = \varepsilon_r \varepsilon_0 \frac{S}{t_{OX}}$$

in which ε_r is the relative dielectric constant, ε_0 is the dielectric constant of free space, S is the gate area and t_{OX} is the thickness of gate oxide, therefore, larger dielectric constant can give a high gate capacitance with a thick gate material (so that gate dielectric is less vulnerable to electric breakdown) (2) gate material should be epitaxially-compatible with channel material such as silicon dioxide grown from silicon etc. (3) gate material should allow minimum leakage current through the gate.

Although dielectric constants of most high-K materials are available, it varied with process. To obtain precisely the dielectric constant of Hafnium dioxide, we made Metal Semiconductor Oxide (MOS) capacitors with the same process as used in making NWFET top gate.

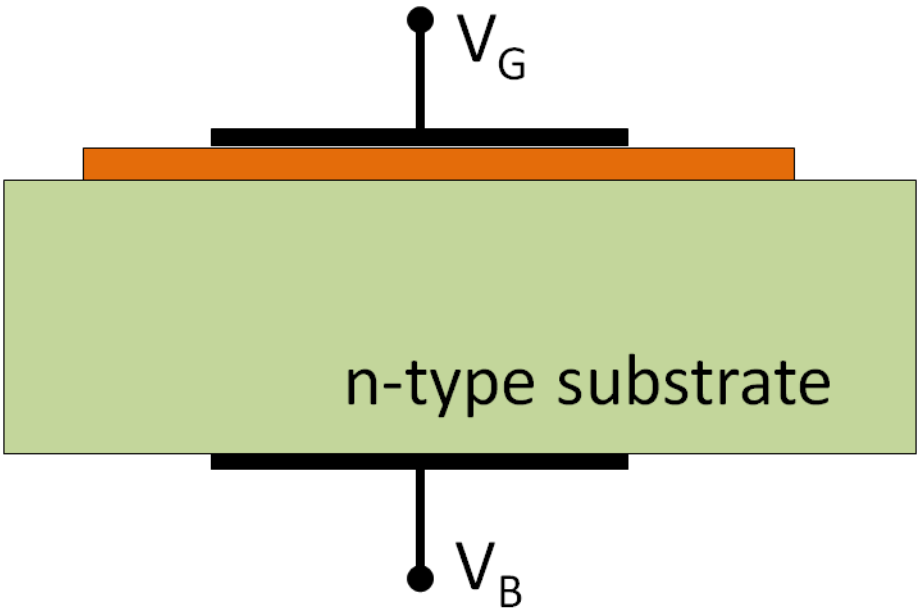


Figure 31 Schematic of Metal Oxide Semiconductor (MOS) capacitor.

Silicon wafer with degenerately doped n-type substrate was firstly etched by HF to remove the surface oxide layer, an estimation of surface oxide thickness is necessary to avoid excessive etching. Etching rate with diluted HF (1 part HF in 6 part H_2O) is roughly 100nm/min. One easy yet useful way to check whether surface (as well as backside) oxide layer is fully etched is to check whether the surface has turned from hydrophilic to hydrophobic: oxide layer results in hydrophilic surface while pure silicon surface is hydrophobic in which case water droplets have ball shapes. Right after surface oxide layer was etched away, atomic layer deposition process is applied to grow hafnium dioxide layer with a thickness of 20nm. The per-step-thickness is carefully measured previously by atomic force microscopy (AFM) so that total gate thickness is guaranteed. MOS capacitors are made in round shape in the same manner by e-beam lithography. The

diameter is set to be 120 micrometers so that no bonding pad is necessary. A Ti/Au layer of 10nm/80nm was used as surface contact. To improve the substrate conductivity, we rubbed the backside of silicon wafer with cotton stick soaked with buffered HF solution to remove the native oxide layer which seemed to have improved the contact.

MOS capacitor as shown in the figure above is a “sandwiched” structure, unlike regular double plate capacitor in which dielectric material is placed between two metal plates, in MOS capacitor, doped silicon substrate works as one metal plate. Therefore, it has unique C-V characteristics.

Depending on the gate to substrate voltage, operation of MOS capacitor can be categorized into three operation modes: accumulation, depletion and inversion. Two critical points define the three modes: flat band voltage and threshold voltage. Flat band voltage is defined as the applied gate voltage when applied to the gate electrode yields a flat energy band in the semiconductor. Accumulation happens when applied voltage is smaller than flat band voltage and electrons on the gate appeals to the holes from the substrate to the gate-semiconductor interface. When applied voltage is higher than flat band voltage, negative charges builds up in the semiconductor, which is initially due to the depletion of the semiconductor starting from the gate semiconductor interface, another way to understand this is that applied voltage expels charges from the semiconductor right under the gate, when charges are evacuated, the semiconductor is depleted of charges. When the voltage across the semiconductor increases to above twice

the bulk potential, negatives charges appears at the gate-semiconductor interface which forms inversion layer. The reason for this name is that the polarity of the charges in the inversion mode is directly opposite to that in accumulation mode and further increase in the gate voltage will barely increases the width of depletion layer however will incur exponential increase in the amount of charges.

Two types of capacitance measurements are normally considered for MOS structure: high frequency measurement and low frequency measurement. The main difference between the two types of measurements is that under high frequency signal, charge in the inversion layer does not vary from the equilibrium value with applied AC signal; therefore, the high frequency capacitance reflects only the charge variation in the depletion layer.

The measured capacitance - voltage relationship is shown in figure below:

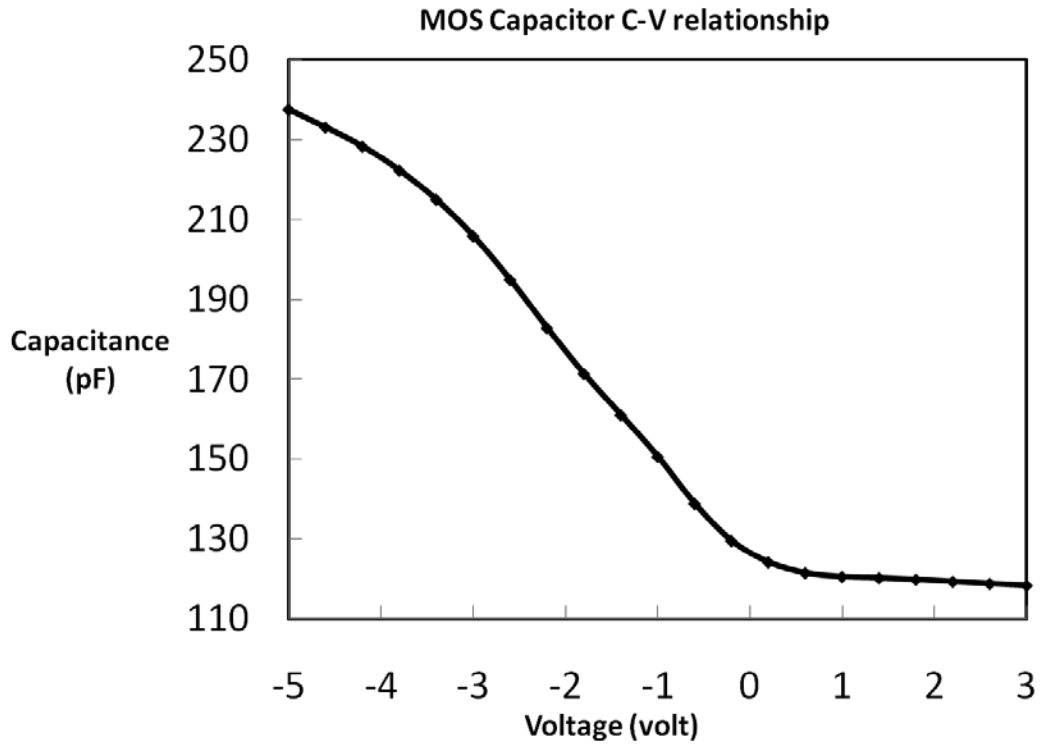


Figure 32 Capacitance – Voltage relationship of MOS capacitor at testing frequency of 1MHz.

The measurement is carried out with AC signal at 1 MHz and therefore capacitance decreases as bias voltage increases, the reason for this is that with high frequency signal, MOS capacitor is not under equilibrium as electrons do not have sufficient time to respond and therefore the inversion layer is not formed. At high bias voltage, the capacitance is relatively stable which reflects the capacitance in deep depletion and can be used for calculation of gate dielectric constant.

Below are equations used for calculating gate dielectric constant:

$$C = \varepsilon \frac{A}{t_{OX}}$$

$$\varepsilon = \varepsilon_0 \varepsilon_r$$

$$A = \frac{1}{4}\pi d^2$$

And the calculated gate dielectric constant of Hafnium dioxide is

$$\varepsilon_r = 24.99$$

Leakage current is a nuisance for nanowire FET because it causes static power dissipation and a number of detrimental effects and therefore should be reduced to its minimum. Although most gate dielectric materials are considered to be insulator in the first place, they inevitably have dissipative component. To accurately extract parameters such as carrier mobility and carrier density, it is therefore important to determine the dissipative factor of the gate dielectric.

When gate dielectric is dissipative, it can be modeled as parallelly connected capacitor and resistor as in figure below, in which the resistor accounts for its dissipative characteristics.

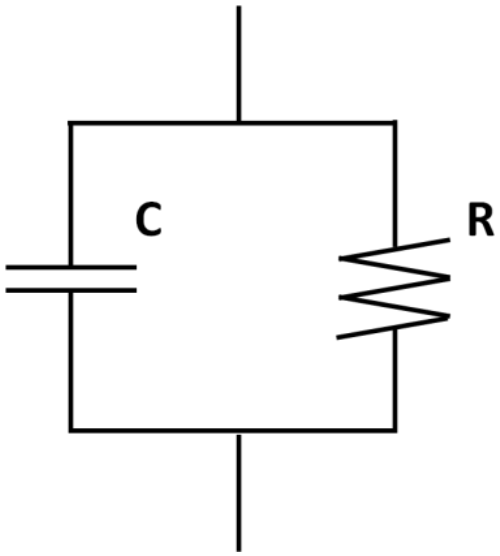


Figure 33 Gate dielectric can be modeled as parallelly-connected capacitor and resistor in which the resistor represents the minor dissipative component and the capacitor reflects the major capacitive component.

The measurement of gate capacitance is carried out through Agilent 4284 LCR meter, in which different testing mode (parallel C-R, serial C-R etc) can chosen and then capacitance and resistance values can be found.

The impedance of parallelly connected capacitor and resistor is

$$|Z| = \left|\frac{R}{1 + SRC}\right| = \frac{R}{\sqrt{1 + (\omega RC)^2}}$$

In the impedance plane, it can be viewed as in figure below:

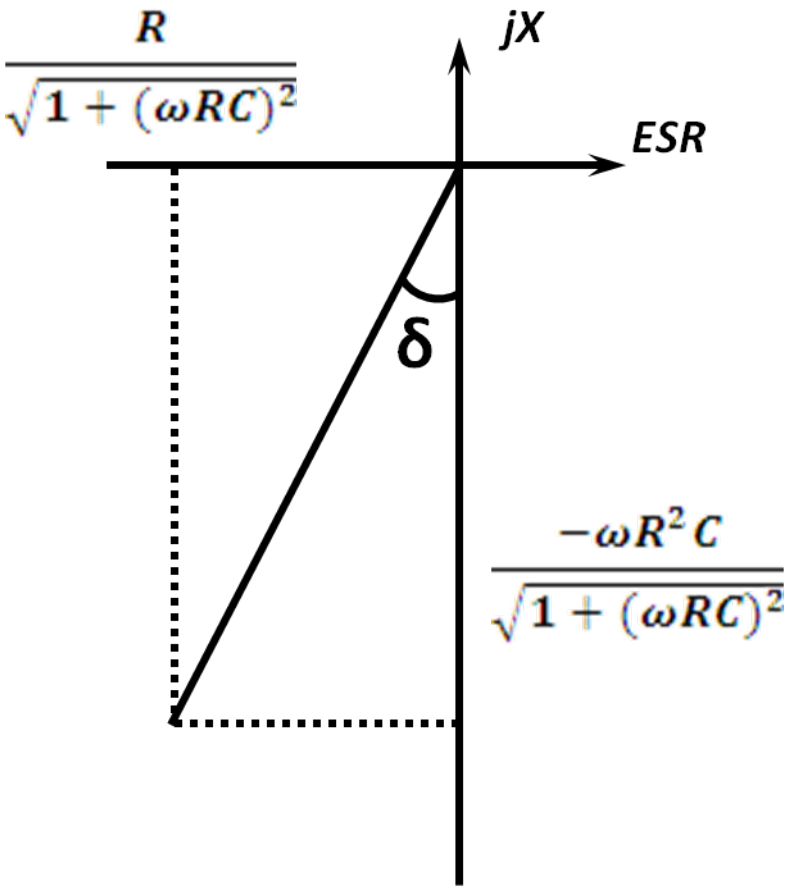


Figure 34 Impedance of a parallelly-connected capacitor and resistor on impedance plane. Dissipation angle is defined as the angle between the negative reactive axis and the capacitor's impedance vector.

Since the real part of the impedance is not the same as the resistor connected in parallel to the capacitor, rather, it is mathematically derived result called equivalent series resistance (ESR). The angle δ is a common way to characterize how dissipative gate dielectric is, and is normally expressed by $\tan\delta$.

The extracted dissipation angle from the fabricated MOS capacitor is shown in figure below:

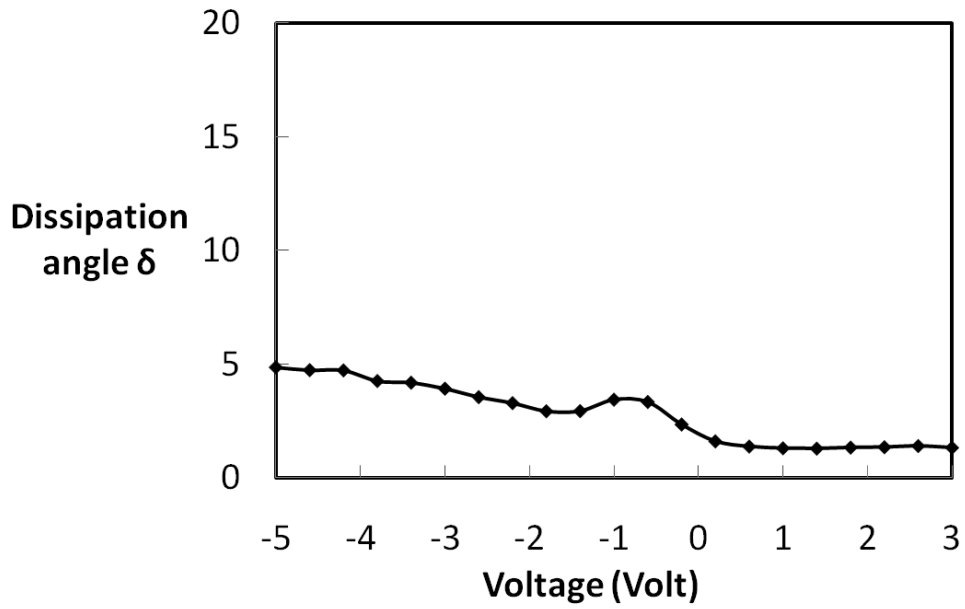


Figure 35 Dissipation angle – Bias voltage diagram of fabricated MOS capacitor.

As can be seen from figure above, under all tested bias voltage, the calculated dissipation angle is smaller than 5 degrees.

2.3.4 Electrical Characterization and Result Analysis.

Nanowire conductivity was measured right after fabrication and nonlinear I-V behavior was observed. Rapid thermal annealing (RTA) was then used to improve nonlinearity. The NWFET was placed in RTA chamber and the chamber was then flushed with N_2 gas, the temperature was then rapidly raised to 350 ℃ and was held for 5 minutes. Further measurement indicates that annealing process not only improves nonlinearity of the nanowire FET, but also increases the conductivity of nanowire as is evidenced also in other reports.[11, 81-84] The impact of thermal annealing on the conductivity of nanowire is difficult to model, however, several mechanisms are possible and are

commonly used to explain its effects: first, thermal annealing reduces lattice strain and rearrange the atoms especially at the grain boundaries and therefore reduce the number of defects; second, thermal annealing reduces the Schottky Barrier and results in Ohmic contact by forming gold-In-Sb alloy.

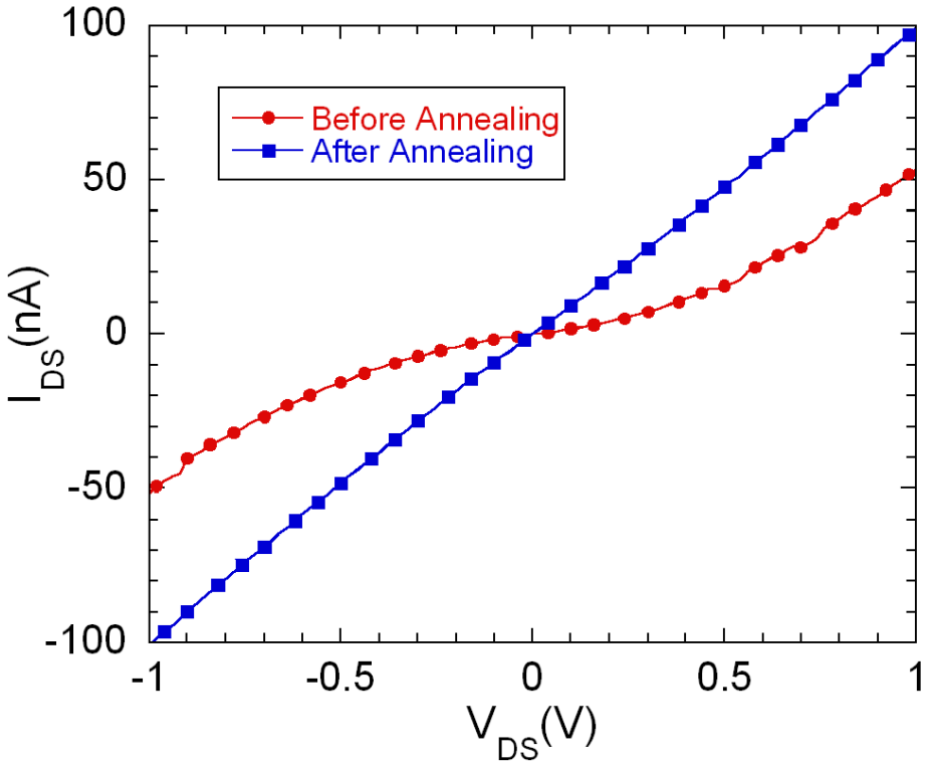


Figure 36 I-V characteristic before and after thermal annealing.

Due to the non-planar shape of the contact at nanowire-metal interface, and also possible nonlinear electrical behavior of the contact, four-point measurement is performed in order to decouple the effect of contact resistance from the resistance of the channel. A schematic of four point measurement is shown in figure below:

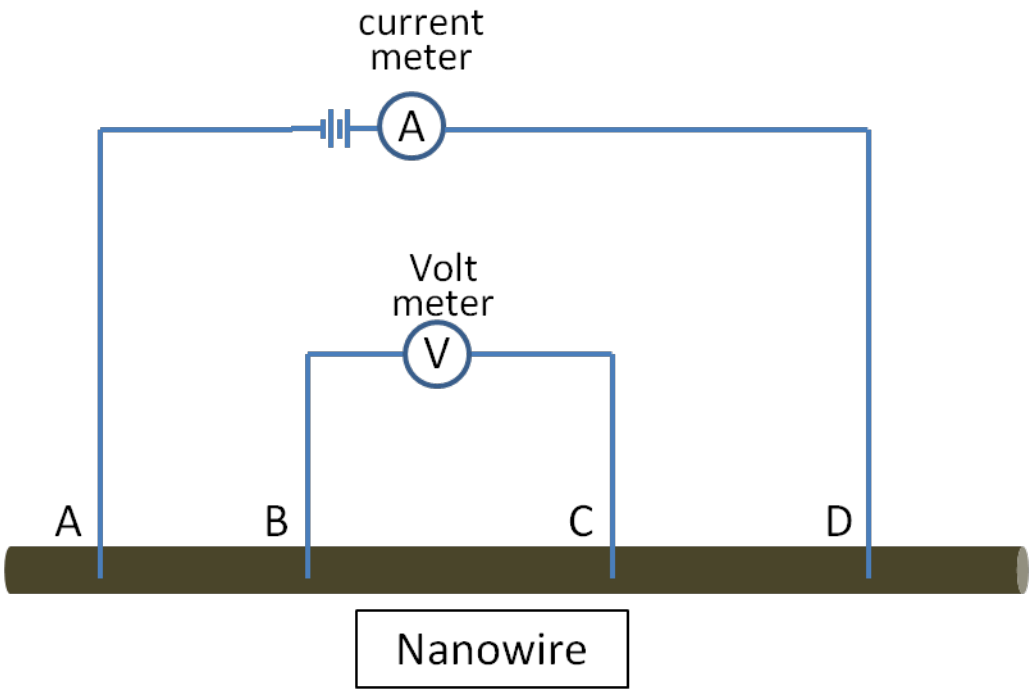


Figure 37 Schematic of four point conductivity measurement of a nanowire sample. The DC current is supplied between terminal A and D from SMU1 and SMU2; and voltage is monitored between VSU1 and VSU2 from Agilent 4155 semiconductor parameter analyzer. The advantage of four point measurement is that it eliminates the voltage drop from contact resistance at nanowire-metal interface, exposing the contact to voltmeter which is considered to have infinitely large output impedance.

The advantage of four point measurement is that it avoids problems caused by contact resistance.[85, 86] Agilent 4155C is used for the measurement in which, static testing current is supplied from terminal A and D connected as SMU1 and SMU2 separately, the voltage drop is monitored between terminal B and C connected as VMU1 and VMU2 separately.

Since a voltmeter can be treated with infinite output impedance, the inside B-C-voltmeter loop can be treated as open, therefore, no current is flowing through the contact and as a

result voltage drop on the contact is negligible, which means the monitored voltage in the voltmeter is the voltage drop solely on the segment BC of the nanowire. The resistance is then calculated through dividing voltage by supplied current.

A SEM image of NWFET sample for four point measurement is shown below:

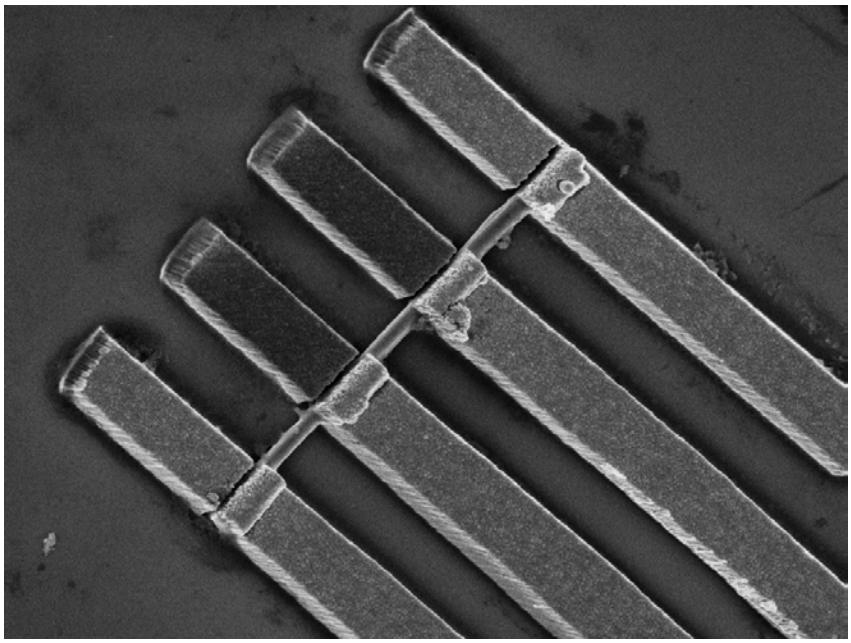


Figure 38 Four point measurement of nanowire, same contact width were used to ensure same contact properties.

One thing worth mentioning here is that the deposited metal contact is thin, normally smaller than 100nm (80nm in our case) in order to get best lift-off results. When a thin film contact covers nanowire, an Ω shape contact is supposedly to be formed, which covers close to 360 degrees of the nanowire radially, in reality however, nanowire itself blocks metal particles from depositing to the "shadowed" areas[87], which results in

seemingly continuous but disconnected metal contacts as can be illustrated in figure below:

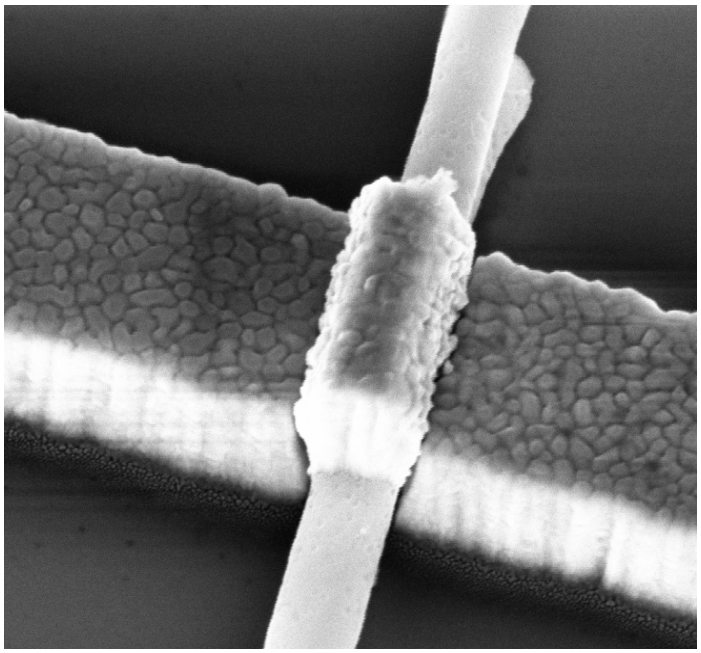


Figure 39 SEM image of broken metal contact on InSb nanowire.

This problem is largely inevitable in regular electron beam deposition system, where metal sources are heated up and metal particles are deposited in one specific direction depending on the position of the substrate and the holder. This problem is solved by multiples metals depositions from different angles respectively. A SEM image of such samples is shown in figure below:

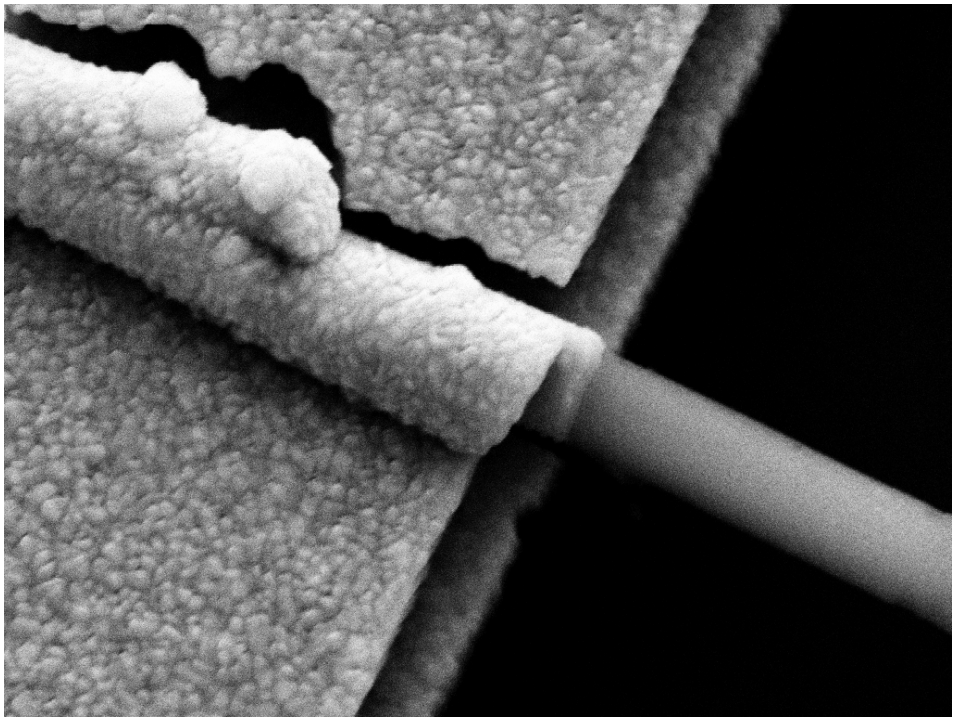


Figure 40 SEM image of improved metal contact which involves patchwork of a second metal deposition.

To accurately extract the carrier mobility, we provided a transistor level circuit model that takes into account the voltage drop on the under-lapped segments of nanowire as schematically shown in figure 41. In a top-gated nanowire FET, the top gate normally does not cover the whole channel between source and drain, therefore, the top gate only modulates the segment of the channel region that is right underneath the top-gate. However, the source to drain voltages is applied to the respective metal contacts, not directly to two terminals of the channel, similarly for gate to source voltage. As a result, V_{DS} and V_{GS} need to be replaced by $V_{D_0S_0}$ and $V_{G_0S_0}$ through equations:

$$V_{D_0S_0} = V_{DS} - I_{DS} \cdot (R_{S1} + R_{S2})$$

$$V_{G_0S_0} = V_{GS} - I_{DS} \cdot R_{S1}$$

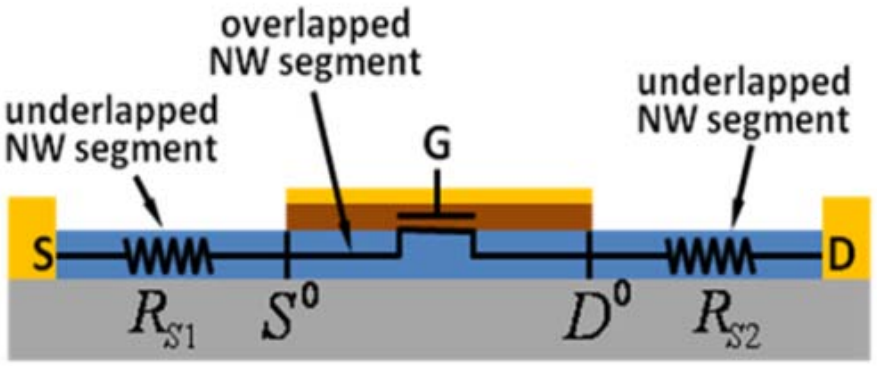


Figure 41 Schematic of NWFET featuring underlapped NW segments in which conductivity of underlapped nanowire segments are determined by backgate voltage.

The transfer characteristic is obtained by fixing V_{DS} and sweeping top-gate voltage, the $I_{DS} - V_{GS}$ curve with and without consideration of underlapped segments is shown in figure 42.

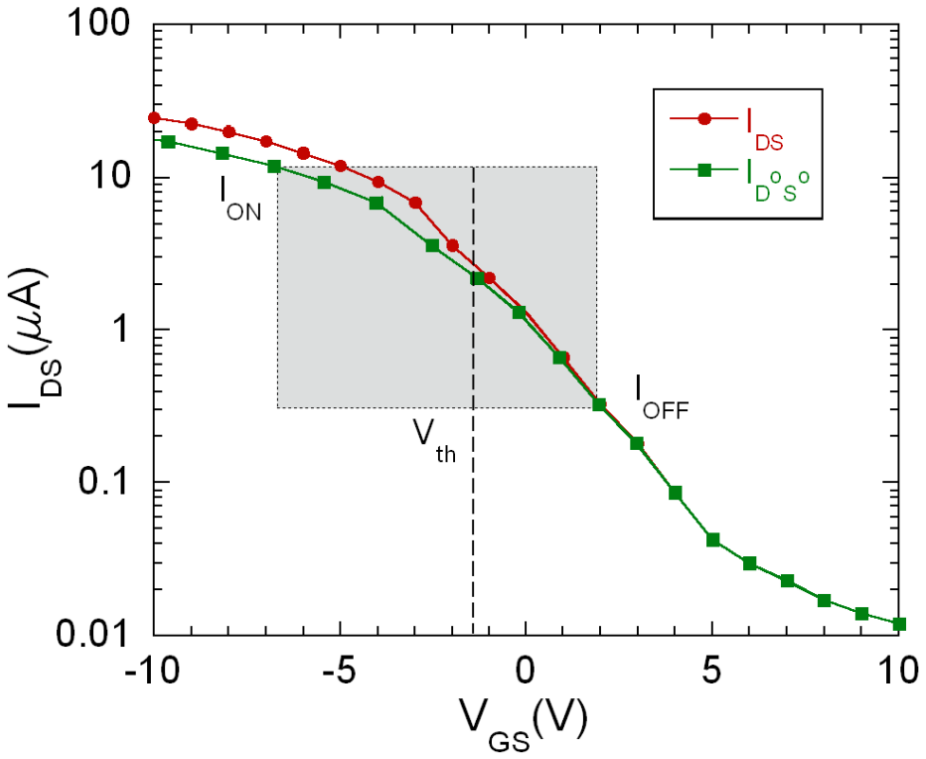


Figure 42 Transfer characteristic of NWFETs, the gray area is specified according to benchmark proposed by Chau R. [65] for extracting critical parameters such as threshold voltage, I_{ON}/I_{OFF} ratio, carrier mobility of fabricated nanowire FET. Green and red lines indicate the difference in drain-to-source current before and after taking consideration of the underlapped segments of nanowire FET.

Strong p-type conduction was observed and the hole density was found to be $1.5 \cdot 10^{7}$ cm^{-3}, we adopted the benchmark suggested by R. Chau in [65] and found the threshold voltage V_{TH} = -1.3V and I_{ON}/I_{OFF} = 40, the hole mobility was found to be 292.8 $cm^2 \cdot (V \cdot s)^{-1}$.

2.4 Conclusion

In this work, we investigated the electrostatic performances of InSb nanowire based field effect transistors (NWFETs). InSb is a direct bandgap material and has the smallest electron effective mass among a variety of semiconductor materials, which gives it

extremely high carrier mobility in bulk form and makes it a potential candidate for high-speed electronic device applications. Nanowire as an example of low-dimensional (1D) material system, has demonstrated unique properties that are superior to its planar counterpart such as more efficient gate control, lower leakage current, higher tolerance to short channel effects. Also, the intrinsic self-assembly capability in nanowire makes possible a complete bottom-up integration scheme.

Two types of nanowires were synthesized here by template-assisted electrochemistry and chemical vapor deposition (CVD) respectively, in both cases, NWFETs were made by electron beam lithography (EBL) and crystallinity was confirmed by transmission electron microscopy (TEM) and selected area diffraction (SAD) patterns. For electrochemistry based nanowire, ambipolar conduction was observed and hole was the major carrier demonstrated by strong p-type conduction, the effect of thermal annealing on the conductivity of metal-semiconductor contact was analyzed, a NWFET model that took into consideration the underlapped region in top-gated NWFET was provided and used to extract hole mobility in the channel, which was 292.84 $cm^2V^{-1}s^{-1}$ with a hole density of $1.5\times10^{17}/cm^3$ at ON state. For CVD based nanowire, the diameter was below 40nm with an average of 20nm. Vapor-liquid-solid (VLS) process was speculated to be the mechanism responsible for nanowire growth. The efficient gate control was manifested by high I_{ON}/I_{OFF} ratio which was on the order of 10^6 and a small inverse subthreshold slope (<200 mV/decade). Scale analysis was used to successfully account for the disparities observed among a number of sample devices by comparing the

screening length and the corresponding channel length. N-type conduction was found in all NWFETs with electron mobility between 110 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 169 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

Chapter 3 Electrical properties of DNA/PNA carbon nanotube conjugate

3.1 Introduction of DNA, PNA and carbon nanotube (CNT)

Deoxyribonucleic acid (DNA) has been under research limelight for decades due to the extremely important role it plays in the process of taking genetic information and converting it to a protein. The information in DNA is stored as a code made up of four chemical bases: adenine (A), guanine (G), cytosine (C), and thymine (T) and these bases are categorized into two types: purines and pyrimidines. Adenine and guanine are five – and six-membered heterocyclic compounds called purines while cytosine and thymine are six-membered rings called pyrimidines. The characteristics of these acids dictate specific parings of A - T and G - C which are called complementary base paring and the hydrogen bonds between purines and pyrimidines can be broken and rejoined without much difficulty. The two strands of DNA in a double helix can therefore be pulled apart and back like a zipper by either mechanical force[88] or high temperature. The ability to selectively form hydrogen bond between bases A – T and G – C has pervasive implications especially when the sequence of the bases being able to be programmed according to specific purposes. In such applications, DNA functions more as a structural material than carrier of biological information. Since the bonding between corresponding DNA bases happens autonomously under certain conditions without external force or manipulation of any sorts, DNA based integration could suit self-assembly purpose. One prominent example is “DNA origami[89]” in which DNA sequence was programmed in a way that when corresponding bases form a bond and got linked to each other, DNA strand folds as it is programmed and therefore the overall folded shape reflect specific

patterns. DNA based self - assembly is not limited to generating patterns solely by DNA itself, but also incorporating chemically modified nanostructures such as nanowires or carbon nanotubes in which cases, DNA often functions as linkers to combine these components for specific purposes. Deng Z. et al had reported the DNA templated fabrication of 1D parallel or 2D crossed metallic nanowire arrays,[90] in which fluid flow was firstly used to prepare parallel or crossed DNA arrays and then metal ions were applied to quickly absorb onto negatively charged DNA backbones and finally palladium nanowires were produced by chemical reduction of the absorbed metal ions. Braun E. et al demonstrated potential application of constructing functional circuits in which hybridization of DNA molecule with surface bound oligonucleotides was first used to stretch it between two gold electrodes and DNA molecule was then was then used as a template for the vectorial growth of conductive silver wire that connects two electrodes. [91] Mirkin C. et al utilized DNA for assembling nanoparticles aggregates in which non-complementary DNA oligonucleotides batches of gold particles were first attached to the surface of two batches of gold nanoparticles, when mixed to the solution of an oligonucleotide duplex that are complementary to the two joined sequences, nanoparticles self-assembled into aggregates.

The use of DNA, however, is limited because of its charged backbone, long probe lengths and low thermal and chemical stabilities. Peptide Nucleic Acid (PNA) which is the artificial analogue of DNA provides a way to utilize the self-assemble advantages while devoid of above mentioned restrictions. Originally designed as a ligand for the

recognition of double stranded DNA,[92] PNA is artificially synthesized polymer of which the backbone is made from repeating N-(2-aminoethyl)-glycine units linked by peptide bonds (as shown in figure below). Because the backbone of PNA does not contain charged phosphate groups, the binding between its strands is stronger than that between DNA strands due to the lack of electrostatic repulsion. Also, PNA oligomers are able to form very stable duplex structures with Watson-Crick complementary DNA, RNA (or PNA) oligomers, and can bind to targets in duplex DNA by helix invasion as well.

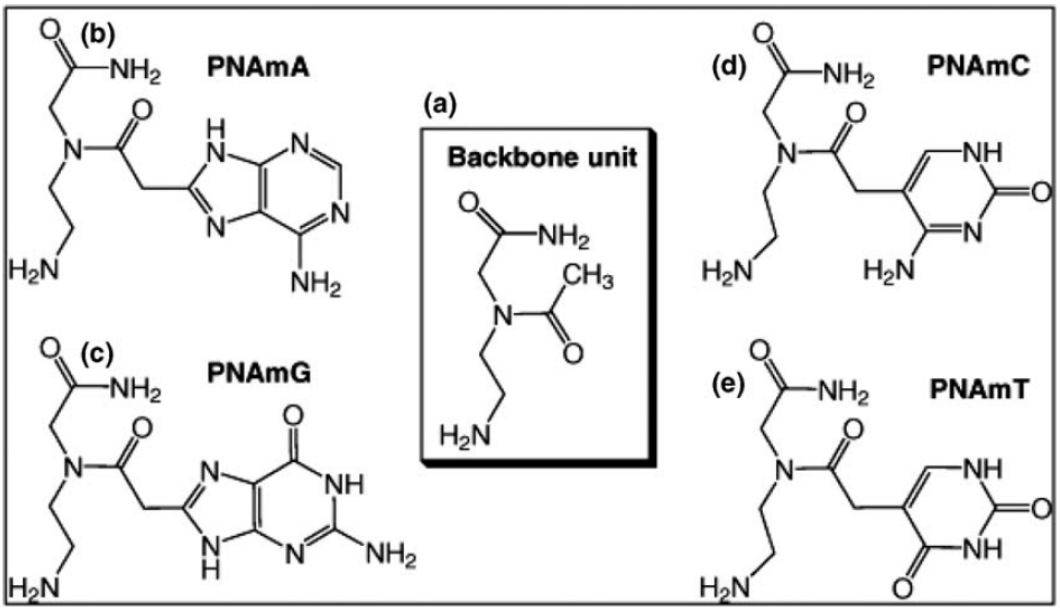


Figure 43 (a) Backbone unit of PNA. (b) - (e) different bases attached to backbone of PNA by methylene carbonyl linkages.

Carbon nanotubes (CNTs) are hollow cylinders of carbon atoms and were first discovered and characterized by Iijima in 1991. [93] One way to understand the structure of carbon nanotube is view it as the rollup of a sheet of graphene (one-atom-thick planar sheet of sp^2-bonded carbon atoms packed in honeycomb crystal lattice). Depending on the rollup

angle (chirality), carbon nanotubes can be metallic or semiconducting with the bandgap ranging from 0 to 2eV. Carbon nanotubes can also be classified into single-wall CNTs and multi-wall CNTs depending on the number of "shells".

Carbon nanotubes had been found to have extraordinary mechanical,[94-98] thermal,[99-102] optical[103-105] and electrical properties that had drawn researchers' attentions for decades. In terms of its electrical properties, Javey A. et al had experimentally and theoretically demonstrated high performance ballistic carbon nanotube transistor with zero or slightly negative Schottky barriers with which the 'ON' state of semiconductor nanotubes can behaves like ohmically contacted ballistic metallic tubes, exhibiting room-temperature conductance near the ballistic transport limit of $4e^2/h$, high current-carrying capability of roughly 25μA per tube and high hole mobility of 4000 $cm^2V^{-1}s^{-1}$.

Since carbon nanotubes are normally grown in bundles, both metallic CNTs and semiconductor CNTs are tangled together most of the time after synthesis. The co-existence of semiconductor CNTs and metallic CNTs forms one of the major challenges in using carbon nanotube as fundamental building blocks for very large scale integration (VLSI) purposes. Gomez L. et al[106] had worked out a way for metal-to-semiconductor conversion of carbon nanotubes for field effect transistors based on both aligned nanotubes and single nanotube devices. By applying light irradiation to inactivate the metallic nanotubes, I_{ON}/I_{OFF} ratio in the channel current was improved up to 5 orders of magnitude. Besides light-induced conversion method, Lin A. et al.[107] had

demonstrated that, with special post-processing techniques, the threshold voltage (Vt) and on-off current ratio (I_{ON}/I_{OFF}) of multiple-tube carbon nanotube field effect transistors can be tuned as much as 2V and 5×10^5.

To find practical use out of low-dimensional nanomaterials, two issues have to be solved: (1) mass production, which means wafer scale synthesis has to be possible. (2) device integration, which means a scheme that integrate not only one but hundreds of, or thousands of unit devices has to be possible. The challenges often lie in the second issue since nanomaterials such as nanowire or carbon nanotubes are highly disordered after synthesis and it's difficult to apply top-down integration approaches to mass-produce a number of devices simultaneously. Therefore, alignment of nanomaterials either during or after synthesis process is highly desirable. Different after-synthesis alignment techniques have been proposed and some successfully carried out experimentally with the core idea of utilizing externally applied electrical field[108, 109], magnetic field [110-114] or fluid force.[115]. However, these methods are all post-synthesis based and unanimously required additional treatment of the sample that often includes a few lithography-based fabrication steps which greatly reduce the transferability of the sample. To have nanomaterials aligned during synthesis seems to be the ultimate answer for the problem. To achieve that, Ryu K. et al. had developed a nanosphere lithography technique for the preparation of catalyst nanoparticles for the synthesis of aligned single-walled carbon nanotubes on quartz, while Kang S. J. et al [116]had successfully

synthesized highly ordered, high quality and well aligned carbon nanotubes with mobility and scaled transconductance as high as 1000 $cm^2V^{-1}s^{-1}$ and 3000 S m^{-1} respectively.

The distinct advantages of DNA/PNA and carbon nanotubes have been discussed based on recent experimental achievements. The marriage of the two therefore, drew great research attentions in the hope that the bio-chemical conjugate could embody the advantages of both. Specifically, the conjugate could be self-assembled to form largely ordered structures for high level device integration, while the chemical component such as carbon nanotubes or nanowires constitute the backbone of unit device.

3.2 Synthesis of PNA-CNT Conjugate

Synthesis of PNA-CNT conjugate mainly consists of three steps: (1) chemical modification of single walled carbon nanotubes; (2) functionalization of PNA solution; (3) carbodiimide coupling of single walled CNT and chemically modified CNTs.

The goal of the first step is to functionalize the end caps of single walled carbon nanotubes to form single walled carbon nanotube bearing NHS esters while minimizing the same effect from taking place at the side walls. The single walled carbon nanotubes were bought from Sigma Aldrich in powder form and were first immersed in 2.4 M of HNO_3 for 14 hours for oxidation. The end caps of single walled carbon nanotubes have curvatures and are fullerenic, therefore, they are more prone to react with acid and get oxidized, which is desirable to our purposes, however, the sidewall of carbon nanotubes can also get oxidized in acid in which case, electrical characterization result of the final

structure does not fully reflect the supposedly PNA-CNT conjugate's properties, to make things worse, PNA molecules could accidentally bridge two neighboring CNTs, creating unwanted connections which affect the accuracy of final characterization results. Therefore, the concentration of nitric acid should be as such so that it is strong enough to fully oxidize both end caps of the single walled carbon nanotubes, but weak enough to not oxidize the side wall of carbon nanotubes. Original single walled carbon nanotubes are fairly long, to increase the possibility of conjugating them with PNA, it is recommended to shorten these nanotubes, this step was done by sonicating the sample at 40℃ at 55 kHz for 1 hour in a 3:1 mixture of concentrated H_2SO_4 (98%) and HNO_3 (70%) [117]. After sonication, the solution was filtered by passing through 0.2-μm thick polycarbonate membrane and washed thoroughly to remove residual acid. By far, oxidized, cleaned and shortened single walled carbon nanotubes have been obtained. To create SWNT bearing NHS esters, the single walled carbon nanotubes were subsequently suspended in water and incubated for 30 minutes in 2mM 1-ethyl-3(3-dimethylaminopropyl) carbodiimide hydrochloride and 5 mM N-hydroxysuccinimide (NHS) and esters are formed based on conventional nucleophilic addition mechanism. Throughout the process, the solution was buffered to have pH value maintained below 5 in order to prevent the hydrolysis of single walled carbon nanotube-NHS esters.

The second step was to prepare functionalized PNA solutions. PNA (sequence: NH_2 – AA-GTGCTCATGGTG-AA-NH_2, AA: amino acid) was purchased from Applied Biosystems Inc. and functionalized on both ends by glutamate amino-acid residue, since

amine present on the PNA backbone is not sufficiently reactive for conjugation purposes. This process starts by dissolving purchased PNA powder in 584 µL water at 50 ℃ and vortexing the solution by whirlpool effect. The final concentration of the solution was 100µM and this solution was then vacuum-evaporated at room temperature and refrigerated at -20 ℃. Due to the curling shape of PNA, it has a strong tendency to aggregate and form tangled bundles, [118] this effect was more severe in this case as both ends of the carbon nanotubes had been functionalized. To reduce the aggregation among PNA molecules, the solution was diluted and sonicated at 40 ℃ for 2 hours which resulted in much smaller PNA molecular clusters.

In the third step, filtered single walled carbon nanotube – NHS esters was then added to the PNA in PBS buffer and left for 1 hour for reaction. Both end of functionalization of PNA led to the formation of single walled carbon nanotubes – PNA conjugate as amide bond was generated between the glutamate amino-acid residue on PNA backbone and single walled carbon nanotube bearing NHS esters. These conjugate were then transferred to water after five cycles of ultra-centrifuge to remove salt from the solution.

3.3 Electrical Characterization of SWCNT-PNA Conjugate

Electrical characterization of single walled carbon nanotube – PNA conjugate focuses on its I-V characteristics and transfer properties. Since detailed research has been done on single walled carbon nanotubes and their electrical properties are well predictable, this

work is mainly projected to explore the role of PNA in electrical properties of CNT-PNA-CNT conjugate.

Since making metal pads directly on PNA sample by electron beam lithography is a time consuming as well as effort consuming process, besides, high energy electron bombarding the target PNA could lead to permanent irreversible damages. In this work, we dropped the solution of CNT-PNA-CNT conjugates onto a substrate that has photolithographically made alignment marks, which helps locating target conjugate, another advantage of these alignment marks is that residual charges can be easily carried away through the substrate to the ground, which makes imaging of these CNT-PNA-CNT samples easier. After dropping the sample solution to the pre-patterned substrate, the next step is locating the sampling by SEM imaging, which was done under focused ion beam (FIB) milling system (LEO XB1540). The fabrication of metal contacts in FIB system is a more straightforward process in which gaseous metal compound was first introduced to the vacuum chamber and allowed to chemisorb onto the sample, by scanning an area with the beam, the precursor gas will be decomposed into volatile and non-volatile components, the non-volatile components (usually metal) were left on the surface as a deposition. The scanned areas are specified by computer program instantaneously and can be in any specified shapes, therefore do not require any lithography-related pattern drawing and aligning steps.

The electrical property of carbon nanotube was first confirmed by I-V measurement, figure 44 is a SEM image of the device:

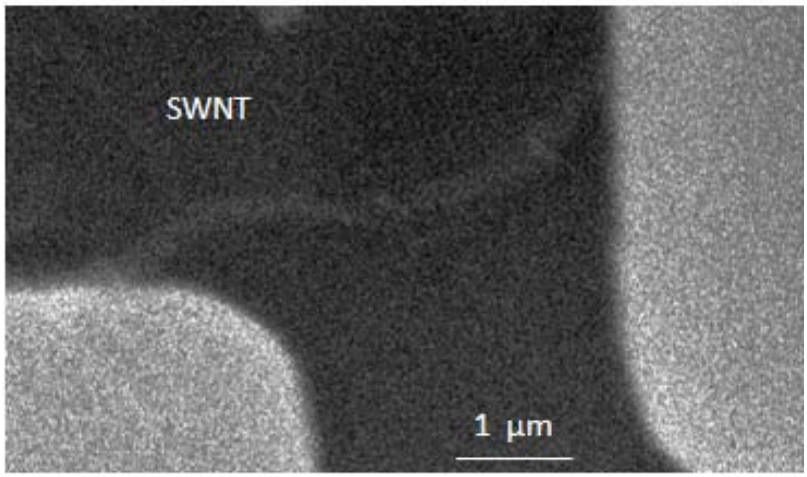


Figure 44 SEM image of single walled carbon nanotube bridging two metal contacts predefined by photolithography.

I-V measurement result of single walled carbon nanotube is shown in figure 45:

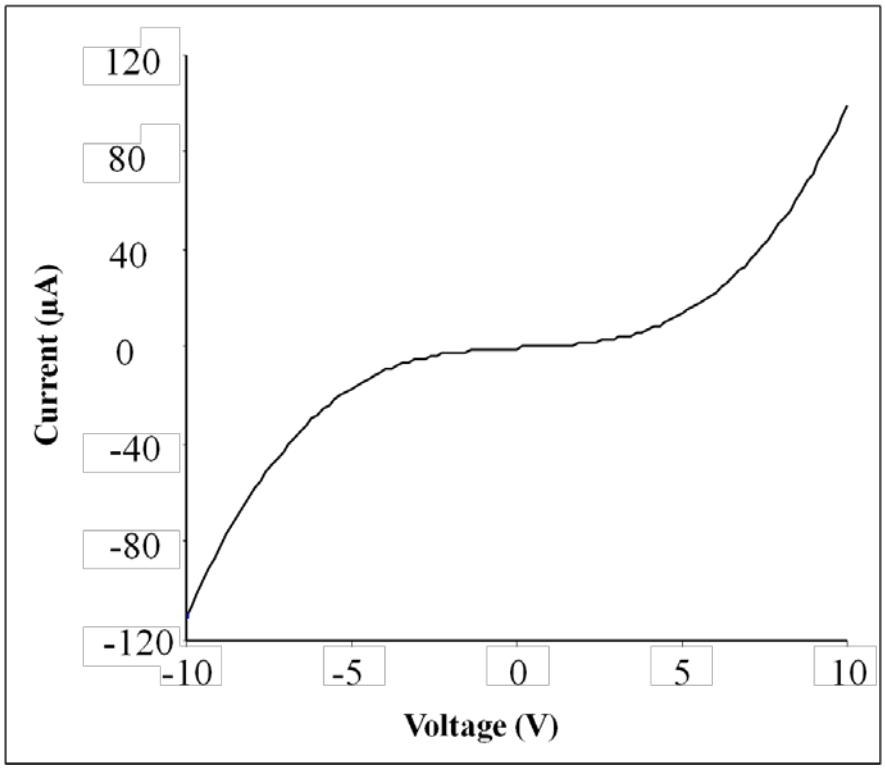
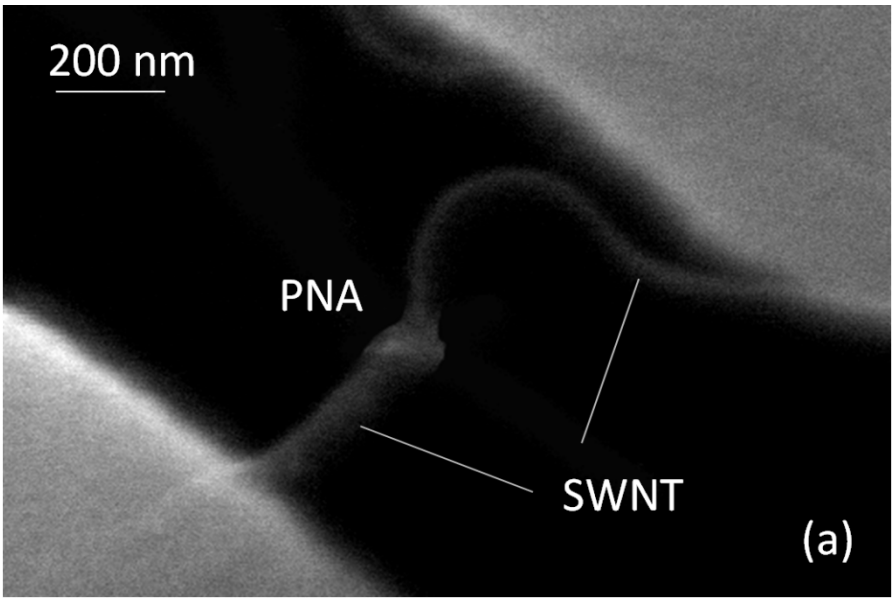


Figure 45 I-V characteristic of single walled carbon nanotube.

Current as high as 120 μA was observed at voltage of 10 volts, however, carbon nanotube also demonstrate high level of nonlinearity as current tends increase exponentially when applied voltage increases on both extremes. The I-V nonlinearity is largely due to the misalignment between the work function of metal contact and carbon nanotubes.

The CNT-PNA-CNT conjugates are identified visually by SEM images; PNA molecules tend to bind together forming ball-shape structure and are relatively bright comparing to carbon nanotubes.

SEM images of a set of sample devices are shown in figure 46:


200 nm
PNA
SWNT
(a)

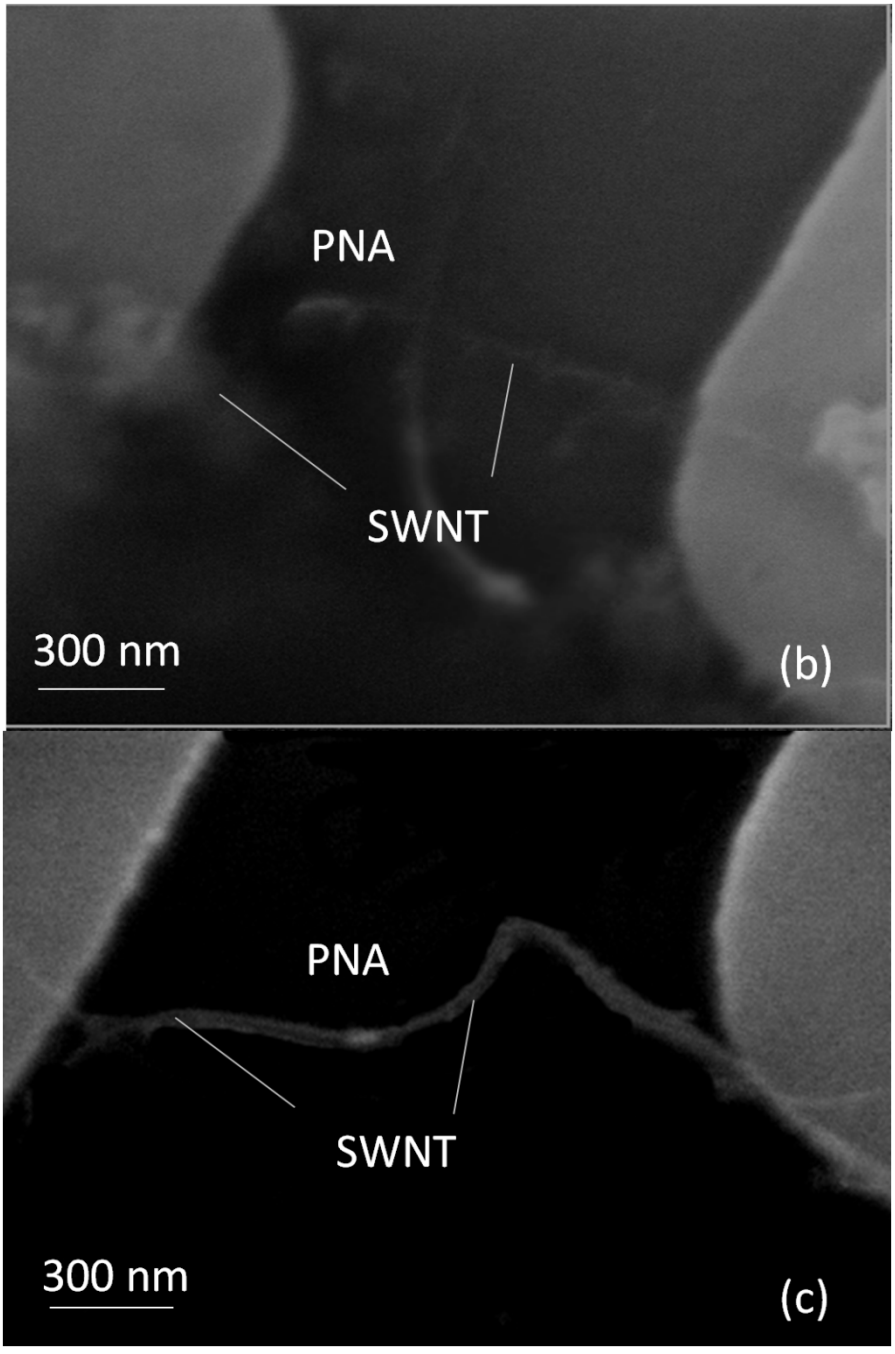


Figure 46 SEM images of CNT-PNA-CNT conjugates. (a) One side of PNA is connected to single-walled carbon nanotube while the other side is multi-walled carbon nanotubes. (b) CNT-PNA-CNT conjugate with carbon nanotube cross-touched by another (c) CNT on both side of are in bundles.

I-V testing results of PNA-CNT-PNA conjugate is shown in figure 47. An interesting feature in its electrical property is that at some points, current drops with increasing voltage demonstrating effect of negative differential resistance (NDR) while in the voltage region without NDR effect, electrical properties does not change radically from pure carbon nanotube samples as in figure 43.

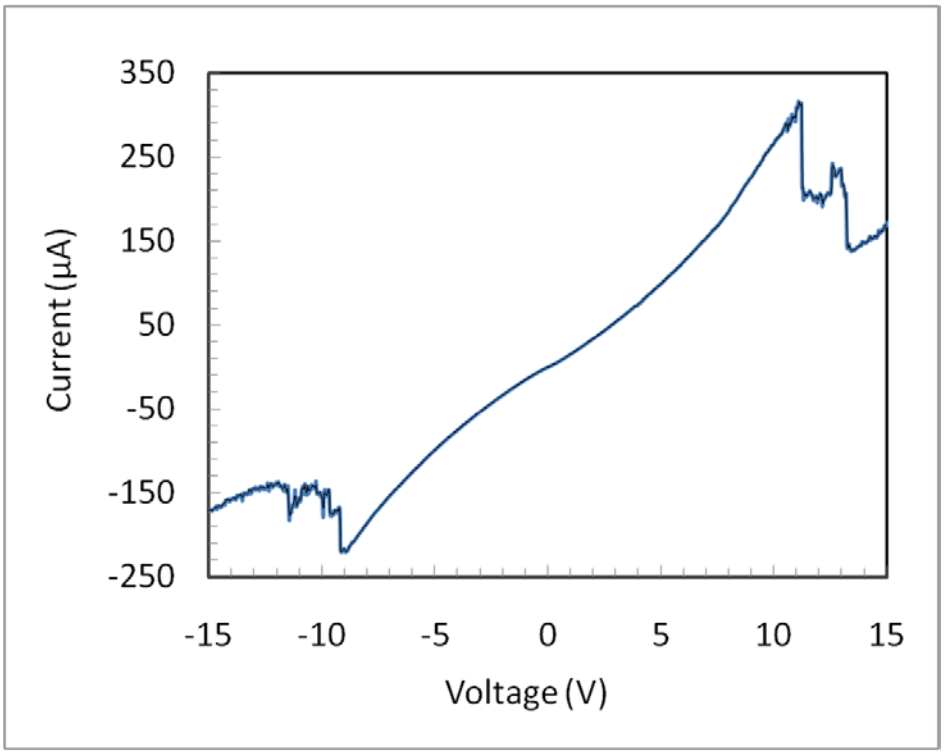


Figure 47 I-V characteristic of CNT-PNA-CNT conjugate, the current level does not vary much from that in pure CNT samples. Negative differential resistance was observed at certain applied voltages which depend upon the alignment of Fermi energy level in one CNT to the resonance states in the PNA.

Negative resistor does not exist as a discrete component in reality, however, some types of diode does exhibit negative resistance in some part of the operating range, such as resonant tunneling diode (RTD). A mechanism similar to RTD was used here to account for the NDR effect in CNT-PNA-CNT conjugate.

The energy band of the conjugate structure is shown in figure 48:

Figure 48 Energy diagram showing potential barriers that leads to NDR effects.

where E_C is the conduction band edge and E_f is the Fermi energy level. The difference in conduction band appears as a result of the conjugate heterostructure, which forms quantum wells for electrons at regions where conduction band is lower than that in neighboring structures without applied voltage.

When voltage is applied to the heterostructure, the whole energy band tilts which is demonstrated in figure 49:

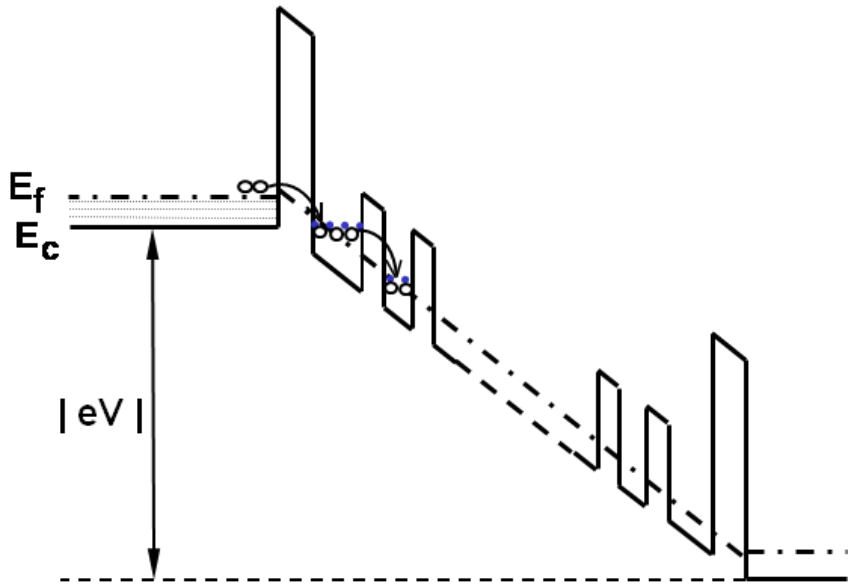


Figure 49 Energy diagram tilted as a result of applied voltage that lead to electrons tunneling or "hopping" through potential barriers.

Energy band tilts because of the electron energy difference caused by the applied voltage: The moving of electrons is however, not smooth due to energy barriers resulted from heterostructure based quantum wells. When the barrier heights are too high for electrons to move out, electrons are "trapped" and can only tunnel through the barrier. The tunneling ratio is expressed as:

$$T^{-1} = 1 + \frac{V_0^2}{4E(V_0 - E)} sinh^2(\frac{2a}{\hbar}\sqrt{2m(V_0 - E)})$$

where T is the transmission ratio, $V_0$is the barrier height, E is electron energy, m is mass of electron and a is the width of potential barrier.

The net tunneling current is calculated by integrating transmitted electrons over transverse direction over all existing energy states and is given by [119]

$$J = \frac{e}{4\pi^3\hbar}\int_0^\infty dk_l \int_0^\infty dk_t [f(E) - f(E')]T^*T\frac{\partial E}{\partial k_l}$$

E and E' refer to energy of incident electron and that of the transmitted. $f(E)$ is the Fermi distribution function given by

$$f(E) = \frac{1}{e^{(E-E_f)/kT} + 1}$$

Energy levels within the potential barriers are highly discrete when the thickness of the "sandwiched" layer is thin as it can be regarded as 1D potential well in which case the available energy levels are also called resonant states.

As a result of applied voltage, energy levels inside the quantum well are lowered down comparing to the source Fermi level during which process several critical points defines the overall I-V characteristic. First one is when the lowest resonance state aligns with the Fermi energy at the source (indicated in figure below). Before this point, current increases with increasing applied voltage as lowest resonance state gets closer to the source Fermi energy.

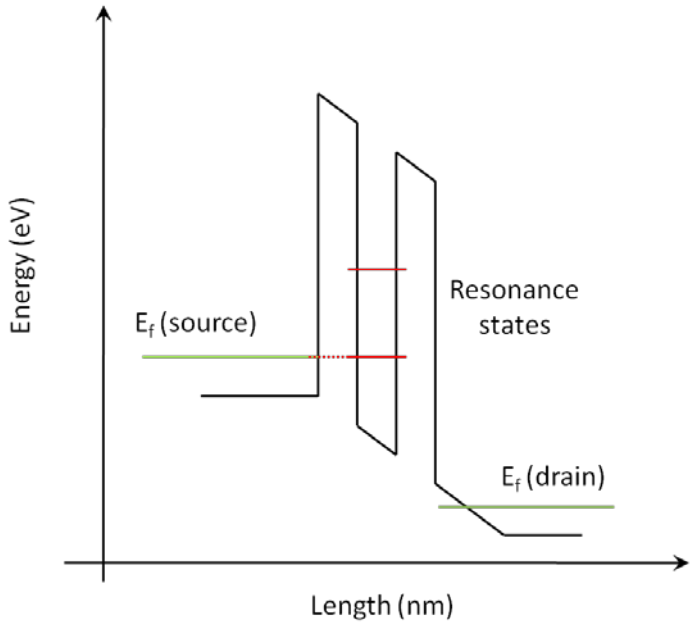


Figure 50 When applied voltage increases to a point that lowest resonance state aligns with Fermi energy at source, current reaches its maximum, and before that point, current keeps increasing with applied voltage.

As applied voltage keeps increasing, lowest resonance states becomes lower than source Fermi level, due to the misalignment between source Fermi level and the resonance state, current starts to decrease, the downtrend in conduction current lasts till the second lowest resonance state is involved to such degree that current contributed by the second resonance state compensates that from the first state. This forms another critical point, as current falls to its minimum. (indicated in figure 51).

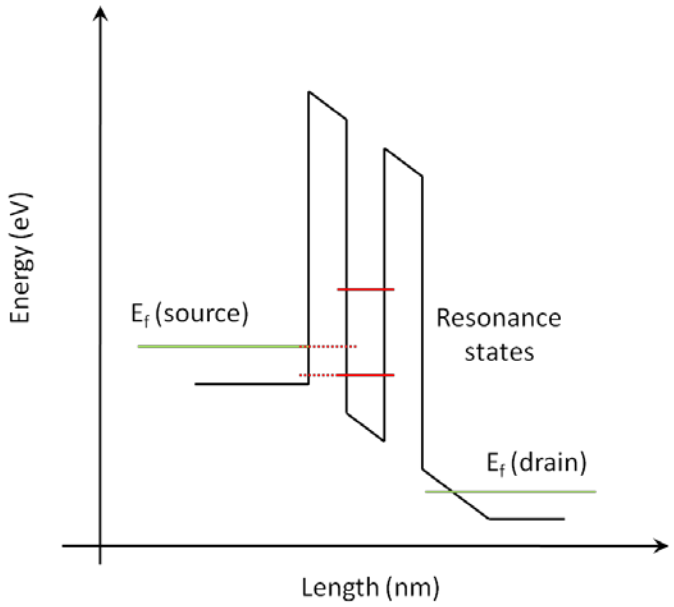


Figure 51 With lowest resonance state shifted away from the source Fermi level, current drops with applied voltage. The decrease in current continues until second lowest resonance state becomes available to accommodate tunneling electrons and current starts to increase.

As the second lowest resonance state gets lower, current increases again. To intuitively understand this, electrons tunneling through the energy barrier need corresponding energy levels to "stay", in the case when there is no energy level to accommodate the tunneled electrons, current decreases.

The electrical conductivity of these bioconjugates was measured under different temperatures ranging from 70K to 400K. As shown in figure 52, NDR effect was observed at all temperatures, though there is a variation in the volatge when NDR takes place. This variation is reported earlier and could be attributed to the large number of amide bonds between SWNTs and PNA.

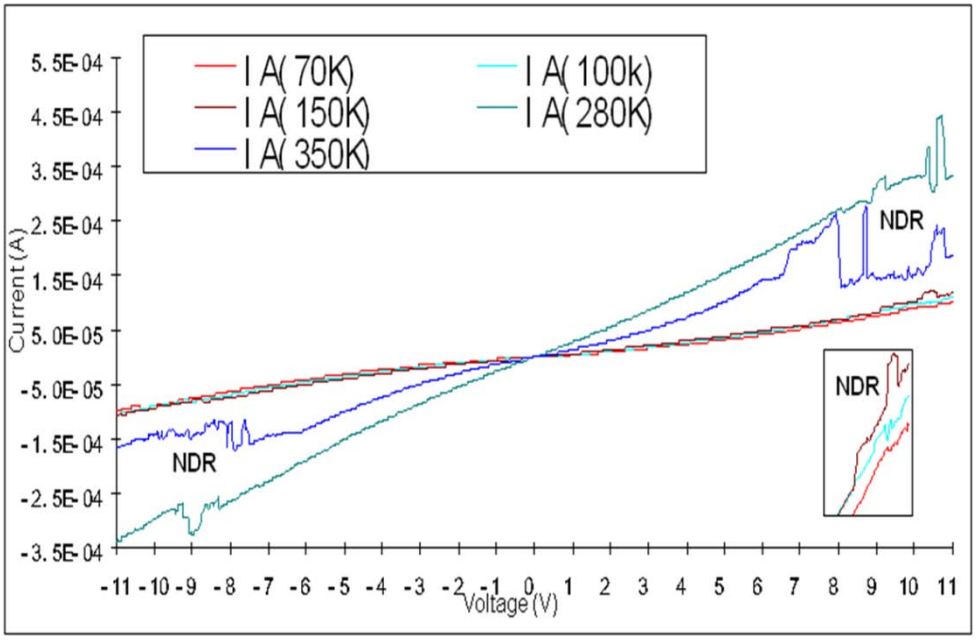


Figure 52 I-V characteristics of CNT-PNA-CNT conjugate at temperatures from 70K to 280K.

For measuring the conductivity applied voltage was limited to 5V as no NDR was observed within this voltage range. As shown in the figure 53, conductivity increases monotonicaly with temperature between 90K and 280K. The modest increase in conductivity results from the increase of electron energies at source, which consequently enhances the transmission coefficient. We also noticed a “breakdown” point at 350K after which conductivity of CNT-PNA-CNT bioconjugate experiences a sudden drop. The mechanism for the abrupt change in conductivity at temperature range from 300K to 400K is observed for the first time. As there is not evidence or explanation of such, we speculate the degradation in conductivity is casued by melting or burning of PNA molecules which leads to the sudden drop in conductivity.

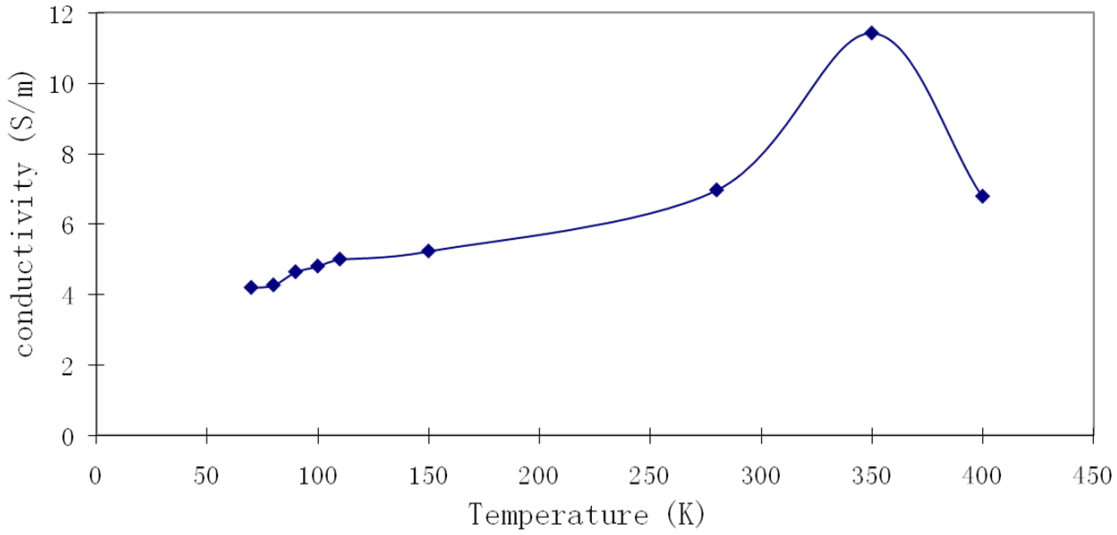


Figure 53 Conductivity – temperature relationship of CNT-PNA-CNT conjugate

3.4 Conclusion

In this work, we synthesized CNT-PNA-CNT conjugate and measured its electrical properties. The synthesis process involves three major steps: chemical modification of single walled carbon nanotubes in which end caps of single walled carbon nanotubes are functionalized to form single walled carbon nanotube bearing NHS esters while minimizing the same effect from taking place at the side walls. The second step is the preparation of functionalized PNA solution in which PNA was functionalized on both ends by glutamate amino-acid residue and the last step was the formation of CNT-PNA-CNT conjugate by adding single walled carbon nanotube – NHS esters to the PNA in PBS buffer and the target conjugate was formed by spontaneously generated bond between the glutamate amino-acid residue on PNA backbone and single walled carbon nanotube bearing NHS esters followed by centrifuge to remove salt from the solution.

The electrical characterization of CNT-PNA-CNT conjugate was carried out by first confirming the electrical properties of single walled carbon nanotube, and then I-V characteristic of CNT-PNA-CNT conjugate was tested. Negative differential resistance was observed in all devices which presents as unique property of this conjugateThe mechanism of NDR effect was explained in loose analogy to resonant tunneling diode in which negative resistance comes from the misalignment between Fermi energy in the source and resonance state in the potential barrier. While the experimentally observed NDR effect takes place in a repeated manner, several uncertainties remain which deserve special attention and further research in order to find practical applications in CNT-PNA-CNT conjugate: first, the applied voltage under which NDR effect occurs has been largely a random value. While the variations in this particular voltage are not too large to estimate, the core relationship between this voltage and the types of PNA remains unclear. In the case of CNT-DNA-CNT conjugate, it has been reported that ups and downs in conduction current is related to the base pairs in DNA. We speculate similar mechanism in PNA conjugate. Secondly, stability of the conjugate needs further study especially with respect to temperature since I-V characteristic has shown great dependence on temperature. The effect of temperature on the conjugate's conductivity is certainly more than just changing the electrons' kinetic energy as conductivity drops abruptly after 350K, though breakdown of molecule-nanomaterial structure is often regarded as the reason, breakdown often tends to be irreversible and brings conduction current to negligible level, which however, is not the case in CNT-PNA-CNT conjugate as the conductivity is still in

the same level as that between 90K and 280K. Lastly, techniques need to be developed to improve the uniformity of CNT-PNA-CNT conjugate in terms of the PNA structures.

Chapter 4 Conclusion

This thesis has summarized research works done on two types of nano-material structures: InSb nanowire and CNT-PNA-CNT conjugates. Both has drawn great amount of research attentions over the years for their unique properties and it is the author's wish that this work adds a meaningful share to the community that has already been saturated with information of all sorts.

The downscaling trend in microelectronics has been reviewed at the beginning which leads to the necessity of discovering new methods to overcome the barrier predicted by Moore's Law. Nanowire electronics and molecular electronics are two of the mostly researched areas. Theoretically, nanowire based electronics has the advantage of high surface to volume ratio, specifically for nanowire based field effect transistors, it has demonstrated high carrier mobility in some material systems and better gate control. The first part of this thesis work is on InSb nanowire field effect transistor. Two methods of nanowire synthesis methods have been implemented namely chemical vapor deposition (CVD) based method and electrochemistry based method. The advantages and disadvantages of both have been reviewed and single crystal nanowires synthesized by both methods have been confirmed by a number of techniques. Critical parameters of nanowire transistor have been extracted through characterizing the performance of nanowire based field effect transistors. In the case of electrochemistry nanowire transistor, p-type conduction was demonstrated with hole mobility of 292.84 $cm^2V^{-1}s^{-1}$ and hole density of $1.5\times10^{17}/cm^3$ at ON state. In the case of CVD based nanowire transistor,

superior performances were observed with excellent gate control demonstrated by I_{ON}/I_{OFF} current ratio on the order of 10^6 and a small inverse subthreshold slope smaller than 200mV/decade. N-type conduction was found in all sets of NWFETs with hole mobility between 110 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 169 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Molecular electronics provides another means to extend Moore's Law beyond the foreseeable physical limit with the most distinctive advantage being the self-assembly capability which allows device integration at unprecedented levels through specific intermolecule interactions. Second part of this work focused on electrical properties of CNT-PNA-CNT conjugate in the hope of bringing the super fine electrical and mechanical qualities of single walled carbon nanotubes together with the self-assembly capabilities of PNA as a possible device platform for future electronics. In electrical characterization of the conjugate, NDR effect was observed consistently among a number of devices which meets with simulation results reported earlier. The proposed mechanism for the phenomenon is explained in similarity to that works in resonant tunneling diode (RTD) in which decrease in conduction current is attributed to the misalignment between resonance state within the potential barriers and source Fermi level. Though a number of issues remains that either needs to be solved, explained or deserves further study, the unique electrical characteristic of CNT-PNA-CNT conjugate has been clearly demonstrated.

The drive for continuous advancement of nanotechnology has never diminished, however daunting each technology node seemed technologically, solutions had always been found even though each step forward is now accompanied with much more effort. There is no

doubt another solution(s) will be found to overcome the physical limit predicted by Moore's Law in the years to come, whether it being nanowire, molecular conjugates or carbon electronics. Even though there is no guarantee that either nanowire based electronics or CNT-PNA-CNT conjugate would practically be used anytime soon, the significance of this work lies in the fact that this is one the very few systematic works on InSb nanowire based devices and the first on exploiting electrical properties of CNT-PNA-CNT conjugate to our knowledge, both works provides experimental references and theoretical basis for future works on nanowire based electronics and PNA based molecular electronics.

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