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Novel Nanocrystal Floating Gate Memory

A Dissertation submitted in partial satisfaction
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Electrical Engineering

by

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I would also like to thank my lab mates for providing the nice laboratory environment.

This thesis is dedicated to my family.

ABSTRACT OF THE DISSERTATION

Novel Nanocrystal Floating Gate Memory

by

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Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, June 2012
Dr. Jianlin Liu, Chairperson

This work is devoted to investigating the feasibility of engineering nanocrystals and tunnel oxide layer with a novel structure. Several novel devices are demonstrated to improve the performance of the novel nanocrystal memories.

A novel $TiSi_2$ nanocrystal memory was demonstrated. $TiSi_2$ nanocrystals were synthesized on SiO_2 by annealing Ti covered Si nanocrystals. Compared to the reference Si nanocrystal memory, both experiment and simulation results show that $TiSi_2$ nanocrystal memory exhibits larger memory window, faster writing and erasing, and longer retention lifetime as a result of the metallic property of the silicide nanocrystals.

Due to thermally stable, CMOS compatible properties, $TiSi_2$ nanocrystals are highly promising for nonvolatile memory device application.

Metal/high-k dielectric core-shell nanocrystal memory capacitors were proposed. This kind of MOS memory shows good performance in charge storage capacity, programming and erasing speed. A self-assembled di-block co-polymer is used to align the NCs to improve the scalability of the overall sample.

An ordered Co/Al_2O_3 core-shell nanocrystal (NC) nonvolatile memory device was also fabricated. Self-assembled di-block co-polymer process aligned the NCs with uniform size. Co/Al_2O_3 core-shell NCs were formed using atomic layer deposition of Al_2O_3 before and after the ordered Co NC formation. Compared to Co NC memory, Co/Al_2O_3 core-shell NC memory shows improved retention performance without sacrificing writing and erasing speeds.

Another new discrete NiSi nanocrystals (NCs) were synthesized by rapid thermal oxygen annealing (RTO) of very thin Si/Ni/Si films on SiO_2 tunneling layer. The RTO process resulted in smooth surface of the NC floating layer, in turn, uniform thickness of subsequent control oxide layer. Metal-oxide-semiconductor capacitor memory was fabricated. Electrical properties of the memory device such as programming, erasing and retention were characterized and good performance was achieved, which is due to the reduction of the leakage paths in the smooth device structure.

Therefore, it is concluded that metallic nanocrystal with aligned core-shell structure memory is a very promising candidate to replace Si nanocrystal for future generation nonvolatile flash memory devices.

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1. Chapter 1: Introduction

1.1 Status of current flash memory devices

1.1.1 Classification of memory

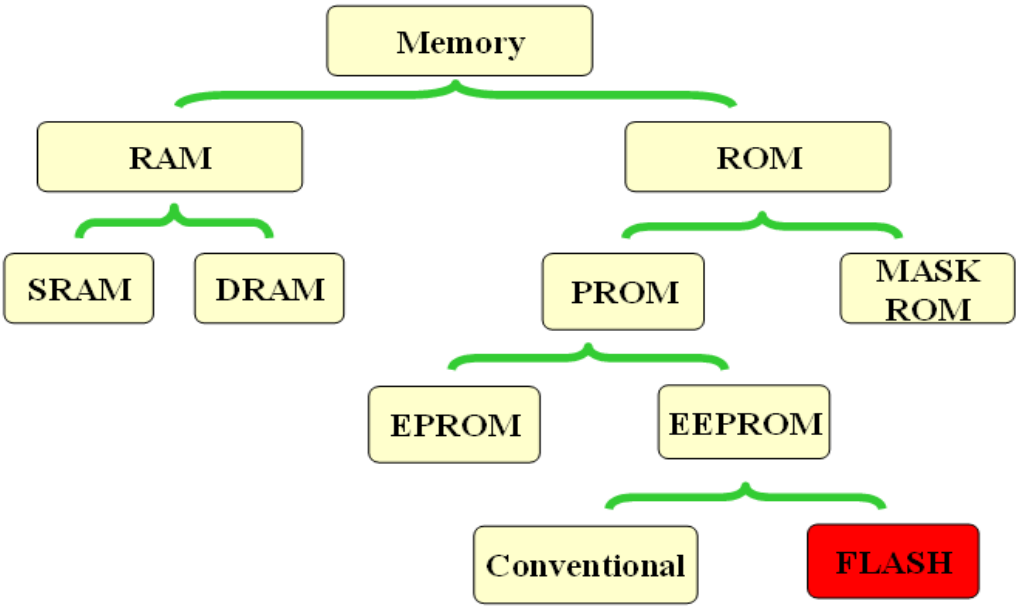

Fig. 1.1 Classification of memory

Memory is one of the key components in computer. It is used for data and information storage.

Based on the properties, it could be classified to two classes: Read Only Memory (ROM) and Random Access Memory (RAM), which include Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) [1-2]

. ROM includes MASK ROM and programmable ROM (PROM) which can be separated to Erasable Programmable ROM (EPROM), Electrically Erasable Programmable ROM (EEPROM) [3-6]. The image of classification of memory is shown in Fig. 1.1.

Flash memory was developed from EEPROM and it is a non-volatile storage memory cell which can be electrically erased and reprogrammed. It (both NOR and NAND types) was invented by Dr. Fujio Masuoka while working for Toshiba circa 1980 [7-8]. Intel found the potential of using the first commercial NOR type flash chip in 1988, which is shown in Fig. 1.2 [9-11]. NOR-based flash allows random access to any memory location.

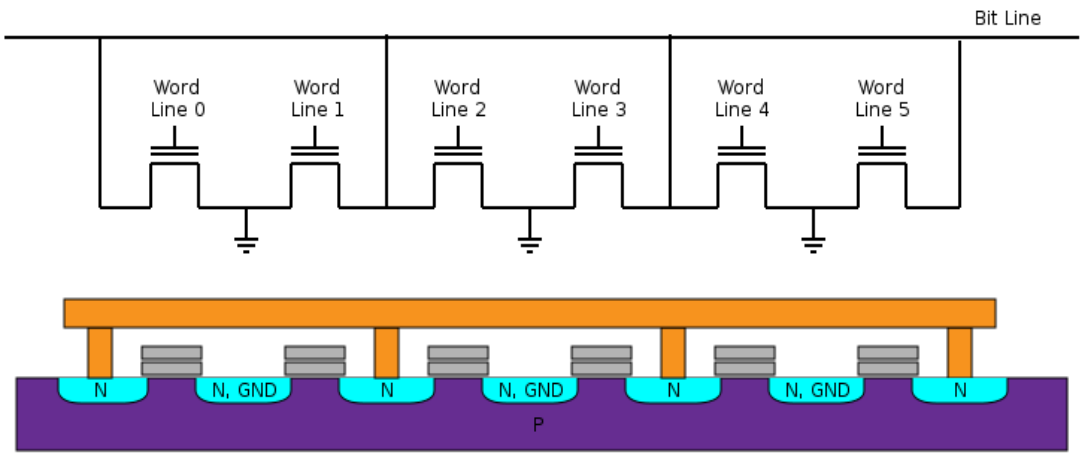

Fig. 1.2 NOR flash layout

Toshiba announced NAND flash at the 1987 International Electron Devices Meeting. It allows greater storage density and lower cost per byte than NOR flash.

However, the NAND flash does not provide a random-access to each bit, which is shown in Fig. 1.3 [12].

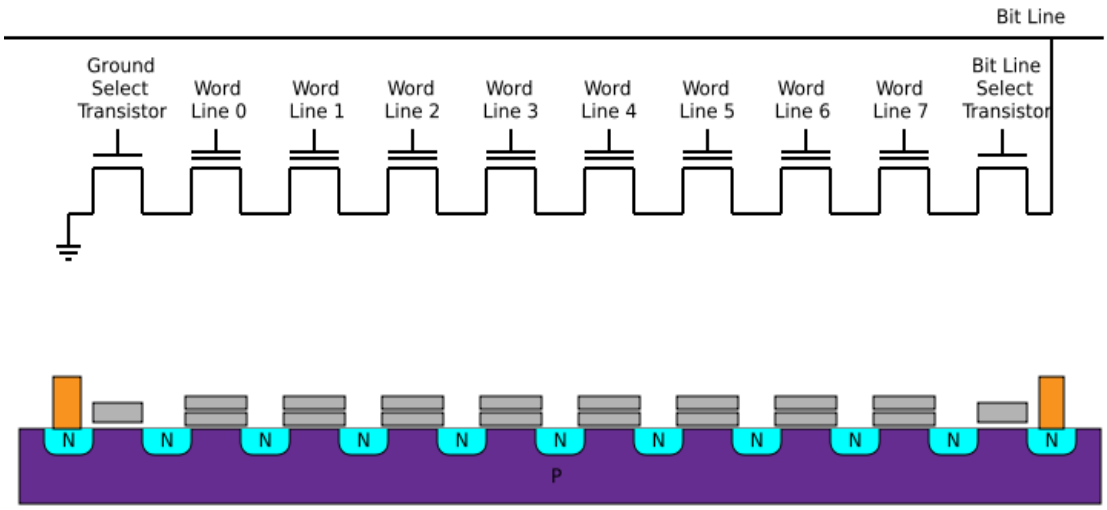

Fig. 1.3 NAND flash structure

1.1.2 Si-based nonvolatile flash memory

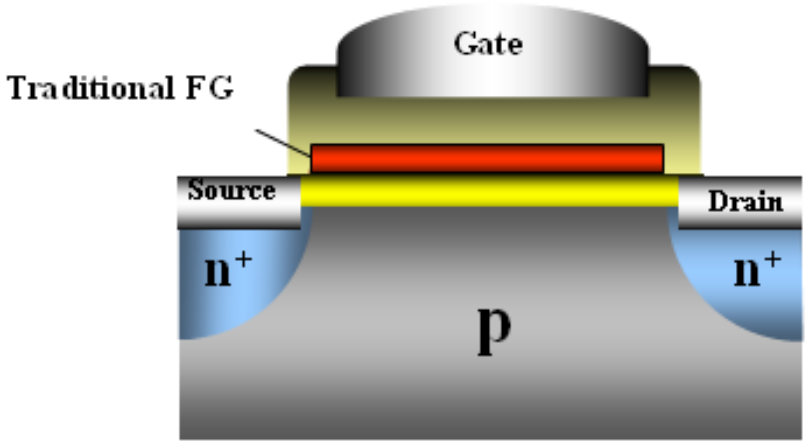

Fig. 1.4 Diagram of conventional floating gate memory

In floating gate flash memory, each memory cell includes a standard MOSFET, except that the transistor has two oxide layers separated by Si. Top one is the control gate. Below the control gate, there is a floating gate insulated by the oxide layers. The electrons trapped in the floating gate would be stored for several years because the floating gate is isolated by insulated oxide layer. Underneath the floating gate, it's tunnel oxide. Si wafer is used as substrate for the flash memory cells [13-15]. The diagram is shown in Fig. 1.4.

When no charges are stored inside the FG and reading, a voltage is applied to the control gate, the channel's conductivity of MOSFET is tested and threshold voltages (V_t) is determined. After the memory device is programmed, the floating gate holds a charge, it screens (partially cancels) the electric field from the control gate, which modifies V_t. When reading, a different voltage is applied to the control gate, the channel's conductivity of MOSFET is tested and new V_t is determined, which is influenced by the charge stored in floating gate. The memory device under uncharged and charged status, testing drain

current changes with gate voltage (I_d~V_g) curves are shown in the Fig. 1.5. The shift of threshold voltage would show the charge storage in floating gate and the reading from drain side would indicate the stored information as “0” state or “1” state.

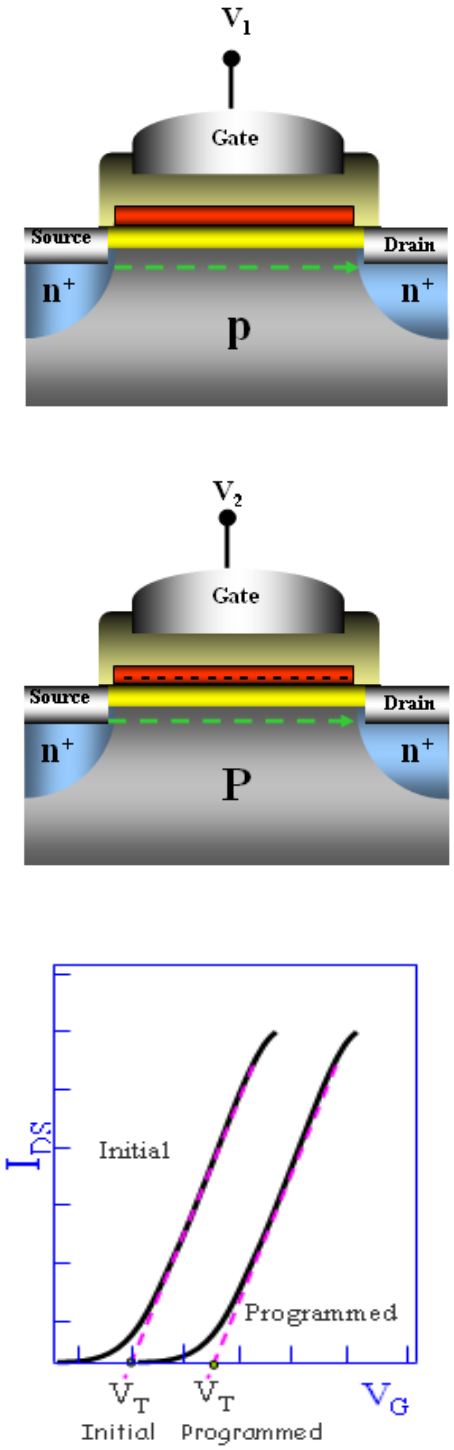

Fig. 1.5 The charged and uncharged status of the memory device and I_d~V_g curve for the two status

When positive voltage is applied on control gate of n channel MOSFET memory, electrons in the substrate go through the tunnel oxide layer and arrive the floating gate, which indicates the charge writing process. When negative bias is applied on the control gate of the device, electrons would be erased from the floating gate, which indicates the charge erasing process. The diagram of the operation of the programming and erasing states is shown in Fig. 1.6 [16-20].

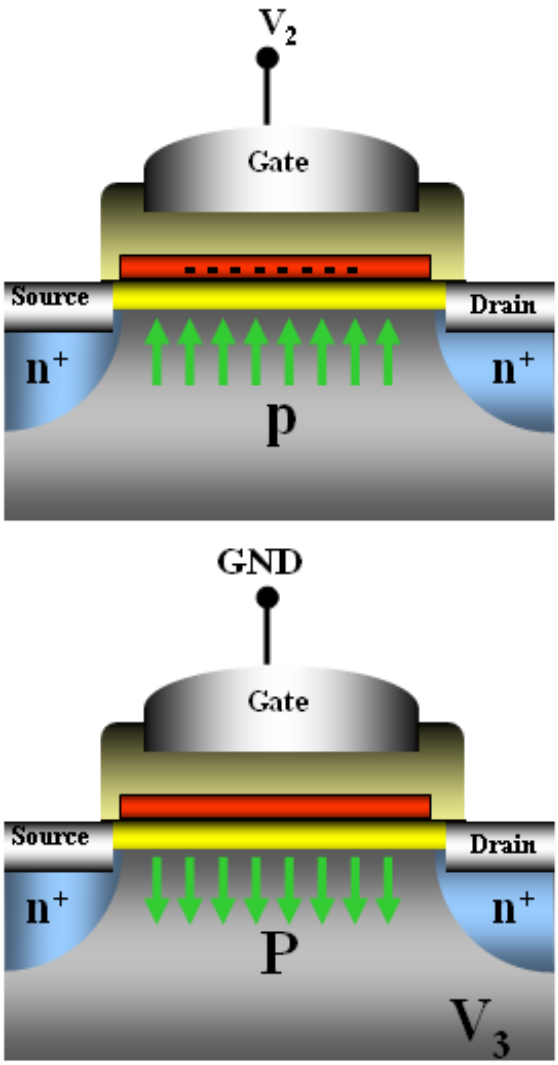

Fig. 1.6 The diagram of the operation of the programming and erasing states

1.1.3 Nanocrystal floating gate memory

In continuous scaling of device structure, thinner tunneling oxide degrades the storage time of electrons and it is the most prominent problem of poly-Si floating gate

memory. To improve the performance of nonvolatile memory, discrete floating gate memory devices have attracted much attention. By using discrete nodes for charge storage such as nanocrystals, it would enable thinner oxide with faster writing and erasing speed and longer retention time [21-23]. The device structure of nanocrystal floating gate memory is shown in Fig. 1.7.

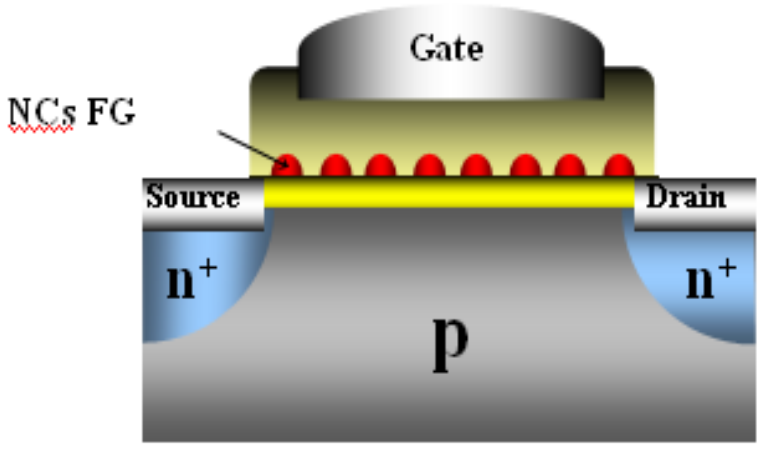

Fig. 1.7 Device structure of nanocrystal memory

Compared with conventional floating gate memory, discrete floating gate memory would hold the charge longer even if some certain defect levels exist in tunnel oxide layer. The diagram of the leakage for conventional floating gate memory and nanocrystal floating gate memory is shown in Fig. 1.8. It is evident that, in conventional floating gate memory, once a leakage path between the floating gate and substrate exists, the charges in the floating gate would keep leaking from the mobile of the electrons in the floating gate. However, in nanocrystal floating gate memory, even if a leakage path exists

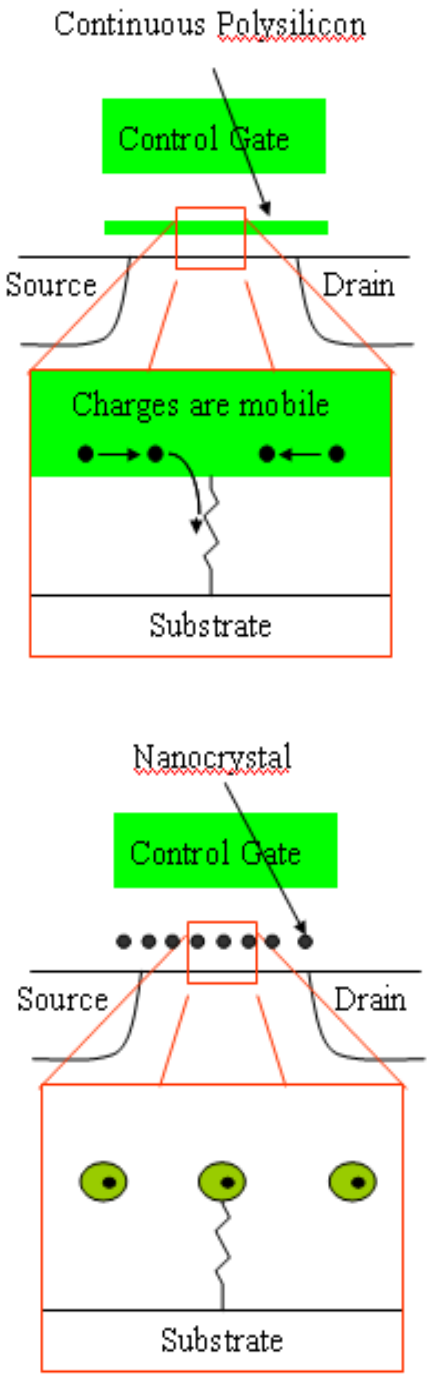

Fig. 1.8 The diagram of leakage for conventional floating gate memory and nanocrystal floating gate memory

somewhere, only the charges close to the path are easy to leak. For electrons far away from the leakage path, they are trapped in the discrete nanocrystal nodes and are hard to be lost. Thus, the retention performance is improved.

1.1.4 Status of current nanocrystal memory devices

Many researchers work on the nanocrystal floating gate memory to improve the performance of the device. The researches fall into two groups: One is tunnel barrier engineering, the other one is work function engineering.

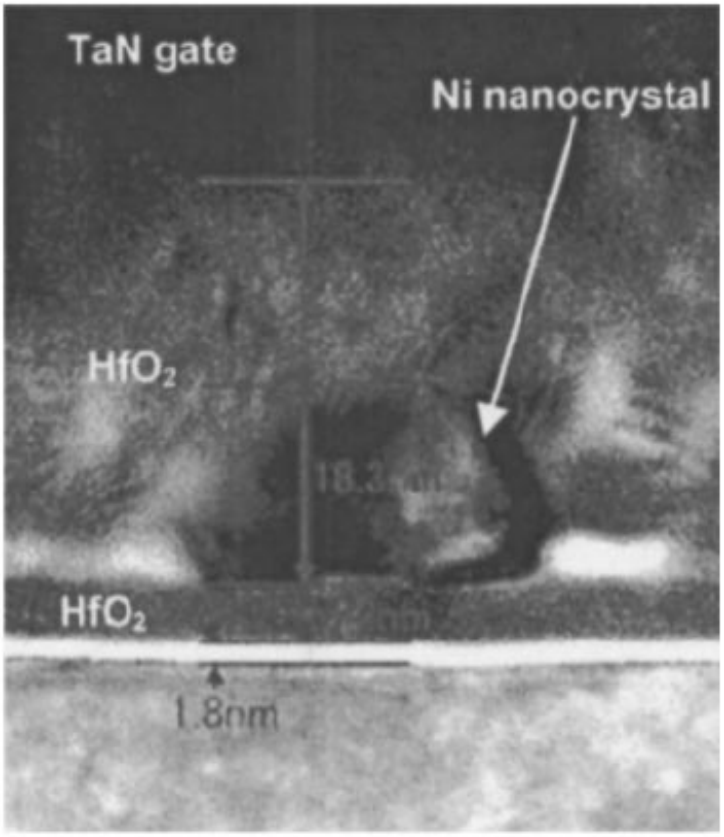

Fig. 1.9 TEM picture of the nickel nanocrystal in HfO_2 [24].

In tunnel barrier engineering, high-k material is used to substitute conventional SiO_2 to prevent the leakage of electrons. Al_2O_3, HfO_2 and related high-k materials are used either in the tunneling layer or in the control oxide layer [25-27]. Fig. 1.9 shows TEM image of Ni nanocrystals embedded in specific HfO_2 layer.

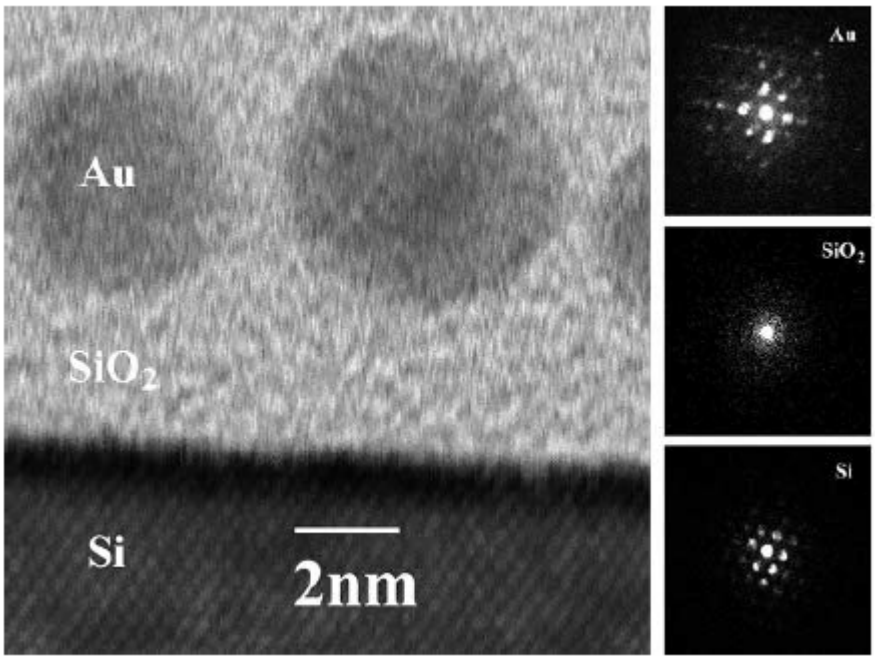

Fig. 1.10 A STEM bright-field cross-sectional image of Au nanocrystals embedded in SiO_2 and CBED patterns of a single Au nanocrystal, the gate oxide, and the Si substrate. The Au nanocrystals are formed by 1.2-nm Au evaporation followed by RTA at 575°C for 10 sec [29].

In work function engineering, different nanocrystals are used to improve the performance [28-30]. One of the proposals is to choose certain work function metallic material which is lower than the work function of Si to increase the depth of the tunneling barrier and finally the retention performance of the nanocrystal memory would be improved. Different materials such as metal, silicide and even hetero-structure nanocrystals are embedded into floating gate memory to prolong the retention performance. Fig. 1.10 shows TEM image of using Au nanocrystals embedded in SiO_2 layer.

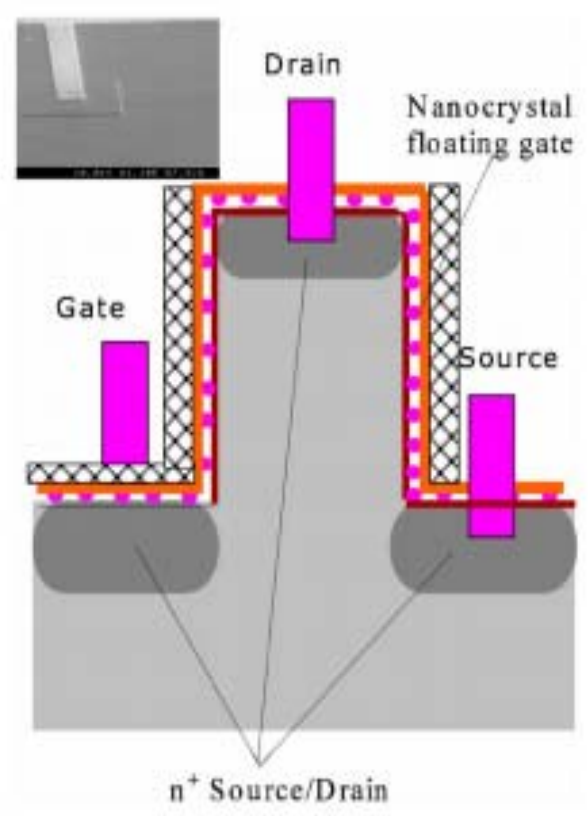

Fig. 1.11 Schematic side view of vertical flash transistor and isometric scanning electron micrograph of a fabricated device (inset) showing the mesa with drain contact on its top and the polysilicon gate contact running to the right[31].

Some vertical structures for nanocrystal memories as gate-all-around NC flash memory are also fabricated to improve the performance. Fig. 1.11 shows the structure of vertical nanocrystal floating gate memory [31].

.

1.2 Outline

1.2.1 Simulation and experiment for metal silicide nanocrystal MOSFET structure

Hetero-dot floating gate memory is proposed here to improve the performance of the nanocrystal memory device. $TiSi_2$ coated Si hetero-nanocrystals form extra quantum well between control oxide and Si nanocrystals. Charges would likely to be stored in $TiSi_2$ well and the additional barrier between Si dot and coated $TiSi_2$ provide an extra protection to the electrons from leakage. The TiS_2 coated Si nanocrystals are fabricated by using self-aligned silicide (salicide) technique. This salicide technique has been widely used in semiconductor industry to form good ohmic contact between metal and Si without any additional masks and it is CMOS compatible process. The device structure and band structure of a $TiSi_2$ coated Si nanocrystal memory cell is shown in Fig. 1.12 [33-34].

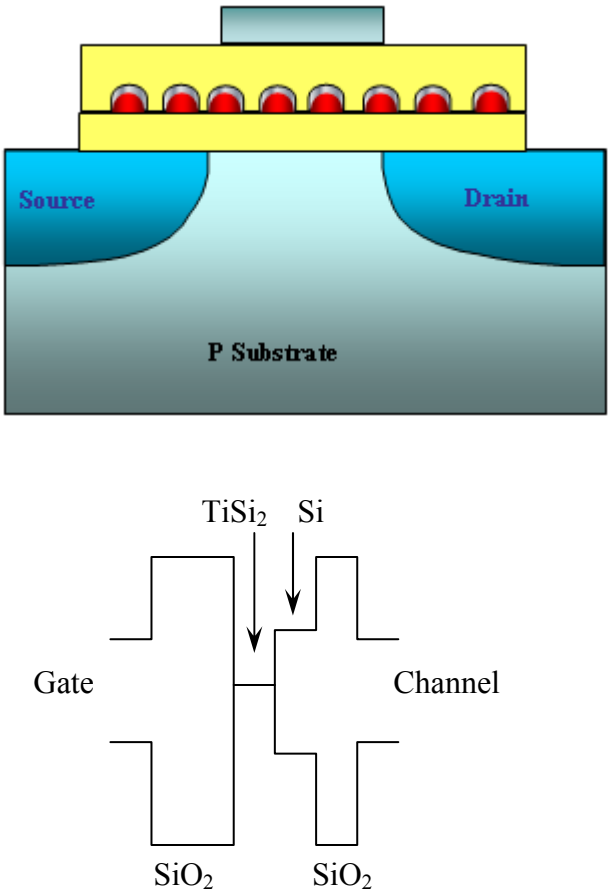

Fig. 1.12 The device structure and energy band structure of the memory with $TiSi_2$ coated Si nanocrystals.

Work function engineering is one of promising approaches to improve the performance of nanocrystal floating gate MOSFET memory. This approach is to engineer the depth of the potential well at the storage nodes by choosing floating gate material with proper work function. The work function of selected metallic material is larger than the electron affinity of Si, which leads to reduced leakage current through the tunneling barrier due to an increased barrier height. Figure 1.13 shows the comparison of the conduction band diagram of Si NC memory and specific metallic (Co) NC memory. In

Fig. 1.13 (b), charges are confined in a deeper quantum well comparing to Fig. 1.13 (a), which improves the retention performance.

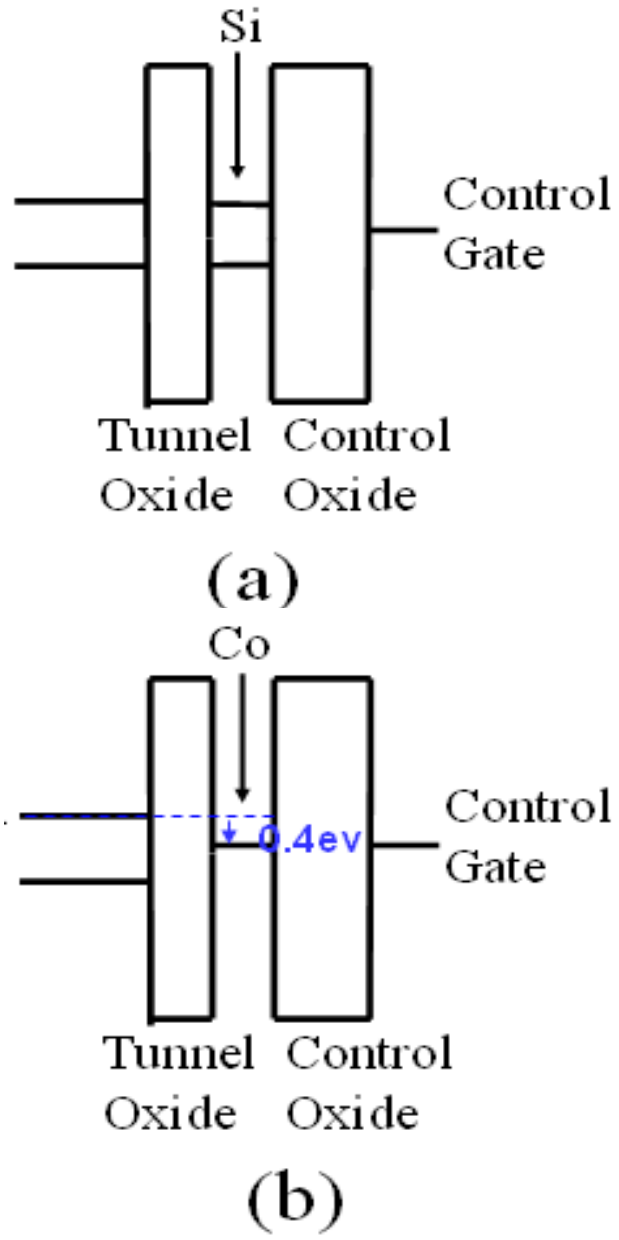

Fig. 1.13 Band diagram for (a) Si nanocrystal memory (b) Co nanocrystal memory

1.2.2 Core-shell dot structure

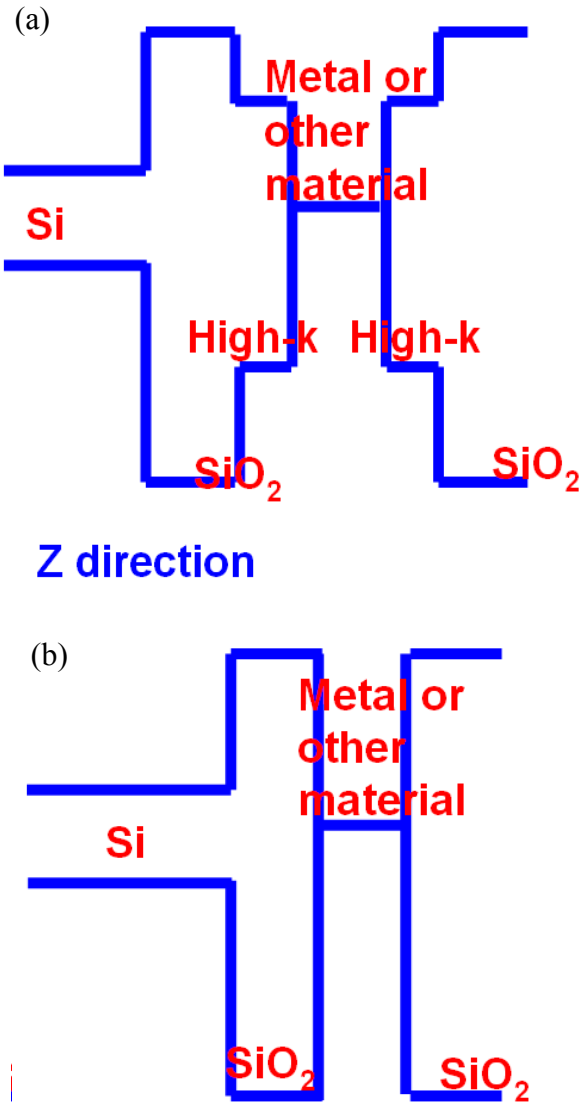

Fig. 1.14 Band diagram for (a) core-shell nanocrystal memory and (b) normal nanocrystal memory

Another approach to improve the NVM device performance is through tunneling barrier engineering. In this study, we employed core-shell structure with a thin high-k

layer as the shell of metal-core to supply an additional barrier, which prevents the charge leakage and improves the retention performance. Fig. 1. 14 shows the band diagram for core-shell NC memory and normal nanocrystal memory.

In the device, normally metallic NC is used as storage node and the charge storage is considered as electron storage. Fig. 1.15 shows the band diagram for core-shell NC memory in operation and retention states. In Fig. 1.15 (a), the band diagram for the structure is in writing state. During the programming, inversion layer is formed at the Si/SiO_2 interface and electrons tunnel through SiO_2 layer to NCs. The conduction band offset of Si/SiO_2 is important in the programming states (the electron path is drawn in blue). In erasing, electrons tunnel back to substrate and the conduction band offset of metallic/high-k and high-k SiO_2 is again important. If we consider that some holes would be erased from Si to metallic NCs and neutralize the electrons in NCs, VBO between SiO_2 and high-k material would be important. The hole tunneling process is drawn in red in Fig. 1.15 (b). In retention, electrons are trapped in the quantum well and the quantum barriers are formed by the edge of conduction energy band, so two additional barriers provided by high-k shell layer improve the retention performance.

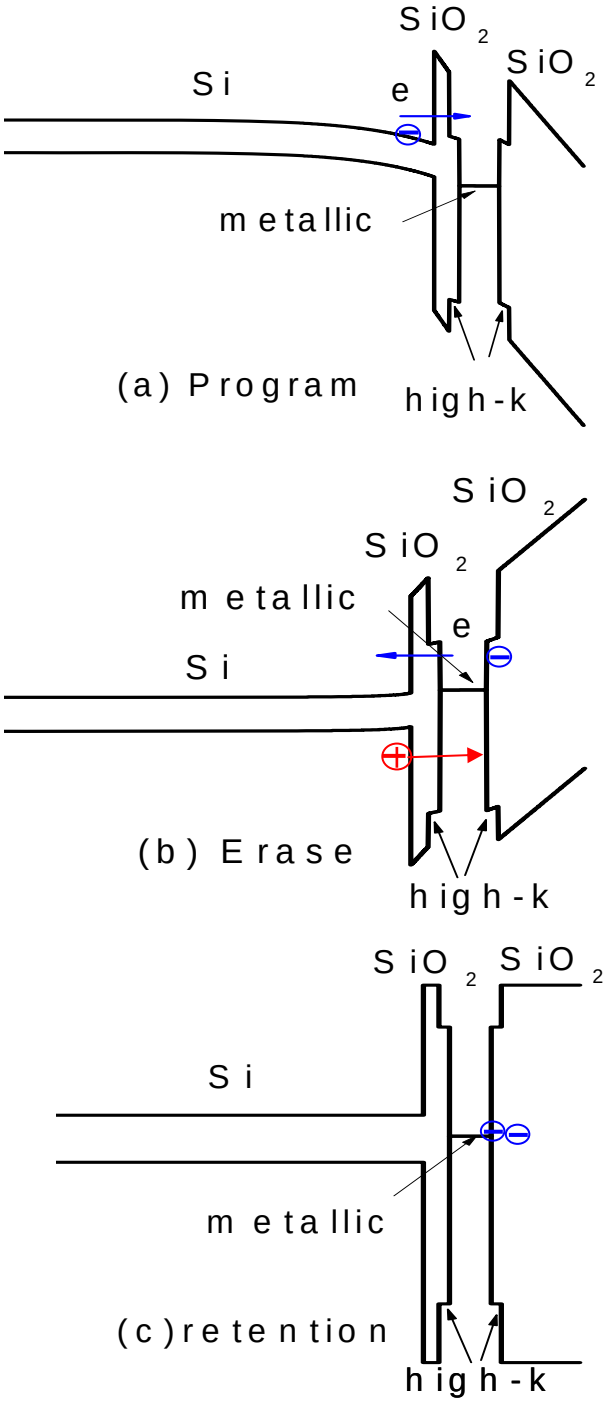

Fig . 1.15 Band diagram for core-shell structure memory in operation and retention states

1.2.3 Aligned core shell dot structure

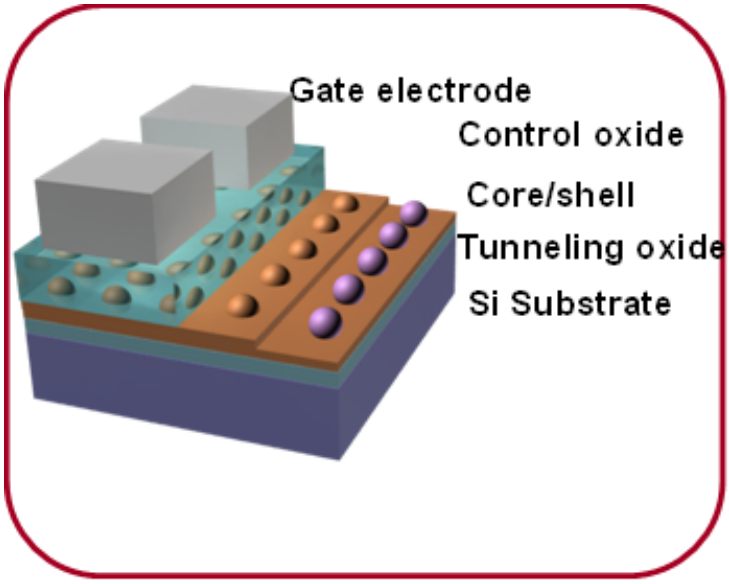

Fig. 1.16 The device structure of aligned core-shell nanocrystal memory.

Nanocrystal floating gate memory has the potential to use thinner tunnel oxide without sacrificing write/erase speed. It has great potential in device performance improvement. However, limited control on nanocrystal size and distribution impacts the device performance, scalability and manufacturability [35]. Many kinds of different ways for the nano particle fabrication were made by people to align the nano particles in an ordered way such as Electron-beam lithography [36], Bio Nano Process (BNP) [37], Template [38] and etc. Here we report our results about spin coating nano particles. In this way, semiconductor and metal nano particles of the length scale <10 nm can be

chemically synthesized with precise control of the size. It's promising in the MOSFET memory device application.

Uniformly distributed NCs are also promising for improving device performance and scalability. The device structure of aligned core-shell nanocrystal memory is shown in Fig. 1.16. The NCs are proposed to be assembled within co-polymer-based template. The uniform distribution throughout the sample is more important for device reliability and manufacturability.

1.2.4 Motivation of this research

The motivation of this work is to demonstrate high performance non volatile floating gate memory and reveal physical mechanism of the nanocrystal memory in programming/erasing and retention for future nanocrystal-based nonvolatile memory.

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Chapter 2: $TiSi_2$ based nanocrystal memory

2.1 Performance enhancement of $TiSi_2$ coated Si nanocrystal memory device

2.1.1 Introduction

The dimensions of Si based memory devices have approached the nanometer scale and Si nanocrystal embedded memory devices have significantly improved the performance of floating gate memory [1]. It was reported that the defects in Si nanocrystals boost up the long-term retention performance [2]. However, the defects based performance improvement is not stable in MOSFET memory device fabrication, in particular under subsequent high temperature annealing step [2]. New types of nanocrystal floating dots, such as double Si dots [3], Ge nanocrystals [4], metal [5-8] or metal-like [9] dots and dielectric nanocrystals (Al_2O_3, HfO_2, Si_4N_3, etc) [10-12], have been proposed to achieve memory devices with longer and stable retention performance. The higher defect levels in the dielectric materials require higher writing voltage, therefore inducing the erasing saturation [13]. A feasible solution to rule out the defect effect is to use nanocrystals with high density of states, such as metal nanocrystals [5-8], but the drawback of using Ge and metal nanocrystals is the inter-diffusion between nanocrystals and tunnel oxide during device integration [14-16]. The inter-diffusion degrades the tunnel oxide and worsens retention characteristics. Since the post annealing is necessary for most of the device process, the thermal stability of a memory cell has become very critical. In this work we proposed and experimentally verified a method to

improve the thermal stability of the memory cell by using self aligned $TiSi_2$ coated Si nanocrystals technique. $TiSi_2$ coated Si nanocrystal memory can not only have faster writing/erasing speed, but also have longer retention performance than pure Si nanocrystal memory as a result of Fermi-level pinning effect and high density of states around the silicide.

2.1.2 Experiment

In device fabrication, first, 5 nm thermal oxide was grown in dry oxygen immediately followed by Si nanocrystal deposition. An ultra-thin (<0.5 nm) blanket Ti layer was then deposited. A modified two-step annealing for silicidation [17] was performed in nitrogen to coat the Si nanocrystals. The first annealing only forms silicide on Si nanocrystal and Ti on oxide remains as metal. After selectively removing the unreacted metal Ti, the wafer was annealed (second annealing) at 900 ^{o}C for 30 seconds to form thermally stable Si-rich silicide [18]. Control oxide of about 15 nm was then deposited, followed by a 350-nm-thick poly-silicon deposition in Low Pressure Chemical Vapor Deposition (LPCVD). After the formation of gate pattern, the poly-silicon gate and source/drain regions were implanted with phosphorus followed by dopant activation.

2.1.3 Results and discussion

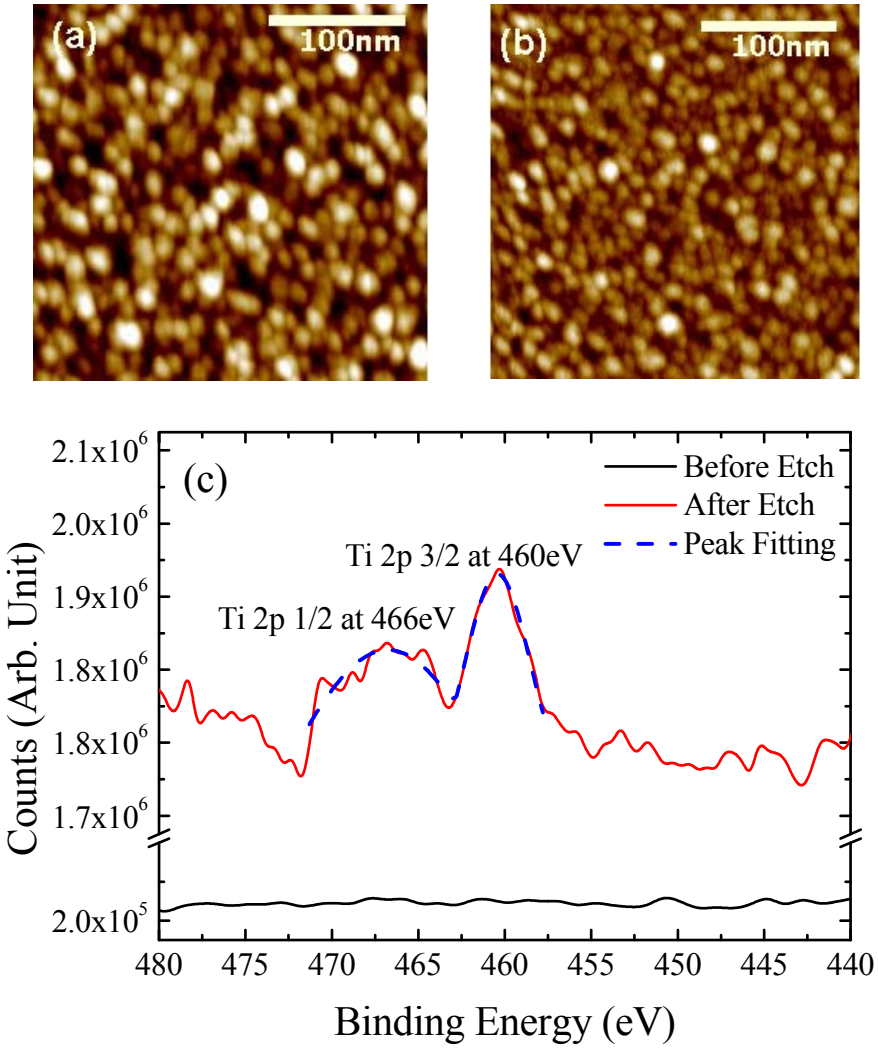

Fig. 2.1.1 AFM images of the $TiSi_2$ coated Si nanocrystals a) before and b) after diluted HF etching c) XPS result of the $TiSi_2$ coated Si nanocrystal sample before and after diluted HF etching

Figure 2.1.1 (a) and (b) show the atomic force microscope (AFM) images of $TiSi_2$ coated Si nanocrystals before and after HF etching, respectively. The nanocrystal diameter is ~ 10 nm and the density is ~ 5×10^{11} cm^{-2}. The Si nanocrystals still exist after

diluted HF etching, which indicates the fact that thin layer of Ti silicide has formed on the surface of the Si nanocrystals. Fig. 2.1.1(c) shows the results of X-ray photoelectron spectroscopy (XPS) of the same samples before and after HF etching. For the as-fabricated nanocrystal sample, there is one evident peak at 460 eV corresponding to Ti 2P3/2 states of $TiSi_2$. This Ti-related signal disappears after HF etching, which means the $TiSi_2$ portions of the nanocrystals were removed. The combination of AFM and XPS results suggests that $TiSi_2$ coated Si nanocrystals have been achieved.

To verify the details of coated shape of the nanocrystals, simple calculation was performed. A half circle shape of Si nanocrystal with height of 8nm and diameter of 16nm was proposed to deposit on SiO_2, as shown in Fig. 2.1.2 (a). Silicide process is suppressed by stress between SiO_2 and Si [19], here we assume the stress σ decreases as it is away from SiO_2: $\sigma_{nn} = Ae^{\frac{B}{n^2}}$.

Combining the concentration differential equation and stress related equation [20], the thickness of $TiSi_2$ is given by

$$\delta(THK) = \frac{\Delta t \times C \times k_s}{N_1}, \qquad k_s = k_{s0} \exp\left(-\frac{E_{k0} + \sigma_{nn} * V_{kp}}{k * T}\right)$$

Where Δt is the annealing time, C is the concentration of elements, K_S is the reaction rate, N_1 is the number of silicon atoms penetrating to the silicide layer,

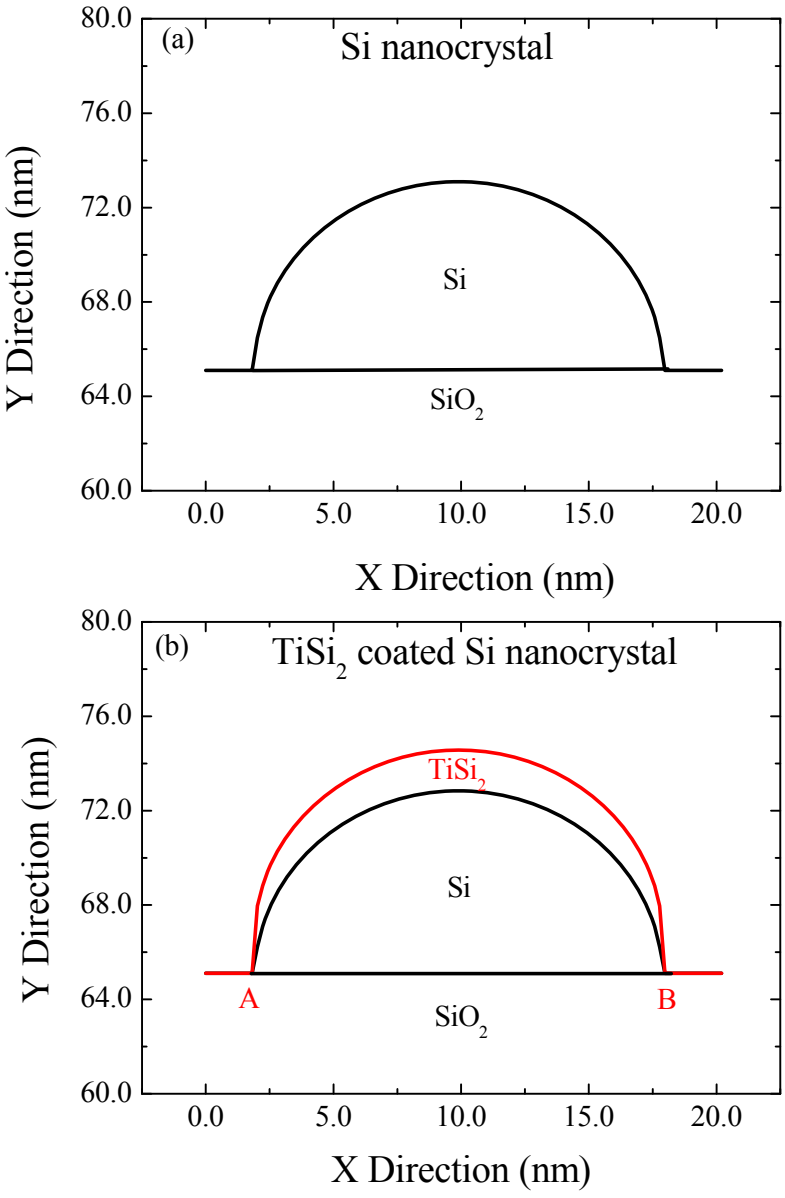

Fig. 2.1.2 a) Nanocrystal structure in the beginning of calculation, b) $TiSi_2$ signal distribution in 2D.

K_{S0}, E_{K0}, V_{KP} are parameters of the model. Fig 2.1.2 (b) shows the 2 dimensional (2D) picture of $TiSi_2$ distribution in this structure. Si shows higher diffusion rate when it is away from the interface between Si and SiO_2. While at the edge of Si nanocrystal, slower diffusion rate results in the crescent shape of the coated $TiSi_2$.

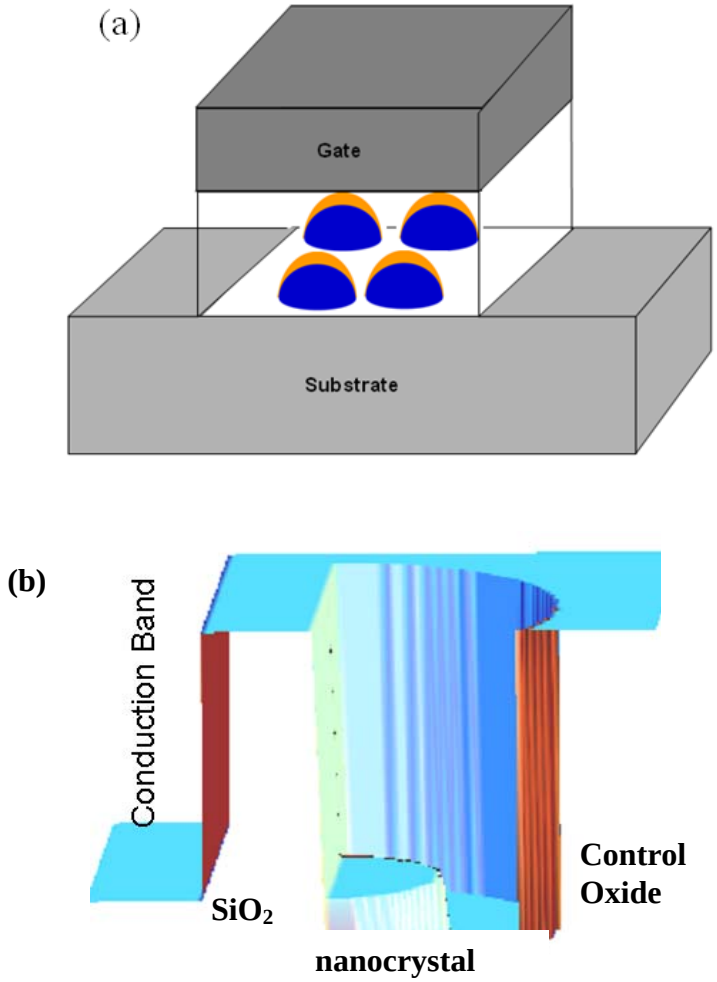

Fig. 2.1.3 (a) Schematic of $TiSi_2$ coated Si nanocrystal memory device, (b) Schematic of 3D conduction band structure of $TiSi_2$ coated Si nanocrystal memory device.

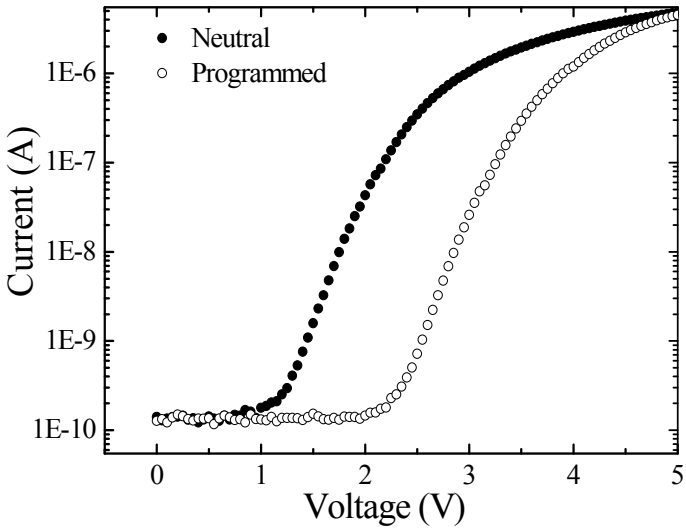

Fig. 2.1.4 Memory effect from $TiSi_2$ coated Si nanocrystal memory cell. The shift of I_{ds}-V_g curve after writing operation indicates the electron storage in the floating gate.

Figure 2.1.3(a) shows the schematic of $TiSi_2$ coated Si nanocrystal memory device. The blue color shows the Si nanocrystal and the orange ring covering the surface of Si nanocrystals represents $TiSi_2$ layer. Fig. 2.1.3(b) shows the 3D conduction band of $TiSi_2$ coated Si nanocrystal memory device. $TiSi_2$ layer which has lower energy level attaches the tunnel oxide and exists between control oxide and Si nanocrystals. Under writing, the electrons from Si substrate go through the tunnel oxide, Si nanocrystal and finally are confined in the $TiSi_2$ region.

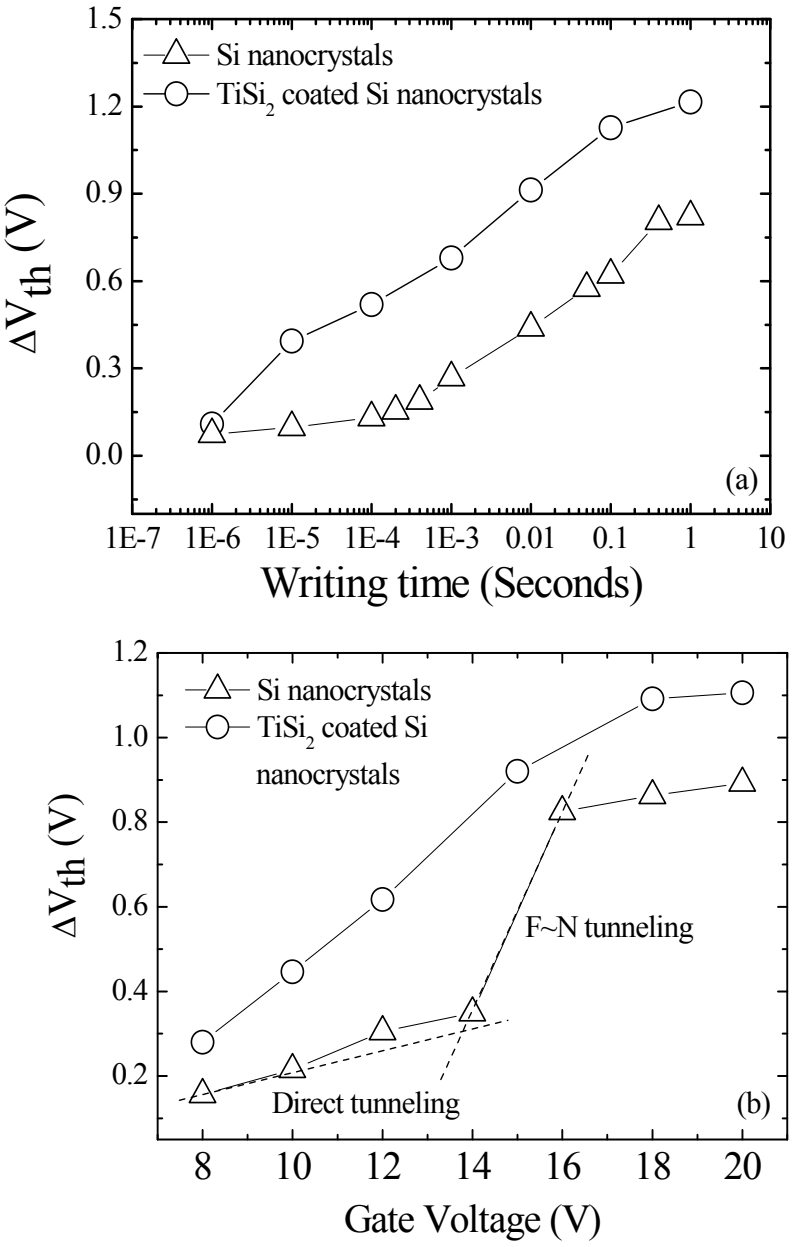

Fig. 2.1.5 Threshold voltage shift as a function of a) writing time and b) writing voltage, for memory cells with $TiSi_2$ coated Si nanocrystals and reference Si nanocrystals.

The devices were characterized by HP 4155A semiconductor analyzer and Agilent LCR meter at room temperature. Memory effect was clearly found for the memory device with $TiSi_2$ coated Si nanocrystals, as shown in Fig. 2.1.4, where the source-drain current (I_{ds}) as a function of gate voltage (Vg) is shown for the neutral state and programmed state, respectively. The programming was performed at 20 V for 1 s. The shift (~1.2 V) of the I-V curve towards higher gate voltage indicates the electron storage in the nanocrystals.

The threshold voltage shift as a function of writing time and writing voltage is shown in Fig. 2.1.5 (a) and Fig. 2.1.5 (b), respectively. It is found that the memory window becomes saturated as the writing time elapses with Vg fixed at 15 V. This is due to the Coulomb blockade effect caused by the small nanocrystal size. The saturated memory window for the device with $TiSi_2$ coated Si nanocrystals is higher than the Si nanocrystal memory device. The saturation level increases with writing voltage which is shown in Fig. 2.1.5 (b). It is interesting to note in Fig. 2.1.5 (b) that the threshold voltage shift exhibits an obvious difference between $TiSi_2$ coated Si nanocrystal and Si nanocrystal memory devices. This is attributed to the different charge injection mechanisms in the two kinds of devices. In $TiSi_2$ coated Si nanocrystal case, $TiSi_2$ layer attaches the tunnel oxide and has lower energy level compared to the reference Si nanocrystals. The charge injection has already established through Fowler–Nordheim (F-N) tunneling at the voltage around 8V. $TiSi_2$ coated Si nanocrystals have more charges to be stored in the silicide because of its higher density of state (DOS). In Si nanocrystals, the energy levels are higher than that of $TiSi_2$ layer and the tunneling is direct tunneling at

the voltage below 14V and F-N type at the voltage larger than 14V. As writing voltage increases further (>16 V), both devices become saturated.

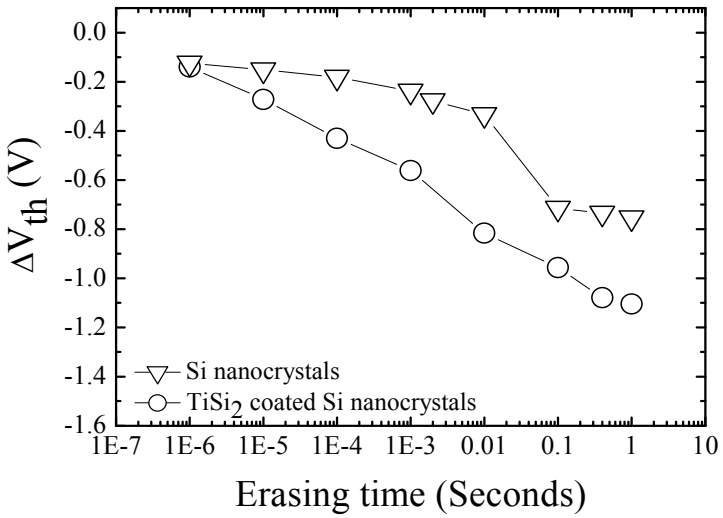

Fig. 2.1.6 Threshold voltage shift as a function of erasing time for memory cells with $TiSi_2$ coated Si nanocrystals and reference Si nanocrystals.

The threshold voltage shift as a function of erasing time at the erasing voltage of -15V is shown in Fig. 2.1.6. The erasing is found speeding up with the increase of the erasing time in both samples. $TiSi_2$ coated Si nanocrystal memory shows higher erasing speed. In the $TiSi_2$ coated Si nanocrystal memory device, two factors make the erasing speed faster than the Si nanocrystal case: First, crescent shape of $TiSi_2$ layer makes the point discharge possible in the sharp area of the $TiSi_2$ layer. Second, tunnel oxide endures larger potential drop in the $TiSi_2$ coated Si nanocrystal, which helps electrons to go through by F-N tunneling.

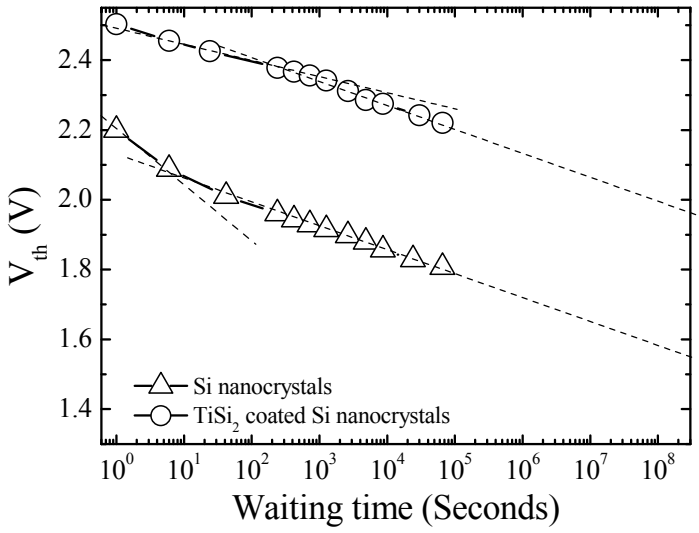

Fig. 2.1.7 Retention performance comparison between a reference Si nanocrystal and $TiSi_2$ coated Si nanocrystal memory devices. The writing was done at 20 V for 1s.

The retention characteristics are shown in Fig. 2.1.7 for the two devices with $TiSi_2$ coated Si nanocrystals and reference Si nanocrystals, respectively. These devices were programmed at 20 V, with an initial memory window of ~1.27V and 0.9V respectively. $TiSi_2$ coated Si nanocrystal memory shows slower charge loss rate in earlier retention stage. In this case, the electrons stay in the $TiSi_2$ channel and most of them have the lower energy level which is difficult to go through the tunnel oxide layer. The other reason is that the interface between the $TiSi_2$ and tunnel oxide has very small area which is blocked by the coulomb blockade effect and results in the difficulty of leakage. After the extrapolation of the curves to 10 years at room temperature, the remaining memory window is predicted to be 0.65 V, which means 52% charge left, while that is only 0.25

V, which means only 28% charges left for the reference Si nanocrystal memory device, as can be seen from Fig. 2.1.7.

2.1.4 Conclusions

In summary, we have successfully fabricated $TiSi_2$ coated Si nanocrystal devices by self-aligned silicidation method. Due to $TiSi_2$ induced lower energy levels, the charge storage occurs mainly in the $TiSi_2$ layer. Therefore, as compared to the reference Si nanocrystal memory, the memory device with $TiSi_2$ coated Si nanocrystals shows a larger charge storage capacity, higher writing and erasing speed and much better retention performance.

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2.2 $TiSi_2$ nanocrystal metal oxide semiconductor field effect transistor memory

2.2.1 Introduction

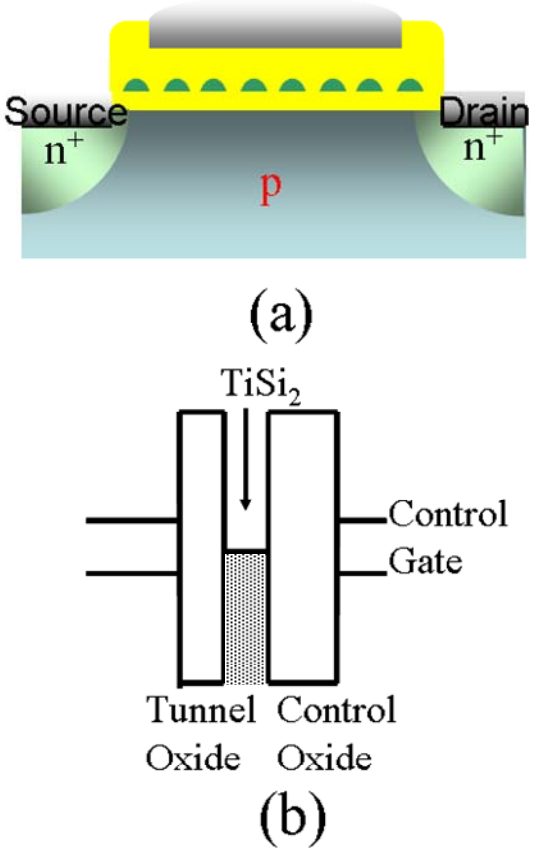

Fig. 2.2.1 (a) schematic cross section of $TiSi_2$ nanocrystal memory device, (b) energy band diagram for $TiSi_2$ nanocrystal memory.

POLY crystalline silicon as a floating gate has been used as a charge storage

material in nonvolatile memory (NVM) for the past three decades [1]. The dimensions of Si based memory devices have approached the nanometer scale and nonvolatile memory utilizing discrete charge storage nodes such as defect traps and Si nanocrystals (NCs) has been considered as a candidate to replace the conventional flash memory [2-3]. It was also reported that the wide distribution of defect related deep levels are associated with the Si nanocrystal memory [4]. Although the existence of these defects in Si nanocrystals results in relatively long retention performance, the defect based performance improvement is not stable in the subsequent high temperature annealing step of metal oxide semiconductor field effect transistor (MOSFET) memory device fabrication [4].

New types of nanocrystal floating dots, such as double Si dots [5], Ge nanocrystals [6], metal [7-10] or metal-like [11] dots and dielectric nanocrystals (Al_2O_3, HfO_2, Si_3N_4, etc) [12-14], have been proposed to achieve memory devices with longer retention performance. Metal nanocrystals are the perfect material to be used as a floating gate to improve the programming speed [15-17]. However, the drawback of using metal nanocrystals is the inter-diffusion between nanocrystals and tunnel oxide during device integration which degrades the tunnel oxide and worsens retention performance [18-20]. Since post annealing is necessary for most of the device process, the thermal stability of such a memory cell has become an issue. In this work we propose and experimentally verify a method to improve the thermal stability of the memory cell by using self aligned $TiSi_2$ nanocrystals.

Figure 2.2.1 (a) and 1 (b) show the cross section schematic and energy band diagram of a $TiSi_2$ nanocrystal memory, respectively. The wide distribution of defect

related deep levels in the forbidden gap of Si associated with Si nanocrystal memory reported in [4,21,22] leads to easy loss of charges during the retention. In contrast, the Fermi level of $TiSi_2$ is within the band gap of Si and 0.6eV below the conduction band edge of Si [23], as shown in Fig. 2.2.1 (b), which significantly prolongs the charge retention. Metallic $TiSi_2$ nanocrystals not only make the devices more stable in the high temperature annealing process during the device fabrication, but also improve the programming speed of the devices, which is proven by the following experiments and simulations.

2.2.2 Experiment

The $TiSi_2$ nanocrystal fabrication process begins with a thermal oxide deposition of about 5nm, which was grown at 850°C. Si nanocrystals were grown at 610°C for 15s with the pressure of 400 mtorr in a low pressure chemical vapor deposition (LPCVD) system. $TiSi_2$ nanocrystals were fabricated with a two-step annealing silicidation method. First a 10-nm-thick metal Ti layer was deposited onto the sample. Then the first annealing was performed in nitrogen at 775°C for 60 s. The unreacted Ti metal on top of nanocrystals as well as in between nanocrystals was removed in selective etchant $NH_4OH:H_2O_2:H_2O$=1:1:5. The second annealing was performed at 880°C for 30 s after the metal removal to form more thermally robust $TiSi_2$ dots. The sample was then capped with control oxide of about 15 nm in a low-temperature oxide CVD furnace. Standard MOSFET process was performed afterwards to form MOSFET memory devices.

2.2.3 Results and discussion

Figures 2.2.2 (a), (b) and (c) show the atomic force microscope (AFM) images of the reference Si nanocrystals, subsequently prepared silicide nanocrystals, and a silicide nanocrystal sample after diluted HF etching, respectively. Both Si nanocrystal density and silicide nanocrystal density are about $5\times10^{11}cm^{-2}$, suggesting excellent self-aligned formation of silicide dots from Si dots. The smooth substrate surface shown in Fig. 2.2.2 (c) indicates that all the silicide nanocrystals were removed by diluted HF. This experiment confirms that all original Si nanocrystals have been converted to silicide nanocrystals during the annealing process. Therefore these nanocrystals are different with our $TiSi_2$/Si heteronanocrystals reported earlier [24]. Further improvement includes more energy levels available in pure silicide nanocrystals over heteronanocrystals, leading to wider memory window and faster programming/erasing speeds. Fig. 2.2.3 (a) shows the result of X-ray photoelectron spectroscopy (XPS) measurement for the silicide nanocrystal

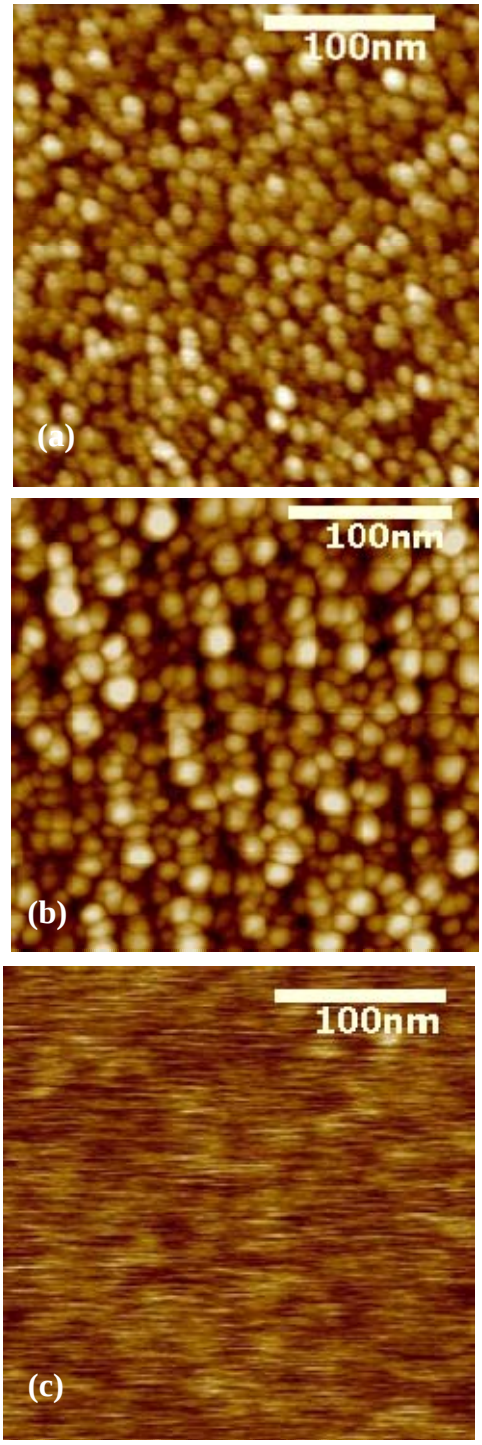

Fig. 2.2.2 AFM images for (a) Si nanocrystals, (b) as-fabricated $TiSi_2$ nanocrystals, (c) $TiSi_2$ nanocrystals after diluted HF etching.

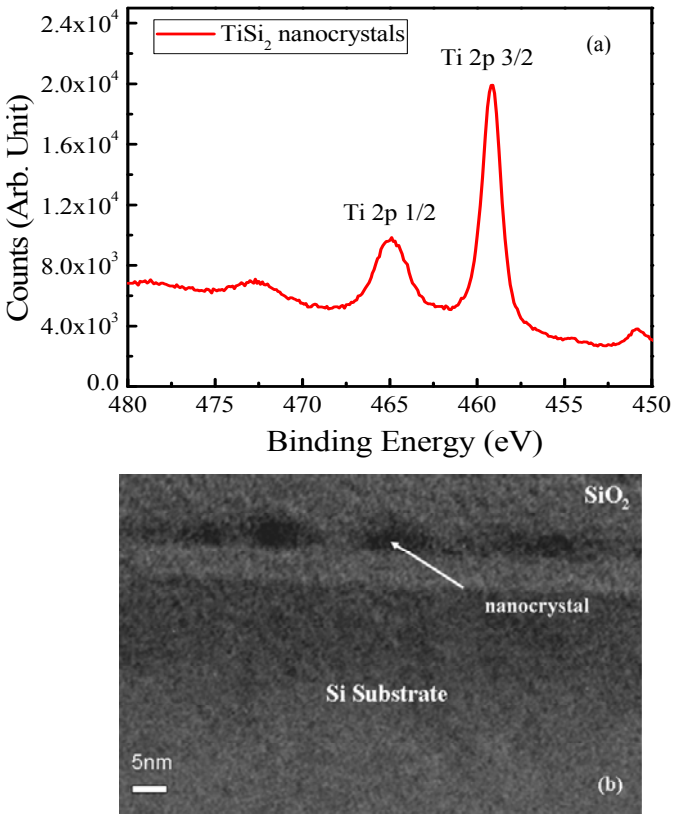

Fig. 2.2.3 (a) XPS for as-fabricated $TiSi_2$ nanocrystals, (b) TEM image for $TiSi_2$ nanocrystals.

sample. One evident peak at ~460eV is corresponding to Ti 2P3/2 states of $TiSi_2$. The combination of AFM and XPS results suggests that $TiSi_2$ nanocrystals have been achieved. Figure 3b shows a typical cross-sectional TEM image of a dedicated $TiSi_2$ nanocrystal device sample. The nanocrystals are of approximate dome shapes. Based on the average of a group of TEM images, the width of nanocrystals are approximately determined to be ~7 nm. The average distance between the nanocrystals is ~5 nm. These values are close to the AFM results, considering the tip effect. The thickness of the tunnel

oxide is ~5 nm and the control oxide is also estimated from these TEM measurements to be ~15 nm, both of which are designed values and consistent with our ellipsometry measurements.

Si nanocrystal and $TiSi_2$ nanocrystal memories were fabricated and characterized. Figure 2.2.4 (a) shows typical high frequency (1MHz) capacitance-voltage (C-V) sweep results for $TiSi_2$ nanocrystal and Si nanocrystal MOS capacitor memories with scanning range between -15V and +15V. The sweep began from inversion region to accumulation region and back to inversion region again. The voltage sweep rate is 0.5V/s. It is found that C-V curves exhibit evident hysteresis with a voltage shift of around 3.1V for $TiSi_2$ nanocrystal memory and 1.1V for Si nanocrystal memory, indicating that $TiSi_2$ nanocrystal memory shows stronger memory effects than that of the Si nanocrystal memory. Fig. 2.2.4 (b) shows the bidirectional C-V sweeps with different scanning range from ±10V to ±15V for $TiSi_2$ nanocrystal MOS capacitor memory. When voltage sweeps from 10 to -10V and back to 10V, a very small flat band voltage shift is observed. When the sweep voltage increases to 12 and 15V, the flat band voltage shift shows larger memory window at 1.5V and 3.1V, respectively. Wider voltage sweep range leads to the fact that more electrons are written/erased from the $TiSi_2$ nanocrystals, therefore larger memory window is achieved.

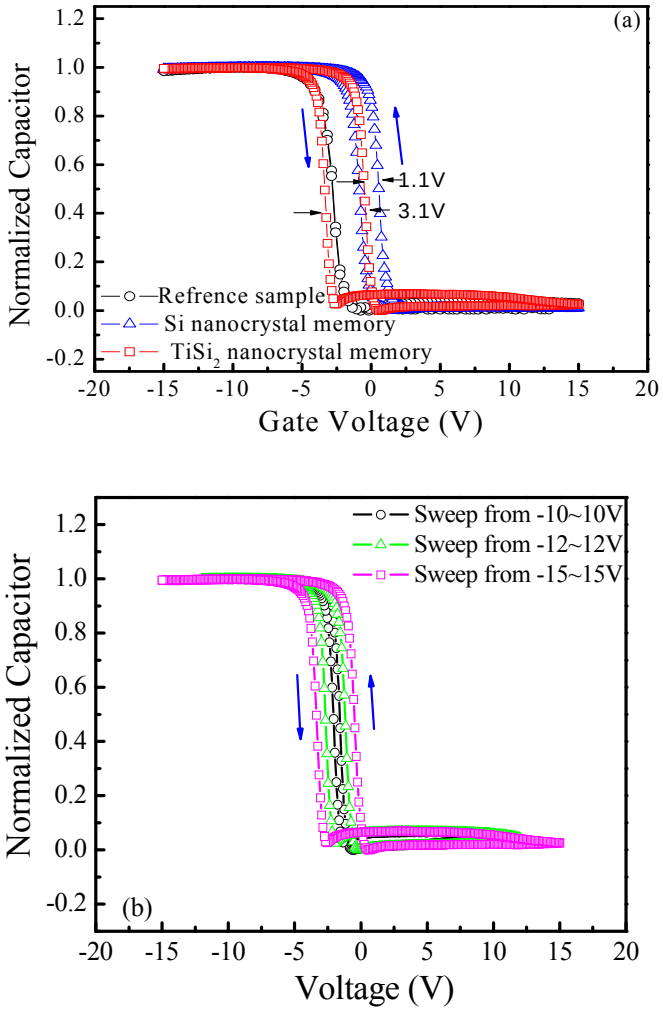

Fig. 2.2.4 (a) Capacitor-Voltage(C-V) sweep measurement for the $TiSi_2$ nanocrystal MOS memory and Si nanocrystal MOS memory capacitor, (b) C-V hysteresis of $TiSi_2$ nanocrystal MOS memory capacitor after sweeps between 10V (-10V), 12V (-12V) and 15V (-15V), The size for the capacitor is 400μm×400μm.

Figure 2.2.5 shows the source-drain current (I_{ds}) as a function of gate voltage (V_g)

for $TiSi_2$ nanocrystal MOSFET memory in the neutral state and writing state, which was characterized with an Agilent 4155A semiconductor analyzer and Agilent 81104A Pulse Generator at room temperature. The programming was performed at 15 V for 100 milliseconds (ms). The shift of the I-V curve towards higher gate voltage indicates the electron storage in the nanocrystals.

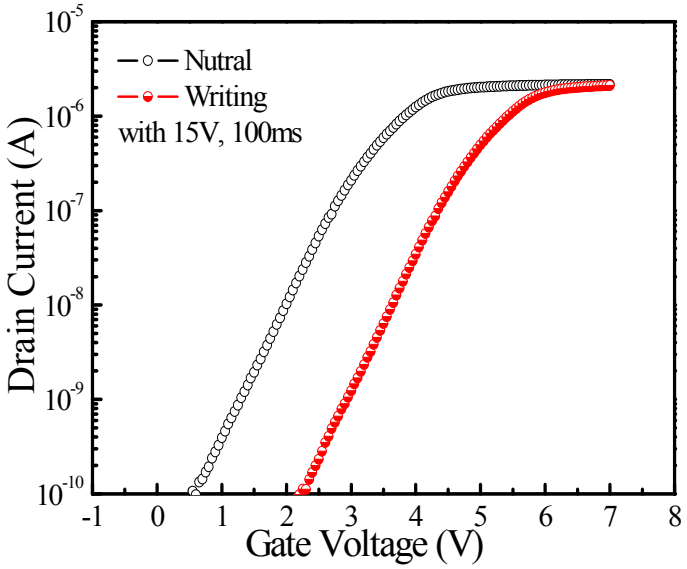

Fig. 2.2.5 Memory effect from a $TiSi_2$ nanocrystal MOSFET memory cell. The shift of I_{ds}-V_g curve after writing operation indicates the electron storage in the floating gate. The channel length of the device is 1μm.

Figure 2.2.6 (a) shows the threshold voltage shift (ΔV_{th}) as a function of writing time in both $TiSi_2$ nanocrystal and reference Si nanocrystal MOSFET memory devices. It is evident that ΔV_{th} increases with writing time until it finally saturates. This is due to the fact that as the writing time increases, more and more electrons are injected into the nanocrystals until they are unable to accept more electrons. Fig. 2.2.6 (b) shows the

dependence of ΔV_{th} on the writing voltage in $TiSi_2$ nanocrystal and reference Si nanocrystal memory devices. At the beginning, the writing voltage is not high enough to make the electrons go through the tunneling oxide by Fowler-Nordheim (F-N) tunneling and almost no electrons are injected to the nanocrystals, therefore, almost no threshold voltage shift was observed. As the writing voltage increases, the edge of the conduction band of tunneling oxide becomes triangular shaped and the slope of the triangle increases, which allows the electrons in the Si substrate to go through the tunneling oxide layer by F-N tunneling and reach the nanocrystals. As the writing voltage reaches ~15V or more, the device ΔV_{th} saturates and the saturation voltage is around 2V. We further calculate the electron storage in terms of their threshold voltage shifting, which is defined as [25],

$$\Delta V_{th} = \frac{Q_{ox} T_{cox}}{\varepsilon_{ox}} \qquad (1),$$

where ε_{ox} is the dielectric constant of SiO_2, T_{cox} the thickness of control oxide. The electrons storage at the saturation is estimated to be 6 electrons per $TiSi_2$ dot.

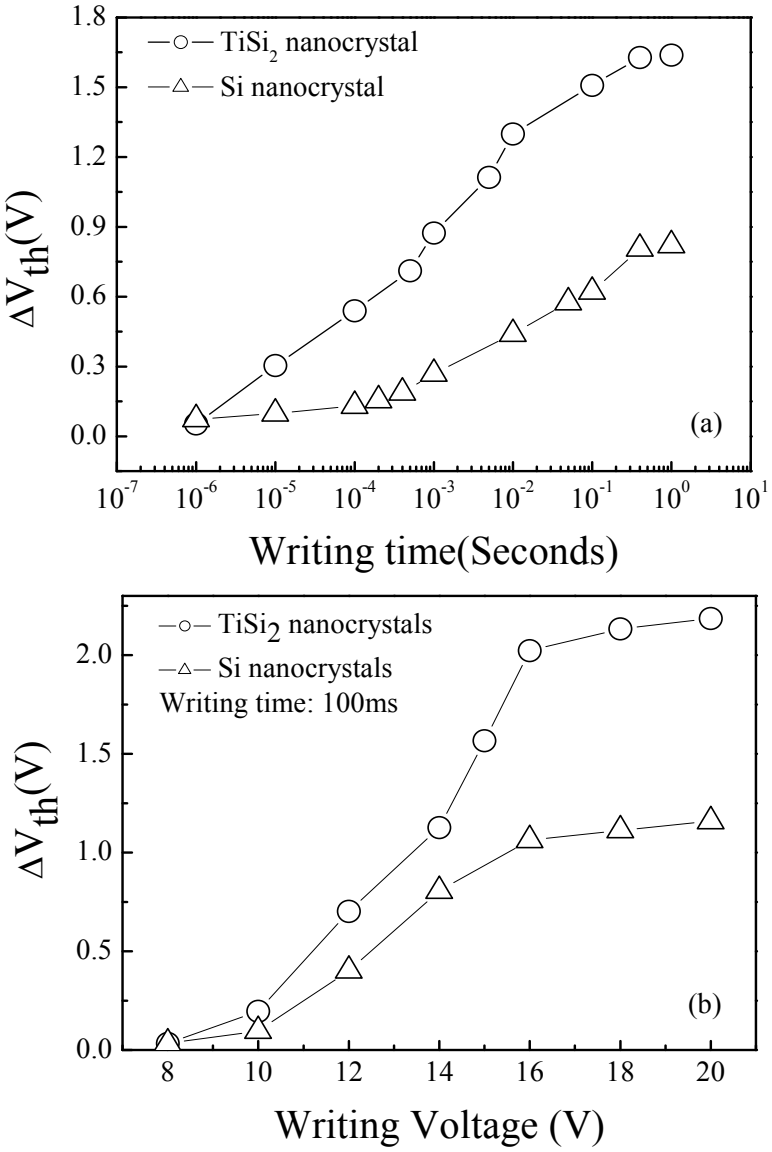

Fig. 2.2.6 ΔV_{th} as a function of (a) writing time at a fixed writing voltage of 15V, and (b) writing voltage at a fixed writing time of 100 ms, for MOSFET memory cells with $TiSi_2$ nanocrystals and reference Si nanocrystals, respectively.

The change in threshold voltage as a function of erasing time is shown in Fig. 2.2.7. The magnitude of ΔV_{th} increases as the erasing time increases in both $TiSi_2$ nanocrystal memory and Si nanocrystal memory. In the $TiSi_2$ nanocrystal memory, because of higher density of state (DOS) than that of Si nanocrystals, more electrons are available to be erased, which makes the ΔV_{th} saturate at a higher value than Si nanocrystal memory device.

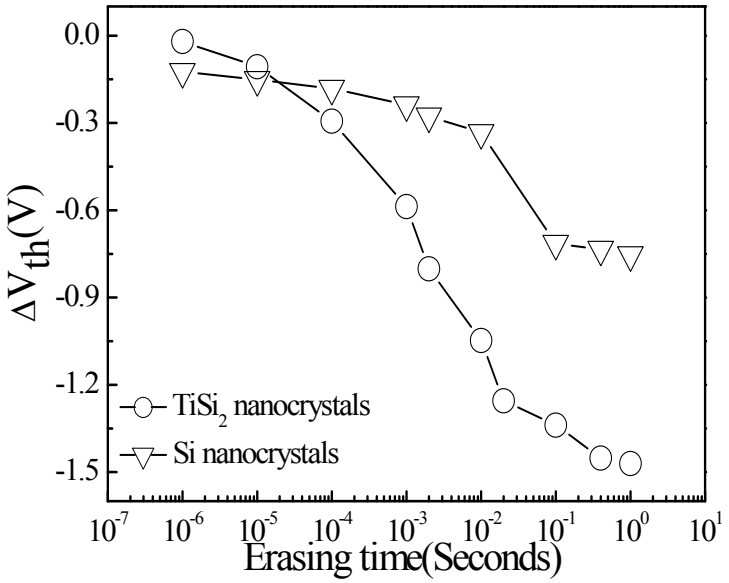

Fig. 2.2.7 ΔV_{th} as a function of erasing time for MOSFET memory cells with $TiSi_2$ nanocrystals and reference Si nanocrystals, respectively.

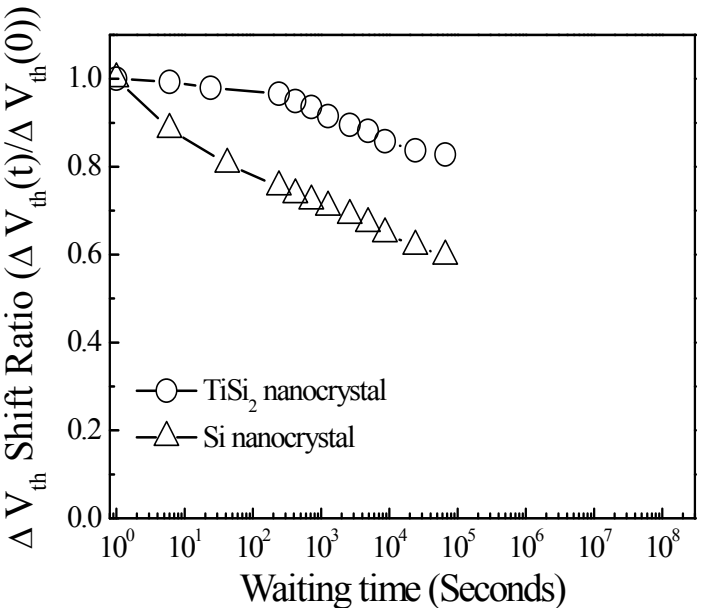

Fig. 2.2.8 Retention performance comparison between reference Si nanocrystal MOSFET device and $TiSi_2$ nanocrystal MOSFET memory device. The writing was done at 20 V for 1s.

The retention characteristics are shown in Fig. 2.2.8 for the two devices with $TiSi_2$ nanocrystals and Si nanocrystals, respectively. The devices were programmed at 20 V for 1 second. $TiSi_2$ nanocrystals lead to slower charge loss rate because of its lower occupied energy levels in the nanocrystals. Electrons in the $TiSi_2$ nanocrystals occupy the low energy level and are more difficult to tunnel through the tunneling oxide layer than electrons in Si nanocrystals. Therefore, the $TiSi_2$ nanocrystal memory device shows better retention performance than reference Si nanocrystal memory device.

2.2.4 Simulation

To clarify the physical mechanism in the writing and erasing process of $TiSi_2$ nanocrystal memory device, Schrodinger equation and Poisson-Boltzmann's equation are combined to calculate the energy band distribution in writing and erasing process by self-consistent calculation in 1-Dimension (1-D) [26-27]. It should be noted that 1-D simulation can provide straightforward and relatively accurate answers to this problem, more accurate results may be obtained through 3-D simulations [28-29].

The electrical potential ϕ (with respective to the substrate potential) satisfies the Poisson-Boltzmann's equation in Eq. (2):

$$\frac{d}{dx}\left(\varepsilon\frac{d}{dx}\phi\right) = q(p - n + D) \qquad (2),$$

where q is the elementary electron charge, ε is the material permittivity, n and p are the mobile electron and hole densities, respectively, and D is the concentration of ionized impurities (p-type doping).

The electron density in the nanocrystal is determined by the Schrodinger's equation:

$$-\frac{\hbar^2}{2}\frac{d}{dx}\left(\frac{1}{m}\frac{d}{dx}u(x)\right) + V(x)u(x) = Eu(x) \qquad (3),$$

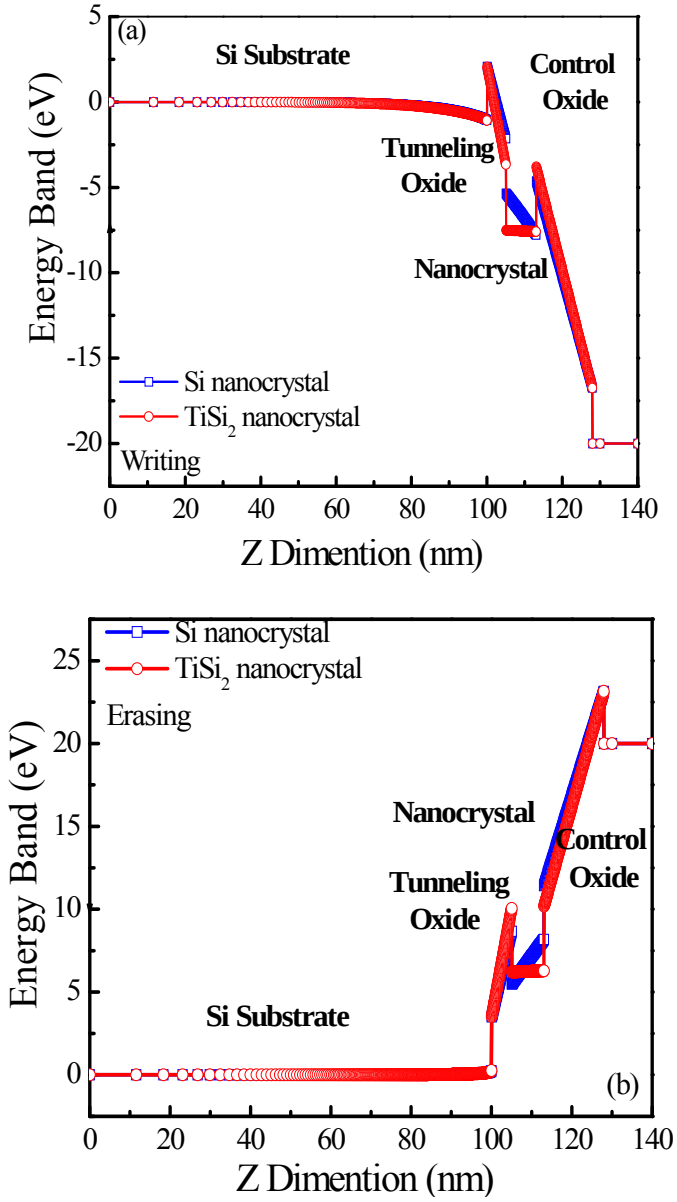

Fig. 2.2.9 The edge of conduction band distribution of $TiSi_2$ nanocrystal and reference Si nanocrystal devices in writing and erasing states (Writing/erasing voltage is 20V/-20V). ε is taken as 500 and 12 in $TiSi_2$ nanocrystal and Si nanocrystal respectively.

where

u, E, V, and $\hbar$ are the wave function, eigen energy, potential energy, and reduced Planck's constant, respectively. The parameters for the devices are similar as those in real devices with 8nm nanocrystal size, 5nm tunneling oxide, 15nm control oxide and the calculation stops when maximum difference between successive potential distributions is 1mV.

Figs. 2.2.9 (a) and (b) show the conduction band edges for the two devices with the embedded $TiSi_2$ nanocrystals and Si nanocrystals in the writing and erasing biases, respectively. In Fig. 2.2.9 (a), when 20V is applied on the control gate, the edge of the conduction band in the tunneling oxide region and control oxide region shows a triangle shape. In the Si nanocrystal region, the edge of the conduction band also shows a triangular shape, indicating that the electric field penetrates the Si naocrystals and a certain amount of voltage drops on them. In the $TiSi_2$ nanocrystal structure, $TiSi_2$ is metallic. When the voltage is applied on the control gate, the electric field is screened at the surface, almost no voltage is dropped in the $TiSi_2$ nanocrystal region. Since the total voltage drop is the same for both devices, the electric field in tunneling oxide is higher in the $TiSi_2$ nanocrystal memory than in the Si nanocrystal memory for a given applied voltage. The higher electric field in the tunneling oxide region increases the F-N tunneling of electrons from the Si substrate into the $TiSi_2$ nanocrystal compared to that of the Si nanocrystal during the writing phase.

The same effect occurs during the erasing process as shown by the conduction band edges plotted in Fig. 2.2.9 (b). In the $TiSi_2$ nanocrystal memory, more voltage drops across the oxide layer compared to that of the Si nanocrystal memory. Thus, for a given voltage, the tunneling rate out of the nanocrystal into the Si is larger for the $TiSi_2$

nanocrystals compared to that of the Si nanocrystals.

The higher density of states (DOS) in the metallic $TiSi_2$ nanocrystal compared to that in the Si nanocrystal combined with the increased electric field in the tunneling oxide explains the difference in the reading and writing properties of the two different systems. During writing, before saturation, the increased electric field in the tunneling oxide of the $TiSi_2$ nanocrystals gives rise to a larger ΔV_{th} for a give voltage or time as shown in Figs. 2.2.6 (a) and (b). The larger DOS of the $TiSi_2$ compared to that of the Si nanocrystals results in a larger saturation value of ΔV_{th} for the $TiSi_2$ nanocrystal structures as shown in Fig. 2.2.6 (b). The larger electric field in the tunneling oxide also explains the larger ΔV_{th} as a function of erase time for the $TiSi_2$ nanocrystal structures compared to that of the Si nanocrystal structures as seen in Fig. 2.2.7, although the reason for the cross-over at very short times is not clear. Thus, overall, the improvement in performance of the $TiSi_2$ nanocrystal memory compared to the Si nanocrystal memory is consistent with an explanation based on (i) the different electric fields in the tunneling oxides resulting from the different screening properties of the nanocrystals and (ii) the different density of states of the nanocrystals.

The writing and erasing tunneling current densities are calculated using the method proposed in [30], considering the quantization of carriers in the inversion layer or the accumulation layer when the device is biased:

$$J = q\int T(E)f(E)\rho(E)F(E)dE \qquad (4),$$

where $f(E)$ is the impact frequency, $\rho(E)$ the 2-dimensional (2-D) density of states, $F(E)$ the Fermi-Dirac distribution function and $T(E)$ the tunneling probability,

respectively. The time concept in a memory device can be defined as the inverse of the tunneling current density [31]. The time τ is presented as:

$$\tau = \frac{q}{J \times L^2} \quad (5),$$

where q, J and L are the electron charge, tunneling current density and size of the nanocrystal, respectively.

Using equation (4) and (5), the calculated voltage dependences of the writing and erasing processes are shown in Fig. 2.2.10 (a) and (b), respectively. It is found that, for both writing and erasing processes, the programming speed increases with the gate voltage. This is due to the change of the shape of the electron barrier in tunneling oxide region with the gate voltage. As the gate voltage increases, the electric field in tunneling oxide increases which makes the electrons easier to go through the tunneling oxide. Since the electric field in tunneling oxide of $TiSi_2$ nanocrystal memory is always larger than that in Si nanocrystal memory, $TiSi_2$ nanocrystal device shows faster programming speed than Si nanocrystal device.

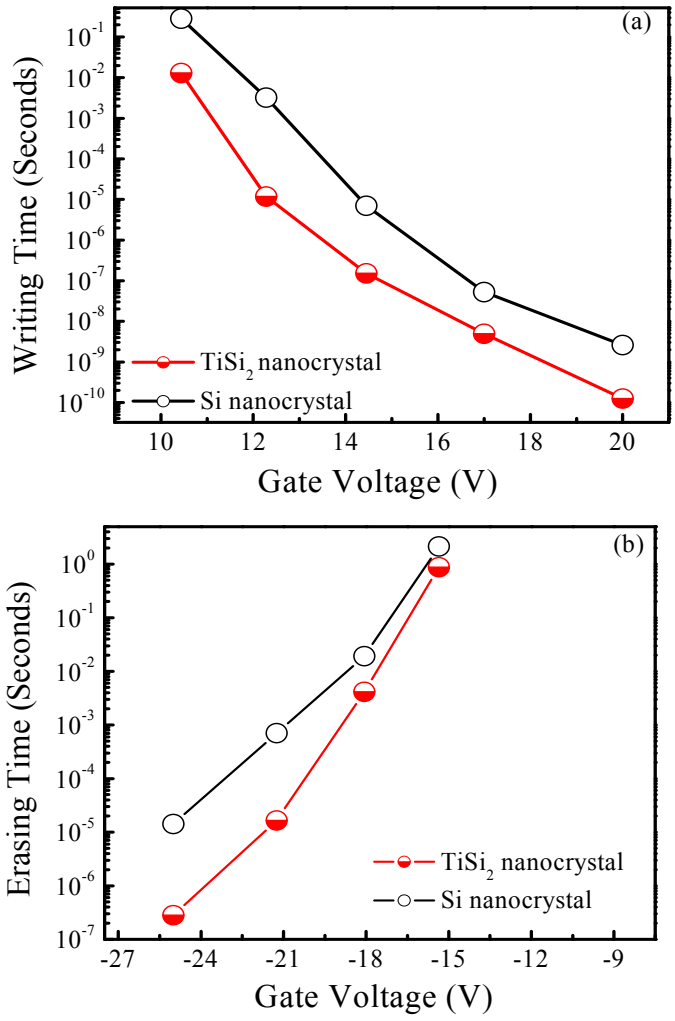

Fig. 2.2.10 Simulated programming speed versus operation voltage. (a) writing time as a function of gate voltage, (b) erasing time as a function of gate voltage. The shift of conduction band between Si and SiO_2 is set to be 3.1eV.

To explain the retention characteristics, the trap-assisted tunneling mechanism is assumed. The retention time of the charge storage is calculated by Poole-Frenkel effect [32]. The leakage current is derived with following method:

$$J = C_3 E \exp\left(-\frac{q\phi_t}{kT}\right) \times \exp\left(\frac{1}{\gamma kT}\sqrt{\frac{q^3}{\pi\varepsilon}E}\right) \quad (6),$$

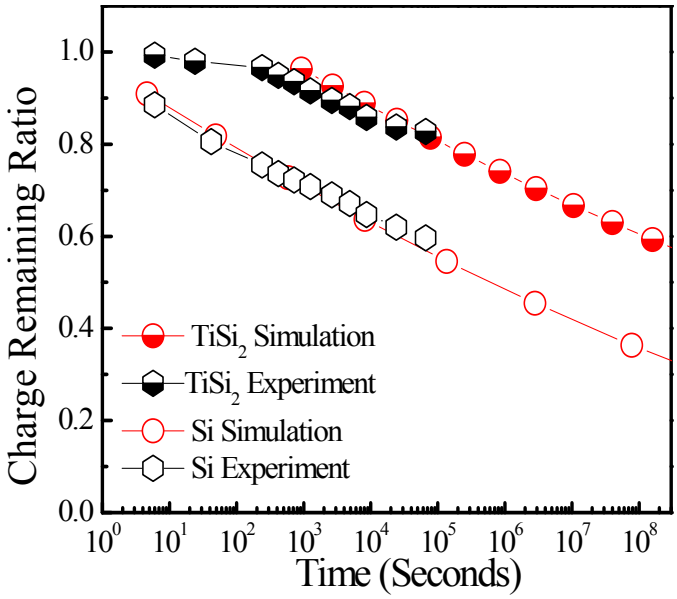

Fig. 2.2.11 Simulated retention performance of reference Si nanocrystal and $TiSi_2$ nanocrystal memory. To match with experiment result, Φ_t is set to be 0.5eV for Si nanocrystal and 0.6eV for $TiSi_2$ nanocrystal system.

where Φ_t is trapped electrons' energy level below the dielectric conduction band and r is the refractive index of dielectic films. $C3$ relates to the trap density. Fig. 2.2.11 shows the retention performance comparison between the $TiSi_2$ nanocrystal memory and Si nanocrystal memory. The hollow symbol curves show the retention performance for Si nanocrystal memory and the solid symbol curves show the retention performance for $TiSi_2$ nanocrystal memory. The black color curves show the retention performance from experiment which is also shown in Fig. 2.2.8. To match the real device, the potential is set to be 0V on the control gate and the electric field in the tunneling oxide layer caused by

the storage of electrons is calculated by Poisson equation. It is found that $TiSi_2$ nanocrystal memory device shows slower charge loss rate and higher charge storage after 10 years, which is similar with the experiment result. $TiSi_2$ nanocrystals store more electrons than Si nanocrystals, moreover, the charge loss is slower due to the deeper well. These result in more electrons left in the nanocrystals after 10 years.

2.2.5 Conclusion

In summary, we fabricated $TiSi_2$ nanocrystal memories by two-step annealing process. Compared with the reference Si nanocrystal memory, $TiSi_2$ nanocrystal memory shows larger memory window, faster writing, erasing speed and better retention performance. Schrodinger equation and Poisson-Boltzmann's equation are combined to do self-consistent calculation to clarify the physical mechanism. Metallic $TiSi_2$ nanocrystal embedded memory shows higher electric field in tunneling oxide region leading to easier F~N tunneling, which explains faster writing and erasing performance in $TiSi_2$ nanocrystal memory. $TiSi_2$ nanocrystal memory also shows better retention performance in the calculation which matches the real device characterization.

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Chapter 3: Core-shell nanocrystal memory

3.1 Memory characteristics of ordered Co/Al_2O_3 core-shell nanocrystal arrays assembled by di-block co-polymer process

3.1.1 Introduction

Nonvolatile memory devices with floating-gate structure are being widely used in MP3 players, digital cameras, and memory cards nowadays [1]. The most prominent problem of poly-Si floating gate memory is the limited potential in continuous scaling of the device structure [2]. Due to excellent memory performance and high scalability, NC floating gate memory devices have attracted considerable attention [3]. Different types of NCs such as double Si dots [4], Ge NCs [5], metal NCs [6-8], silicide NCs [9-12], and dielectric NCs [13] have been proposed to achieve memory devices with longer retention performance. Among these NCs, metallic NCs have larger work function than the electron affinity of Si NCs, and are advantageous to reduce the leakage current through the tunneling barrier due to increased barrier height [14]. These NC memories also achieved high programming/erasing speeds based on the high density of states in NC storage [15-16]. Nevertheless, all NCs are randomly distributed, limiting the device performance and overall scalability. The synthesis of uniform, well ordered NC arrays is one of the key limitations for device fabrication, garnering much of the research focus at the moment [17-18]. Additionally, as the memory technology scales down further, thinner

SiO_2 tunnel layer is required for lower power operations. However, thinner oxide increases leakage, leading to compromised retention. It is well known that leakage current of high-k materials is smaller than that of SiO_2 for the same equivalent oxide thickness (EOT). To improve the retention performance of memory devices, recent studies have tried to use high-k dielectrics such as Al_2O_3 and HfO_2, instead of SiO_2 layers, for the tunnel and control oxide layers to reduce the leakage [19].

In this work, we developed Co NC ordered arrays with uniform size and distribution using a di-block co-polymer synthesis process. In addition, thin Al_2O_3 high-k layers were deposited by atomic layer deposition (ALD) as shell of the NCs. The purpose is twofold: the ability of minimizing segregation of Co metal atoms to tunnel oxide during high-temperature device process and the increase of EOT. The benefit is enhanced retention performance. Uniformly distributed Co/Al_2O_3 core-shell NCs are embedded in metal-oxide-semiconductor (MOS) memory system. The Co/Al_2O_3 core-shell NC memory achieved a higher retention performance as compared to Co NC memory reference sample.

3.1.2 Experiment

A self-assembly di-block co-polymer process was used to deposit highly ordered Co NC arrays. First, a 3.0-nm-thick thermal oxide was grown in dry oxygen at 850ºC as the tunnel oxide. A thin Al_2O_3 layer approximately 1 nm thick was then deposited on the SiO_2 layer by ALD at 250ºC, using Cambridge Savannah 100&200. Self-assembly of Co

NCs was achieved by mixing PS-b-P4VP, toluene and $CoCl_2 \cdot 6H_2O$ for 48 hours, followed by spin-coating onto the sample surface. The polymer was subsequently removed by exposure to oxygen plasma for 3 minutes. The obtained Co NCs were reduced from CoO by performing a forming gas annealing at 400ºC for 30 minutes. A layer of Al_2O_3, approximately 1nm, was deposited over the Co NC array to encapsulate the particles and form the desired core-shell structure. A control oxide layer of about 15 nm was then deposited by LPCVD and then, electrode was patterned to form MOS structure memory capacitor. Additionally, a sample with only Co NCs and another sample with pure Al_2O_3 were prepared as reference samples to compare their device performances.

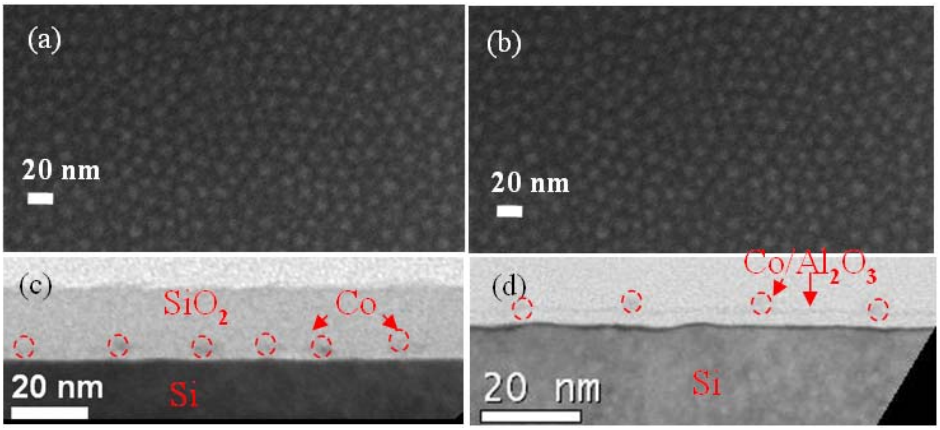

Fig. 3.1.1 (a) SEM image of ordered Co NCs on SiO_2. Di-block co-polymer remains on the surface, (b) SEM image of ordered Co NCs on Al_2O_3. Di-block co-polymer remains on the surface, (c) TEM image of Co NC memory, (d) TEM image of Co/Al_2O_3 core-shell NC memory.

3.1.3 Results and discussion

Figures 3.1.1 (a) and (b) show scanning electron microscope (SEM) images of Co NCs on SiO_2 and Co NCs on Al_2O_3 aligned with the di-block co-polymer process, respectively. The NC arrays are well ordered with uniform size and spacing between particles, resulting in a density of ~$5x10^{11}$ NCs/cm^2 in both cases. Figs. 3.1.1 (c) and (d) show the cross-sectional transmission electron microscope (TEM) images of Co NC memory and Co/Al_2O_3 core-shell NC memories after device fabrication, respectively. Based on these measurements, the average diameter of the spherical NCs is determined to be ~6 nm with an average distance spacing of ~14 nm. The thickness of the tunnel oxide is ~3 nm and the control oxide is ~15 nm. As shown in Fig. 3.1.1 (d), thin Al_2O_3 shell layer is clearly shown between the Co dots, indicating the existence of Al_2O_3 layer. Further energy dispersive x-ray spectroscopy analysis proved the existence of core/shell structure.

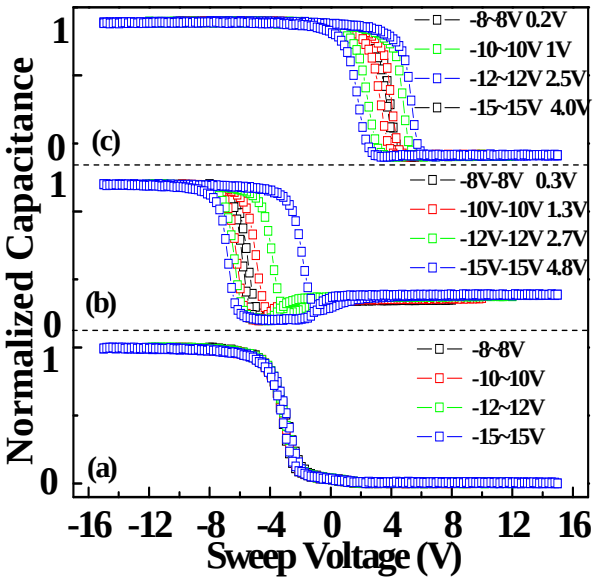

Fig. 3.1.2 Normalized C~V sweep result for capacitor memories with (a) Al_2O_3 shell only, (b) Co NCs, and (c) Co/Al_2O_3 core-shell NCs. The size of top contact is $100\times100\mu m^2$.

The MOS capacitor memories were characterized using an Agilent LCR meter at room temperature. A typical high-frequency (1MHz) capacitance-voltage (C-V) sweep results with a scanning range between ±8 V to ±15 V for the devices with Al_2O_3 shell only, Co NCs and Co/Al_2O_3 core-shell NCs are shown in Figures 3.1.2 (a)-(c), respectively. The sweep started from the inversion to the accumulation, and finally back to the inversion region at a rate of 0.5 V/s.

In Fig. 3.1.2 (a), as voltage is swept from -8~8 V, -10~10 V, -12~12 V and -15~15 V, a tiny memory window (~0.2 V at ±15 V sweep) is shown, which may be caused by defects in the Al_2O_3 layer. As the NCs are added to the device structure, an obvious

hysteresis is observed as the gate voltage increases (Fig. 3.1.2 (b)). Starting at ±8 V, the memory window is estimated to be ~0.3 V. Increasing the sweep voltage range to 10V, 12V and 15 V resulted in a memory window increase of 1.2 V, 2.7 V, and 4.8 V, respectively. Fig. 3.1.2 (c) shows obvious hysteresis curves at different sweep voltages. A small memory window of ~0.2V is obtained as the voltage is swept at ±8 V. As the sweep voltage range increases to 10 V, 12 V and 15 V, the memory window increases to 1 V, 2.5 V, and 4 V, respectively. Wider voltage sweep range leads to the fact that more electrons are programmed to the NCs and erased from the NCs, therefore larger memory window is achieved.

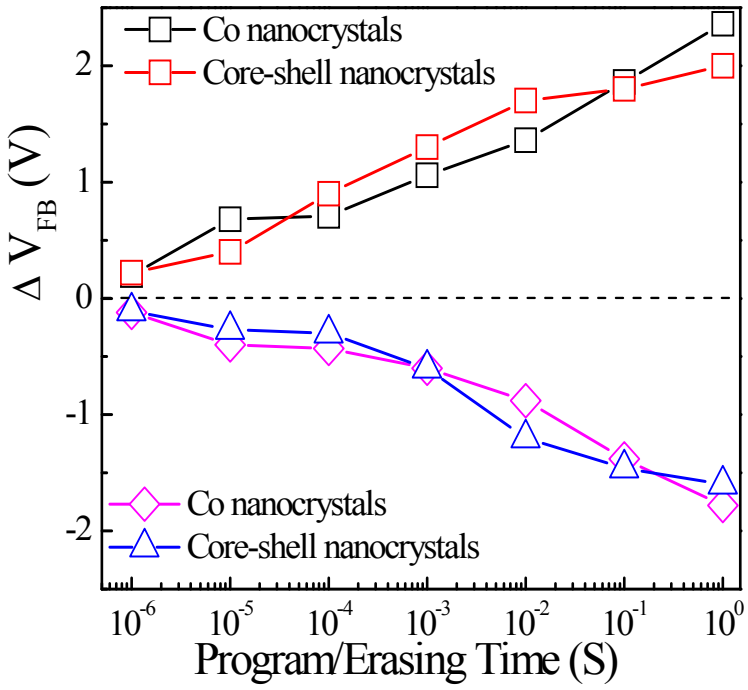

Fig. 3.1.3 Programming/erasing transient characteristics for capacitor memories with Co/Al_2O_3 core-shell NCs and Co NCs without shell.

Figure 3.1.3 shows the flat band voltage shift, ΔV_{FB}, changes with programming and erasing (P/E) time for Co and Co/Al_2O_3 core-shell NC memory, respectively, when using a P/E voltage of ±15V. As programming time increases, more electrons are injected into the NCs until a saturation is achieved and, no more electrons are able to enter the NCs. The same situation is observed as the device is erased. As the erasing time increases, more electrons are extracted from the NC core-shell structures. Although core-shell NC memory has additional Al_2O_3 shell layer, electric field concentration effect [20] caused by the high-k properties makes most of the voltage drop on SiO_2 layer. This makes Co NC memory and Co/Al_2O_3 core-shell NC memory appear to have similar P/E speeds.

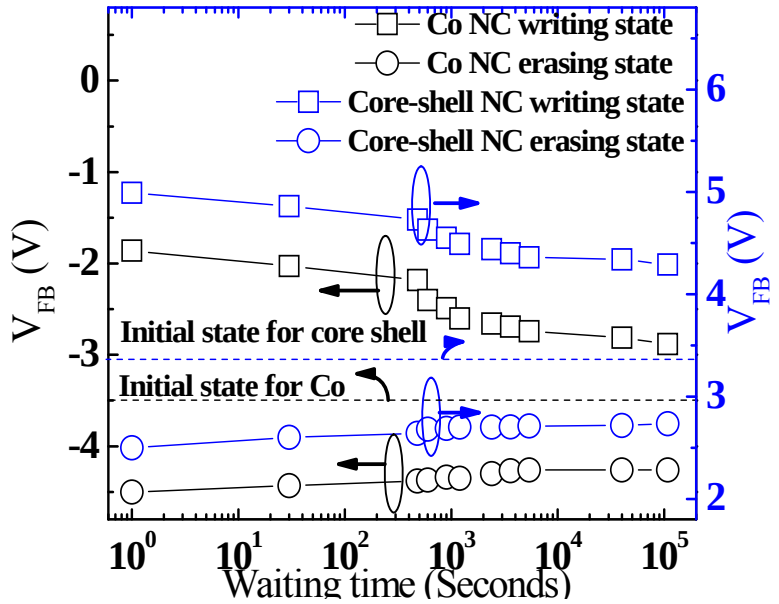

Fig. 3.1.4 Retention characteristics for capacitor memories with Co/Al_2O_3 core-shell NCs and Co NCs without shell.

Figure 3.1.4 shows retention characteristics of the two capacitor memories with Co and Co/Al_2O_3 core-shell NCs at programmed and erased states, respectively. The programming and erasing conditions are 15 V and -15V for 1 second, respectively. After

programming, transient capacitance at the same read voltage is recorded intermittently. The Co/Al_2O_3 core-shell NC capacitor memory leads to a slower charge loss ratio. After $\sim 10^5$ seconds, ~70% charge is left in the Co/Al_2O_3 core-shell NC memory capacitor and ~50% charge is left in the Co NC capacitor memory, which is reasonable for a tunnel oxide of 3 nm. The electrons are confined in the Co NCs and high-k Al_2O_3 shell acts as an additional barrier to the electrons compared to the Co NC memory, which contributes to the slower charge loss ratio and longer retention time.

Figure 3.1.5 shows the endurance characteristics of the two capacitors with Co and Co/Al_2O_3 core-shell NCs, respectively. The programming and erasing conditions are ±16V for 200ms. The memory windows of the two devices stay open up to 10^5 times of operation, although the magnitude shrinks about 23%. The up-shift of the threshold voltage with times of operation is due to the accumulated trapped charges in the Al_2O_3 layer.

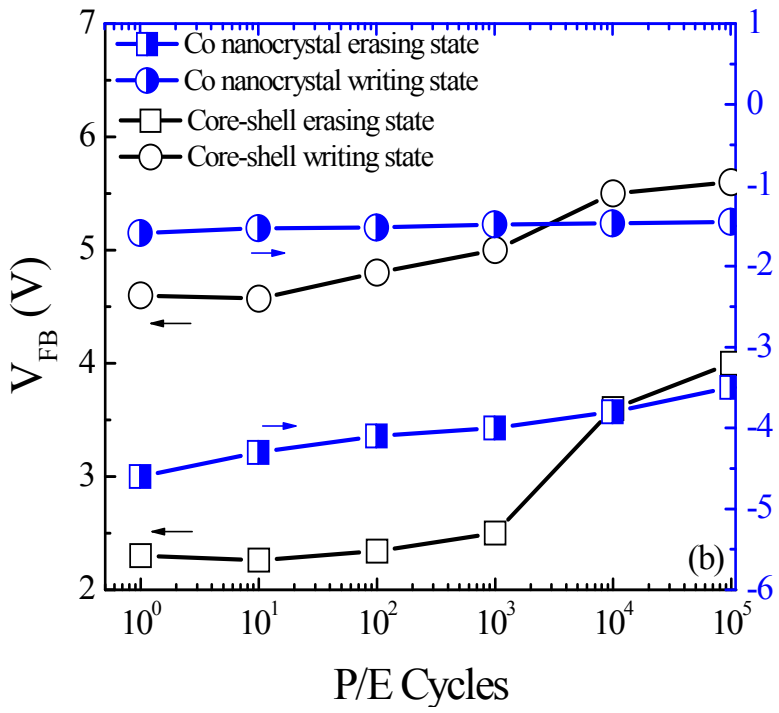

Fig. 3.1.5 Endurance characteristics for capacitor memories with Co/ Al_2O_3 core-shell NCs and Co NCs without shell.

3.1.4 Conclusion

In summary, a core-shell NC MOS memory was demonstrated. Uniform NC size and spacing are obtained by a di-block co-polymer fabrication process. The uniform NC distribution throughout the sample is critical for device scalability, reliability and manufacturability. High-k Al_2O_3 layer is used as shell in the core-shell structure, which improves the retention performance. Reliable di-block co-polymer process to make metal/high-k core-shell NC memory may open up opportunities for memory applications.

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3.2 Co/HfO_2 Core-Shell Nanocrystal Memory

3.2.1 Introduction

Nanocrystal (NC) floating gate memory devices have received considerable attention due to its excellent memory performance and high scalability [1-4]. In this kind of memory structure, discrete trapping is used to store charges, which improve charge loss ratio encountered in conventional flash memories. Several approaches, such as deeper well nanocrystals [5,6], dielectric nanocrystals[7,8], and double-layer nanocrystals [9,10] were tried to obtain wider memory window, longer retention time, and faster writing/erasing speed. Metal nanocrystals have larger work function than that of silicon nanocrystals, and are advantageous to reduce the leakage current through the tunneling barrier due to the increased barrier height [12]. These metal particles were demonstrated to achieve better memory performance [10-12]. To avoid reaction between the metal nanocrystal and oxide layer, silicide coated hetero-structure nanocrystals were also proposed, with the goal of prolonging the retention time [13]. At the same time, different high-k materials such as HfO_2, Al_2O_3 were used as the tunneling oxide to improve the retention performance of the memory devices [14-16]. In this chapter, we report our novel structure of using core-shell nanocrystals for charge storage, which will improve the retention time, and programming/erasing (P/E) performances. We also demonstrate metal/high-k core-shell nanocrystal memory through a low temperature co-polymer process.

3.2.2 Experiment

For comparison, the nanocrystals were prepared in two ways. First, a 5.0-nm-thick thermal oxide was grown in dry oxygen at 850^0C. A thin HfO_2 layer of around 3nm was then deposited on SiO_2 layer by ALD (Atomic Layer Deposition). An ultra-thin (~2nm) blanket Co layer was deposited through e-beam evaporation followed by RTA (Rapid Thermal Annealing) in N_2 at 650^0C to form nanocrystals. Another thin HfO_2 layer of around 3nm was deposited again on the nanocrystals to create Co/HfO_2 core-shell structure. Control oxide of about 15 nm was then deposited by LPCVD (Low Pressure Chemical Vapor Deposition). After control gate pattern formation, the control gate and backside gate were formed to make a MOS structure memory capacitor.

A self assembly di-block co-polymer process was used to deposit a highly ordered nanocrystal array. First, a 5.0-nm-thick thermal oxide was grown in dry oxygen. A thin HfO_2 layer of around 3nm was then deposited on SiO_2 layer by ALD. Self-assembly of cobalt was achieved by mixing PS-b-P4VP, toluene and $CoCl_2 \bullet 6H_2O$ followed by spin-coating onto the sample surface. The polymer was subsequently removed by exposure to an oxygen plasma for 3 min. The ordered Co particles were formed after a forming gas annealing at 400^oC for 30 minutes to reduce the surface cobalt oxide to cobalt [20]. A thin HfO_2 layer of ~3nm was deposited again on Co nanocrystals to form core-shell structures. Control oxide of about 15 nm was then deposited by LPCVD and MOS structure memory capacitor was fabricated.

3.2.3Results and discussion

Figures 3.2.1 (a) and (b) show the 3-D (3 Dimensional) schematic and energy band diagram of Co/HfO_2 core-shell nanocrystal memory, respectively. In Fig. 1 (a), the core-shell nanocrystals are well ordered. The core-shell structure is represented by orange spheres with a transparent red shell. The band alignment of the core-shell nancrystal memory along z direction is indicated in Fig. 3.2.1 (b) [17-18]. Similar to the hetero-structure nanocrystals, HfO_2 acts as a barrier, increasing the charge trapping ability and resulting in longer retention times [19].

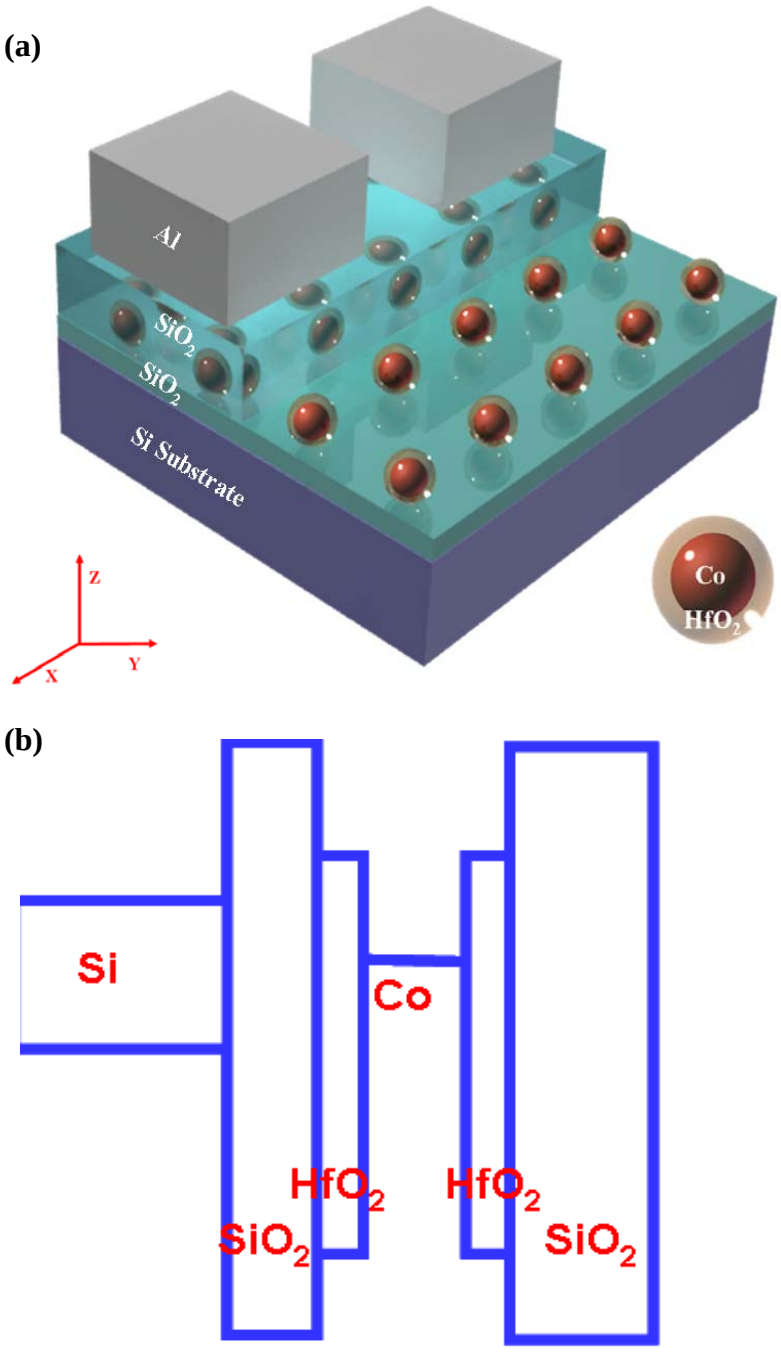

Fig. 3.2.1 a) Device structure of Co/HfO_2 core-shell dot memory, b) band diagram of Co/HfO_2 core-shell dot memory.

Figure 3.2.2 (a) shows the 2D diagram of core-shell structure. A single electron is located in the center nanocrystal while the neighboring structures are empty. The potential distribution around the electron is calculated semi-classically. According to the following equations $\oint_S \varepsilon \bullet \vec{E} d\vec{S} = Q$ and $\phi = -\int_{\infty}^{R} \vec{E} d\vec{l}$, the potential distribution along the red line in Fig. 3.2.2 (a) is shown in Fig. 3.2.2 (b). The red line in Fig. 3.2.2 (b) shows the potential distribution of the core-shell structure. Potential distribution of the nanocrystal without shell is represented by the blue curve in (b). It is clearly seen that in the nanocrystal region, the potential of the core-shell structure is lower than the nanocrystal without shell. This means the shell structure screens the potential and reduces the Coulomb Blockade effect between particles. As a result of screening, the core-shell structure increases the electrons stored per nanocrystal.

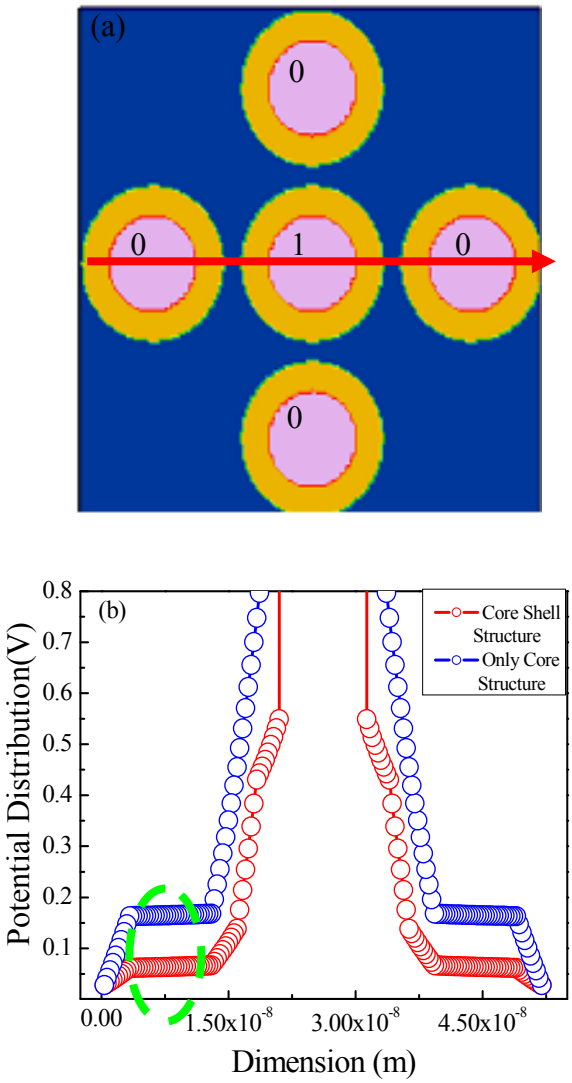

Fig. 3.2.2 a) 2D diagram of core-shell structure, an electron is set in the center nanocrystal while surrounding nanocrystals remain empty, b) Potential distribution of the core-shell structure along red line of a), Potential difference highlighted in green shows the core-shell structure reduces the Coulomb Blockade effect between particles.

Figures 3.2.3 (a), (b) and (c) show the AFM (Atomic Force Microscope) images of the Co/HfO_2 core-shell nanocrystals prepared by e-beam evaporation, Co nanocrystals and Co/HfO_2 core-shell nanocrystals prepared by the co-polymer respectively. Fig. 3.2.3 (a) shows a non-uniform nanocrystal size ranging between 3 - 12nm. Fig. 3.2.3 (b) shows uniform nanocrystal size and spacing between particles. The size of nanocrytals is ~10nm with a spacing of ~8nm. After the HfO_2 layer was deposited on the Co nanocrystals, the AFM still show uniform particle size and spacing, which is indicated in Fig. 3.2.3 (c).

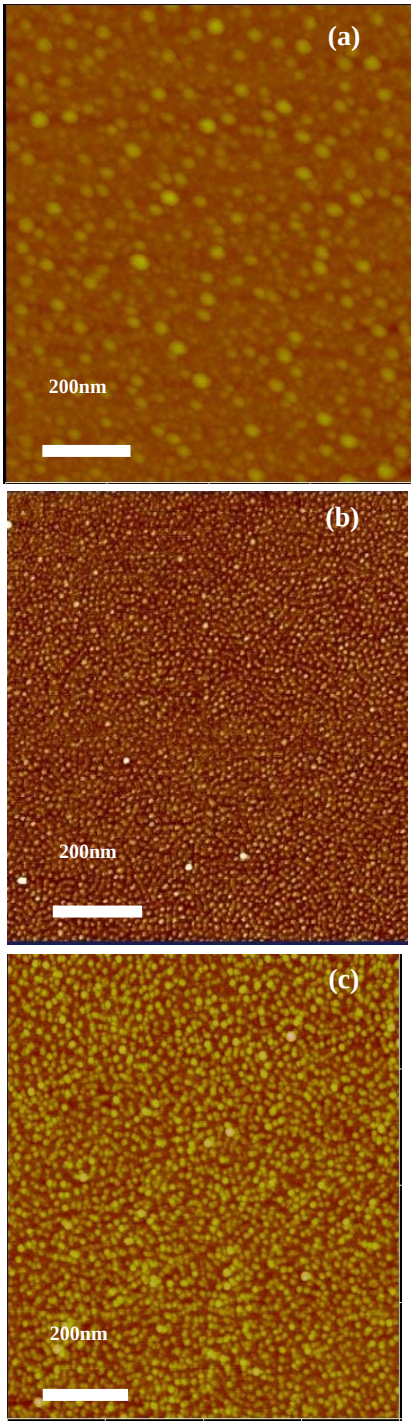

Fig. 3.2.3 AFM images for a) Co/HfO_2 core-shell particles by e-beam evaporation, b) Co co-polymer particles, and c) Co/HfO_2 core-shell particles by co-polymer.

The capacitors were characterized by Agilent LCR meter at room temperature. Figures 3.2.4 (a), (b) and (c) show typical high frequency (1MHz) capacitance-voltage (C-V) sweep results with a scanning range between ±8V to ±12V for the memory capacitors with only HfO_2 shell, Co/HfO_2 core-shell structure prepared by co-polymer, and Co/HfO_2 core-shell structure prepared by e-beam evaporation, respectively. The sweep was run from the inversion to accumulation region and back with a sweep rate of 0.5V/s.

In Figure 3.2.4 (a), when voltage is swept from -8~8V, -10~10V and -12~12V, a tiny memory window (~0.01V at ±12V sweep) is shown which may be caused by defects in the HfO_2 layer. Fig. 3.2.4 (b) exhibits an obvious hysteresis as the gate voltage is increased. A memory window of ~6.7V is observed as the voltage is swept at ±8 V. When the sweep voltage is increased to 10V and 12 V, the memory window is increased at 8V and 8.4V, respectively. Wider voltage sweep range leads to the fact that more electrons are programmed to the nanocrystals and erased from the nanocrystals, therefore larger memory window is achieved. A similar response is observed in the Co/HfO_2 core-shell structure prepared by e-beam evaporation. In Fig. 3.2.4 (c), when voltage is swept from -8~8V, -10~10V and -12~12V, it shows an increasing memory window of 2.5V, 3.4V and 7.9V, respectively. This means more and more electrons are programmed and erased with the increase of sweeping gate voltage.

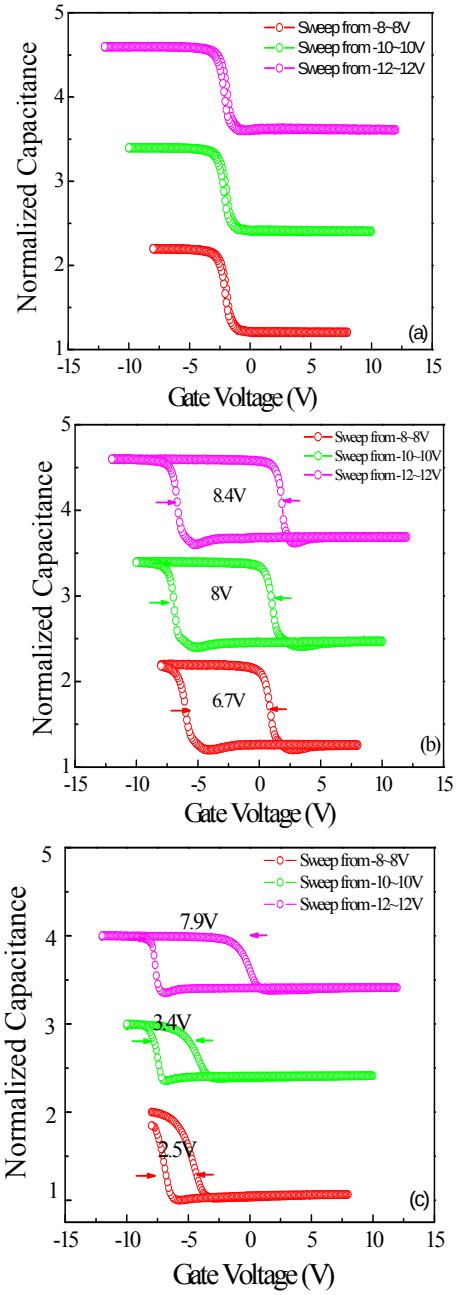

Fig. 3.2.4 C-V sweep memory window for a) capacitor with only HfO_2 shell, b) capacitor with Co/HfO_2 core-shell particles by di-block co-polymer, and c) capacitor with Co/HfO_2 core-shell particles by e-beam evaporation.

Figure 3.2.5 (a) shows the flat band voltage shift (ΔV_{FB}) as a function of programming and erasing (P/E) time in co-polymer based Co/HfO_2 core-shell nanocrystal memory capacitor. It is evident that ΔV_{FB} increases with P/E time until saturation occurs. This is due to the fact that as the programming time increases, more and more electrons are injected into the nanocrystals until they are unable to accept more electrons. The same situation is observed as the device is erased. When increasing the erasing time, more and more electrons are erased until saturation. It is found that when the P/E voltage is increased, more electrons can go through the tunneling layer by F-N tunneling and are injected to nanocrystals or erased from nanocrystals. The higher P/E voltage is, the larger flat band voltage shift is achieved. A similar case happened in the core-shell nanocrystals prepared by e-beam evaporation, as shown in Fig. 3.2.5 (b). The magnitude of ΔV_{FB} increases as the P/E time and voltage increase until saturation.

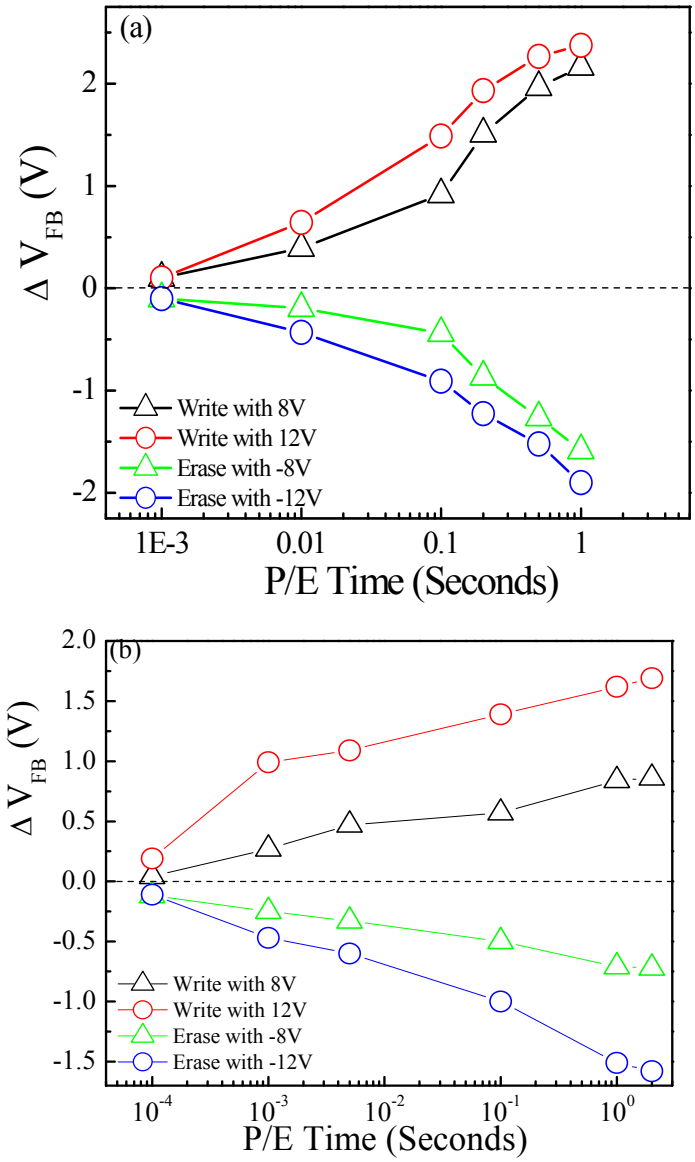

Fig. 3.2.5 Writing/Erasing performance for capacitors with Co/HfO_2 core-shell particles, (a) by co-polymer, and (b) by e-beam evaporation.

The retention characterization is shown in Fig. 3.2.6 for the two capacitors with Co/HfO_2 core-shell nanocrystal memory capacitors. The capacitors were programmed at

15 V for 1 second. The co-polymer based Co/HfO_2 core-shell nanocrystal memory capacitor leads to a slower charge loss ratio. The evaporated Co/HfO_2 capacitor had a charge remaining ratio of 52% and a 93% charge remaining ratio was achieved in the co-polymer based system when extrapolated to 10 years. The lower nanocrystal preparation temperature and uniform nanocrystal size and distribution of the di-block co-polymer contribute to the slower charge loss ratio.

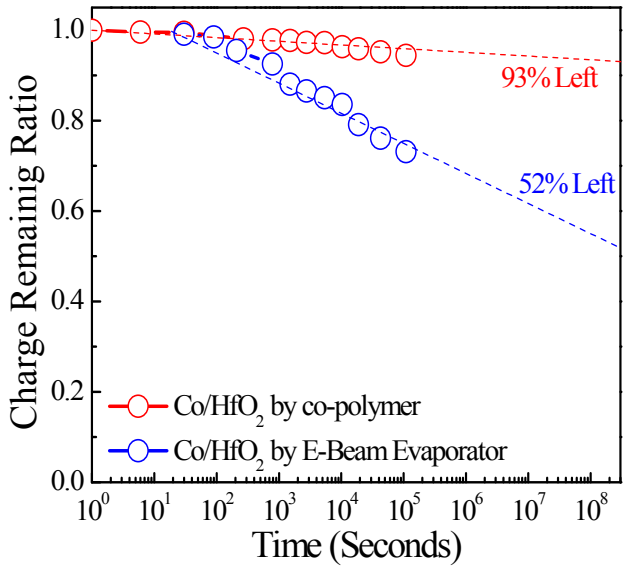

Fig. 3.2.6 Retention performance for capacitors with Co/HfO_2 core-shell particles by co-polymer and e-beam evaporation

3.2.4 Conclusion

In summary, a novel core-shell nanocrystal MOS memory has been proposed and

demonstrated. Wide memory windows of 7.9V and 8.4V was achieved at the ±12 V voltage sweep for memories based on randomly distributed and ordered Co/HfO_2 core-shell nanocrystals, respectively. Uniform particle size and spacing are obtained by a di-block co-polymer fabrication process. The uniform nanocrystal distribution throughout the sample is critical for device reliability and manufacturability. A low-temperature core-shell synthesis process minimizes possible reaction between the metal core and tunneling layer that may deteriorate the device retention performance. The simple and reliable di-block co-polymer process to make core-shell nanocrystal memory may open new opportunities for memory applications.

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3.3 Temperature-dependent electron transport in highly ordered Co/Al_2O_3 core-shell nanocrystal memory synthesized with di-block co-polymers

3.3.1 Introduction

Nonvolatile memory devices with floating-gate architectures are widely used in many of the current electronic devices, specifically flash driver, digital cameras, and memory cards [1]. Scaling limitations in conventional floating gate nonvolatile memories have led to the development of novel memory devices that allow for high density storage [2-4]. Nonvolatile memory with discrete-trap type storage nodes, particularly nanocrystal (NC) trap storage nodes, has attracted much attention as a promising candidate for future low power electronics [5-9]. New types of NC floating dots, such as double Si dots [10], Ge nanocrystals [11], metal [12] or metal-like [13] dots and dielectric NCs (Al_2O_3, HfO_2, Si_4N_3, etc) [14-16], have been proposed to achieve memory devices with long retention performance. Among these efforts, metallic NCs have some advantages over the proposed semiconductor NCs, such as higher density of states around the Fermi level with a smaller energy perturbation. Furthermore, the metallic NCs form deep quantum wells between a control oxide and a tunnel oxide due to large work functions [17-18]. Recently, several approaches to fabricate high density core-shell NC memory devices have been implemented to achieve improved performance [19-20]. Co/Al_2O_3 core-shell NC memory, using Fowler–Nordheim (FN) tunneling for program/erase (P/E) operation, has been demonstrated to achieve enhanced retention performance without sacrificing P/E speed.

Uniformly distributed NCs assembled by di-block co-polymer were employed in the devices, which is promising for improving device performance, scalability and manufacturability [20]. In most nonvolatile memory works, the P/E characteristics are usually investigated at room temperature, and direct experimental observations of temperature dependent P/E characteristics are very rare [21-24]. The ambient temperature can vary significantly during operation of nonvolatile memory, therefore, it is essential to investigate the temperature effect on the memory performance and to estimate the performance of memory embedded circuit under different ambient temperatures [25]. In this section, we report the temperature-dependent P/E and retention characteristics of di-block co-polymer assembled core-shell NC nonvolatile memory.

3.3.2 Experiment

Figure 3.3.1(a) shows the cross-section schematic of the core-shell NC metal oxide semiconductor (MOS) capacitor memory. The device consists of a 3-nm thermally grown SiO_2 layer on Si (100), a layer of Co/Al_2O_3 core-shell floating gate fabricated using a PS-B-P (4VP) di-block co-polymer process of Co NCs followed by atomic layer deposition of Al_2O_3, respectively. Finally, a SiO_2 control oxide of about 15nm was deposited using a LPCVD process and an Al metal gate contact was evaporated onto the stack. The detailed fabrication process is reported in chapter 3. Fig. 3.3.1 (b) and (c) show the atomic force microscope (AFM) images of the Co NCs on top of Al_2O_3 layer with di-block co-polymer and core-shell NCs, respectively. The NC arrays are well ordered with uniform size and

spacing between particles, resulting in a density of ~5x10^{11} NCs/cm^2. The average diameter of the NCs is determined to be ~6 nm with an average distance spacing of ~14 nm.

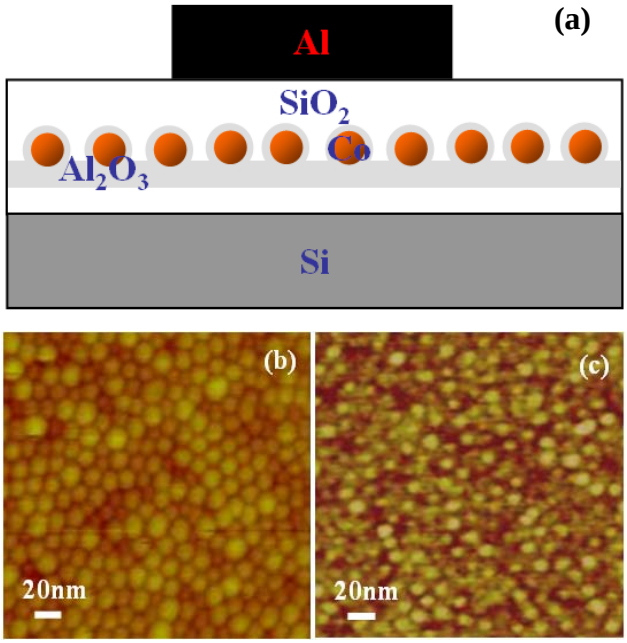

Fig. 3.3.1 (a)Schematic cross section of core-shell NC memory; (b) AFM image for Co NCs with di-block co-polymer on Al_2O_3 surface (c) AFM image for core-shell NCs.

3.3.3 Results and Discussion

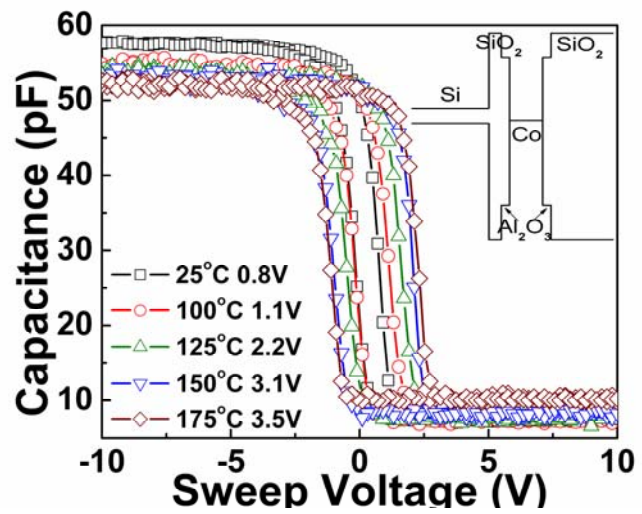

Fig. 3.3.2 C~V sweep memory window for core-shell NC memory at different temperature. Inset is flat band diagram of the device.

The MOS capacitor memories were characterized using an Agilent LCR meter at various substrate temperatures. Figure 3.3.2(a) shows typical high-frequency (1MHz) capacitance-voltage (C-V) response using a scanning range between ±10 V for the fabricated core-shell NC memory devices with a scan rate of 0.5 V/s. At 25°C, the capacitor memory window of 0.8V was achieved. As expected, increasing the temperature causes an increase of the memory window due to thermal energy aiding in the tunneling of electrons through the oxide layers. As the temperature increases from 100 °C to 175 °C at 25 °C intervals, a maximum memory window of 3.5 V was obtained. At 175 °C, the NC arrays become saturated and are no longer able to accept more electrons, limiting the window to 3.5 V.

Figures 3.3.3 (a) and (b) show P/E characteristics of the core-shell NC memory measured at different P/E gate bias at 25 °C and 125 °C, respectively. As shown in Fig.

3.3.3 (a), using a gate bias of 6 V, the flat band voltage shift (ΔV_{FB}) is only 0.2V, which is believed to be caused by direct tunneling of the electrons. Increasing the gate bias to 16V increases the ΔV_{FB} to 1.1 V and 1.8 V for the two temperatures, respectively. The increase in ΔV_{FB} confirms that more electrons are activated then injected and trapped in the NCs at higher temperatures, which are considered to be caused by thermally assisted activation. More importantly, the increase of ΔV_{FB} indicates that the programming efficiency is increased at higher temperatures. The physical process of the electron transport in the memory capacitor is illustrated in the inset of Fig. 3.3.3 (a), red color illustration shows more electrons are activated at higher temperature. Similarly, with the application of a negative gate bias, the ΔV_{FB} increases with temperature from 1.0 V to 1.3 V as shown in Fig. 3.3.3 (b). Similar with programming case, the increase of ΔV_{FB} indicates electrons are erased from the NCs at a higher rate due to the increased thermal energy of the electrons at higher temperature. The inset in Fig 3.3.3 (b) shows the band diagram depicting erasing process, which indicates that more trapped electrons are activated and tunneling back to substrate, leading to large ΔV_{FB} shift. To quantitatively clarify the relation between programming/erasing speeds and temperatures, self-consistent calculation of Schrodinger equation and Poisson equation was carried out to obtain the programming/erasing speeds for one electron to go through the tunneling layer at the temperature of 25 °C, 125 °C and 175 °C and at different gate voltage, which is shown in Fig. 3.3.3 (c) and Fig. 3.3.3 (d), respectively. Detailed information about self-consistent calculation can be found elsewhere [7]. The temperature is found to follow an exponential relation with programming/erasing speeds as a result of temperature-

dependent Fermi-Dirac distribution function, which is shown as solid fitting curves. The straightforward exponential relation between temperature and programming/erasing speeds indicates the temperature assisted effect in NC nonvolatile memory device.

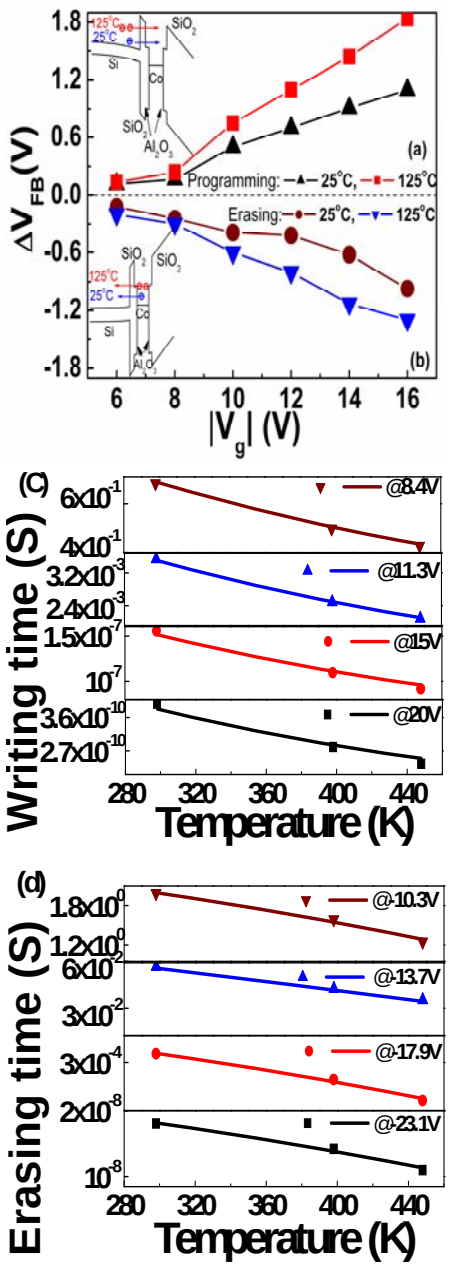

Fig. 3.3.3 (a) Programming and (b) erasing characteristics for core-shell NC memory at 25°C and 125°C, respectively. (c) Programming and (d) erasing speed change with temperature at different gate voltage in core-shell NC memory, respectively. In (c) and (d), symbols are simulated results, solid lines are fitting results. The fitting results show the exponential relationship between programming/erasing speed and temperature.

Figure 3.3.4 (a) shows retention characteristics at 25 °C, 100 °C, and 125 °C to determine the effect of temperature on measured lifetimes. Initial flat band voltage shift for the device is 1.9V at room temperature, 2.1V at 100 °C and 2.2V at 125 °C respectively. At room temperature, the remaining charge ratio is ~70% after 10^5 s. When the charge retention curve is extrapolated to 10 years, the remaining charge ratio is predicted to be ~50%. Increasing the operating temperature to 125 °C, only 20% of the charge is predicted to remain in the NCs. Clearly, the retention performance degrades as temperature increases. In order to quantify this temperature dependence, the retention time τ is extracted from the charge ratio at 90 %, 80 % and 70 %, shown in the insert of Fig. 3.3.4 (a). The inset plots τ as a function of the reciprocal of the thermal energy 1/(kT). Assuming the retention rate follows the first-order temperature dynamics, as defined by the Arrhenius equation: $\tau_r = \tau_0 e^{E_A/kT}$, it is possible to extract the activation energy, E_A, for the charge loss process from the linear fit of the exponential graph [26]. According to the fitting, the E_A were found to be 0.17 eV, 0.19 eV, and 0.22 eV for 90%, 80%, and 70% charge remaining ratios, respectively. According to experiment results and subsequent calculation through $\Delta V_{FB} = \frac{Q_{OX} T_{COX}}{\varepsilon_{OX}}$, the number of electrons stored per dot is found to be ~6. Combining the values of E_A with the quantum well depth of 3.6eV for 0% charge remaining ratio, an exponential decay fitting is found to match the data points and the electron occupying energy levels are obtained from the fitting curve, as shown in Fig. 3.3.4 (b). The high occupying energy level results in the high leakage rate after the charge was programmed into the NCs. As the electron numbers decrease, the Al_2O_3 layer acts as

a barrier for the electrons, preventing the leakage, yielding longer retention times and an improved performance. Nevertheless, E_A is found to follow the relation of ln (n), n is occupying electron numbers, which indicates the electron occupation in the practical device.

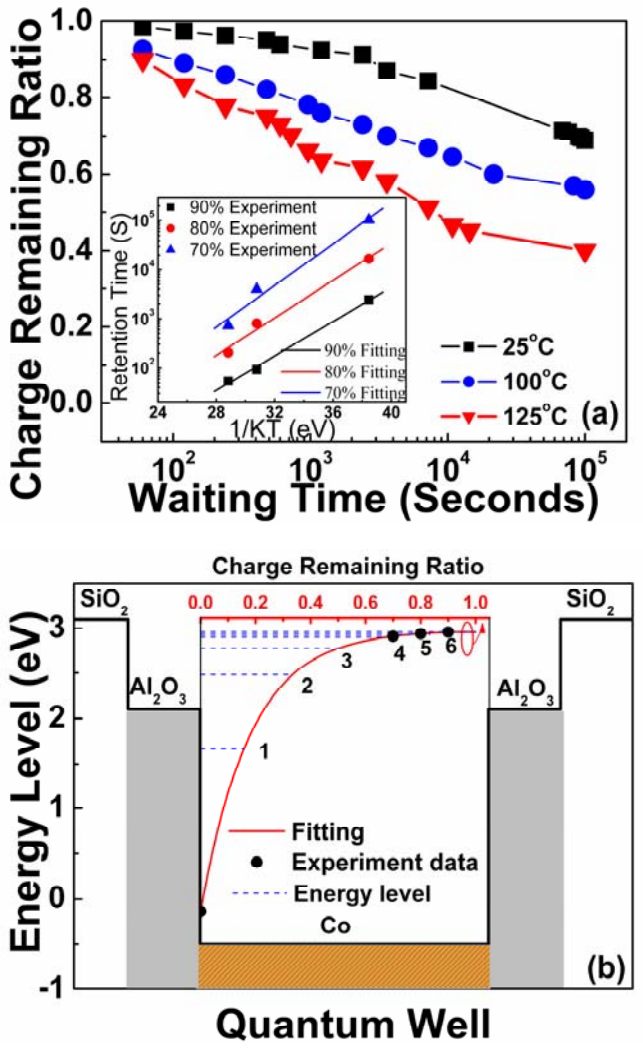

Fig. 3.3.4 (a) Retention characteristics for core-shell NC memory at different temperature, inset image shows linear fitting of E_A, (b) Occupying energy level of stored electrons by fitting which quantitatively explains the electron transport in retention.

3.3.4 Conclusion

In summary, the temperature-dependent electron transport properties in an ordered Co/Al_2O_3 core-shell NC MOS memory have been studied. The memory window increases with ambient temperatures, from 0.8V to 3.5 V with the substrate temperature increased from 25°C to 175°C. When operated at elevated temperatures, more electrons are able to tunnel into and out of the Co NCs due to an increased thermal energy, resulting in an increase in ΔV_{FB}. Programming and erasing performance is found to follow the exponential relation with ambient temperature by self-consistent calculation and fitting. Additionally, the retention performance indicates the increased thermal energy aids the tunneling of electrons out of the NCs, decreasing the overall retention times. Considering the exponential relationship between thermal energy and the retention time, a curve was fitted based on the measured leakage ratio and E_A was extracted for the trap states. The electron occupation states, which follows the relation of ln(n) with n, the occupying electron numbers, are achieved from the temperature dependent retention result, showing clear physical mechanism of electron transport in retention.

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Chapter 4: Rapid thermal oxygen annealing formation of nickel silicide nanocrystals for nonvolatile memory

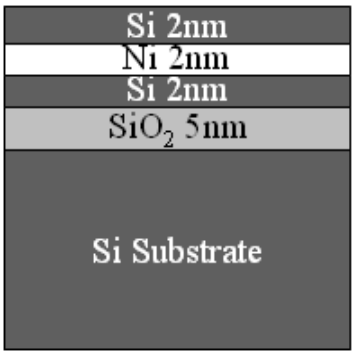
4.1. Introduction

A great deal of current research is focused on seeking a solution for the continued scaling of nonvolatile memory [1-2]. Nanocrystal (NC) based memory devices have been extensively studied since they were discovered by Tiwari et al. [3] Memories based on NCs synthesized by different ways, such as chemical/physical vapor deposition (CVD/PVD) [4-6], vapor solid solid (VSS) growth [7], evaporation [8] and chemical synthesis [9] were fabricated in order to improve the device performance. Furthermore, new types of NC floating dots, such as Ge NCs [10], metal [11-14] or metal-like [15] dots and dielectric NCs (Al_2O_3, HfO_2, Si_3N_4, etc) [16-18], were used to achieve memory devices with prolonged retention performance. Among these materials, silicide was recognized as a good candidate for a floating gate due to its high thermal stability and large work function [19]. However, discrete NCs formed by the above methods often have sphere or dome shape. Subsequent control oxide growth leads to very rough control oxide surface as the layer follows the shape of the NCs. It leads to high possibility of forming leakage paths between the pit region of the control oxide surface and NCs due to electric field concentration effect [20]. Therefore further scaling down NC memory by shrinking both tunnel oxide and control oxide thickness for low-power operations is severely limited.

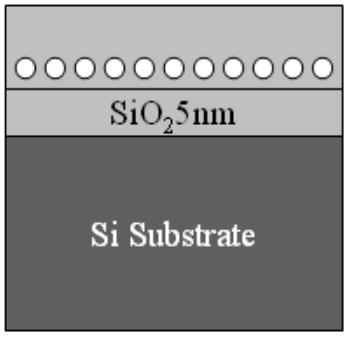
To achieve both high thermal stability of NCs and low leakage possibility between control gate and NCs, in this work, we carried out in-situ RTO annealing of a two-dimensional Si/Ni/Si multi-layer structure to form NiSi NCs. Flat surface is formed on control oxide after RTO annealing process, which reduces the leakage paths in the top control oxide and improves the retention performance.

4. 2 Device fabrication and characterization

The RTO annealing process of fabricating NiSi NCs began with a 5-nm thermal oxide deposition at 850 °C. Si, Ni, and Si thin films of 2 nm each were grown sequentially in an electron beam evaporation system. Then the annealing procedure was performed in oxygen at 650 °C for 30 s to form NiSi NCs. Transmission electron microscopy (TEM), atomic force microscopy (AFM), and x-ray photoelectron spectroscopy (XPS) were used to characterize the morphology and chemical nature of the NCs. The sample was then capped with control oxide of about 20 nm in a low-temperature oxide CVD furnace. The process of in-situ formation of NCs is illustrated in Fig. 4.1. Electrode was then patterned to form metal-oxide-semiconductor (MOS) capacitor memory structure. The MOS capacitor memory was characterized using an Agilent LCR meter at room temperature. Typical high-frequency (1MHz)



RTO



LTO

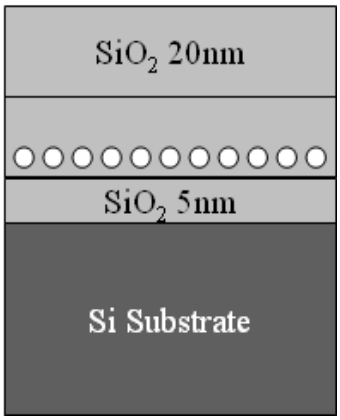


Fig. 4.1 Process flow for NiSi nanocrystal memory by rapid thermal oxidation (RTO).

capacitance-

voltage (C-V) sweep operations with a scanning range between ±18 V to ±22 V were used for the device. The sweep started from the inversion to the accumulation, and finally back to the inversion region at a rate of 0.5 V/s.

4.3. Results and discussion

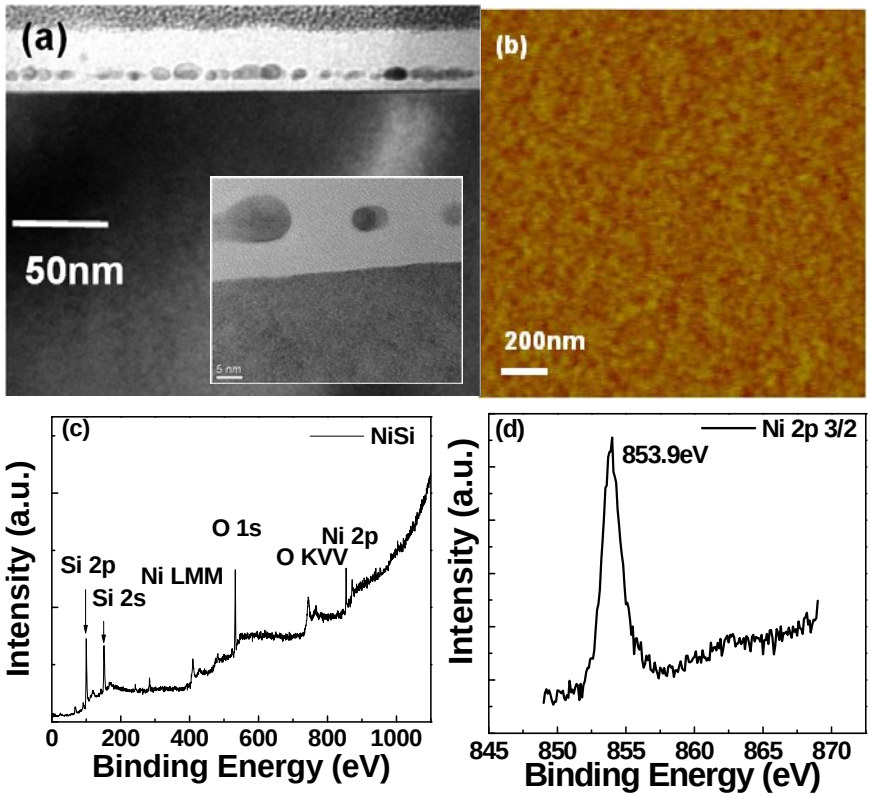


Fig. 4.2 (a) Cross-sectional TEM bright-field image of NiSi NC memory. The inset is a high-resolution TEM image of NiSi NCs, (b) AFM image of NiSi NC layer, (c) XPS survey spectrum of NiSi NCs on SiO_2/Si substrate, and (d) high-resolution scan of the Ni 2p peak.

Figure 4.2 (a) shows a cross-sectional TEM image of NiSi NCs memory. The small inset in Fig. 4.2(a) shows a high-resolution TEM image of NiSi NCs, indicating that these NCs are in sphere shape. The lattice constant of the NCs of 2.6Å obtained from TEM imaging suggests that the material is of NiSi phase [21]. Fig. 4.2 (b) shows an AFM image of NiSi NCs after RTO annealing process. Root-mean-square (RMS) roughness of only 1.5 Å is achieved. The smooth surface of the NC layer allows the subsequent control oxide layer to be smooth across the cell area, which cannot be done in other NC formation processes. Both smooth tunnel oxide and control oxide in this device can reduce leakage paths, therefore prolonging the retention. An XPS survey spectrum collected from the NCs is shown in Fig. 4.2(c).

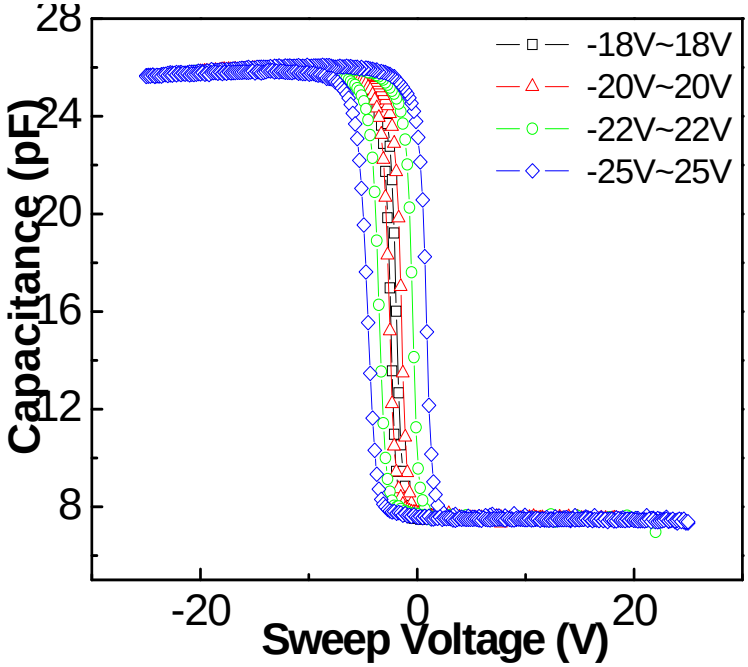


Fig. 4.3 Typical C-V sweeping curves of MOS capacitor containing NiSi NCs.

Fig. 4.2 (d) is the high-resolution spectrum of the Ni 2p level. The peak of Ni 2p3/2 exists at 853.9eV, which is associated with the stable silicide state of NiSi [22-25].

Figure 4.3 shows C-V sweeping curves for the voltage ranges of -18~18 V, -20~20 V, -22~22 V and -25~25 V. A small memory window of ~0.4 V is shown at ±18 V sweeping. As the sweeping voltage increases, hysteresis becomes evident. When the sweeping voltage range increases to 20V, 22V and 25 V, memory window increases to 1.6 V, 3 V, and 5.6 V, respectively. Wider voltage sweeping range leads to more electrons to be programmed into the NCs and erased from the NCs, and therefore results in larger memory window.

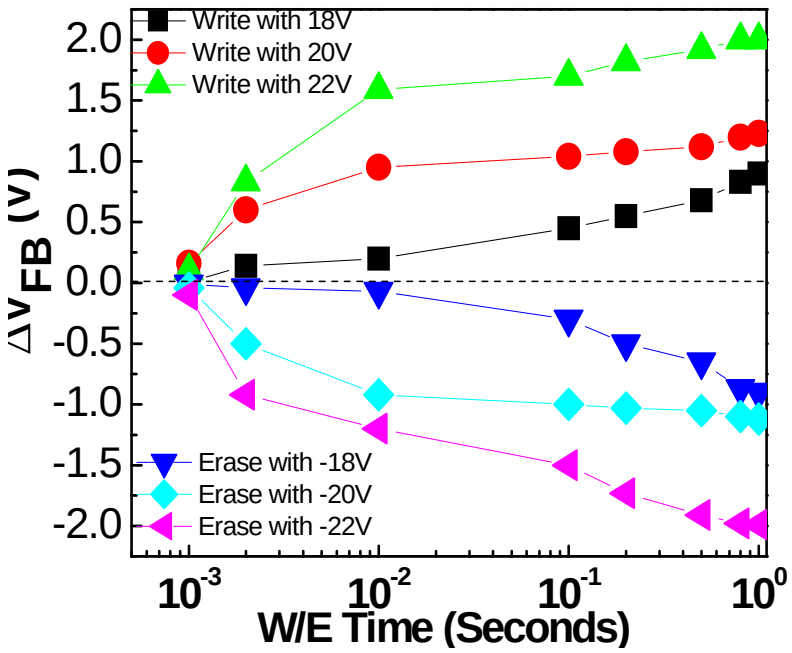


Fig. 4.4 Flat band voltage shift as a function of writing time and erasing time under different writing and erasing voltages.

Figure 4.4 shows the flat band voltage shift (ΔV_{FB}) as a function of writing time and erasing time. It is evident that ΔV_{FB} increases with the increase of the writing time until it finally saturates. This is due to the fact that as the writing time increases, more and more electrons are injected into the NCs until they are unable to accept more electrons. As the writing voltage increases, ΔV_{FB} also increases fast, which indicates that more electrons go through tunnel oxide layer by F~N tunneling at higher voltage. Similar to the writing case, ΔV_{FB} increases with the increase of the erasing time, which indicates that more and more electrons are erased from the NCs. In addition, ΔV_{FB} increases with the increase of the erasing voltage, indicating that more electrons go through the oxide layer by F~N tunneling at higher voltage.

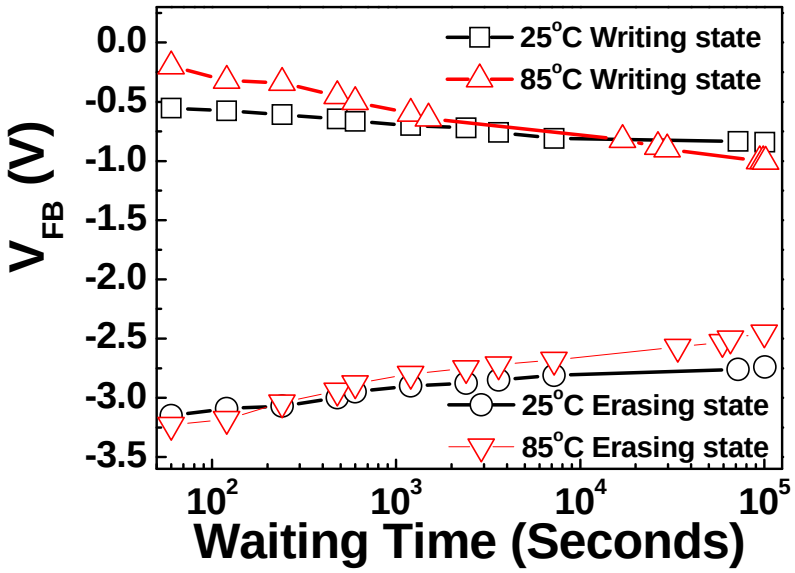


Fig. 4.5 Retention characteristics of MOS capacitor with NiSi NCs. Data retention time is obtained by monitoring the capacitance at zero gate bias after electron charging at 22 V for 100ms or hole charging at −22 V for 100ms, respectively, at both room temperature and 85°C.

Figure 4.5 shows retention characteristics of NiSi NC memory under programmed and erased states at different temperature. The device was programmed and erased with gate voltages of +/-22 V, respectively, for 100 milliseconds at room temperature and 85°C. At room temperature, after 10^5 seconds, the memory window shrinks to 75% of the original value, and from extrapolation, 71% electrons would remain after 10 years. At an elevated temperature of 85°C, the memory window shrinks to 50% of the original value after the same waiting time of 10^5 seconds. When the curves are extended to 10 years, the device can still operate without memory window close up.

4.4 Conclusion

NiSi NCs were synthesized by RTO process to reduce the charge leakage possibilities for future scaled memory devices. MOS capacitor memory with NiSi NCs as the floating gate was fabricated and characterized. Programming, erasing and retention performances were demonstrated. Due to flat surface formation and superior thermal stability properties of the silicide NCs, NiSi NC memory fabricated by RTO process showed wide memory window and high retention performance. The RTO fabrication process to synthesize NiSi NC is also easy to be implemented, which is promising for future nonvolatile memory technologies.

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Chapter 5: Conclusion

(1) We have successfully fabricated $TiSi_2$ coated Si nanocrystal memory devices by self-aligned silicidation method. Due to $TiSi_2$ induced low energy levels, the charge storage occurs mainly in the $TiSi_2$ layer. Therefore, as compared to the reference Si nanocrystal memory, the memory device with $TiSi_2$ coated Si nanocrystals shows a larger charge storage capacity, higher writing and erasing speed and much better retention performance.

(2) We fabricated $TiSi_2$ nanocrystal memories by two-step annealing process. Compared with the reference Si nanocrystal memory, $TiSi_2$ nanocrystal memory shows larger memory window, faster writing, erasing speed and better retention performance. Schrodinger equation and Poisson-Boltzmann's equation were combined to do self-consistent calculation to clarify the physical mechanism. Metallic $TiSi_2$ nanocrystal embedded memory shows higher electric field in tunneling oxide region leading to easier F~N tunneling, which explains faster writing and erasing performance in $TiSi_2$ nanocrystal memory. $TiSi_2$ nanocrystal memory also shows better retention performance in the calculation which matches the real device characterization.

(3) A core-shell NC MOS memory was demonstrated. Uniform NC size and spacing are obtained by a di-block co-polymer fabrication process. The uniform NC distribution throughout the sample is critical for device scalability, reliability and manufacturability. High-k Al_2O_3 layer is used as shell in the core-shell structure, which improves the

retention performance. Reliable di-block co-polymer process to make metal/high-k core-shell NC memory may open up opportunities for memory applications.

(4) A novel core-shell nanocrystal MOS memory has been proposed and demonstrated. Wide memory windows of 7.9V and 8.4V are achieved at the ±12 V voltage sweep for memories based on randomly distributed and ordered Co/HfO_2 core-shell nanocrystals, respectively. Uniform particle size and spacing are obtained by a di-block co-polymer fabrication process. The uniform nanocrystal distribution throughout the sample is critical for device reliability and manufacturability. A low-temperature core-shell synthesis process minimizes possible reaction between the metal core and tunneling layer that may deteriorate the device retention performance. The simple and reliable di-block co-polymer process to make core-shell nanocrystal memory may open new opportunities for memory applications.

(5) The temperature-dependent electron transport in an ordered Co/Al_2O_3 NC MOS memory is studied. The memory window is shown to increase proportionally up to 3.5 V with the substrate temperature. When operated at elevated temperatures, the electrons are able to tunnel into and out of the Co NCs due to an increased thermal energy, resulting in an increase in ΔV_{FB}. Additionally, the retention performance indicates the increased thermal energy aids in the tunneling of electrons out of the NCs, decreasing the overall retention times. Considering the exponential relationship between thermal energy and the retention time, a curve is fitted based on the measured leakage ratio and E_A is extracted

for the trap states. The electron occupation states are also achieved from the temperature dependent retention result, which shows clear physical mechanism of electron transport in retention.

(6) NiSi NCs were synthesized by RTO process to reduce the charge leakage possibilities for future scaled memory devices. MOS capacitor memory with NiSi NCs as the floating gate was fabricated and characterized. Programming, erasing and retention performances were demonstrated. Due to flat surface formation and superior thermal stability properties of the silicide NCs, NiSi NC memory fabricated by RTO process showed wide memory window and high retention performance. The RTO fabrication process to synthesize NiSi NC is also easy to be implemented, which is promising for future nonvolatile memory technologies.