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UNIVERSITY OF CALIFORNIA, SAN DIEGO

**Design of Millimeter-wave Power Amplifiers using InP Heterojunction
Bipolar Transistors**

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Tomás O'Sullivan

Committee in charge:

      Professor Peter M. Asbeck, Chair
      Professor Robert Bitmead
      Professor William Griswold
      Professor Lawrence Larson
      Professor Gabriel Rebeiz

2009

The dissertation of Tomás O'Sullivan is approved,

and it is acceptable in quality and form for publi-

cation on microfilm and electronically:

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Chair

University of California, San Diego

2009

DEDICATION

For Anu, whose endless love and support

inspires me everyday.

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Finally, I wish to thank my parents for supporting me throughout my long journey to this point. Their support, love and encouragement has always been a constant help in everything I do. The last (but not least) person to thank is my wife, Anu. Her love, kindness, support and laughter have helped me immensely throughout the course of my graduate school career. She has been through as much as I have in completing this work, and I look forward to sharing the rest of our lives together.

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PUBLICATIONS

T. O'Sullivan and P. M. Asbeck, "Design of Cascode Power Cells and Monolithic Power Combiner for InP HBT-based Millimeter-wave Power Amplifiers", submitted to *IEEE Transactions on Microwave Theory and Techniques*, 2009.

T. O'Sullivan, M. Urteaga, R. Pierson and P. M. Asbeck, "InP HBT Millimeter-wave Power Amplifier Implemented using Planar Radial Power Combiner", *IEEE MTT-S International Microwave Symposium Digest*, volume 3, June 2008.

T. O'Sullivan and P. M. Asbeck, "Investigation of RF de-embedding approaches for device characterization", *70th ARFTG Measurement Symposium*, November 2007.

T. O'Sullivan, M. Le, P. Partyka, R. Milano and P. M. Asbeck, "Design of a 70 GHz power amplifier using a digital InP HBT process", *Bipolar Circuits and Technology Meeting (BCTM)*, October 2007.

T. O'Sullivan, P. M. Asbeck, J. C. Li and B. Brar, "InP HBT modeling for mm-wave amplifier applications", *Compact Modeling for RF (CMRF) Workshop*, October 2007.

T. O'Sullivan and P. M. Asbeck, "A dual mode branchline coupler for reconfigurable power amplifiers", *IEEE Power Amplifier Symposium*, January 2006.

T. O'Sullivan, R. A. York, B. Noren and P. M. Asbeck, "Adaptive duplexer implemented using single-path and multipath feedforward techniques with BST phase shifters", *IEEE Transactions on Microwave Theory and Techniques*, volume 53, issue 1, January 2005.

T. O'Sullivan, R. A. York, B. Noren and P. M. Asbeck, "Adaptive duplexer implemented using feedforward technique with a BST phase shifter", *IEEE MTT-S International Microwave Symposium Digest*, volume 3, June 2004.

ABSTRACT OF THE DISSERTATION

Design of Millimeter-wave Power Amplifiers using InP Heterojunction Bipolar Transistors

by

Tomás O'Sullivan

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2009

Professor Peter M. Asbeck, Chair

The focus of this dissertation is on the development of high power, monolithically integrated amplifiers for millimeter-wave wireless communication systems utilizing InP DHBT devices. Due to the ever increasing bandwidth requirements of wireless communications systems, the large amount of spectrum available at millimeter-wave frequencies is making these frequency bands increasingly more relevant. This spurs the need for the development of the various circuit and system building blocks required for implementation of reliable communications systems taking advantage of these wide-band channels.

The challenges posed in the development of millimeter-wave power amplifier design range from device model development, to circuit design aspects and also compact power combiner design. The large signal nature of power amplifier operation

requires device models, which accurately capture the nonlinear and heating effects of the devices used in the power amplifier design. Techniques for the measurement and model extraction of InP DHBT devices for millimeter-wave applications are discussed in detail.

As part of the design of a compact millimeter-wave power amplifier, the optimum design of thermal ballasting networks and cascode termination impedances are described. Design tradeoffs in the choice of load resistance for the design are also explained. Using these techniques, a compact power amplifier operating at 72GHz was designed exhibiting 20.6dBm output power and 13.9% PAE.

Finally, the design of a novel planar radial power splitter and combiner architecture is described. Transmission lines, vertical transitions and microstrip crossovers required for the implementation of this structure are explained in detail. Using this structure a high power amplifier is designed with a center frequency of 72GHz. This amplifier demonstrates an output power of 24.6dBm along with a PAE of 8.9%.

Chapter 1

Introduction

In recent years there has been an explosion in the use of wireless communications for a variety of applications. The increase in the amount of data transmitted wirelessly has led to high demand for high bandwidth and high data-rate wireless communication systems. In this chapter the possibilities of millimeter-wave frequency bands for high data-rate wireless communication systems will be discussed, as well as the suitability of Indium-Phosphide (InP) hetero-junction bipolar transistors (HBT's) for implementing these systems.

1.1   Millimeter-wave wireless communications

In recent years wireless communication systems have been emerging at ever higher frequencies including 24GHz [1, 2], 40GHz [3, 4], 60GHz [5, 6], E-Band [7] and 77GHz [8, 9]. This trend is driven by the increasing demand for wireless transmission of large bandwidth signals such as wireless HDMI, streaming internet content, digital TV, automotive radar and 3G and 4G cellular.

50MHz   8GHz

TV Broadcast, Radio Broadcast, Mobile Phones, Wireless
Networking, GPS, Amateur Radio, UWB communications etc.

71GHz   76GHz

81GHz   86GHz

91GHz   94GHz

13GHz Spectrum allocation for E-band communication systems
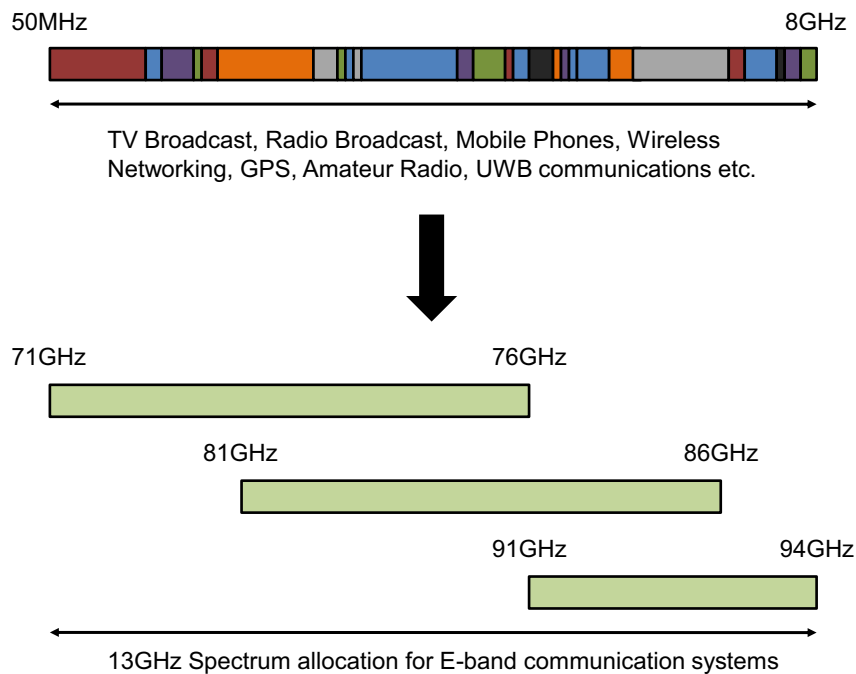
Figure 1.1: Channel bandwidth comparison between E-band radios and sub 8 GHz communication systems

Expanding the information handling capability of a wireless communication system can be achieved by two methods; (1) increasing the modulation order of the communication system to increase the amount of information transmitted for a given channel bandwidth or (2) increasing the channel bandwidth, while keeping the

modulation order low. At lower frequencies where the spectrum is more congested and expensive the first method is pursued. The disadvantage associated with increasing the modulation order is that the signal possesses an increasing peak to average ratio. This results in very stringent linearity requirements being placed on both the transmit and receive circuit blocks to prevent corrupting the signal and resulting in data loss.

At millimeter-wave frequencies, the approach of expanding the channel bandwidth is possible by utilizing the large amounts of spectrum available. The vast difference between available channel bandwidths at millimeter-wave and sub 8 GHz frequencies is illustrated in figure 1.1. For low frequencies, channel bandwidths are limited to less than 50 MHz, whereas for the E-band radio system, channel bandwidths ten times larger are available. By following the approach of widening the channel, the linearity requirements of the transceiver can be relaxed, due to the use of a simpler modulation scheme. Hence the design can focus on the challenge of simple and compact chipset development for millimeter-wave wireless systems.

The major bandwidth allocations for millimeter-wave wireless are 60GHz and E-band. For 60GHz wireless communications there exists worldwide ISM (instrumentation, scientific and medical) bands. These bands are 59GHz-66GHz and 57GHz-64GHz for Japan and the USA respectively. These bands present the opportunity for the development of wireless links with capacities approaching 1Gbps. The other millimeter-wave band allocated in the USA is for E-band communications. This consists of frequency bands from 71-76GHz, 81-86GHz and 91-94GHz for a total of 13GHz of available spectrum. The large amount of bandwidth available in these frequency

bands allows for larger channels with more information handling than possible at lower frequencies.
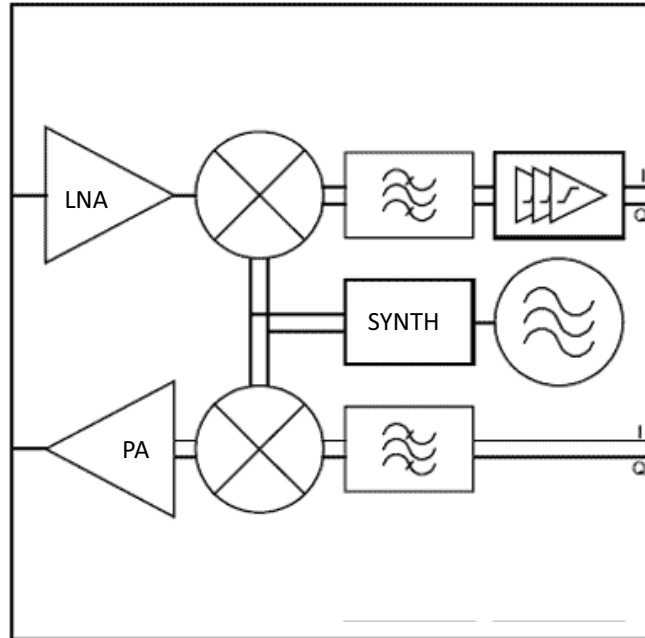
Figure 1.2: Simplified transceiver block diagram

1.2   InP HBT's for millimeter-wave applications

Many technology choices are available for the realization of millimeter-wave trans-ceivers which have different trade-offs. Firstly, at millimeter-wave frequencies, integration of as many analog blocks as possible in a single chip is very desirable. This is due to the fact that the off-chip to on-chip transitions needed in a multi-chip design are difficult to design robustly, and introduce significant losses to the signal

Table 1.1: Comparison of device technologies for millimeter-wave wireless design

Technology	Integration	Ft/Fmax	Voltage Handling
InP DHBT	Medium/High	>500GHz	Medium
SiGe HBT	High	>400GHz	Low
CMOS	High	>300GHz	Lowest
GaN HEMT	Low	200GHz	High
InP HEMT	Low	>500GHz	Medium

path.

Another requirement for the successful implementation of millimeter-wave wireless systems is a technology with high Ft (unity current gain) and high Fmax (unity power gain). Without sufficiently high Ft and Fmax (at least 200GHz each) the design of a successful millimeter-wave transceiver is extremely difficult, as multistage amplifiers are required to build up gain in both the transmitter and receiver.

Along with these universal requirements, many of the individual blocks in the system have other requirements from the technology. To illustrate this, a simple transceiver block diagram is shown in figure 1.2. On the receive side, low-noise performance for the low noise amplifier (LNA), as well as high linearity switching devices for the down-converter are required. On the transmit side, good linearity and voltage handling capability for the power amplifier (PA) are of paramount importance. Also important for area savings in the PA design are high power density devices. Integration of the voltage controlled oscillator (VCO) and prescaler on-chip

is also desirable to prevent off-chip routing of the LO waveform. Baseband and other low frequency synthesizer blocks can be implemented separately in a lower cost and lower speed technology. In table 1.2 the possible technology choices for implementing millimeter-wave transceivers are compared with respect to the above requirements.

From this comparison the InP DHBT technology stands out as a good choice for full integration of a millimeter-wave wireless transceiver system. Firstly, it provides the possibility for high levels of integration, not possible in HEMT technologies. Secondly, the high gain and voltage handling capability allow for the development of all required building blocks of a wireless communication system from the LNA to the up- and down- mixers and finally the PA. The DHBT devices also exhibit good linearity and high power density to allow for compact circuit design. With these considerations in mind InP DHBT is chosen as the technology for circuit implementation in this work.

1.3   Design Issues for millimeter-wave Power Amplifiers

The design of the power amplifier block for a millimeter-wave transmitter poses many design challenges. The first of these is at the device model level. The devices in a power amplifier are exercised over a large voltage and current range at the maximum power levels. First pass design success and optimization requires device models, which correctly predict the large signal amplifier performance.

Stabilization of the high-gain transistors required for millimeter-wave design is another important design issue for this block. The power amplifier design requires techniques to ensure unconditional stability of the amplifier core all the way down to DC, while maintaining the amplifier high gain performance at the desired millimeter-wave frequency.

Losses due to transmission line interconnects become significant at millimeter-wave and limit the efficiency achievable in power amplifier design. This drives the need for compact matching network and power combiner design for reduction of transmission line losses. Another aspect of this issue is the development of low-loss transmission line structures to enable more complex power combiner design.

1.4   Scope of dissertation

The focus of this dissertation is on the design of compact power amplifiers for millimeter-wave communication systems, by leveraging the recent technology developments achieved with InP DHBT devices. The main challenges addressed are as follows:

- Compact model extraction for high frequency InP DHBT devices
- Development of compact, high power density cascode power cell
- Design of monolithic planar radial power amplifier

The first step in leveraging the technology advancements of InP DHBT's for millimeter-wave power amplifier design is development of a full set of accurate models,

which is covered in chapter 2. Firstly, the accurate measurement of these high speed and high power density devices is investigated, with particular attention paid to the de-embedding of high frequency measurements. The extraction of the Agilent HBT model to capture the performance of the InP DHBT devices is then described. The measurement and fitting techniques explained here illustrate the steps in developing accurate compact models for these high performance devices.

Following the model development of the previous chapter, the design of a compact power amplifier core is then pursued. Chapter 3 deals first with the choice of amplifier topology. Then the development of a ballasting network, which optimizes both thermal and electrical stability, is described. Finally the important issue of the design of the AC ground impedance at the base terminal of the common-base device in the cascode amplifier is studied in detail, and the optimum distributed capacitance connection is developed. Simulation techniques for embedding the active device models within an s-parameter model for the power-cell core are also presented, which result in successful first pass design of the final power amplifier.

The next chapter deals with the design of a monolithically integrated millimeter-wave power amplifier. Transmission line choices and compact matching network design are first discussed. The design of a 20dBm single stage power amplifier is then presented. This is followed by describing in detail the design of a novel planar radial power splitter and combiner network. Transmission line design, vertical transition design, and microstrip crossover design are all covered. Using this planar radial structure, a high power planar radial power amplifier is presented achieving 24.6dBm

output power.

In the final chapter, the contributions of the thesis are summarized, and some topics for future research in the area are identified.

Chapter 2

InP HBT Measurement and Modeling for Millimeter-wave Applications

As explained in chapter 1, Indium Phosphide (InP) hetero-junction bipolar transistor (HBT) devices are chosen for the implementation of the power amplifier designs described in this thesis. This chapter covers many aspects of measuring and modeling single InP HBT's with the specific goal of millimeter-wave power amplifier design in mind. Firstly, measurement of the HBT devices is discussed with emphasis on the de-embedding of high frequency S-parameters. Extraction techniques for various device parameters are then discussed. Also, the choice of compact model to best fit the devices for the millimeter-wave power amplifier application is discussed.

2.1 Measurement of discrete devices - the need for de-embedding

When measuring any solid state device, it is necessary to remove all effects of the measurement system from the DC and RF results to ensure that the extracted model is based on the intrinsic DUT [10]. In figure 2.1(a) many of the parasitic elements, which are introduced by the measurement system, are illustrated. Also at the wafer level, the device is embedded in a measurement padframe, seen in figure 2.1(b), and this padframe introduces parasitic elements in the measured results. In order to characterize the measurement environment a number of extra measurements are made without the DUT in place. The data from these measurements is then used to model the measurement environment and de-embed the DUT data. Various techniques will now be described for de-embedding DC and RF measurements.

2.2 De-embedding DC measurements

In a DC measurement the only parasitic elements which can be introduced are resistances either in series or shunt with the device under test (DUT). The resistances to be considered here are in series with the HBT terminals as seen in figure 2.2. To calculate these resistances to the device plane, an on-wafer short structure is utilized. A current-voltage plot is obtained for ports 1 and 2 independently and this can be used to get a value for the parasitic resistances in series with the device terminals.
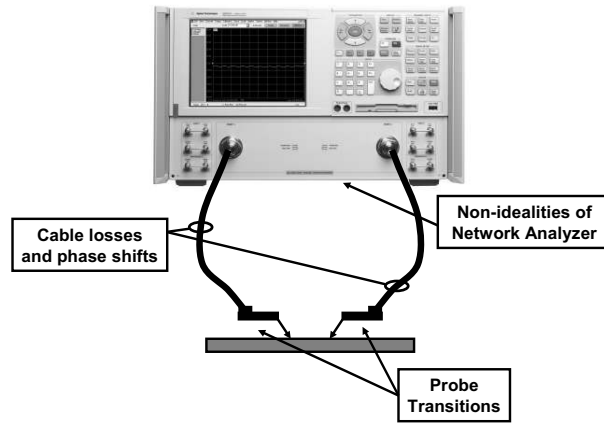
(a) Parasitics from measurement system
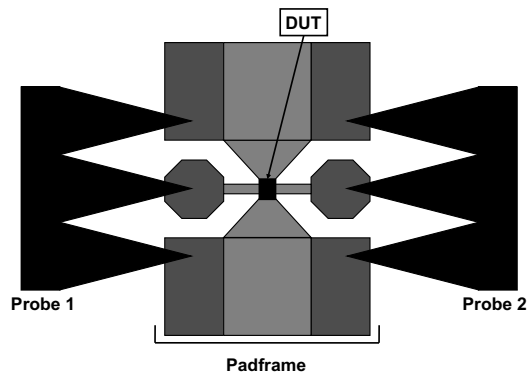
(b) Parasitics from padframe

Figure 2.1: Parasitics introduced in the measurement of devices

For port 1, the measured resistance is the sum of the parasitic base and emitter resistances associated with the measurement system, while port 2 is the sum of the parasitic collector and emitter resistances. Using the extracted values for the parasitic resistances, all DC measurements can be fully de-embedded. For small devices, resistances measured in this fashion are sufficiently accurate ($\pm 0.2\ \Omega$), while for larger

devices (for which devices resistances can be below 100m Ω) Kelvin connections for

resistance de-embedding are required.
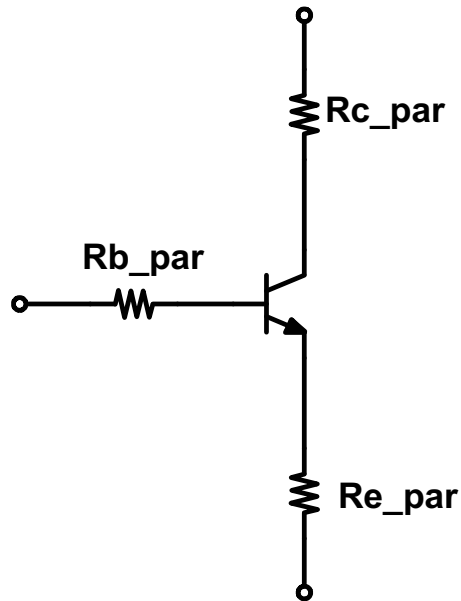
Figure 2.2: Parasitic resistances to be de-embedded for DC data

2.3 De-embedding RF measurements

When de-embedding high frequency measurements the situation becomes more

complex. Reactive parasitic components are now present as well as the resistive ones.

To perform an accurate measurement at high frequencies a 2-tier calibration technique

is employed. Firstly, the system is calibrated off-wafer using a calibration substrate.

This can be done using the SOLT (Short-Open-Load-Thru) [11], LRM (Line-Reflect-Match) [12], LRRM (Line-Reflect-Reflect-Match) [13] or other similar calibration technique to move the reference plane of the measurement to the probe tips. Then a second de-embedding technique is used to remove the parasitics introduced by the device padframe. The most commonly used methods to de-embed padframe parasitics are the Open-Short [14] technique and the TRL (Thru-Reflect-Line) [15] technique. In the following sections these techniques are briefly described. Then a simulation based method is introduced, which is used to compare de-embedding performance across frequency and padframe size.

2.3.1   Open-Short De-embedding

The Open-Short technique assumes a lumped equivalent model of the padframe as shown in figure 2.3, with series impedance and shunt admittance terms. Dummy open and short structures are provided on the wafer, and measurements of these structures lead to the extraction of the impedance and admittance terms of the lumped equivalent padframe model. These terms are then subtracted from the device measurement to give de-embedded results. This technique works well for low frequencies and small padframe sizes. As the frequency or padframe size increases however the lumped approximation to their effect as a single L and single C becomes less valid and so errors are introduced.
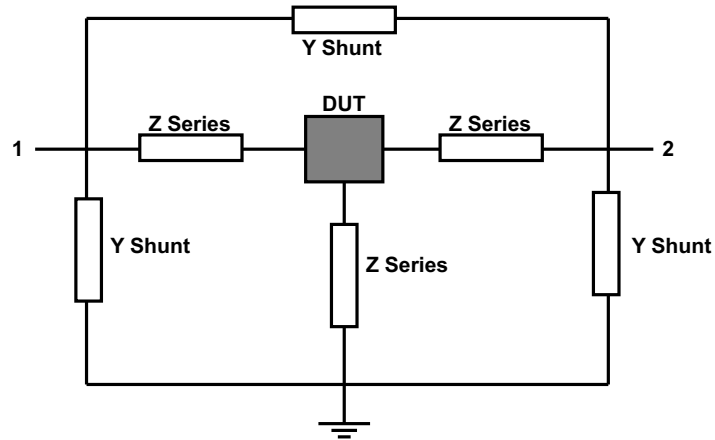
Figure 2.3: Padframe parasitics as represented in Open-Short technique

2.3.2 TRL De-embedding

In contrast to the Open-Short technique, the TRL is a transmission line based algorithm which properly captures the distributed nature of the input and output interconnect parasitics. This results in a band-limited solution with the bandwidth of validity set by the difference in electrical length, ΔL, between the thru and line standards. NIST guidelines [16] specify that the valid frequency range for the TRL algorithm is for ΔL having an electrical length between 30° and 150°. Error box cascading matrices at ports 1 and 2 are solved for using the information from the thru, reflect and line measurements. No lumped equivalent assumptions are made in this technique and so no loss in de-embedding accuracy occurs as the measurement frequency is increased. An important consideration when using the TRL algorithm is that the resulting S-parameters are de-embedded to reference planes at the device. Since this is a transmission line based reference plane shift, the inductance associated

with vias connecting from the transmission lines to the DUT are not removed. This situation is shown graphically in figure 2.4. Additionally, effects of ground inductance for the device cannot be eliminated; the method only succeeds in de-embedding the pads up to the new reference planes close to the device.
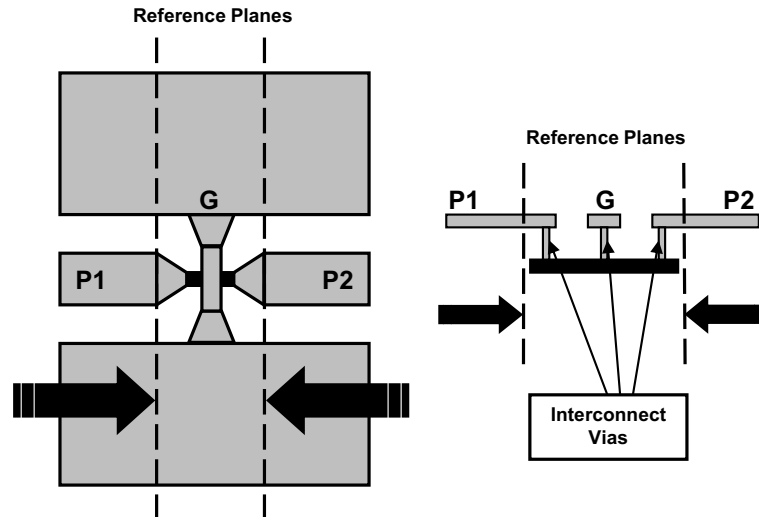
Figure 2.4: Illustration of reference planes after TRL de-embedding with un-deembedded inductance shown

A final important difference between the techniques is that the Open-Short requires only two standards be measured, namely the open and short structures. In the TRL algorithm three standards are required: thru, line and reflect (open or short). If a wider frequency range is required for the TRL then multiple line standards are needed. This leads to the obvious conclusion that the TRL requires more wafer area, a precious resource.

2.3.3 EM Simulation based comparison technique

The goal of this study is to show how much error versus frequency is introduced for a given padframe size. The TRL technique is investigated here in the higher frequency ranges where the errors from the Open-Short technique become significant, giving a measure of the improvement in de-embedding accuracy, which can be achieved with one technique versus another. In this section a technique similar to that adopted in [17] is used.

Two different padframe types are investigated: butterfly padframes, shown in figure 2.5(a), and CPW padframes, shown in figure 2.5(b). Three padframe sizes are investigated, corresponding to three increasing probe pitches of 100µm, 150µm and 200µm. Only the Open-Short method is considered on the butterfly padframes since the butterfly structure is not amenable to thru and line standards. For the CPW padframes both de-embedding techniques will be simulated.

The purpose of using the EM simulation comparison is to reproduce the situation encountered in the measurement domain. In the simulation domain we know the desired device parameters and so the effectiveness of de-embedding can be quantified. Carrying out this study in the simulation domain also allows us to remove any errors associated with the measurement of the DUT and de-embedding structures, such as calibration drift or probing repeatability. In this way we are comparing only the numerical limits of the TRL and Open-Short algorithms in this study.

The perfectly calibrated local port [18] has recently been introduced in the Sonnet [19] electromagnetic simulation software suite. This port type allows an EM
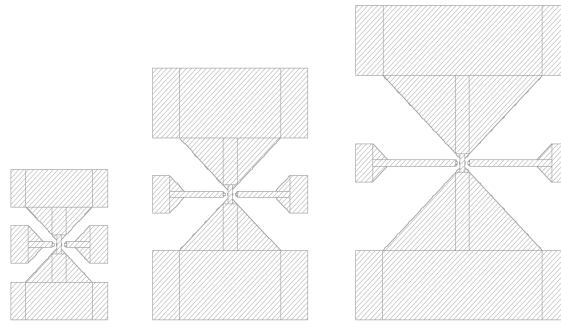
(a) Butterfly Padframes
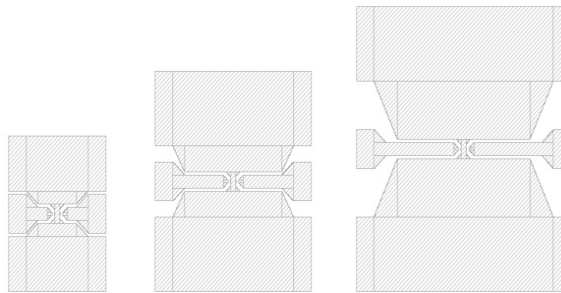
(b) CPW Padframes

Figure 2.5: Different padframe types and sizes to be included in the study

simulation to be performed with both local and global ports present, and the para-

sitics associated with both port types are removed during the solver calibration step.

The concept of a global port has long been established, where the port parameters

are referenced to a global ground point. The internal local ports are referenced to

another ground, termed the generalized local ground (GLG). The calibration step in

the Sonnet tool removes the parasitic capacitance and inductance introduced by the

local ground plane, whereas in other solvers this step does not occur.

A simple simulation study to illustrate this difference was setup as shown in

figure 2.6. Here, two identical microstrip line structures are simulated, with the difference being that for one simulation two local ports are inserted at the midpoint of the line. The s-parameters from each simulation are then compared. With perfect local port de-embedding the s-parameters of the 2-port simulation should be identical to those of the 4-port simulation when ports 3 and 4 are shorted. This study was performed using both the Sonnet and Momentum electromagnetic solvers.
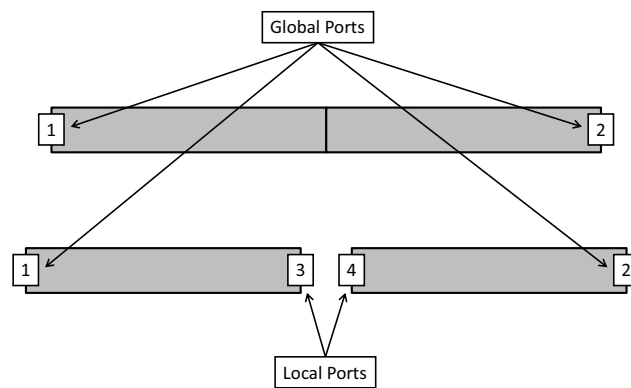
Figure 2.6: Simulation setup for microstrip line with and without local ports

The results of this simulation are plotted in figure 2.7, where the S11 from each simulation is compared. Here it is seen that for the Sonnet simulator with local port de-embedding, the effects of the local ports are fully removed and the the results from the 2-port and 4-port simulations overlap exactly. The results from the momentum simulator show differences between the 2-port and 4-port simulations. These differences are due to the local port parasitics, which are not removed by the Momentum simulator.

There can be multiple GLG reference planes in a single EM simulation, each
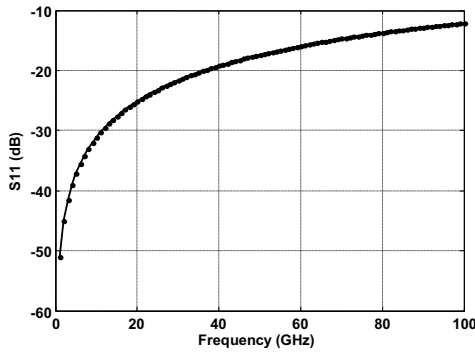
(a) Sonnet simulation results
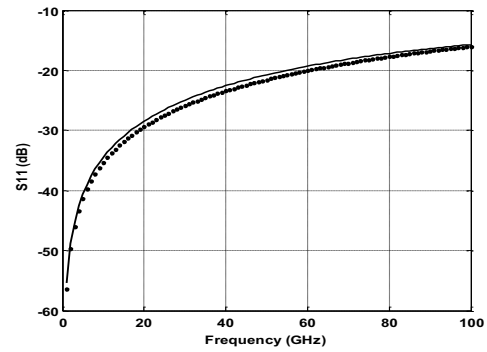
(b) Momentum simulation results

Figure 2.7: GLG de-embedding simulation study results for both solvers (solid: 2 port, dotted: 4 port)

corresponding to a different device. This is illustrated in figure 2.8, where ports one and two are global ports referenced to the global ground and ports three, four and five are local ports referenced to the GLG plane. Using this capability Sonnet can generate five port S-parameters for a DUT structure with two global and three local ports, similar to that shown schematically in figure 2.8. This five port s-parameter block is then imported into the Agilent ADS [20] circuit simulator, where the local ports are used to embed a known device into the DUT s-parameters. This simulation setup is shown in figure 2.9. Here a typical transistor is represented with a small signal model based on lumped elements. This results in a set of two-port S-parameters of a device embedded in a padframe. When using S-parameters in a nodal simulation, all the ports of a given device must be referenced to the same ground plane to ensure correct results i.e. global ports are referenced to the global ground, but local ports must be referenced to internal local grounds and not the global ground.
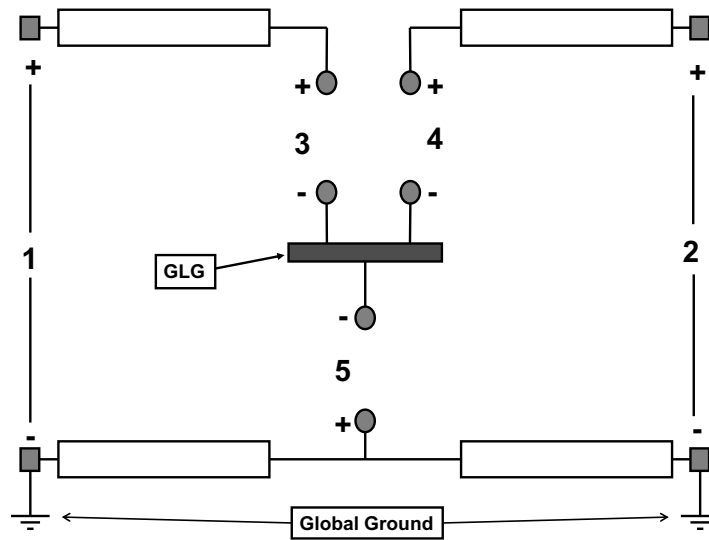
Figure 2.8: Example circuit with both local and global ports

Sonnet is also used to simulate open, short, thru and line standards for each padframe type and size to be investigated. Using these S-parameter files both Open-Short and TRL de-embedding can be performed on the embedded DUT. The resulting de-embedded S-parameters can then be compared to the known device S-parameters to show how accurate the de-embedding has been.

2.3.4   Comparison Results for Open-Short and TRL De-embedding

The previously described technique is now applied to various padframe types and sizes. For each padframe type the following sizes are investigated: 100μm pitch, 150μm pitch and 200μm pitch. The frequency range for the study is 1-100 GHz and
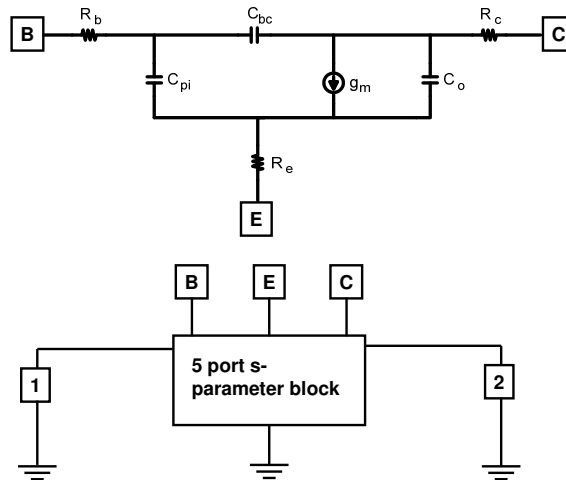
Figure 2.9: Embedding a known device using local ports

the thru and line lengths for the TRL algorithm are chosen to make the TRL de-embedding valid over the span of 20-100 GHz. For frequencies below this range the TRL algorithm is expected to be less effective.

The transistor small signal model used in the simulation corresponds approximately to an InP HBT with f_t=330 GHz and f_{max}=360 GHz. In figure 2.10 the results for a 150μm CPW padframe are shown. S_{11} is plotted on a polar plot showing the results of both de-embedding types along with the true DUT S_{11} and the un-deembedded S_{11}. This plot shows that the different schemes are better over different parts of the plot. The true device S-parameters are plotted with the thick trace. It can be seen that the TRL algorithm diverges from the desired trace at low frequencies and agrees much better at higher frequencies. The opposite is true for the Open-Short trace. The third trace on this plot shows the S_{11}, which would be obtained without

any de-embedding. A frequency point at 20 GHz is marked to provide a reference. To facilitate more straight-forward comparisons between different cases the following measure is used. In figure 2.11, ΔS_{ij} is illustrated. This is the difference between the desired S-parameter, and that which results from de-embedding. ΔS_{ij} includes both amplitude and phase errors introduced by the de-embedding scheme. The final measure used in the comparisons is ΔS_{TOT} which is defined in equation 2.1.

$$\Delta S_{TOT} = \sum_{i,j=1}^{2} |\Delta S_{ij}| \qquad (2.1)$$
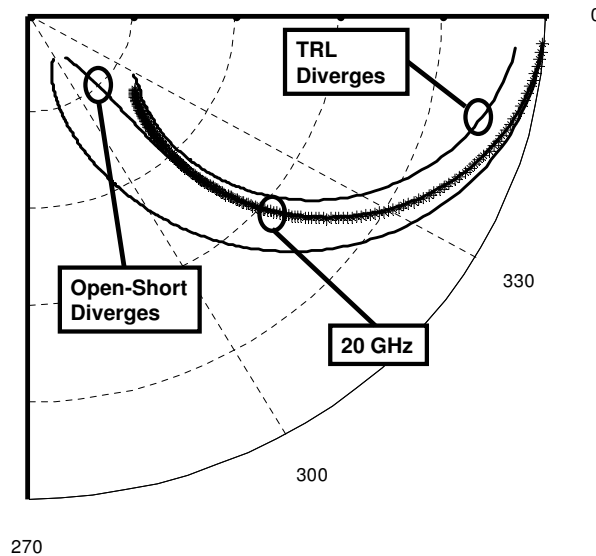
Figure 2.10: S_{11} results for 150µm CPW padframe
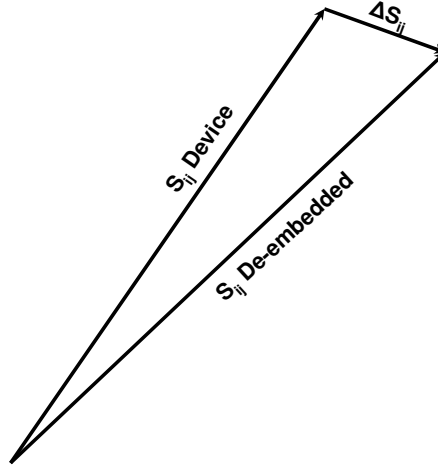
Figure 2.11: Graphical illustration of ΔS_{ij}

It must be noted that with this definition ΔS_{TOT} does not provide any weighting factors for different S_{ij}'s, thus the large S-parameters (such as S_{21}) influence the result more than the small ones (S_{12}). Using the definition of ΔS_{TOT} as described above, the results from the different cases are plotted in figures 2.12, 2.13 and 2.14. In figure 2.12, the performance of the Open-Short technique for three sizes using the butterfly padframe is plotted. Figures 2.13 and 2.14 show results for the CPW padframe. The ΔS_{ij} terms at 20 and 80 GHz for the case of the 150µm butterfly padframe are given in Table 2.1. It can be seen that the error contributed from the $|\Delta S_{21}|$ terms will have more influence on ΔS_{TOT} at lower frequencies, but at higher frequencies $|\Delta S_{11,22}|$ terms dominate.

It is clear from figures 2.12 and 2.13 that the error introduced by the Open-Short de-embedding technique increases with both frequency and padframe size. To
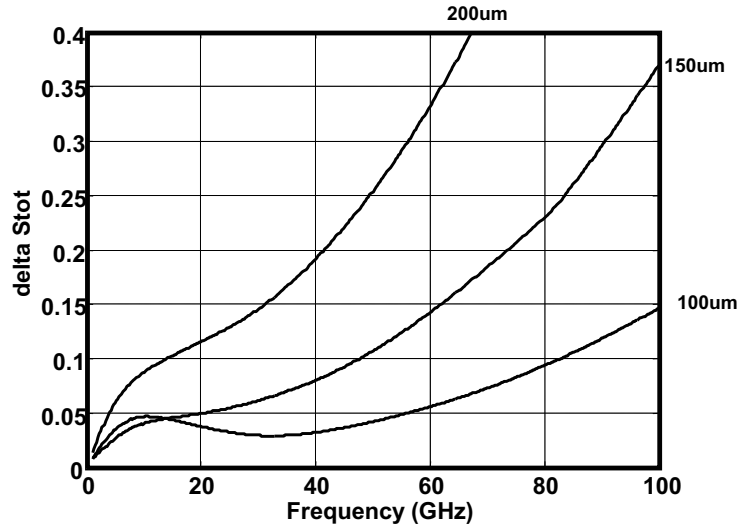
Figure 2.12: ΔS_{TOT} for Butterfly padframes using the Open-Short technique

keep the error below the level of 0.1 for ΔS_{TOT}, the 100µm padframe can only be used up to 80 GHz and the 150µm padframe can only be used up to about 45 GHz. It is also seen that for the same padframe size, the CPW type structure introduces slightly less error in the de-embedded results than the butterfly type structure when the Open-Short technique is used. In figure 2.14 it is shown that the TRL technique works equally well as the padframe size increases. This is expected since the algorithm will move the reference plane to the device equally well, even as the length of connecting transmission line is varied, once the thru and line standards are correctly defined. It is also clear that no advantage is achieved in using the TRL algorithm for the smallest padframe size, but for larger padframes at higher frequencies, TRL is required for accurate de-embedding.

As discussed previously, the TRL algorithm moves the reference planes of the
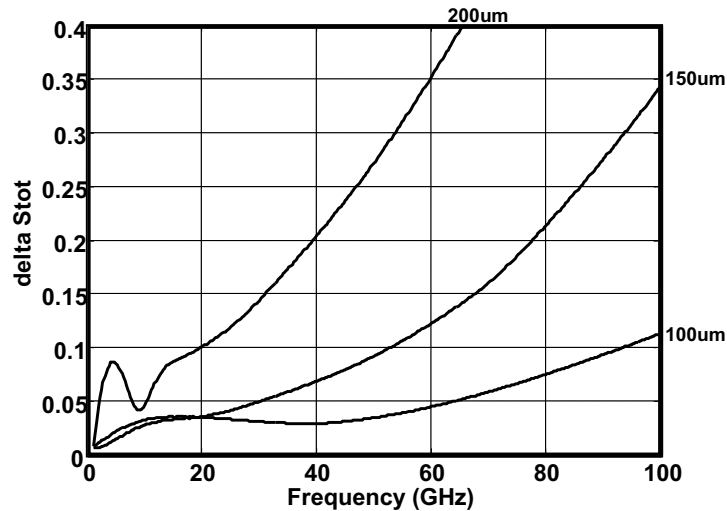
Figure 2.13: ΔS_{TOT} for CPW padframes using the Open-Short technique

measurement along the transmission lines to the device planes. Inductances involved
in bringing the signal from the transmission line to the device ports are not removed
and so in this study they will contribute to the error signal in the TRL algorithm. If
these inductances are included as part of the device model then the TRL algorithm
error signal is greatly reduced. This is shown in figure 2.15 for the 150µm CPW
padframes.

2.3.5   Conclusions of De-embedding Study

From the de-embedding study it was shown that the Open-Short algorithm
performs well up to 50 GHz for the 100µm pitch padframe. Given the improved
performance of the Open-Short algorithm as the padframe size is reduced, one may
think that even smaller padframes would result in even higher frequency performance
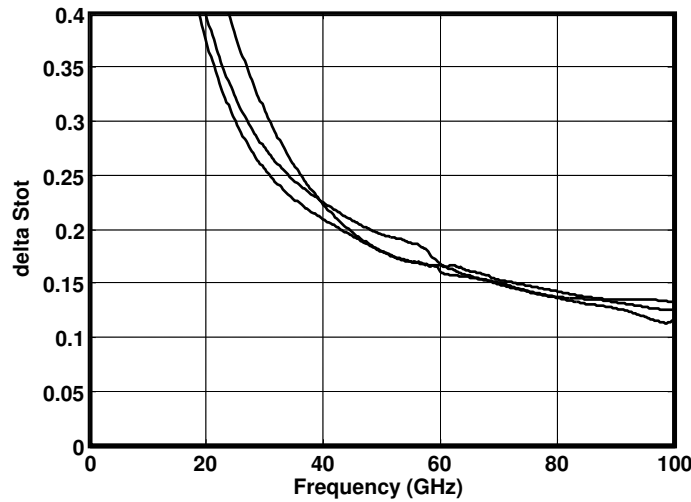
Figure 2.14: ΔS_{TOT} for CPW padframes using the TRL technique

from this simple algorithm. Another important effect is present at high frequencies for small padframes - increased feed-through from probe to probe coupling resulting in poor S_{12} measurements of devices. With this constraint in mind, the following guidelines an be adopted for de-embedding device measurements. For frequencies up to 50 GHz the Open-Short algorithm can be used for good accuracy de-embedding for 100µm pitch padframes - if larger padframes are used this upper frequency is reduced. Beyond this the Open-Short algorithm begins to introduce significant errors, which cannot be reduced by reducing padframe size due to poor S_{12} measurements caused by probe to probe feed-through. Hence at higher frequencies the TRL algorithm is required for accurate de-embedding, while maintaining sufficient isolation between probes with correctly sized padframes.

Table 2.1: ΔS_{ij} at 20 GHz and 80 GHz for 150µm Butterfly Padframe

	20 GHz	80 GHz
$\|\Delta S_{11}\|/\|S_{11}\|$	0.006/0.583=0.010	0.110/0.265=0.415
$\|\Delta S_{12}\|/\|S_{12}\|$	0.001/0.118=0.008	0.010/0.269=0.037
$\|\Delta S_{21}\|/\|S_{21}\|$	0.035/5.673=0.006	0.002/1.854=0.001
$\|\Delta S_{22}\|/\|S_{22}\|$	0.007/0.527=0.013	0.109/0.019=5.737

2.4 Compact Model Choice for High Speed InP HBT Applications

Many options of compact model are available for fitting the characteristics of bipolar devices. The most common models are Gummel Poon [21], VBIC (Vertical Bipolar Inter-Company) [22], MEXTRAM (Most EXquisite TRAnsistor Model) [23], HICUM (HIgh CUrrent Model) [24] [25] and Agilent HBT [26]. The focus of this work is the design of high frequency power amplifier circuits using InP HBT devices. This requires a model which can capture both the high frequency and large signal effects present in III-V HBT devices. The Agilent HBT model was formulated to reproduce the unique characteristics of both GaAs and InP HBT devices and was the model of choice for this work. The integrated non-linear transit time model included as part of the Agilent HBT model allows the complex current and voltage dependance
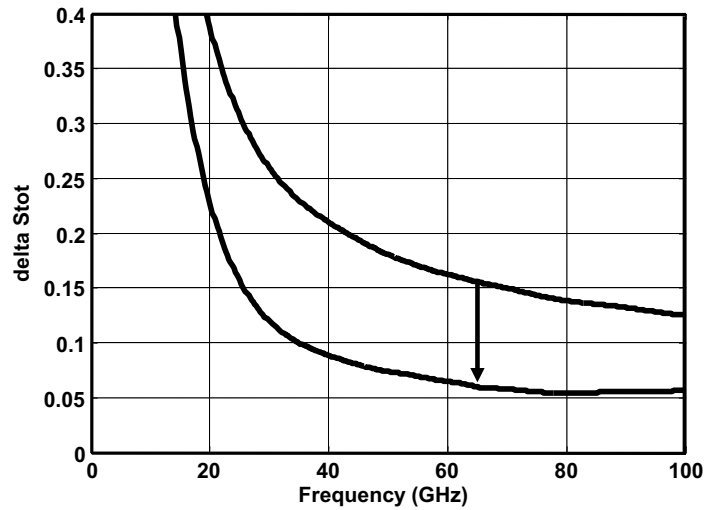
Figure 2.15: Reduction in ΔS_{TOT} for TRL algorithm when via inductance is accounted for

of collector current to be captured accurately. This model also includes a two-pole time constant self-heating network, parameters accounting for hetero-junction effects and a collector-base capacitance model with fully depleted collector effects.

2.5 Measurement Setup and Required Measurements

For complete extraction of all the Agilent HBT model parameters, a full set of both DC and RF measurements over at least two temperatures are required from the devices. A full list of the required measurements is given below:

- Forward Gummel for different collector voltages
- Reverse Gummel

- Base current driven DCIV

- Z_{12} versus bias

- C_{be} and C_{bc} versus bias

- S-parameters versus frequency and bias

- f_t and f_{max} versus bias

All of the measurements are performed at both room temperature and elevated temperature. The measurement setup required to extract this set of data is a semiconductor parameter analyzer, a high frequency network analyzer and a temperature controlled wafer chuck. The full set of measurements is made using the Agilent IC-CAP measurement and modeling software, which is then used to extract the model.

2.6 Extraction Procedure for the Agilent HBT Model

The first step is to extract R_{th} (thermal resistance), R_e, R_c and low current C_{be} and C_{bc}. Once these are known the DC curves are fit versus temperature. Finally, the S-parameters and f_t and f_{max} versus bias are fit. A number of iterations of the fitting are performed until the final model is arrived at. During the course of this thesis work, models have been extracted for the Vitesse, HRL Laboratories and Teledyne Scientific InP HBT processes. The extraction procedure is identical for each process. In the following sections the extraction process is described using data from the Teledyne Scientific process.

2.6.1   Device Burn-in

Before data is taken on the devices for model extraction purposes, it must be ensured that the device has been fully "burned in". Over the first set of temperature cycled data, the device characteristics change slightly and then reach a steady state condition. The model extraction data is then taken on the device, which is ensured to be consistent over all measurements. The effects of device burn-in are shown in figure 2.16.
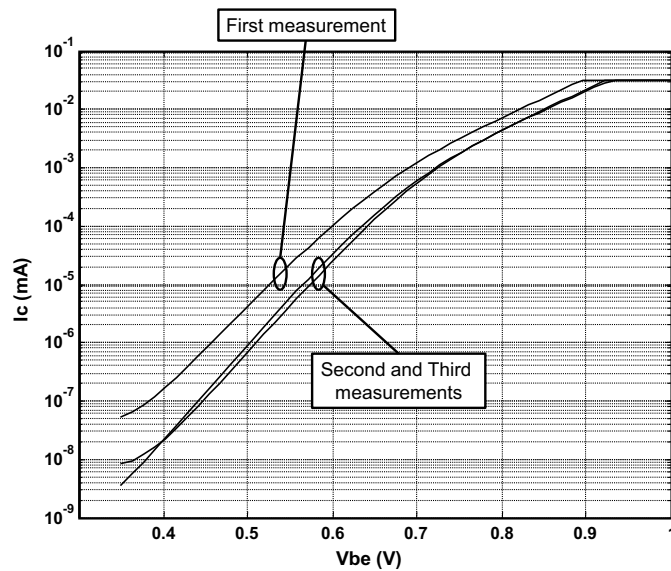
Figure 2.16: Variation in collector current due to device burn-in

Here the collector current is plotted for the same device before and after a full temperature cycle. The device then converges to have a repeatable performance once the burn-in cycling is complete.

2.6.2   Thermal Resistance (R_{th})

The thermal resistance of the HBT devices is extracted from the temperature dependence of V_{be} [27]. In figure 2.17 the variation of V_{be} versus power dissipation is plotted for three temperatures for constant emitter current. The emitter current is held constant to ensure that the variation in V_{be} is due solely to temperature changes. The power dissipation is varied by sweeping V_{ce}, but keeping emitter current constant. For this extraction technique the effect of V_{ce} on emitter current is assumed to be negligible. The relationship of V_{be} versus temperature is given in equation 2.2. The $\frac{\Delta V_{be}}{\Delta T}$ term is extracted at a single power level as illustrated in figure 2.17. R_{th} is then extracted from the slope of V_{be} at the three ambient baseplate temperatures.

$$V_{be}(T_{amb}, P_{diss}) = V_{be}(I_e) + \frac{\Delta V_{be}}{\Delta T}(T_{amb} - T_1) + \frac{\Delta V_{be}}{\Delta T}R_{th}P_{diss} \tag{2.2}$$

The results of the R_{th} extraction are shown in figure 2.18. It can be seen from this plot that the extracted value of R_{th} depends on both the ambient temperature and power dissipation of the measurement. The compact model allows only a single value of R_{th} to be specified, so this must be chosen to correspond most closely to the operating conditions of the circuit to be designed. For the current model the R_{th} value used is 1500 °/W. It has been shown [28] that R_{th} can be influenced by the metal connections to the device and the proximity of the pads.
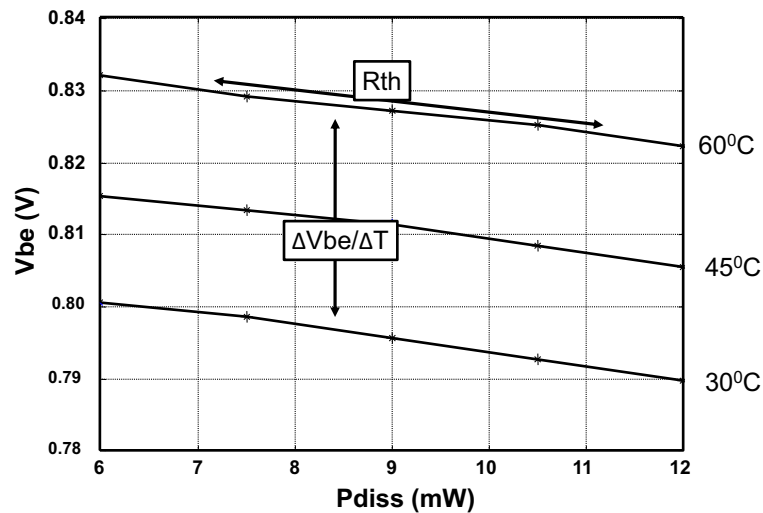
Figure 2.17: Variation of V_{be} versus power dissipation for constant emitter current

2.6.3 Emitter Resistance (R_e)

For extraction of the emitter resistance two different techniques are used. One method is based on measurement of low frequency Z_{12} [29] and the other is based on DC sweeps of $1/g_m$ versus $1/I_c$ [30] for different power levels. For the Z_{12} technique, the Z_{12} at 1GHz is plotted versus $1/I_e$ as seen in figure 2.19. The value of Z_{12} for low frequencies is real and equal to the emitter resistance plus a current dependent trans-resistance. When Z_{12} is extrapolated to the zero value of $1/I_e$, the value of R_e is found since the trans-resistance is proportional to $1/I_e$. From figure 2.19 the extracted value for this measurement is 1.5Ω. For this technique the measurement and padframe parasitics are de-embedded from the results using both an SOLT calibration of the network analyzer and open-short de-embedding to remove padframe parasitics, hence
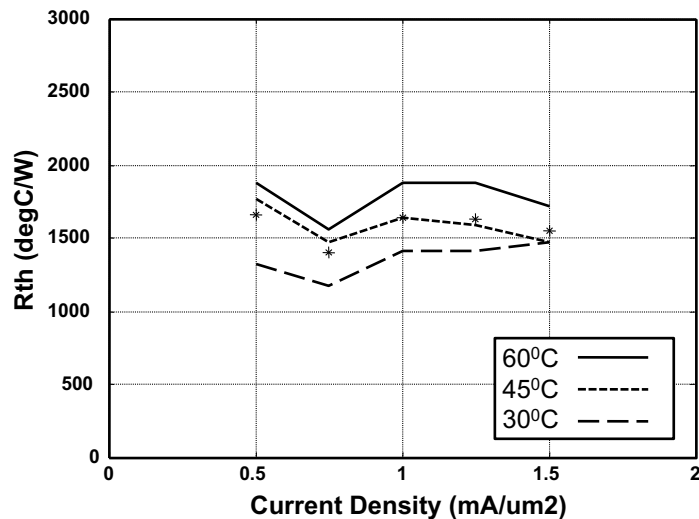
Figure 2.18: Extracted R_{th} values from different temperature curves

the calculated R_e is due to the intrinsic device only.

$$\frac{1}{g_m} = \frac{dV_{be}(T, I_c)}{dI_c} = (\frac{\delta V_{be}}{\delta I_c})|_T + (\frac{\delta V_{be}}{\delta T})|_{I_c}\frac{dT}{dI_c} \qquad (2.3)$$

$$\frac{1}{g_m} = \frac{nkT}{qI_c} + \frac{Rb + Re}{\beta} + Re + \alpha RthV_{ce} \qquad (2.4)$$

For the DC technique $1/g_m$ versus $1/I_c$ is plotted. The value of $1/g_m$ is shown

in equation 2.3, which is calculated fully in equation 2.4, where the α term represents

the change in V_{be} versus temperature at a fixed I_c. It can be seen that extrapolating

$1/g_m$ versus $1/I_c$ to $1/I_c = 0$ gives a power dissipation dependant estimate of R_e. If

these values are then plotted versus V_{ce} to a value of V_{ce}=0 the true value of R_e is

found. These extrapolations are shown in figure 2.20. A value of 1.7Ω is extracted
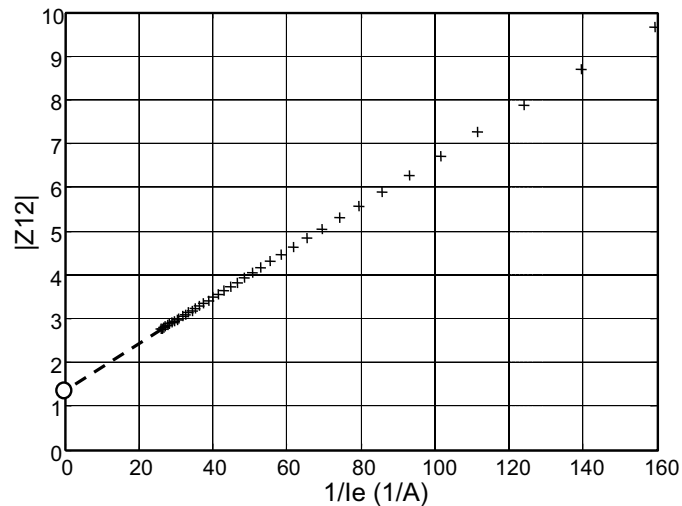
Figure 2.19: Extraction of Emitter Resistance from Z_{12} plot

for R_e, after the 0.6Ω parasitic emitter resistance is accounted for. There are some difficulties in extrapolating the emitter resistance values using this technique for these devices. This is seen from figure 2.20 where a straight line extrapolation of $1/g_m$ versus $1/I_c$ is not easy since the lines have some of curvature, which is also seen in the Gummel plots. For the extracted value of 1.7Ω , the $1/g_m$ plot is extrapolated at the high current region of the plot. For this reason the Z_{12} technique is the preferred R_e extraction technique in this work.

2.6.4 Base Resistance (R_b)

To extract a value for the total base resistance the modified circle impedance technique [31] is used. Here a polar plot of $1/(Y_{11} + Y_{12})$ is extrapolated to infinite frequency on the x-axis. The Y_{12} term is included to remove the effect of extrinsic C_{bc}
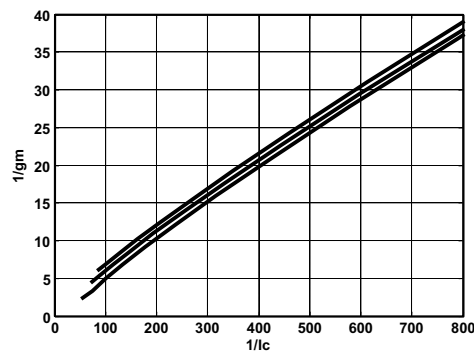
(a) Plot of $1/g_m$ versus $1/_c$ for power depen-

dant R_e extraction
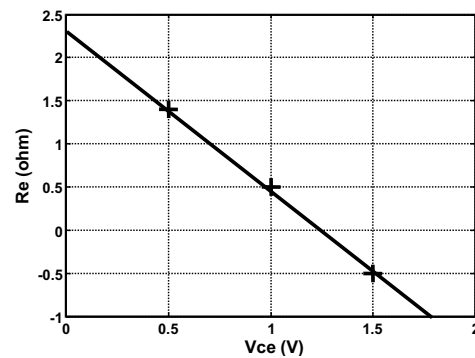
(b) Extrapolation of R_e to true value at low

power dissipation

Figure 2.20: Extraction of Emitter Resistance

from the extraction. The small signal equivalent circuit used to derive this extraction

technique is shown in figure 2.21. From this equivalent circuit the expression for

$1/(Y_{11} + Y_{12})$ can be derived as shown in equation 2.5

$$\frac{1}{Y_{11} + Y_{12}} = R_b + R_e + \frac{1}{\frac{1}{R_\pi} + j\omega(C_\pi C_\mu)} \tag{2.5}$$

From this equation the low frequency value of the polar plot is equal to the

sum of R_b, R_e and R_π, while at high frequencies R_π is shorted, and the polar plot

is just equal to the sum of R_b and R_e. For the intermediate frequency range, the

expression plots a semi-circular line along the real-imaginary plane. This is seen in

figure 2.22 for various bias points. It is seen that the value for R_b converges on the

x-axis to a single value regardless of bias point. This gives a value for the total base

resistance. Later in the fitting procedure after the f_t curves have been fit, the intrinsic

(R_{bi}) and extrinsic (R_{bx}) base resistance ratio is extracted by fitting the f_{max} curves. For final fine tuning of the R_b value, S_{11} versus frequency plots can be used to verify the base resistance extraction.
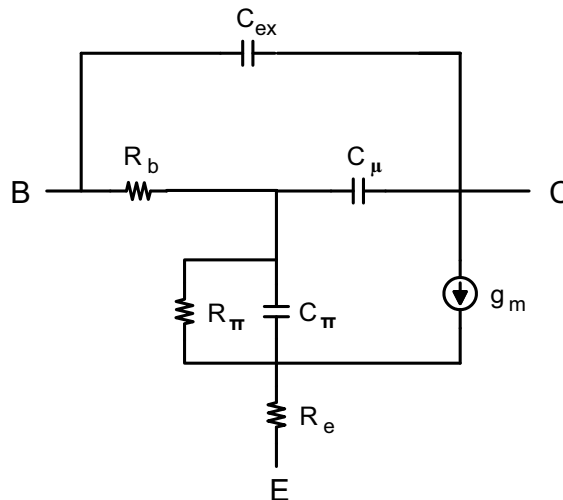
Figure 2.21: Small signal Equivalent circuit for Base Resistance extraction

2.6.5 Collector Resistance (R_c)

In this work, the forced beta method was used for the extraction of collector resistance [32]. S-parameter based extraction techniques [33] were found to give inconsistent results and so these were not used here. For collector resistance determination, the transistor output characteristics in the saturation region are utilized. The current gain, β, is determined and V_{ce} versus I_c is plotted for constant β. The slope of this plot is given by equation 2.6.
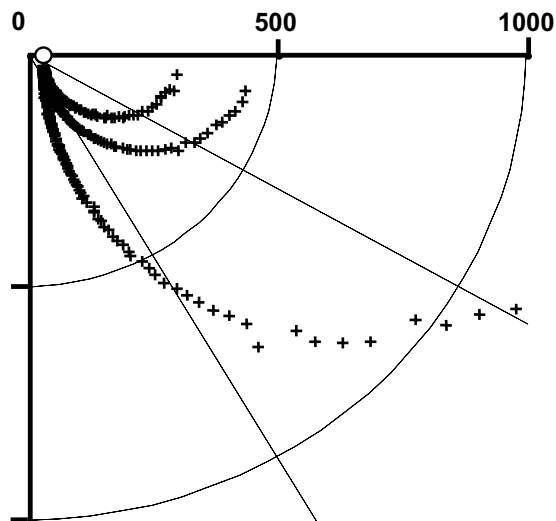
Figure 2.22: Extraction of Base Resistance using modified circle impedance method

$$m = R_c + (1 + \frac{1}{\beta})R_e \qquad (2.6)$$

R_e and β are known, so R_c is easily determined from the slope. The output characteristics and V_{ce} versus I_c plot for constant β are shown in figures 2.23(a) and 2.23(b) for a sample device. In this case, a value of 3.1Ω was extracted for R_c for the given device after the effects of parasitic DC resistances are removed. This value was extracted for a constant β value of 15. It can be seen in figure 2.23(b) that the data point at the lowest collector current is not used in the slope fitting for R_c extraction. It was found that the extraction was most accurate when applied to data in the middle of both the collector current and DC current gain ranges. Later in the fitting procedure the slope of collector current in the saturation of the DCIV curves should fit well to confirm that an accurate value of collector resistance has been determined.
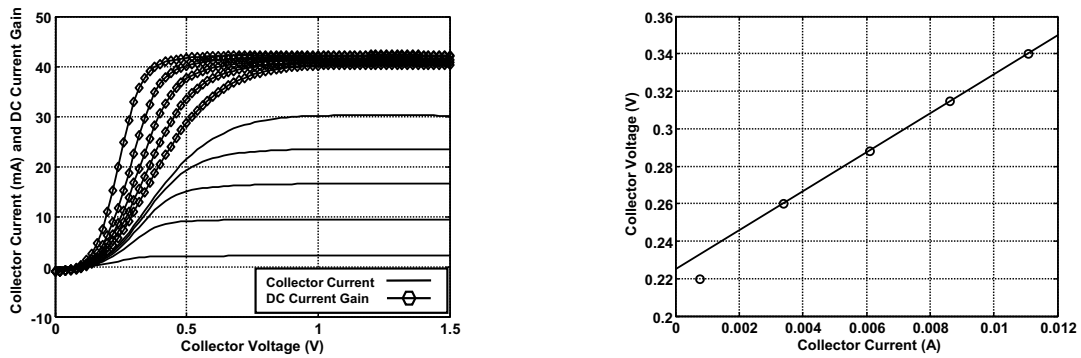
(a) Plot of both Collector Current and DC Current Gain to be used for R$_c$ extraction

(b) Extraction of R$_c$ from Slope of best fit line

Figure 2.23: Representative plots for Forced Beta method for Collector Resistance extraction

2.6.6 Base-Emitter and Base-Collector Capacitances (C$_{be}$ and C$_{bc}$)

The base-emitter and base-collector capacitances are extracted from device Y-parameters using equations 2.7 and 2.8.

$$C_{be} = \frac{1}{IM[Y_{11} + Y_{12}] * \omega} \tag{2.7}$$

$$C_{bc} = -\frac{1}{IM[Y_{12}] * \omega} \tag{2.8}$$

These measurements are made with the device in the off condition. C$_{bc}$ for higher collector currents is also measured and this is used along with Ft measurements to fit the dynamic high frequency effects present in the devices.

(a) Extraction of C_{be} (b) Extraction of C_{bc}
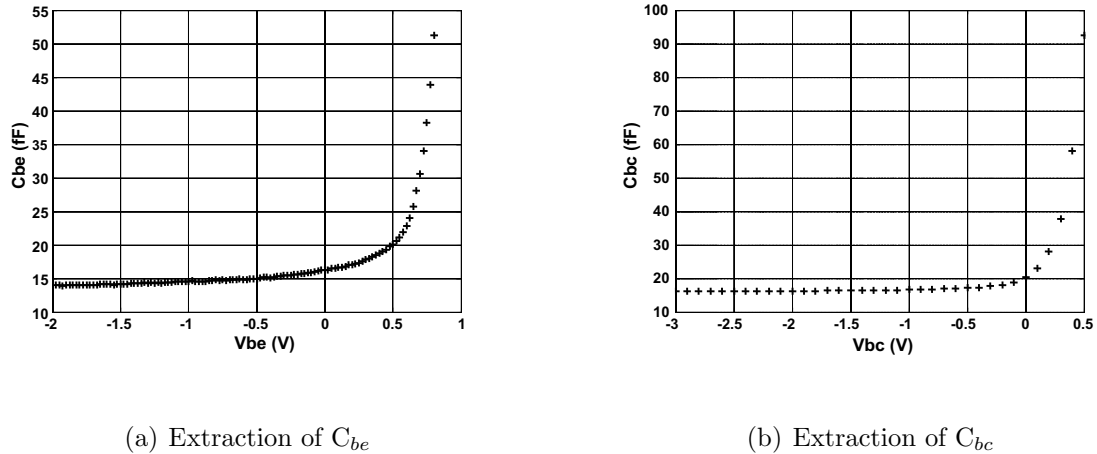
Figure 2.24: Cold capacitance measurements of C_{be} and C_{bc}

2.6.7 DC and RF Parameter Fitting

Once the previously described parameters have been extracted, the Agilent model DC and RF parameters are fitted. Forward Gummel, reverse Gummel and DCIV plots over temperature are used to extract all of the DC parameters, while S-parameter sweeps and Ft and Fmax versus bias curves are used to fit high frequency parameters.

In figure 2.25, the results of fitting a 0.5x10 um^2 emitter area device from the Teledyne InP DHBT process are presented. From 2.25(a) it is seen that the model fits well at high current levels, but at low currents there is a significant deviation between measured and modeled results. The devices exhibit a large change in ideality factor as V_{be} is increased and the model does not have the capability to accurately capture this effect. There are some parameters in the model (I_{SA} and N_A) which are used to attempt to model the effect due to the base-emitter heterojunction, but the fit at low

currents is still poor.
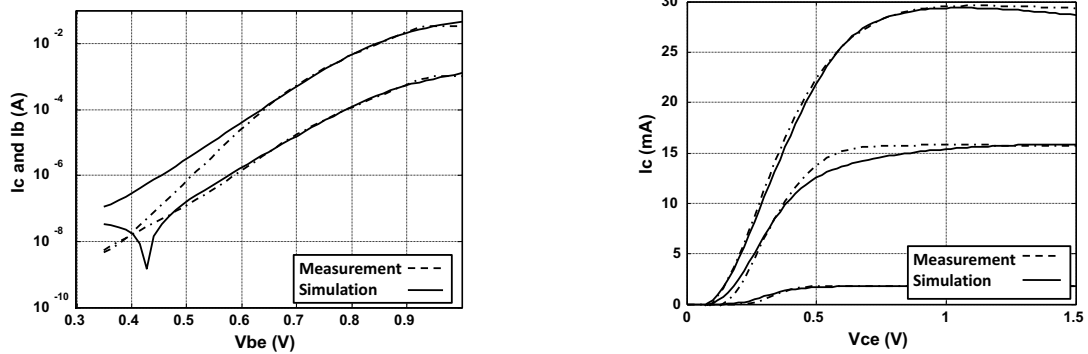
(a) Measurement versus simulation of Gummel plot

(b) Measurement versus simulation of forced I_b DCIV

Figure 2.25: DC fitting results for Agilent HBT model extracted for Teledyne InP DHBT process

The results for fitting the high frequency parameters for the same Teledyne devices are plotted in figure 2.26. Both Ft and Fmax fit well over a wide range of collector currents and voltages. The fit is optimized to fit as well as possible over the full bias range of the measurements. This is required for good simulation during large signal circuit design since the devices will experience signal swings across a large area of the DCIV plane. This is much different to the case of small signal circuit design where device performance at a number of discrete operating points is sufficient for design purposes.
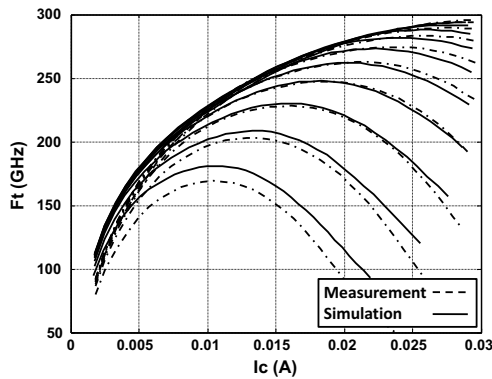
(a) Measurement versus simulation of Ft versus collector current and voltage
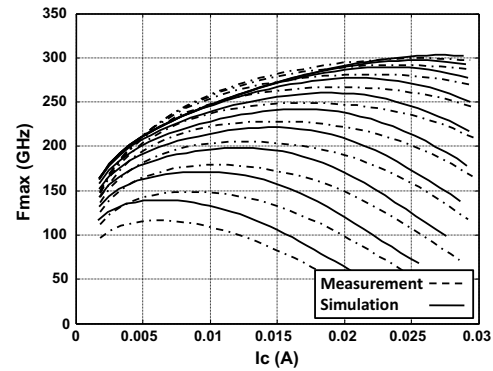
(b) Measurement versus simulation of Fmax versus collector current and voltage

Figure 2.26: RF fitting results for Agilent HBT model extracted for Teledyne InP DHBT process

2.7 Conclusion

In this chapter the measurement and modeling of InP HBT devices for millimeter-wave applications has been presented. The de-embedding of RF measurements for device modeling has been extensively investigated, focusing on the Open-Short and TRL de-embedding algorithms. Extraction techniques for various bipolar device parameters have been shown and finally the model fitting performance of the Agilent HBT model for high frequency InP HBT devices has been presented.

Portions of chapter 2 appear in the Proceedings of the 70th ARFTG Measurement Symposium, 2007. Contributions from the co-author P. M. Asbeck are greatly appreciated. The dissertation author was the primary investigator and author of this paper.

Chapter 3

Design of Millimeter-wave Power Cells

In this chapter many of the aspects involved in the design of millimeter-wave power cells are discussed. Some of the conclusions are specific to InP HBT based amplifier design, but others are more general and can be applied to other device technologies when designing high frequency power amplifiers. Device sizing and operating current density are first discussed. This is followed by choices for amplifier configuration and a discussion of thermal ballasting options. Later in the chapter various effects due to parasitic elements in large power cell arrays at millimeter-wave frequencies, as well as simulation techniques for parasitic estimation, are discussed.

3.1 Device sizing and operating current density

The first consideration in the design of the millimeter-wave amplifier is the correct choice for both the device size and operating current density. The Ft and Fmax for increasing emitter finger length are plotted in figure 3.1. These are measurement results from 3 different device sizes with emitter areas of 0.5x3um^2, 0.5x5um^2 and 0.5x10um^2. Here there are three sets of curves corresponding to different current densities of 1mA/um^2, 2mA/um^2 and 4mA/um^2, with both Ft and Fmax increasing as current density is increased.
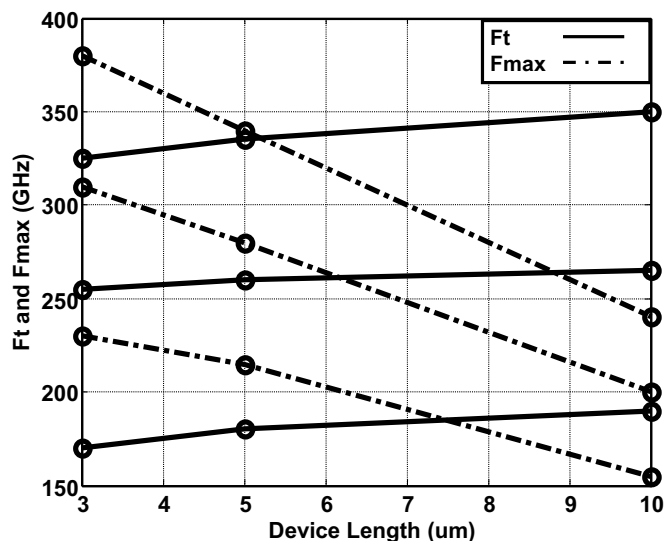
Figure 3.1: Variation of Ft and Fmax with finger length

From this figure it is clear that the device Ft is not degraded as device length is scaled, whereas the Fmax is reduced by 30%. The reason for this reduction in Fmax is due to the increase of the base interconnect resistance as the device length

is increased. The small signal model used to explain this effect is given in figure 3.2. In this model both the base resistance and collector to base capacitance are divided into intrinsic and extrinsic portions. Using this model the equation for Fmax can be expressed as in equation 3.1 [34].

$$Fmax = \sqrt{\frac{Ft}{8\pi[(R_{Bx})(C_{BCx} + C_{BCi}) + R_{Bi}(C_{BCi})]}} \qquad (3.1)$$

This equation illustrates that the partition between intrinsic and extrinsic R_B has a large effect on the Fmax of the device, with a larger portion of intrinsic base resistance leading to higher Fmax. As the device length increases, the total base resistance is reduced, and the collector-base capacitance is increased, and results in the total $R_B C_{BC}$ product remaining nearly constant. However, increasing device length leads to an increased portion of the total base resistance being contributed by the base metal interconnect. This results in a less favorable partition between intrinsic and extrinsic base resistance, and hence lower Fmax for longer finger length.

For the implementation of the power amplifier in this work the device with emitter area of 0.5x10um^2 was chosen. This device size is a tradeoff between power density and amplifier gain. For longer finger lengths more power could be obtained from the amplifier, but at the cost of reduced gain. For this device size the Fmax of the device is just over 3 times larger than the desired operating frequency of the amplifier.

The next consideration for the design of the power amplifier cell is the current density of the devices. In this design a class A mode of operation for the amplifier is
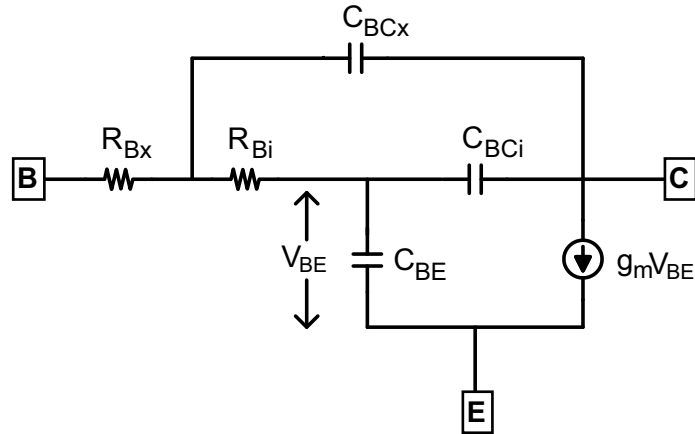
Figure 3.2: Small signal model for Fmax calculation

chosen, such that in the ideal case the device load-line for the common base device is as shown in figure 3.3(a). In this case the maximum current and voltage swings are limited by the device current handling and breakdown properties, which for these devices are $6mA/um^2$ and 6V respectively. The variation of device gain (Fmax) is plotted in figure 3.3(b). From these two plots the device operating current density of $3mA/um^2$ is chosen. At this current density the Fmax is over 250GHz and this allows the current to swing up and down along the load-line without exceeding the maximum device operating current.
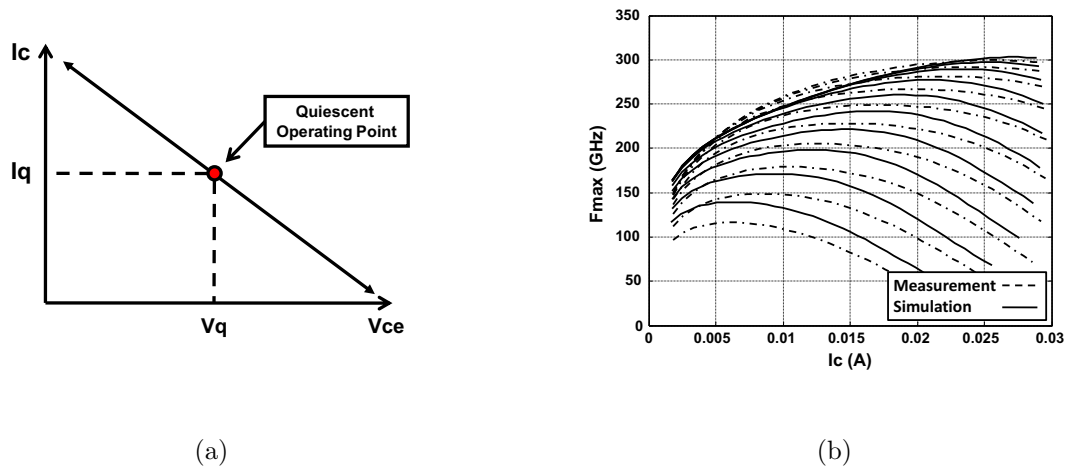
Figure 3.3: (a) Loadline swing for class A operation with quiescent operating point shown (b) Variation of Fmax with collector current and voltage

3.2 Choice of Amplifier Configuration: Common Emitter, Common Base and Cascode

When designing amplifiers using a bipolar process the three configurations available are: common emitter, common base and cascode topologies. The three topologies are shown schematically in figure 3.4. In the common-emitter amplifier the emitter terminal is grounded and in the common-base topology the base terminal is grounded. The cascode topology is then a cascade of the common-emitter and common-base topologies. The choice of topology specific to the case of millimeter-wave PA design using InP HBT devices will be investigated in this section while considering the tradeoffs between gain, stability, ease of match and power consumption. For this comparison single finger devices with emitter area of 0.5x10 um^2 biased at 3 mA/um^2 are used as a representative case.
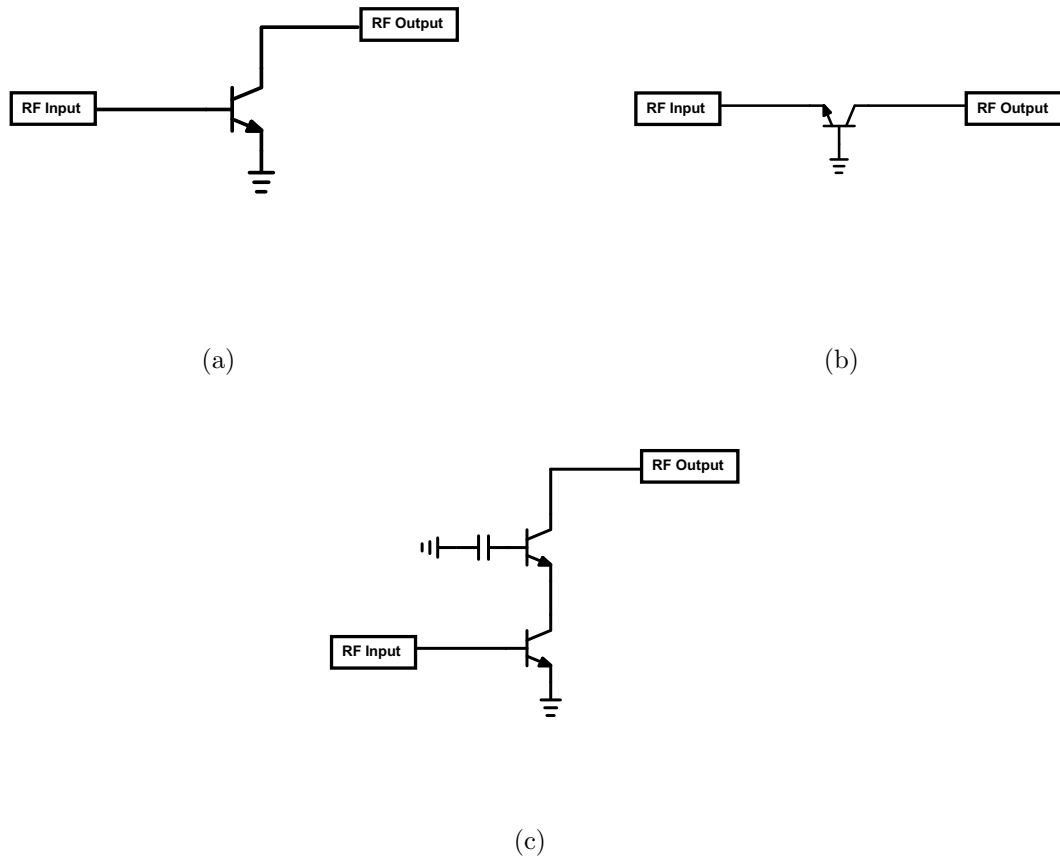
Figure 3.4: Common emitter (a), common base (b) and cascode (c) amplifier topologies

In figure 3.5 the gain performance of the different amplifier configurations is plotted. For the common-emitter and common-base amplifiers the V_{CE} across the devices is 2.5V and for the cascode amplifier the voltage across both devices is 4V, with 1.3V across the common-emitter device and 2.7V across the common-base device. For the common-base device in both the cascode and common-base amplifiers the AC ground at the base terminal is provided though an ideal 200fF capacitor. For these simulations no interconnect inductance is included. When plotting the small
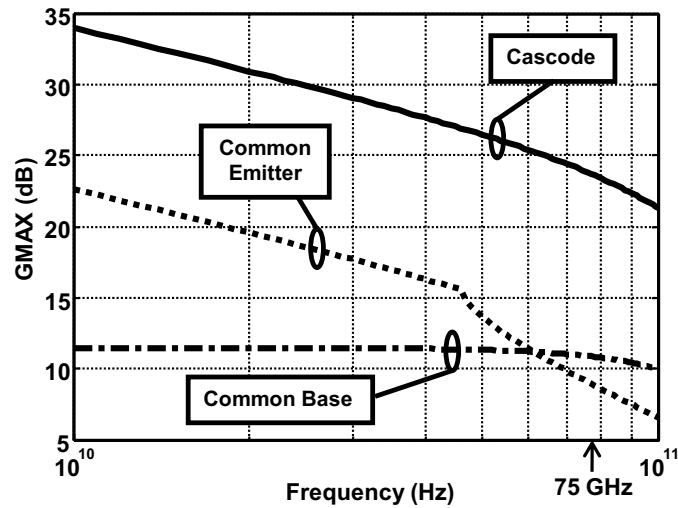
Figure 3.5: Comparison of Maximum Gain for different amplifier configurations

signal gain of an amplifier the value of gain used depends on whether the amplifier is unconditionally stable or not. If the amplifier is unconditionally stable, then the Maximum Available Gain (MAG) is plotted. MAG is the maximum gain achievable from the amplifier under conjugate matching conditions. In the case where the amplifier is conditionally stable, the Maximum Stable Gain (MSG) is plotted. MSG is the maximum gain achievable from the amplifier under the matching conditions, which keep the amplifier in a stable state. The cascode cell has the highest gain of all three configurations across the entire frequency band. When choosing between common-emitter and common-base stages, it is seen that the common-emitter has higher gain at low frequencies, but at millimeter-wave frequencies the gain of the common-base stage exceeds that of the common-emitter.

The stability measure for each configuration is plotted in figure 3.6. The cas-

code and common-base topologies have poor stability performance up to millimeter-wave frequencies, whereas the common-emitter topology is more stable at higher frequencies. When using the cascode or common-base topologies in millimeter-wave amplifiers, stabilization must be provided both in-band and at low frequencies, but, with the common-emitter topology, only lower frequency, out of band stabilization techniques are required. At millimeter-wave frequencies the AC ground connection at the base of the common-base devices dominates the stability performance of both the cascode and common-base topologies. This will be discussed in more detail in section 3.4. The common-emitter amplifier does not have this AC ground connection and so is inherently more stable at millimeter-wave frequencies.
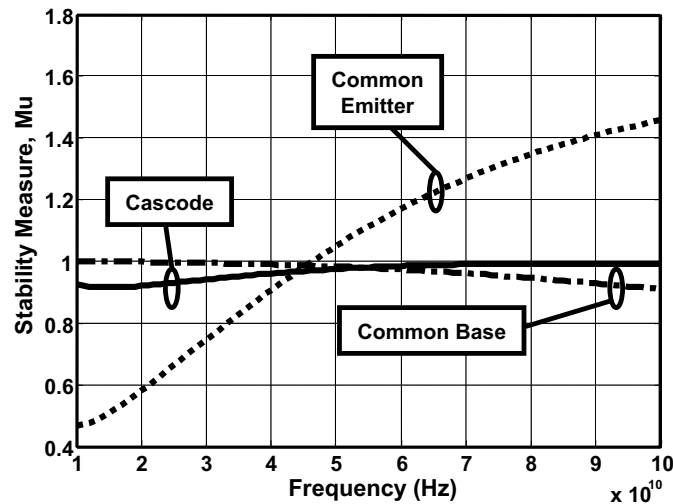
Figure 3.6: Comparison of Stability Measure for different amplifier configurations

The next aspect to be considered is the ease of matching to the power cell at millimeter-wave frequencies. In figures 3.7(a) and 3.7(b) the input and output

impedances presented by the different topologies are plotted for a frequency point at 75 GHz (using a Smith chart with a reference impedance of 50Ω). The common-base topology is seen to have a slightly lower input impedance than the other topologies. The real parts of the input impedance are 16.95Ω 16.05Ω and 11.85Ω respectively for the common-emitter, cascode and common-base topologies. This difference is due to the fact that the cascode and common-emitter use the base as input terminal, whereas the common-base topology has an emitter input terminal. The real part of the input impedance at the base terminal is dominated by R_B, the base resistance. The real part of the input impedance at the emitter terminal is $1/g_m$ of the device, which is much lower than R_B.

In the case of the output match it is seen that the common-emitter has a higher output resistance than the other topologies. At high frequencies the low impedance at the base terminal reduces the output resistance of both the common-base and cascode amplifiers. This impedance is lower due to the extrinsic C_{BC} capacitance, which shunts the device to ground with only the extrinsic base resistance in series to ground.

The final considerations when choosing an amplifier topology are power dissipation and voltage swing capabilities. In the case of power dissipation, both the common-emitter and common-base topologies dissipate similar amounts of DC power for the same class of operation. In the case of the cascode cell, 2 devices are stacked and hence a higher supply voltage is required to ensure both devices operate in the high gain linear region. All topologies have the same collector current and so the

(a) S11 for different topologies   (b) S22 for different topologies
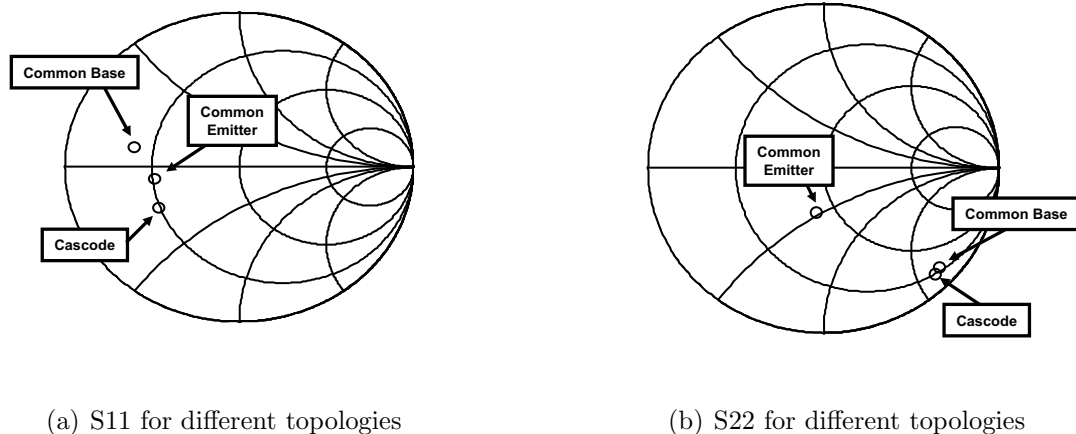
Figure 3.7: Input and output impedances presented by the devices in the three different topologies

cascode amplifier will have the highest DC power consumption.

For voltage swing the common-emitter topology is limited by the BVceo, whereas for the cascode and common-base topologies the swing is limited by the BVcbo, which is a higher voltage value. This is due to the low impedance presented at the base of the common-base devices in the CB and cascode topologies [35]. In the case of InP DHBT's with ft/fmax values of 300 GHz the BVceo is about 4.5 volts and the BVcbo is close to 6V. The common emitter topology can be designed to operate with voltage swings above BVceo, but below BVcbo. This can be done by careful design of the bias and matching network at the base terminal. If this impedance can be made low then the device can support voltage swings above BVceo.

For this work, the cascode topology is chosen for the amplifier design due to its high gain and voltage swing characteristics. The major issue with implementing the cascode topology for millimeter-wave power amplifiers is ensuring stability of the

high gain transistors over the full bandwidth. In the next sections techniques for stabilizing the power cells will be discussed.

3.3   Ballasting for Cascode Power Cells

When designing multi-finger power cells in a bipolar process, ballasting of the individual fingers (or groups of fingers) is necessary to ensure thermal stability of the device. The two choices available to a designer for ballasting are base (R_B) or emitter (R_E) ballasting as illustrated in figure 3.8(a). These resistors reduce the gain of the electro-thermal feedback loop of the device (figure 3.8(b)) and so prevent any single finger from becoming a current hog and leading to thermal runaway in the array. Increasing the value of the ballast resistors has the effect of decreasing the $\frac{dI}{dT}$ term in the electro-thermal loop, and hence reducing the loop gain. This can be seen as follows: (1) device temperature increases leading to an increase in device current, (2) increased device current leads to increased voltage drop across external ballast resistors and hence reduced intrinsic device V_{BE}, (3) reduced device V_{BE} in turn reduces device current. From the feedback loop the condition for thermal stability is derived to be given by equation 3.2.

$$(\frac{dT}{dI})(\frac{\delta I}{\delta T}) \leq 1 \tag{3.2}$$

Expanding equation (3.2) leads to equation (3.3) [36, 37]. This allows for the minimum value of ballast resistance required for thermal stability to be found given
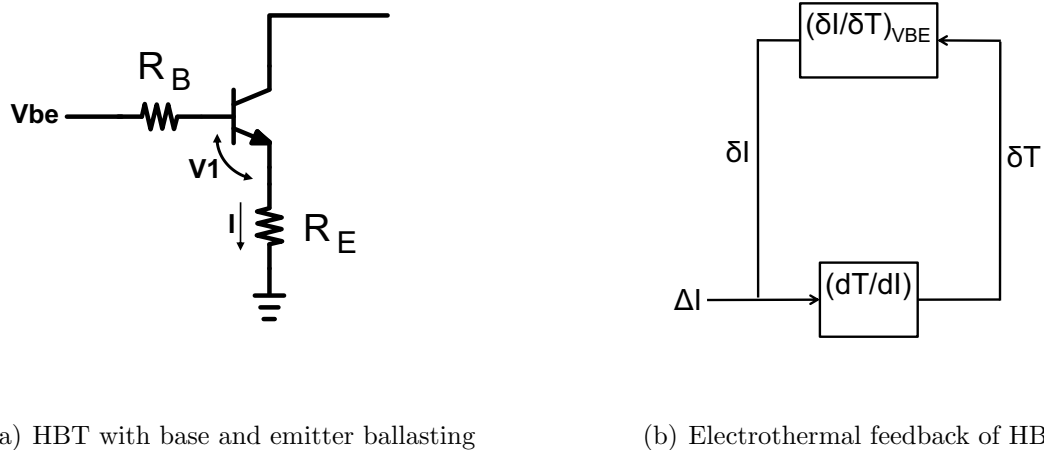
(a) HBT with base and emitter ballasting

(b) Electrothermal feedback of HBT

Figure 3.8: Figures for calculation of HBT ballast resistance

the operating voltage and current of the device.

$$\frac{R_E}{\alpha} + \frac{R_B}{\beta} \geq R_{TH}.V_C.\frac{\delta\,V_{BE}}{\delta\,T}\bigg|_{I_C} - \frac{nkT}{qI_C} \qquad (3.3)$$

In the case of the cascode power cell the device to which this equation applies is the common emitter device, so V_C is the voltage across this device only. It is clear that the correct choice of either base or emitter ballasting resistor values will lead to identical thermal performance from this first order analysis. When the decrease of current gain, β, with temperature in a HBT is considered, it can be shown that base ballasting is slightly superior to emitter ballasting for HBT devices [37].

The small-signal performance of the cascode power cell, however, is affected by the choice of either base or emitter ballasting in different ways. The small signal circuit which will be used for the analysis of ballasting on the performance of the cascode device is shown in figure 3.10. Here just the common emitter stage of the
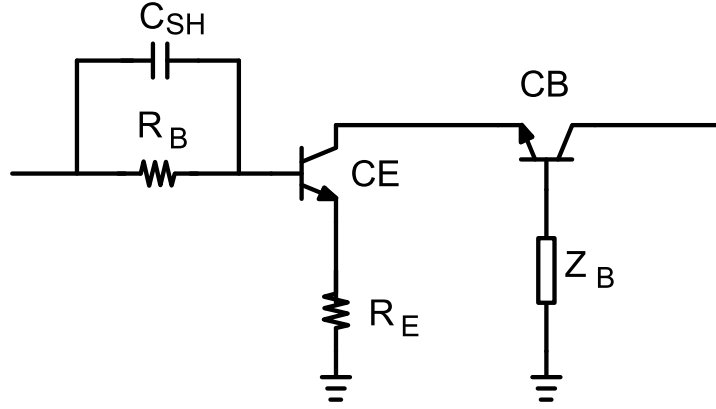
Figure 3.9: Cascode cell schematic with base and emitter ballasting

cascode device is considered, since the ballasting is applied at this stage. The Z-parameters of this circuit are given in (3.4-3.7).

$$Z_{11} \approx R_B + R_E + \frac{1}{g_m} - j\frac{\omega C_\pi}{g_m^2} \tag{3.4}$$

$$Z_{12} \approx R_E + \frac{1}{g_m} - j\frac{\omega C_\pi}{g_m^2} \tag{3.5}$$

$$Z_{21} \approx R_E + \frac{1}{g_m}\left(1 + \frac{C_\pi}{C_\mu}\right) + j\frac{1}{\omega C_\mu} \tag{3.6}$$

$$Z_{22} \approx R_E + \frac{1}{g_m}\left(1 + \frac{C_\pi}{C_\mu}\right) - j\frac{\omega C_\pi}{g_m^2}\left(1 + \frac{C_\pi}{C_\mu}\right) \tag{3.7}$$

Using these Z-parameters the Rollett stability factor, K, can be determined as shown in (3.8) and (3.9). From (3.9) it is seen that an increase in R_B will increase the stability factor much more than an increase in R_E, due to the fact that R_E is in both
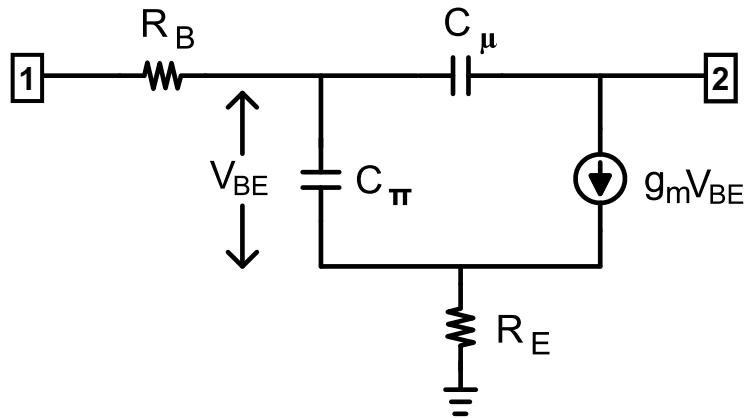
Figure 3.10: Small signal model for stability analysis

the numerator and denominator of the expression. Also from (3.3) we know that the value of R_B required is β times larger than R_E to achieve the same thermal stability. Hence, we can say that base ballast provides a more electrically stable cascode power cell.

$$K = \frac{2real[Z_{11}]real[Z_{22}] - real[Z_{12}Z_{21}]}{|Z_{12}Z_{21}|} \qquad (3.8)$$

$$K = \frac{\omega C_\mu}{R_E + \frac{1}{g_m}}\left[\left(2R_B + R_E + \frac{1}{g_m}\right)\right. \qquad (3.9)$$
$$\left.\left(R_E + \frac{1}{g_m}\left(1 + \frac{C_\pi}{C_\mu}\right)\right)\right]$$

The base ballast also reduces the gain of the cascode power cell more than emitter ballast does, which is not desired. Bypass capacitors, C_{SH}, can be imple-

mented to shunt the base ballast resistors at millimeter-wave frequencies and thus restore the device gain at these frequencies. The stability measure, μ, and maximum gain, Gmax, of a single finger cascode cell (shown in figure 3.9) are simulated using a InP HBT device model based on the Teledyne process [38]. The device dimensions considered are single emitter finger devices with emitter dimensions of 0.5x10 um^2. For the simulation the bias current through each finger was 15mA (corresponding to a current density of 3mA/um^2) with a bias voltage across the cell of 4V. For this device dimension R$_{TH}$ and α_{TH} were extracted to be 1550 °C/W and 0.4 mA/°C respectively. The results are shown in figures 3.11 and 3.12 for the three cases of emitter ballast, base ballast and base ballast with shunt capacitor. The values for the ballast resistors are R$_B$=400Ω , R$_E$=5Ω and C$_{SH}$=50fF.

In figure 3.11 it is shown that the stability of the base ballasted circuit is superior to the emitter ballasted case. With the addition of the shunt capacitor the stability performance of the base ballasted case is degraded, but is still better than the emitter ballasted circuit. In figure 3.12 the higher gain of the emitter ballasted cascode cell is shown. It is also clear that most of the gain is restored to the common-base amplifier at millimeter-wave frequencies with the addition of the shunt capacitor. It has been shown that the choice of base ballast with shunt capacitor has the same thermal characteristics and high frequency gain characteristics as emitter ballast, but with improved stability in the low frequency region. For this reason base ballasting has been implemented for the power amplifier designs in this work.
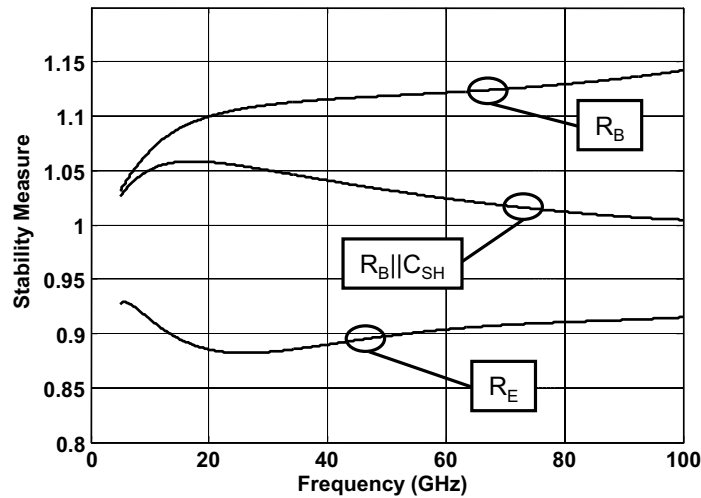
Figure 3.11: Stability measure (μ) versus frequency for different ballasting configurations

3.4 AC Ground Impedance at Base of Common Base Stage of Cascode Cell

An important aspect in the design of cascode amplifiers is a well designed RF ground connection at the base terminal of the common-base stage. In this section the effect of this impedance is studied in more detail. The circuit of figure 3.9 is used for the study in this section. The impedance, Z_B, presented at the base of the CB stage of the cascode cell is varied as shown in figure 3.13. The variation of the impedance follows a constant resistance circle (with a resistance of 1Ω), from the capacitive to inductive regions of the Smith chart. This contour models increasing series inductance present at the base of the CB device, an important parasitic at millimeter-wave frequencies. With all other parameters held constant, the effect of
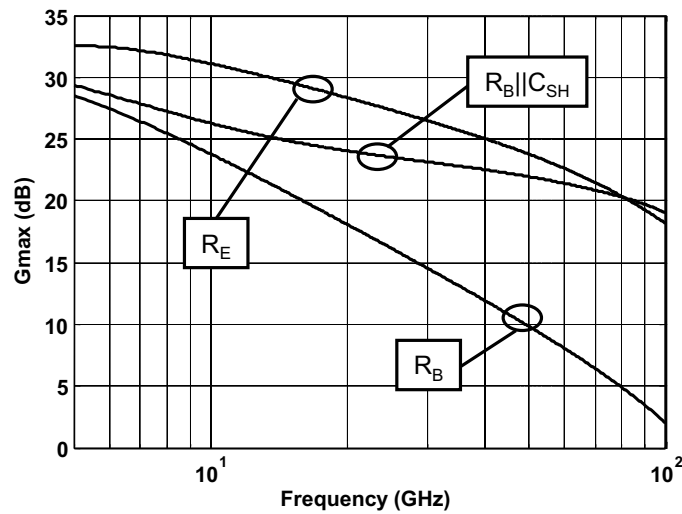
Figure 3.12: Maximum gain versus frequency for different ballasting configurations

the impedance change on both maximum gain and stability measure is plotted in figure 3.14. These stability and gain curves are plotted at a frequency of 75GHz, but the trends apply at all frequencies.

Firstly, looking at the stability factor it is seen to decrease as the impedance is swept along the constant resistance circle. Secondly, the maximum gain of the cascode cell increases until the transition from the MAG (Maximum Available Gain) to MSG (Maximum Stable Gain) region occurs at the point where the stability measure drops below unity. After this point the gain begins to decrease monotonically. At higher frequencies the transition from MAG to MSG regions will occur for lower inductance values due to the increased rotation around the Smith chart from capacitive to inductive regions for a given inductance value. As the frequency of millimeter-wave amplifiers scales higher, designing stable common-base and cascode amplifiers
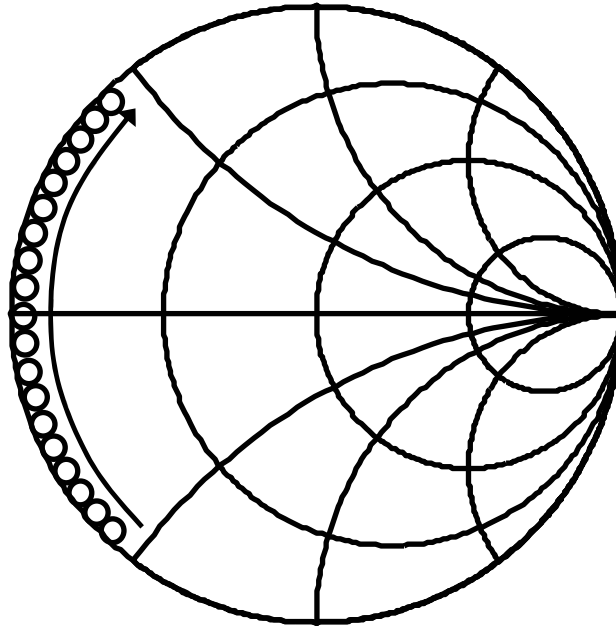
Figure 3.13: Variation of Impedance Presented at base of CB stage of cascode cell

becomes more difficult and accurate modeling of the AC ground connection becomes

one of the most important aspects of the design. For this reason many of the highest

frequency amplifiers are designed using cascaded common-emitter or common-source

designs for their improved high frequency stability properties [39, 40]. The effect of

the base impedance change on S11 and S22 of the device is plotted in figure 3.15.

As expected, there is little effect on S11, but there is a large variation in S22, which

moves outside the Smith chart to the unstable region.

From the previous discussion the strong effect of parasitic inductance at the

base of the CB stage is evident on the gain, stability and matching properties of the
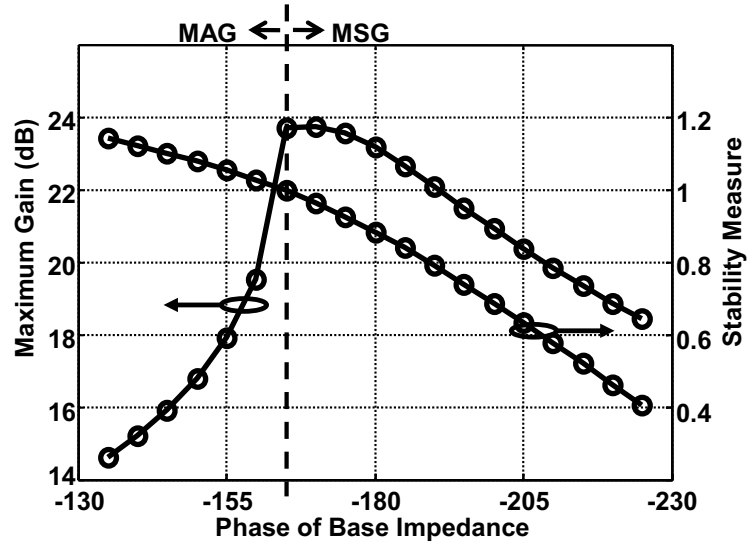
Figure 3.14: Maximum Gain (Gmax) and stability measure (μ) versus impedance variation at base of CB stage of cascode cell

cascode cell. In the design of millimeter-wave power cells, inductance is introduced at the base of the CB stage due to the finite length of interconnect required to connect each finger in the array to the AC grounding capacitor. The inductance associated with these interconnects must be accurately modeled across multi-finger arrays to ensure amplifier stability. This topic will be discussed in the next section.

3.5   Powercell Design, Simulation and Measurement

The power cell core of the power amplifier designs in this work is a base ballasted 12 finger cascode layout. This design is shown schematically in figure 3.16. The individual finger sizes are 0.5x10um^2 (emitter area). An important design issue is thermal stability. The fingers are spaced 16um apart to prevent excessive increase in thermal resistance [28] and the resulting self-heating and associated performance
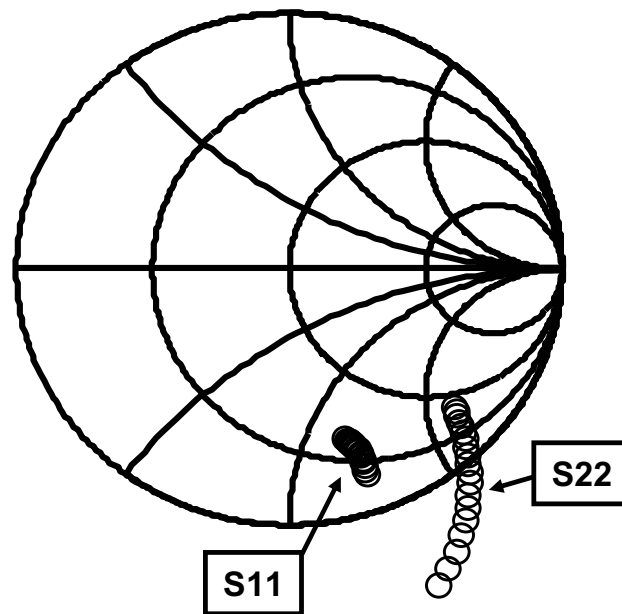
Figure 3.15: S11 and S22 at 75 GHz versus impedance variation at base of CB stage of cascode cell

degradation. Base ballasting is implemented at the common emitter fingers to prevent thermal runaway in the fingers. A shunt capacitor is placed across each ballast resistor to boost the gain at high frequencies as discussed in the section 3.3. The values used for these components are 350Ω and 40fF respectively.

The importance of accurately determining the layout parasitics of the power cell was seen in section 3.4. It was shown that the impedance presented at the base of the CB stage has a strong affect on the gain, stability and matching of the cascode cell. In order to calculate these interconnect parasitics a full method-of-moments simulation of the entire structure is run using IE3D from Zeland Software [41], with
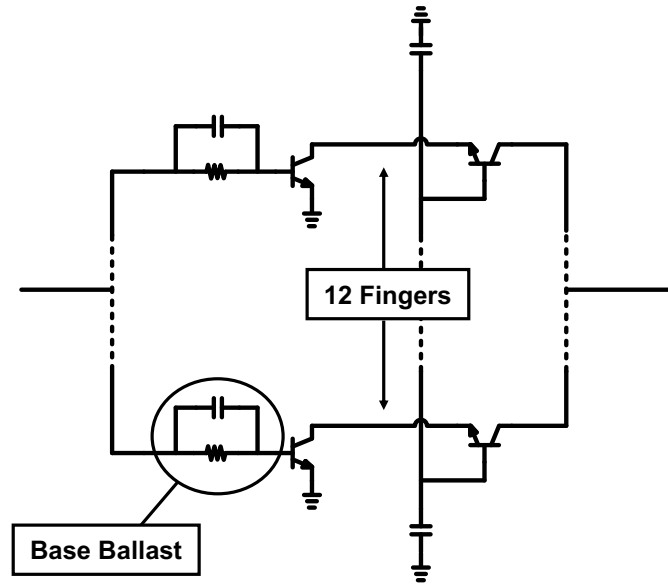
Figure 3.16: Schematic view of 12 finger millimeter-wave power cell

local ports to allow connections to the individual device fingers [42, 43, 44]. The full, simulated structure is shown in figure 3.18. The amplifiers are designed using an inverted microstrip transmission line environment, as shown in figure 3.17. This allows for a ground plane to be used over the devices with no cutouts, a layout scheme which reduces ground inductances. For the image in figure 3.18 this upper ground plane layer is removed to facilitate viewing of the interconnect structure below. The capacitor providing an RF ground at the base of the common base devices is distributed across the array. This is to reduce and equalize the inductance to ground seen by all fingers, and thus improve the stability of the amplifier.

The results of this simulation are shown in figure 3.19. Here the inductance to ground at the base of the CB stage is plotted for each finger in the 12 finger array. The
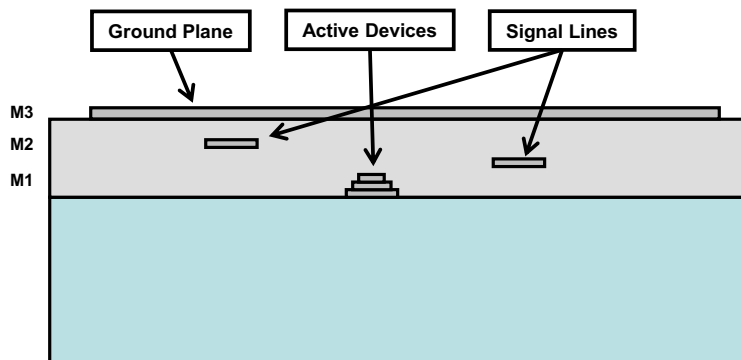
Figure 3.17: Cross section of inverted microstrip transmission line topology

difference between 2 and 3 ground connections is as expected with the inductance for the center fingers 4.5 pH higher than in the 2 connection case. The inductance varies by 1.25 pH across the array in the 3 connection case, so the extra area requirement of distributing the grounding capacitance further will not lead to much improvement in circuit performance. Using this RF ground connection ensures that stability and optimum power transfer can be achieved from each device in the array. The design of the distributed capacitance across the array is both frequency and device dependent. The design should be performed for a wide range of frequencies above the design band to ensure the impedance presented to the individual devices does not lead to unstable operating conditions.

Measurements of power cell breakouts were performed to investigate the accuracy of the interconnect simulation. The measurement setup is shown in figure 3.20. Here the RF signals are applied through DC-110 GHz bias tees. The bias current is controlled by a current source at the base of the common-emitter device provided
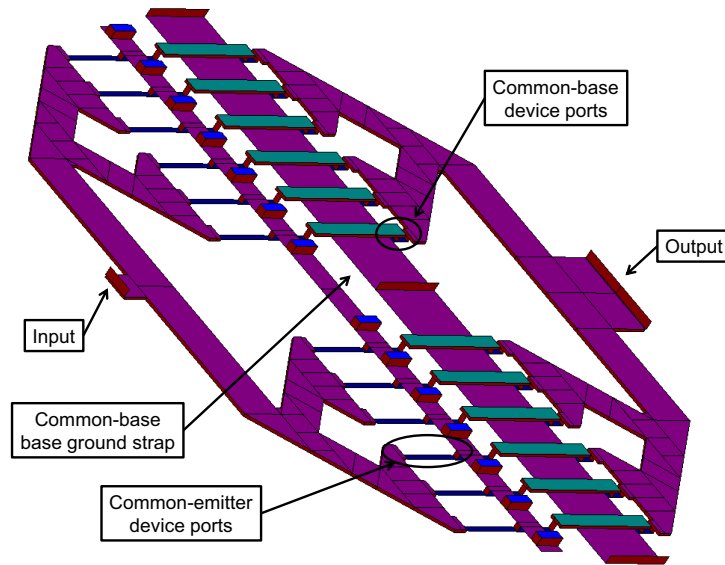
Figure 3.18: EM simulation schematic view of millimeter-wave power cell
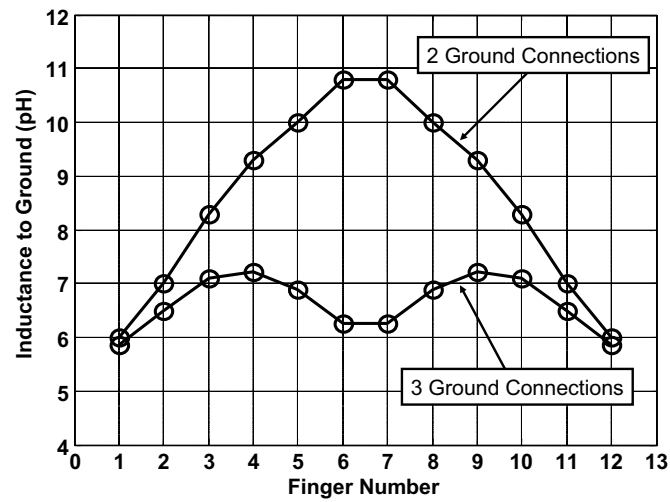
Figure 3.19: Variation of Inductance to ground at base of CB stage across array
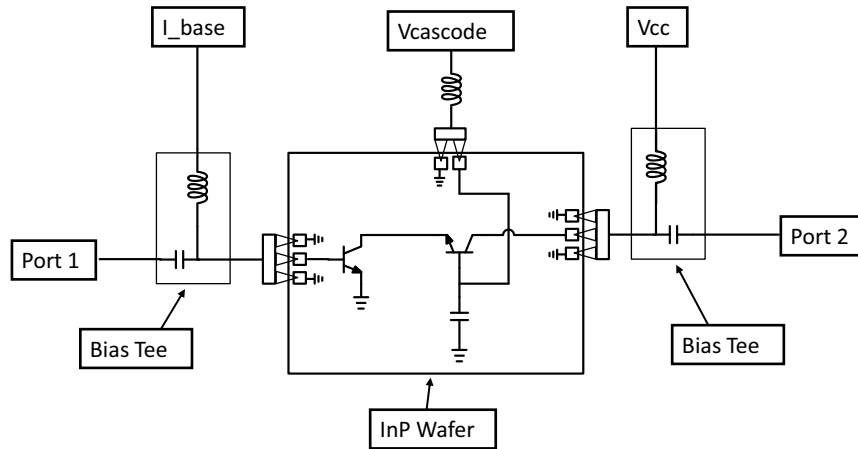
Figure 3.20: Measurement setup for cascode power cell test
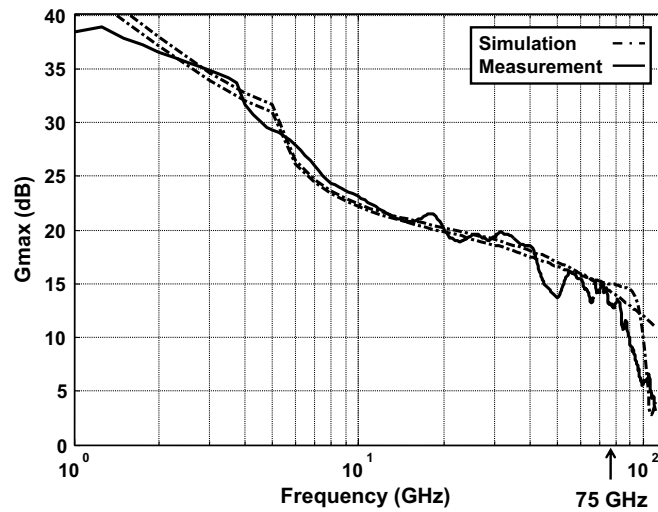
Figure 3.21: Simulated and measured Gmax of 12 finger cascode power cell
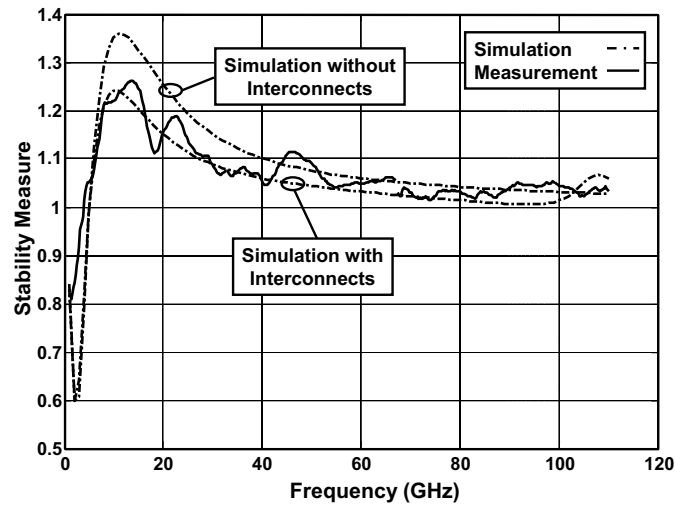
Figure 3.22: Simulated and measured stability measure of 12 finger cascode power cell

off chip, and the cascode and collector voltages applied are 2.1V and 4V respectively. The following comparisons are made for a collector current of 95mA. It is seen from figures 3.21 and 3.22 that the stability and gain of the power cell are well predicted by the simulation. Traces for both the ideal power cell and with the parasitics are shown. It can be seen that the gain is very similar for each case. This is a result of opposing effects due to the interconnect parasitics. Firstly, emitter degeneration inductance at the emitter of the CE stage will have the effect of reducing the gain of the cascode cell. Counteracting this is the increase in gain shown in section 3.4 due to inductance to ground at the base of the CB stage. Using the accurate MoM simulation of the interconnect structure, the gain of the power cell can be optimized while still maintaining stable operation of the amplifier. It is seen in figure 3.22 that the power cell is less stable when interconnect parasitics are accounted for in the sim-

ulation, which confirms that gain boosting would have occurred if not for the presence of the emitter degeneration inductance.

3.6   Conclusion

In this chapter, the design, simulation and measurement of millimeter-wave cascode power cells was presented. Firstly, the choice of amplifier topology was discussed. This was followed by ballast network design for cascode amplifiers operating at millimeter-wave. A study of the effect of the variation of impedance at the base of the CB device in cascode amplifiers was presented along with simulation results demonstrating an optimum design of this impedance for millimeter-wave. Finally, the design and measurement of a 12 finger millimeter-wave cascode power cell was presented utilizing the design techniques presented earlier in the chapter.

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Chapter 4

Power Amplifier and Power

Combiner Design

This chapter covers various components of millimeter-wave power amplifier design. The topology for a compact single-ended 20dBm millimeter-wave power-amplifier, implemented using the power-cell described in the previous chapter, is presented. The design aspects involved in implementing this design are then discussed. Firstly, transmission line choices are discussed with a comparison of thin film microstrip and co-planar waveguide topologies. Secondly, the design of compact single stage matching networks is covered. This is followed by single stage amplifier design, simulation and measurement. Finally, an on-chip radial power combining technique is presented, along with a power amplifier utilizing this power combining technique.
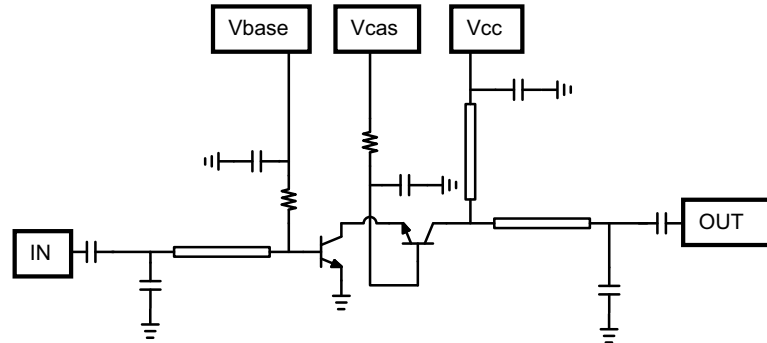
Figure 4.1: Simplified schematic overview of millimeter-wave power amplifier

4.1 Millimeter-wave Power Amplifier Topology

The power amplifier topology implemented in this work is shown in figure 4.1. The amplifier core is the 12 finger cascode power cell described in the previous chapter. Compact single-stage matching networks are implemented for both input and output matching. The collector bias voltage is supplied through a capacitively shorted quarter-wave transmission line, with the base bias voltages of both the common-emitter and common-base stages supplied through 350Ω and 35Ω resistors respectively. In the following sub-sections detailed descriptions of amplifier design aspects are presented.

4.1.1   Transmission Line Choices - Thin Film Microstrip Versus Co-Planar Waveguide

The technology for the implementation of the power amplifiers in this work is the InP DHBT from Teledyne Scientific [38]. The process includes a 3 metal back-end but lacks the capability for through wafer vias, so all ground return current for any transmission line implementation must flow through a top of wafer metal. The transmission line choices to be considered are thin film microstrip and finite-ground co-planar waveguide, which are illustrated in figure 4.2. Here the wafer substrate is Indium Phosphide (InP) with a dielectric layer of benzocyclobutene (BCB) on top. The metal layers M1, M2 and M3 are embedded in the BCB dielectric. Gold metallization is used for all three metal layers, all three metal layers are 1um thick, and the vertical spacing between layers is also 1um. The InP substrate has a dielectric constant of 13.5 and the BCB has a dielectric constant of 2.7.

The microstrip transmission line topology has a signal conductor above a ground plane. The characteristic impedance of this type of transmission line is defined by the ratio of signal line width to signal-to-ground spacing. To maintain a constant characteristic impedance as the signal-to-ground spacing is reduced, the signal line width must be reduced. This reduction in signal line width leads to increased transmission losses due to increased resistance per unit length of the signal conductor. In the case of thin-film microstrip, the signal line width must be significantly reduced to maintain reasonable characteristic impedance levels required for matching network
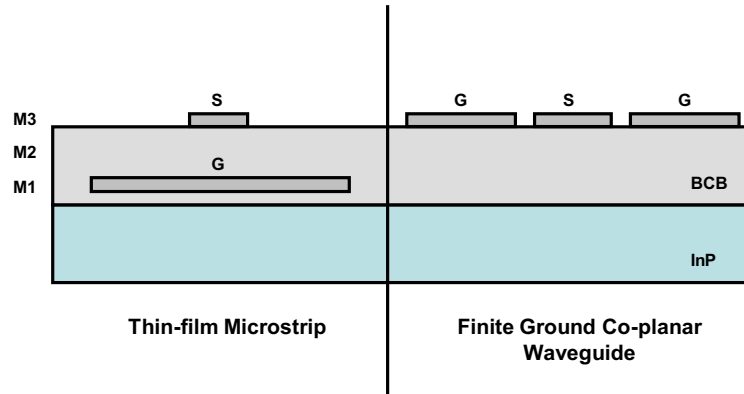
Figure 4.2: Topology comparison of Microstrip and Co-planar Waveguide Transmission Lines

implementation.

For the co-planar waveguide transmission line there are two ground conductors and one signal conductor. For this transmission line the characteristic impedance is once again defined by the signal-to-ground spacing and signal conductor width. This topology can have lower transmission line losses than thin-film microstrip, due to the ability to scale both the signal to ground spacing and signal line width.

To compare the performance of the microstrip and CPW transmission lines, several simulations were performed using the IE3D electromagnetic solver. The dielectric and metal layer structure of the process was entered exactly in the simulator along with the dimensions of the various transmission lines. Using the simulation results the loss per wavelength of the various transmission lines can be compared.

In figure 4.24, the loss per quarter-wave (at 75GHz) of the microstrip transmission line is plotted for various characteristic impedances. The dimensions of each line are given in table 4.1.1. For the narrow 50Ω line the 0.455dB loss is 0.1dB higher

Table 4.1: Microstrip Line Dimensions

Signal Width	Signal to Ground Spacing	Characteristic Impedance
6um	3um	50Ω
12um	3um	31.6Ω
33um	3um	15.8Ω

than for the wider, low impedance lines. In comparison a CPW transmission line with a characteristic impedance of 50Ω has a loss per quarter-wave of 0.303dB, which is 0.07dB lower loss than the wider microstrip lines. The dimensions of the CPW line are a signal width of 30um, signal to ground spacing of 5um and a ground plane width of 95um. The loss of the CPW line can be made almost independent of characteristic impedance as there is independent control of both the signal to ground spacing and signal line width (unlike in microstrip where the signal to ground spacing is fixed). In this way if higher characteristic impedance is needed the signal to ground spacing can be increased, with out needing to make the signal line narrow and lossy.

Another important aspect in the choice of transmission line topology is the ease of connecting components between signal and ground lines, such as shunt matching capacitors. The ground connections for both transmission line types are illustrated in figure 4.4. In the case of CPW since the signal and ground lines are on the same plane, shunt components can be placed without the need for via connections between metal layers. In the case of microstrip, vertical vias are required to make ground connections, as the ground and signal lines lie on different metal layers. This results
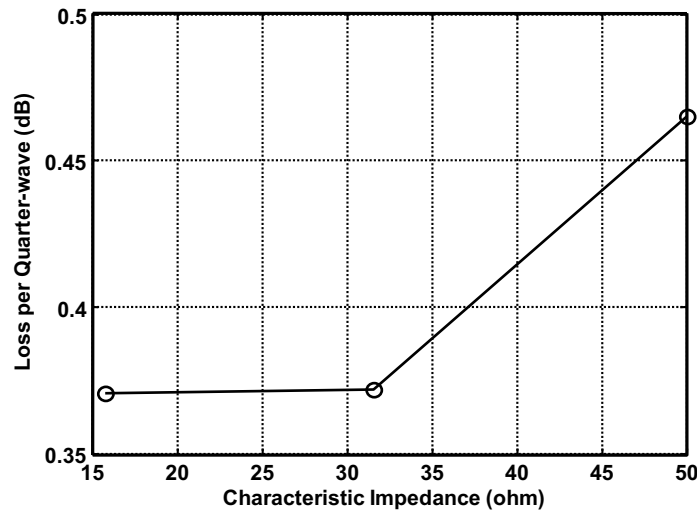
Figure 4.3: Variation in loss per quarter wavelength at 75GHz for Microstrip line

in increased ground inductance for the microstrip transmission line. This inductance is small however, since thin film microstrip is being used. The inductance of a 3um high, 1um x 1um wide via is just 1.5pH, which is approximately j1Ω at 100GHz.

For the implementation of the millimeter-wave amplifier the microstrip transmission line is chosen. The major advantages of using the microstrip line are the large area savings and simpler routing design on-chip. Routing CPW lines carries much more area overhead due to the fact that three lines need to be routed (signal plus two ground planes). The slightly higher loss of microstrip over CPW line is the primary disadvantage, but as most interconnects are much shorter than a quarter wavelength, this penalty is not significant.
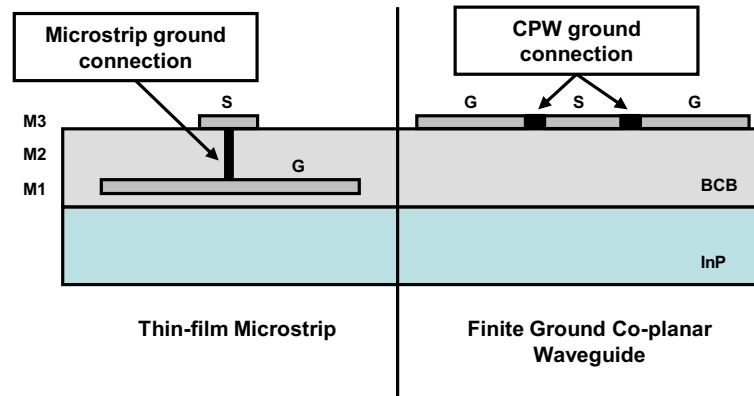
Figure 4.4: Comparison of ground connections for microstrip and CPW transmission lines

4.1.2 Matching Network Design and Simulation

Using the thin film microstrip transmission line described in the previous section a compact LC matching network was designed using a short section of transmission line and 2 MIM (Metal-Insulator-Metal) capacitors as shown in figure 4.1. The first capacitor is shunted to ground to provide impedance transformation and the second capacitor is a DC blocking component. The design of the input and output matching networks is governed by different criteria. The input matching network is designed for maximum power transfer, and so is a conjugate match to the impedance presented by the cascode power cell. The output matching network is designed to achieve the maximum output power from the devices and so is a designed to be a load-line match using load-pull simulation.

The MIM capacitors are modeled in the foundry design kit using a lumped model as shown in figure 4.5. At millimeter-wave frequencies this model is no longer accurate, so for the design of the matching networks both the transmission lines and
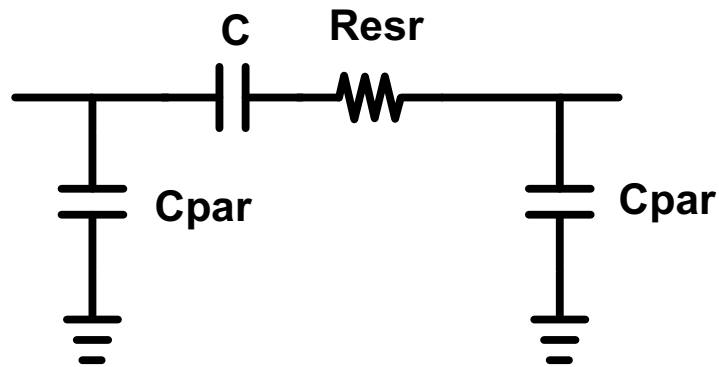
Figure 4.5: Lumped element model of MIM capacitors

the MIM capacitors are simulated using a full electromagnetic solver. In this way all the parasitics associated with the MIM capacitors are captured for accurate high frequency matching network design. The dimensions of these capacitors are small enough, such that even at the design frequency they can still be thought of as lumped element components (the size of the largest capacitor is less than 0.05 times a full wavelength at 75GHz). The capacitance per unit area of these MIM components is 0.25 fF/um^2.

Both the input and output matching networks described in this section are designed to match the amplifier to a 25Ω environment. This is done to optimize the bandwidth of the matching networks for the radial power amplifier described in section 4.3. For this amplifier a two stage matching topology is chosen, with a 50Ω to 25Ω impedance transformation implemented in the radial combiner/splitter network
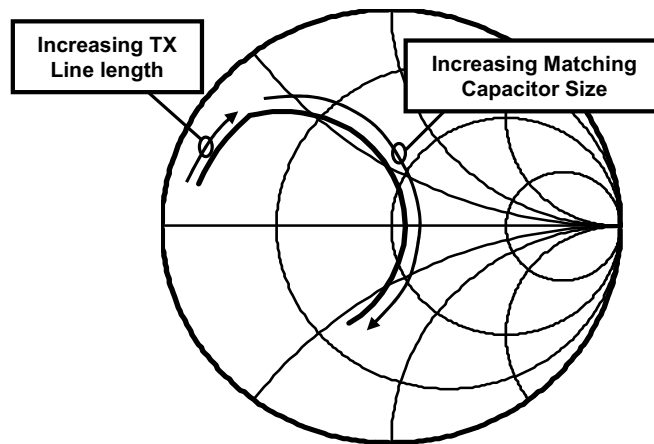
Figure 4.6: Impedance transformation contour of compact LC input matching network

and then the input and output matching networks transform the amplifier to a 25Ω environment. For the measurement of the unit amplifiers in a 50Ω test environment, a quarter-wave transmission line matching network is implemented at both the input and output.

For the input match the contour traced by varying the transmission line length and shunt capacitor size is plotted in figure 4.6 at a frequency of 75GHz. The low impedance presented by the input of the cascode power cell is transformed to a 25Ω impedance. The transmission line has a characteristic impedance of 35Ω and is varied from an electrical length of 1° to 7° in the plot. The matching capacitor is then swept from 1fF to 300fF.

Traditionally millimeter-wave matching networks are implemented with both series and shunt transmission line elements. Here the shunt transmission line is re-
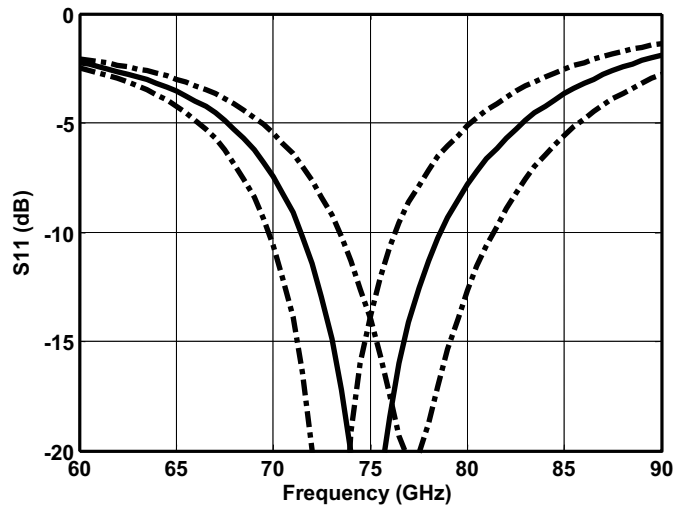
Figure 4.7: Variation of S11 as input matching capacitor varies +/- 15% from its nominal value (nominal - solid, capacitor variation - dashed)

placed with the shunt MIM capacitor. This MIM component has the disadvantage of having more variation across process. Figure 4.7 illustrates the variation of the input matching performance as the shunt capacitor value varies +/- 15% from its nominal value. It is seen that, at the design frequency of 75GHz, the S11 remains better than 10dB as the capacitor varies across process.

The output matching network is designed using load-pull simulation techniques. Load-pulling simulations are performed by varying the impedance presented at the output of the amplifier and generating contours of constant output power and efficiency. Using these contours the optimum matching conditions for maximum output power from the devices can be found. The output matching network is then designed to present this optimum impedance to the devices.

The load-pull simulation setup is shown in figure 4.8. In this simulation both
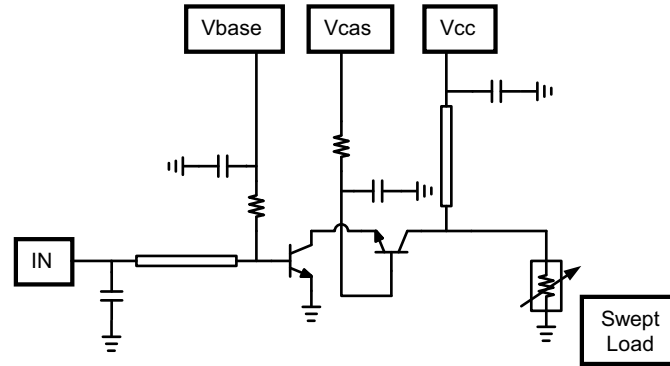
Figure 4.8: Load-pull simulation setup to determine maximum output power impedance condition

the input matching network and the quarter-wavelength bias choke feed are included. In the simulation these are modeled using s-parameter files generated from electromagnetic simulation of both the input match and the quarter-wave bias choke. Also the full device plus electromagnetic model of the 12 finger power-cell is included in the simulation, using the same techniques as described in section 3.5. In this way all of the parasitics associated with the device layout, input matching network and the collector bias choke are included in the load-pull simulation for improved accuracy in the output matching network design.

Using this simulation deck, the load presented at the bias feed is swept to determine the optimum impedance for maximum output power from the devices. The results of this simulation are shown in figure 4.9, with contours of constant output power plotted in 1dB steps. From this simulation with an input power of 12dBm
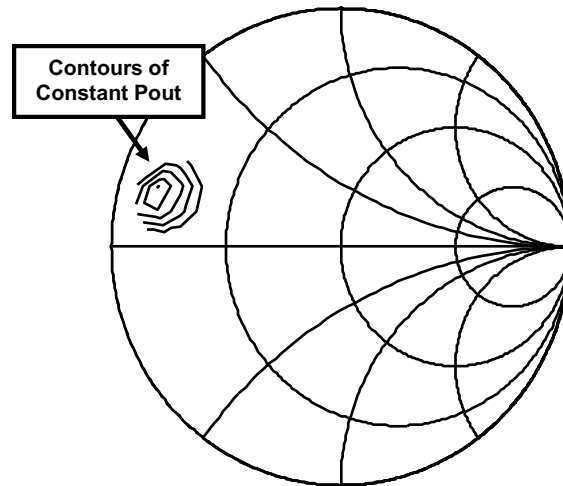
Figure 4.9: Load-pull simulation results showing contours of constant output power

the output power at the optimum impedance is 20.5dBm. The impedance at this point is 2.275+j*3.825, which is then used as the design goal for the single stage LC matching network at the amplifier output. Measurements presented in the following section show good agreement with the predicted output power from the load-pull design technique. The load-pull simulation was also performed for an input power of -20dBm, such that the amplifier is operating in small signal mode. In this case the optimum impedance is 1.55+j*3.65. This lower impedance is the conjugate match for the output matching network, but results in a lower voltage swing at higher signal levels and so is not the optimum power match.

The final input and output matching network layouts are illustrated in figure 4.10. From this figure the structure of the LC match is seen and the location of all matching and DC blocking capacitors are clearly visible. In this figure the metal 3

(a) Input matching network   (b) Output matching network
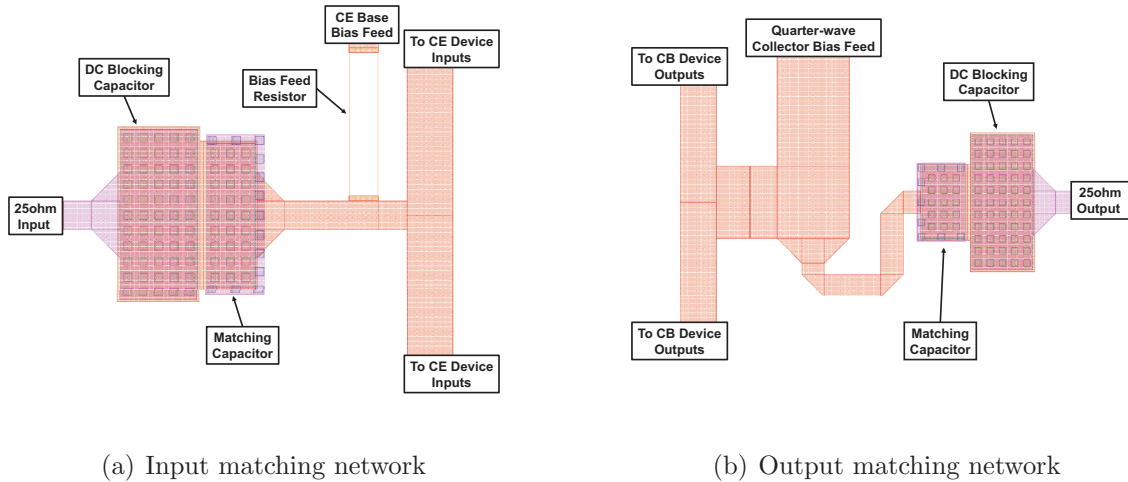
Figure 4.10: Layout of input (a) and output (b) matching networks (M3 top layer removed for clarity)

(M3) ground layer used for the inverted microstrip transmission lines, which overlays the entire layout, has been removed for clarity.

4.1.3   20dBm Amplifier Design, Simulation and Measurement

The millimeter-wave PA was designed using the previously described power cell as shown in figure 3.16. Single stage LC matches are implemented for both the input and output matches. The collector bias is supplied through a capacitively shorted quarter-wave feed, and at the input the base bias current is supplied through a 350Ω resistor. The bias voltage at the base of the CB stage is supplied through a 35Ω resistor. This helps to reduce the gain at lower frequencies by providing a resistive impedance. At millimeter-wave the grounding capacitors shunt this resistor so no gain degradation occurs.

The amplifier is designed to operate in class A with a quiescent bias point of

CE HBT's   CB HBT's
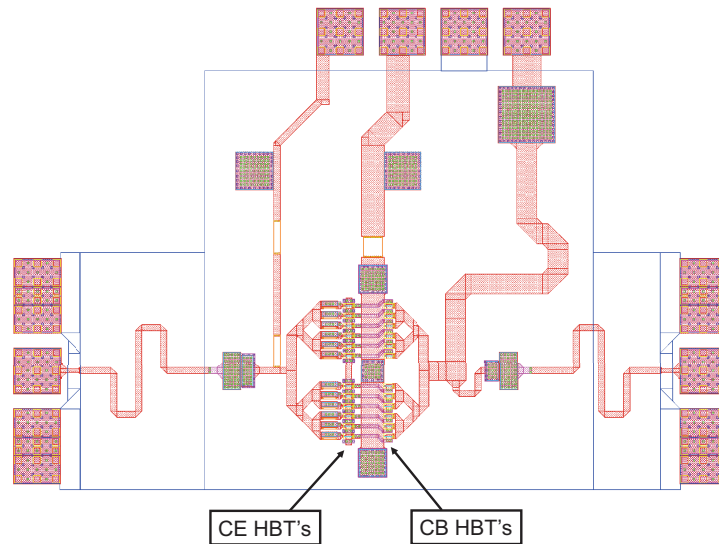
Figure 4.11: Final layout image of unit power amplifier - chip dimensions including pads 1140um x 770um

4V and 180mA. This corresponds to 15 mA per cascode finger, or a current density of $3mA/um^2$, the choice of which was discussed in section 3.1. The input match is designed to be a conjugate match to the input impedance of the power cell. For the output side a load pull simulation is performed to locate the optimum load impedance for maximum output power from the device. As described in the last section this simulation was performed with the quarter wave bias feed in place, which provides a short at the second harmonic at the output of the power cell.

Inverted microstrip transmission lines are used in the implementation of the amplifier with ground plane on the upper metal level M3. This is chosen over regular thin-film microstrip since no cutouts are required in the ground plane and the ground return paths are shorter and more clearly defined. The final layout image is shown in figure 4.11 and the chip dimensions including pads are 1140um x 770um.
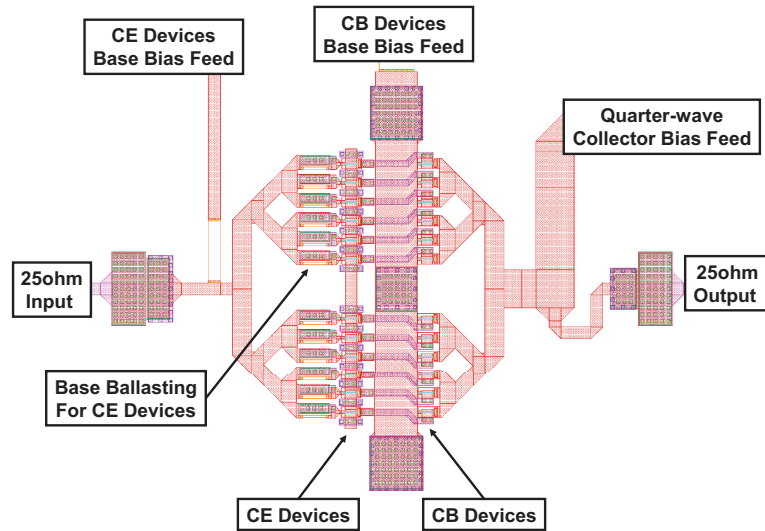
Figure 4.12: Layout image of core of unit power amplifier - core dimensions 520um x 370um

More details of the amplifier core are illustrated in figure 4.12 and the design details discussed in chapter 3 can be seen. The parallel RC base ballasting networks for the array of CE devices is shown at the amplifier input, and also the distributed grounding network for the base connection of the CB devices is shown. The input and output matching networks are clearly seen connecting the the amplifier input and output respectively. Finally the various bias feed connections are also marked. The dimensions of the core amplifier, including matching networks, are 520um x 370um, which is very compact.

The final amplifier is simulated using the Agilent ADS simulation tool. To capture all layout and interconnect related parasitics the entire amplifier structure is simulated in a method-of-moments electromagnetic simulator. The amplifier layout is divided into four subsections for efficient modeling and simulation. These sections
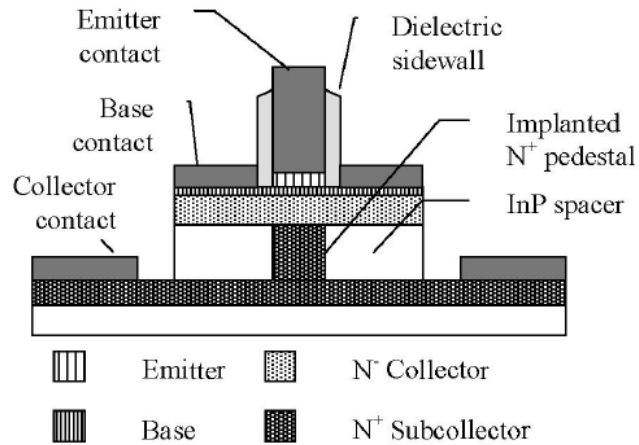
Figure 4.13: Teledyne InP DHBT device cross-section

are the input matching network, the output matching network, the collector quarter-wave bias feed and the core device interconnect structure. The input and output probe to pad transitions are designed to provide low reflection transitions, so both the input and output ports are modeled as ideal 50Ω terminations. The final aspect to be considered in the simulation is the DC probe parasitics. For the base bias connections to both the common-emitter and common-base devices, this is modeled as a 1nH inductance in series with a 1Ω resistance. For the collector DC connection a 100nF capacitor to ground is also included after the 1nH inductor to model the low frequency return path to ground provided on the probe card. Using this simulation deck both the on-chip and off-chip parasitics are accurately modeled.

The amplifiers are implemented in the InP DHBT process at Teledyne Scientific and Imaging [38]. An illustrated cross-section of an HBT device is shown in

figure 4.13. An ion implanted collector pedestal is included as part of the process for C_{BC} reduction. The pedestal results in low extrinsic C_{BC} by having low doping in the collector except for the area under the emitter. Dielectric sidewall spacers are also utilized to form self aligned base emitter junctions. These spacers provide electrical isolation between the emitter and base contacts. These features are integrated into the fabrication flow to result in a high yield manufacturable InP DHBT process.

For characterization of the amplifier both small and large signal sweeps are performed. For the small signal tests a 110 GHz network analyzer is used to measure the s-parameters of the amplifiers. A full 2-port Short-Open-Load-Thru (SOLT) calibration is used to define the reference planes of the small signal measurement at the amplifier input and output pads. The network analyzer used for these tests is the Agilent N5250C PNA, which operates from 10MHz to 67GHz. This analyzer is combined with external up-conversion and down-conversion frequency extension modules to provide a measurement range extending from 67GHz to 110GHz. To interface with the test wafer Cascade ACP-110 high frequency probes are used, which have a frequency range extending up to 110GHz. The SOLT calibration used to define the measurement reference planes is performed using a calibration substrate, whose calibration constants are used to remove interconnect and transition related non-idealities up to the probe tips. To confirm the accuracy of the calibration a short section of 50Ω transmission line is measured on the calibration substrate. The results of this calibration are shown in figure 4.14. From this figure it is seen that the S11 is better than -30dB across the band and variation in S21 is less than +/- 0.1dB. From
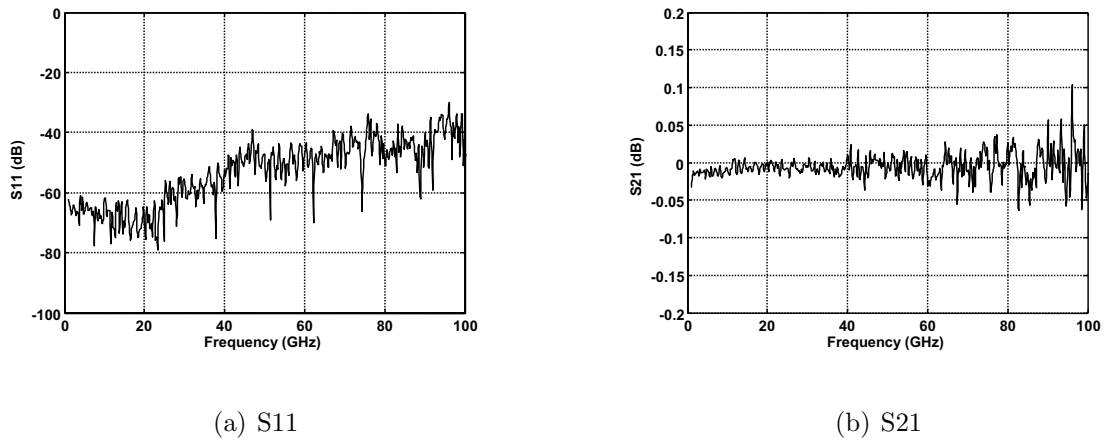
Figure 4.14: Measurement of 50Ω transmission line after SOLT calibration (a) S11 (b) S21

this data it is concluded that the calibrated measurements of the amplifier are accurate to within 0.1dB for the gain. Also the noise floor for S11 and S22 measurements is approximately -30dB at the highest frequencies.

The measurement setup for the large signal power sweeps is shown in figure 4.15. Here a narrow-band, but high power Gunn diode based oscillator is used as the power source and the maximum power available from the source is 19.75dBm. The power from this source is routed through low-loss waveguide to the device input port, with power control implemented using a passive attenuator. At the output, the power produced by the amplifier is passed from a 1mm-type coaxial cable to a waveguide power detector to give an accurate reading of the amplifier output power. The attenuator at the output is used to limit the power incident on the power detector, which has a maximum input level of 20dBm. The accuracy of this measurement relies on careful measurement of the losses introduced by each component.
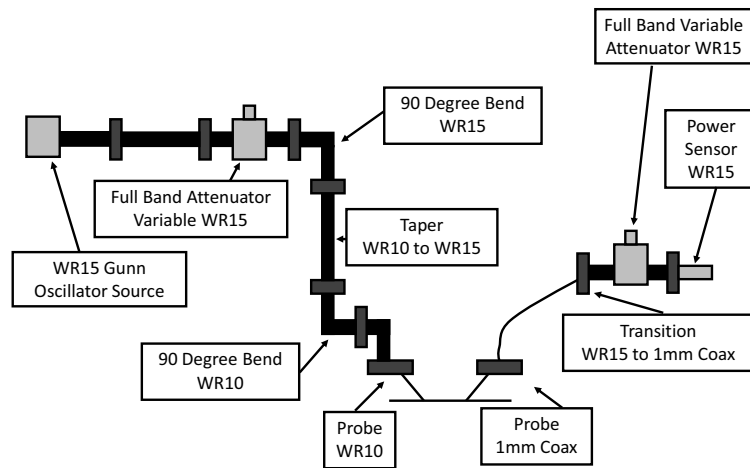
Figure 4.15: Measurement setup for millimeter-wave power sweeps

Table 4.2: Input Losses for Power Measurements

WR-15 Bends	Attenuator	Transition	Probe	Total Loss
0.4	0.28	0.2	1.3	2.18

Table 4.3: Output Losses for Power Measurements

Probe	Cable	Transition	Attenuator	Total Loss
0.7	3.2	0.7	5.4	10.0

The loss of each component in the chain is measured individually and listed in tables 4.1.3 and 4.1.3. For characterizing the waveguide components each one is tested individually using the Gunn source and calibrated power detector. The 1mm cable losses are found by measuring the return loss of each cable with a short terminating the other end of the cable. The S11 from this measurement gives the round-trip loss of the wave passing along the cable. The entire chain, from source to detector, is then measured using a short on-chip transmission line. This loss agrees with the expected loss from the sum of the loss measurements of the individual components to within 0.1dB. When measuring the amplifier the loss of the measurement setup is assumed to be the same as in the calibrated condition, which requires matched conditions for both amplifier ports. Small signal measurements show that in the desired band this is true, so the loss calibration can be taken as accurate. The measurement setup is organized such that the loss at the input side is minimized for maximum power transfer to the amplifier inputs, to drive each one into saturation.

Experimental results for this amplifier are presented in figures 4.16, 4.17 and 4.18. The amplifier is designed to operate with a center frequency of 75 GHz and the measured center frequency is 72 GHz. The measured peak gain is 12.5 dB and the amplifier 3dB bandwidth is 14 GHz, giving a fractional bandwidth of 18.6 %. For the power sweep the maximum measured output power is 20.6 dBm with a saturated gain of 7.1 dB. The PAE at this point is 13.9 %. It is seen in figure 4.16 that the measured small signal results agree very well with the simulation prediction, confirming the accuracy of both the HBT model extraction and the electro-magnetic interconnect
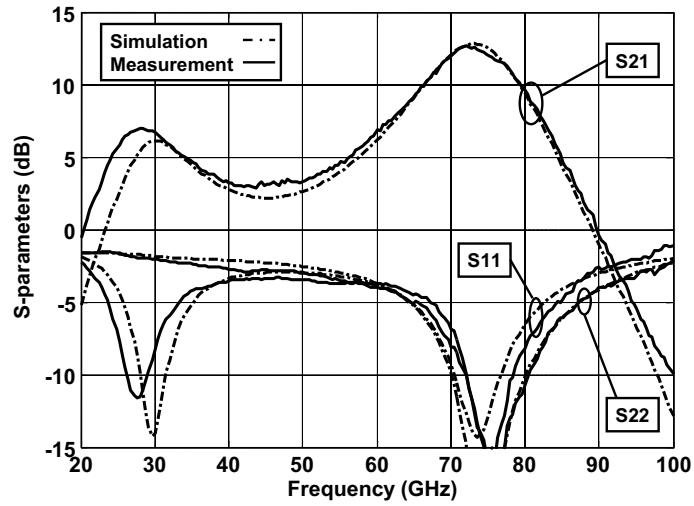
Figure 4.16: Small signal performance of unit power amplifier - simulation and measurement results
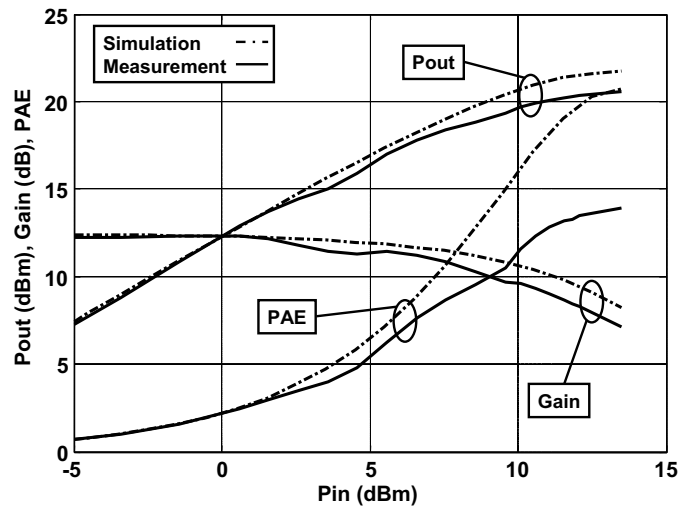
Figure 4.17: Large signal power sweep of unit power amplifier at 71 GHz - simulation and measurement results
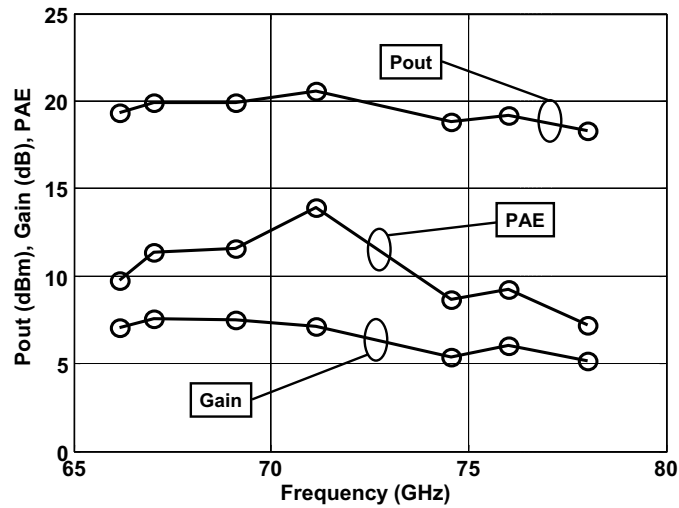
Figure 4.18: Saturated output power performance of unit power amplifier from 66-78 GHz

simulation. The simulation results for both output power and gain in figure 4.17 also agree to within 1.1 dB across the full input power range from small signal to when the amplifier is fully saturated. The PAE prediction is higher than measured by 7 % at saturation. This is due to the model predicting a drop in DC collector current as the amplifier enters saturation; this collector current drop is not seen in measurement.

Several Gunn oscillator sources were used to perform large-signal sweeps at different frequencies, the results of which are plotted in figure 4.18. The maximum output power is greater that 18.5dBm across the frequency range of 66-78GHz, which represents just a 2dB drop in maximum output power over a 16.5 % fractional band-width.

The amplifier small signal performance was also tested versus bias current, as illustrated in figure 4.19. Here the bias current in the amplifier is varied in 30mA
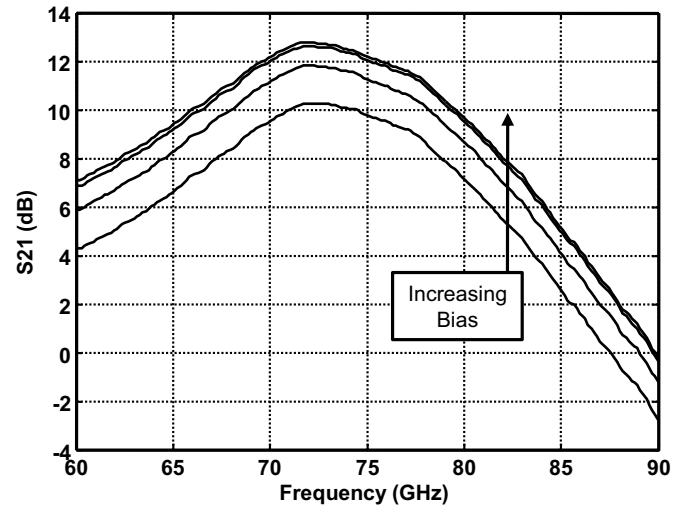
Figure 4.19: Change in amplifier gain versus bias current
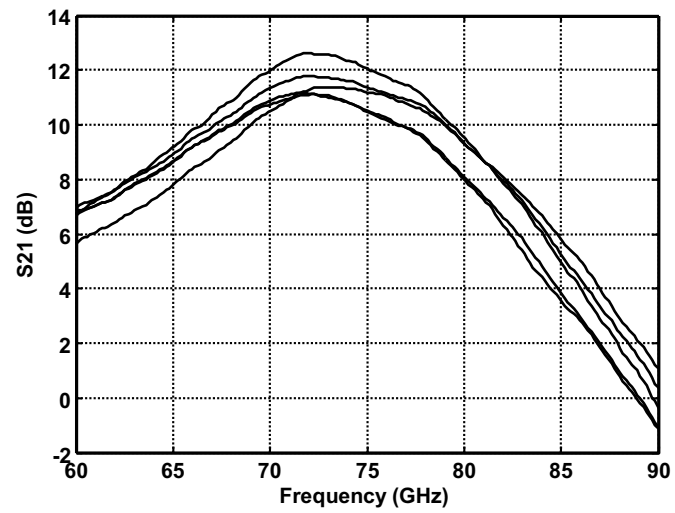
Figure 4.20: Variation in amplifier gain across wafer

steps from 90mA to 180mA. The amplifier gain increases from 10.2dB to 12.5dB, with the final two bias points having equal gain performance. The amplifier center frequency does not vary across bias current.

Yield and reproducibility of the amplifier was also tested. For all reticles tested the amplifier was functional and operated at the correct center frequency, exhibiting excellent yield performance. In figure 4.20 the amplifier gain for identical bias conditions at five different reticle locations is plotted. The gain varies by approximately 2dB across the wafer and the center frequency varies by almost 2GHz. Overall the amplifier shows very good yield and reproducibility characteristics across the single wafer which was tested.

4.1.4 Analysis of Amplifier Efficiency performance

The measured amplifier PAE and collector efficiency numbers are 13.89% and 17.24% respectively. For an ideal class A design the maximum collector efficiency is 50%. In this section the factors involved in the efficiency degradation will be discussed. The non-idealities to be considered in this section are the finite knee voltage of the amplifier, the output transmission line loss and the non-optimal load-line impedance. To quantify these effects, each of their contributions to the overall efficiency is found and expressed in equations 4.1 and 4.2.

$$\eta_{TOT} = \eta_{classA} * \eta_{Vknee} * \eta_{Rload} * \eta_{OPLoss} \tag{4.1}$$
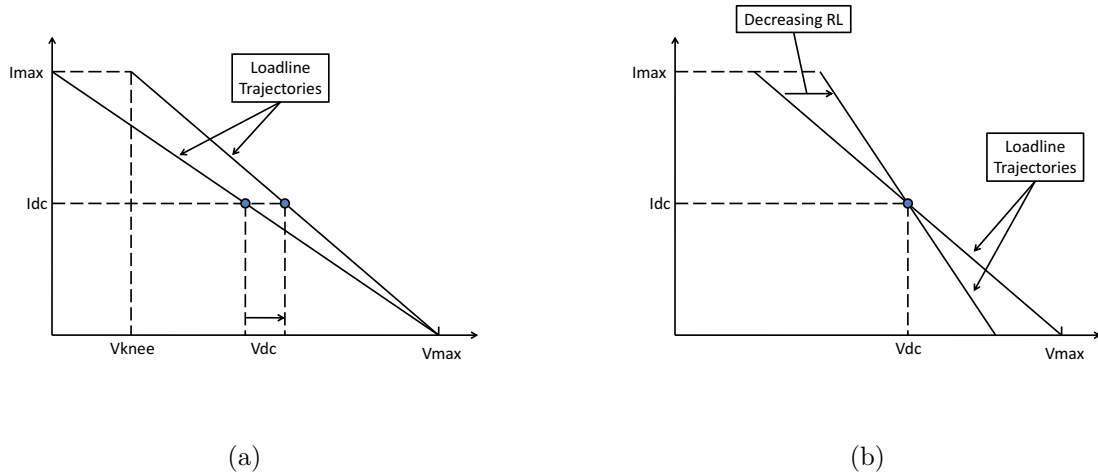
Figure 4.21: Effect of (a) increasing knee voltage and (b) reducing load resistance on load-line swing

$$\eta_{TOT} = \eta_{classA} * \left[\frac{V_{max} - V_{knee}}{V_{max} + V_{knee}} \right] * \left[\frac{R_{load}}{R_{opt}} \right] * G_{OP} \tag{4.2}$$

The effects of increasing knee voltage and decreasing load resistance are illustrated in figure 4.21. From this figure it is seen that both mechanisms have the same effect of reducing the maximum voltage swing at the output of the amplifier. The effect of increasing knee voltage is to increase the lower voltage limit of the output swing and hence the total swing is reduced, since the upper limit remains fixed by device voltage handling capability. This knee voltage is higher in a cascode topology compared to a common-emitter topology due the extra voltage required to keep both devices in the cascode in the linear region. The effect of reduced load resistance is also a reduced voltage swing, due to the fact that the maximum current swing is fixed, so a reduced load resistance leads to reduced voltage swing.

Using equation 4.2 and the DCIV of the power cell devices, the maximum

efficiency expected can be compared with the measurement results. The simulated DCIV curves of the power cell devices is shown in figure 4.22 with the optimum load-line overlaid across these curves. The knee voltage is approximately 1.5V and the optimum load-line resistance is 15Ω. With this knee voltage and load resistance the collector efficiency is 30%. When the effect of the 0.3dB output transmission loss is included in the efficiency calculation, the efficiency number reduces to 27.68%. The rest of the efficiency degradation is due to the non-optimum load resistance chosen for the design. As discussed in section 4.1.2, the output load is found from load-pull optimization of output power, at an input power of 12dBm. This resulted in a load impedance close to the the conjugate match for gain, and not the load-line match for collector efficiency. This was required to keep the gain high under maximum output power conditions for higher PAE. The load impedance applied at the output of the power cell is 2.275Ω. This impedance is transformed up through an LC match composed of the powercell interconnect lines and the individual device output capacitance. At the internal device plane this impedance is transformed up to approximately 9.5Ω resulting in an efficiency of 17.5%.

4.2   Power Combiner Design - On-Chip Radial Power Combiner

A power amplifier demonstrating higher output power, utilizing on-chip power combining, was also designed. The higher output power is desired to increase the
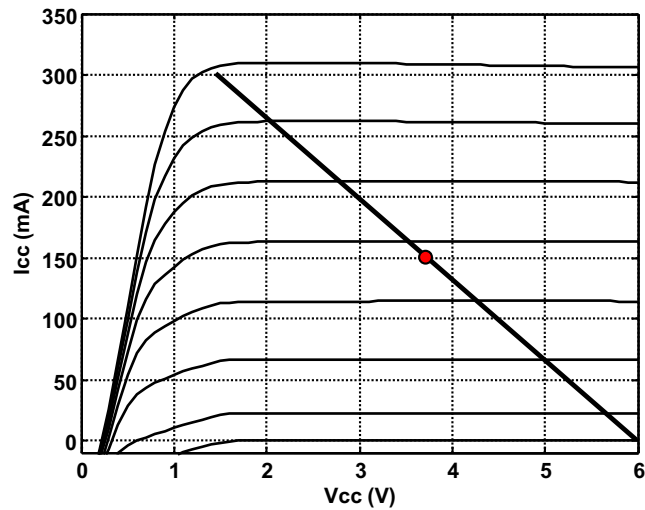
Figure 4.22: Simulated I-V characteristics of powercell with optimum loadline overlaid

range of E-band communications systems, as increased output power directly contributes to increased link budget for the communications channel. E-band radios are permitted under FCC rules to operate with up to 3W of output power [7].

4.2.1 Choice of Power Combiner Topology

When designing power combining networks for power amplifiers there are many options available. The first aspect to be considered is on-chip versus off-chip power combining techniques. Off-chip combining can be achieved by either waveguide based power combining [45,46] or spatial power combining [47,48,49]. The major advantage of off-chip combining is the lower combiner loss than can be achieved compared to on-chip combining. Waveguide based power combining also achieves bandwidths of at least 10%. The disadvantages of waveguide based combining are size, cost and the difficulty of low-loss microwave on-chip to off-chip transition design. Waveguide

based combiners are mechanically large structures, which require ever more expensive precision machining as the operating frequency is increased. Much more compact and mechanically simple spatial power combining can be achieved using grid amplifier structures, but these are not considered for high data rate applications as the achievable amplifier bandwidth is less than 1%.

On-chip power combining was implemented in this design for the advantages of monolithic integration, small size and low cost. Several techniques are available for this approach including Wilkinson combiners [50,51], Lange couplers [52,53], rat-race couplers [54] and the distributed active transformer (DAT) [55,56]. Both ring hybrid and Lange couplers can only be used to combine the power of two amplifiers, unless a corporate combining network is employed. This is not considered for the current design due to the increased transmission line losses incurred in a multi-stage corporate power combining network. For this reason it is desirable to combine the power of as many amplifiers as possible in a single stage of combining. This can be achieved using the DAT or an N-way Wilkinson combiner. As explained in [56], design of a DAT at millimeter-wave frequencies is quite difficult and on-chip parasitics result in different load impedances being presented at the outputs of the amplifiers to be combined. Also the input splitter network implemented with Wilkinson dividers, results in an input loss of 6dB, which degrades the amplifier PAE significantly. The N-way Wilkinson is a good candidate for combining multiple amplifiers in a single stage. For this design, however, this N-way Wilkinson concept is combined with the radial power combiner network topology [57,58] to provide an on-chip planar radial

power amplifier topology. The advantages of this approach are the ability to combine the power from multiple amplifiers in a single stage in a compact fashion. This is achieved by allowing the splitter and combiner networks to overlap on-chip and in this way save area.

4.2.2 Radial Power Combiner Overview and Operation

The amplifier was implemented using a planar radial splitter/combiner topology. The overall layout of a 4-way radial power splitter and combiner circuit is shown in figure 4.23. The signal enters the amplifier from the left and is then split equally using a planar radial structure and fed to the inputs of four unit power amplifiers. The output power from each of these four amplifiers is then combined using another planar radial structure. In this figure the locations for the unit power amplifiers are marked, as well as the locations of vertical transitions and input/output circuit overlap locations. No isolation resistors are present in this amplifier topology. Isolation resistors are usually present in radial power combiner networks to dissipate any out of phase power present at the output. Without the presence of these isolation resistors this out of phase power will flow between the unit power amplifiers and could lead to odd-mode instabilities or inter amplifier load-pulling effects. Since this radial structure is integrated monolithically on-chip, all of the unit amplifiers are well matched and will present equal phase power at the output, and hence isolation is not required. In the following sections the transmission line design, vertical transition design and input/output overlap design are discussed in more detail.
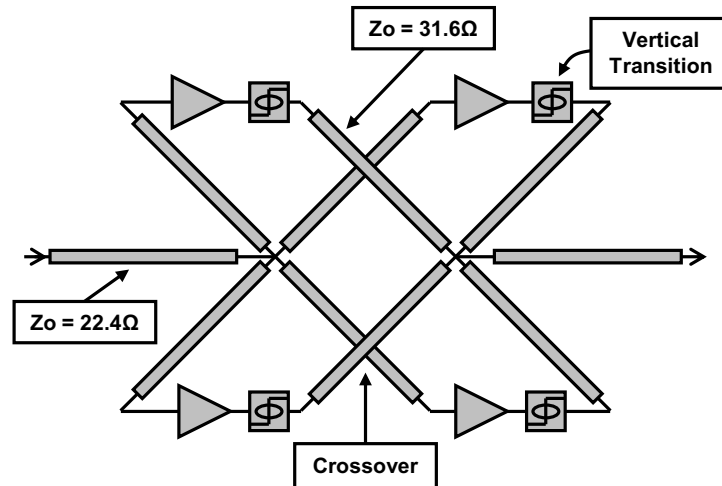
Figure 4.23: Schematic overview of 4-way planar radial splitter/combiner layout

4.2.3   Transmission Line Design

For this design both the input splitter and output combiner are implemented using microstrip transmission lines. The back-end of the process and transmission line simulation techniques are identical to that described in section 4.1.1. For the splitter, the lowest metallization layer M1 is used for the signal with M3 as the ground; and for the combiner M3 is the signal and M1 is ground. The need for the crossover components would have been eliminated by using M2 as a common ground plane with M1 and M3 as the signal lines for the splitter and combiner respectively, but this leads to increased transmission line losses.

A finite ground microstrip transmission line topology is chosen to allow for simple microstrip crossover circuits to be designed. The width of the finite ground plane is determined from simulation. The ground plane width in the microstrip wave mode
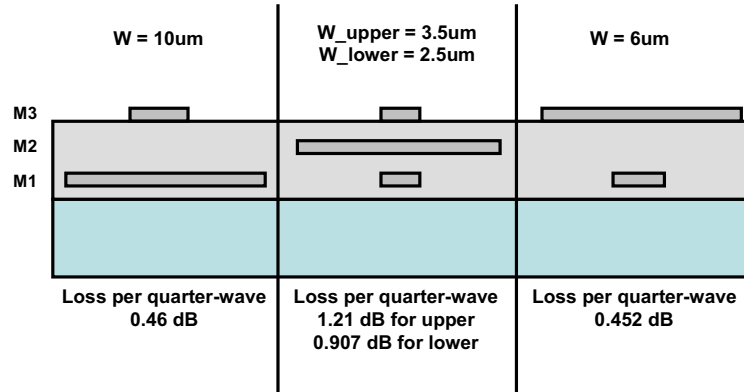
Figure 4.24: Transmission line losses for various microstrip configurations

ideally does not affect the characteristic impedance of the transmission line. With this constraint, the width of the ground plane was increased until the characteristic impedance converged asymptotically to the microstrip characteristic impedance for an infinite width ground plane. This finite ground place microstrip transmission line has the same characteristics as that of infinite ground plane microstrip lines due to the fact that the ground return current is concentrated in the area directly beneath the signal line, and so removing ground plane far from the signal line has negligible affect on both the return current and microstrip mode fields.

The three microstrip configurations are shown in figure 4.24, as well as the 50Ω signal width and simulated loss per quarter-wave at 75 GHz for each 50Ω line. It is clear that the microstrip configurations with maximum signal to ground spacing provide lower loss. These have been adopted for this design. By utilizing this transmission line choice a loss saving of 1.2 dB is achieved in the splitter/combiner circuit.

4.2.4 Inverted Microstrip to Microstrip Transition

In order to utilize both the splitter and combiner in a single circuit a transition from inverted microstrip to microstrip must occur at some point. The transition involves the signal line going from M1 to M3 and the ground plane going from M3 to M1. This happens in 3 steps, as shown in figure 4.25, in order to minimize the reflections occurring at the transition.
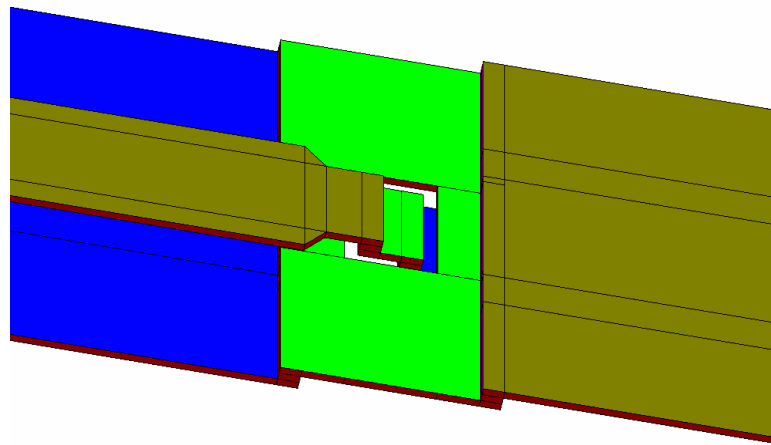
Figure 4.25: Vertical inverted microstrip to microstrip transition

In the first step the ground plane is stepped from M3 to M2. To keep a constant characteristic impedance the width of the signal line on M1 is reduced. In the second step the signal line transitions from M1 to M3 through a hole in the ground plane in M2. The dimensions of the ground plane cutout are optimized to increase the capacitance to ground to compensate for the inductance of the via. In the final step the ground plane is stepped from M2 to M1 and the signal line, which is now on M3, is widened to maintain the correct characteristic impedance. The transitions of

the ground plane from one metal layer to another is accomplished by using a row of minimum spaced square vias. This via array approximates the performance of a single slot via between the metal layers. The transitions are optimized using IE3D and the results are plotted in figure 4.26. Here a simulated return loss of at least -30 dB from 1-100 GHz is observed.
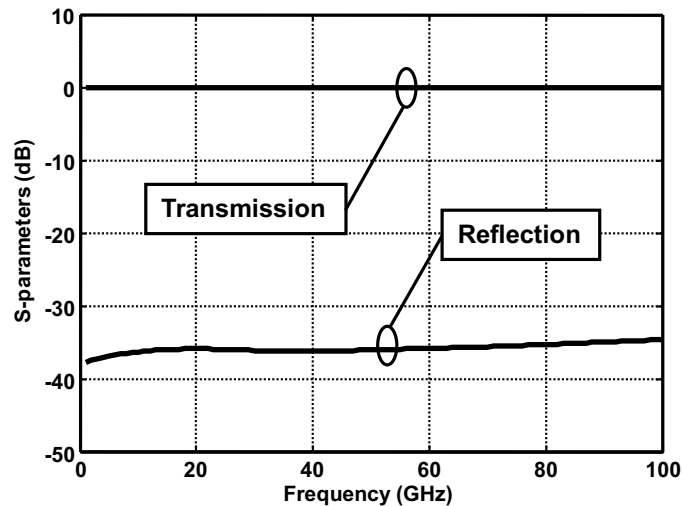
Figure 4.26: Simulated Transmission (S21) and Reflection (S11) parameters of microstrip transition

4.2.5 Microstrip Crossover

As illustrated in figure 4.23 the splitter and combiner overlap at 2 locations in the layout. A crossover design with high isolation between the splitter and combiner is required, while remaining transparent to the transmitted signal. The splitter and combiner paths cross at right angles and the crossover design is shown in figure 4.27. At the crossover point both paths share a common ground plane on M2 and the signal

lines on M1 and M3 are narrowed to maintain a constant characteristic impedance. This structure was optimized in IE3D and the final simulation results are plotted in figure 4.28. Here isolation between the crossing transmission lines of greater than 40 dB from 1-100 GHz is observed, and the return loss at each port is also at least -25 dB across this frequency range.
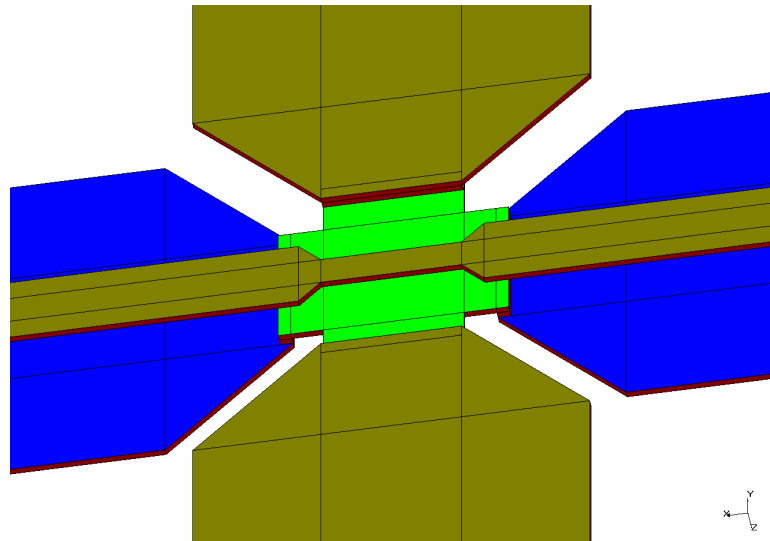
Figure 4.27: Splitter and combiner crossover design

4.2.6   Back to Back Results

For the implementation of the splitter/combiner circuit, the design frequency was chosen to be 75 GHz. An impedance transformation from 50Ω to 25Ω was built into the design and all line lengths were designed to be quarter wavelength at 75 GHz.

Due to space constraints only a back-to-back test version of the circuit was fabricated. The fabricated circuit is seen in figure 4.29. A section of 25Ω transmission
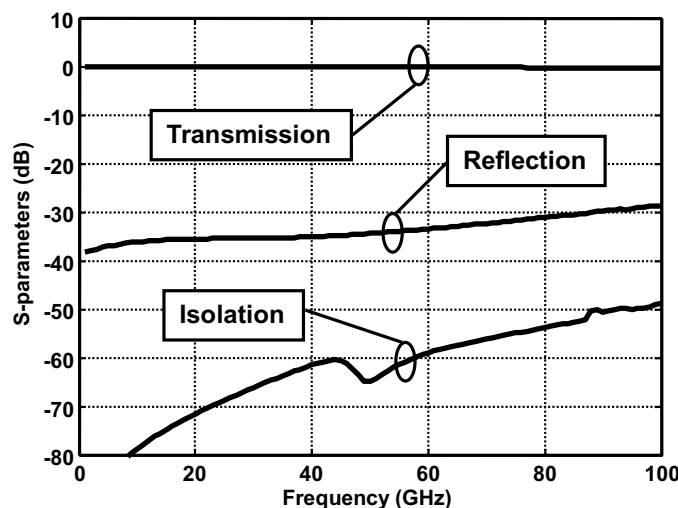
Figure 4.28: Simulated Transmission (S21), Reflection (S11) and Isolation (S31) parameters of microstrip crossover

line is inserted between the splitter and combiner. In the final amplifier implementation this section of transmission line is replaced with the unit amplifiers to be power combined. The circuit dimensions are 2025um x 840um. In figure 4.30 both the measured and simulated transmission and reflection parameters of the back-to-back splitter/combiner network are plotted. The combiner performs well with simulation and measurement showing good agreement. For the measured circuit a center frequency of 73 GHz is observed and the measured back-to-back insertion loss at this frequency is 3.45 dB, of which 0.1 dB is due to reflection and 3.35 dB is due to dissipative loss in the transmission lines. The -10 dB return loss bandwidth of the combiner extends from 60-85 GHz for a 25 GHz bandwidth. When comparing the measurements to simulation it is seen that the center frequency has shifted lower from the simulated value of 76 GHz to 73 GHz, but the -10dB reflection bandwidth agrees well

with simulation. Also the insertion loss at higher frequencies is larger than predicted in simulation. In the desired band of 71-76 GHz however the discrepancy in insertion loss is less than 1 dB.
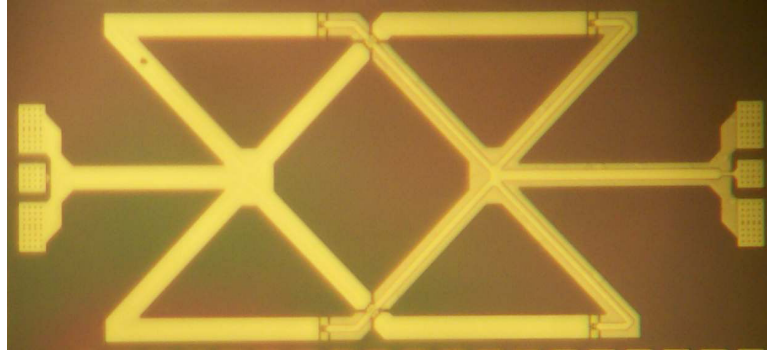
Figure 4.29: Die photograph of planar radial circuit layout (circuit dimensions 2025um x 840um)
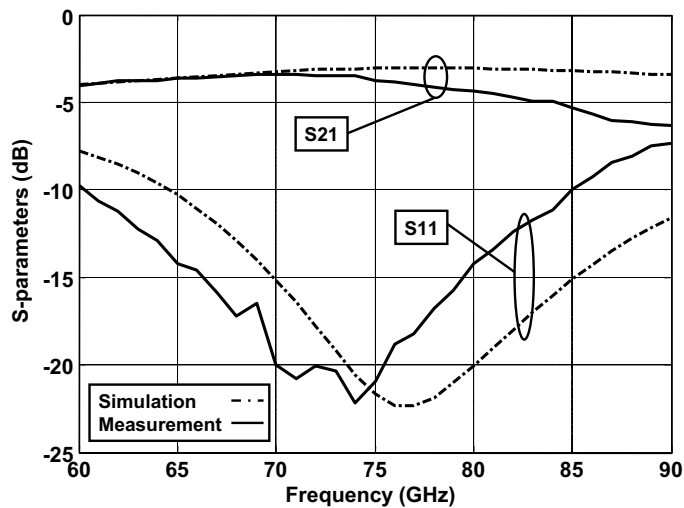
Figure 4.30: Performance of back-to-back radial splitter/combiner circuit

Given the measured performance of the back-to-back circuit, both the splitter and combiner can be assumed to have an insertion loss of 1.72dB. Using these

numbers, the expected radial amplifier performance can be found in terms of output power, gain and efficiency. If four of the previously measured amplifiers are combined using this structure, the expected drop in gain is 3.45dB, resulting in a gain of 9.05dB. The output power resulting from combining four unit amplifiers with a combiner loss of 1.72dB is 24.88dBm (20.6dBm+6dB-1.72dB). Finally, the collector efficiency of the radial power amplifier is also expected to be 11.55% (17.32% for the unit amplifier) given the 1.72dB combiner loss.

4.3   Planar Radial Power Amplifier Design

Using the building blocks described in the previous sections the final planar radial power amplifier was designed. The unit amplifiers are placed at the 25Ω points in the planar radial splitter/combiner circuit. The resulting circuit is a 4 way combined amplifier. Figure 4.31 shows the full power amplifier die photograph. The total die size including pads is 2025um x 1920um. Each of the four unit amplifiers is biased independently with each having pads for Vcc, ground, CB device base connection and CE device base connection. All ground and Vcc pads are shorted together off-chip to provide common DC power rails for the entire amplifier. High frequency ground return current is all confined on chip and hence amplifier performance is not dependent on the high frequency characteristics of these off-chip power and ground connections.

This power splitter/combiner design provides little isolation between the output ports of the 4 amplifiers to be combined, as no loss element is introduced to dissi-

pate odd mode power transfer between the ports, such as is the case in the Wilkinson combiner circuit. The need for isolation is important if the output signals from the unit amplifiers can become unintentionally phase shifted relative to each other. From simulations the unit amplifiers produce equal phase signals, so load pulling and signal transfer between the unit amplifiers is not expected, or seen in measurement.
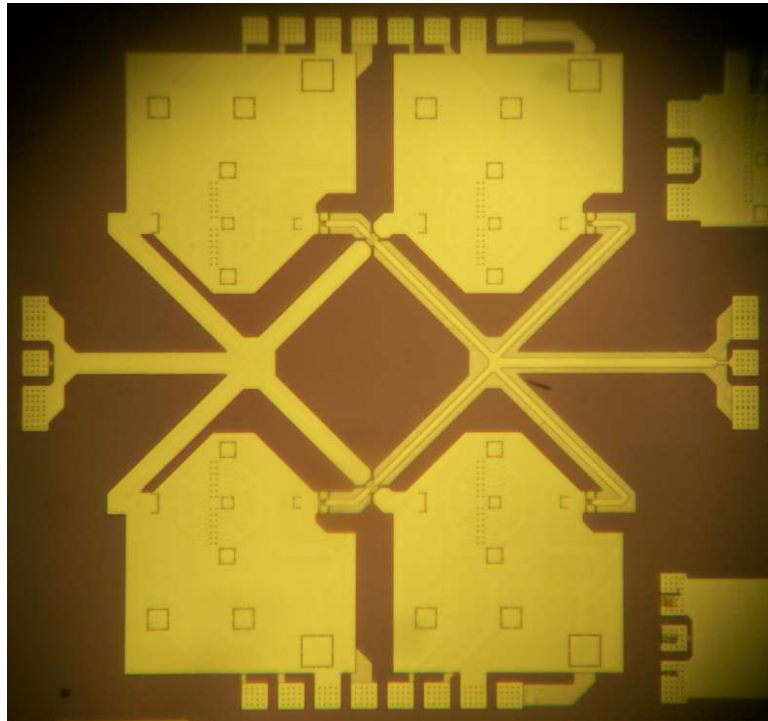
Figure 4.31: Die photograph of 25dBm Planar Radial Power Amplifier (circuit dimensions 2025um x 1920um)

The test setups for both the small and large signal measurements are as described in section 4.1.3. The major limitation of the test setup is the maximum power level, which can be supplied to the amplifier input from the Gunn oscillator source. The maximum power from the source is 19.75dBm, supplied through a loss of 2.18dB, resulting in 17.57dBm at the chip.
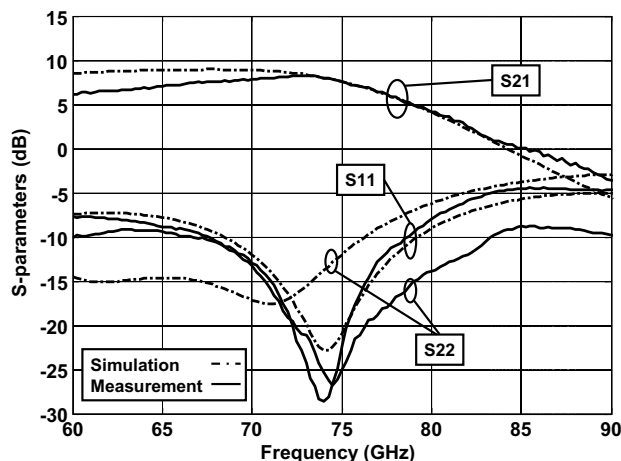
Figure 4.32: Small signal performance of the Planar Radial Power Amplifier

Figures 4.32 and 4.33 demonstrate the small and large signal amplifier performance. The measured and simulated small signal results agree well, with the S-parameters showing that the gain is correctly centered in the design band, with at a center frequency of 72 GHz. The maximum measured small signal gain peaks at 8.25dB, while the corresponding input and output return losses are better than -15dB. The 3dB gain bandwidth extends from 54.5GHz to 78.5GHz for a fractional bandwidth of over 40 %. The small signal simulation included the full models for each of the unit amplifiers developed in 4.1.3 and s-parameter models for the splitter and combiner networks from electromagnetic simulations. Comparing to the expected gain of 9.05dB from section 4.2.6, the measured gain is 0.8dB lower. The calculation in section 4.2.6 does not include the effect of reflection loss on the gain of the overall amplifier, and so a degradation from the predicted gain is expected.

The power sweep of figure 4.33 is performed at a frequency of 72GHz, with the
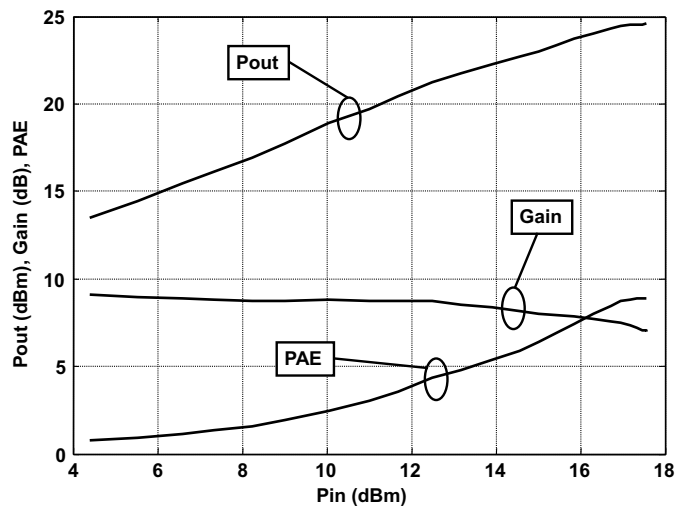
Figure 4.33: Large signal performance of the Planar Radial Power Amplifier

amplifier reaching an output power level of 24.6dBm. At this power level the gain has

compressed to 7dB and the amplifier demonstrates a Power-Added-Efficiency (PAE)

of 8.9 %. From the figure it is seen that the amplifier is not yet fully compressed, but

the measurement was performed up to the maximum source power available in the

laboratory. The power sweep was performed using Gunn diode based sources and a

V-band power sensor. All cable and probe losses at the input and output were ac-

counted for using a loss calibration identical to that described in section 4.1.3. Large

signal simulation results are not available for direct comparison with this measure-

ment, due to harmonic balance simulator convergence problems when all 4 amplifiers

are power combined. The measurements of both the unit amplifiers and the radial

splitter/combiner give an expected output power of the radial power amplifier of

24.9dBm when fully saturated as described in section 4.2.6, which agrees closely with

the measurement.

A comparison of this work with recently published state of the art millimeter-wave power amplifier designs is presented in table 4.4. From this summary it is seen that the design presented in this work represents the highest reported output power for an amplifier in a bipolar process at these frequencies. Also from this table it can be concluded that InP HBT devices in a manufacturable technology can be utilized to approach the power levels previously only reached by InP or GaN HEMT based devices. The amplifier also achieves good efficiency performance along with wide bandwidth. Comparing to other bipolar solutions the presented work combines the best performance for output power and efficiency, and equals the best bandwidth performance of previously published designs.

4.4   Conclusion

In this chapter many of the aspects involved in the design of millimeter-wave power amplifiers were discussed, including transmission line choices, compact matching network design and planar radial power combiner design. Using these techniques an E-band power amplifier with measured output power of 24.6 dBm was designed and fabricated. This represents the highest reported output power and efficiency for any bipolar process at these frequencies.

Portions of chapter 4 appear in the Proceedings of the International Microwave Symposium, 2008 and have been submitted for publication in the IEEE Transac-

Table 4.4: Comparison with recent Millimeter-wave Power Amplifier results

Frequency (GHz)	Technology	3dB Bandwidth	Psat	P1dB	S21max	PAE	Reference
72	InP DHBT	23	24.6	22.4	8.25	8.9	This Work
72	InP DHBT	14	20.6	17.8	12.5	13.9	This Work
90	SiGe HBT	18	19.6	18.8	10.6	15.4	Chang [59]
60	SiGe HBT	-	23	-	20	6.3	Pfeiffer [56]
85	SiGe HBT	24	21	-	8	3.4	Afshari [60]
75	InP DHBT	-	19	19	5.5	8	Wei [61]
94	InP HEMT	-	26.3	-	12	20	Ingram [62]
80	GaN pHEMT	12	27	24	15	12	Micovic [63]

tions on Microwave Theory and Techniques, 2009. Contributions from co-authors M. Urteaga and R. Pierson of Teledyne Scientific and Imaging and P. M. Asbeck of UCSD are greatly appreciated. The dissertation author was the primary investigator and author of these papers.

Chapter 5

Conclusion and Future Work

With the onset of the Information Age in the past decade, the amount of data being transmitted both wired and wirelessly has grown exponentially. It has also become clear that in this era access to information, regardless of location, has become a common expectation. The combination of these forces has led to an explosion in the bandwidth requirements of wireless communication systems. Expanding the bandwidth of a wireless communication system can be achieved by two methods; (1) increasing the modulation order of the communication system to increase the amount of information transmitted for a given channel bandwidth or (2) increasing the channel bandwidth, while keeping the modulation order low. It is the second of these two approaches, which is being pursued in the development of millimeter-wave wireless communication systems, where the availability of wide frequency bands can be leveraged in the development of high data rate wireless communication systems.

The goal of the work which has been presented in this thesis, was the devel-

opment of power amplifier circuits to enable the next generation of millimeter-wave wireless communication systems. The design of compact, high power and monolithically integrated power amplifiers, as achieved in this work using InP DHBT technology, demonstrates the feasibility of integrating the power amplifier with a full millimeter-wave transmitter.

5.1 Summary of Dissertation

The work presented in this thesis focused on investigating and solving three issues related to the development of millimeter-wave power amplifiers. As a first, the measurement and modeling of discrete InP DHBT transistors was required before the design of any power amplifiers could continue with confidence in the underlying device models. Secondly the development of compact, high-power, multi-finger power transistor cells was pursued to provide a core for full power amplifier design. Finally, power amplifier and compact, low loss power combiner circuits were developed, leveraging the earlier work of the dissertation.

5.1.1 Compact Modeling of Discrete InP DHBT Devices

The development of high speed and high voltage handling InP DHBT devices in recent years has opened up possibilities for the design of compact power amplifiers at millimeter-wave frequencies. In order to take advantage of this technology for the development of power amplifiers, accurate models are required, which capture the

characteristics of the devices over a wide range of operating voltages and currents. For the design of a small signal circuit, such as a low noise amplifier, a simple model, which captures the device characteristics around the desired operating point will yield good results. In a power amplifier however, the device is operated in large signal mode, and a large range of operating voltage and current is exercised. For this reason the Agilent HBT model was chosen as the compact model to best capture the operation of the InP DHBT devices. This model was developed to include the unique characteristics of both GaAs and InP DHBT devices and contains the capability to capture heterojunction barrier effects, non-linear Cbc effects and complex ft and fmax curves versus both collector current and voltage. The model can also be used to accurately capture the temperature dependent effects seen in high power density DHBT devices.

The modeling work began with the careful measurement of the devices to be modeled, with particular attention paid to correct measurement de-embedding at millimeter-wave frequencies. Using the measurement results the DC, RF and temperature dependent model parameters are extracted. The final outcome of this work was a set of compact models, which accurately capture the InP DHBT device operation over a wide range of operating points and frequency.

5.1.2 Millimeter-wave Cascode Power Cell Design

The next step in the design of millimeter-wave power amplifiers is the design of the power amplifier core. This was addressed in chapter three of the dissertation.

Firstly the choice of device dimensions and operating point were investigated from the aspects of linearity and gain. Once the choice of amplifier configuration was picked, the remainder of the work focused on two critical aspects of the core cell design. The first of these considerations is the design of a thermal ballasting network for the millimeter-wave amplifier core. The final ballasting network was a parallel RC network at the base of each finger in the amplifier core, which was shown to be optimal for both thermal ballasting and amplifier stability.

The next aspect of the amplifier core design is the design of the AC ground connection at the base terminal of the common-base transistor in the cascode topology. The optimal design of this connection for stability and gain performance was found to be a distributed capacitor layout, which ensures equal contribution to the output power from each of the transistor fingers in the power cell. Using these design techniques the amplifier power cell was then completed and fully characterized in both simulation and measurement. The power cell showed good gain and stability performance across the full frequency band from 1-100GHz.

5.1.3   Radial Power Combiner and Power Amplifier Design

The millimeter-wave power cell was then incorporated in the design of a monolithically integrated power amplifier, which utilized a novel planar radial power splitting and combining technique. Firstly the design of a compact unit power amplifier was described. This amplifier was fully characterized in the lab and achieved an output power of 20.6dBm. The design of a novel planar radial power splitter and

combiner circuit was then described, with all important aspects of the design covered in detail. A back-to-back splitter and combiner was characterized in the lab, and was shown to be a low loss and compact splitter-combiner network.

The final part of the work involved utilizing four unit power amplifiers along with the planar radial network to design a planar radial power amplifier circuit. This design achieved an output power of 24.6dBm and a PAE of 8.9 %. This performance achieves both the highest output power and efficiency of any published power amplifier at these frequencies in a bipolar process. This performance is also comparable to the published results of HEMT based amplifiers. Hence the amplifier demonstrates the feasibility of monolithically integrating the power amplifier with the transmitter for compact millimeter-wave wireless communication chipsets.

5.2   Future Work

While many demonstrations of millimeter-wave power amplifier solutions have been published utilizing many different device technology options, there are still several opportunities for future work in this area. From a device perspective the resistance of the base metal contact can be optimized to result in higher fmax for long fingers. This improvement could be used to develop higher power amplifier core cells, to approach or exceed the performance of HEMT based amplifiers.

Another area for investigation would be to extend the planar radial power splitter and combiner network to combine the power of six or eight amplifiers in a

single stage. This would require the design of more compact unit power amplifiers, a task which would be helped by the development of an optimized base metal contact for longer finger length devices as just described. The design of a six or eight way radial power amplifier network would also be helped by the presence of extra metal layers in the back-end, by allowing the input and output networks to overlap more and further compact the design.

Once a compact and high efficiency power amplifier has been developed, the next design challenge for future work would be monolithic integration with an up-converter and pre-driver amplifier. Demonstration of such a solution is very attractive for its low cost, small size and ease of interface with a low frequency chip which would provide the data stream at the intermediate frequency (IF).

As the need for higher bandwidth wireless communication links increases, the commercial viability of millimeter-wave communications will become a reality, along with the resources which will make possible the development of these future millimeter-wave chipsets.

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