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Screening-engineered Field-effect Photovoltaics and Synthesis, Characterization, and Applications of Carbon-based and Related Nanomaterials

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Screening-engineered Field-effect Photovoltaics and Synthesis, Characterization, and Applications of Carbon-based and Related Nanomaterials

by

William Raymond Regan

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requirements for the degree of

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University of California, Berkeley

Committee in charge:

Professor Alex K. Zettl, Chair

Professor Michael F. Crommie

Professor Ali Javey

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Abstract

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Carbon nanomaterials, and especially graphene (a 2D carbon allotrope), possess unique electronic, optical, and mechanical properties and allow access to both new physical phenomena and reinventions of familiar technologies. In the first part of this thesis (chapter 2), the low carrier density and high conductivity of graphene are used to repurpose the electric field effect (used for many decades in transistors) into a universally-applicable doping method for electrically-contacted semiconductors. This method, referred to as "screening-engineered field-effect photovoltaics" as the electric field doping is enabled by a carefully-designed poorly-screening electrode (e.g. graphene), is shown to open up many new low-cost and abundant semiconductors for use in high efficiency solar cells. We extend this method beyond ultrathin materials such as graphene and show that 1D nanowire electrodes made of *any* material also allow penetration of applied electric fields. The next part of this thesis (chapter 3) focuses on the fundamental properties of graphene – its structure, synthesis, characterization, and manipulation – and on using graphene as a building block for other nanostructures: grafold, graphene sandwiches and veils, and graphritos. In chapter 4, various graphene electronics are constructed and tested. Graphene field-effect transistors (FETs) and p-n junctions are fabricated to study the influence of the substrate on graphene carrier mobility and doping. Graphene nanoribbons and grafold FETs are made to investigate the effects of additional confinement on electronic transport. Chapter 5 summarizes synthesis methods and additional experiments with other nanomaterials, including dichalcogenides and chalcogenides (magnesium diboride, gallium selenide, and tin sulfide), carbon nanomaterials (carbon nanotubes and graphene), and copper oxide. Additional measurement and fabrication methods are discussed in appendix A.

To Vicki

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This thesis is dedicated to Vicki Hsieh for her constant support and for believing in me.

Chapter 1

Introduction

This is an exciting time to study nanomaterials. With the explosion of computing power in the past few decades and development of several new experimental techniques to fabricate 1D and 2D materials, there has perhaps never been more low-hanging fruit. In just one example, the many possible chiralities of single walled carbon nanotubes that can be sythesized has been equated to suddenly opening up a new periodic table.

In this thesis, I discuss my work on 1D and 2D nanomaterials, with special emphasis on graphene, a single-atom-thick sheet of sp^2-bonded carbon. I begin by focusing on an ongoing photovoltaics project that touches on many aspects of my research, materials synthesis (both quasi-1D and 2D materials) and fabrication/measurement of electronic devices. In later chapters, I expand upon these concepts in greater depth, focusing especially on the synthesis, manipulation, and application of graphene. I then describe the synthesis and application of other nanomaterials and close with a section on tips and tricks developed for fabrication and testing.

In chapter 2, I explain how graphene's optical and electronic properties inspired a new type of solar cell design called "screening-engineered field-effect photovoltaics" (SFPV). The SFPV concept uses a partially screening electrode to allow an applied electric field to tune the carrier density and type of a semiconductor, accomplishing the same effect as chemical doping in a manner that is compatible with any semiconductor. SFPV designs for graphene (2D) and nanowire (1D) partially-screening electrodes will be discussed, along with ways to sustain the applied electric field internally.

Chapter 3 covers graphene theory, synthesis (by chemical vapor deposition, or CVD), characterization, and manipulation. I discuss optimization of synthesis methods and an ultraclean graphene transfer process, which together have paved the way for in-depth fundamental studies of CVD graphene properties. This chapter also includes discussion on our discovery and studies of several graphene nanostructures: grafold, graphene sandwiches/veils, and "graphritos."

In chapter 4, I discuss electronic devices made with CVD graphene: field-effect

transistors (FETs), p-n junctions, nanoribbons, and grafold FETs. Our studies of graphene FETs reveal that the graphene substrate is a dominant source of scattering for CVD graphene, and the use of hBN as opposed to SiO_2 is sufficient to attain very high mobilities (enough to explore much of the rich physics of 2DEGs) for present-day CVD graphene. The graphene p-n junctions also make us of substrate effects, particularly the difference in doping seen on hBN and SiO_2 subtrates. Likewise, our studies of nanoribbons make use of the excellent properties of boron nitride (in this case, boron nitride nanotubes or BNNT).

Chapter 5 summarizes other nanomaterial synthesis methods and related projects completed and in progress. Materials include MgB_2, carbon nanotubes (CNT), graphene (exfoliation, additional CVD methods using thin catalyst films), chalcogenides (GaSe and SnS), and copper oxide (Cu_2O).

In the appendix (chapter A), I record several tips and tricks of fabrication and device measurement which I hope will save future group members time and frustration.

Chapter 2

Screening-engineered field-effect photovoltaics

2.1 Background, promise, and challenges

Global electricity demand is presently around 17,000 TWh per year. Incident sunlight bombards the earth with over 8,000 times this much power. Not surprisingly, photovoltaic energy conversion is expected to play a major role in fulfilling our future energy needs. However, present technologies cannot harvest this power in a sufficiently cost-effective way, due to a combination of raw material and processing costs [79, 103].

2.1.1 Structure of an inorganic solar cell

A schematic of a typical inorganic solar cell and a corresponding band diagram are shown in figure 2.1. The base is a singly-doped semiconductor, and the emitter is a thinner, oppositely-doped semiconductor. Light is absorbed (and excitons are created) primarily in the thicker base region. The excitons are weakly bound (Mott-Wannier excitons) and dissociate easily into holes and electrons at room temperature. These freed carriers then diffuse and drift to regions where they are majority carriers, pushed by the internal electric field set up by the p-n junction. Once the photoexcited carriers become majority carriers, recombination is much less likely, and they can be extracted by the metal contacts.

2.1.2 Challenges in p-n junction formation

Commercial-scale production of inorganic solar cells[1] has so far relied on a limited subset of semiconductors which can be divided into two distinct classes, (1) materials

[1]Dye-sensitized and organic photovoltaics, so-called excitonic solar cells due to the strong exciton binding (Frenkel excitons) relative to the weak exciton binding (Mott-Wannier excitons) in most inorganic p-n junction cells, will not be discussed in this work.

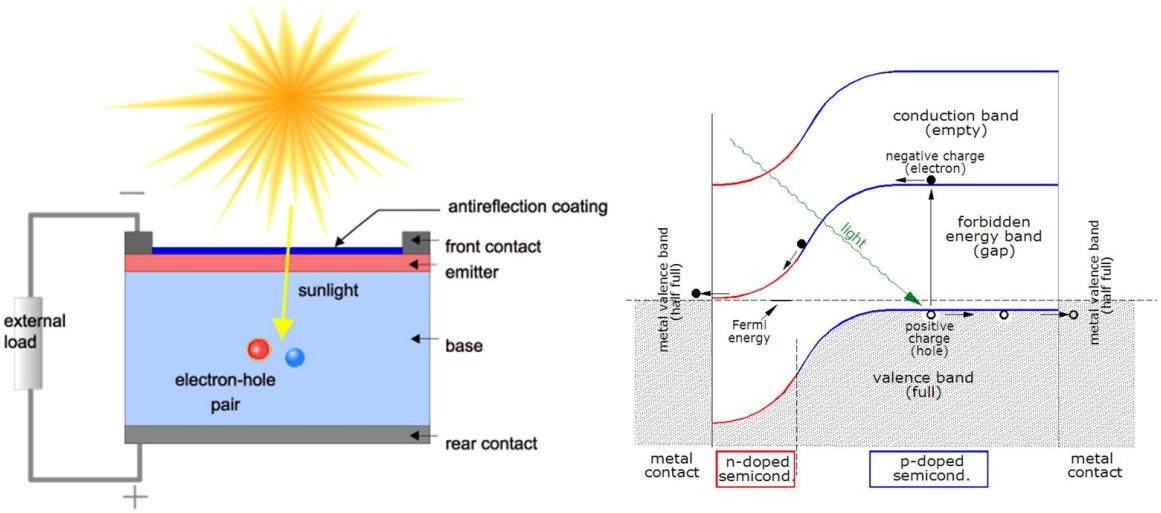

Figure 2.1: A typical inorganic solar cell (left, source: pvcdrom.pveducation.org) and corresponding band diagram (right, source: wikipedia.org). Light is absorbed and creates excitons in the thick base material, which is p-doped in this example. Excitons dissociate into electrons and holes easily; these charge carriers feel the electric field created by the p-n junction and drift into regions where they are majority carriers, where they are then extracted at the metal contacts.

that can be easily doped (Si, GaAs, InP) and (2) materials that make reasonable p-n heterojunctions, such as p-type CdTe or CIGS heterojunctions with n-type CdS.

However, there are many other semiconductors with bandgaps that sit near the peak of the Shockley-Queisser efficiency limit curve [87]. Many of these high-efficiency potential materials are also extremely abundant and affordable (metal oxides, phosphides, sulfides, etc), as shown in table 2.1, but most cannot be doped or form poor heterojunctions [100].

2.1.3 Gating with an electric field

In the absence of ways to dope or form good heterojunctions with the earth-abundant semiconductors, it may seem that these materials can never be used for low-cost, high-efficiency photovoltaics. However, there are other methods besides doping to tune or even invert the carrier concentration in semiconductors, namely applying an electric field by gating as is commonly done in metal-oxide-semiconductor field-effect transistors (MOSFETs). One might imagine that this gating strategy could entirely displace the need for doping, allowing local inversion of a p-type semiconductor into a n-type semiconductor. Indeed, the use of effective gating in photovoltaics is a several decades old strategy, begining with metal-insulator-semiconductor (MIS) solar cells, in which a thin insulating layer is used to block recombination current. MIS cells

Material	Annual production potential (TWh)	Efficiency limit (%)
CIGS	5,000	33
CdTe	60	32
FeS_2	500,000,000	30
CuO	10,000,000	26
Cu_2S	10,000,000	33
Zn_3P_2	9,000,000	31
Bi_2S_3	4,000	33

Table 2.1: Abundance and efficiency limits of non-silicon semiconductors. Current heterojunction fabrication techniques limit industry to using only CIGS and CdTe. Many of the more abundant materials (FeS_2 especially) cannot be doped and form poor heterojunctions [100].

employ fixed, uncompensated charges within a dielectric coating (often Cs^+ in Si_3N_4) to increase the semiconductor band bending at the MIS interface. These cells have achieved high efficiencies [40, 106, 107] but have notoriously short operating lifetimes due to the instability of surface states under illumination [37]. Implementation of direct gate "doping," where a metal-insulator gate is used to invert a region of semiconductor [27, 32, 106, 107] is limited by screening of the gate near the top contact, as illustrated in figure 2.2. These gating methods must rely on strategies such as doping under the top contacts [27, 32] or the formation of a large Schottky barrier at the top contacts [40, 106, 107], both of which are incompatible with the earth-abundant semiconductors discussed above. Some success has been achieved with low density-of-states Schottky contacts [66, 98, 99], but such approaches will not necessarily work for any semiconductor.

2.2 Screening-engineering for effective gating

The core challenge in achieving effective gate-induced doping (without relying on chemical doping or large intrinsic Schottky barriers) is that the electrode beneath the gate must simultaneously conduct well (to be an effective and low series resistance contact) but also have few enough charge carriers that the charge induced by the gate field is shared between the contact and the underlying semiconductor. Graphene, a single-atom thick sheet of hexagonally-bonded carbon (as will be discussed in detail in the following chapters), satisfies these two seemingly contradictory requirements. Graphene has very few charge carriers near its neutrally doped state, but has a remarkably low sheet resistance of 500Ω/□–1kΩ/□; in addition, monolayer graphene is fairly transmittive, only absorbing $\pi\alpha \sim 2.3\%$ of visible light [22, 71]. Thus, when gating a monolayer graphene contact on a semiconductor (as seen in figure 2.3), the induced charge can be shared between the graphene and semiconductor. The resulting

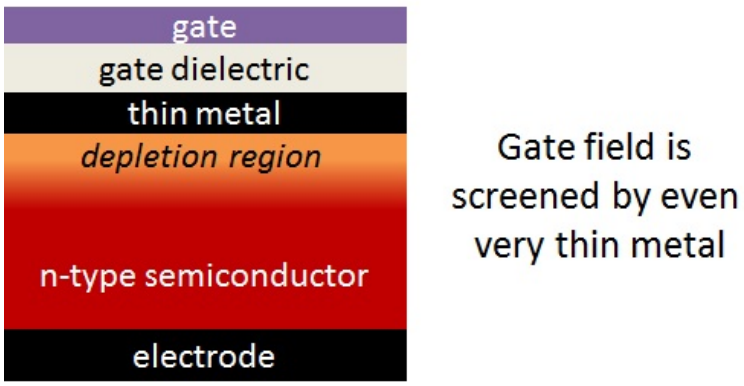

Figure 2.2: This schematic illustrates the challenge of using an applied electric field to tune a Schottky barrier solar cell. For any practical top electrode, the applied gate field will be screened, preventing effective carrier modulation in the semiconductor.

cell is hereafter referred to as a screening-engineered field-effect photovoltaic (SFPV) cell. Much of the remaining work in this chapter was done in collaboration with Steven Byrnes of Professor Feng Wang's group at UC Berkeley, along with assistance from Will Gannett, Onur Ergen, and Dr. Oscar Vazquez-Mena of the Zettl group. Steven performed all theoretical calculations, and additional information on these calculations can be found in his PhD thesis, currently in preparation. Several of the following sections also contain information found in our recent *Nano Letters* article [82].

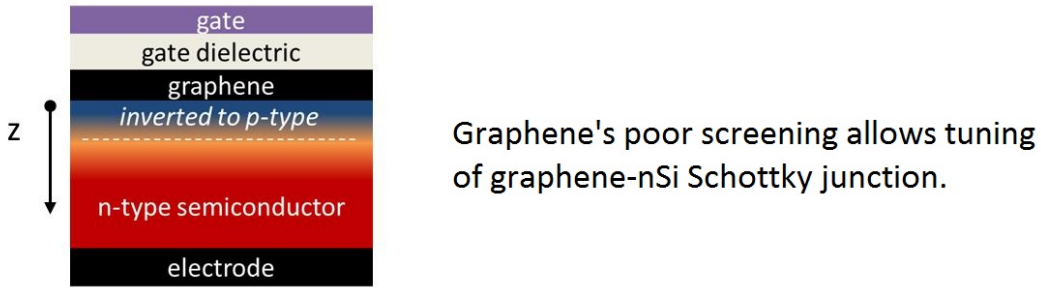

Figure 2.3: Screening-engineered field-effect photovoltaic (SFPV) cell using a graphene top contact. Graphene allows simultaneous contact to and carrier modulation (with an applied electric field) of the underlying semiconductor.

This first instance of a SFPV cell requires an ultrathin contact. As more graphene layers are added to decrease sheet resistance, the tunability of the junction is diminished; when the monolayer graphene layer in contact with the semiconductor no longer shares any of the induced charge, the semiconductor can no longer be influenced by

the gate field. As previously mentioned, metals are incompatible with this technique due to their high charge carrier concentrations and extremely short Debye screening lengths. However, other contact materials – semimetals and light- to medium-doped semiconductors – may allow penetration of the gate field. However, for optimal device performance, these materials must also have very low sheet resistances. In order to extend the SFPV structure to arbitrary materials, we need to consider dimensional confinement in directions *other* than out of plane (ultrathin).

So far, we have only constrained the contact material in the z direction (perpendicular to the plane of the semiconductor surface), which leaves us to consider the x and y in-plane dimensions. If we suffiently confine top contacts in either the x or y direction, one might expect that an applied gate field could exert some influence on the contact-semiconductor junction. As will be shown in the following section, confining the top contact dimension to be smaller than the bulk depletion width in the semiconductor allows the gate field to influence the contact-semiconductor junction, reminiscent of the action of a wave passing around a sub-wavelength obstruction. In this instance, the confined top contact may be composed of any material (even metals); a schematic is shown in figure 2.4.

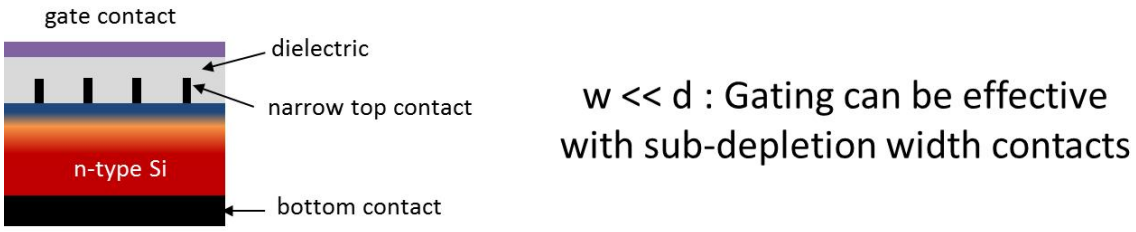

Figure 2.4: SFPV using a "nanofinger" top contact (with a width less than the bulk depletion width of the semiconductor)

In the following section, we will consider both of these types of SFPV cell (both ultrathin and ultranarrow top contacts) theoretically and experimentally using Si as a prototypical semiconductor.

2.3 SFPV based on silicon Schottky junctions

To investigate the challenge of simultaneous electric contact to and carrier modulation of a semiconductor (using Si as a test case) via an applied electric field, we (1) solved a system of coupled equations using Matlab to simulate ultrathin (graphene) contact SFPV and (2) performed finite element simulations in COMSOL to simulate ultranarrow contact SFPV. For these test cases, we start by forming a Schottky junction solar cell (an alternative to the standard p-n junction), as the cells are relatively simple to both model and fabricate. A Schottky junction is formed between a metal

contact and a singly-doped semiconductor. As shown in figure 2.5, a large difference between the metal work function and the semiconductor's Fermi level causes charge transfer at the metal-semiconductor (MS) interface, forming a depletion layer and setting up an electric field to drive the drift current. Unfortunately, intrinsic Schottky junctions cannot produce open circuit voltages larger than half the semiconductor bandgap, and the MS interface has a very large recombination velocity. MIS cells solve these problems by introducing a tunnel insulator between the metal and semiconductor. The SFPV approach may solve these problems in a different way, by adding a potential barrier that increases open circuit voltage and reduces the recombination velocity.

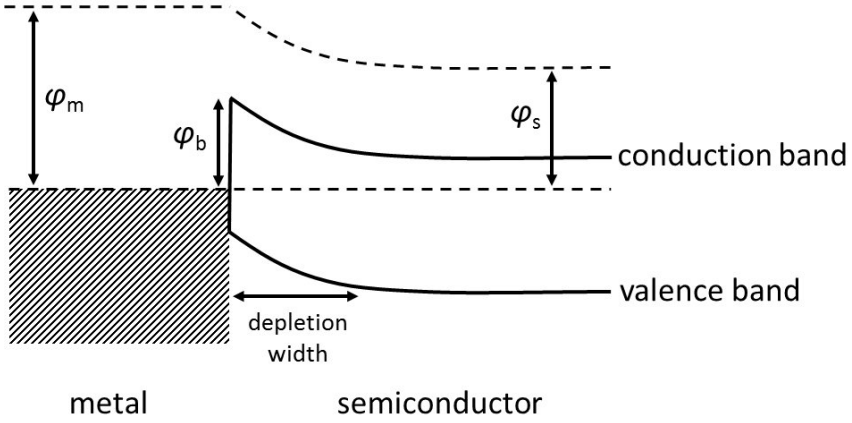

Figure 2.5: Schottky junction band diagram for a metal contact to a n-type semiconductor. The differences in semiconductor and metal work function (ϕ_s and ϕ_m) result in charge transfer and band bending at the MS interface.

2.3.1 Ultrathin contact (graphene) SFPV

Graphene is an attractive choice for an ultrathin SFPV top electrode. It is very transparent yet reasonably conductive as mentioned above, makes Schottky contact to both n- and p-type Si [16, 62], and allows electric fields to effectively partially penetrate it and influence underlying semiconductors, thus allowing for simultaneous gate-induced carrier modulation, electrical contact, and light tranmission. To simulate graphene top contact SFPV, we solve the following system of coupled equations:

1. $Q_{gr}/A = D_{gate} - D_{surf}$
2. $\chi_{gr} = \chi_{cnp-gr} + \hbar v_F |Q_{gr}/q|^{1/2} \text{sign}(Q_{gr})$
3. Satisfy the drift-diffusion-Poisson equations in the Si, where χ_{gr}'s effect on the boundary affects D_{surf}.

Here Q_{gr} is the graphene charge, D_{gate} and D_{surf} are the D-fields in the gate and at the surface of the silicon, and χ_{gr} and χ_{cnp-gr} are the work function of the graphene modified by the gating and at the charge neutral point, respectively. The work function of the graphene (determined by the charge in the graphene via the graphene density of states) determines the Schottky barrier height (via the Schottky-Mott equation). The charge in the graphene is determined by the charge in the gate and semiconductor space-charge region (these three must sum to zero). The Schottky barrier height, applied voltage, and gate voltage determine the total charge in the semiconductor space-charge region. When these equations are solved self-consistently, one is able to determine the effective Schottky barrier height as a function of applied gate voltage. Using the Schottky-Richardson equation, one is able to determine the current as a function of gate voltage (and thus the photovoltaic performance). χ_{cnp-gr} is approximated as 4.6 eV [108]. Other parameters for the simulation were silicon type and doping (n-type, $N_D \sim 1.1 \times 10^{16}$ e^-/cm^3), electron and hole carrier mobility lifetimes of 100 µs, and crystalline silicon properties obtained from Sze's *Physics of Semiconductor Devices* [95]. Bilayer graphene is treated similarly, as two monolayer graphene sheets with their own separate work functions. Multi-layer graphene is treated as the limit of infinitely many sheets. These simulations ignore certain parameters such as the limiting effects of sheet resistance (important for thinner graphene contacts) and transparency (an issue for very thick graphene contacts), as significant strides are being made by many other research groups to optimize graphene as a transparent electrode [67, 86, 96, 113].

Results of these simulations (performed in Mathematica) are shown below. Figures 2.6 and 2.7 show the Si potential profile (for saturated gate, indicated by the dashed line in figure 2.7) and the Schottky barrier height as a function of gate charge (Q_{gate}). Limiting efficiencies as a function of gate charge are shown in figure 2.8.

As seen in figure 2.8, monolayer graphene performs quite well, achieving limiting efficiencies of up to $\sim 19\%$, as it permits the most field penetration. In realistic cells, the high series resistance of the monolayer graphene would have to be mitigated with additional metal busbars or by heavy graphene doping, though the large gate field effectively puts graphene into a highly-doped regime.

Having demonstrated high performance theoretically, we then fabricate and test experimental prototypes. We start by growing chemical vapor deposited graphene, as discussed later in chapters 3 and 4. Monolayer graphene is transferred from its Cu growth substrate to n-type Si ($N_D \sim 10^{16}$ e^-/cm^3), with a total active cell area of about 0.04 cm^2, large enough to neglect the added active area due to the large ($\sim$100 µm) minority carrier diffusion length in low-doped crystalline Si. The graphene is contacted with evaporated Cr/Au, and bottom contact to the Si is made by thermally evaporating Al. A gate is applied using 1-ethyl-3-methylimidazolium bis (trifluoromethylsulfonyl)imide ionic liquid (EMI-BTI, Sigma Aldrich No. 11291). Current-voltage curves as a function of gate voltage (V_g) are seen in figure 2.9, with an inset showing a picture of the device. The graphene was held at ground and a bias

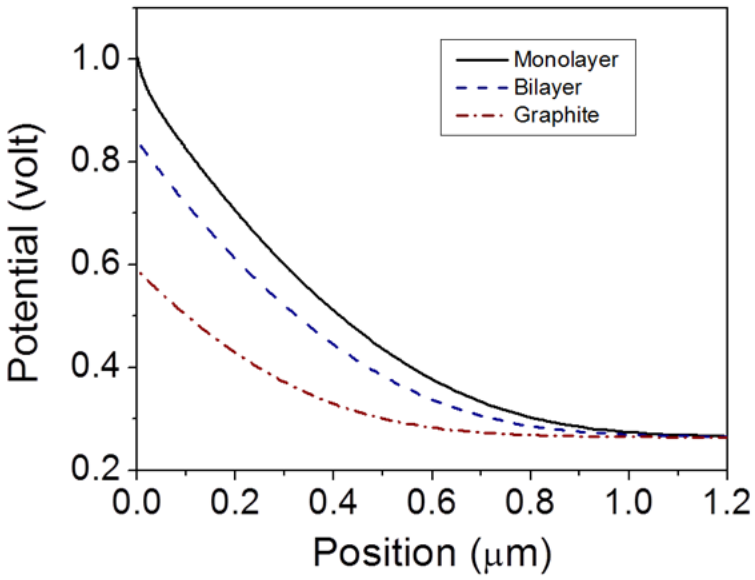

Figure 2.6: Potential in Si with saturated gate ($Q_{gate} \sim 1.5 \times 10^{13}$ e^-/cm^2) for monolayer, bilayer, and multi-layer graphene.

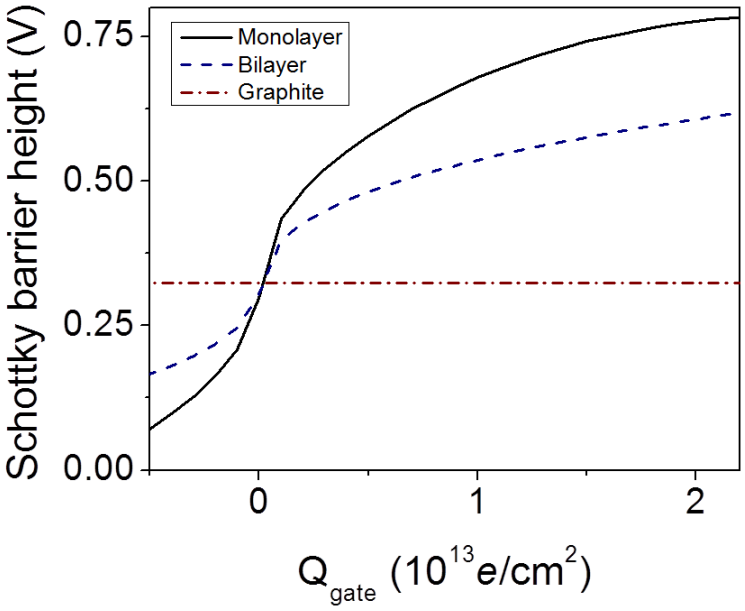

Figure 2.7: Schottky barrier height versus Q_{gate} for monolayer, bilayer, and multi-layer graphene.

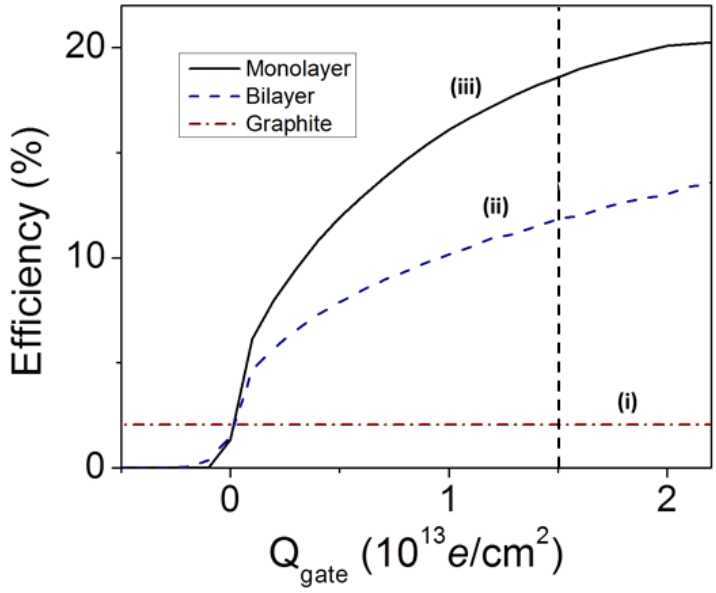

Figure 2.8: Efficiency versus Q_{gate} for monolayer, bilayer, and multi-layer graphene. The dashed line at $Q_{gate} \sim 1.5 \times 10^{13}\ e^-/cm^2$ shows the gating used in figure 2.6. (from [82])

voltage (applied to the bottom electrode) was swept while the gate is held at a fixed voltage. Details of the measurement process and testing apparatus are found in the appendix (A.1).

Negative gate voltage repels electrons and attracts holes to the top of the n-type Si and graphene, notably enhancing V_{OC}, short circuit current (I_{SC}), and fill factor (FF). With the application of a modest gate voltage (which consumes negligible power due to the $\sim$ nA gate leak current) of $V_g = 1.2$ V, power conversion efficiency (PCE) increases from $\sim 1.5\%$ to $\sim 1.8\%$. A variety of factors are likely keeping us far from the efficiency limits predicted by theory, including the high graphene series resistance, gate transparency, and the lack of an antireflection coating or surface texturing. To investigate the performance of graphene "bilayers," we transferred another graphene monolayer onto the existing monolayer graphene on silicon cell. Again, we applied a gate with an ionic liquid, and current-voltage curves as a function of gate voltage (labels) are shown below in figure 2.10.

For the bilayer cell, performance increases with increasingly negative V_g, as seen for the monolayer. However, V_{OC} and the ultimate performance of the cell are consistently lower than that seen for the monolayer case; this may be due to the shielding of the gate electric field by folds introduced during transfer of the second monolayer. The effectiveness of the gating quickly diminishes with increasing graphene layers. Since the performance of many-layer graphene on Si has already been extensively

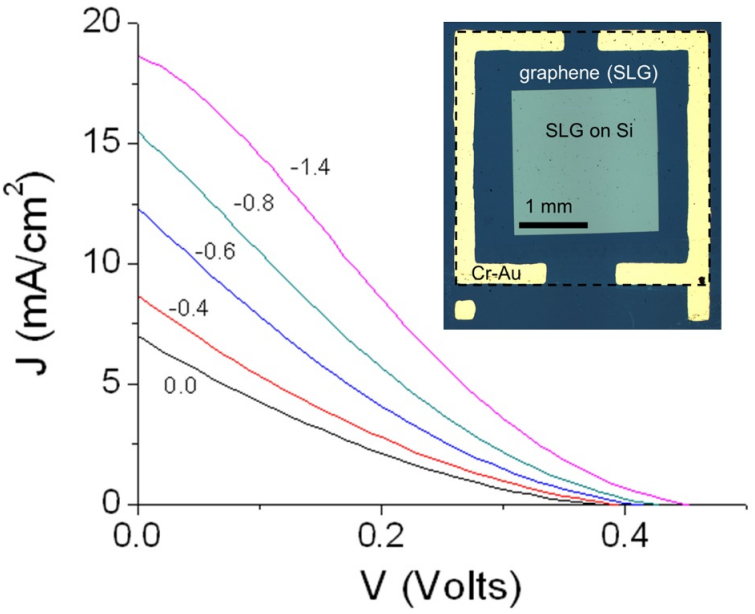

Figure 2.9: Current-voltage curves versus gate voltage for monolayer graphene silicon SFPV cell (AM1.5), with an inset showing an optical micrograph of the cell. (from [82])

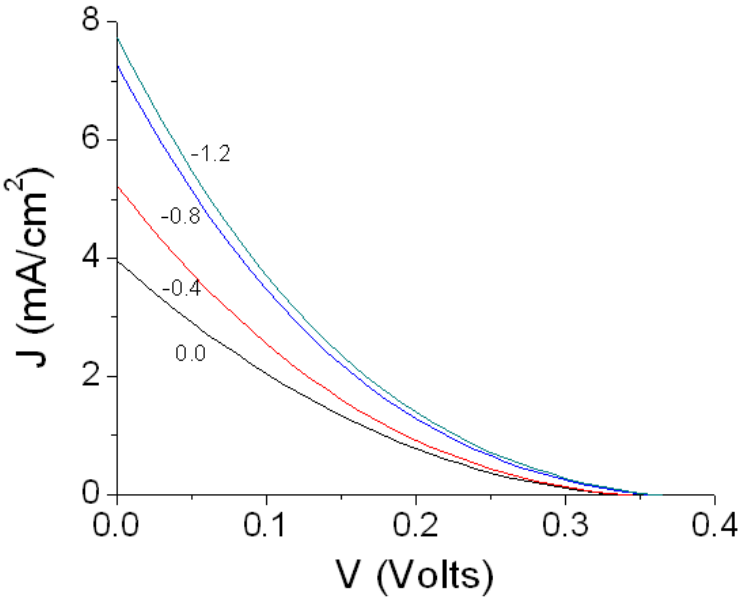

Figure 2.10: Bilayer graphene SFPV cell performance as a function of gate voltage (AM1.5). (from [82])

studied in the literature [62], we did not repeat the test with thicker graphene using additional transferred monolayers.

These results show that graphene can serve as an effective ultrathin SFPV contact. No known metals would be compatible with this ultrathin geometry, as the screening length is significantly shorter than the minimum viable thickness for a continuous metal sheet. Low-doped semiconductors may be compatible with this approach, though it may be challenging to simultaneously achieve low carrier concentration and low sheet resistance.

We will now consider additional contact confinement strategies that are compatible with a wide range of contact materials, not just graphene and low-doped semiconductors but high carrier concentration materials such as metals.

2.3.2 Nanofinger SFPV: ohmic and Schottky contacts

Graphene is not an ideal rectifying contact for many semiconductors, so it would be beneficial to have strategies to use other materials (metals, highly-doped semiconductors, etc) for SFPV cells. By constraining at least one of the in-plane dimensions of the top contact, this is in fact possible for arbitrary contact materials.

To theoretically consider the performance of these "nanofinger" SFPV cells, we performed finite-element simulations in COMSOL to solve the drift-diffusion-Poisson equations. The simulations are two dimensional (extruding nanofingers infinitely into the third dimension) and have periodic boundary conditions (assuming equally-spaced nanofingers). The Poisson equation is satisfied in the semiconductor and gate dielectric, and the top, bottom, and gate metal contacts define the boundary conditions. The Crowell-Sze model is used to determine majority carrier transport at the metal-semiconductor Schottky barriers [23], and image-force lowering of the barrier is modeled by self-consistently modifying the contact work function based on the local electric field [95]. To simplify simulations, recombination at the bottom contact is set to zero (assuming passivation with a back-surface field). AM1.5 illumination was used, and the silicon absorption coefficient was set at $\alpha = 3 \times 10^3/\text{cm}$. As in the graphene simulations, carrier lifetimes were set at 100 µs (assuming only Shockley-Read-Hall recombination). Other material properties used include the following: silicon type (n), carrier density $N_D = 10^{15}\ e^-/\text{cm}^3$, wafer thickness D = 10 µm, and depletion width d = 1 µm (determined by N_D); gate dielectric properties (thickness t = 100nm and dielectric constant $\kappa = 3.9$); and contact properties (work function ϕ (4.45 eV for ohmic and 4.8 eV for Schottky contacts), width w, and center-to center separation s). We only consider silicon Schottky contacts, and there is room for considerable exploration with other cell types such as MIS, semiconductor-insulator-semiconductor (SIS), and perhaps even partially chemically-doped cells, as will be discussed near the end of this chapter.

Results of our simulations of nanofinger SFPV are seen in figure 2.11, with planar ($w = \infty$), w = 400 nm, and w = 100 nm wide ohmic (i-iii) and Schottky (iv-vi)

contacts to the n-type Si.

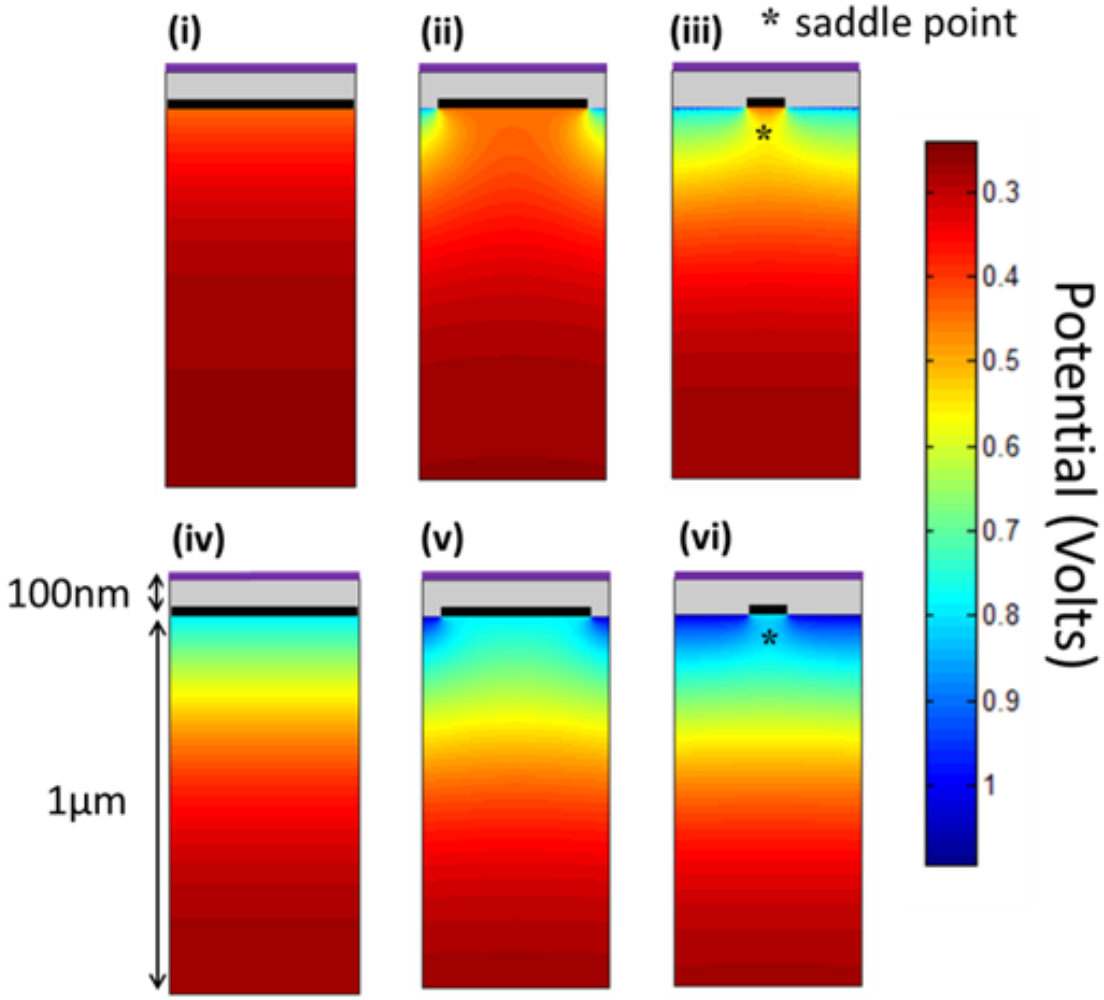

Figure 2.11: Simulated potential plots for ohmic and Schottky nanofinger SFPV. (from [82])

In the simulation, fingers are held at ground and the gate is fixed at a large negative voltage (-10 V), which is sufficient to saturate the effect and make the choice of gate metal work function arbitrary. As expected, wide fingers (i,iv) screen out the effect of the gate completely, but sufficiently narrow fingers (iii,vi) permit the formation of an added potential barrier underneath the electrode. Majority carriers are blocked by this added barrier and are forced to flow around to the strongly-gated sides of the contact. Thus, this added barrier can increase the effective Schottky barrier height, lowering the diode saturation current and improving open circuit voltages and efficiencies. Corresponding current-voltage curves for these six cells are seen in figure 2.12.

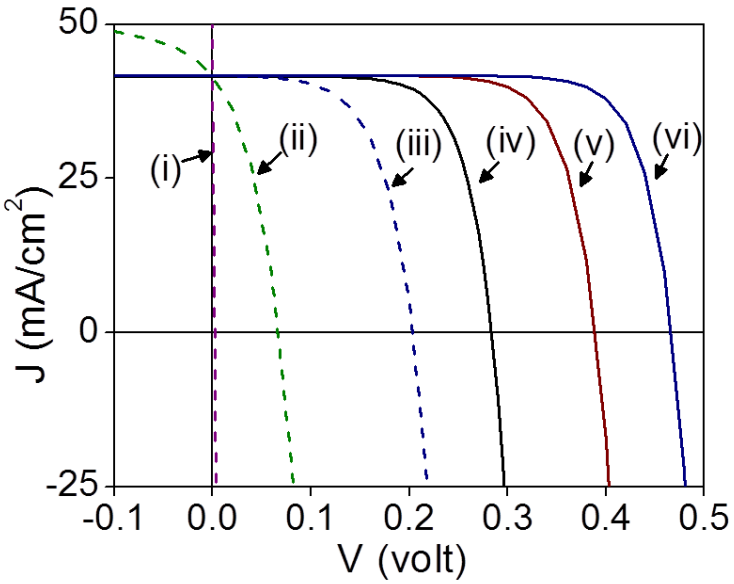

Figure 2.12: Current-voltage curves for the ohmic and Schottky SFPV devices in figure 2.11. (from [82])

We repeated these simulations for a range of finger widths, from planar down to w = 10 nm, and plotted the open circuit voltages and efficiencies in figure 2.13.

The observed performance increases greatly exceed that expected by simply reducing contact areas (which reduces recombination current) [39]. Effective gating is seen for finger widths well below the bulk semiconductor depletion width (in this case, d = 1 µm), which is as one might expect since d is the distance over which potentials can vary in the semiconductor. Forward bias and the intrinsic Schottky barrier height are also important factors influencing the resulting added potential barrier formation. We see that, given suffiently narrow fingers, the effect is strong enough to form a large potential barrier below ohmic contacts, raising efficiencies from 0% up to about 8% for w = 10 nm.

Finally, we also consider the effect of finger separation (s). The above results were obtained for s = 10 µm, as this seemed to be a realistic middle ground for balancing light transmission and sheet resistance. Using a fixed finger width w = 100nm, we simulated the effect of a changing finger spacing s, and resulting efficiencies and open circuit voltages are shown in figure 2.14.

Decreasing the spacing increases saturation current and shading but also decreases series resistance. Since we don't consider shading or series resistance in these simulations, only the effect of changing saturation current is seen, with larger spacing resulting in higher performance.

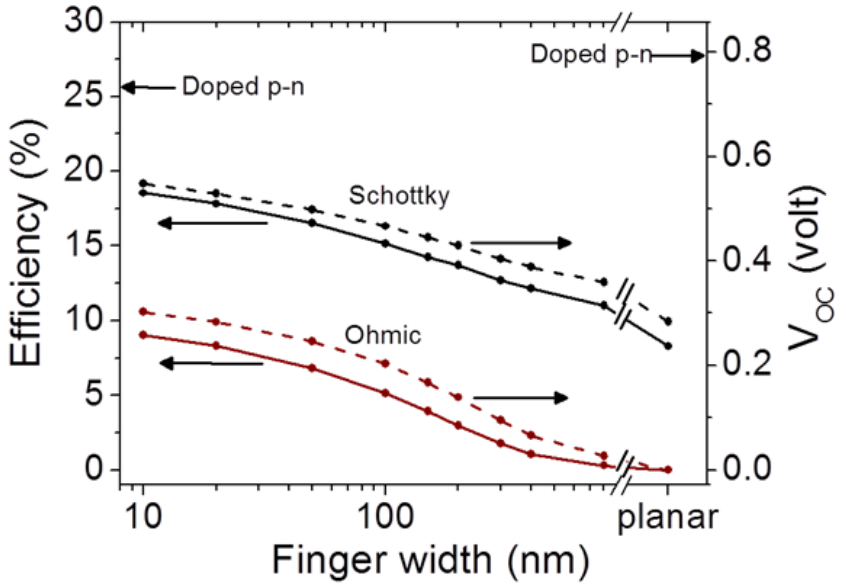

Figure 2.13: Maximum efficiency and V_{OC} for ohmic and Schottky nanofinger SFPV. (from [82])

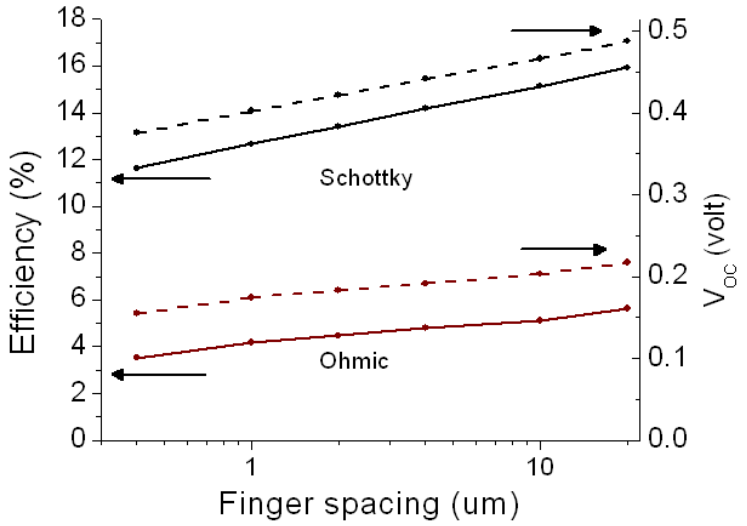

Figure 2.14: Effect of finger spacing on SFPV performance (finger width fixed at 100nm). (from [82])

Experimental nanofinger silicon SFPV using ohmic contacts

To validate these models, we next fabricated and tested experimental prototypes. First, to isolate the SFPV effect from improvements due to better surface passivation,

we fabricate silicon SFPV cells with intrinsically ohmic (annealed Al) 250 nm wide contacts to p-type ($N_A \sim 1 \times 10^{16}/cm^3$), with a similar w/d ratio to the device seen in part ii of figure 2.11. The finger spacing is set at 5 µm, which (as we have shown) should not greatly diminish performance. An optical image of the resulting cell is shown in figure 2.15. Gating is achieved with 150 nm of electron-beam evaporated SiO_2 and a ∼40% transparent Cr/Au gate contact. Current-voltage plots as a function of gate voltage (V_g) are shown in figure 2.16 (AM1.5 illumination).

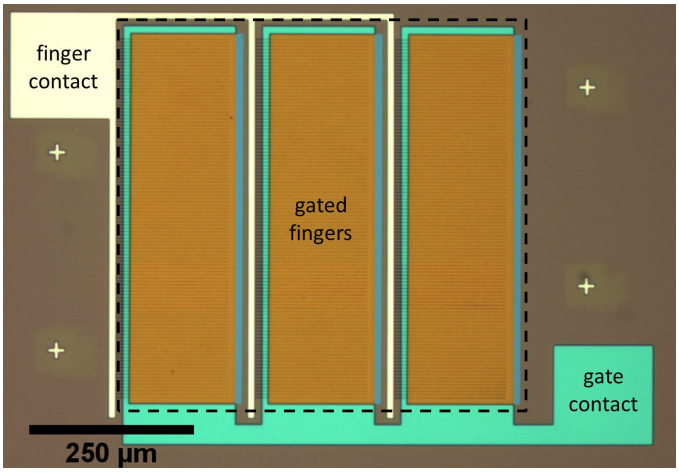

Figure 2.15: Optical micrograph of (ohmic) Al nanofinger silicon SFPV cell. The active area is outlined with a dashed line. (Note: This device has an ITO top gate, not Cr/Au as tested for figure 2.16.)

As we did previously with graphene SFPV cells, the partially-screening contact is fixed at ground while bias voltage on the bottom contact is varied. Positive gating repels holes and attracts electrons to the top of the p-type Si, causing inversion between fingers and eventually adding an extra potential barrier underneath the contacts. The initially ohmic behavior (a straight IV curve through the origin) is tuned into a slightly Schottky contact, and open circuit voltage (V_{OC}), short circuit current (I_{SC}), fill factor (FF), and shunt resistance (R_{shunt}) increase monotonically with stronger gating. PCE increases from 0% to ∼ 1.4% (with V_{OC} ∼0.09 V) with V_g = 3.2 V, near our model's predictions. We should note that this cell is far from optimized, and performance may be improve through better gate transparency and thickness, dielectric quality, antireflection coatings, and surface texturing. The gate field requires minimal power to maintain (several orders of magnitude below the cell's generated power), as the gate contact draws only 6 nA at the highest applied V_g. We note that this particular cell area was rather small (600 µm × 600 µm), so a 100 µm carrier diffusion length may reduce real cell efficiencies by up a multiplicative factor of 0.56. However, regardless of this correction, the SFPV effect is still shown to be distinct from surface passivation.

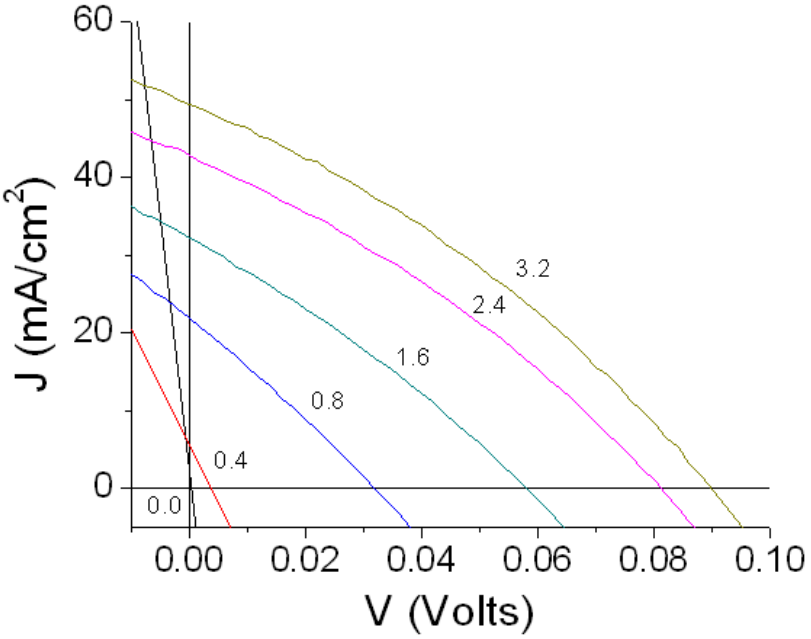

Figure 2.16: Current-voltage curves for ohmic nanowire SFPV (AM1.5) (from [82])

Of course, as our model suggests, we can expect to attain much higher cell efficiencies by starting with Schottky contacts.

Experimental nanofinger silicon SFPV using Schottky contacts

We repeated the fabrication steps above using Schottky contact (Cr) to the p-type silicon ($N_A \sim 3 \times 10^{15}/cm^3$). For these cells, w = 300 nm (similar to part v of figure 2.11) and the cell area was 200 µm × 200 µm. All other parameters were identical to the ohmic silicon SFPV cells in the previous section. Current-voltage curves for positive gating are shown in figure 2.17. Again, the nanofinger is fixed at ground, the gate is fixed at various voltages, and bias voltage on the bottom contact is swept for each fixed gate voltage. As with the ohmic case, positive gating causes inversion between fingers and adds an extra potential barrier underneath the contacts, improving V_{OC}, I_{SC}, FF, and efficiency.

In the positive gating regime, efficiency for these cells is increased from $\sim$ 0.7% (V_g =0.0 V) to $\sim$ 9% (V_g =2.8 V). The small area may reduce the efficiency by a factor of 4 (given L_e $\sim$100 µm).

Just as an ohmic contact can be made rectifying, a Schottky contact may be made ohmic. We demonstrate this by gating the Schottky SFPV device with a negative voltage, thus attracting holes and repelling electrons from the top of the semiconductor. As seen in figure 2.18, a sufficiently negative gate voltage is able to shrink the

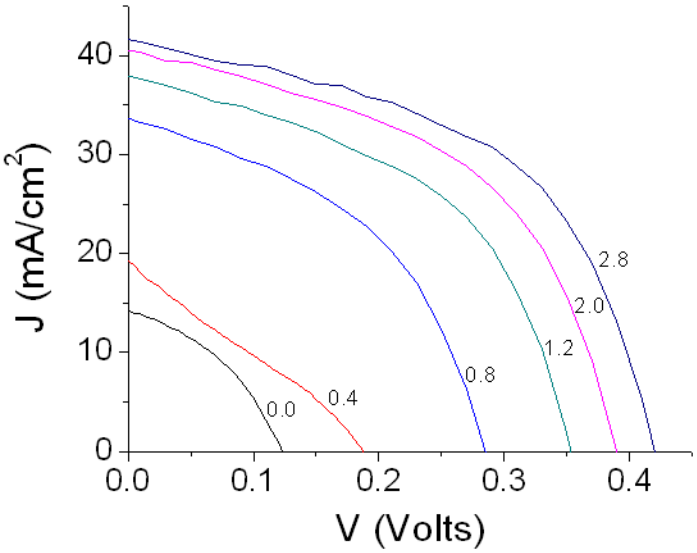

Figure 2.17: Current-voltage curves for Schottky nanowire SFPV: positive gating (AM1.5 illumination). (from [82])

depletion region to the point at which there is effectively no barrier. This flexibility may offer some interesting opportunities for improving non-ideal ohmic contacts.

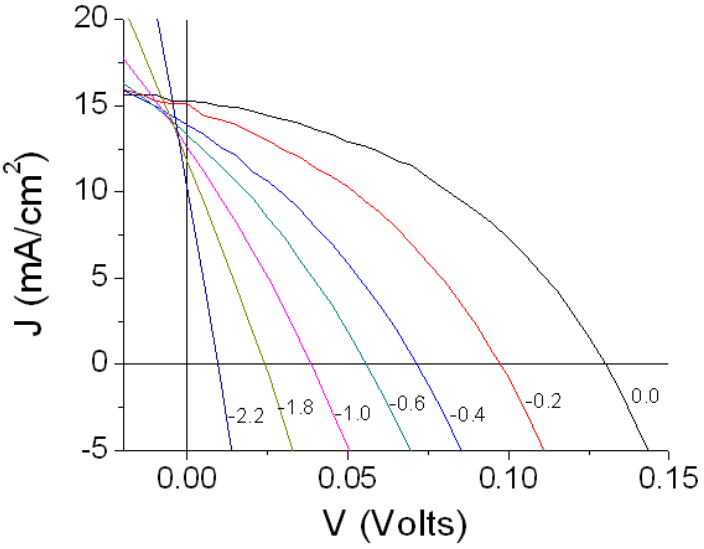

Figure 2.18: Current-voltage curves for Schottky nanowire SFPV: negative gating (AM1.5 illumination) (from [82])

So far we have shown the versatility of the SFPV design, with multiple possible geometries (ultrathin or ultranarrow contacts) and tuning strategies (ohmic to Schottky, Schottky to more Schottky, Schottky to ohmic, and high resistance ohmic to low resistance ohmic). Additionally, we have shown that the power consumed by the gate will be negligible compared to generated photovoltaic power. However, practical (commercial) photovoltaic devices require simplicity and low cost, and adding a third, powered electrode may seem like a recipe for disaster. In the next section, we will discuss how we solved this problem and effectively removed the need for an isolated, third electrode.

2.4 Self-contained gating for practical SFPV cells

The SFPV gate electrode introduces a few complications. For one thing, the need for external batteries will increase the cost and complexity (without even considering increased failure rates for panels as batteries die) of cells and panels. Furthermore, modules are typically made by connecting many cells in series; this would mean that local grounds would increase for every cell in the string, and gate voltages must track these grounds appropriately. Fortunately, we devised a simple way to power this third electrode internally and in a way which tracks the local ground.

Self-gating feedback loop

If we connect the cell output directly to the gate, the gate can be self-powered and have an appropriately floated ground. The power drawn by the gate is negligibly small compared to the photo-generated power, and the typical operating voltage of a Schottky or heterojunction cell (0.1–1 V) can be sufficient to produce an impactful gate field. Self-gating thus sets up a feedback loop, which increases the cell operating voltage from the intrinsic heterojunction operating voltage to a higher level, given careful choices of gate metal, gate dielectric material and thickness, and porous top electrode (which forms an initially Schottky or heterojunction contact). To model this self-gating effect, we repeated our previous simulations using a thin gate dielectric and appropriately chosen gate metal (with work function outside of the band gap). As shown in figure 2.19, given careful choices of gate contact and dielectric, self-gating can achieve nearly the same efficiencies as those achieved with a saturated, externally-powered gate.

We experimentally demonstrated self-gating using a SFPV cell with with 250 nm wide Schottky (Cr) contacts to $N_A \sim 3 \times 10^{15}\ e^-/\mathrm{cm}^3$ p-type Si and an EMI-BTI ionic liquid gate. Figure 2.20 shows V_{OC} versus time while the gate is toggled between ground and the cell output; illumination is AM1.5. We see a significant and reversible increase of about 30% in V_{OC} over the non-gated Schottky barrier configuration and a ∼60% increase in photoconversion efficiency.

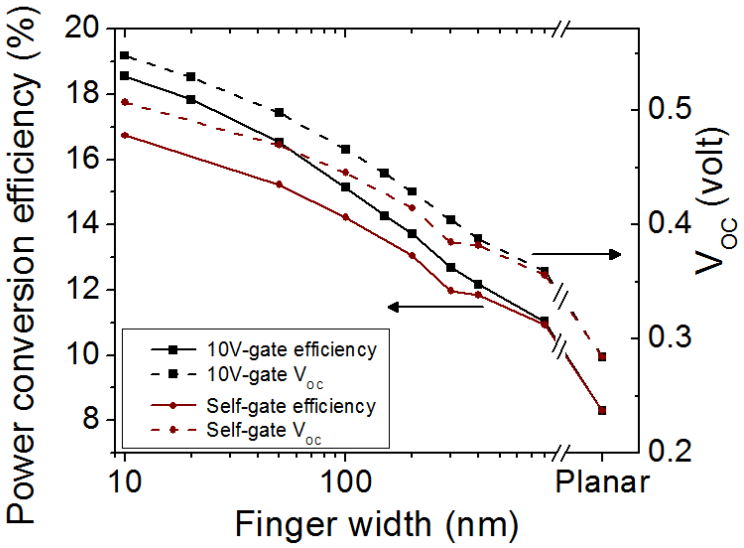

Figure 2.19: Simulation of self-gating performance versus finger width for Schottky SFPV (from [82])

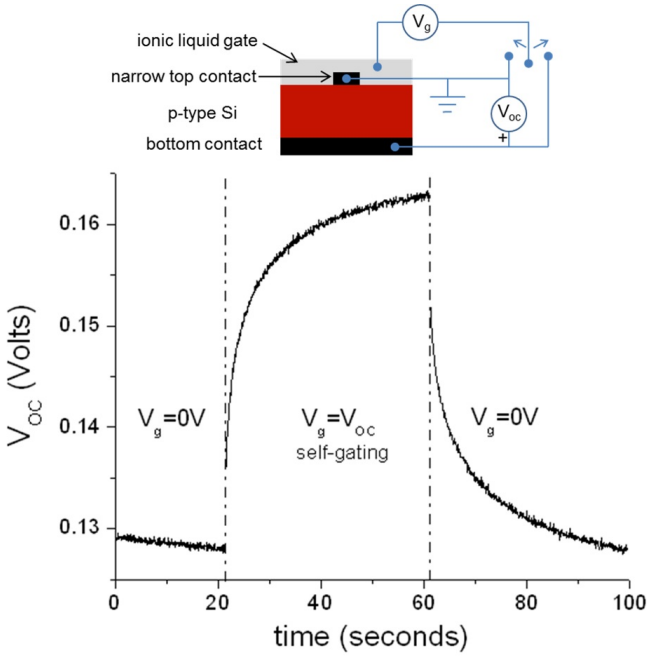

Figure 2.20: Experimental demonstration of self-gating feedback loop. After toggling the gate to V_{OC}, V_{OC} increases significantly. (AM1.5 illumination) (from [82])

Additionally, this gating may also be achieved through the use of dielectrics, electrolytes, ferroelectrics, or other materials with fixed surface charges or polarizations, as will be discussed in the following section.

Gating via fixed charge or polarization

Besides metal-dielectric gates, there are other ways to generate local electric fields. Some dielectrics can have a large fixed charge (either positive or negative) at the interface with other materials. For instance, as shown in table 2.2, Al_2O_3 deposited by atomic layer deposition (ALD) has been demonstrated to hold up to 10^{12}–$10^{13} e^-/\text{cm}^3$, sufficient to passivate highly doped Si and enough to invert medium-doped Si (10^{14}–10^{16} e^-/cm^3) [1, 85]. Additionally, materials such as ferroelectrics can be poled to have large built-in polarizations, equivalent to a very large fixed surface charge [109]. Such materials enable SFPV cells without the added complexity of a powered gate. Further, they do not require metal gate contacts, which can reduce light transmission into the cell, and are themselves transparent and can be tailored to be reasonable single-layer antireflection coatings. As such, they are likely the easiest and most commercially-viable long-term solution for implementing SFPV cells.

Si bulk doping (e^-/cm^3)	Areal charge density for inversion (e^-/cm^2)
10^{14}	3×10^{10}
10^{15}	1×10^{11}
10^{16}	3×10^{11}

Fixed charge/polarization material	Maximum areal charge density (e^-/cm^2)
Al_2O_3 (ALD)	10^{12}–10^{13} [1, 85]
Si_3N_4 (Cs-doped)	2–3$\times 10^{12}$ [26]
P(VDF-TrFE) (ferroelectric)	6 $\times 10^{13}$ (using 0.1 C/m^2) [109]

Table 2.2: Areal charge density for inversion as a function of Si bulk doping (derived using depletion widths from Mott-Schottky relation), as compared with areal fixed charge density in various dielectrics and ferroelectrics.[1, 26, 85, 109].

2.5 Criteria for promising SFPV semiconductors

The true benefit of the SFPV cell structure, in addition to avoiding the damage and cost of traditional chemical doping, is that it can be applied to virtually any semiconductor. While silicon Schottky junction SFPV cannot attain the efficiencies of doped Si photovoltaic cells, SFPV structures made with other types of silicon photovoltaics (e.g. MIS) and various heterojunctions made with other materials may be

able to perform at commercially interesting efficiency levels. In addition to semiconductor stability (for example, FeS_2 may be corrode and leach sulfuric acid (H_2SO_4) in the presence of moisture), one key criterion for useful SFPV materials is the semiconductor's bulk depletion width, as determined by its carrier concentration and dielectric constant. More heavily doped semiconductors ($> 10^{17}$ e^-/cm^3) will require stronger electric fields to achieve inversion, and at some point dielectric breakdown will occur before you can apply a sufficiently strong electric field. Additionally, heavily doped semiconductors will have smaller depletion widths, and useful widths for SFPV nanofinger contacts will become vanishingly small. Fortunately, there are still many semiconductors which have low to medium doping and are feasible for SFPV cells. Some promising semiconductors are listed below in table 2.3.

Material	Bandgap (eV)	Carrier concentration (e^-/cm^3)
Zn_3P_2	1.4–1.5 (direct)	10^{15}–10^{17} (p)
Sb_2S_3	1.7 (direct)	$\sim 10^{12}$ (n)
SnS	1.2–1.3 (direct), 1.0 (indirect)	10^{14}–10^{15} (p)
Cu_2O	2.1 (direct)	10^{13}–10^{15} (p)
CdTe	1.5 (direct)	varies (p)
CIGS	1.0–1.7 (tunable, direct)	varies (p)
CZTS	1.0–1.5 (tunable, direct)	varies (p)
amorphous Si	1.7 (direct)	varies (n,p)
crystalline Si	1.1 (indirect)	varies (n,p)
GaAs	1.42 (direct)	varies (n,p)
InP	1.35 (direct)	varies (n,p)

Table 2.3: A few candidate materials for SFPV cells. Three rough classes of materials are listed. The first group (phosphides, sulfides, oxides) represents the "new" materials that are incompatible with chemical doping and form poor heterojunctions. The second group (CdTe, CIGS, CZTS) can already form reasonably good p-n heterojunctions but may be improved by the SFPV design. The third group (cSi, GaAs, InP) includes materials that can be successfully chemically doped to form high efficiency solar cells but may be cheaper to make (or attain higher efficiencies) using the SFPV geometry in conjunction with mild doping, heterojunctions, or MIS configurations. Sources for these data are as follows: Zn_3P_2 [9, 55], Sb_2S_3 [14, 84], SnS [43, 73, 88], Cu_2O [10, 70], and CZTS [4].

We have explored this effect with earth-abundant Cu_2O and are considering other such materials (SnS and Zn_3P_2).

2.5.1 Cuprous oxide

To demonstrate the universality of the SFPV effect, we studied Cu_2O, a hard-to-dope, earth-abundant semiconductor often touted as a high potential (up to 20% conversion efficiency), low-cost PV material [70]. As seen in 2.3, the doping range puts Cu_2O well within the range of feasibility for SFPV devices.

Before constructing experimental prototypes, we first modeled the system using COMSOL finite element simulations (used previously for silicon nanofinger SFPV) to estimate the potential for Cu/Cu_2O Schottky junction SFPV cells. Cu is known to form a fairly large Schottky barrier with Cu_2O, and tends to form at the surface of most metal-Cu_2O junctions (as most other low work function metals, needed for high barrier Schottky contacts, will be oxidized by the Cu_2O and leave a layer of reduced Cu). Parameters used for the simulation include the following: SiO_2 properties used in silicon SFPV simulations and thickness of 100nm, Cu_2O properties (p-type doping with $N_A \sim 10^{14}/cm^3$, minority carrier lifetime ~1 µs, $E_g \sim 2.2$ eV, $\alpha \sim 3 \times 10^5/cm$, thickness = 10 µm), and Cu contact separation of 2 µm. This doping level results in a depletion width of about 1 µm, so a contact width of 300 nm wide should allow for effective gating. Results for these simulations are shown in table 2.4.

Cell	V_{OC} (V)	I_{SC} (mA/cm^2)	Efficiency (%)
planar	0.6	5.1	1.7
SFPV (w = 300 nm)	0.79	7.8	3.9

Table 2.4: Cu/Cu_2O planar and SFPV simulations.

As seen in the table, the SFPV geometry is able to more than double in efficiency. In fact, this may not be the limit of attainable efficiencies, as the same SFPV cell achieved ~ 10% higher efficiencies (above 4% absolute) when doping was increased to $3 \times 10^{14}/cm^3$.

Motivated by this result, we created nanofinger Cu_2O SFPV cells. Instead of using Cu, we used indium tin oxide (ITO) contacts, as this has been shown to achieve higher V_{OC}; because the ITO is already an oxide, a layer of reduced Cu does not form and limit the barrier height as seen with low work function metals. Thermal oxidation is used to convert ~100-250 µm thick Cu foils (Puratronic, Alfa Aesar No. 42974) into polycrystalline Cu_2O wafers. These are then mechanically polished and chemically treated (using 2 vol% Br_2-MeOH at room temperature for 2 minutes) right before contact deposition to avoid a surface layer of CuO or other undesirable decomposition products. Full details of the Cu_2O growth can be found in chapter 5.

Heterojunctions are created using w = 750nm ITO nanofingers (5 µm spacing) contacting the p-type Cu_2O. A top gate is formed with electron-beam evaporated MgO dielectric (125nm) and sputtered ITO (40nm). Silver epoxy (Epotek H20E) is used to make ohmic contact to the bottom of the Cu_2O. Efficiency enhancement

(AM1.5 illumination) versus gate voltage is seen in figure 2.21, with an optical image of the device shown as an inset. A fairly small V_g (20mV) improves the efficiency by a factor of nearly 1.6. Our absolute efficiencies are quite small ($\sim 10^{-5}\%$) likely due to the high reactivity of the Cu_2O surface to moisture, which is known to drastically reduce V_{OC}. However, if applied to optimized devices (higher mobility Cu_2O with a non-damaged surface), the SFPV architecture may enable much higher efficiencies than present world records and make Cu_2O interesting for commercial PV cells or at least some electronics applications (e.g. 2.1eV laser diodes).

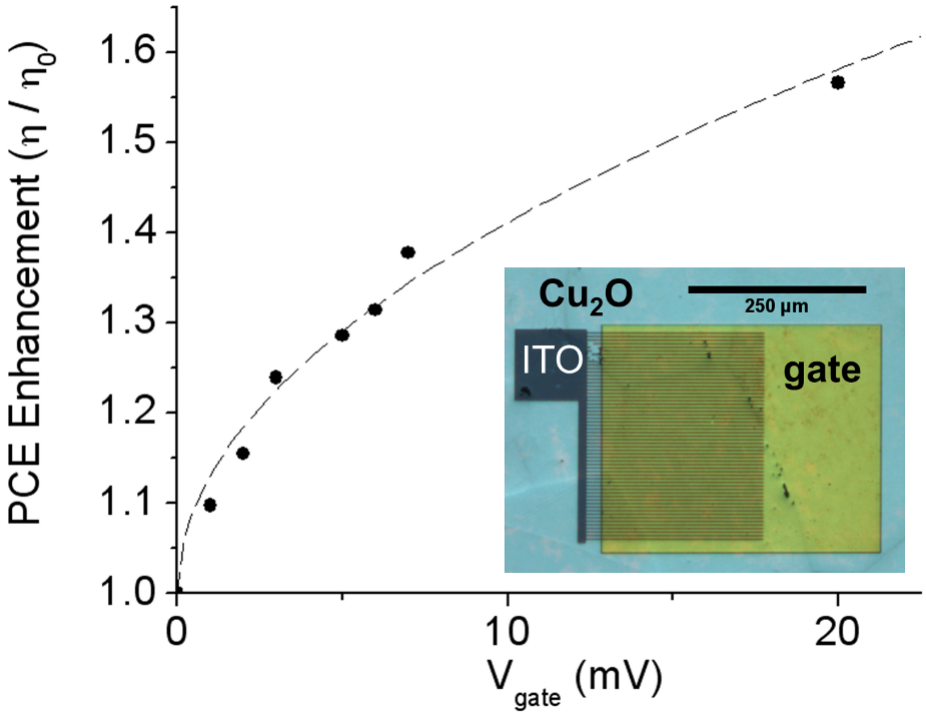

Figure 2.21: Efficiency enhancement versus gate voltage for Cu_2O SFPV cells, with an optical image of the device shown as an inset. (from [82])

2.5.2 Other candidate materials in progress

Besides Cu_2O, we are considering several other abundant oxides, phosphides, and sulfides for SFPV cells. Two of the most interesting materials, as shown in table 2.3, are SnS and Zn_3P_2.

Tin (II) sulfide

SnS has an orthorhombic crystal structure (seen in figure 2.22), with weak van der Waals bound bilayer planes stacked in the c direction. Like graphite and other weakly bound layered systems, crystalline SnS can be exfoliated to produce large, atomically-flat surfaces.

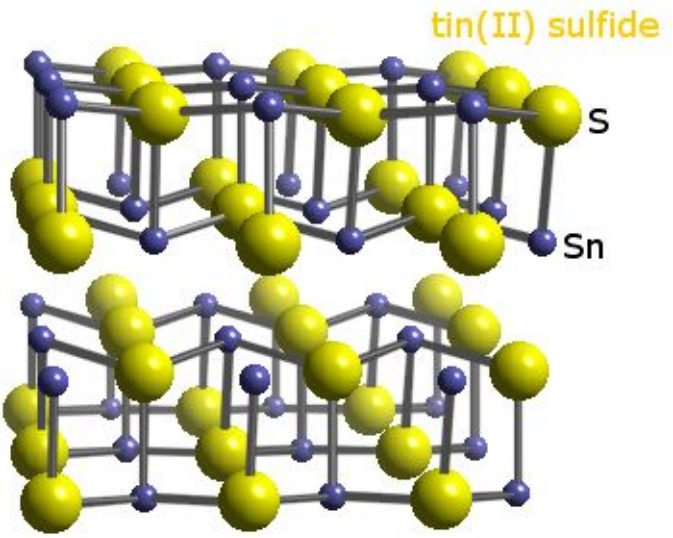

Figure 2.22: SnS crystal structure. Source: webelements.com

SnS has an indirect gap at 1.0 eV and a direct gap around 1.2–1.3 eV, allowing it to achieve $> 25\%$ PV efficiency. Single crystals of SnS have been grown with reasonable resistivity (120 Ω-cm) and high in-plane (perpendicular to the c-axis) mobility of 34 cm^2/V-s [43]. Efficiencies of up to 1.3% have been obtained using chemical spray pyrolysis grown SnS [80], and it stands to reason that higher crystallinity samples should enable higher performance efficiencies. This paper used a SnO_2 ohmic and In-doped CdS heterojunction contact, but other reports have suggested that In and (non-annealed) Al make good ohmic and Schottky contacts, respectively.

To investigate the potential of SnS SFPV cells, we grew SnS via vapor phase transport (details in chapter 5) and exfoliated the resulting single crystals onto SiO_2/Si substrates. Cleaving reveals large, smooth, pristine planes, as seen in figure 2.23. This image also shows a schematic of a possible SFPV cell, with an In microsoldered ohmic contact and Al nanofingers (on which a top gate could be applied), which exploits the high SnS in-plane mobility. Such cells would likely have low I_{SC}, as exfoliation tends to produce submicron thickness sheets. However, these cells could be tested at higher illuminations to simulate complete absorption of AM1.5 sunlight. Dr. Oscar Vazquez-Mena and Onur Ergen are continuing this work in the Zettl lab.

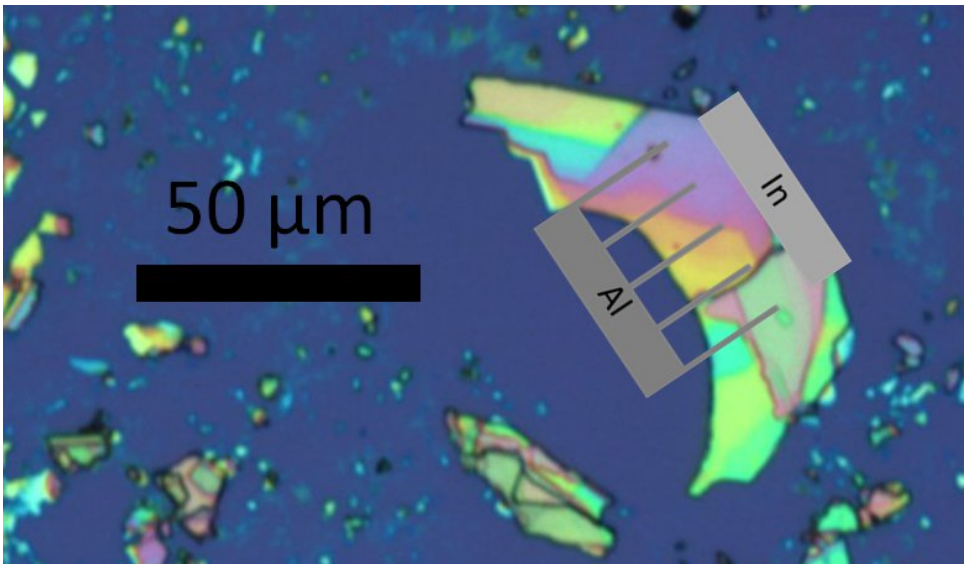

Figure 2.23: Exfoliated tin sulfide single crystals on SiO_2 and a schematic of a planned SFPV cell (In ohmic and Al nanofinger Schottky contacts). As noted in chapter 5, these crystals were revealed to be SnS_2, an indirect semiconductor with gap around 2 eV.

Future directions: Zinc phosphide, CdTe, CIGS

Zinc phosphide (Zn_3P_2) is another hard-to-dope but very promising PV material, with a direct bandgap of 1.5eV. Record efficiencies currently stand around 6%, using Mg Schottky contacts (which may alloy with the surface of the Zn_3P_2 upon annealing) [9]. We plan to construct nanofinger SFPV cells using Mg/Zn_3P_2 Schottky or Mg/(hBN or SiO_2)/Zn_3P_2 MIS cells. Growth methods for high quality Zn_3P_2 include vapor regrowth of stoichiometric ratios of Zn and P and molecular beam epitaxy. We have had some discussions with the Atwater research group at Caltech, experts in both these growth methods, to initiate collborations for Zn_3P_2 SFPV cells.

SFPV cells may also offer benefits to commercial p-n heterojunctions, namely those formed between n-type CdS and p-type CdTe or $CuIn_xGa_{1-x}Se_2$ (CIGS). CdTe and CIGS cells can currently achieve efficiencies in the high teens to low twenties, though they ought to be able to break 30%. Two problems with these cells include slightly non-ideal heterojunctions and parasitic absorption (absorption and nonradiative recombination) in the CdS. The SFPV geometry could address both of these issues by minimizing the area of CdS contact needed (by inverting the CdTe or CIGS in regions between the CdS) and increase the band bending that normally results from the junction with CdS. CdS is most often deposited on these cells by a chemical bath process. Due to the safety concerns in handling the waste that results from this bath process, we are considering alternate n-type materials such as bath-deposited

ZnS(O,OH) or sputtered ZnO. To make SFPV cells that could beat current industry costs, we would need a non-lithographic nanofinger contact deposition method such as electrospinning or spin-coating of premade nanowires and would also likely use a self-gating strategy with a fixed charge or polarization material.

2.6 Conclusions and future work

Our new SFPV method has shown that careful choice of the top contact geometry enables formation of high quality, electric-field-induced semiconductor p-n junctions. It offers the benefits of MIS and field-induced junctions (energy savings and minimized damage from chemical doping) and also relaxes the limitation of top contact heterojunction or Schottky barrier heights and may allow many previously impossible p-n junctions to be constructed, namely those using difficult-to-dope compound semiconductors that may hold the key to making solar energy an affordable energy source. Since SFPV cells use thick dielectrics ($\sim$ 100nm) instead of 1-2nm thick tunnel oxides, SFPV cells may prove more robust than MIS cells.

Several SFPV projects continue in the Zettl group, led by Dr. Oscar Vazquez-Mena and Onur Ergen. A few promising SFPV projects in progress include the following:

1. MIS silicon cells repeating Si SFPV cell design with a SiO_2 or other tunnel insulator
2. SnS cells using vapor grown, exfoliated single crystals
3. Zn_3P_2 or Cu_2O in collaboration with Caltech's Atwater group
4. Improving commercial CdTe or CIGS cells by selectively removing contacts and gating with P(VDF-TrFE)

Chapter 3

Graphene and carbon nanomaterials

3.1 Background

Graphene is an hexagonal 2D lattice of sp^2-bonded carbon. The carbon-carbon bond length is 0.142 nm and the unit cell consists of two inequivalent sites, A and B, as shown in figure 3.1.

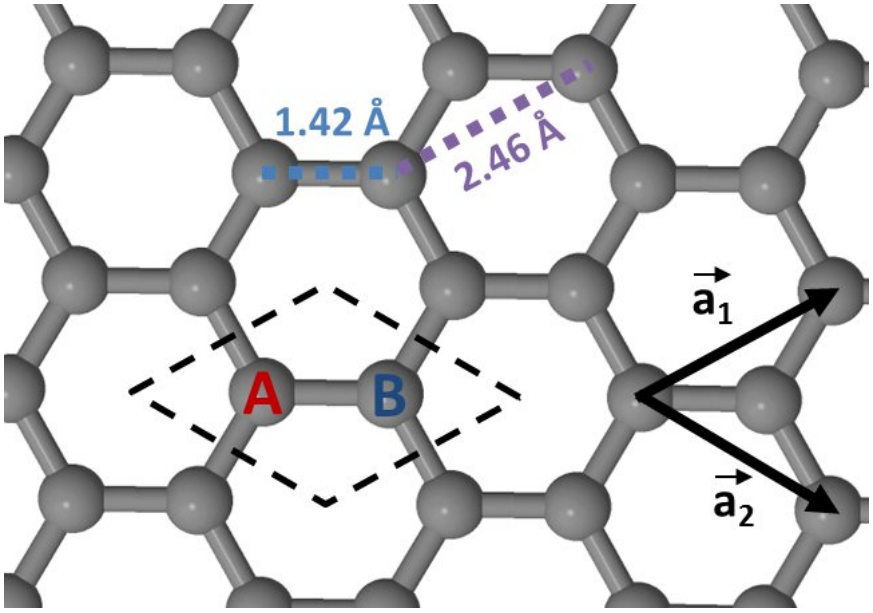

Figure 3.1: Graphene structure

Graphene's band structure can be estimated with tight binding, as reported by P. R. Wallace [101]. The result is a Fermi surface consisting of six Dirac points (three

sets of inequivalent K and K' points) and a linear dispersion relation (E= $\hbar v_F k$) at small energies around the Dirac points, as shown in figure 3.2 [12, 101].

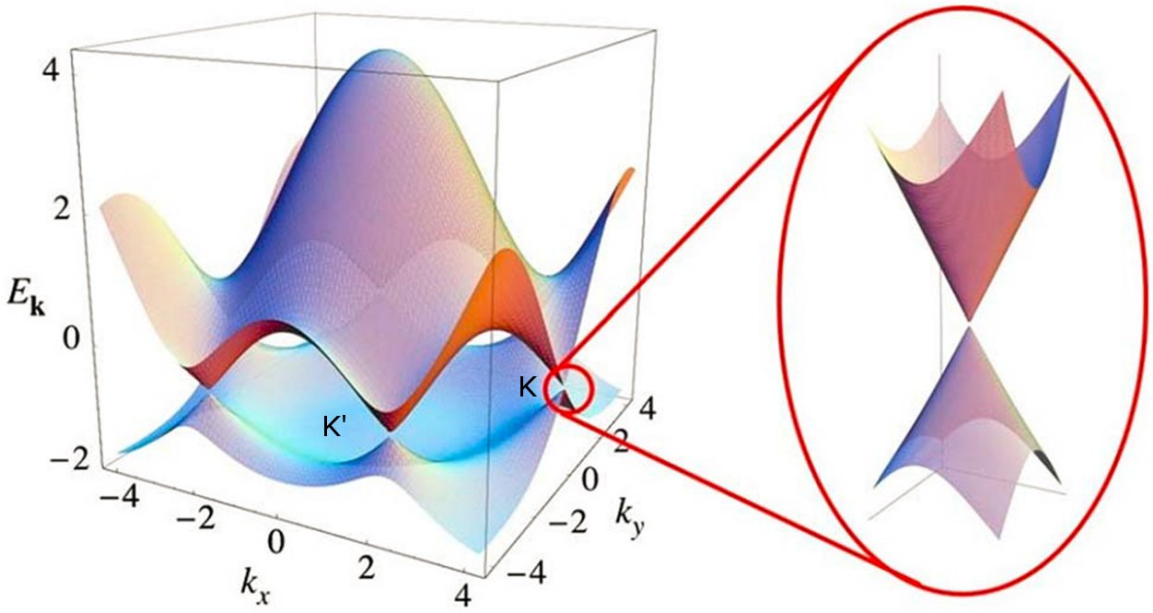

Figure 3.2: Band structure of graphene [101](image from Castro-Neto et al. [12])

This unusual band structure, which results in charge carriers behaving as relativistic massless Dirac fermions with an effective "speed of light" of $\sim c/300$ (10^6 m/s), leads to many of graphene's unique properties. Graphene's low density of states near the Dirac point makes it highly tunable with applied electric fields, as was shown in chapter 2 and will be discussed more fully in chapter 4.

3.2 Graphene growth by CVD

Novoselov and Geim's exfoliation techniques resulted in very low yields, typically at best a few 10 µm sized flakes per cm^2 Si wafer. Fortunately, a highly scalable and simple monolayer graphene growth method – chemical vapor deposition (CVD) – was developed in 2009. This was first demonstrated by the Ruoff group, using Cu as a growth substrate [63]. Hydrocarbons are flowed over the Cu substrate, which is maintained at a high temperature (enough to crack the hydrocarbon). The hydrocarbon, typically methane, adsorbs on the Cu, cracks, and graphitizes. Cu has a very low carbon solubility, and as a result only the cracked C is forced to remain on the surface until it graphitizes. Higher carbon solubility transition metals, such as Ni and Fe, result in the formation of few- or many-layer graphene [83]. In the Ruoff process, methane (CH_4) and a small amount of hydrogen (H_2) is flowed over

Figure 3.3: A picture of the carbon CVD system used for graphene and carbon nanotube synthesis. A quartz tube sitting in a furnace holds the growth substrate; gases enter the tube through the steel lines on the left and exhaust to a vacuum (or bubbler, for atmospheric pressure recipes) on the right.

Cu at 950°C –1040°C for 1–30 minutes. This can be performed at a reduced pressure (10 mTorr – 5 Torr) or at atmospheric pressure; in the latter case, a carrier gas such as argon is used and flow rates are increased from a few tens of sccm to hundreds of sccm.

Following the first published CVD growth recipe, my early growth recipes used a simple ramp to 1000°C in 10 sccm H_2 (to reduce and then prevent re-oxidation of the Cu substrate), followed by a 20 minute growth at 1000°C with 10 sccm H_2 and 40 sccm CH_4. A picture of the Lindberg Blue Mini Mite growth furnace is seen in figure 3.3. After growth, the tube and graphene-covered Cu were cooled to ∼25°C while flow rates for the methane and hydrogen gases were maintained. Such growth procedures resulted in grain sizes on the order of 1 µm.

To improve the grain size and quality of graphene, this simple recipe was later modified to a two stage growth process, adapted from Li et al. [64]. This modified recipe, is shown in figure 3.4. As shown in the figure, the two stage recipe begins with a high temperature anneal in H_2, to reduce the Cu and partially smooth its surface. Next, a low methane pressure growth step yields sparse nucleation of graphene grains, which grow until they begin to touch. To fully stitch together the grains, a higher methane partial pressure is then used. The sample is cooled to room temperature while maintaining H_2 and CH_4 flow. This two-stage CVD graphene has significantly larger grains, typically tens of µm, than the single stage CVD graphene. Additionally,

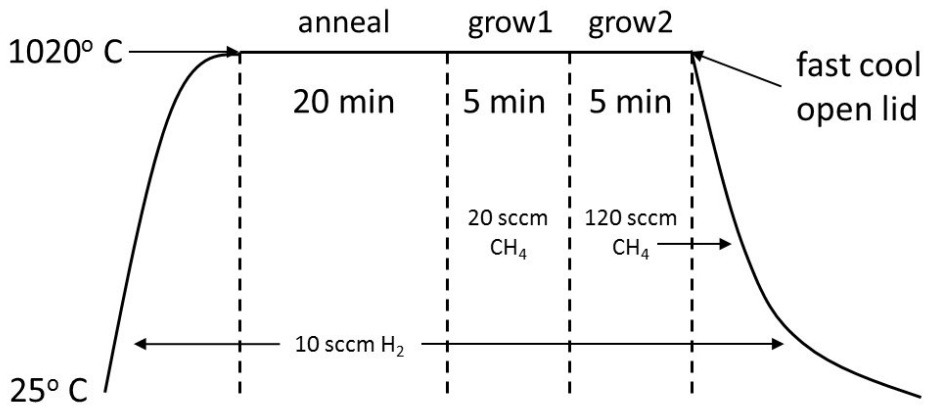

Figure 3.4: Two-stage CVD graphene growth recipe. The growth is preceeded by an anneal at high temperature, to reduce and smooth the Cu growth substrate. The first growth stage uses a low methane partial pressure, resulting in sparse nucleation and hence larger grains, and the second stage uses a higher methane partial pressure which fills in the cracks between grains.

the graphene is predominantly monolayer ($> 95\%$).

Our carbon CVD system was originally built for carbon nanotube growth and was not quite ideal for graphene growth. Lower methane partial pressure is crucial for large grain graphene; unfortunately, our vacuum pump couldn't achieve very low base pressures and the methane mass flow controller (MFC) couldn't operate below 10 sccm. Additionally, the system's placement in the center of the room prevented use of any possible toxic gases (e.g. for doping). Working with Kris Erickson, I designed and built a more verstaile CVD system (seen in schematic form in figure 3.5) which could perform graphene growth from a variety of precursor gases (methane for standard growth and acetylene for lower temperature growth). In addition to graphene, this system was designed to also perform hexagonal boron nitride (hBN) synthesis, from ammonia (NH_3) and boron trichloride (BCl_3) or from borazine. The pump could achieve a base pressure around 1 mTorr, lower than our carbon CVD system. Like the carbon CVD, this new system also uses a Lindberg Blue Mini Mite furnace. The pump has a slightly higher volumetric pumping rate (to achieve a better base pressure) and uses Fomblin PFPE oil which is compatible with the caustic byproducts used in hBN growth. Additionally, the entire CVD system was housed in a fume hood as a safety precaution (again due to the hazardous hBN precursors).

For nearly all studies in this thesis, CVD graphene growth was performed on 25 µm thick Cu foil (Alfa Aesar No. 13382, 99.8%). However, graphene growth may be performed on a variety of substrates: different metals; foils or thin films of these metals; directly on dielectric substrates; and others. Results and experiments using graphene grown on alternate substrates are found in section 5.3.

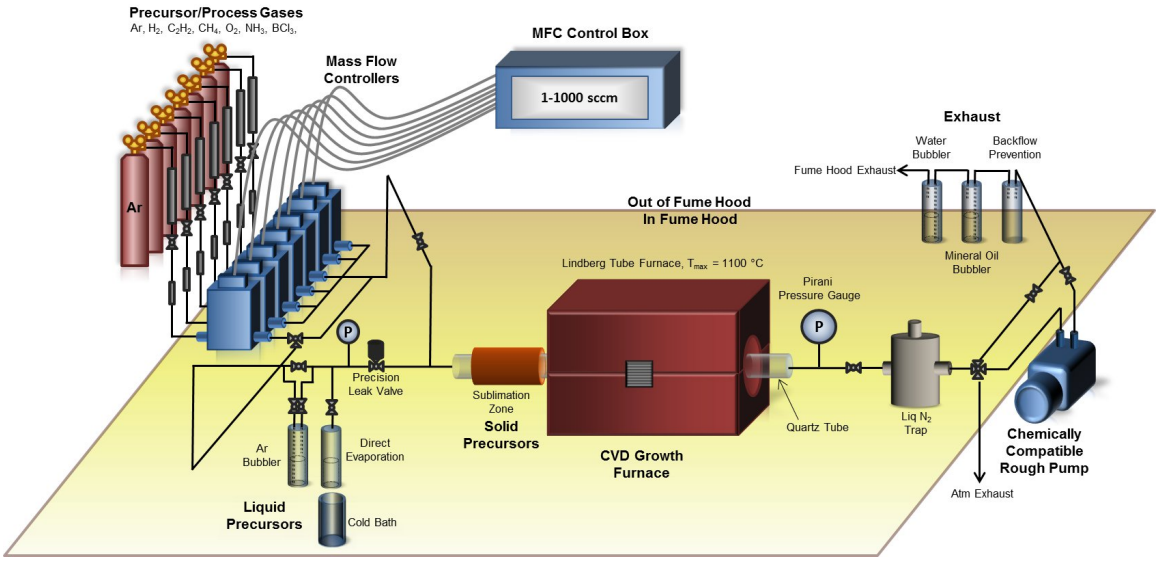

Figure 3.5: CVD system for graphene and hBN growth (schematic courtesy of Kris Erickson)

3.3 Manipulation of CVD graphene

After CVD growth but before characterization, we must first remove graphene from its Cu growth substrate. Additionally, nearly all interesting applications require removal of the Cu metal to prevent shorting. A more suitable graphene substrate would be an insulator, such as SiO_2 or (as will be shown in chapter 4) hexagonal boron nitride (hBN). Most methods of transferring CVD-grown graphene from its Cu growth substrate to a new substrate involve some variation of (1) stabilizing the atom-thick graphene with a polymer or other thick but flexible temporary support, (2) wet etching of the Cu[1], (3) adhesion of the graphene and support to the new target, and (4) removal of the temporary support. In this section, several methods of CVD graphene transfer will be described, and their limitations and advantages will be highlighted.

3.3.1 Polymer-supported graphene transfer

One versatile graphene transfer method uses a spin-coated polymer support, typically poly(methyl methacrylate) (PMMA), as a temporary support during Cu etching which is later dissolved away. The procedure is as follows:

1. Spin coat PMMA (A4 950 - Microchem) onto graphene/Cu at 3000 rpm for 30

[1]Fortunately, graphene is stable enough to resist oxidation by most wet etchants used to remove Cu.

seconds and cure at 175°C for 15 minutes.

2. (Optional) Remove graphene on the opposite side of the Cu with an oxygen reactive ion etch (Zettl group RIE: 50 sccm O_2, 50 W, 20 seconds). This is recommended for persulfate etchants (as the bottom graphene layer often remains partially adhered to the top) but is not necessary for iron chloride.

3. Snip off any PMMA edge beads and remove any visible PMMA on the backside, as this will mask the Cu etching.

4. Float the PMMA/gr/Cu foil on a dish of Cu etchant (0.1 g/mL $FeCl_3$ or 0.25 g/mL $Na_2S_2O_8$) with the Cu side facing down. Etching of 25 µm thick Cu foils takes about 40 minutes.

5. Rinse the PMMA/gr membrane by carefully transfering it to a dish of deionized water (DI); we use a Teflon-coated steel spoon or clean Si wafer as the transfer vehicle. After 20 minutes, transfer to another clean dish of DI and allow to soak for another 30 minutes.

6. Skim the PMMA/gr membrane out of the DI with your target substrate. Evaporate trapped water by placing the PMMA/gr/target on a 60°C hotplate for 15 minutes.

7. (Optional) "Reflow" the PMMA by heating it above the PMMA glass transition temperature to relax the PMMA/gr membrane and allow it to confirm to the target substrate. We typically reflow at 190°C for 10 minutes.

8. Remove the PMMA by submerging the sample in room temperature acetone for 2 hours (or 55°C acetone for 30 minutes). Rinse in IPA and blow dry.

Different polymers may be used, such as polystyrene (which has been reported to be somewhat cleaner than PMMA) or PDMS (which lets you stamp graphene onto targets, avoiding the need to dissolve the PDMS), but we consistently achieve high yields with few breaks and manageable contamination with PMMA.

The reflowing process mentioned in the procedure (and shown in figure 3.6) was developed[2] by me and Will Gannett to minimize tearing in transferred graphene. We observed striping patterns in transferred PMMA/graphene membranes and reasoned that these were due to the PMMA conforming to the wavy Cu substrate (a result of the foil rolling procedure). When we transferred to a very flat Si substrate, the reasonably firm PMMA could not conform to the Si and much of the graphene would be unsupported as the PMMA dissolves in acetone. We speculated that this was the cause of the severe cracking seen on the left in figure 3.6. We therefore decided to

[2]A similar method was reported in the literature by the Ruoff group shortly after we developed this procedure [94].

heat the PMMA above its glass transition temperature (about 125°C for Microchem PMMA) to allow it to soften and conform to the Si, allowing the graphene to uniformly adhere to the SiO_2 surface. After reflowing the PMMA at 190°C for 10–20 minutes and performing a standard acetone liftoff, we observed significantly reduced graphene tearing, as shown on the right in figure 3.6.

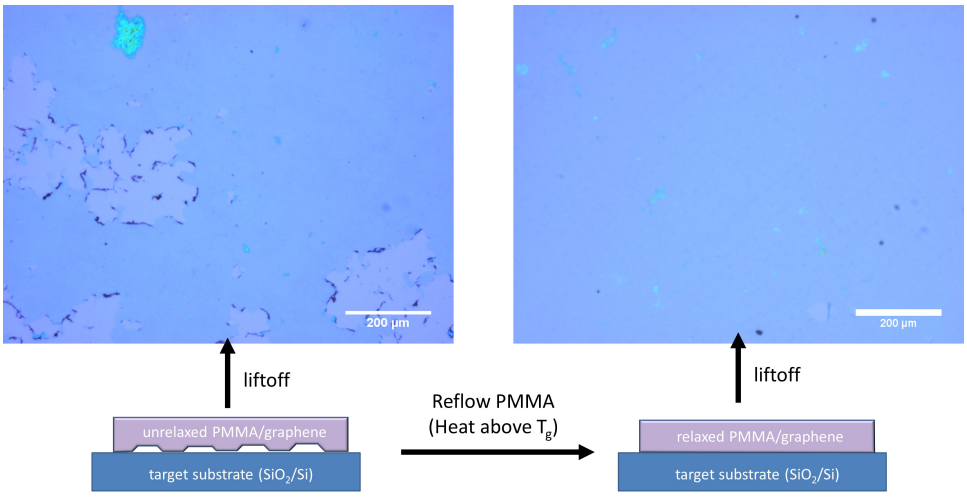

Figure 3.6: Improved graphene transfer with PMMA reflowing

Using a PMMA support allows for transfer to almost any target, even curved or rough surfaces. However, it inevitably leaves some PMMA residue, which is tolerable for most electronic devices but is a problem for procedures requiring very clean graphene such as atomic force microscopy (AFM) or high resolution transmission electron microscopy (TEM). To prepare ultraclean graphene for these and other applications, a direct and polymer-free transfer method was developed.

3.3.2 Direct, polymer-free transfer of CVD graphene

The direct graphene transfer method exploits the strong adhesion of graphene to perforated amorphous carbon films, namely Quantifoil or lacey carbon Au TEM grids, which are used as *both* the temporary and the final graphene support [81]. In short, the direct transfer process uses the evaporation of isopropanol (or other clean liquids) to pull the thin, flexible TEM grid coating into contact with the graphene on Cu. After adhesion, the Cu substrate is etched away and the graphene remains stuck to the grid (which is supported with a tough-to-etch metal such as Au); the yield is extremely high (near 100%) and the process introduces no additional contaminants. A schematic for the direct transfer process is shown in figure 3.7, along with TEM micrographs of the resulting graphene-covered Quantifoil TEM grid. Further detail and much of the remaining section is also found in our *Applied Physics Letters* article [81].

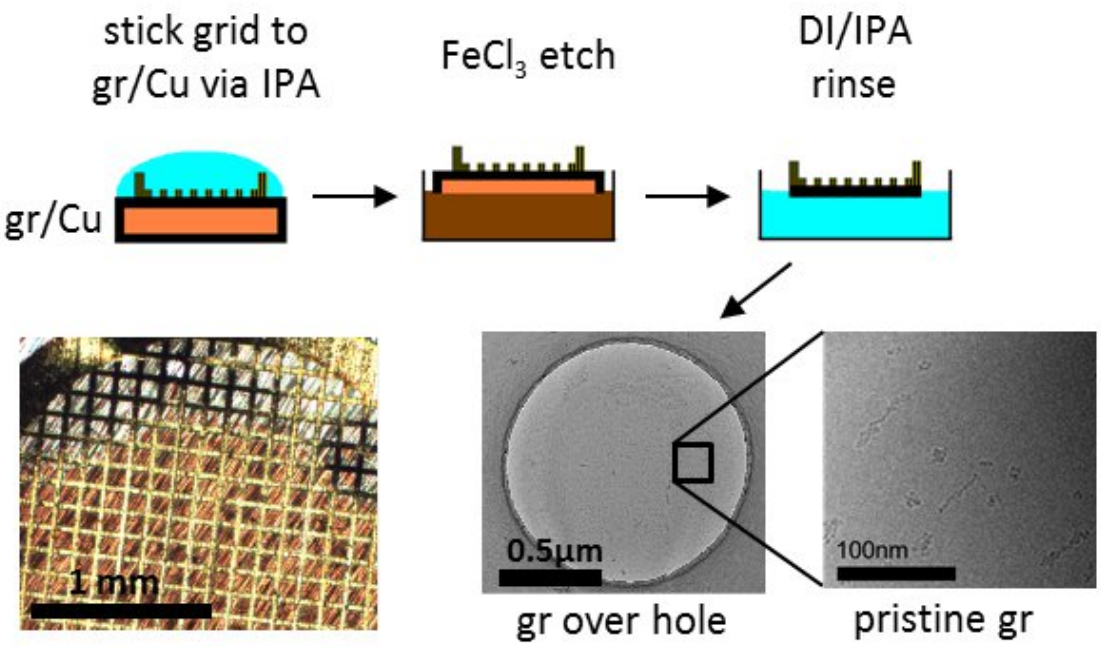

Figure 3.7: Direct graphene transfer to TEM grids. Graphene is adhered (via IPA evaporation) to the flexible carbon coating of a Quantifoil TEM grid; the optical micrograph shows reddish contrast for adhered regions. The Cu support is etched and the graphene-covered grid is rinsed in DI and IPA. TEM images acquired with the Zettl group's JEOL 2010 at 100kV show the extremely high cleanliness of the resulting suspended graphene. (from [81])

The suspended membrane transferred to the TEM grid is confirmed to be monolayer graphene by TEM diffraction, as shown in figure 3.8. An hexagonal diffraction pattern is evident as expected for graphitic materials, and the diffraction spots do not change significantly in intensity upon tilting of the sample, a sign of monolayer graphene.

The direct transfer is far quicker than polymer-supported transfers and results in very clean, suspended graphene. As a result, this method was used to prepare samples for most of the experiments descibed in this chapter and continues to be used extensively in the Zettl group. Motivated by the success of the direct transfer, we pondered alternate methods to free the graphene from Cu and eventually devised transfer-free suspended graphene sample preparation.

3.3.3 Transfer-free synthesis of suspended CVD graphene

An alternative to removing all of the Cu and transferring graphene to a new substrate is to selectively etch small pits to create locally suspended graphene mem-

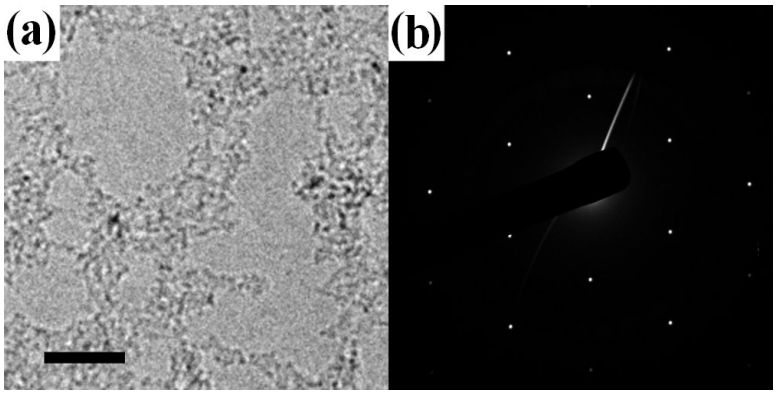

Figure 3.8: TEM imaging and diffraction of suspended graphene. Part (a) shows a relatively clean region of suspended graphene (scale bar = 25 nm), and part (b) shows diffraction data taken in this region, revealing the familiar hexagonal pattern for graphene. The intensity of diffraction spots is unchanged upon tilting, further evidence of monolayer thickness. (from [81])

branes. We refer to this as the transfer-free method of Cu removal. In this method, developed with former Zettl group member Dr. Benji Aleman, lithography is used to define etch sites on the back of graphene/Cu foils and etching is performed through the foil at these sites to small suspended graphene regions. A schematic of the process is seen in figure 3.9.

Using this method, home-made graphene TEM grids (with Cu supports) were fabricated, as shown in figure 3.10. Some non-unformities in the etch rate are manifested in the varying Cu hole diameter seen on the right. Besides making TEM grids, the process can also be adapted for other applications of suspended graphene, such as chemical filters, sensors, speakers, etc.

Both electron energy loss spectroscopy (EELS) and energy dispersive x-ray spectroscopy (EDS) were performed by Dr. Shaul Aloni (LBNL) on $FeCl_3$-etched graphene TEM grids to analyze contamination due to the etching and fabrication process, as shown in figure 3.11. It was revealed that $FeCl_3$ copper etching resulted in disperse iron oxide nanorods. It was later shown that such residue could be avoided by using one of several persulfate Cu etchants ($Na_2S_2O_8$ or $(NH_4)_2S_2O_8$).

Once graphene was removed from its Cu growth substrate, we performed a variety of characterization methods to assess its quality. Some of the more convenient and useful methods are optical microscopy, Raman spectroscopy, and transmission electron microscopy.

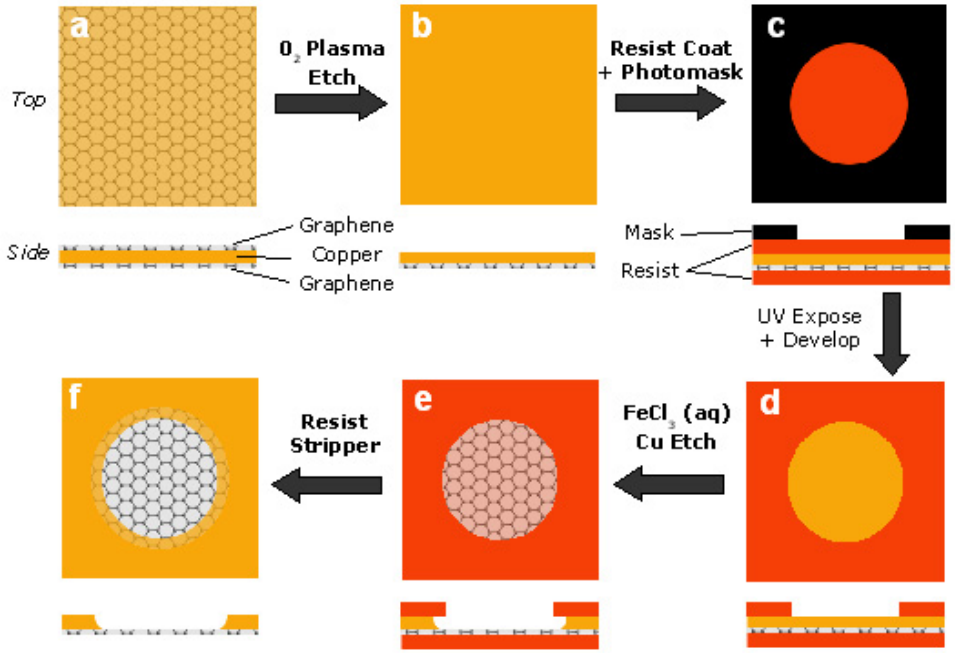

Figure 3.9: Fabrication process for transfer-free graphene/Cu TEM grids. (image from [2])

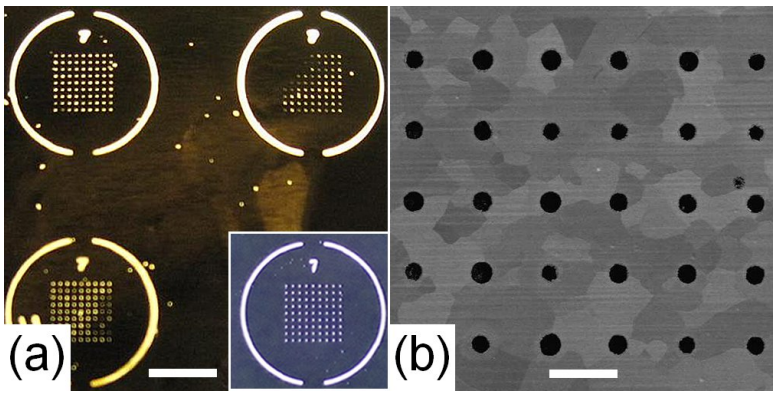

Figure 3.10: Graphene/Cu TEM transfer-free TEM grids, showing (a) grids with arrays of suspended graphene (with a Cr/quartz photolithography mask show as an inset) and (b) a SEM micrograph of one grid with graphene-covered holes. Scale bars are (a) 1.5 mm and (b) 150 µm. (image from [2])

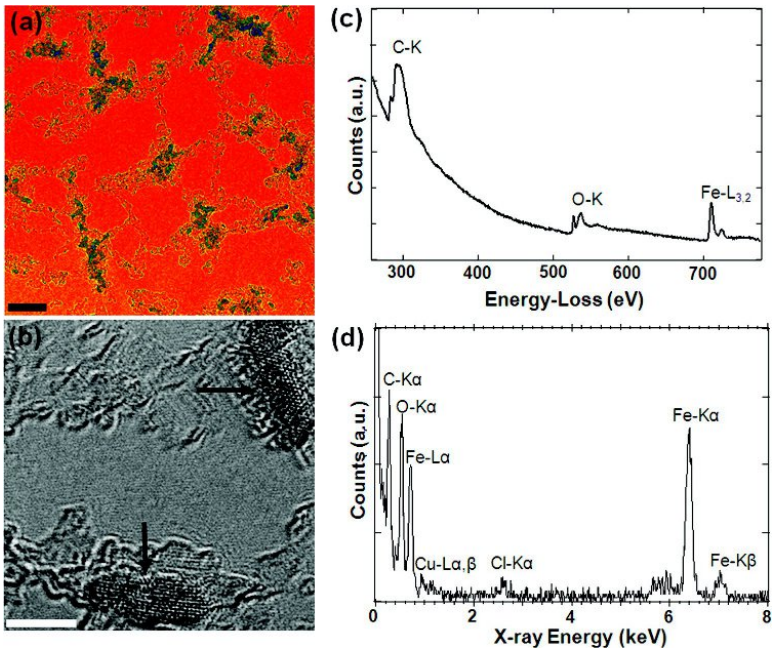

Figure 3.11: EELS and EDS spectra on graphene TEM grids showing $FeCl_3$ etchant residue in the form of iron oxides. (image from [2])

3.4 Characterization of CVD graphene

3.4.1 Optical microscopy of graphene

The simplest and quickest methods for graphene characterization are optical methods. When placed on certain thicknesses of SiO_2 on Si wafers, even monolayer graphene can be made visible to the naked eye. Using a simple optical interference calculation, it can be shown that monolayer graphene has about a 7% green contrast difference per layer on 285nm SiO_2 on Si [11]. Optical identification of exfoliated bilayer graphene is described in chapter 5 (figure 5.8). Optical identification of CVD-grown monolayer graphene is not so simple, as transfer of graphene to SiO_2 is most commonly accomplished with a PMMA support, which leaves residue with its own contribution to the optical contrast. Generally, higher contrast means more PMMA contamination, though a detailed analysis has not been performed and there may be regimes in which thicker PMMA residue leads to reduced contrast.

3.4.2 Raman spectroscopy of graphene

A more versatile optical method of graphene charcterization is Raman spectroscopy, which uses inelastic Raman scattering to probe the vibrational and electronic structure of target samples. A spectrometer measures the small shift in frequency be-

tween incident and re-emitted light which results from the annihilation (anti-Stokes shift) or creation (Stokes shift) of a phonon in the material. The measured Raman shift is expressed in cm^{-1}, with positive shift corresponding to the Stokes process, a much stronger signal than the anti-Stokes at room temperature. Multiple phonon resonant Raman processes can also sometimes be detected.

The Zettl group uses a Renishaw inVia micro-Raman spectrometer, which consists of an optical microscope with movable table, a bank of 3 lasers (with excitation frequencies of 485nm/514nm, 633nm, and 785nm), optics to focus the lasers onto the sample, and a spectrometer to analyze the Raman-shifted signal emitted from the sample. This system can focus the excitation light down to a ∼1 µm diameter spot, allowing relatively precise local characterization to be performed, as well as large scale mapping of the uniformity of graphene structure.

Raman processes in monolayer graphene were first convincingly demonstrated by Ferrari et al. [30], who corroborated the monolayer graphene Raman signal with diffraction data. The photon and phonon transitions involved in the common graphene Raman modes are shown schematically in figure 3.12. The G peak (at ∼1580 cm^{-1}), seen for all graphitic materials, is a first-order process involving a zone-center phonon and corresponds to the in-plane stretching of C-C sp^2 bonds. The D peak (at about 1350 cm^{-1}), or defect peak, is a second-order intervalley process involving phonon scattering off of defects. One should be aware that not all defects will yield a D signal, as zigzag edges have been shown to disallow intervalley scattering [57]. The G' or 2D peak (at about 2680 cm^{-1}) is a double resonance, from a real state in K to a real state in K' and back.

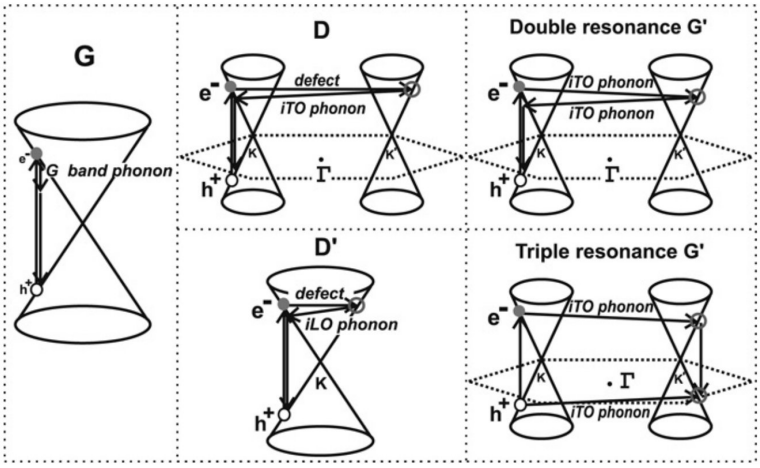

Figure 3.12: Raman modes of monolayer graphene (image from [68])

Raman spectra for SiO_2-supported and suspended monolayer graphene is seen in figure 3.13. The key features of monolayer spectra are a 2D peak intensity greater than the G intensity and a 2D peak shape that can be fit with a single Lorentzian curve.

For bilayers the 2D/G ratio is 1 or less, and the 2D peak begins to have shoulders (and can be fit with 4 Lorentzians, or more for thicker layers). Additionally, we see that the 2D/G ratio is significantly larger for suspended samples, as substrates tend to suppress the 2D process.

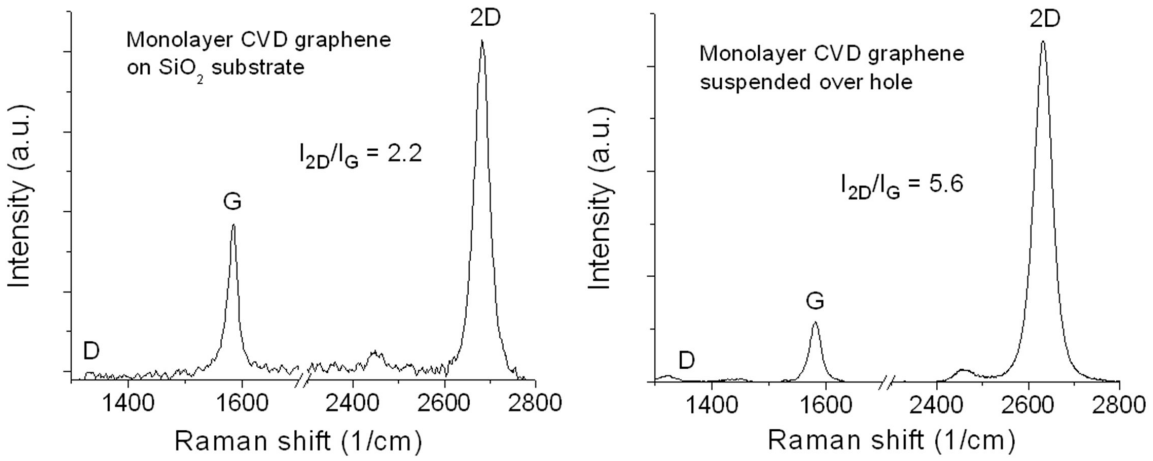

Figure 3.13: Typical Raman spectrum for SiO_2-supported and suspended CVD graphene (514nm excitation).

Thus, Raman spectra are able to determine (with precision down to the wavelength limit) the local crystallinity and thickness of graphene. A highly defective sample will have a large D peak, while the D peak should be negligible ($I_G/I_D << 1$) for pristine monolayer graphene.

While as-grown bilayer graphene samples are almost always AB stacked, one can artificially create rotated bilayer graphene by transferring two graphene monolayers onto a substrate. The varying overlap of Dirac cones in rotated "bilayer" graphene creates new resonant processes and modifies the G and 2D peak (shown schematically in figure 3.14), thus enabling determination of the rotation angle of the sheets. This work was lead by Kwanpyo Kim of the Zettl group and collaborators in the Cohen and Louie groups.

As instructive and easy as these Raman studies are, the most exact characterization method for graphene (besides scanning tunneling microscopy, not discussed here) is transmission electron microscopy (TEM). Aberration-corrected TEM, such as that performed with the TEAM 0.5 and TEAM 1.0 at LBNL's National Center for Electron Microscopy (NCEM), can tell you the exact position of every atom in monolayer graphene.

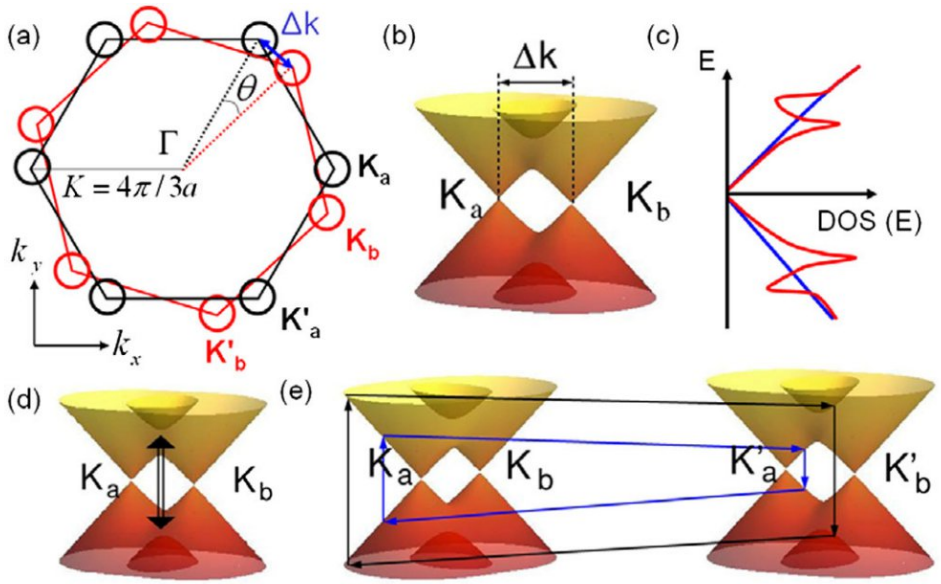

Figure 3.14: Band structure and modified Raman modes of bilayer graphene rotated by θ (image from [52])

3.4.3 TEM studies of graphene

Transmission electron microscopy uses a beam of high energy electrons (10s to 100s of keV, and sometimes up to MeV) to analyze the structure of very thin (<10 nm) samples, with electrons serving an analagous role to photons in transmission optical microscopy. Instead of using glass lenses, TEMs use magnetic and electrostatic lenses to focus and expand the electron beam. Though an electron energy of 100 keV corresponds to a sub-angstrom wavelength, the relatively poor lenses limit resolution. However, with post-processing aberration correction, atomic resolution imaging can be performed, as demonstrated by NCEM's TEAM microscopes.

Graphene is uniquely suited for analysis by TEM. Since it is all surface, imaging normal to the graphene plane can precisely map every constituent atom. Using our ultraclean direct-transfer graphene TEM grid preparation described earlier in this chapter, we undertook several studies to more fully understand CVD graphene: grain boundary structure, beam-induced graphene tearing, and high temperature stability. These studies were spearheaded by Kwanpyo Kim of the Zettl group. Much more detail for these projects and additional projects can be found in Kwanpyo's PhD thesis, currently in preparation.

TEM analysis of graphene grain boundaries

Within a single grain of CVD-grown graphene, the crystallinity of the graphene seems comparable to that of exfoliated graphene. However, as we will discuss in the

next chapter in the context of CVD graphene transistors, the electronic properties (mobility, etc) of CVD graphene are still somewhat inferior to that of exfoliated. Part of the reason for this is that exfoliated monolayers are most commonly single grains. Electronic devices made from CVD graphene, on the other hand, will often contain many grain boundaries, potential sources of disorder. Thus, knowledge of the size, shape, and orientation of CVD graphene grain boundaries is important for developing high performance CVD graphene electronics.

TEM is very well suited for this challenge. Two methods were used to map graphene grain boundaries. The first is selected area diffraction (SAD), in which an aperture is used to limit diffraction to a very small region (as small as a few tens of nanometers). The diffraction pattern is correlated with the local grain orientation, so by rastering the sample under the SAD aperture one can detect when the grain changes orientation (at a grain boundary). By scanning the x and y position of the sample relative to the SAD aperture, one can map out the grain boundaries and local grain orientations over a large area, as shown in figure 3.15. An alternate method to perform this mapping is dark field imaging, described in detail in Kwanpyo Kim's PhD thesis.

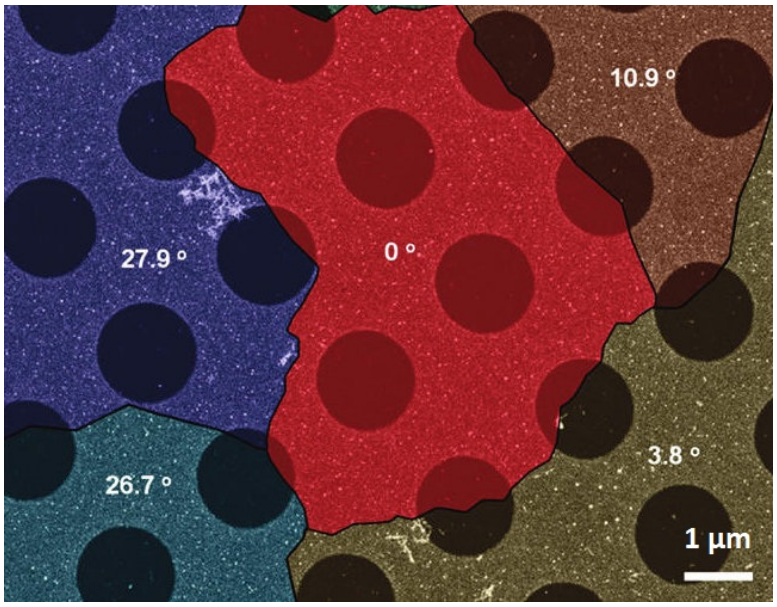

Figure 3.15: TEM mapping of CVD graphene grains on a Quantifoil TEM grid, as determined by scanning selected area diffraction (SAD) (image from [54])

Additionally, the bonding structure of graphene grain boundaries is critical to understanding polycrystalline graphene's electronic transport and mechanical properties. Using the aberration corrected TEAM 0.5 microscope, the atomic structure at a CVD graphene grain boundary was determined (figure 3.16). The high angle tilt grain boundary seen in this figure is revealed to have a repeating 5-7 structure.

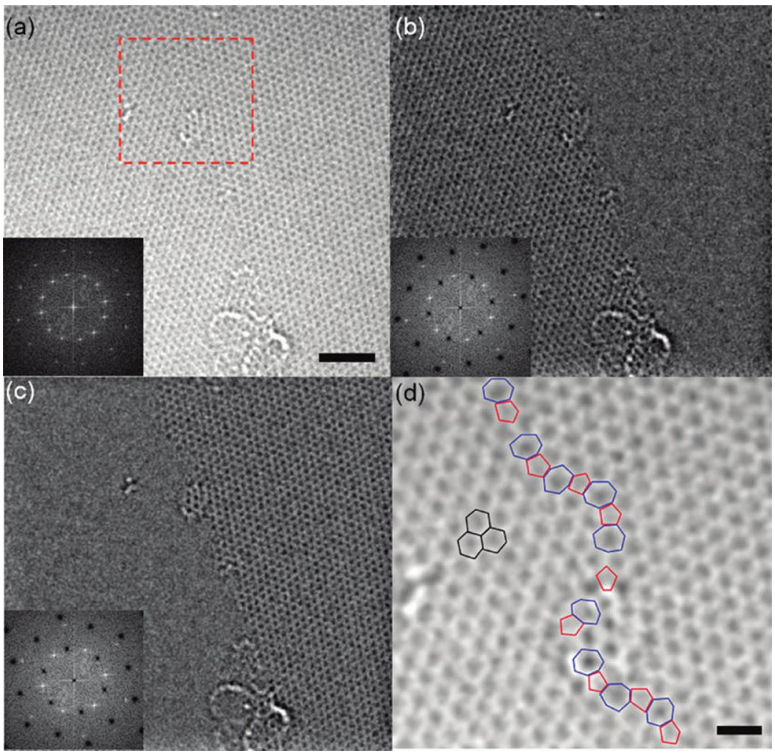

Figure 3.16: Atomic resolution imaging of graphene grain boundary (using NCEM's TEAM 0.5 microscope at 80 keV with Zonghoon Lee). (a) Atomic resolution image of CVD graphene grain boundary (scale bar = 2 nm). (b) and (c) Processing (a) with FFT, removing one hexagonal pattern, and inverting the FFT to make one of the grains disappear. (d) A zoomed image of the boundary, revealing a pentagon-heptagon structure (scale bar = 0.5 nm). (image from [54])

Graphene torn under the TEM electron beam

Understanding the mechanical properties of CVD graphene is also critical to applications such as flexible electronics and mechanical resonators. For instance, it is not known if grain boundaries are the weak links in CVD graphene or if ripping occurs along certain preferred directions within pristine grains.

To investigate the tearing of graphene, direct-transferred CVD graphene TEM grids were imaged in the Zettl group's Jeol 2010 TEM. Tears resulting from the graphene transfer process were imaged, and it was observed that these tears could be made to propagate further under the beam. The rate of propagation could be very fast (around 1 µm/s with only 0.01 A/cm^2 of beam current). The TEM was operated at 100 keV, above the knock-on damage threshold of 86 keV, but beam-induced tear propagation was also performed at much lower beam energies. The mechanism of tear extension is thought to be due to the transfer of energy to highly-strained

carbon bonds at tear edges.

In this study, tears were observed to propagate preferentially along zigzag and armchair directions. A typical tear is shown in figure 3.17, alternating between armchair and zigzag directions. The inset to this figure shows a histogram of the observerd tears throughout the grid, again highlighting the preference for zigzag and armchair tearing. Collaborators Vasilii I. Artyukhov and Professor Boris I. Yakobson at Rice University performed theoretical studies which supported these results, showing that zigzag and armchair tears are preferred to other directions.

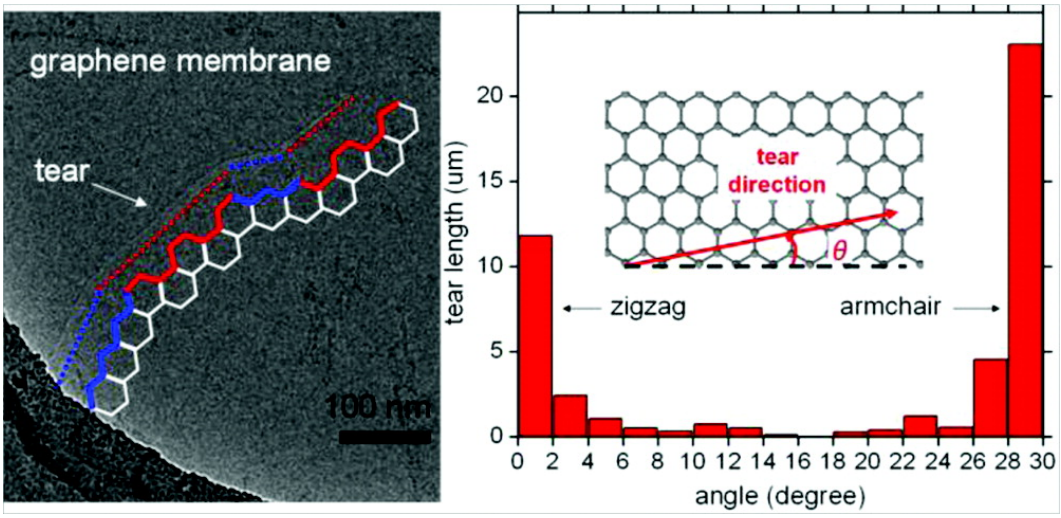

Figure 3.17: Preferred graphene tearing directions. A tear passing through armchair and zigzag directions is shown on the left, and a histogram of tear directions seen throughout the grid is shown on the right. (image from [51])

This study suggests that grain boundaries do *not* seem to be the limiting factor in polycrystalline graphene strength, as tears prefer to move along zigzag or armchair directions even when crossing grain boundaries.

3.4.4 Graphene's mixed success as an oxidation barrier

Graphene's short-term oxidation resistance

There have been several reports of graphene's potential as an anticorrosion coating for metals such as Cu [18, 76]. In the short term, this has been shown to be true for thermal oxidation and submersion in corrosive solutions. Thermal oxidation resistance of graphene-covered Cu, as compared to bare Cu, is dramatically demonstrated in figure 3.18.

Over a few minutes or hours, graphene-covered Cu or Ni show only sporadic oxidation at graphene defect sites, tears, and grain boundaries. Optical and SEM

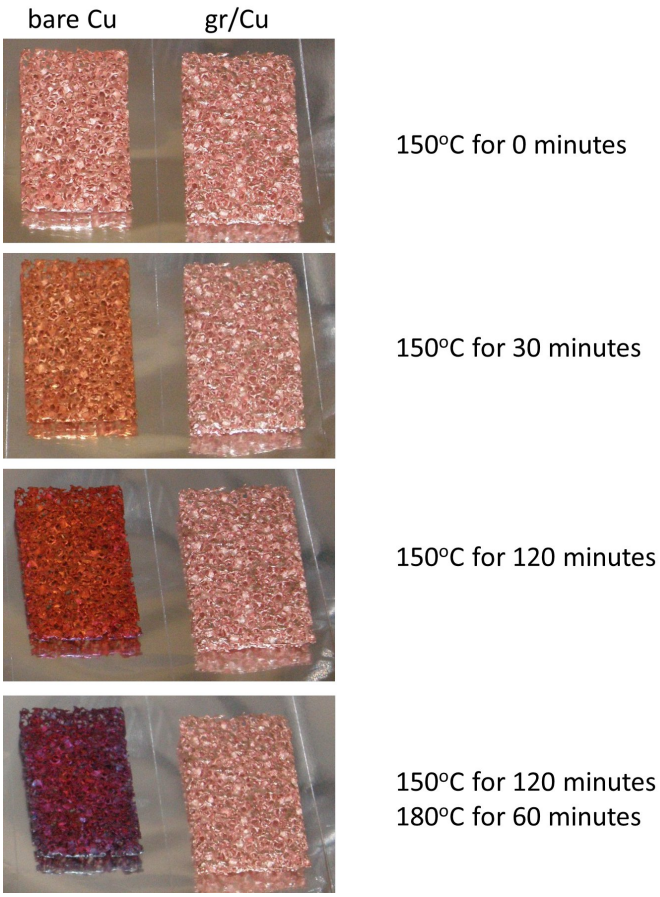

Figure 3.18: Thermal oxidation of bare and graphene-covered Cu. The Cu used in this example is a Duocell Cu foam (No. C10100, 8–10% density).

images of graphene-covered Cu heated at 185°C for 20 minutes are shown in figure 3.19.

"Aging" of graphene on Cu and galvanic corrosion

Despite the short-term oxidation resistance of graphene coatings, we also observe that graphene on Cu foils will "age" over time, eventually oxidizing the Cu quite strongly, much moreso than completely bare Cu. This is shown for aged bare, reduced/annealed, and graphene covered Cu foils in figure 3.20.

In contrast with previous reports, we propose that this long-term oxidation is encouraged by graphene, catalyzing galvanic corrosion in moist environments, with a rate limited strongly by diffusion of water and/or oxygen between the graphene and Cu. Moisture is present as atmospheric humidity where the samples are stored. The work function of graphene is around 4.6 eV for neutral doping and can vary

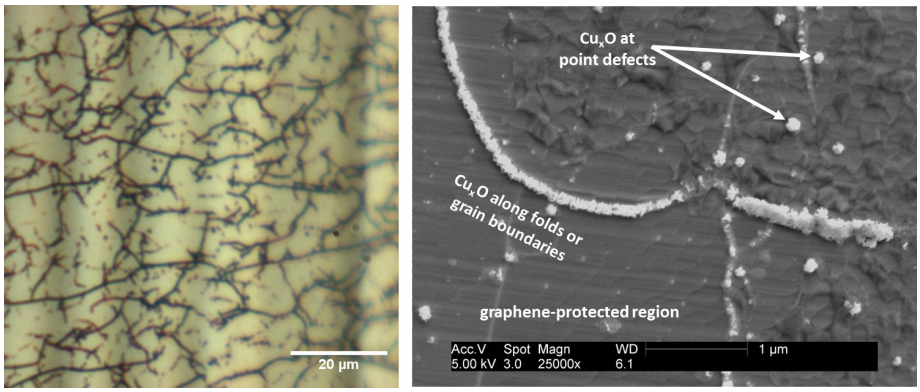

Figure 3.19: Thermal oxidation resistance of graphene-covered Cu. After 20 minutes at 185°C , graphene-covered Cu remains largely unoxidized, with Cu_xO forming only at defects (grain boundaries, folds, point defects), as seen in optical micrographs (left) and higher resolution SEM images (right).

between 4.5–4.8 eV [108], with slight p-doping typical for atmospheric conditions. The work function of Cu depends on crystal direction; values for a few common facets are 4.48 eV (110), 4.59 eV (100), and 4.94 eV (111) (from [7]). Thus, certain Cu facets are anodic to graphene, and we expect electron transfer from these facets to graphene (figure 3.21). Moisture and O_2, when present, can complete the redox reaction, forming Cu_xO or $Cu(OH)_x$. The difference in work function for different Cu facets may explain our observation that certain graphene-covered Cu grains don't appear to oxidize or at least oxidize more slowly relative to others due to the smaller potential difference with the graphene. Alternatively, this different rate of aging could be due to tighter bonding of graphene to certain Cu facets. The local Cu work function may also be a fairly minor factor influencing corrosion; simply introducing the graphene conduction pathway to the surface could be the most significant factor encouraging continued corrosion reactions.

Despite this driving force, a graphene-covered Cu surface still takes weeks or months to appreciably oxidize. This may be due to the slow diffusion of water between the graphene and Cu. The permeability of graphene to water is not fully understood, but if pristine graphene blocks water from directly contacting Cu, water may be forced to first enter at a point defect or grain boundary. Once the Cu has been oxidized at a defect, oxidation may spread further as water squeezes through the gap opened by the local oxidation.

Galvanic corrosion as the mechanism for graphene "aging" is also consistent with improved oxidation resistance of Cu/Ni alloys, as Ni has a much larger workfunction (ϕ_{Ni} ~5 eV), and the Cu/Ni alloy may have a sufficiently large workfunction to suppress electron transfer to graphene [18]. This explanation of corrosion, if accurate, implies methods to improve oxidation resistance, such as n-doping (perhaps

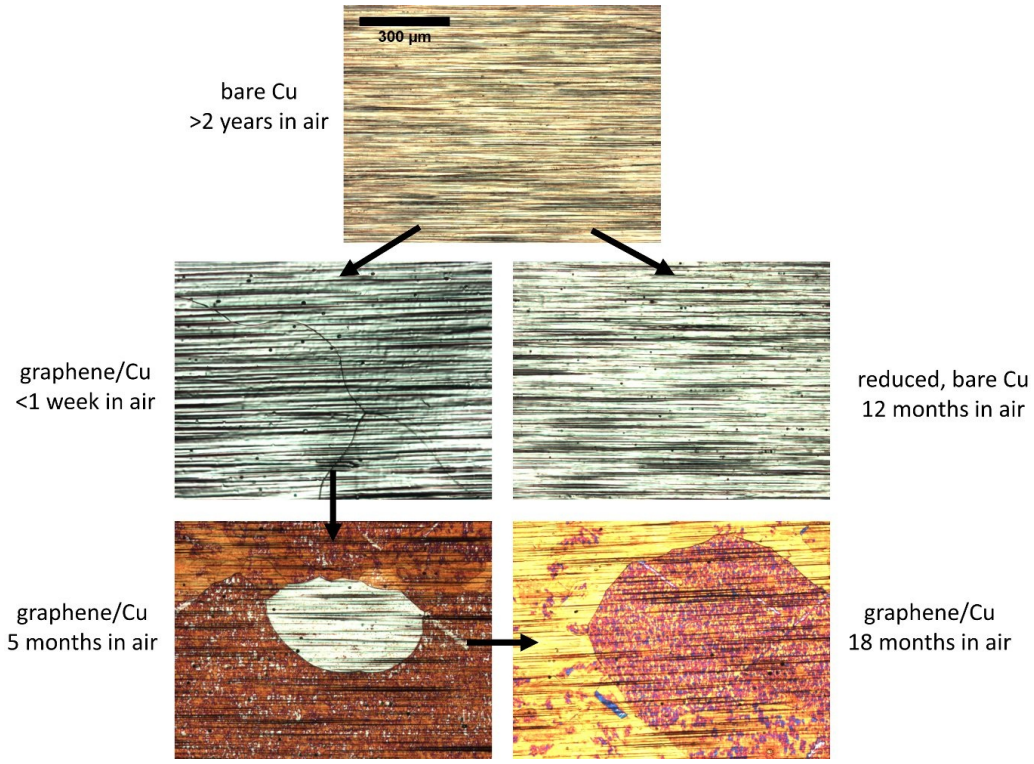

Figure 3.20: Aging of bare and graphene-covered Cu. Bare Cu forms a passivating oxide that limits further corrosion, whereas graphene-covered Cu continues to oxidize over time. Certain Cu grains oxidize at different rates; for instance, we see a large barely-oxidized patch in the middle of a sea of heavy oxidation for the 5 month old graphene/Cu sample. All images are real color optical micrographs, captured using the same lighting conditions.

nitrogen-doping with ammonia or N_2 plasma) the graphene enough to decrease its work function below those of all the common Cu facets.

Forced thermal oxidation of graphene-covered Cu

In addition to long-term galvanic corrosion of graphene-covered Cu, one can also force thermal oxidation of graphene-covered Cu at temperatures lower than the oxidation onset for graphene. This may be due to a combination of partial graphene oxidation and increased diffusion of oxygen into Cu at graphene defects, coupled with increased diffusion of oxygen through the Cu. A graphene-covered Cu sample heated at 250°C for 17 hours is seen in figure 3.22, revealing uniform copper oxidation and the formation of Cu_2O "flowers" and CuO nanowires under the graphene. Raman spectroscopy performed on this sample reveals that graphene is still present on the surface, with a decreased signal presumably due to the increased surface roughness.

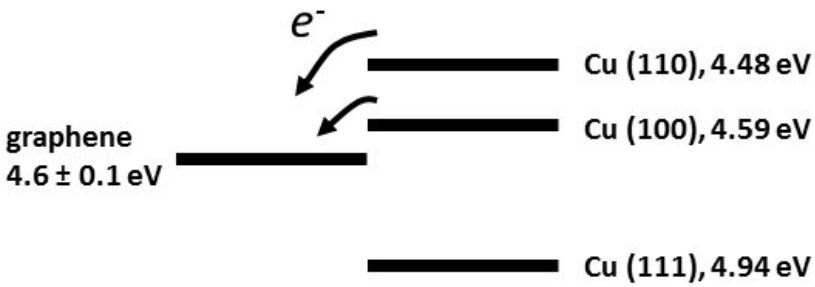

Figure 3.21: Galvanic corrosion of graphene-covered Cu. Due to a difference in graphene and Cu work functions, electrons will transfer from Cu (110) and Cu (100) to graphene. The rate of corrosion may be affected by externally doping the graphene. Based on this model, Cu (111) might not corrode beyond the typical native oxide.

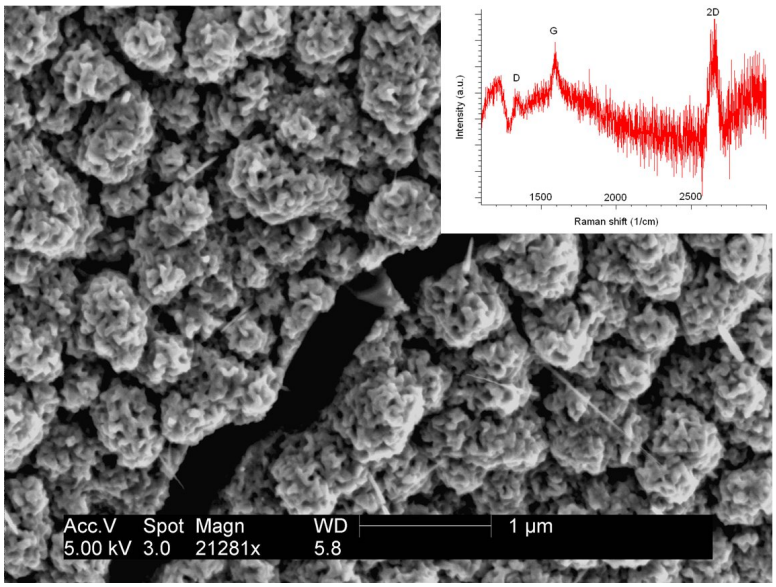

Figure 3.22: Graphene/Cu oxidized at 250°C for 17 hours, revealing uniform conversion of Cu into Cu_2O "flowers" and CuO nanowires. Raman spectroscopy confirms that graphene remains intact on the surface, with a signal largely diminished by the significantly increased surface roughness.

Similar oxidation is expected at a lower rate at lower temperatures, though CuO nanowires may not form below 200°C . This system, graphene/(Cu_2O,CuO)/Cu, may be interesting for electochemical or gas sensing applications.

3.5 Novel graphene superstructures

Graphene is often described as the mother of all sp^2-bonded carbon allotropes. Graphite (3D) is produced by stacking sheets of graphene (2D), and carbon nanotubes (1D) and fullerenes (0D) are produced by slicing and rolling up bits of graphene. As the art of origami demonstrates, many other varied shapes may be produced by folding sheets. Thus, we investigated many structures which may be produced by rolling, folding, or otherwise manipulating graphene.

3.5.1 Grafold

While graphene is a fairly rigid sheet, it can be made to fold into different structures. Though bent or strained graphene comes at an energy cost, the van der Waals interaction between sheets can lower the overall energy of a locally folded region relative to a flat sheet. Thus it is not surprising that when manipulating CVD graphene we often create locally folded regions.

Locally folded regions of graphene, termed "grafold," are frequently observed in CVD graphene directly transferred to TEM grids and to SiO_2/Si substrates, as seen in figure 3.23. Grafold's discovery and initial TEM analysis were spearheaded by Kwanpyo Kim of the Zettl group. More information such as theoretical calculations performed by collaborators in the Cohen group, as well as some data discussed below, can be found in our *Physical Review B* paper [53].

An atomic-resolution TEM image of a single recumbent grafold and a rendering of its structure is seen in figure 3.24.

Similar to nanotubes, grafold structures can be tuned in many ways, by varying folding angles, number of folds, edge functionalization, and intercalants between folds. Preliminary work has shown that grafold can be intercalated with C_{60}, similar to C_{60}-filled carbon nanotube peapods [90] or boron nitride nanotube silos previously reported by the Zettl group [69]. Electronic transport measurements on "intrinsic" grafolds (no intercalants other than PMMA residue) were performed by me and Will Gannett and are found in chapter 4.

3.5.2 Graphene sandwiches and veils

In addition to quasi-1D grafold nanostructures, graphene can be mated with nanoparticles to create new types of staged compounds referred to as graphene sandwiches and veils. Such structures are created by first depositing nanoparticles (or other materials) onto a clean graphene monolayer. Next, another graphene monolayer is transferred on top, trapping the nanoparticles between the two layers of graphene. Depending on the density of nanoparticles, these structures are referred to as either graphene sandwiches (dense) or veils (sparse). In veiled structures, the graphene bilayer is able to locally seal off the isolated nanoparticles, sealing them in

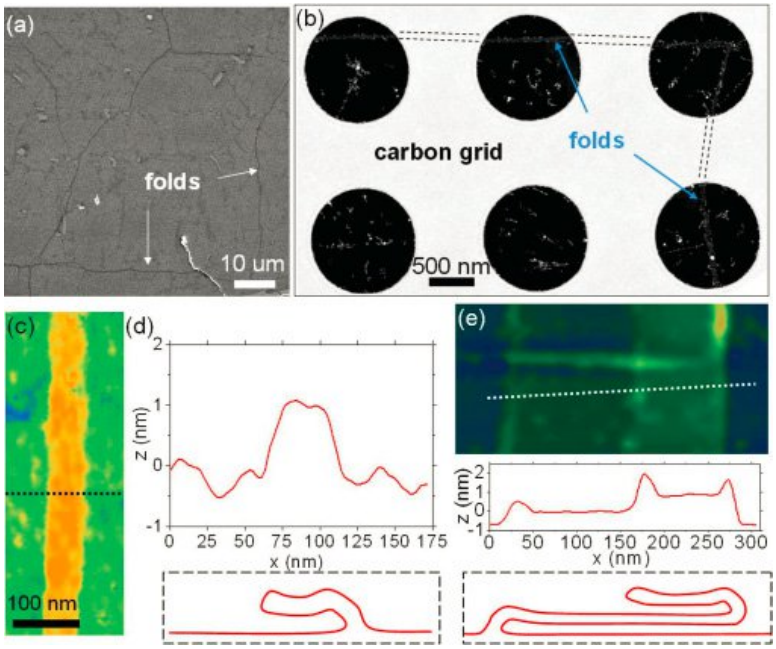

Figure 3.23: Grafolds seen in (a) SEM, (b) TEM, and (c) (e) AFM. In (d), a height profile across the grafold in (c) implies a single recumbent fold structure (shown schematically). The height profile of the grafold in (e) shows a more complicated double fold structure. (image from [53])

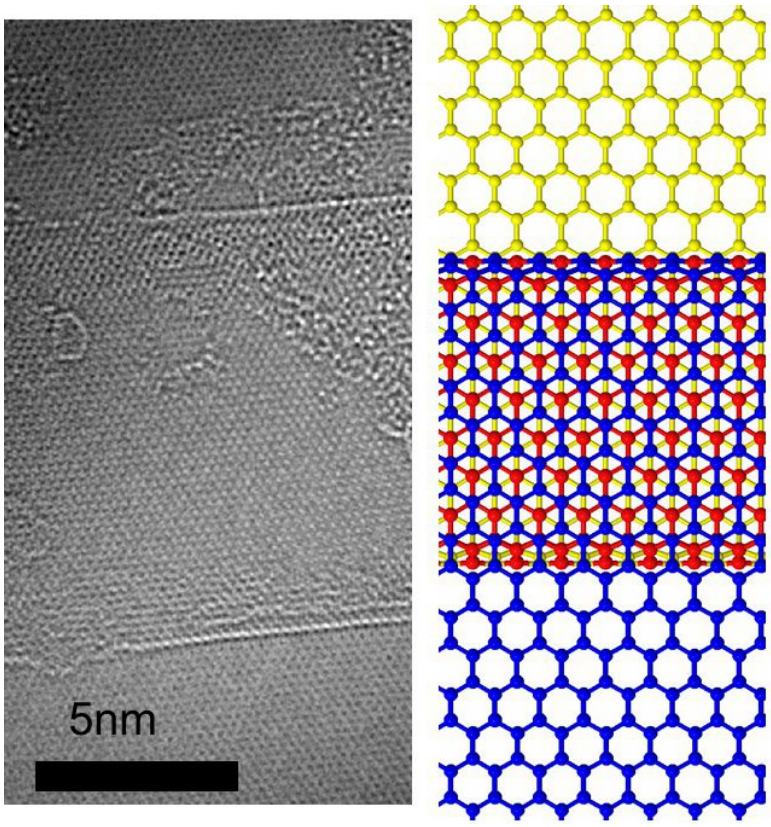

Figure 3.24: Atomic resolution TEM image of grafold (NCEM TEAM 0.5, operated at 80 keV), and at right a rendering of the grafold's structure (images courtesy of Kwanpyo Kim)

their own little carbon chambers. This can be repeated many times to create combinations of sandwiches and veils, as shown in figure 3.25. This work was spearheaded by Jongmin Yuk, previously of the Zettl group.

Graphene is an excellent platform for TEM analysis of nanoparticles. It is atomically thin, low-Z, and crystalline, allowing any small graphene signal to be effectively subtracted from images of very small nanoparticles. Graphene sandwiches and veils thus provide excellent imaging platforms, allow unprecedented resolution in-situ TEM observations of chemical reactions.

3.5.3 Graphritos

In the absence of substrate adhesion, graphene prefers to scroll up. As mentiond previously when discussing grafold, sheet-sheet van der Waals interaction can overtake the energy cost of strained regions and lower the overall energy of crumpled or scrolled graphene. Exfoliated graphene which is poorly adhered to SiO_2 can be made to scroll

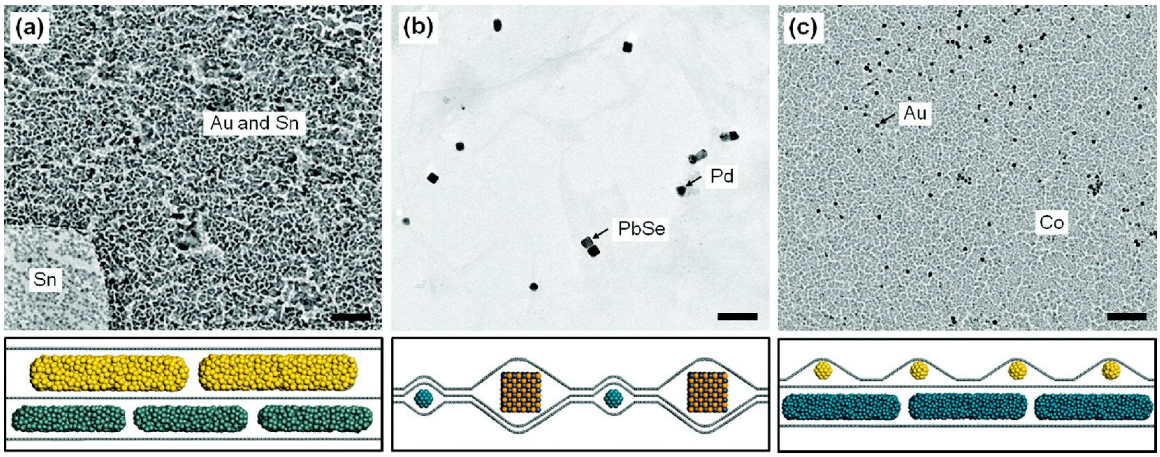

Figure 3.25: TEM images of various compound graphene sandwiches and veils (image from [110])

by submersing it in isopropanol [104]. Such structures, which are somewhere between graphene and nanotubes, may prove interesting for applications where high surface areas are important (e.g. batteries or H_2 storage).

Inspired by this work and by burritos, we attempted to fabricate carbon nanoscrolls with arbitrary filling, thus creating filled carbon nanoscrolls or "graphritos." The fabrication for these structures was as follows:

1. Grow graphene via CVD on Cu
2. Coat graphene with "filling" (i.e. metallic or insulating nanoparticles)
3. Drop PDMS[3] on graphene and cure at 150°C on a hot plate for 2 minutes
4. Etch the supporting Cu film with $FeCl_3$ and rinse PDMS/filling/graphene in deionized water.
5. Rub the PDMS stamp across a target substrate. This results in graphritos with axes perpendicular to the rubbing direction.

The fast, high temperature PDMS curing builds up strain which leads to cracking in the graphene film, perhaps due to the mismatched expansion/contraction rates of the PDMS, Cu, and graphene. This cracking may happen as the graphene is freed from its Cu substrate (during the etch), leading to scrolling of the newly created graphene edges. PDMS-transferred graphene which has been stamped onto a SiO_2/Si wafer is seen in figure 3.26. Cracking occurs roughly on the scale of a few to tens of microns, and the edges on the resulting graphene flakes tend to scroll.

[3]Sylgard 184 (Dow Corning), mixed 10:1 PDMS:hardener by weight

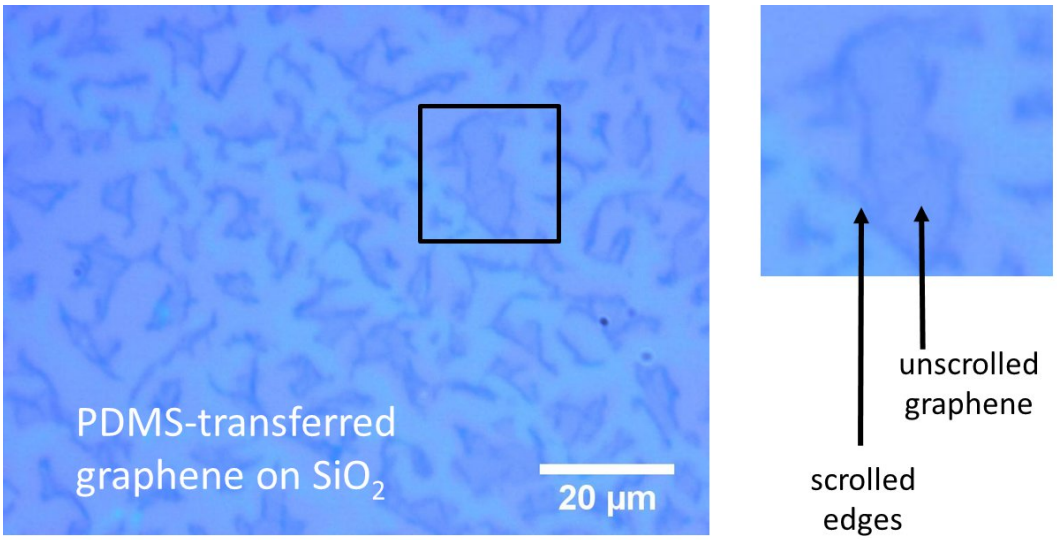

Figure 3.26: Optical images of cracked and scrolled PDMS-transferred CVD graphene on a SiO_2/Si substrate. The stamp was pressed straight down to avoid a preferential rolling direction. Sliding the stamp in a certain direction would create graphritos with symmetry axes perpendicular to the sliding direction.

When we put "toppings" on the graphene before etching, we may reduce the attraction between sheets and inhibit spontaneous scrolling. However, the action of rubbing the PDMS stamp across a surface is sufficient to overcome this barrier, even with very thick graphene coatings. SEM images of PMMA-filled (about 150nm thick) graphritos are seen in figure 3.27.

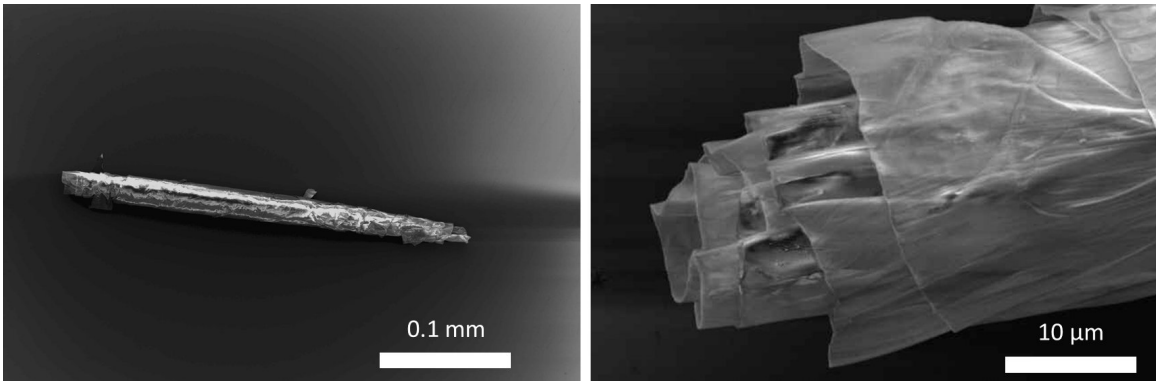

Figure 3.27: SEM micrographs of PMMA-filled graphritos

This technique should prove very versatile, though the graphene coatings must be resistant to the copper etchant used. Possible interesting materials could include insulators, piezoelectrics, semiconductors, and etchant-resistant metals.

Chapter 4

Graphene electronics

4.1 Basic properties

As described in the previous chapter, monolayer graphene has a linear dispersion relation ($E = \hbar v_F k$, where $v_F \sim c/300$) at energies near the Dirac point. Graphene's conductance can be estimated using the Drude model, with contributions from electrons and holes, as

$$\sigma = n_e e \mu_e + n_h e \mu_h$$

where n and μ are the carrier density and carrier mobility (for electrons and holes).

The carrier density can be tuned by the electric field-effect. We typically accomplish this by exfoliating or placing graphene on 285 nm of thermally-grown SiO_2 on Si wafers, a convenient oxide thickness for both back gating and optically identifying monolayers. For graphene on 285 nm SiO_2, the carrier density is

$$n = \frac{c_g}{e}|V_g - V_D|$$

where V_D is the gate voltage needed to reach the Dirac point and c_g is the gate's specific capacitance (115 aF/cm^2).

Thus, we can estimate the carrier mobility with a linear fit to the conductance versus gate voltage (in the regime away from the Dirac point, neglecting short range scattering) as

$$\mu \sim (\frac{d\sigma}{dV_g})/c_g$$

The mobility of graphene is a good metric of its electronic quality. Highly pristine graphene can have a very high electronic mobility, up to $\sim$200 m^2/V-s. Most of the exciting electronic applications and studies of graphene require high electronic mobility. In practice, the electronic mobility of graphene is typically much lower, due

to a combination of scattering from substrate effects, dopant impurities, and defects. Common themes in this chapter include the effect of substrate choice on the carrier mobility (section 4.2) and doping (section 4.3) of graphene. Additionally, experiments on other graphene structures – graphene nanoribbons (GNRs) and grafold field-effect transistors (FETs) – will be discussed. The research in this chapter was conducted in collaboration with fellow Zettl group member Will Gannett, who was instrumental in device measurement and data analysis. More information on all of these topics can be found in Will Gannett's PhD thesis, currently in preparation, and additional information specifically about graphene FETs can be found in our *Applied Physics Letters* article [34].

4.2 High electronic mobility graphene FETs

It was recently shown that hexagonal boron nitride (hBN)[1] is an excellent substrate for graphene [28]. Exfoliated hBN is chemically inert (due to the lack of out-of-plane bonds), flat, and nearly lattice matched to graphene. Using exfoliated graphene and exfoliated hBN (obtained from K. Watanabe and T. Taniguchi of NIMS), C. R. Dean and others in Columbia University's Hone group produced graphene field-effect transistors (FETs) with μ_e up to 60 m^2/V-s [28]. However, this method is extremely time consuming, compounding the low yield of graphene exfoliation with that of hBN exfoliation. A more suitable method for rapid and parallel device fabrication would require continuous graphene and/or hBN sheets. Large scale and highly crystalline hBN growth is still in development, but large area monolayer graphene growth by CVD has been attained. Using identical SiO_2 substrates, reported carrier mobilities in CVD graphene (typically ∼1–3 m^2/V-s) have so far lagged those in exfoliated graphene (10–20 m^2/V-s), but the reasons for this difference are unclear [34]. As CVD graphene grain sizes are increased and atomic-resolution studies continue to show no fundamental difference in crystallinity within CVD and exfoliated graphene grains, one would expect that CVD graphene should behave comparably to exfoliated samples. Perhaps reported differences are not due to graphene crystallinity but instead result from impurities introduced during manipulation and transfer of the CVD graphene to SiO_2. To investigate this further, we constructed FETs using CVD graphene transferred to exfoliated hBN substrates, with the hBN supported by SiO_2/Si wafers (SQI arsenic doped, n-type, 1-5 mΩ-cm). To be consistent with C. R. Dean et al., hBN samples were obtained from the same source (K. Watanabe, T. Taniguchi). CVD graphene was grown by the 2-step process described in figure 3.4.

To construct these FETs, we exfoliated hBN flakes onto a SiO_2/Si wafer. We

[1]The structure of hBN is analogous to graphite with a few exceptions: the A and B sites are boron and nitrogen instead of two carbons, the boron-nitrogen in-plane bond length is 0.144 nm instead of 0.142 nm as for graphene's carbon-carbon sp^2 bond, and the planes stack such that a boron is always directly above a nitrogen (and vice versa).

calcined the wafer at 450°C to burn off any tape residue on the hBN surfaces, and then transferred CVD graphene onto the wafer using PMMA-supported transfer. Two steps of e-beam lithography were performed, the first to define an oxygen plasma etch mask to pattern the graphene and the second to define Hall bar contacts (source, drain, and two sets of sense electrodes) to the graphene. The fabrication process for these CVD graphene FETs is summarized in figure 4.1.

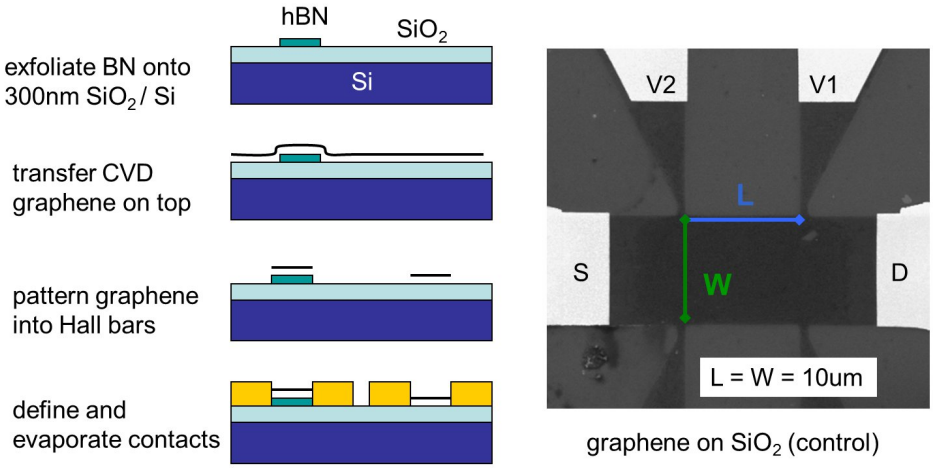

Figure 4.1: Fabrication process for CVD graphene FETs (with hBN or SiO_2 substrates), and an SEM image of a resulting graphene/SiO_2 FET, with graphene leads contacted with Cr/Au.

After transfer of CVD graphene onto the hBN/SiO_2/Si, SEM imaging revealed unusual patterns on graphene-covered hBN flakes, as seen in figure 4.2. These patterns were likely due to transfer residue (etchant, water, isopropanol) trapped between the graphene and hBN or perhaps due to PMMA resist residue on top of the graphene. However, we were able to largely remove this residue by atmospheric pressure annealing (3 hours at 340°C , 410 sccm Ar and 450 sccm H_2 in a 1" quartz tube).

We performed electronic transport experiments both before and after this annealing procedure. Devices were measured in a Desert Cryogenics probe station in the four-point probe configuration (source and drain current leads and Hall bar voltage sense probes), at a pressure of $\sim 10^{-6}$ Torr and at several temperatures between 4.2K and 300K. A small AC bias current ($\sim$100 nA peak, 17 Hz) is applied across the FET using the sine output of a Stanford Research Systems SR830 lock-in amplifier, and the resulting voltage difference between the sense leads is measured with the lock-in's A and B high impedance inputs. The gate voltage is applied with a Keithley 2400 sourcemeter. A schematic of the measurement setup is seen in figure 4.3, and plots of low temperature (4.2K) conductivity versus gate voltage for typical hBN- and SiO_2-supported devices (before and after annealing) are seen in figure 4.4.

The electron mobilities listed in figure 4.4 are obtained by a simple fit to the linear

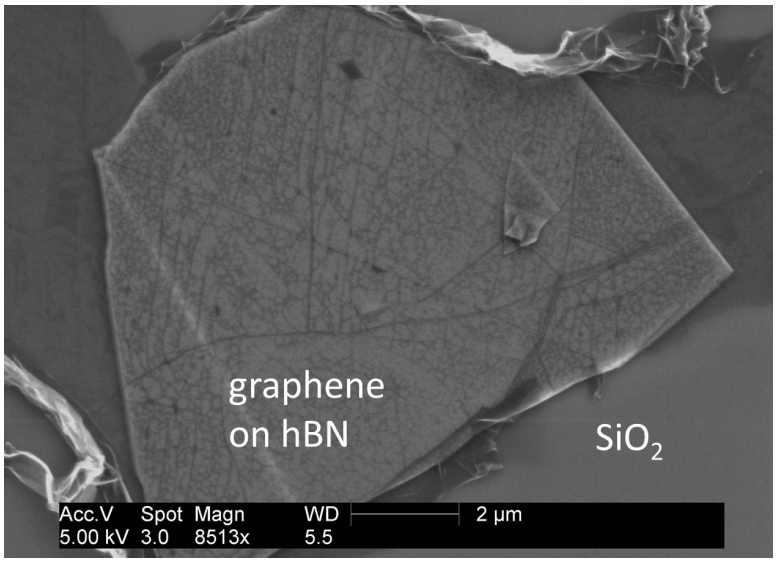

Figure 4.2: SEM image of contamination on graphene-covered hBN, reminiscent of a leaf's vein structure. Such features are not seen for graphene transferred to SiO_2.

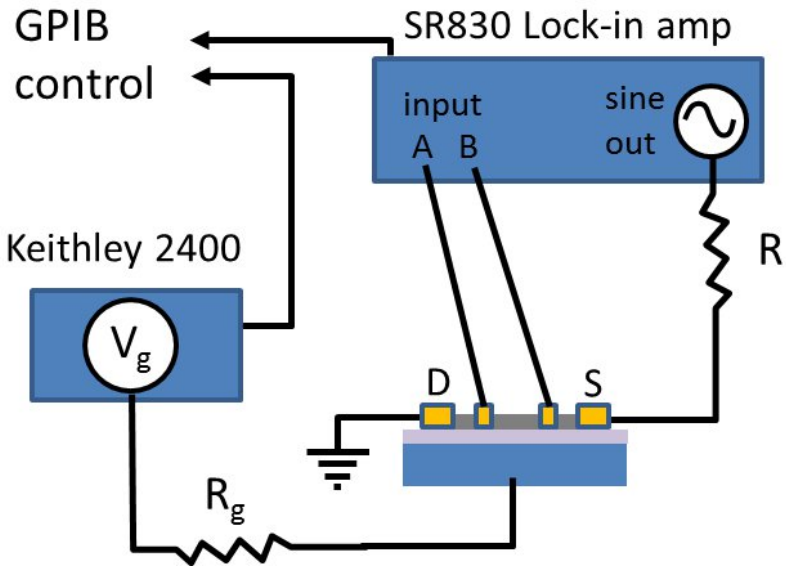

Figure 4.3: Measurement setup for gated graphene FETs

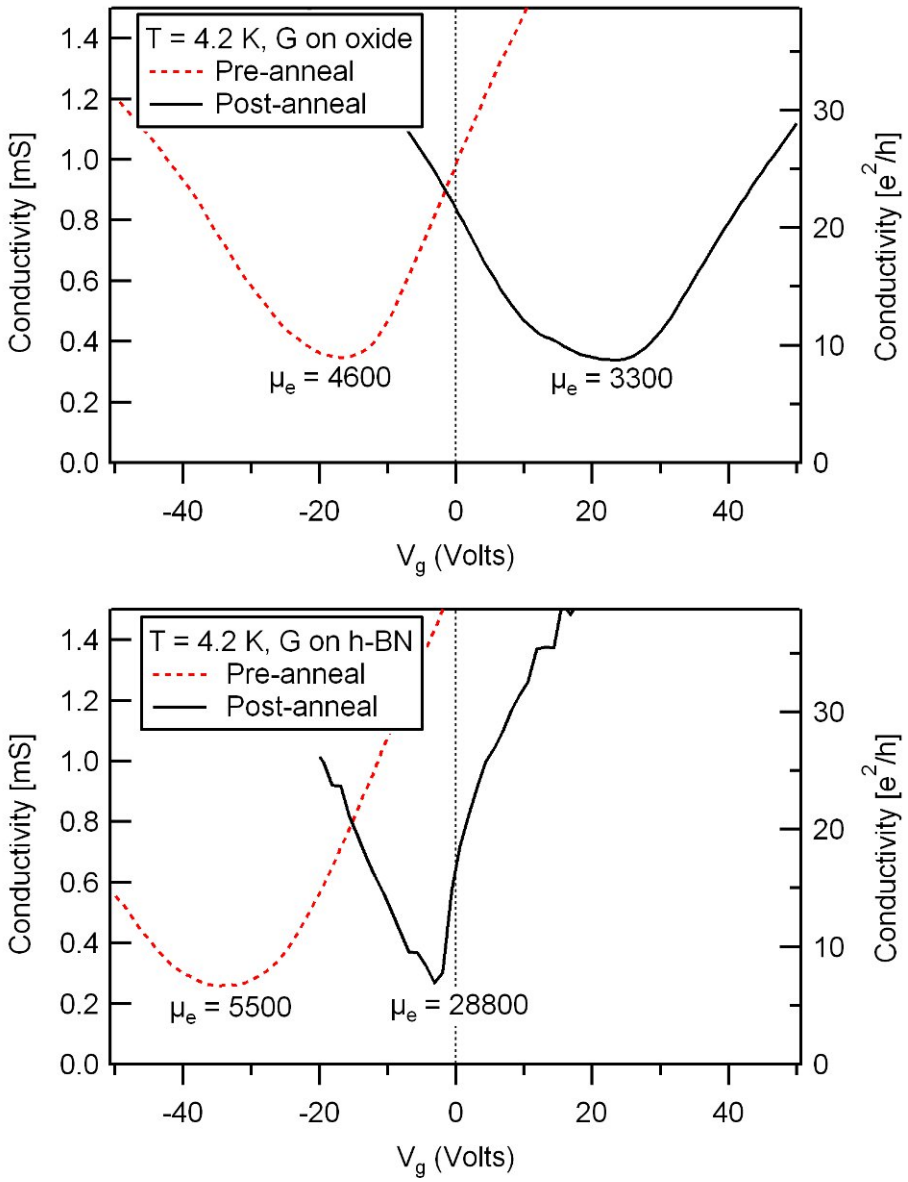

Figure 4.4: Conductivity versus gate voltage for hBN- and SiO_2-supported graphene FETs. (image from [34])

regime of the σ-V_g plot, as described in the beginning of this chapter. The specific capacitance for hBN-supported FETs was reduced appropriately, using $\epsilon_{hBN} \sim 4$ and using hBN thicknesses measured with AFM. Before annealing, SiO_2-supported FETs have μ_e of 4000–5400 cm^2/V-s and slight n-doping. After annealing, μ_e for these FETs drops a bit ($\sim$ 3000 cm^2/V-s) and they become strongly p-doped. However, while hBN-supported FETs start with similar μ_e before annealing (1900–5500 cm^2/V-s), their μ_e rise significantly after annealing, to between 9200–28800 cm^2/V-s. At the time of this experiment, these were by far the highest reported CVD graphene mobilities and were large enough to demonstrate that CVD graphene could already be made at sufficient quality to explore many physics phenomena (quantum Hall measurements, etc.).

One can also use a more sophisticated fit to separate the effects of Coulomb and short range scattering, giving

$$\sigma^{-1} = (ne\mu_c + \sigma_0)^{-1} + {\sigma_s}^{-1}$$

where μ_c is the contribution to mobility from Coulomb scattering, σ_0 is the residual conductivity at the Dirac point, and ${\sigma_s}^{-1}$ is the resistivity due to short range scattering [46]. Using this fit, we obtained μ_e up to 37000 cm^2/V-s for hBN-supported graphene FETs.

Gated conductance measurements and mobility calculations were repeated for many temperatures between 4.2K and 300K, both before and after annealing. These data, as well as corresponding plots of conductivity minima, are shown in figure 4.5.

The observed mobilities are fairly insensitive to temperature, with the slight increase at lower temperatures likely due to electron-phonon scattering. The sharp decrease between 4.2K and 6K may be due to cryosorption of contamination introduced by the stage heater (which is first turned on to heat up from 4.2 to 6K). Values of the conductivity minima, between 6 e^2/h and 8 e^2/h, are similar to those in the literature with weak intervalley scattering [17].

4.2.1 Additional comparisons of hBN and SiO_2 substrates

Besides measurements of electronic mobilties, additional evidence of the utility of hBN as a CVD graphene substrate was reported by collaborators in the Crommie group. Following up on their previous work (Yuanbo Zhang et al. [112]), Regis Decker and others in the Crommie group performed scanning tunneling microscopy and observed significantly reduced charge pooling and surface roughness for CVD graphene supported on our hBN substrates (relative to CVD graphene on SiO_2 substrates) [29]. This difference helps explain the greatly-reduced substrate-induced scattering for hBN-supported CVD graphene.

Additionally, we characterized hBN and SiO_2 supported graphene FETs with Raman spectroscopy, as seen in figure 4.6. The SiO_2-supported graphene has a negligible

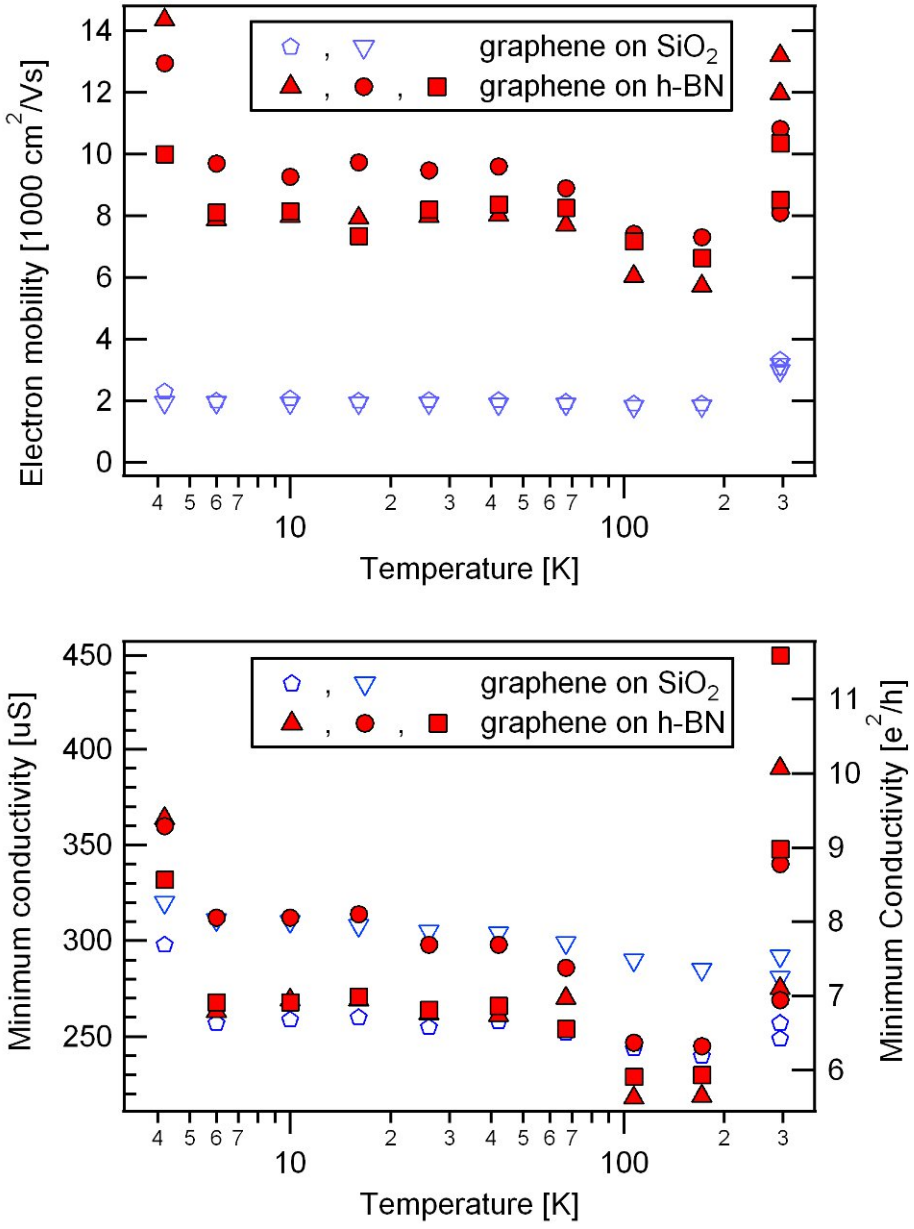

Figure 4.5: Mobilities and minimum conductivity for hBN- and SiO_2-supported graphene FETs (image from [34])

D peak and G and 2D peaks near expectations [30], at 1595 cm^{-1} and 2694 cm^{-1}. Graphene supported by hBN has G and 2D peaks at somewhat redshifted values of 1584 cm^{-1} and 2689 cm^{-1}, and the D peak is obscured by the strong G-like hBN peak at 1366 cm^{-1} (also where expected [38]). The softened G peak and enhanced 2D/G ratio for hBN-supported graphene is is consistent with reduced substrate-induced doping ([24]) and damping. This trend of increased 2D/G ratio reaches its limit for completely suspended graphene, as shown previously in figure 3.13.

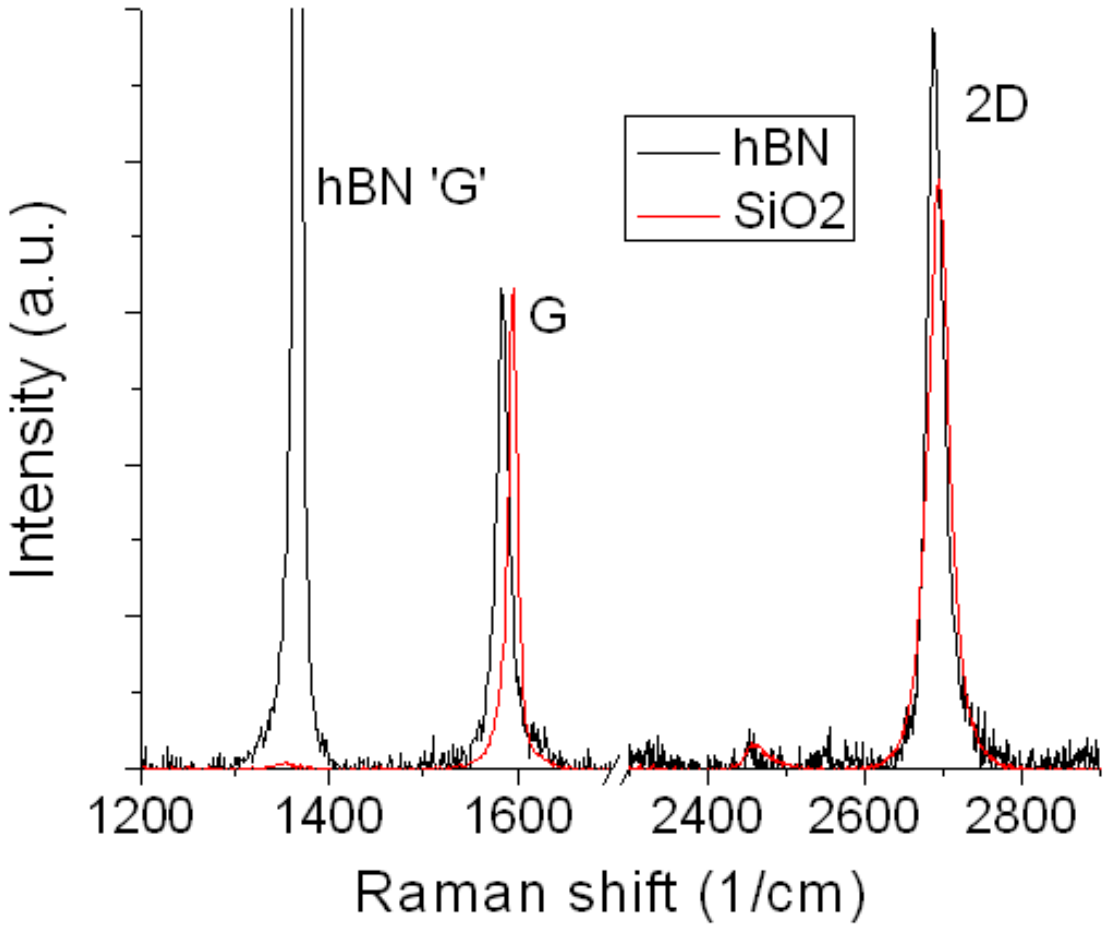

Figure 4.6: Raman spectra of hBN- and SiO_2-supported graphene

4.3 Graphene p-n junction

As described in the previous section, graphene field-effect transistors show different doping behavior on SiO_2 and on hBN. As-fabricated, graphene tends to be weakly electron-doped (n-type) on SiO_2 and strongly electron-doped (n-type) on hBN. After

atmospheric pressure annealing at 325°C in H_2/Ar, graphene tends to be strongly hole-doped (p-type) on SiO_2 and neutrally doped on hBN. This disparity presents an opportunity. In either the pre- or post-annealing case, a strip of graphene placed partially on SiO_2 and partially on hBN will exhibit a large difference in local doping. With the additional knob of electrostatic gating, these regions can be tuned to create n-n, p-p, or p-n junctions.

Graphene p-n junctions have a number of interesting applications, including fabrication of Veselago lenses (electron lenses)[15] and photodetectors and investigation of phenomena such as Klein tunneling. Previous efforts to make graphene p-n junctions have required difficult or finicky processes such as multiple electrostatic gates, proximity doping by polymers, or "electrical stress" in the substrate [19, 33, 59, 75, 78]. Our procedure, draping graphene over an hBN step, offers a simple and stable process for p-n junction fabrication. The process for fabrication of such devices (with one such device seen in figure 4.7) is performed as follows:

1. Prepare an array of Cr/Au alignment marks on 285 nm SiO_2 on Si wafer.
2. Exfoliate hBN onto SiO_2/Si wafer and calcine in air at 450°C for 3 hours to burn off tape residue.
3. Transfer CVD graphene to Si wafer and identify clean graphene on hBN regions near alignment marks in SEM.
4. Create NPGS pattern and selectively etch (via oxygen RIE) graphene, creating a strip of graphene partially supported by hBN and partially supported by SiO_2.
5. Lithographically define two point probe Cr/Au contacts.

The device was measured in a Desert Cryogenics four point probe station, at a pressure of 2 x 10^{-6} Torr and room temperature. A 1 µA peak AC current was applied with an Stanford Research Systems SRS-830 lock-in amplifier, and the resulting AC voltage was measured using the 10MΩ impedance SRS-830 input. A gate voltage was applied to the highly doped Si wafer through the 285nm thermally-grown SiO_2 with a Keithley 2400 sourcemeter. A plot of the device resistance versus gate voltage (figure 4.8) reveals two widely-separated Dirac points (the peaks in resistance at V_g =+55V and V_g =-27V), likely arising from the series-connected n-doped (hBN-supported) and p-doped (SiO_2) graphene regions.

As seen in figure 4.9, a slight difference was seen under some illumination (uncalibrated probe station light), as compared to dark conditions. However, we were not able to measure any appreciable photocurrent in the p-n junction regime (for instance, at zero gate voltage). Further research with more concentrated local light probes (e.g. a 1 µm diameter laser spot), may allow us to produce a measurable photo- or photothermal-response. The local stress induced by hBN step edge may also have an impact on the local electronic properties of the graphene.

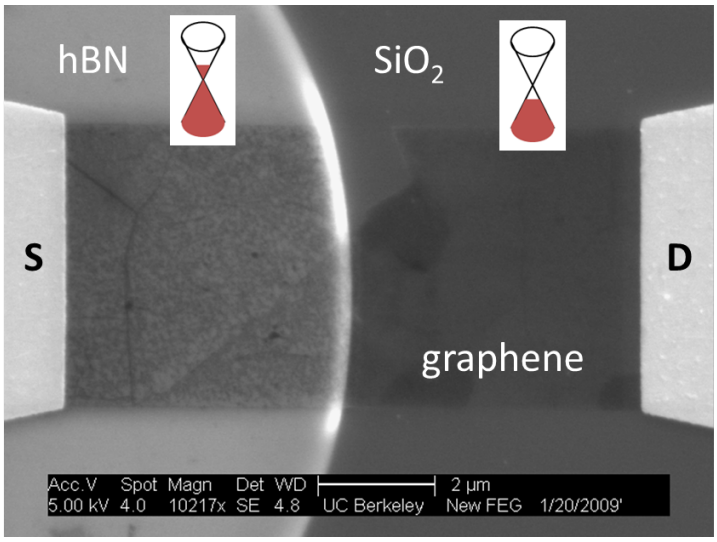

Figure 4.7: Substrate-induced (hBN and SiO_2) graphene p-n junction. The SiO_2-supported graphene tends to be p-doped and the hBN-supported graphene tends to be n-doped, as indicated in the band structure insets. Uniform back gating through the hBN/SiO_2 substrate can move the device into n-n, p-p, and p-n regimes. A small graphene tear and fold is seen in the top center of the p-n junction.

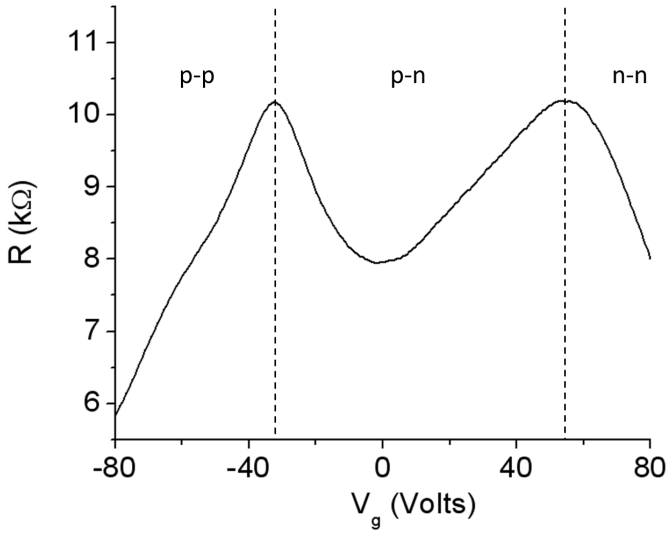

Figure 4.8: Resistance versus gate voltage for a graphene p-n junction (under zero illumination). Two widely-separated Dirac points are evident (peaks in resistance), arising from the n-doping of hBN-supported graphene and p-doping of SiO_2-supported graphene. Note: only one direction of sweeping is shown, but hysteresis was minor.

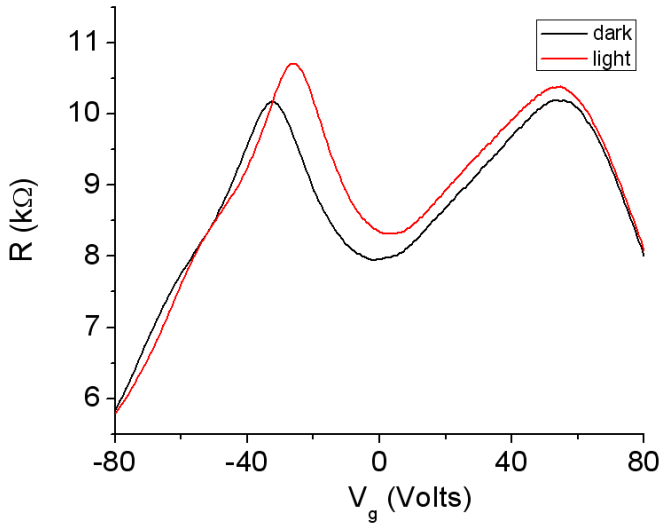

Figure 4.9: Resistance versus gate voltage for a graphene p-n junction (with and without illumination) There is a slight shift in Dirac points in the light (+55V,-27V) and dark (+53V,-33V), though this is within the scale of the hysteresis.

4.4 Graphene nanoribbons via BNNT etch masks

The graphene devices discussed so far have been in the 2D regime; the length and width of these devices have been fairly large (>1 µm). To approach 1D behavior, like that seen for single-walled carbon nanotubes, we need to shrink one of our in-plane dimensions down to the 10's of nanometers range, at which point confinement effects start to become significant. In this limit, one can open up a transport gap, which is vital for many electronic applications.[2]

Graphene nanoribbons (GNRs) have been synthesized in the past by a variety of means, including oxygen plasma etching with resist masks [41, 42], sonication of exfoliated graphite in PmPV [61][3], partial etching of resist-shielded carbon nanotubes [50], or "unzipping" of carbon nanotubes [56].

The electronic structure of GNRs starts to diverge from graphene as GNR width approaches tens of nanometers and, much like carbon nanotubes, depends both on the width and chirality[4] of the ribbon. From a simple 1D infinite square well model, one expects a confinement gap inverse with the width, and somewhat more sophisticated models in this vein initially seemed to match well with experimental measurements [42]. However, more recent work has shown that edge disorder (especially with oxygen etched ribbons) and substrate interaction (e.g. charge pooling from SiO_2 substrates)

[2]In practice, graphene nanoribbons made with lithography-defined oxygen etching may be dominated by hopping transport between disorder-induced local states.

[3]poly(m-phenylenevinylene-co-2,5-dioctoxy-p-phenylenevinylene)

[4]For instance, zigzag ribbons with H termination are shown to possess edge magnetism [92].

can lead to disorder-dominated transport, with the observed transport gap explained by Coulomb blockade through a series of quantum dots [41].

To better understand the intrinsic properties of GNRs, it is desirable to minimize as many extrinsic factors as possible, such as resist contamination and substrate charge puddle formation. To address these issues, we devised a 1D twist on our hBN-supported CVD graphene FETs – utilizing 1D boron nitride nanotubes (BNNT) [21]. To avoid resist contamination and provide at least a partial BN dielectric environment for GNRs, we used BNNTs as an etch mask to fabricate GNRs. We first spun down BNNT on graphene. After identifying regions where clean graphene was covered by straight BNNT, we proceeded to fabricate Cr/Au contacts at several points along the BNNT. After the deposition of the contacts, we performed a reactive ion etch with O_2 to remove graphene not covered by the BNNT or contacts. This resulted in an electrically-contacted graphene nanoribbon (GNR) with a width on the order of the BNNT diameter. The fabrication process for our BNNT-masked GNRs is represented schematically in figure 4.10.

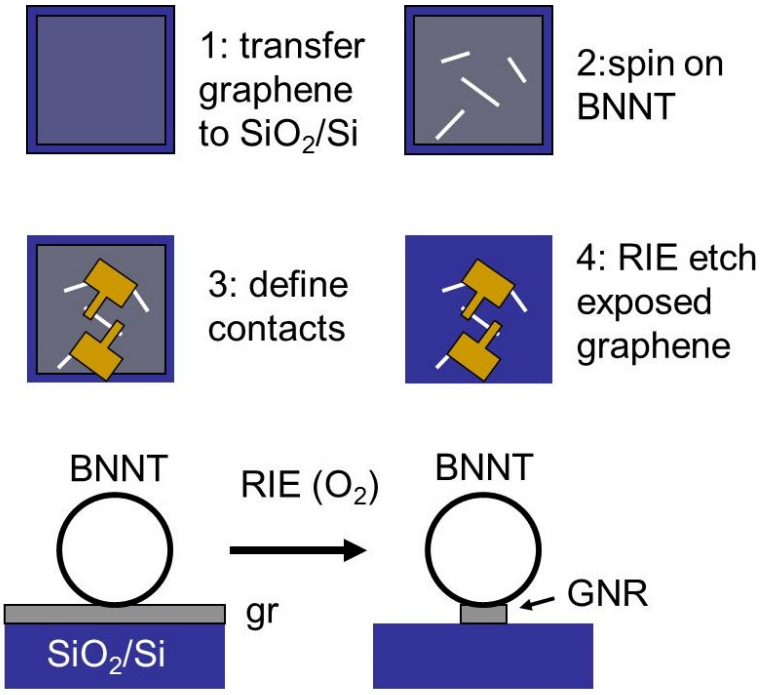

Figure 4.10: A graphene nanoribbon device made with a BNNT etch mask.

Using this process, we fabricated GNRs out of exfoliated and CVD graphene. Figure 4.11 shows a device fabricated using CVD graphene right before the reactive ion oxygen etch step. Graphene was supported by SiO_2 for these devices, but for future work hBN would likely be a much more ideal substrate; in this case, the

resulting GNRs would be entirely enclosed in a BN environment, with hBN below and BNNT above, minimizing substrate effects.

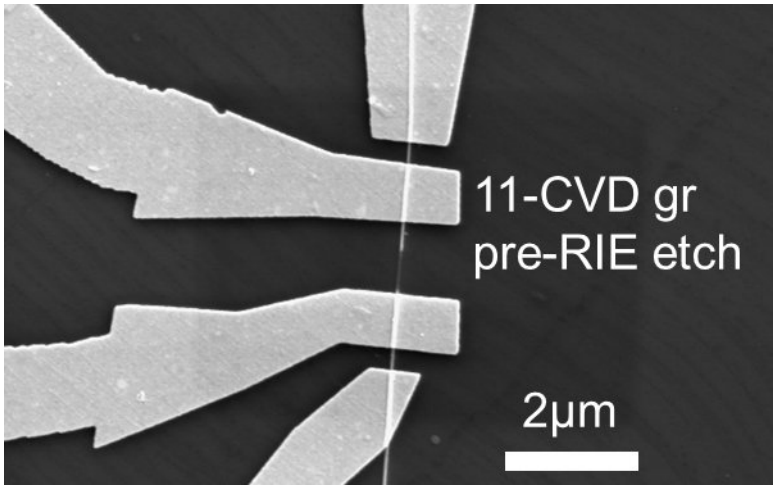

Figure 4.11: SEM image of BNNT-masked GNR FET, prior to O_2 plasma.

We performed 2-point, back-gated electronic transport on BNNT-masked GNRs at room temperature and at liquid N_2 temperatures (∼78 K), using the same cryogenic probe station and biasing/measuring setup as with our hBN-supported graphene FETs. A plot of resistance versus gate voltage for an exfoliated-graphene-derived GNR is shown in figure 4.12.

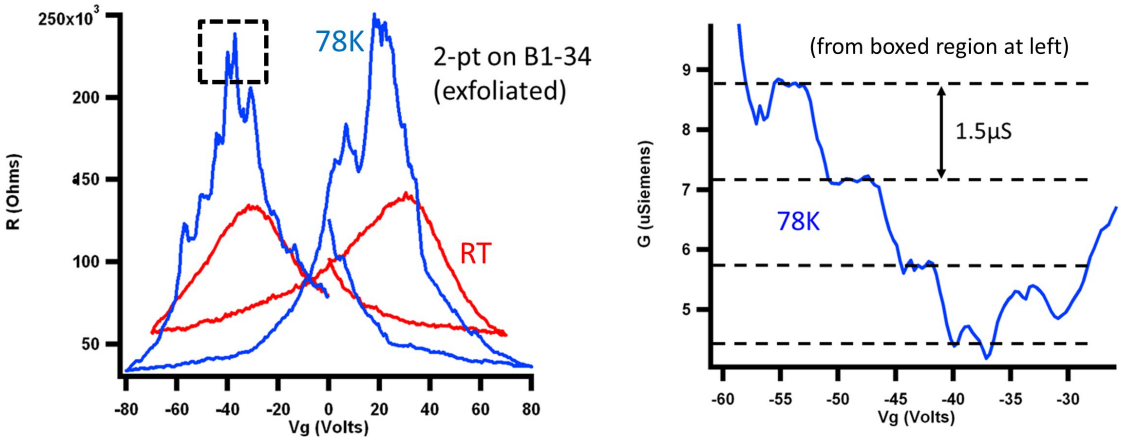

Figure 4.12: Resistance versus gate voltage for BNNT-masked graphene nanoribbon. Large hysteresis is seen at both room temperature and 78K. Equally-spaced conductance steps are seen at 78K, perhaps a sign of 1D subband formation.

The room temperature measurement looked fairly "normal," similar to a very resistive graphene FET (as would be expected for a very narrow, long channel) with

a lot of hysteresis due perhaps to mobile impurities. However, this hysteresis does not freeze out at low temperature (78 K) as we normally see, and we also see some unusual low temperature features in the resistance near the neutrality point in the negative gating regime. If we zoom in on this region (shown on the right in figure 4.12), we see conductance steps with a roughly equal spacing of 1.5 µS. These steps are much smaller than the 77 µS ($2e^2/h$, conductance quantum) steps seen for Landauer-Buttiker transport [25]. However, these conductance steps are very similar to that seen by Lin et al. for ∼30 nm wide GNRs oxygen etched with a polymer mask and are consistent with the onset of 1D subband formation [65]. We did not attempt to estimate mobilities for these devices, as the aspect ratio and effective capacitance are both hard to determine without removing the BNNT and an electrostatics simulation, respectively.

These devices and other quasi GNRs (bilayer grafold ribbons) are currently being studied by Will Gannett and Seita Onishi, and further details can be found in Will Gannett's PhD thesis, currently in preparation.

4.5 Grafold transport

Grafold, discussed in chapter 3, exists in a sort of middle ground between 1D and 2D. Grafold is embedded in graphene (2D), but the edges of grafold, with lots of highly strained sp^2 bonds, likely share some properties with carbon nanotubes. Additionally, for very narrow folds, the folded region itself could act as a mono-, bi-, or trilayer graphene nanoribbon, depending on the interaction between sheets.

This section will discuss cryogenic transport experiments performed on grafold FETs of two geometries, parallel and perpendicular. In parallel grafold FETs, the source-drain current (I_{SD}) runs parallel to the symmetry axis of the fold.[5] In perpendicular folds, I_{SD} runs perpendicular to the fold. This is shown in figure 4.13.

Device fabrication followed the same steps as that for standard graphene FETs, except that we intentionally aligned the graphene channel to run parallel to (and include) or perpendicular through a grafold, instead of avoiding folds as we previously did. A completed device is shown in figure 4.14.

Again similar to the methods used for graphene FET analysis, we performed electronic transport experiments (measuring resistance versus gate voltage) at room temperature and at low temperature (∼4K).

Figure 4.15 shows resistance versus gate voltage for a parallel fold device (sample F75). This device looks almost no different than a normal graphene FET, except that its peak resistance is about 1/3 that of a monolayer graphene FET of the same width. A reasonable explanation for this is that the bottom layer was gate modulated

[5]We are assuming that the relatively straight folds used in these experiments consist of a single recumbent fold with parallel folding axes; if the two folding axes were not parallel, the fold would not have a symmetry axis.

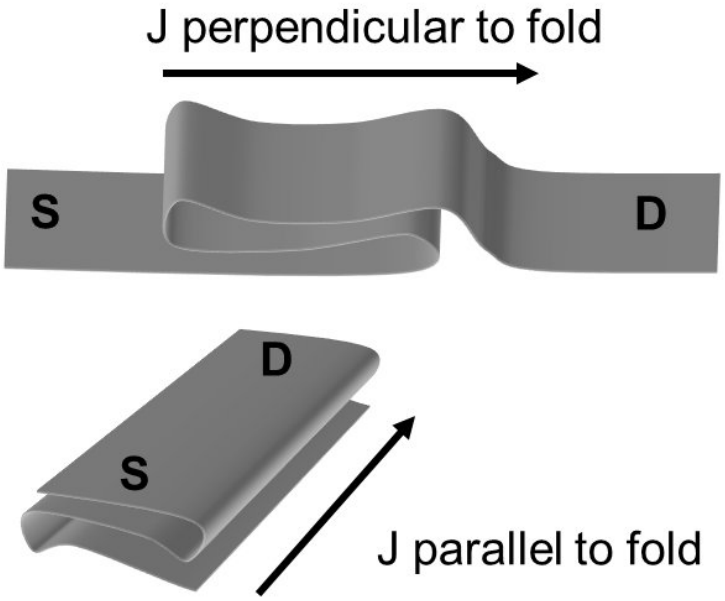

Figure 4.13: Parallel and perpendicular grafold FETs. In realistic devices, parallel folds will be embedded in a slightly wider graphene channel (as we cannot oxygen etch the graphene exactly up to the edges of the grafold). These FETs would sit on SiO_2/Si wafers to enable back-gating.

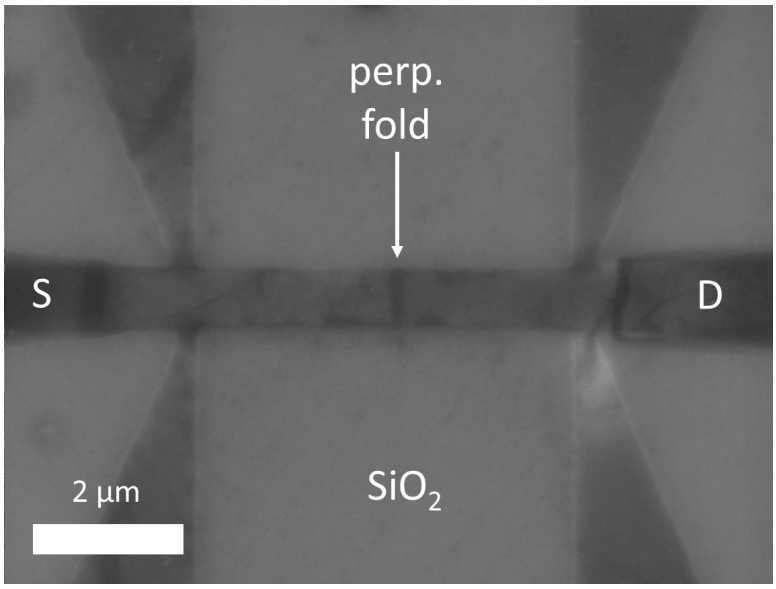

Figure 4.14: SEM image of perpendicular grafold FET (sample F41). The fold symmetry axis is aligned with the white arrow, perpendicular to I_{SD}. The graphene source, drain, and sense leads connect to Cr/Au contacts outside of the image.

as usual, and the resistance of the top two layers (or more, if this was a more complex fold) remained relatively unchanged due to partial screening of the electric field by the bottom layer. Additionally, any unusual electronic behavior in the parallel fold may be shorted out by the finite width of monolayer graphene on either side of the fold.

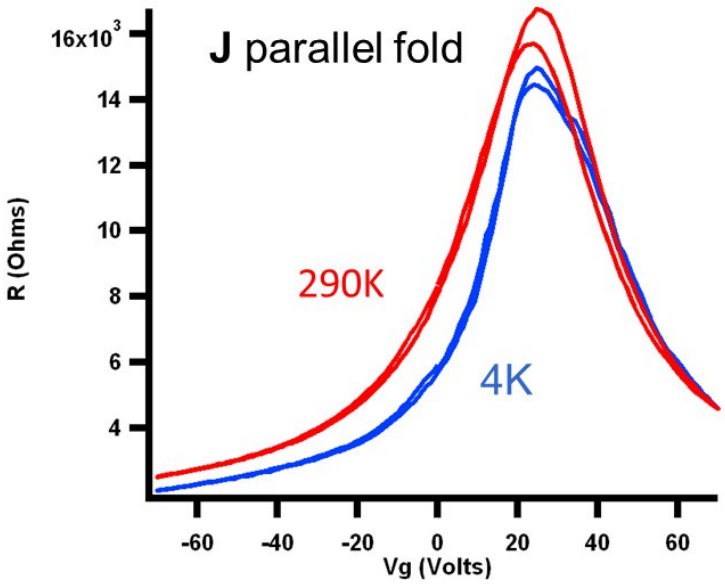

Figure 4.15: R-V_g for parallel grafold FET

The perpendicular fold is somewhat more interesting as current is *forced* to travel through the fold, though the overall contribution to the FET resistance will likely be smaller as the perpendicular fold only accounts for a few % of the total FET channel length. Resistance versus gate voltage for a perpendicular fold (sample F24) is seen in figure 4.16.

At room temperature, the perpendicular grafold FET is indistinguisable from a graphene FET of the same width. However, at T = 4K, we see somewhat noisy but repeatable features near the charge neutral point. These unusual jumps in resistance are reminiscent of the subband formation we observed with graphene nanoribbons, and may be related to the quasi-1D edges on both sides of the fold.

More control over this system is needed to extract meaningful conclusions. In these devices, the detailed structure of the fold is not entirely known, and the layer interaction at folds may vary considerably due to varying amounts of PMMA or other contamination. Future studies could intentionally decouple layers with a known thickness of insulating intercalants. For such devices, the exact current pathway through the fold could be determined.

Intrinsic or intercalated grafold FETs may also offer a pathway to another interesting system – bilayer nanoribbons – as will be discussed next.

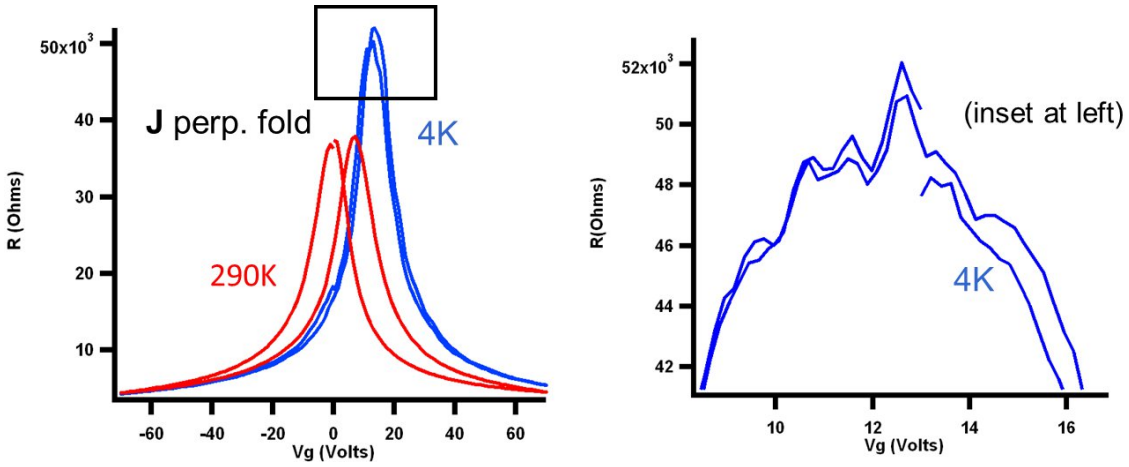

Figure 4.16: R-V_g for perpendicular grafold FET, showing unusual low temperature behavior near the Dirac point.

4.5.1 Grafold to nanoribbons via fluorination

Another exciting possibility is to use grafolds as a kind of mask to create high quality bilayer graphene nanoribbons. Oxidation is a fairly destructive process, permeating multiple layers at a time. However, one can fluorinate few layer graphene, turning only the top layer into the insulator "fluorographene" [72, 111]. Thus, a fluorinated single recumbent grafold embedded in an otherwise flat graphene monolayer can be transformed into an bilayer graphene nanoribbon with a monolayer fluorographene covering. This is currently being studied in the Zettl group by Will Gannett and Seita Onishi, and details of this experiment will be found in Will Gannett's PhD thesis (currently in preparation).

Chapter 5

Synthesis methods and other research

5.1 Magnesium diboride

Magnesium diboride (MgB_2) is the highest temperature type I superconductor known, with a T_c of nearly 40 Kelvin [20]. Additionally, MgB_2 has a layered structure, potentially opening up the possibility of exfoliating very thin layers, and thus potentially allowing one to tune carrier concentration and dependent properties such as T_c with a gate. To investigate this possibility, I obtained high purity MgB_2 flakes from Paul Canfield at Ames Laboratory.[1] Exfoliation of these crystals (seen in figure 5.1) was attempted using Scotch tape, super glue (cyanoacrylate), and scraping with razor blades. However, the strong interlayer bonds resulted in poor cleaving, preventing the production of usable areas of thin flakes.

A more promising route to large area thin films may be bottom-up growth, introducing Mg vapor to a solid boron substrate or vice versa. All methods of preparation must also contend with the oxidation of freshly exposed MgB_2 surfaces, on which MgO forms within hours of exfoliation, as shown by EDAX of fresh and oxidized surfaces in figure 5.2.

5.2 Carbon nanotubes

Carbon nanotubes are quasi-1D structures that are formed by cutting out a rectangle of graphene and wrapping it into a closed cylinder [47]. The width and angle

[1] In-house growth was also attempted, using Mg and B powder (with a slight stoichiometric excess of Mg to balance its volatility) sealed in tantalum tubing. The tantalum tube with Mg and B powder was cold welded shut in an inert environment (Ar glove box) and placed in a quartz tube in a chemical vapor deposition furnace. The tube was heated at 850°C for an hour. This method was never successful, as the chamber would split open and allow oxygen to form MgO or boron oxides.

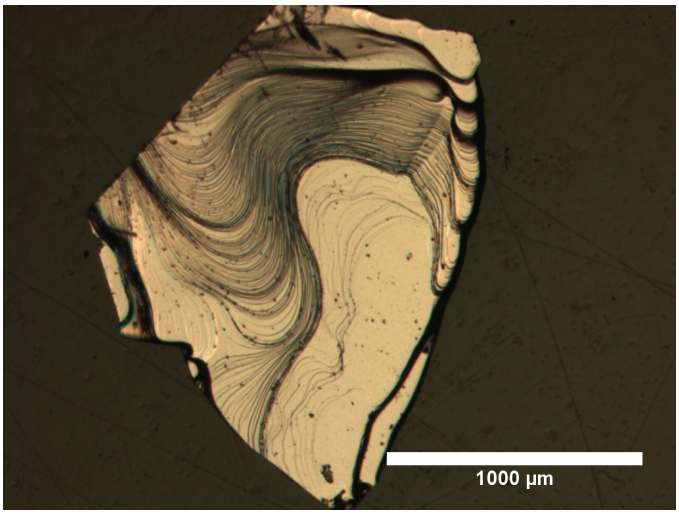

Figure 5.1: Optical micrograph of MgB_2 single crystal. The layered structure is seen in the contour-like curves.

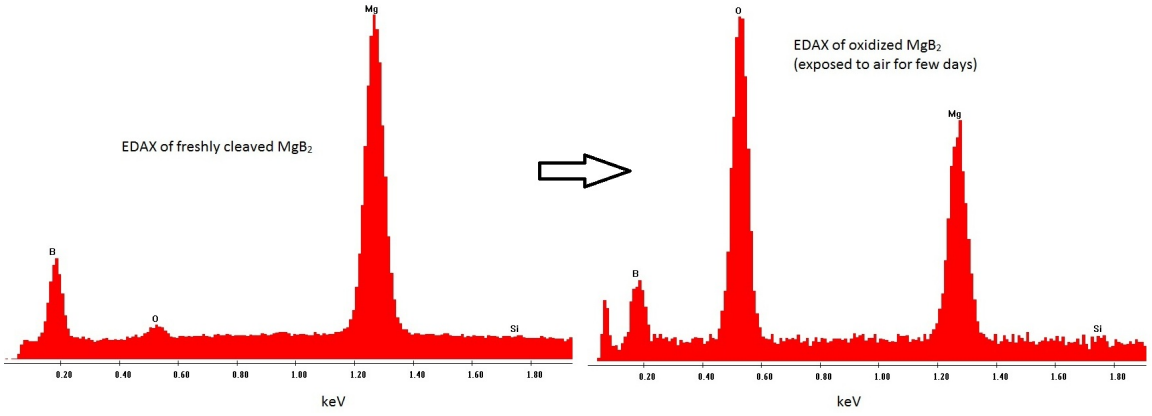

Figure 5.2: EDAX of freshly cleaved and oxidized (in room air for days) MgB_2 surfaces

chosen to form this rectangle define the chirality, which determines the diameter and twist of the nanotube. Figure 5.3 shows the chiral vector, a sum of integer multiples (n,m) of the graphene lattice vectors, for a general carbon nanotube.

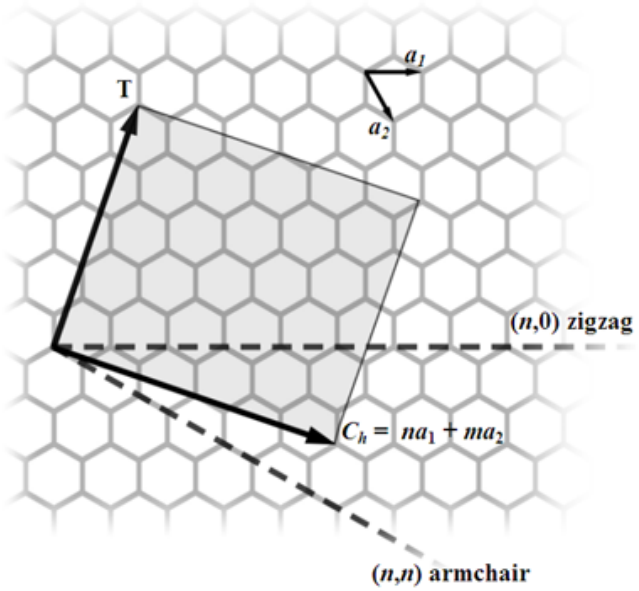

Figure 5.3: Chiral vector **C** of a carbon nanotube. **T**, normal to **C**, denotes the tube axis (image source: wikipedia.org)

Chirality determines the electronic behavior of a single walled nanotube, which can either be metallic if (n-m)/3 is an integer or semiconducting with a bandgap of up to about 1 eV for the smallest diameters [102]. Thus, selection of specific chiralities is crucial for most electronic applications of nanotubes. Unfortunately, most synthesis methods require high temperature catalysis from transition metal nanoparticles (Ni or Fe), and even initially very monodisperse nanoparticles tend to fluctuate in size and shape at these high temperatures (for example, by Ostwald ripening). Chirality is strongly affected by the nanoparticle size and facet structure, so it is suspected that catalyst-grown nanotubes may never be able to be grown with a single chirality [44]. Much effort is instead focused on ways to separate chiralities after synthesis, but the tendency of single-walled tubes to bundle presents additional problems. Thus, an alternate growth method which could preferentially select for certain chiralities would be desired.

5.2.1 Controlled chirality nanotubes

One such method of controlling chirality is to chemically synthesize defined chirality seeds ("carbon nanohoops") which can then be stitched together or extended

into a long tube. Working with Dr. Ramesh Jasti (formerly of the C. Bertozzi at UC Berkeley and now an assistant professor at Boston University), we attempted to take such seeds (specifically [9]-,[12]-, and [18]-cycloparaphene) and extend these into armchair nanotubes of varying diameters. A schematic of this process for both armchair and zigzag nanotubes is shown in figure 5.4.

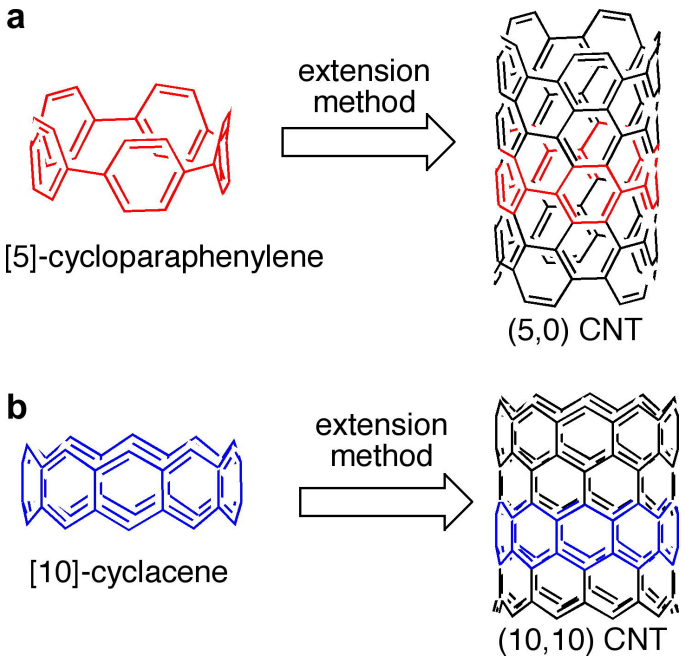

Figure 5.4: Stitching of carbon nanohoops into armchair or zigzag CNT. (image from Jasti et al. [49]).

Before attempting synthesis with these molecules, which have extremely high built-in strain energy, thermogravimetric analysis (TGA) was performed to get some sense of their temperature stability. A solution of [12]-cycloparaphenylene in CH_2Cl_2 solvent was dried in the TGA's Pt basket until 17 µg of the molecule was in the basket. The basket was then gradually heated to 900°C in atmosphere (80/20 N_2/O_2) while recording the mass. Results are shown in figure 5.5.

The seeds appear to have similar robustness (no significant mass loss below 500° C) to other sp^2-bonded carbon materials, though the mechanism behind the initial rise in mass is not clear. Further experiments by Dr. Jasti showed degradation in the molecule's fluorescence (arising from of its ring structure) after heating above 300° C. Given these bounds on stability, we subjected the seeds to a variety of synthesis procedures, as follows:

1. Solution-based methods: sonication, Bechgaard salt growth (following [6])
2. Regrowth of single-walled CNT via CVD (following [105])

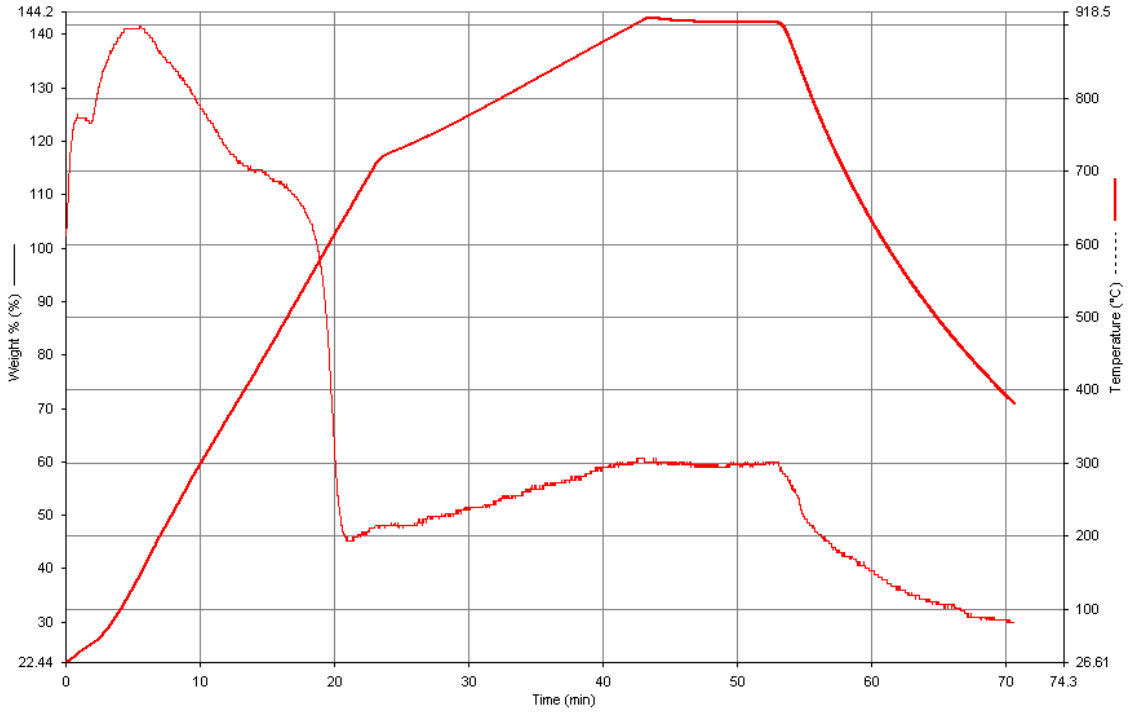

Figure 5.5: Thermogravimetric analysis of 12-cycloparaphenylene. An initial rise in mass at low temperature may be due to partial oxidation after loss of hydrogen termination. The molecule starts to decompose significantly above 500°C which is consistent with many other sp^2-bonded carbon materials.

3. Regrowth using plasma-enhanced CVD (using a modified version of the above CVD recipe)

4. Vapor transport (following Zettl group procedures for C_{60} single crystal growth)

Most of these methods did not appear to produce crystalline products. CNT did grow with CVD methods, but were multiwalled; it is likely that the seeds were simply decomposed by the catalysts. However, we noticed that needle-like clusters formed as the CH_2Cl_2 solvent gradually evaporated. We redissolved these needles in CH_2Cl_2 and spin-coated them onto lacey carbon TEM grids for analysis. A TEM image of one of these needles is seen in figure 5.6.

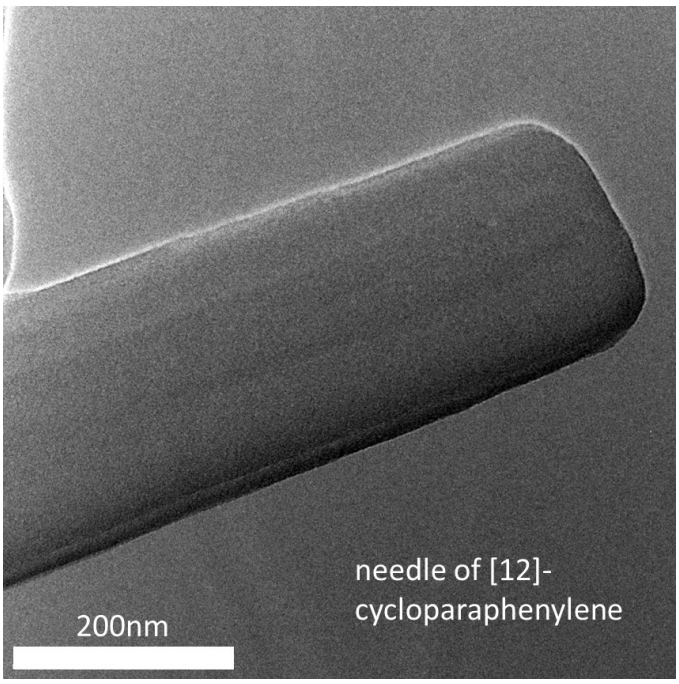

Figure 5.6: TEM image of a 12-cycloparaphenylene needle. Imaging performed by Dr. Nasim Alem using the Zettl group's Jeol 2010 TEM.

Recent work by Dr. Jasti has suggested that single crystals of cycloparaphenylene tend to form into straight bundles of armchair-stacked nanotubes [49], which may be consistent with the needle structure we observed. Such a structure, if one could covalently bond the molecules within the single nanotubes, would be close to the goal of controlled chirality growth, though the issue of unbundling remains challenging. Dr. Jasti is continuing this work at Boston University.

5.2.2 Patterned carbon nanotubes via Co abrasion

In addition to chirality control, simple methods of patterning and placing carbon nanotubes are an important step for practical CNT electronics. Cobalt has been shown to be an excellent catalyst for growing ultralong single-walled carbon nanotubes [45]. In addition, Co can be abraded onto many surfaces. We used this property and abraded Co onto a SiO_2/Si substrate, thereby creating patterned Co catalyst as simply as drawing on paper with a pencil (following stainless steel abrasion by Alvarez et al. [3]). After patterning, we performed CVD growth of ultralong CNT by Co-catalyzed decomposition of ethanol at 850°C , following a recipe developed by Huang et al. [45]. As seen in figure 5.7, long and fairly dense CNT are seen emerging from the long strip of Co catalyst. This method provides a simple way to pattern and grow CNT without the need for lithography and Co evaporation.

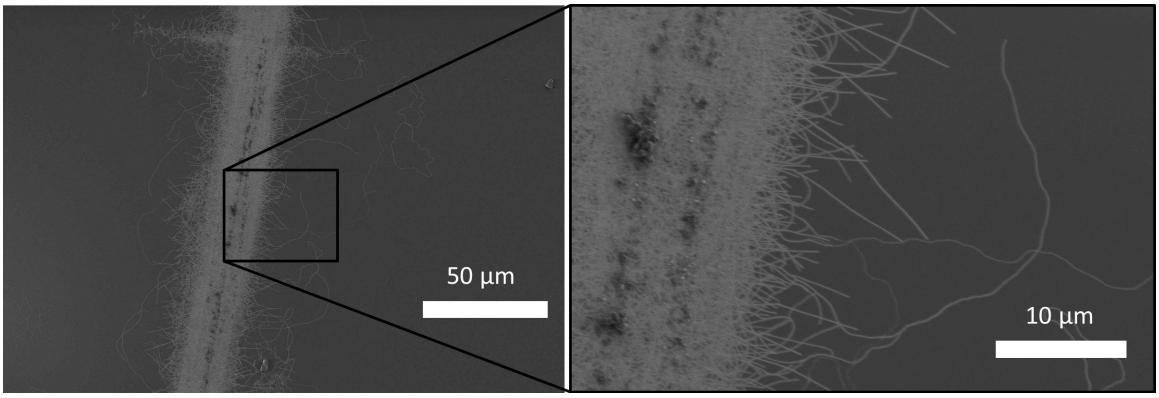

Figure 5.7: SEM of CVD-grown SWCNT with abraded Co catalyst

5.3 Alternate methods of graphene synthesis

5.3.1 Graphene exfoliation

Exfoliation of graphite was used in 2004 by Geim and Novoselov to create the first isolated graphene monolayer on an insulating substrate [74].[2] Though more recently-developed methods (namely CVD) are used to create much larger polycrystalline graphene sheets, exfoliation is still used to create the highest quality monolayer graphene samples, with mobilities up to 200 m^2/V-s [28].

This method requires only a few steps – substrate preparation, graphite exfoliation, and identification of monolayers. Some of the best results have been achieved

[2]Growth of few-layer graphene on silicon carbide was developed by Berger al al [8] at a similar or slightly earlier time than exfoliation, but this graphene was somewhat more difficult to work with and was not as widely used.

with Kish graphite, a byproduct of steel-making. Highly oriented pyrolytic graphite (HOPG) may also be used, but smaller monolayer flakes typically result (ironically) due to the reduced impurities compared to Kish graphite. Sources for these and other types of graphite can be found in Çağlar Girit's PhD thesis [36]. The procedure for exfoliation is as follows:

1. Piranha etch SiO_2/Si substrate, rinse with deionized water, blow dry, and heat on hot plate at 100°C for a few minutes to drive off residual water.

2. Stick a small flake of graphite (few mm diameter, 0.1mm thickness) on a strip of 3M Scotch tape and exfoliate 10-15 times, or until the tape is uniformly covered with a light gray coating of thin flakes.

3. Remove the Si substrate from the hot plate and allow to cool for 20 seconds, and then stick the tape to the surface. Press the tape down with a rubber eraser to ensure uniform contact. Leave the tape on the substrate for at least a day to improve graphene yield and decrease tape residue.

4. Peel the tape at a 90° angle relative to the substrate, while pressing down the edge of the tape with the blunt side of a razor blade.

5. Identify flakes in the optical microscope, with Raman spectroscopy, etc. Green contrast should be approximately 7% for a monolayer on 285 nm of SiO_2.

Optical contrast between thin graphene layers and SiO_2 is most apparent on 90 or 285 nm SiO_2/Si. A thin region of exfoliated graphene on 285 nm SiO_2 is seen in figure 5.8. The boxed region is estimated to be bilayer graphene, based on the observed 14% green contrast (7% per layer).

After optical identification, layer thickness can be confirmed by Raman spectroscopy (as described in chapter 3) or by other means such as atomic force microscopy. To fabricate devices with identified graphene, samples are mapped by taking a series of optical micrographs at various magnifications. After coating samples with PMMA resist for electron-beam lithography, small scratches can be made in the resist to serve as alignment marks.

5.3.2 CVD growth of graphene on Cu and hBN thin films

As discussed in chapter 3, graphene can be grown by chemical vapor deposition on Cu substrates. However, so far we have only discussed growth on thick Cu foils. One can also grow graphene on thin Cu films, with these thin films supported by other substrates, using a nearly identical CVD recipe. Thin film growth presents one new challenge – dewetting of the Cu at the high growth temperature. However, this dewetting can be minimized by careful substrate choice and reduced time at high temperature. Dewetting may also offer an advantage – allowing Cu to dewet

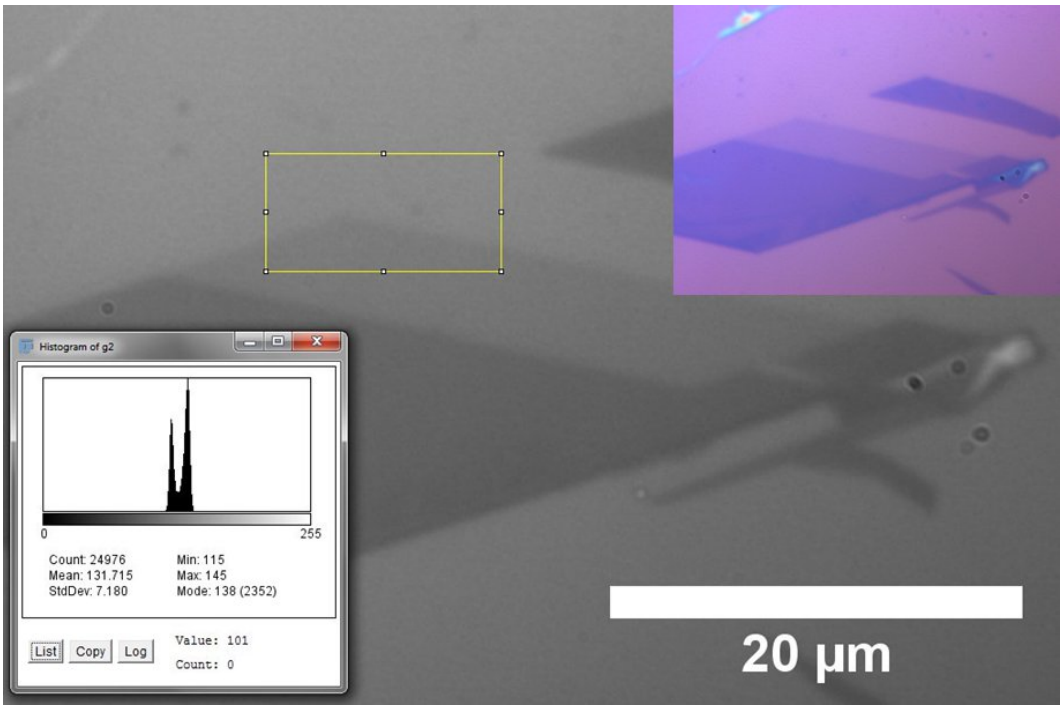

Figure 5.8: Thin exfoliated graphene on 285 nm SiO_2. The large image is the green layer of an RGB stack (using ImageJ), and the original color image is shown in the upper right. A histogram of the boxed region reveals approximately a 14% contrast difference between the graphene and bare SiO_2, consistent with bilayer graphene.

and recede after graphene growth to deposit graphene directly onto an underlying dielectric substrate, as reported by Ismach et al. [48].

Graphene CVD on Cu thin films

We performed graphene growth on Cu thin films (thickness from 300nm–2µm) on a variety of substrates (c-cut sapphire, quartz, and thermally-grown SiO_2 on Si). To minimize dewetting, we pushed the substrate into the furnace hot zone (kept at a slightly cool 975°C) and retracted it immediately after growth (10 mins with 10 sccm H_2 and 35 sccm CH_4). This sample movement can be accomplished by a boat on a magnetically-coupled rod or by using a long quartz tube and sliding the furnace back and forth (with the latter method a bit more dangerous). Significant dewetting is observed for SiO_2 and quartz substrates, along with pitting caused perhaps by carbo-thermal decomposition ($SiO_2 + C \rightarrow SiO + CO$). Fairly minimal dewetting is observed with thicker Cu substrates (500nm or thicker) on c-cut sapphire, and no etch pits are seen.

Graphene CVD directly on hBN

In addition to Cu substrates, we attempted direct growth on exfoliated hBN on SiO_2/Si, a method with some precedent in the literature [91]. As discussed in chapter 4, hexagonal boron nitride (hBN) is an excellent substrate for graphene. To avoid the need for separate graphene and hBN growth and transfer, it would be preferable to be able to grow graphene directly on hBN. We performed low pressure CVD growth at 1000°C with 10 sccm H_2 and 40 sccm CH_4 on hBN/SiO_2/Si. Unfortunately, we only observed some slight amorphous carbon deposition on the hBN.

Dewetting thin Cu (on hBN) for graphene on hBN

We were able to semi-directly deposit graphene on hBN using a combination of these two prior methods. We first exfoliated hBN onto SiO_2/Si or c-cut sapphire wafers and then coated everything with thin films (300 nm) of Cu. We performed the two-stage graphene CVD growth (shown in figure 3.4) at a slightly lower temperture of 980°C . After growth, we annealed at a higher temperature (∼1000°C) for about 30 minutes to encourage Cu dewetting and evaporation. As the Cu recedes and evaporates, graphene grown on the Cu thin film falls onto the exfoliated hBN flakes. hBN did not appear to react with SiO_2, Al_2O_3, or Cu at these temperatures. Results are shown in figure 5.9 for sapphire substrates.

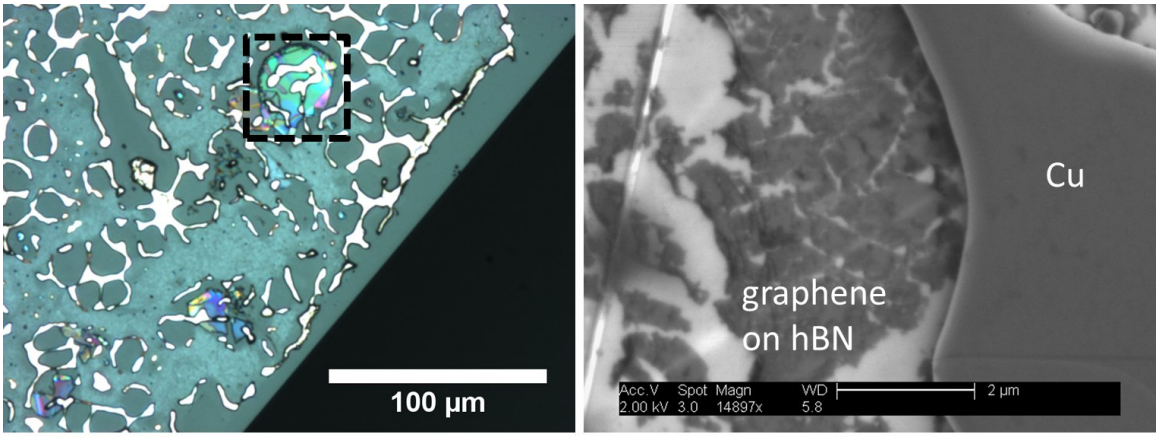

Figure 5.9: Graphene on hBN enabled via Cu dewetting. Graphene is grown on thin film Cu on hBN/sapphire. After growth, a higher temperature annealing step causes the Cu to recede and evaporate. An optical image of the sample after annealing is shown on the left, with a large graphene-covered hBN flake highlighted in the boxed region. On the right is an SEM image of a typical hBN flake with high graphene coverage (darker regions) and some remaining Cu.

This work provides a simple method for obtaining very clean graphene on hBN. However, since dewetting is somewhat difficult to control, we also developed an additional method for creating relatively clean thin film Cu grown graphene on dielectric substrates which only requires on lithography step, which is described in the following section.

5.3.3 One-step graphene devices on thin copper films

One of the drawbacks of CVD-grown graphene is that growth must be performed on metal substrates; for almost all electronic applications, the graphene must be transferred off of this substrate to avoid shorting. However, growth of graphene on very thin (few hundred nanometer thick) metal on insulating substrates opens up an alternative device fabrication procedure. By exploiting the isotropic nature of Cu wet etching, we can completely underetch the graphene in certain areas and maintain contact with Cu in other areas, as shown in figure 5.10. This method requires only a single lithography step, such as a "bowtie" pattern (where the contacts are wide and the central graphene channel is narrow) so that graphene/Cu contact is maintained in the wide regions. After lithography and developing, reactive ion etching is performed to etch through the exposed graphene. Then the Cu is wet etched, freeing graphene in the narrow regions; it should be noted that graphene channels can be made arbitrarily narrow by this method, but the channel length will be a minimum of twice the Cu thickness (due to the isotropic nature of the etching). This method was developed with Will Gannett, and similar work was reported by Levendorf et al. [60].

In addition to time savings due to minimal preparation steps, this method can potentially produce cleaner devices than typical fabrication procedures (as described in previous chapters) which require a transfer step, patterning step, and often a third, aligned contact deposition step. To demonstrate this method, a four probe van der Pauw device was fabricated (also shown in figure 5.10) using CVD graphene grown on 500nm Cu on a polished c-cut sapphire wafer. Graphene growth was performed at a somewhat low temperature of $\sim 975^{\circ}$C to minimize dewetting; some pinholes are still present, as seen in the device in figure 5.10. Despite the advantages (speed, cleanliness) of this method, dewetting of thin film Cu currently limits useful application to crystalline sapphire substrates. Bottom-gating, as is commonly performed using thin thermal SiO_2 on doped Si, cannot be performed as easily through these thick sapphire substrates.

5.4 Chalcogenide growth via Bridgman technique

Much research in the Zettl group is focused on the unique properties of 2D layered materials, previously charge density wave (CDW) materials and layered superconductors and more recently graphene and hBN. For sufficiently thin semiconducting or

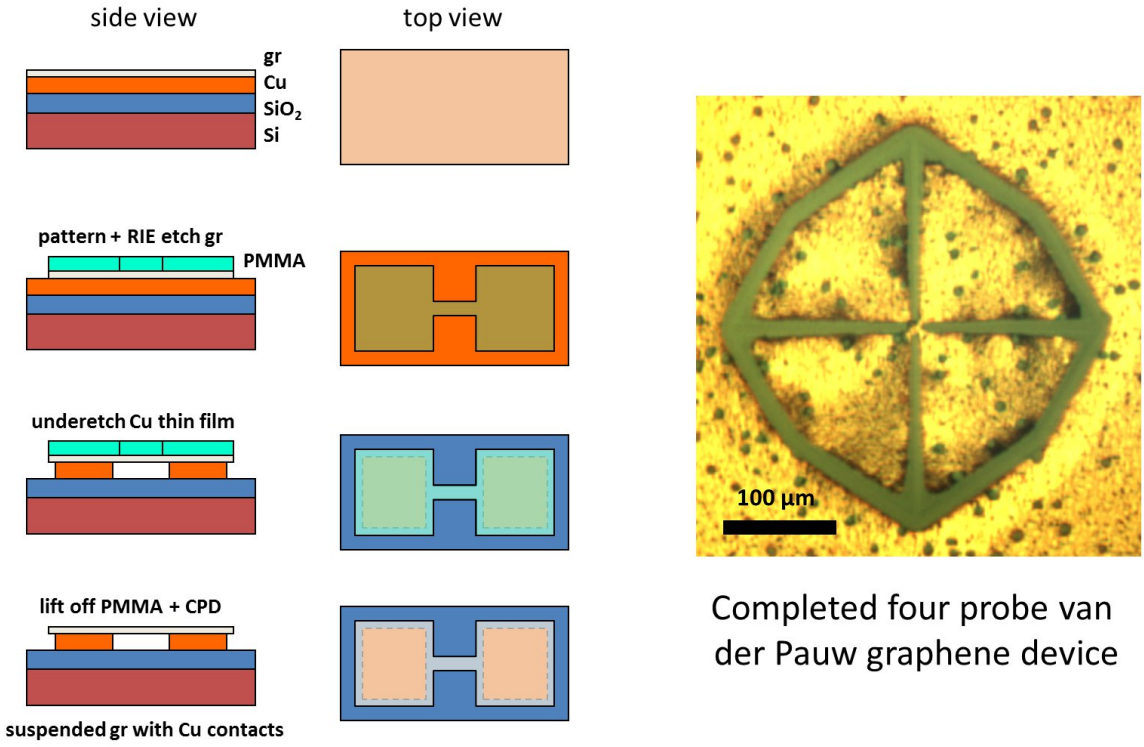

Figure 5.10: At left, the process is shown for single-lithography-step CVD graphene devices using underetching of thin Cu growth substrates. A resulting four probe van der Pauw graphene device is shown on the right. Etched areas are shown in grey, and the resulting graphene channel is located at the center of the four triangular Cu contacts. Some dewetting of the Cu during graphene growth is evident in the pinholes.

semimetallic samples, electric field gating is able to drastically change the charge carrier concentration throughout the entire sample, allowing one to tune properties such as T_C. Additionally, band structures can dramatically change as sample thickness approaches a few layers, as seen in the case of graphite and graphene. Recent studies have shown that the chalcogenide MoS_2 can change from an indirect to a direct gap semiconductor as it is thinned to a monolayer [93].

In the context of the SFPV studies (chapter 2), we were interested in the properties of two such layered semiconductors, gallium (II) selenide (GaSe) and tin (II) sulfide (SnS). GaSe has an indirect gap at 2.1eV and has been studied in past decades for its nonlinear optical properties. We were interested to see if, like MoS_2, GaSe would change bandgap size and type as it was thinned to the monolayer. SnS, as mentioned in chapter 2, has a direct gap at around 1.2–1.3 eV.

Single crystals of both of these materials can be grown with a variation of the

Bridgman technique, in which amorphous or polycrystalline material is heated above its melting point and recrystallizes on a seed in a slightly cooler area. Precursor materials are placed in quartz ampoules with one closed end. The open end is pumped on with a turbo vacuum until the pressure reaches approximately 10^{-5}–10^{-6} Torr. In some cases, the ampoule is back filled with a small amount of Ar or I to aid in vapor transport. The ampoule is then sealed using a H_2/O_2 torch while continuing to pull on the volume with the vacuum.

5.4.1 Gallium selenide (GaSe) growth

Gallium selenide was grown by me and Will Gannett following a technique developed by Voevodin et al. [97], seen in figure 5.11. A quartz ampoule with Ga on one end and Se pellets on the other is sealed at 10^{-5} Torr. (In our growth, 0.35 g Ga and 0.31 g Se were sealed in a 1/4" inner diameter quartz tube.) Due to the high vapor pressure of Se, the first step vaporizes the Se at a temperature where its vapor pressure would not fracture the ampoule and allows the Se to safely alloy with the Ga. Once this is complete (about 16 hours), it is safe to raise the temperature (as there is little unalloyed Se left). Next, the temperature is uniformly elevated, and then a slight temperature gradient is developed to cause large single crystal GaSe to eventually form (after several days) on the slightly cooler end.

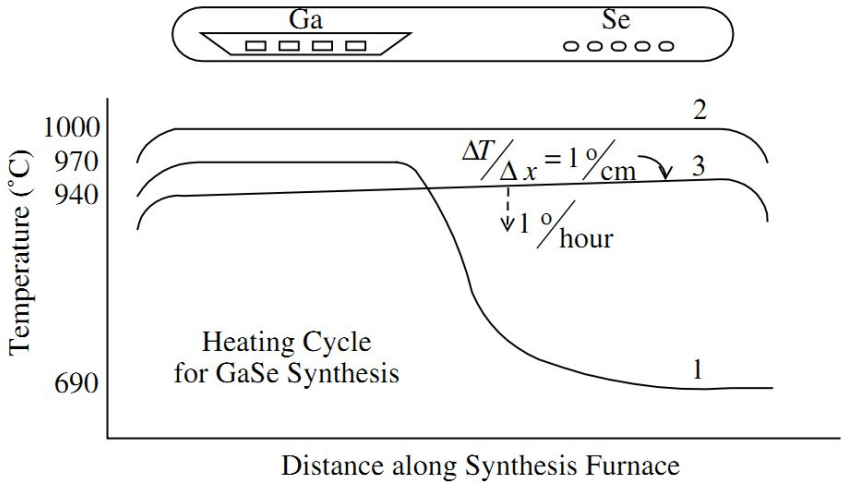

Figure 5.11: Gallium selenide synthesis recipe (image from Voevodin et al. [97]). In our synthesis, Ga is not held in a crucible; instead, the tube is slightly angled to let gravity keep the Ga in place after melting.

After growth, the sample is gradually cooled to room temperature and the quartz ampoule is carefully opened (weakened first with a diamond scribe). An optical micrograph of a region of the resulting boule is seen in figure 5.12, revealing the large

crystalline order.

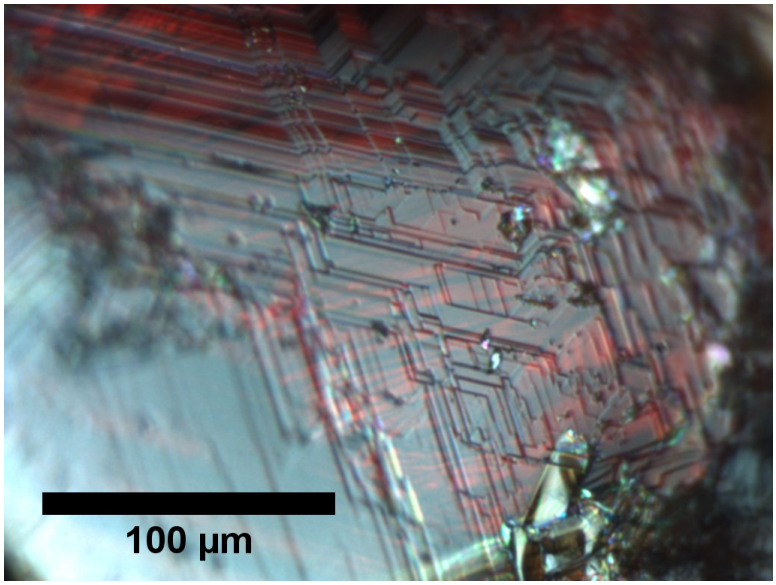

Figure 5.12: Optical micrograph of GaSe boule

These crystals were then Scotch tape exfoliated onto a SiO_2/Si wafer, following the standard procedures used for graphene exfoliation. Figure 5.13 shows a region with very thin GaSe; the very light blue trapezoidal shape (attached to the brighter triangle at the center) was shown by Will Gannett to be only 3 layers thick using AFM (assuming ϵ-GaSe stacking).

Raman spectroscopy was performed on the exfoliated crystals, and the resulting spectra (shown in figure 5.14) agree with published values for GaSe [5]. One additional peak, at 230 cm^{-1} for thick and redshifted to 220 cm^{-1} for a thinner sample, is not seen in the literature. This may be be due to a contaminating phase or an interaction with the SiO_2 substrate.

Will Gannett and I attempted to perform transport on these devices, with and without optical excitation. We chopped ($\sim$10-200 Hz) the output of a monochromated solar simulator to look for the onset of optical absorption, which could give us information about the bandgap of the few-layer GaSe. One such device is shown in figure 5.15, where a GaSe bilayer is contacted with thermally-evaporated In fingers. Unfortunately, the extremely thin GaSe in this example proved far too resistive to measure, though further effort could be made on somewhat thicker devices or with closer spaced electrodes. Recently, there has been related work in the literature [58]. Despite this development, there is still potential for new investigation with thin GaSe for SFPV cells and devices mated with CVD graphene.

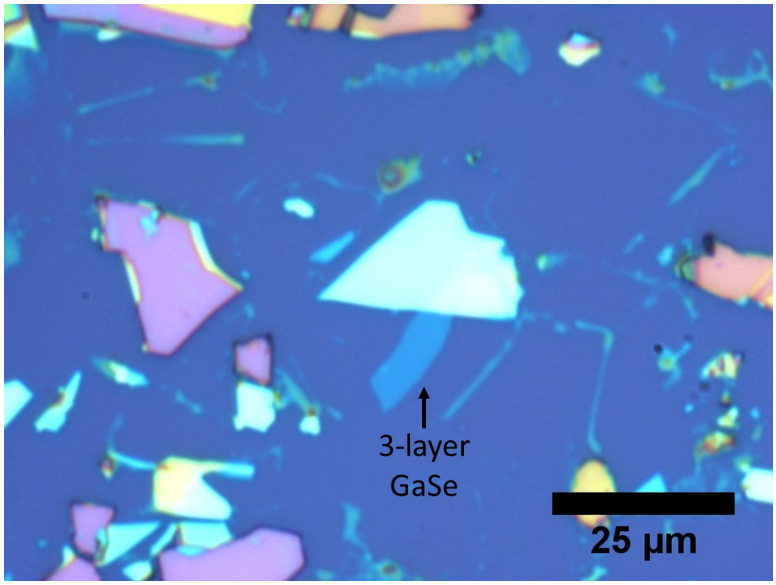

Figure 5.13: Few-layer exfoliated GaSe on SiO_2/Si

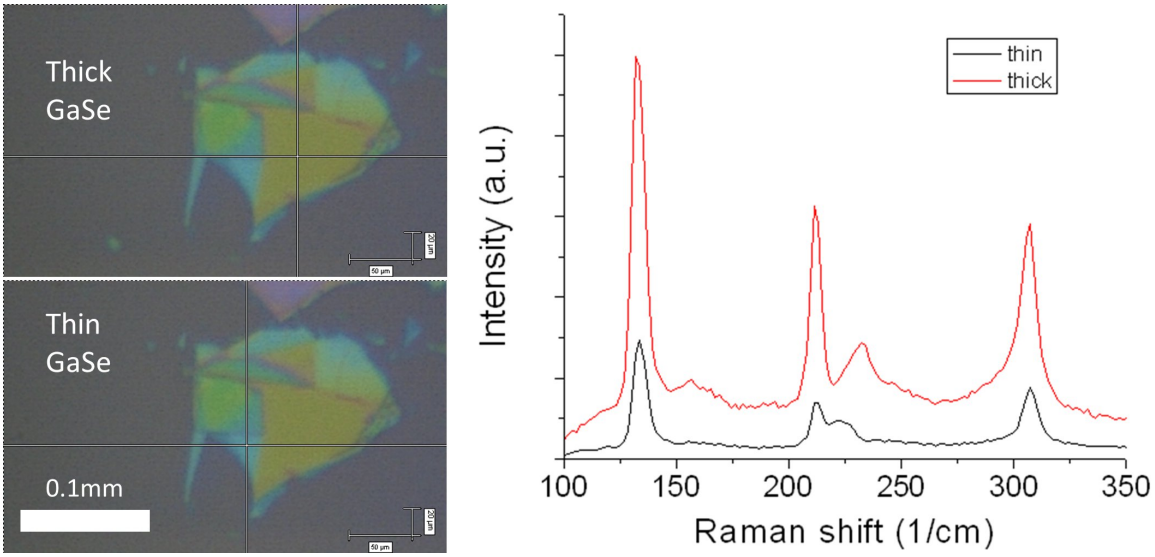

Figure 5.14: Raman spectroscopy of exfoliated GaSe on SiO_2/Si (514 nm excitation). The dominant peaks agree with published values for GaSe [5].

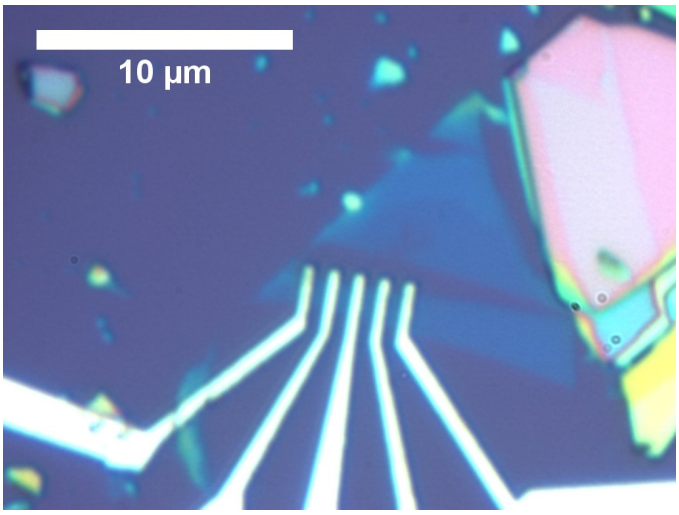

Figure 5.15: Bilayer GaSe on SiO_2/Si with In contacts

5.4.2 Tin sulfide (SnS and SnS_2) growth

The growth conditions for SnS follow a recipe reported by Hegde et al. ([43]), but our starting material is SnS powder (Alfa Aesar No. 14051, 99.5%). (Hegde first grows polycrystalline SnS using elemental Sn and S and then grinds the polycrystalline SnS into powder before regrowth.) We seal a few grams of SnS powder (first compacted into pellets) in a 1 cm inner diameter quartz ampoule at a pressure of 10^{-5} Torr. The ampoule was then placed in 3 zone furnace, with the hot end (SnS starting position) held at 890°C and the cool end held at 830°C . This is maintained for 3 days, after which it is uniformly cooled. After cooling to room temperature, the quartz ampoule is carefully opened. The resulting boule from such a growth is seen in figure 5.16.

Though much amorphous material remains in the melt, large flakey brown crystals (∼1–3 mm in diameter and thickness) comprise a large portion of the boule. These single crystals are then Scotch tape exfoliated onto SiO_2/Si substrates to produce thin, flat surfaces, as shown in figure 5.17.

To confirm the phase of the SnS, we performed Raman spectroscopy on these exfoliated crystals. Unfortunately, Raman data (seen in figure 5.18) on the exfoliated crystals is consistent with SnS_2, a wider gap semiconductor, and not SnS [13, 89]. Though the stoichiometry was chosen appropriately for SnS, poor temperature control may have caused SnS_2 to be the preferred phase.

This is not a complete loss, as SnS_2 is also a semiconductor (indirect gap around 2eV), and may in fact behave similarly to MoS_2 and open a direct gap as thickness is decreased to a monolayer. Future experiments on applications to SFPV cells will likely be conducted by Dr. Oscar Vazquez-Mena, using these SnS_2 crystals or properly synthesized SnS.

Figure 5.16: Boule of tin sulfide grown with the Bridgman technique. Most of the material appears amorphous, but large flakey brown crystals are also present.

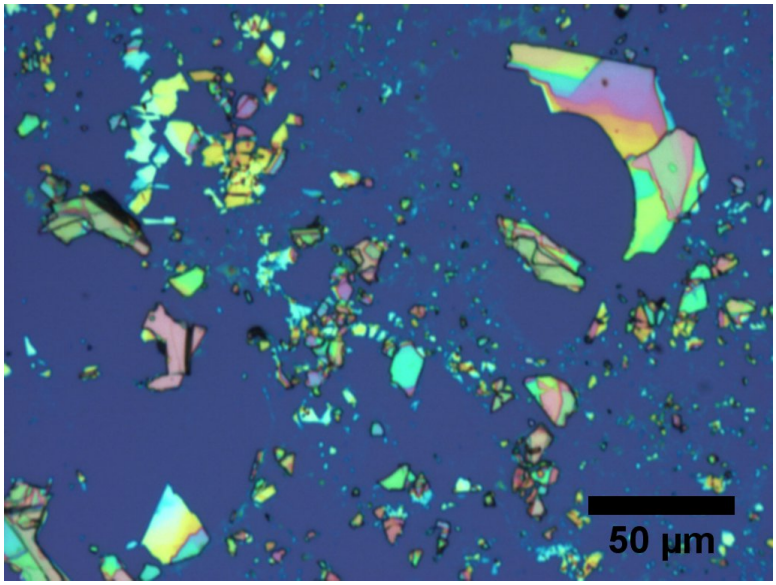

Figure 5.17: Tape exfoliated tin sulfide on 300nm SiO_2 on Si wafer

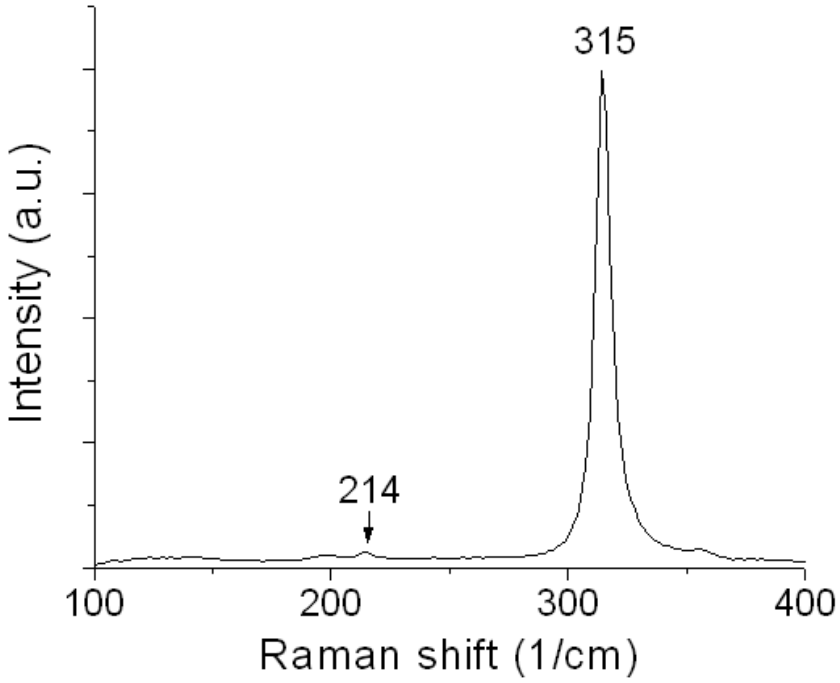

Figure 5.18: Raman spectrum of exfoliated SnS reveals phase is in fact SnS_2.

5.5 Cuprous oxide growth

Cuprous oxide (Cu_2O) is a direct bandgap semiconductor with $E_g \sim 2.1$eV. Synthesis of Cu_2O may at first seem relatively straightforward, as it is simply thermal oxidation of metallic Cu. In practice, all recipes involve a tradeoff, as larger grains tend to correlate with lower carrier concentration (and higher resistivity). (Cu_2O tends to be p-doped due to oxygen vacancies, and recipes which produce larger grains result in fewer oxygen vacancies.) There are in fact two stable phases of copper oxide, cupric oxide (CuO) and cuprous oxide. As shown in the phase diagram in figure 5.19, the CuO phase is preferred at lower temperatures [77].

Therefore, to preferentially grow the Cu_2O phase at a given oxygen partial pressure, we typically ramp up temperatures while flowing an inert gas and only start flowing oxygen once past the CuO/Cu_2O transition temperature. Additionally, the growth of larger grains (and higher mobilities, reduced grain boundary recombination) requires higher temperatures.

5.5.1 High temperature growth on thick Cu foils

We performed high temperature oxidation of Cu foils in a Lindberg Blue Mini Mite 1" tube furnace. We modified a recipe from F. Biccari's PhD thesis [10], with

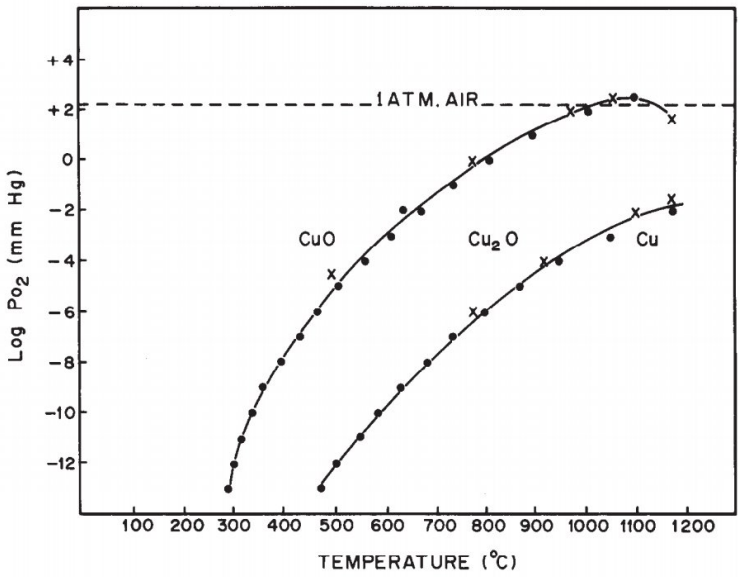

Figure 5.19: Pressure-temperature phase diagram of copper oxides (image from Rakhshani et al. [77])

an initial oxidation at 910°C followed by a higher temperature anneal to enlarge grains; our recipe is shown below in figure 5.20. The Cu foil (100–250 µm thick, Alfa Aesar Puratronic) is supported by Pt foil on an alumina boat in a standard high strength 1" outer diameter quartz tube. The Pt substrate is required because at high temperature Cu_2O reacts violently with almost all materials (except for Pt and possibly Tl, and Tl is rather toxic).

An as-grown crystal of Cu_2O is shown below in figure 5.21. The crystal is a ruby red, with minimal formation of CuO on the surface due to the short amount of time spent at temperatures where CuO is preferred (thanks in part to the deionized water quench).

The resulting wafers are typically rather rough (∼1 µm), as the Cu must expand significantly as oxygen is incoporated into the structure. Therefore, mechanical polishing is used to smooth surfaces prior to lithography, as described in section A.3 of the appendix. Any surface CuO is easily removed in this polishing step, though additional post-polishing surface treatments are typically needed to re-oxidize the now smooth surface.

After polishing, resistivities were typically between 10–100 kΩ-cm and grains were between 0.1–1 mm^2 (for 100 µm foils, the grains were single crystalline through the sheet except for a small void region in the center).

Given that Cu_2O is a direct gap semiconductor, only about 1 µm is needed to fully absorb sunlight. Therefore, we can sacrifice grain size and mobility for very thin samples. It turns out that, despite the predictions of the phase diagram shown in

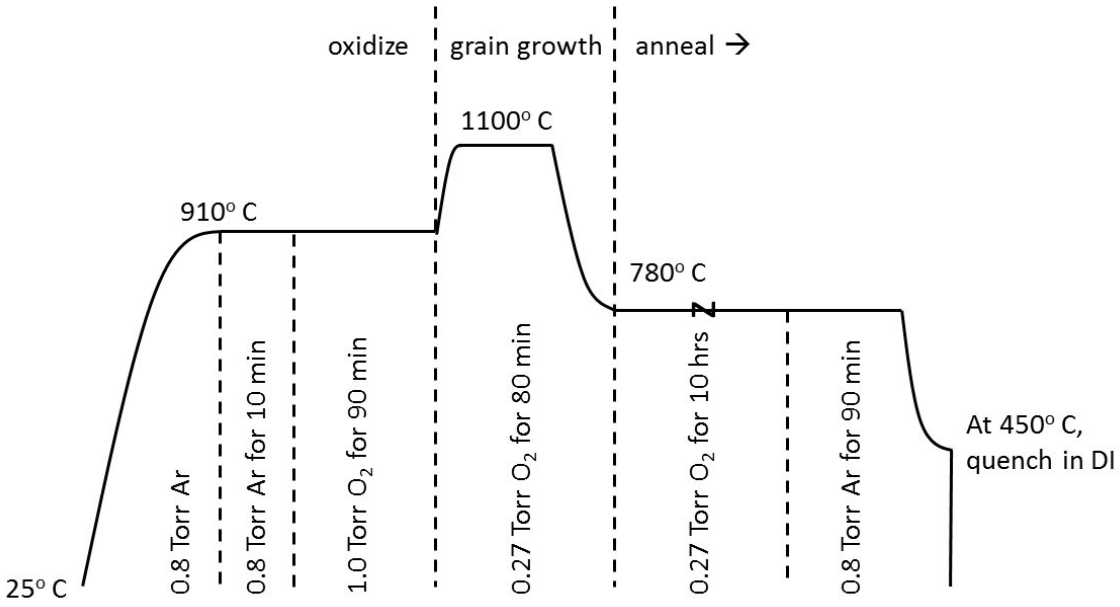

Figure 5.20: Recipe for high temperature Cu_2O foil growth

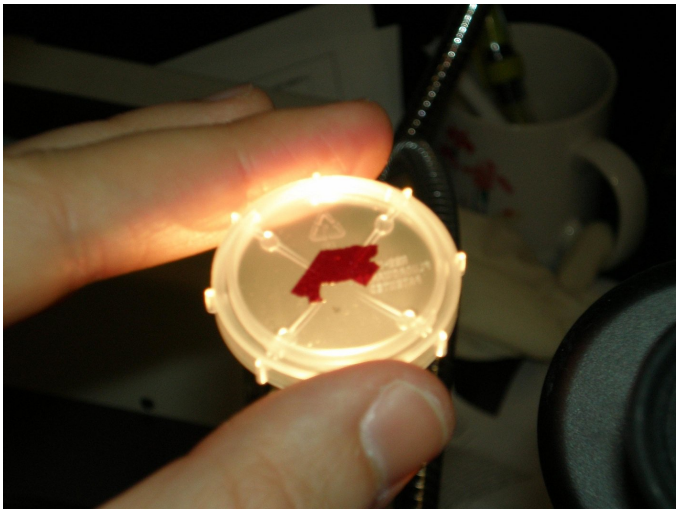

Figure 5.21: Cu_2O wafer grown via high temperature, low pressure thermal oxidation

figure 5.19, you can preferentially grow Cu_2O at low temperature (200–300° C) and atmospheric pressure.

5.5.2 Thin film cuprous oxide growth

Following a recipe from Figueiredo et al. [31], we performed low temperature (250°C) oxidation of thermally-evaporated Cu films (between 200 and 500nm thick). This was performed in a tube furnace, though it could have easily been performed on a hot plate. The benefit of the tube furnace is that inert gas can be flowed during the ramp up and ramp down, though it is likely that growth of other phases during these steps would be minimal as full oxidation at 250°C requires about two hours. The Cu films were supported by various substrates, including quartz and evaporated Au on SiO_2/Si. Because temperatures were sufficiently low, the Cu_2O did not seem to react with the substrates. Carrier concentration ($N_A \sim 2 \times 10^{15}/cm^3$) and Hall mobility (10 cm^2/V-s) were consistent with results obtained in the literature [31]. A SFPV cell made with low temperature Cu_2O (with Au under the Cu to serve as the bottom ohmic contact to the Cu_2O) is shown in the appendix in figure A.8. Unfortunately, these SFPV cells could not be made rectifying, perhaps due to other phases (CuO) formed between the very small grains.

An alternate method for creating thin film of Cu_2O is sputtering deposition, either sputtering of Cu_2O in a low oxygen partial pressure or reactive sputtering of Cu metal in the presence of a few mTorr of oxygen. We preferred the reactive sputtering method due to its ∼10X faster deposition rate, about 0.1 µm/min. An image of reactive oxygen sputtered Cu_2O, deposited by Dr. Oscar Vazquez-Mena with the Randex sputterer in the Berkeley Nanolab, is seen in figure 5.22.

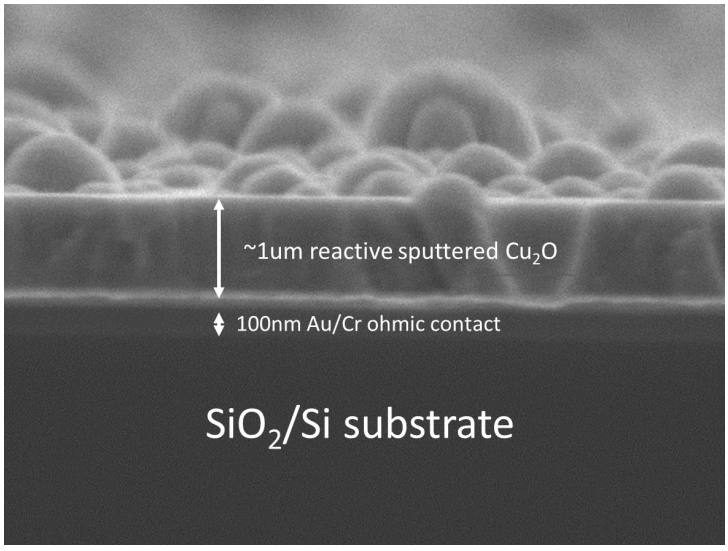

Figure 5.22: Reactive oxygen sputtered Cu_2O on Au/SiO_2/Si

We deposited not just on $Au/SiO_2/Si$ substrates but also on quartz wafers in order to measure optical properties. A graph of optical absorption versus wavelength, measured with the P. Alivisatos group's UV-vis system, is shown for reactive oxygen sputtered copper oxide deposited at different oxygen partial pressures. CuO forms preferentially at higher oxygen partial pressures, whereas Cu_2O is dominant for lower pressure deposition.

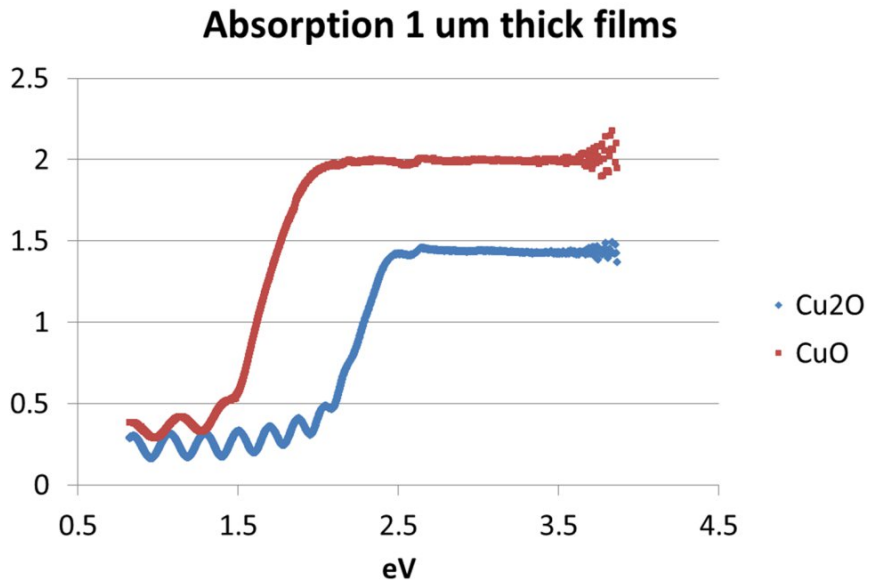

Figure 5.23: Absorption versus wavelength for reactive sputtered CuO and Cu_2O, measured by Dr. Oscar Vazquez-Mena in collaboration with the Alivisatos group

Unfortunately, all SFPV cells made with thin film Cu_2O made ohmic contact with Cu and ITO contacts, indicating that surfaces were of low quality (likely CuO, which makes ohmic contact to both of these materials), making efficient cells impossible. The best SFPV cells were made with high temperature, low pressure thermally oxidized Cu.

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Appendix A

Fabrication and measurement techniques

A.1 Photovoltaic measurements

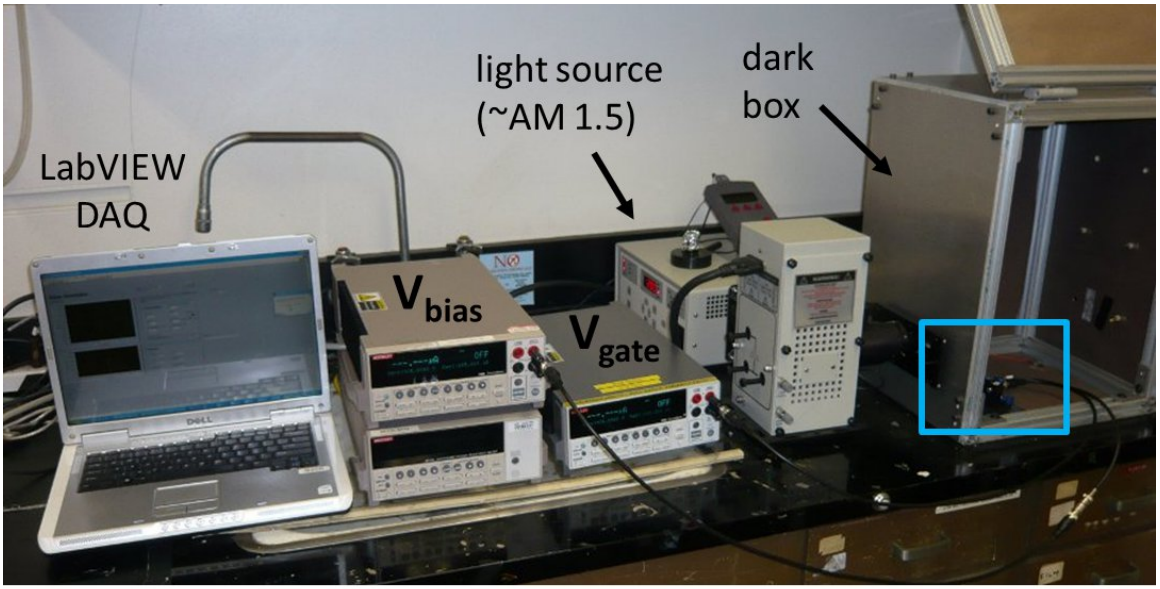
Our photovoltaic measurement system, shown in figure A.1, consists of the following components: Oriel solar simulator (No. 67005) for AM1.5 illumination, two Keithley 2400 sourcemeters (for biasing, measuring current, and applying a gate voltage), a dark box to eliminate external sources of light, and a laptop equipped with LabVIEW code to acquire and interpret data from the sourcemeters. Contacts to solar cells are generally either wires adhered with silver paint (for large cells) or pin probes (for small samples). Most of the cells tested in chapter 2 were contacted using a home-built 3-point probe station, seen in figures A.1, A.2, and A.3.

The probe station provides top and bottom contacts (one grounded) and a third contact (e.g. for an applied gate voltage), and was designed to fit on the stage for our Olympus BX60 optical microscope to allow pin probes to be precisely placed on very small contacts (see figure A.2).

In addition to standard solar cell configurations where light is incident on the same side as the contacts, the probe station is also set up to test "inverted" geometries, where the contacts are on top but light is incident from the bottom. These two configurations are seen in figure A.3, in which light passes through a small hole to reach the sample in the inverted configuration.

A.1.1 In-tipped pin probes for fragile contacts

The three pin probes are Cu or CuBe alloy and have 25 µm diameter tips. For sensitive or fragile electrodes (such as gate contacts on thin dielectrics), the probes were tipped with indium, a soft metal, to avoid scratching through the cell and risking shorts. The procedure for indium tipping, inspired by Çağlar Girit's excellent processing for In microsoldering [35], is as follows:



Zettl Group photovoltaic measurement system (above)

A device under illumination (inset above and right)

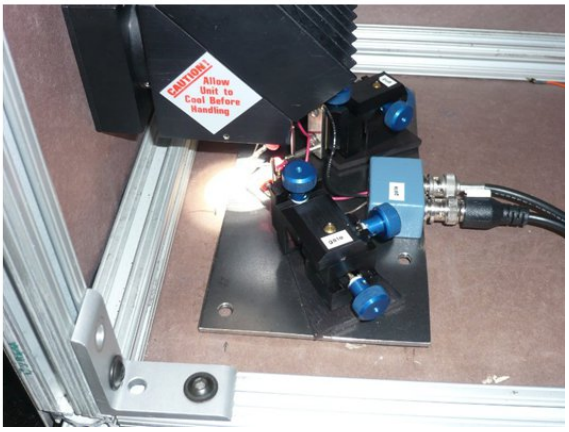


Figure A.1: Zettl Group photovoltaic measurement system. Small samples are contacted with a 3-point probe station (inside the dark box and shown enlarged in the lower image).

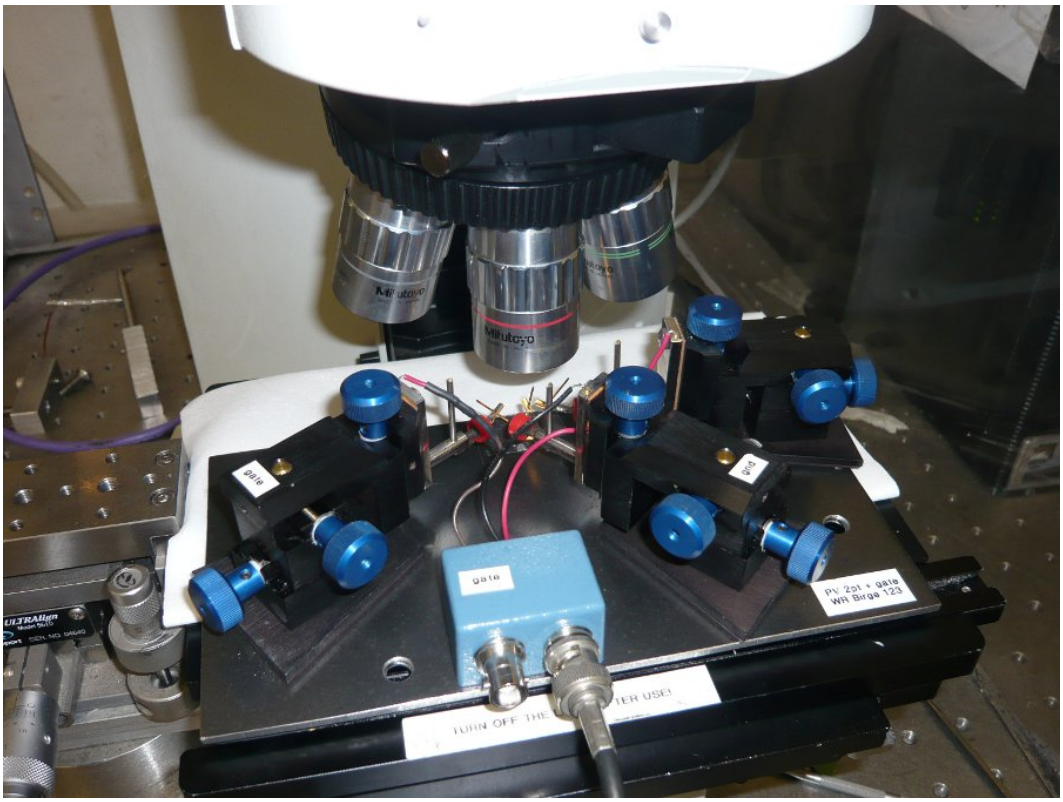


Figure A.2: Aligning probe contacts under the optical microscope

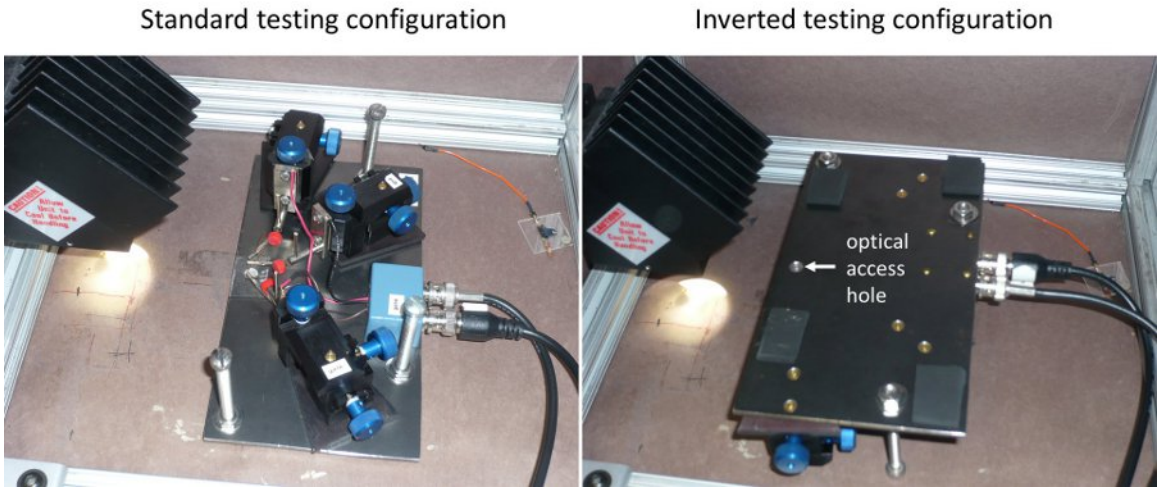


Figure A.3: Probe station in standard (light from above) and inverted (light from below) configurations. In the inverted configuration, 3 bolts are used as legs, to prevent bumping the probe manipulators and shifting the pins.

1. Heat a small (1–2mm diameter) chunk of pure In (99+%) on a piece of Al foil on a hotplate at 190°C until the In melts. The melting point of In is considerably lower ($\sim$ 156°C), but the higher setpoint temperature results in more consistent adhesion to the Cu pin and better contact shape.

2. Once the In melts, dip a clean Cu pin into the melt and quickly retract. The In wets the Cu sufficiently to stick and rapidly solidifies as the Cu pin is withdrawn. The resulting In spike is typically a few mm long and has a very fine ($\sim$5 µm) but soft tip.

3. The In-tipped Cu probe can be carefully remounted in the micromanipulators. With careful use, the In tip can last for many measurements before detaching or becoming irreparably deformed.

A.2 Lithography and evaporation tips and tricks

Though we have occasional use for photolithography (e.g. alignment marks) or hard shadow masks, we tend to rely almost exclusively on electron-beam lithography for contact deposition. E-beam lithography can produce extremely small features (<100 nm) with sub-micron accuracy, and the PMMA resist used does not seem to drastically affect graphene or carbon nanotube properties, unlike the I-line resist we use for photolithography. We use Dr. J. C. Nabity's Nanometer Pattern Generation System (NPGS) to control the electron beam in our FEI Sirion XL30 SEM. Patterns are written at an acceleration voltage of 30 keV and a somewhat overexposed dose of 350–400 µC/cm^2. A typical lithography process proceeds as follows:

1. Spin-coat A4 PMMA 950 (Microchem) onto sample at 3000 rpm (3 second ramp and deceleration), cure on hotplate at 180°C for 20 minutes.

2. Put small scratch in PMMA or use Au colloid to allow you to focus on the sample plane in the SEM.

3. Write pattern in SEM using NPGS.

4. Develop and rinse – 90 seconds in MIBK:IPA (1:3) and 30 seconds in IPA. Blow dry with N_2. (Optional: heat at 100°C to drive off any remaining solvent).

5. Evaporate contacts in thermal or e-beam evaporator. (Or etch away graphene in reactive ion etcher, etc).

6. Lift off resist and metal in acetone (60°C) for 30 minutes. Agitate acetone with syringe or mild sonication if necessary. Rinse in IPA and blow dry with N_2.

A.2.1 Sputtered or thick contacts

Sputtering is much more conformal than electron-beam or thermal evaporation, due to the much higher pressure (and hence lower mean free path) during deposition. As a result, lithographically-defined sputtered contacts (or also thick, evaporated contacts) often face difficulties in liftoff. To mitigate this problem, one can use a MMA/PMMA bilayer. MMA is etched slightly more than PMMA, so a bilayer (MMA on the substrate, then PMMA on the MMA) will result in an underetched resist mask, as seen in figure A.4. This overhang guarantees a break in the contact for the resist solvent to penetrate, providing that the sputtered or evaporated thickness is less than the MMA height and that the mean free path in the sputterer is larger than the MMA height.

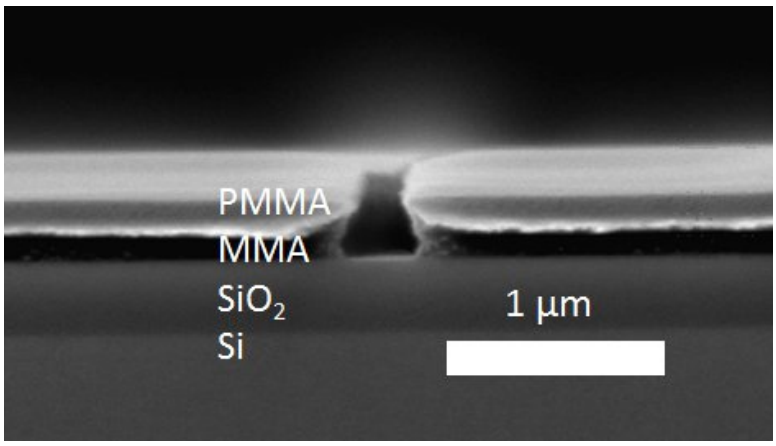


Figure A.4: SEM image of developed MMA PMMA bilayer

This technique proved useful for sputtering relatively thick but rather narrow ITO contacts onto Cu_2O SFPV cells. Standard PMMA exposures ($\sim$350 µC/µm^2) were sufficient for exposing PMMA/MMA bilayers. To make sure the MMA and PMMA layers were well defined, MMA was first spun to a thickness of around 200 nm and cured at 180°C for 5 minutes, followed by spin coating of $\sim$250 nm of PMMA and curing at 180°C for 20 minutes.

A.2.2 Evaporation pitfalls: narrow contacts and step edges

Electron-beam and thermal evaporation are performed at pressures around or below 10^{-5} Torr and are therefore very directional. This can be helpful when using a hard mask to define contacts (as the bleed will be over an order of magnitude smaller than the mask-sample air gap), but it can present problems when depositing very narrow lithographically-defined contacts or when attempting to make a continuous contact over a tall step edge, as shown in figure A.5. For narrow contacts, the crucible

must be able to "see" all parts of the trench to ensure the desired contact width is achieved. To avoid continuity issues at step edges, the sample can be angled to ensure continuous contact over the step.

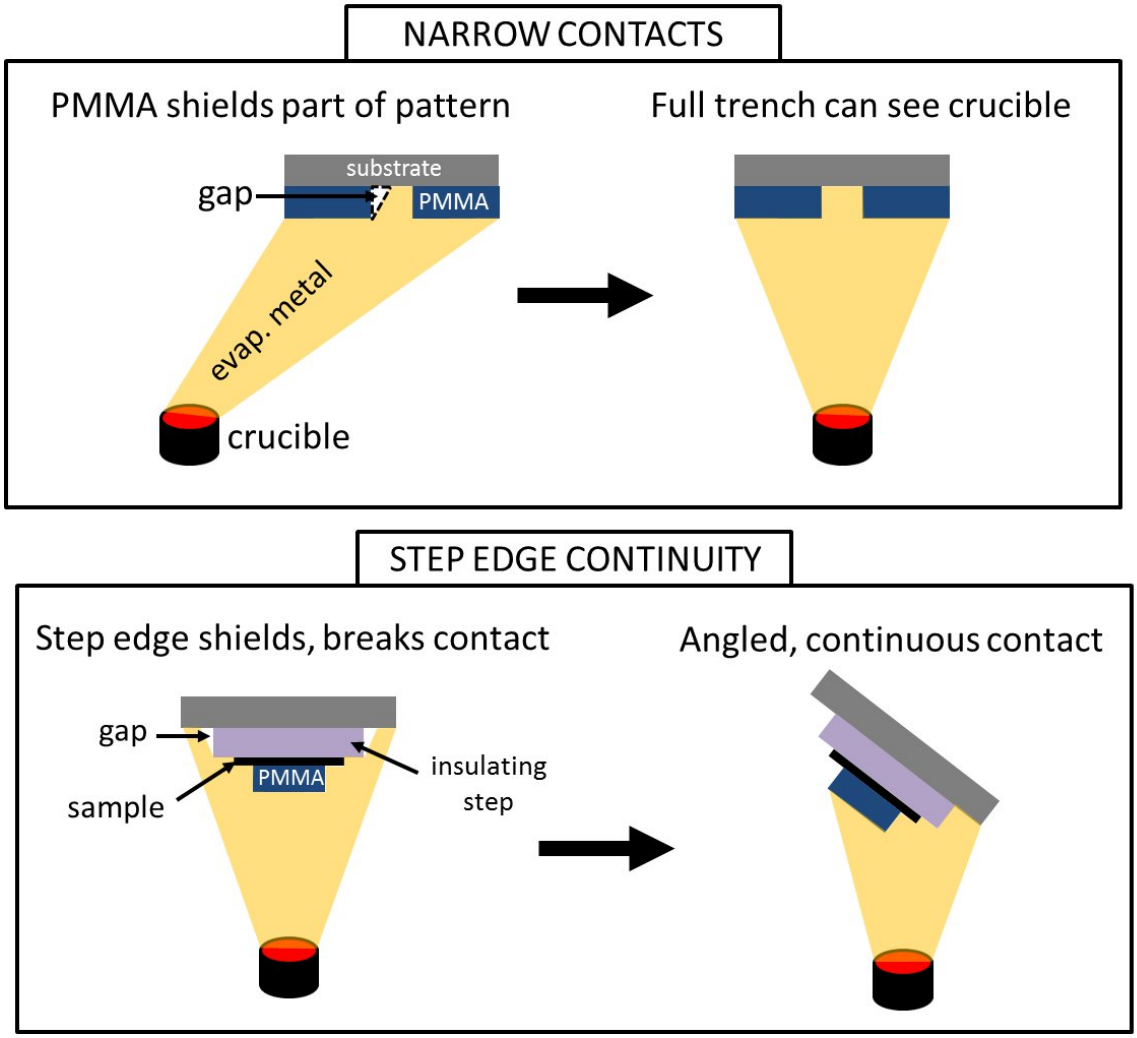


Figure A.5: Problems with evaporation with narrow lithographically-defined contacts and step edges

A.3 Cuprous oxide: surface treatments and SFPV devices

In chapter 2, cuprous oxide (Cu_2O) was studied as a promising material for SFPV cells. The synthesis, high temperature oxidation of Cu foils, results in large single

crystals and minimal contaminating phases (e.g. CuO). However, the sudden introduction of oxygen into the Cu structure dramatically swells the Cu foil, and the resulting Cu_2O tends to have a $\mathcal{O}(\mu m)$ lumpy surface (especially between grains). Contacts deposited directly on as-grown polycrystalline Cu_2O will inevitably have many breaks and sticking problems, seen in figure A.6.

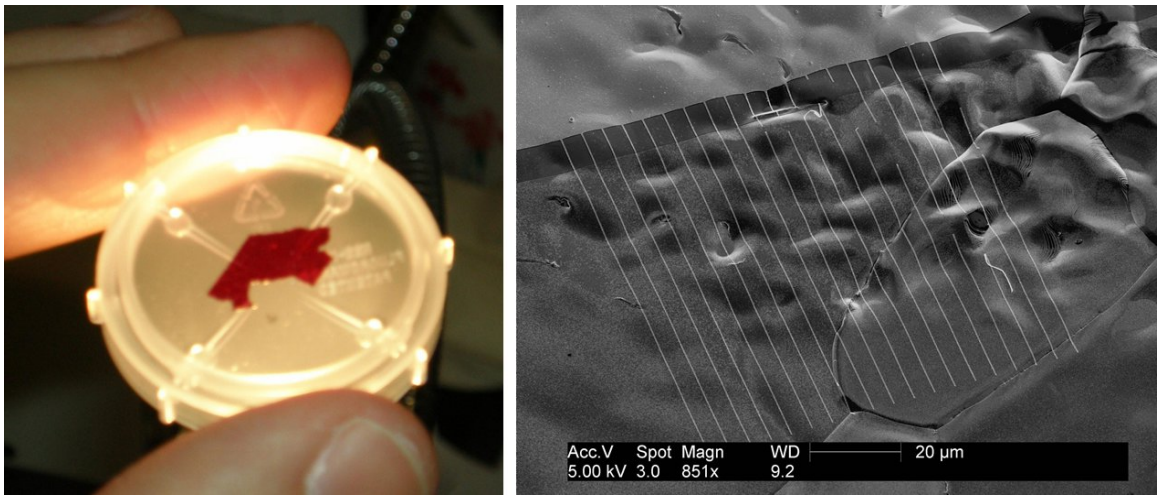


Figure A.6: At left, a picture of as-grown polycrystalline Cu_2O. At right, SEM imaging reveals that contacts deposited on unpolished Cu_2O have severe sticking problems and breaks.

To solve this, we could conformally deposit (e.g. sputter) electrodes, but we may then have issues with liftoff as the nanowires are fairly narrow. Instead, we mechanically hand polish the Cu_2O foils. Though the surface is only a few µm rough, we often remove over half of the crystal thickness to remove voids in the center of the foil. These voids form due to the isotropic oxidation process – oxygen reaches the middle from both sides simultaneously. Cu_2O samples are affixed to metal blocks with wax, and coarse polishing is performed with 800 grit sandpaper. This is followed by 1200 grit paper until there are no more visible deep scratches. Finally, 1 µm colloidal silica polish is used to achieve a shiny finish. Unfortunately, this polishing corrupts the surface of Cu_2O, covering it with a mix of CuO and Cu hydroxides. Therefore, after mechanical polishing, the sample is placed in a beaker of bromine-methanol (2 vol% bromine in methanol) for 1 minute to restore the surface to Cu_2O. SFPV cells made with polished and treated Cu_2O are seen in figure A.7; improved contact adhesion and continuity is apparent.

To avoid the need for mechanical polishing altogether, one can instead use thin film Cu_2O deposited by sputtering or grown by low-temperature oxidation of Cu thin films, as described in chapter 5. However, these films also tend to have a thin CuO surface phase, so it is generally recommended to perform at least the bromine-methanol

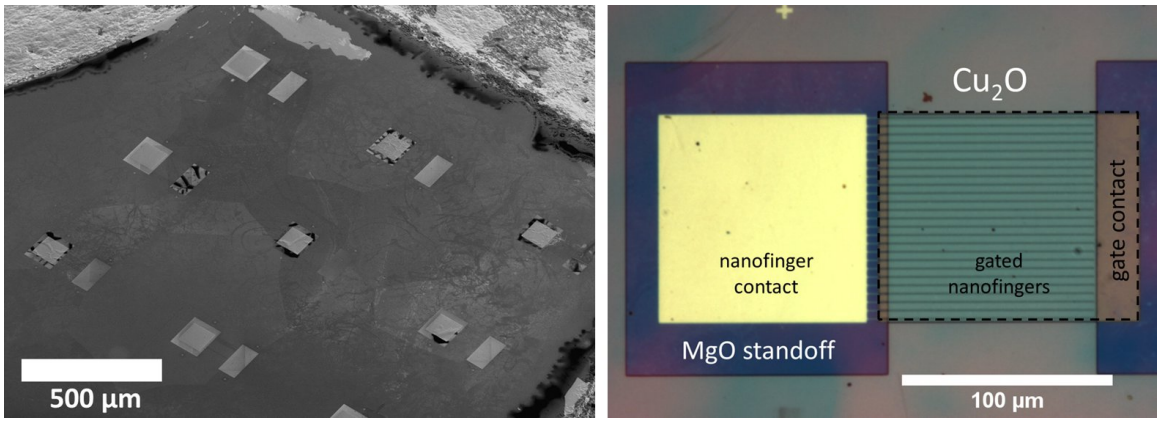


Figure A.7: SEM and optical images of SFPV devices made with polished, treated Cu_2O. Surface roughness is noticably decreased and contact adhesion and continuity are improved.

surface treatment prior to contact deposition. An optical image of a Cu_2O SFPV cell made with low-temperature oxidized Cu_2O and a graphene contact is shown in figure A.8. As mentioned previously, these cells boasted lower series resistances than the high temperature Cu_2O foils but their photovoltaic performance was significantly worse, perhaps due to the small grain sizes (causing increased recombination at the many grain boundaries).

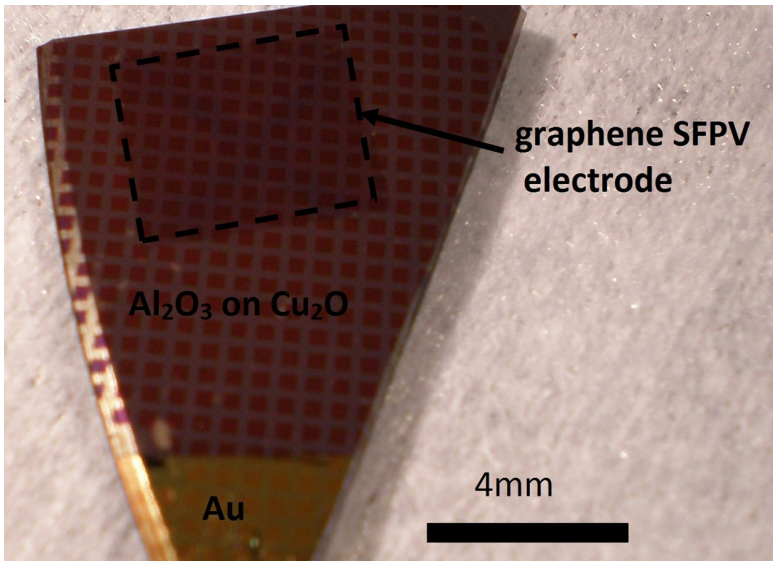


Figure A.8: SFPV device made with thin film, low temperature Cu_2O

A.4 Piranha etching

Many of the materials we study are highly sensitive to surface properties; after all, graphene is all surface and no volume. Therefore, careful surface treatments are often crucial. One common treatment is piranha etching, which helps to improve yields and preserve neutral doping when exfoliating graphene or transferring CVD graphene onto SiO_2.

Piranha treatment removes organics and results in increased SiO_2 hydrophilicity. Additionally, it adds hydroxyl groups (OH-) to the SiO_2 surface which makes it more "sticky" and improves exfoliated graphene yield. The process for piranha treatment is as follows:

1. Clean substrate (typically SiO_2/Si wafers). Sonicate, first in acetone and then in isopropanol, for about 10 minutes. Blow these samples dry with N_2 and place in a beaker.

2. Heat a water bath to 100°C.

3. Pour 3 parts concentrated sulfuric acid (68 wt.%) into beaker, covering samples, and then add 1 part H_2O_2 (30 wt.%). Heat beaker in water bath for about 30 minutes.

4. Dispose of piranha waste in acid waste. Refill beaker with deionized water and empty (except for samples) into acid waste. Repeat 3-4 more of these rinses with deionized water. Blow samples dry.