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A Resonant Dual Extended LC-tank Dickson Converter with 50% Two-Phase Operation at Odd Conversion Ratios

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Abstract—This paper describes a resonant Dickson-based topology that achieves complete soft-charging with two-phase operation and a convenient 50% duty cycle at all odd conversion ratios. A brief analysis is presented that shows how the resonant switching frequency can be calculated as a function of inductor and capacitor values. One solution sets all capacitors and both inductors equal, and results in switching devices experiencing a constant blocking voltage that is largely independent of load and fly capacitor voltage ripple. The requirement for capacitor matching and subsequent low capacitance density C0G dielectrics is compensated by a weakly bounded voltage swing: no switching devices are present on intermediary nodes connecting L and C elements allowing for very large voltage ripple and highly effective utilization of each fly capacitor’s energy density. A discrete 1:5 prototype validates the proposed topology with measured waveforms illustrating 50% two-phase operation and a load-independent maximum blocking voltage across switching devices. An output power of 129 W with a 94% peak efficiency was measured for an input voltage of 20 V. Measuring 11.45 mm × 12.95 mm × 2.8 mm, this prototype achieves a very high power density of 311 kW/liter (5,096 W/inch³) despite the use of diodes for simplicity and 66% of the converter’s volume being comprised of PCB and free space.

Index Terms—Resonant Converter, Dickson, Soft-Charging

I. INTRODUCTION

Hybridized switched-capacitor-inductor power converters have shown significant promise in recent years with extremely high power-densities having been reported [1]–[3]. Switched-capacitor converters which introduce assistive inductive elements can achieve complete mitigation of the slow-switching-limit (SSL); a loss mechanism described analytically in [4] and which has largely prevented widespread adoption of capacitor-based power converters. This approach, termed ‘soft-charging’ in [5], allows fly capacitors to be operated efficiently with increased voltage ripple, significantly improving passive energy density utilization.

To date, several topologies eligible for hybridization have been explored with additional attempts made at mathematical analyses used to identify key enabling conditions (e.g. [6]). However, new hybridized topologies continue to emerge, setting the stage for future comparative analysis. One such topology, the dual extended LC-tank Dickson converter depicted in Fig. 1, is described here, and offers a simple solution with several desirable traits for fixed integer odd conversion ratios.

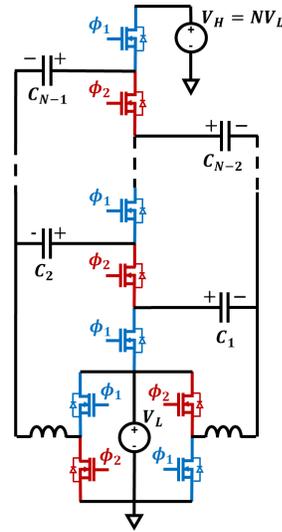


Fig. 1. Proposed dual-inductor Dickson converter with two extended LC-tanks. For odd conversion ratios this topology achieves complete soft-charging of all fly capacitors with a convenient and efficient 50% duty cycle on all switches.

The Dickson topology is an attractive choice for hybridization due to its relatively relaxed voltage stress on switching devices throughout the circuit. Previous attempts to hybridize this topology using a single inductor have suggested adoption of a split-phase switching scheme, allowing for zero-voltage switching (ZVS) conditions to be realized among several switches throughout the ladder [7]. Unfortunately this approach requires the introduction of several additional tertiary phases which each need to be controlled with precision if SSL losses are to be fully mitigated. [8] introduced a dual inductor topology well-suited for regulation at large conversion ratios, however the capacitor sizing scheme required by this approach results in rapidly increasing capacitance with increased switched-capacitor conversion ratio. Conversely, [9] proposed a ‘‘stacked-ladder’’ variant which conveniently allows for 50% two-phase resonant operation with all fly capacitors equal at both even and odd conversion ratios. However, this approach requires a decoupling capacitor column of theoretically infinite size. Fortunately, practical values can be realized by interleaving two such converters with a shared decoupling column for near-perfect ripple cancellation.

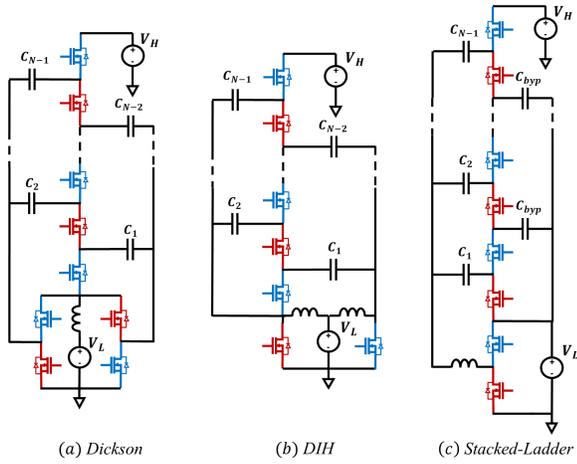


Fig. 2. Previously published soft-charged variations on the Dickson topology. (a) odd version of variant used to demonstrate split-phase switching in [7] and [10], (b) the dual-inductor hybrid (DIH) converter presented in [8], and (c) the stacked-ladder topology from [9].

The topology proposed here bears a resemblance to all three of the aforementioned designs, with a ladder similar to [7] and [8], and an H-bridge pumping dual-inductors similar to the interleaved stacked-ladder variant of [9]. In addition, all capacitors can be equal in value reducing cost and simplifying design effort. This condition also necessitates equal inductor values that experience balanced current loading. Moreover, this topology exhibits a significantly reduced switch count, comparable to the single-inductor variant in [7] with all switches experiencing a 50% duty cycle for reduced RMS currents. Lastly, since there are no switching devices present on the nets connecting L and C elements, voltage ripple is bound only by the voltage ratings of the passive devices themselves. This characteristic allows for very large voltage ripple that effectively utilizes the energy density of the fly capacitors without imposing load-dependent stress on the converter's switching devices. Akin to [8] and [9], to operate effectively the proposed topology requires precise capacitor matching, preventing the use of low-cost Class-2 multilayer ceramic chip (MLCC) capacitors whose values vary significantly with age, temperature and applied DC bias [11]. Instead, stable Class-1 C0G dielectrics are effectively employed, satisfying the concerns raised in [12]. Class-1 MLCC capacitors offer excellent loss factor, fine tolerances, stability and low ESR over a wide range of operating conditions, however, at low voltages ($< 100\text{ V}$) these dielectrics have much lower energy densities than their Class-2 MLCC counterparts. Fortunately, the large voltage ripple afforded by this topology allows for maximal capacitor utilization with capacitors rated on the order of the converters high-side voltage, V_H .

Section II discusses the theory of operation and presents the steps allowing calculation of the natural resonant switching frequency, illustrating a 50% two-phase capability. Section III presents a discrete prototype and Section IV concludes this paper.

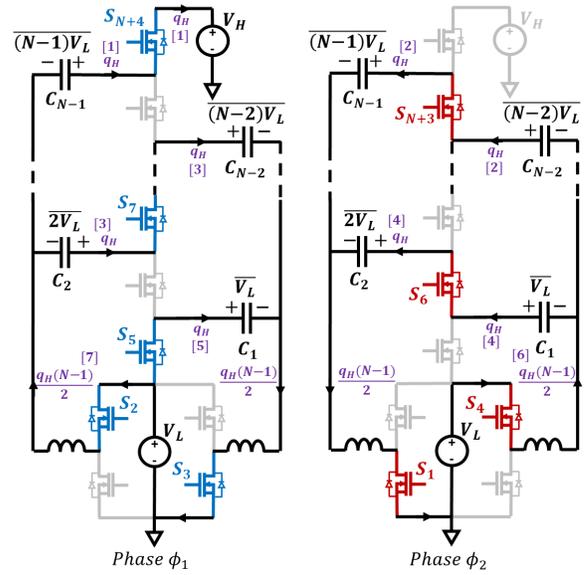


Fig. 3. Phases of operation for a 1:N converter. The steps towards determining charge-flow through each element, normalized with respect to the charge flowing through the high-side port V_H (q_H) is [annotated] sequentially.

II. THEORY OF OPERATION

Figure 3 depicts the two phases of operation for a 1:N instance of the proposed converter. At no-load, fly capacitors maintain DC holding voltages, \bar{V}_x , which are multiples of the low-side voltage V_L , as per conventional switched-capacitor converter operation. With an applied load to the high-side port V_H , a voltage ripple is incurred across all fly capacitors as charge is conducted through the stage. Straightforward charge flow analysis, such as that described in [4] and annotated in Fig. 3, reveals that all fly capacitors in this topology experience equal charge conduction throughout a full period which is also equal to the normalizing high-side charge conducted per period, q_H . Applying the constraint that all fly capacitors are equal in size ($C_i = C$) results in the same voltage ripple, $\pm\Delta$, being observed on all fly capacitors, where Δ can be expressed in terms of current throughput and the converters switching frequency;

$$2\Delta = \frac{q_H}{C} = \frac{I_H}{Cf_{sw}} \quad (1)$$

To verify complete soft-charging of all fly capacitors their large signal voltage ripple must be considered. Figure 4 depicts the instantaneous voltages present on each capacitor at the start and end of each phase in a 1:N converter, assuming the fly capacitor's DC holding voltages do not deviate with applied load¹. By assessing the KVL loops presented at the start of each phase, while ignoring both inductors as high-impedance chokes, it is apparent that all voltage loops are satisfied, removing the possibility of any transient inrush currents leading to SSL losses.

Through a similar voltage loop assessment, it becomes apparent that the voltage stress experienced by all switches

¹This assumption can be validated by applying volt-second balance constraints on the inductors.

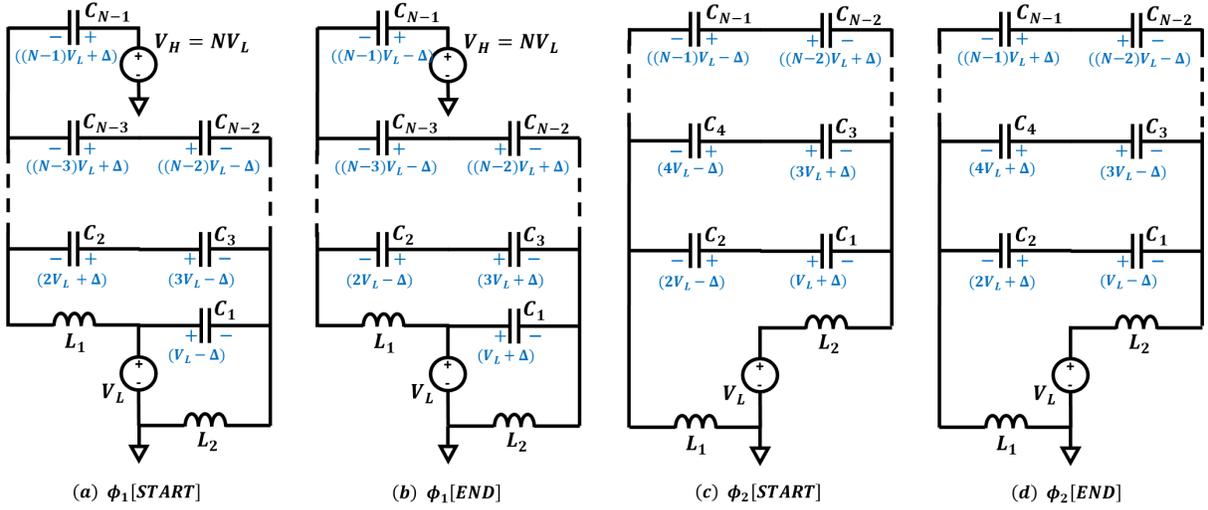


Fig. 4. Fly capacitor voltages both at the start and end of each phase, including superimposed voltage ripple Δ which is dictated by the load. Each capacitor holds a DC voltage equal to an integer multiple of the low-side voltage V_L .

is independent of Δ , implying that very large voltage ripple across the fly capacitors can be realized in practice. This in turn implies highly effective energy density utilization as the energy transmitted through these passives, denoted $E_{TX,x}$ in Eqn. (2), can approach or even greatly exceed the DC energy stored therein for biasing purposes (Eqn. (3)).

$$E_{TX,x} = \frac{1}{2}C_x(\overline{V}_x + \Delta)^2 - \frac{1}{2}C_x(\overline{V}_x - \Delta)^2 \quad (2)$$

$$E_{DC,x} = \frac{1}{2}C_x(\overline{V}_x)^2 \quad (3)$$

To determine the resonant duration of each phase and subsequent overall converter resonant switching frequency, both phases are simplified into the AC models depicted in Fig. 5 (a). Within ϕ_1 there is a virtual ground on each of the nodes bridging left and right converter sides (depicted with grey dashed line). As such, both phases can be further reduced into Fig. 5 (b). Given all fly capacitors are equal in value, by setting $L_1 = L_2$ we observe identical natural resonant frequencies throughout both phases. This results in a 50% duty cycle and two-phase resonant operation for all odd conversion ratios.

The theoretical operation of this topology is validated by simulation in LTSpice for an example 1:5 converter with $C_x = C = 100$ nF and $L_1 = L_2 = 126.6$ nH, resulting in a resonant switching frequency of ~ 1 MHz. Steady-state waveforms of inductor currents, fly capacitor voltages and switch voltages are depicted in Fig. 6, where $V_L = 10$ V and a resistive load of 25Ω is applied to the 50 V high-side output V_H . As a result of the applied load, $q_H = 2 \mu\text{C}$, and $\Delta = 10$ V, as per Eqn. (1). As depicted, smooth sinusoidal voltage ripple on the fly capacitors, with no discontinuities, indicates complete soft-charging. Additionally, despite very large fly capacitor ripple, switch blocking voltages are insensitive to load, with required ratings equal to V_L or $2V_L$.

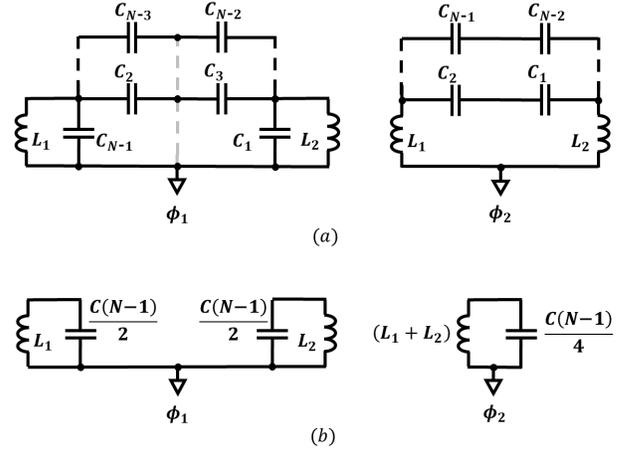


Fig. 5. Simplified AC models of both switching phases. Recognizing the “virtual grounds” in ϕ_1 assists in further simplification.

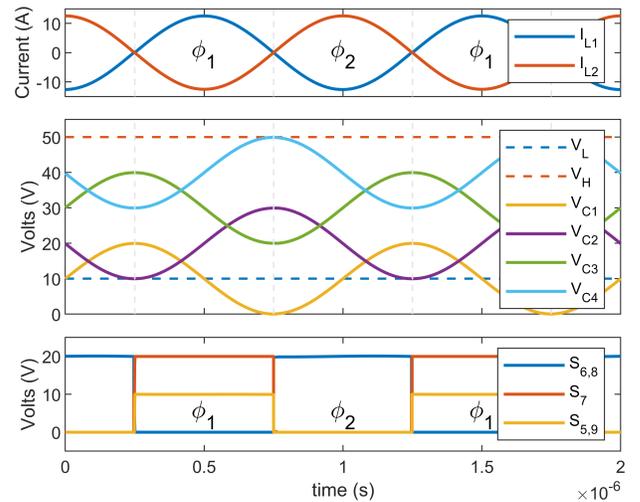


Fig. 6. Simulated current and voltage waveforms of a 1:5 example with low-side input voltage $V_L = 10$ V and a 25Ω load. Large sinusoidal ripple across fly capacitors, with no discontinuities implies complete soft-charging and highly effective energy density utilization.

III. DISCRETE PROTOTYPE

Figures 7 and 8 depict a discrete prototype constructed on a two-layer 0.8 mm thick PCB with 2 oz. copper metallization. As shown in Fig. 9, diodes were used in place of several high-side switches. These diodes conduct for the full duration of their respective phases, as predicted in simulation and as illustrated in Fig. 13, and may be replaced with active switches without altering converter operation. Moreover, a fully synchronous design would allow for bi-directional power-flow, enabling step-down applications. Here, diodes are used for simplicity and reduced part count at the expense of worsened efficiency with the introduction of forward voltage drops and increased parasitic capacitance. Gate drive power is delivered to switches S_{1-4} using conventional bootstrapping (Fig. 10).

Figure 11 illustrates converter volume breakdown and Table I lists components used. For a fixed resonant switching frequency, larger flying capacitors conduct greater charge for the same voltage ripple with reduced inductor size; a desirable trend given relative passive energy densities. However, non-negligible parasitics and a decreasing Q-factor ultimately limit this shift with a resulting increase in output impedance. In this prototype limitations due to diode forward conduction losses further directed modest fly capacitor values of 18.8 nF while still achieving appreciable voltage ripple.

Figures 12 and 13 depict measured voltage waveforms demonstrating converter operation. Large uniform sinusoidal voltage ripple is observed across all fly capacitors, signifying complete mitigation of all SSL loss and very high capacitor utilization, with C_{fly1} even undergoing a periodic negative bias at heavy load. As depicted in Fig. 13, D_{2-4} must tolerate a maximum blocking voltage of $\sim 2V_L$ with little load dependency. While D_1 and D_5 nominally block V_L (S_5 and S_{N+4} in Fig. 3), inherently clamped ringing may reach as high as $2V_L$ if no steps towards mitigation are taken. This ringing has the potential to occur during ϕ_2 since the fly capacitor network has no low impedance path to ground while in this state. No timing adjustments, snubber or damping techniques were applied to mitigate this effect, although this may be desirable in practice for reduced EMI.

Switching at 1.2 MHz, measured efficiency versus output power is plotted in Fig. 14 and shows a peak efficiency of 94% and a maximum output power of 129 W when subject to forced air cooling using a standard 12V computer fan. Subsequently, with a total best-fit cuboid volume measuring 415.18 mm³, this prototype obtains a power density of 5,096 W/inch³ when discounting cooling system volume.

Table II compares this work with several recently published fixed-ratio resonant converter topologies. Similar to other LC-tank type converters, the voltage ratings of switching devices within this topology are largely independent of load with passive dielectric strength instead bounding voltage ripple. Simple 2-phase control can be used with a 50% duty ratio for straightforward clock generation and reduced RMS conduction losses. Furthermore the recorded power density is competitive despite the use of diodes in this prototype.

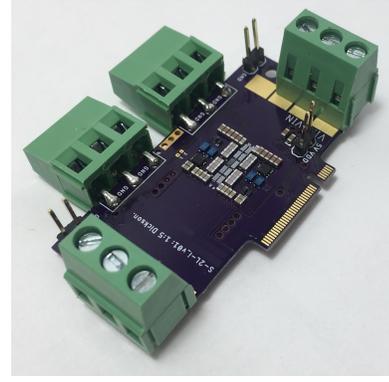


Fig. 7. Photograph of the constructed 1:5 prototype.

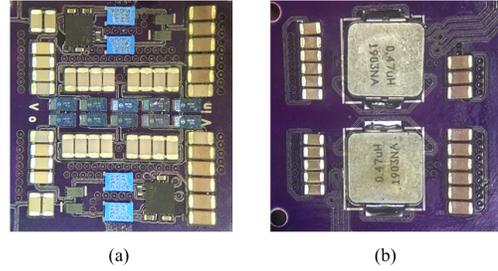


Fig. 8. Photograph of active area. (a) top, (b) bottom. A best-fit cuboid encompassing all active circuitry, including input and output capacitance, measures 11.45 mm \times 12.95 mm \times 2.8 mm.

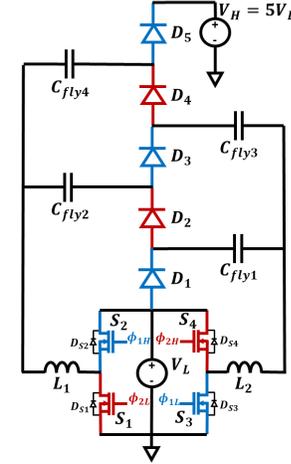


Fig. 9. Schematic of constructed prototype

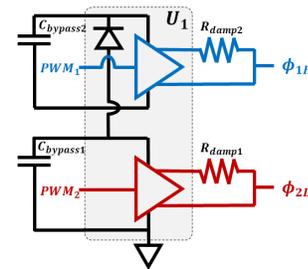


Fig. 10. Standard half-bridge driving circuitry used for switch pairs S_1 and S_2 , and S_3 and S_4 .

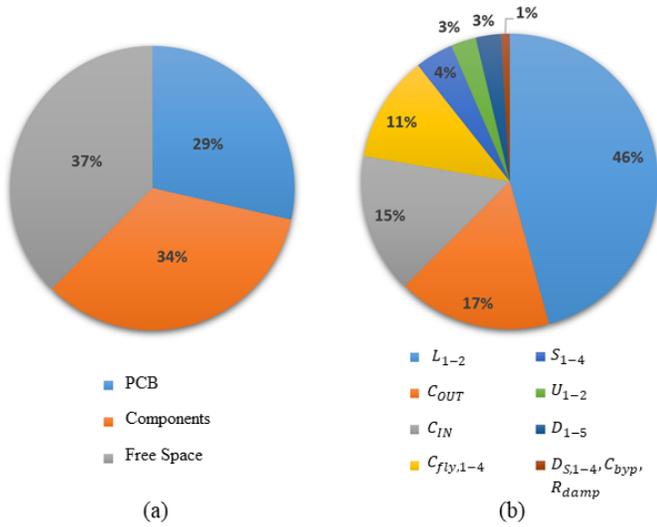


Fig. 11. Volume breakdown of a best-fit cuboid encompassing the entire solution. (a) volume type, (b) in-depth component volume breakdown.

TABLE I
COMPONENT DETAILS

Component	Details	Part Number
L_{1-2}	470nH 18A 18.2m Ω	IHLP2020ABERR47M01
C_{IN}	21 \times 2.2 μ F 50V X5R 0603	GRT188R61H225KE13D
C_{OUT}	23 \times 0.1 μ F 100V X7R 0603	GCJ188R72A104KA01D
$C_{fly,1-4}$	4 \times 4.7nF 100V C0G 0603	CGA3E1COG2A472J080AC
S_{1-4}	16m Ω 40V 10A	EPC2014C
D_{1-5}	2 \times 30V 2A Schottky	NSR20F30NXT5G
$D_{S,1-4}$	20V 0.5A Schottky	PMEG2010BELD
U_{1-2}	1.2A/5A 80V Gate Driver	LMG1205
$C_{bypass,1-4}$	0.1 μ F 25V 0201	GRM033C81E104KE14D
$R_{damp,1-4}$	5.1 Ω 25V 0201	RC0201JR-075RIL

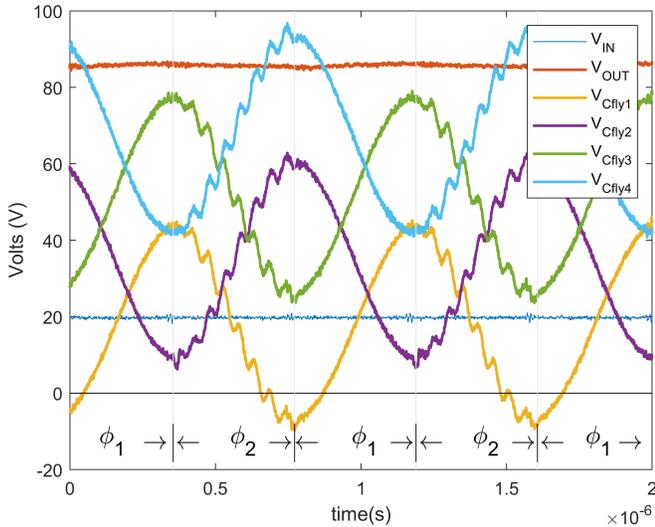


Fig. 12. Measured waveforms at heavy load depicting large voltage ripple across all fly capacitors leading to effective energy density utilization.

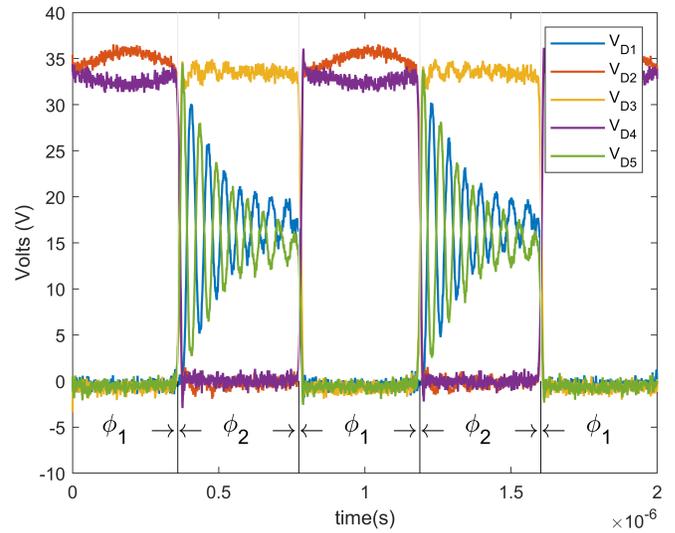


Fig. 13. Measured blocking voltage experiences by diodes D_{1-5} for $V_L = 20V$ and heavy load conditions.

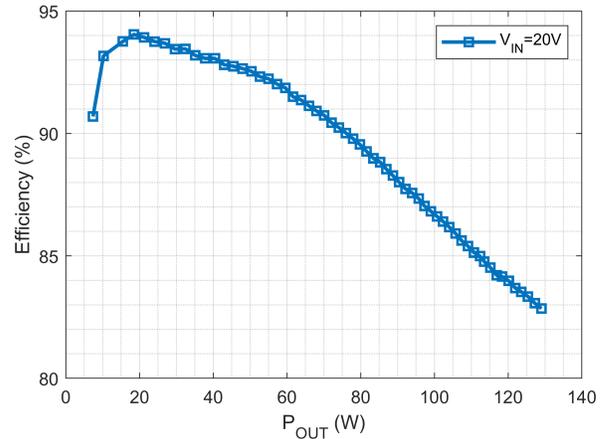


Fig. 14. Measured efficiency versus output power with $V_L = V_{IN} = 20V$.

IV. CONCLUSION

This paper demonstrates a new resonant dual extended LC-tank Dickson converter topology operating with two phases and a convenient 50% duty cycle for odd conversion ratios, avoiding the timing complexities of split-phase switching while still achieving complete soft-charging. Its switching devices do not impose a limit on fly capacitor voltage ripple allowing for increased energy density utilization and effective use of Class-I MLCC dielectrics. A discrete prototype measuring 11.45 mm \times 12.95 mm \times 2.8 mm recorded a maximum output power of 129 W before thermal failure, with a peak efficiency of 94%. This resulted in a very high measured power density of 311 kW/liter (5,096 W/inch³) despite using diodes for ease of implementation. Future fully synchronous variants are expected to yield further improvement without any added clock generation complexity.

TABLE II
COMPARISON WITH PRIOR ART

	Ellis [1]	Ye [3]	Macy [10]	This Work
Topology	1:5 Cockcroft-Walton	4:1 Cascaded Doubler	1:4 Dickson	1:5 Dickson
Switching Scheme	Split-Phase (Complex)	2-Phase (50% Duty)	Split-Phase (Complex)	2-Phase (50% duty)
Switch Type	GaN	MOSFET	GaN	GaN + Diodes
# of Inductors	1	2	1	2
Max C_{ry} Ripple	Switch Limited	Switch Limited	Switch Limited	Dielectric Limited
f_{sw}	744 kHz	100kHz	1.2 MHz	1.2 MHz
% Peak Eff.	94.9%	98.9%	92%	94%
$P_{\text{OUT-MAX}}$	190W	600W	263W	129W
$V_L @ P_{\text{OUT-MAX}}$	19.7V	15V	33V	19.8V
$V_H @ P_{\text{OUT-MAX}}$	92V	60V	117V	82.2V
Power Density (Best-fit Cuboid)	483 kW/L (7,920 W/inch ³)	133 kW/L (2,180 W/inch ³)	61.7 kW/L (1,011 W/inch ³)	311 kW/L (5,096 W/inch³)

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