UNIVERSITY OF CALIFORNIA, SAN DIEGO

Advanced CMOS Circuits for Microwave and Millimeter-Wave Communications

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Berke Cetinoneri

Committee in charge:

Professor Gabriel M. Rebeiz, Chair
Professor James F. Buckwalter
Professor Gert Cauwenberghs
Professor William S. Hodgkiss
Professor Lawrence E. Larson

2011

The dissertation of Berke Cetinoneri is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

_____

_____

_____

_____

_____
Chair

University of California, San Diego

2011

DEDICATION

To my parents, Ferdi and Sabahat

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

I still remember the days that lead to my Ph.D. journey at UCSD. During my last year in college in Turkey, I was applying to multiple universities in the United States for admission to a graduate program in electrical engineering and sending e-mails to the professors in my area asking for funding. Only one of them answered my e-mail and that was Prof. Gabriel Rebeiz. By a great chance, he was coming to Istanbul to attend a MEMS conference and was willing to talk to me. We met at the lobby of the Marmara Hotel in Taksim Square on a snowy day and I told him about what I did as an undergraduate student. He seemed to be impressed by the work I did, especially my internship project about a power amplifier design that was done with Yusuf Atesal. This lead to our admission to UCSD and my journey has started.

During the first days, Yusuf and I were sitting at the far end of the meeting table in our 6^{th} floor office, trying to understand what the people were talking about. At that time we did not know what we will be working on, so we were attending every RFIC, MEMS and antenna group meetings, going on for hours. Then, in about a year, the discussions started to make more sense as we took classes and learned more about our field. After working on many interesting yet challenging projects, we finally made our way to graduation from UCSD with a Ph.D. degree.

I would first like to thank my advisor Prof. Gabriel M. Rebeiz since he was the one who made this journey possible by accepting me to his research group at UCSD. He is a great advisor in many ways and I learned a lot from his experience. He trains his students not only in their technical field, but also in other aspects such as how to give a good presentation, and even how to talk and behave in professional environments. I truly understood the quality of my education when I was an intern at Qualcomm. Everything that he tries to teach is actually all you need to be successful in a company or in academia. His research lab is always made up of top quality state-of-the-art equipments that enable cutting-edge research. His broad technical insight, passion and enthusiasm in research lead to new ideas that result in major breakthroughs. I especially find two of his phrases very inspirational: ”I want you to build the impossible!” and ”Never give up!”. All of these have been a great motivation for me to complete my degree without giving up and encourage me to undertake bigger challenges in my future career.

Next, I would like to thank my dissertation committee members, Prof. Larry Larson, Prof. James F. Buckwalter, Prof. Gert Cauwenberghs and Prof. William Hodgkiss for their time, interest, and valuable comments about my research. UCSD is a great school to get a Ph.D. in electrical engineering and the courses that are offered are very valuable. The multidisciplinary aspect of the distinguished faculty makes the learning experience much more enriching.

I would also like to thank Prof. Yasar Gurbuz at Sabanci University, Istanbul, Turkey, who supported and encouraged both me and Yusuf to do a Ph.D. in the U.S.

As I mentioned at the beginning, I came to UCSD with Yusuf Atesal and we worked together in every project almost till the end. His technical knowledge and brightness made a great contribution to all of our projects, and his friendship made it possible to survive the sleepless and stressful tape-out periods. For this reason, I want to thank him first for being such a good companion in this long journey. I am sure that we will be working together again in the future.

Special thanks go to my closest friends Mehmet Uzunkol and Ozgur Inac, with whom I shared the same house for more than two years. We were "The Sabanci Mafia" in the group. I would also like to thank Mehmet Parlak for his friendship and support, and for inviting us to many of his fun events.

I would like to thank Yusuf Atesal, Jeong-Geun Kim, and Andy Fung for their contribution to the work in this thesis. I would also like to thank the team from U.S. Navy SPAWAR SSC Pacific in San Diego, namely, Dr. Richard A. Kroeger, Dr. Jon Losee, Dr. Charles Hicks, and Mr. Marc Rasmussen, for their contributions to the gamma-ray detector project in this thesis. Regarding the same project, my thanks also extend to Dr. Gary Tepper from Virginia Commonwealth University for his valuable comments and inputs.

There are many people in the TICS group that I would like to acknowledge here for their support and friendship: Michael Chang, Chris Galbraith, Carson White, Byung-Wook Min, Sang-June Park, Jeong-Geun Kim, Balaji Lakshminarayana, Kwang-Jin Koh, Mohammed El-Tanani, Tiku Yu, Jason May, Isak Reines, Alex Grichener, Dong-Woo Kang, Sang-Young Kim, Ramadan Alhalabi, Chirag Patel, Jen Edwards, Kevin Ho, Yusuf Atesal, Mehmet Uzunkol, Ozgur Inac, Fatih Golcuk, Ozan Dogan Gurbuz, Seyhmus Cacina, Tumay Kanar, Woorim Shin, Donghyup Shin, Yu-Chin Ou, Choul-Young Kim, Yi-Chyun Chiou, Chih-Chieh Cheng, Rashed Mahameed, Hojr Sedaghat Pisheh, Hosein Zareie and Chenhui Niu. I would also like to thank Romain Stefanini for making life enjoyable when he was with us in San Diego.

The support and encouragement of my parents, Ferdi and Sabahat Cetinoneri, was a great contributor in completing my Ph.D. degree. They have done everything to make sure that I get the best education since when I was a child and I always feel their good wishes and prayers for me when the times are tough. I can never forget their support, dedication and unending love throughout my life. They are a true blessing for me. I also thank to my close relatives for their great support and good wishes. I always see their excitement, warmth and love in their eyes

when I go back to Istanbul.

I would also like to thank George and Carol Hahn, who kindly hosted me and Yusuf by opening their home to us when we first arrived to San Diego, which started our friendship. They accepted both Yusuf and me as a part of their family, and I will always remember the great meals shared and times spent together. I am so happy that I got to know them. They became a part of my family.

The material in this dissertation is based on the following papers which are either published, or has been submitted for publication.

Chapter 2 is based on and mostly a reprint of the following paper:

- B. Cetinoneri, Y. A. Atesal, A. Fung, and G. M. Rebeiz, "W-band amplifiers with 6 dB noise figure and mW-Level 170-200 GHz doublers in 45-nm CMOS," submitted for publication in IEEE Trans. Microwave Theory and Tech., May 2011.

Chapter 3 is based on and mostly a reprint of the following papers:

- B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A miniature DC-70 GHz SP4T switch in 0.13-μm CMOS," IEEE MTT-S Int. Microwave Symp. Dig., pp. 1093-1096, Jun. 2009,
- Y. A. Atesal, B. Cetinoneri, and G. M. Rebeiz, "Low-loss 0.13-μm CMOS 50-70 GHz SPDT and SP4T switches," IEEE Radio Frequency Integrated Circuits Symp., Jun. 2009, pp. 127-130.

Chapter 4 is based on and mostly a reprint of the following papers:

- B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "An 8$\times$8 Butler matrix in 0.13-μm CMOS for 5-6 GHz multibeam applications," IEEE Trans. Microwave Theory and Tech., vol. 59, no. 2, pp. 295-301, Feb. 2011.
- B. Cetinoneri, Y. A. Atesal, J.-G. Kim, and G. M. Rebeiz, "CMOS 4$\times$4 and 8$\times$8 Butler matrices," IEEE MTT-S Int. Microwave Symp. Dig., pp. 69-72, May 2010.

Appendix A is based on and mostly a reprint of the following paper:

- B. Cetinoneri, Y. A. Atesal, R. A. Kroeger, G. Tepper, J. Losee, C. Hicks, M. Rasmussen, and G. M. Rebeiz, "A microwave-based gamma-ray detector," IEEE MTT-S Int. Microwave Symp. Dig., pp. 469-472, May 2010.

The dissertation author was the primary author of the work in these chapters, and coauthors (Prof. Gabriel M. Rebeiz, Dr. Yusuf A. Atesal, Dr. Jeong-Geun Kim, Dr. Andy Fung, Dr.

Richard A. Kroeger, Dr. Gary Tepper, Dr. Jon Losee, Dr. Charles Hicks, and Mr. Marc Rasmussen) have approved the use of the material for this dissertation.

Berke Cetinoneri
La Jolla, California
May, 2011.

VITA AND PUBLICATIONS

2002 - 2006	B. S. in Microelectronics Engineering, Sabanci University, Istanbul, Turkey
2006 - 2008	M. S. in Electrical Engineering, University of California, San Diego, La Jolla, California
2008 - 2011	Ph. D. in Electrical Engineering, University of California, San Diego, La Jolla, California

B. Cetinoneri, Y. A. Atesal, A. Fung, and G. M. Rebeiz, "W-band amplifiers with 6 dB noise figure and mW-Level 170-200 GHz doublers in 45-nm CMOS," *IEEE Trans. Microwave Theory and Tech.*, submitted for publication, May 2011.

B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "An 8×8 Butler matrix in 0.13-μm CMOS for 5-6 GHz multibeam applications," *IEEE Trans. Microwave Theory and Tech.*, vol. 59, no. 2, pp. 295-301, Feb. 2011.

Y. A. Atesal, B. Cetinoneri, M. Chang, R. A. Alhalabi, and G. M. Rebeiz, "Millimeter-wave wafer-scale silicon BiCMOS power amplifiers using free-space power combining," *IEEE Trans. Microwave Theory and Tech.*, vol. 59, no. 4, pp. 954-965, Apr. 2011.

Y. A. Atesal, B. Cetinoneri, K. Ho, and G. M. Rebeiz, "A two-channel 8-20-GHz SiGe BiCMOS receiver with selectable IFs for multibeam phased-array digital beamforming applications," *IEEE Trans. Microwave Theory and Tech.*, vol. 59, no. 3, pp. 716-726, Mar. 2011.

B. Cetinoneri, Y. A. Atesal, J.-G. Kim, and G. M. Rebeiz, "CMOS 4×4 and 8×8 Butler matrices," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 69-72, May 2010.

B. Cetinoneri, Y. A. Atesal, R. A. Kroeger, G. Tepper, J. Losee, C. Hicks, M. Rasmussen, and G. M. Rebeiz, "A microwave-based gamma-ray detector," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 469-472, May 2010.

Y. A. Atesal, B. Cetinoneri, R. A. Alhalabi, and G. M. Rebeiz, "Wafer-scale W-band power amplifiers using on-chip antennas," *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, pp. 469-472, May 2010.

Y. A. Atesal, B. Cetinoneri, K.-J. Koh and G. M. Rebeiz, "X/Ku-band 8-element phased arrays based on single silicon chips," *IEEE Int. Microwave Symp. Dig.*, pp. 1258-1261, May 2010.

B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A two-channel Ku-band BiCMOS digital beamforming receiver for polarization-agile phased-array applications," *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, pp. 127-130, Jun. 2009.

B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A miniature DC-70 GHz SP4T switch in 0.13-μm CMOS," *IEEE Int. Microwave Symp. Dig.*, pp. 1093-1096, Jun. 2009.

Y. A. Atesal, B. Cetinoneri, and G. M. Rebeiz, "Low-loss 0.13-μm CMOS 50-70 GHz SPDT and SP4T switches," *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, pp. 43-46, Jun. 2009.

G. M. Rebeiz, K. J. Koh, T. Yu, D. Kang, C. Y. Kim, Y. Atesal, B. Cetinoneri, S. Y. Kim, and D. Shin, "Highly dense microwave and millimeter-wave phased array T/R modules and Butler matrices using CMOS and SiGe RFICs," *IEEE Int. Symp. Phased Array Sys. and Tech.*, pp. 245-249, Oct. 2010.

W. Elsallal, D. Jensen, R. Palandech, J. Timmerman, J. West, Y. A. Atesal, B. Cetinoneri, and G. M. Rebeiz, "A SiGe-based Ku-band digital beamforming array for high speed on-the-move comm/radar system," *IEEE Int. Symp. Phased Array Sys. and Tech.*, pp. 868-875, Oct. 2010.

ABSTRACT OF THE DISSERTATION

Advanced CMOS Circuits for Microwave and Millimeter-Wave Communications

by

Berke Cetinoneri

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2011

Professor Gabriel M. Rebeiz, Chair

The thesis presents advanced circuits in CMOS for microwave and millimeter-wave communications. First, low-noise W-band amplifiers and mW-level 170–200 GHz output doublers in 45-nm Semiconductor-On-Insulator (SOI) CMOS technology are presented. The transistors are modeled using R/C extraction and full electromagnetic modeling. The measured f_t of a 30×1-μm transistor is 200–210 GHz at a bias current of 0.3–0.5 mA/μm. A 3-stage W-band amplifier shows a record noise figure of 6.0 dB and a saturated output power of 7.5–8.0 dBm with a power added efficiency of 9%, all at 95 GHz. The G-band balanced doubler results in an output power of 1 mW at 180 GHz. A W-band amplifier/G-band doubler chip is also demonstrated, with a peak output power of 0.5–1 mW at 170–195 GHz and a conversion gain of -2 – -1 dB. This work shows that 45-nm SOI CMOS, built for digital and mixed-signal applications, results in state-of-the-art performance at W-band and G-band.

Next, a miniature DC-70 GHz single-pole four-throw (SP4T), 50-70 GHz single-pole double-throw (SPDT), and single-pole four-throw (SP4T) switches built in a low-cost 0.13-μm CMOS process are presented. The DC-70 GHz SP4T switch is based on a series-shunt design with input and output matching circuits. Deep n-well (also called triple-well) CMOS transistors are used to minimize the substrate coupling. Also, deep trench isolation is used between the different ports to minimize the port-to-port coupling. The SP4T results in a measured insertion loss of less than 3.5 dB up to 67 GHz with an isolation of greater than 25 dB. The measured port-to-port coupling is less than 28 dB up to 67 GHz. The measured P1dB and IIP3 are independent of frequency and are 9-10 dBm and 20-21 dBm, respectively. The active chip area is 0.24$\times$0.23 mm^2. When this work was published, it represented the widest bandwidth SP4T switch in any CMOS technology to-date.

The 50-70 GHz single-pole double-throw (SPDT) and single-pole four-throw (SP4T) switches are based on tuned λ/4 designs with output matching networks. High substrate resistance together with deep trenches and isolation moats are used for low insertion loss. The SPDT and SP4T switches result in a measured insertion loss of 2.0 and 2.3 dB at 60 GHz, with an isolation of $>$ 32 dB and $>$ 22 dB, respectively. The measured output port-to-port isolation is $>$ 27 dB for both designs. The P1dB is 13-14 dBm with a measured IIP3 of $>$ 23 dBm for both switches. Both designs have a return loss better than -10 dB at all ports from 50 to 70 GHz. The active chip area is 0.39$\times$0.32 mm^2 (SPDT) and 0.59$\times$0.45 mm^2 (SP4T). When this work was published, it presented the lowest loss 60 GHz SPDT and SP4T switches and also the highest isolation SPDT switch in any CMOS technology to-date.

In another project, 5–6 GHz 8$\times$8 and Ku-band 4$\times$4 Butler matrices are presented in a 0.13-μm CMOS implementation. The 8$\times$8 design results in an insertion loss of 3.5 dB at 5.5 GHz, with a bandwidth of 5-6 GHz and no power consumption. The chip area is 2.5$\times$1.9 mm^2 including all pads. The 8$\times$8 matrix is mounted on a Teflon board with 8-antennas, and the measured patterns agree well with theory and show an isolation of $>$ 12 dB at 5–6 GHz. The 4$\times$4 design results in an insertion loss of 2.4 dB at 12 GHz with a bandwidth of 11–13 GHz. The chip area is only 0.85$\times$0.65 mm^2 including all pads, and the power consumption is $\sim$0 mA from a 1.5 V power supply. The 4$\times$4 matrix is mounted on a Teflon board with 4-antennas, and the measured patterns agree well with theory and show an isolation of $>$ 11 dB at 11–13 GHz. CMOS Butler matrices are an excellent candidate for MIMO systems, and can also replace small-element phased-array systems for high-gain transceivers. The applications areas are in high data-rate communications.

Finally, a contactless, microwave-based gamma ray detector for detecting low-energy gamma ray photons is presented as an appendix. The detection is based on a microwave cavity perturbation method, and uses a reflection-type cavity resonator with a detector-grade CZT crystal. The reflected power from the cavity is measured and this monitors the changes in the photoconductivity of the CZT crystal in the presence of a gamma-ray. A gamma ray detection sensitivity of < 100 keV is achieved at room temperature. The proposed system can be used in homeland security or radioactive material characterization applications.

Chapter 1

Introduction

1.1 Thesis Overview

This thesis presents advanced circuits for microwave and millimeter-wave communications using CMOS technology. Millimeter-wave CMOS circuits are an active research topic in the past few years with a broad range of applications. Some essential components are the low-noise amplifier for receive applications, and a transmitter source which is capable of generating greater than 1 mW of power above 100 GHz. Hence, the second chapter is based on the demonstration of a low-noise W-band amplifier and mW-level 170–200 GHz output doublers. For a multi-band millimeter-wave transceiver system, high performance single-pole multiple-throw switches are required and various CMOS switches are presented which show a measured state-of-the-art insertion loss and isolation up to 67 GHz. The multi-band operation can be combined with multiple simultaneous beams, which is made possible by the use of Butler matrices, and 8×8 and 4×4 Butler matrices are presented at 5–6 GHz and at 12 GHz, respectively. As an appendix, an interesting project for detecting gamma-rays using microwave radiation is presented.

Chapter 2 presents a W-band low-noise amplifier with a record noise figure and balanced frequency doublers capable of high output power at 170–200 GHz range. These circuits are fabricated using IBM's 45-nm Semiconductor-On-Insulator (SOI) CMOS technology, which was developed for digital and mixed-signal circuits with an f_t of 485 GHz referenced to the transistor and therefore offers a lot of potential for 90–200 GHz applications. The chapter starts with an analysis of the SOI CMOS technology in detail and presents the measured and simulated transistor-level results. Then, the W-band low-noise amplifier design is discussed and the mea-

sured results are presented. Next, a balanced doubler design is demonstrated with simulations showing the doubler optimization and the measured results are discussed in detail. The amplifier and the doubler designs are eventually cascaded and the measured results show a peak output power of 0.5–1 mW at 170–195 GHz and a conversion gain of -2 – -1 dB. The chapter concludes with performance summary and comparison tables, which indicate that the circuits built using 45-nm SOI CMOS technology result in state-of-the-art performance at W-band and G-band.

Chapter 3 demonstrates millimeter-wave single-pole multiple-throw CMOS switches, which are becoming increasingly important for multi-band systems such as automotive radars, narrowband ISM and Giga-bit-per-second (Gbps) communication systems at 24 and 60 GHz. A miniature DC–70 GHz single-pole four-throw (SP4T), 50–70 GHz single-pole double-throw (SPDT), and single-pole four-throw (SP4T) switches are built using 0.13-μm CMOS process. Several key transistor and CMOS technology features such as deep n-well transistors, high substrate contact resistance, and deep trench isolation are discussed. The DC-70 GHz SP4T switch is based on a series-shunt design with deep n-well CMOS transistors to improve the performance and occupies an active chip area of 0.24×0.23 mm^2. Next, 50–70 GHz single-pole double-throw (SPDT) and single-pole four-throw (SP4T) switches, which are based on tuned λ/4 designs with output matching networks, are presented. Finally, the insertion loss, isolation, and large-signal measurement results are presented.

Chapter 4 presents 5–6 GHz 8×8 and Ku-band 4×4 Butler matrices in 0.13-μm CMOS technology. The lumped-element design is discussed in detail with an emphasis on how the on-chip cross-overs are realized with good isolation. The fabricated Butler matrix chips are mounted on a Teflon board with 8 or 4 antennas, and the input/output matching networks are designed by considering the bondwire transitions from the chip to the board. Complete pattern and gain measurements versus frequency are presented and the measured patterns agree very well with simulations. A modified 8×8 matrix is also shown, where the angular coverage can be improved by introducing phased delay before the antennas using switched CMOS L-C networks.

Appendix A demonstrates a microwave-based gamma-ray detector. The system is developed mainly for homeland security applications in order to detect low-energy gamma-ray photons at room temperature with high energy resolution and good efficiency. The operation principle and the system-level design is discussed in detail, and the measurement results are presented. Next, new cavity designs, which can achieve higher electric field by applying a high DC voltage, are presented with initial simulation results for low-energy single photon detection. The proposed microwave-based detection principle may result in an improved performance.

Chapter 2

W-Band Amplifiers with 6 dB Noise Figure and mW-Level 170-200 GHz Doublers in 45-nm CMOS

2.1 Introduction

Millimeter-wave and Terahertz applications of SiGe and CMOS circuits are an active research topic in the past few years with applications in passive and active imaging systems [1–3], short-distance high-data rate communications [4], and sensing. Also, it is possible to integrate an efficient antenna in the SiGe and CMOS backend above 100 GHz, thereby removing the need for transitions in and out of the wafer, which are very lossy. SiGe has lead the way in this area due to the high f_t and more mature millimeter-wave back-end [5–7], and CMOS circuits are currently being demonstrated at 100–200 GHz [8]. Some essential components are the low-noise amplifier for receive applications, and a medium power amplifier or a source which is capable of generating mW level power in the 200 GHz range.

CMOS amplifiers at 90–150 GHz have been demonstrated using 90-nm and 65-nm technologies [9–11]. Also, CMOS oscillators were demonstrated at 200–600 GHz, but with very low power and poor phase noise [12, 13]. In fact, the phase noise of fundamental and harmonic CMOS oscillators is not quoted in all published papers. We believe that a better way to obtain RF power at 200–400 GHz is to use a low phase-noise mm-wave oscillator with a high performance PLL and an amplifier/multiplier chain (Fig. 2.1). The final phase noise increases by n^2, but is still much lower than oscillators which are operating close to f_{max}. Recently, 45-nm SOI CMOS,

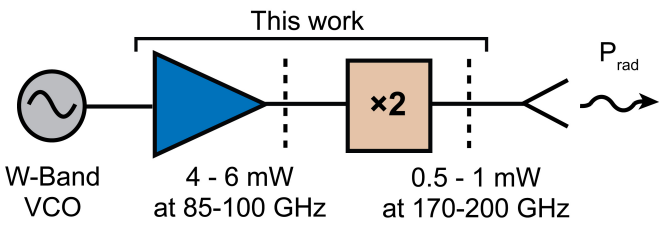


Figure 2.1: Block diagram of W-to-G-band multiplier chain.

which was developed for digital and mixed-signal circuits with an f_t of 485 GHz referenced to the transistor [14], was used to obtain low-noise amplifiers with record noise figure of 3.3–5.7 dB at 45–85 GHz, respectively [15]. The 45-nm SOI CMOS technology has therefore a lot of potential for 90–200 GHz applications and this paper presents a low-noise amplifier with record W-band noise figure, and record output power at 170–200 GHz using balanced doublers.

2.2 Technology

The IBM 45-nm SOI CMOS process cross-section is shown in Fig. 2.2. The transistor body is partially depleted and contained inside a 225-nm thick buried oxide, which isolates the transistor from the 13.5 Ω-cm silicon bulk. There are 11 metal layers above the device layer built using copper except the 2.2-μm thick aluminum top metal LB. The shielded coplanar waveguide (CPW) transmission line is designed using LB for the signal line and B3 for the ground plane, and the LB side grounds are connected to B3 using UA and UB metal layers. A signal line width of 8 μm with 9 μm spacing to the side grounds results in a 50 Ω transmission line at millimeter-wave frequencies.

The floating-body NFET devices in the IBM model library are used in the amplifier and doubler designs. The SOI process offers a superior performance compared to the bulk CMOS technology due to reduced source/drain junction capacitances and improved device isolation. IBM reports a peak f_t of 485 GHz with a relaxed poly-pitch layout referenced to a 30-μm device at the polysilicon layer [14]. However, the transistors in the available design kit have the minimum poly-pitch layout, which increases the terminal capacitances and lowers the peak f_t to 340 GHz. Furthermore, the transitions from the transistor up to the top metal result in added via resistance and capacitance, which significantly deteriorate the transistor performance. A 30×1-μm common-source transistor test cell is shown in Fig. 2.3 and is measured using a TRL calibration up to the reference planes. This measurement includes the transitions and associated parasitics from the top metal down to the transistor, and the measured f_t is 200 GHz at 0.3 mA/μm current

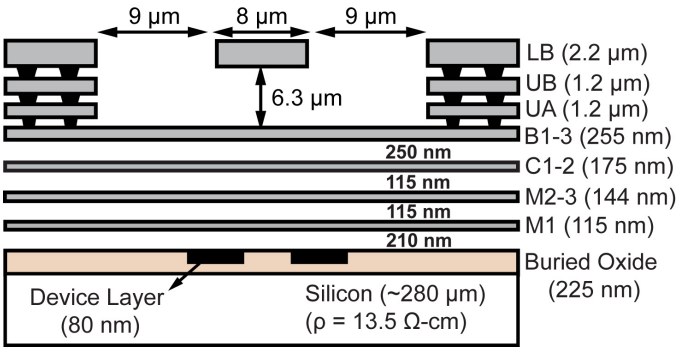


Figure 2.2: 45-nm SOI CMOS process metal stack-up and 50 Ω T-line cross-section (not to scale). All metal layers are copper except the aluminum top metal.

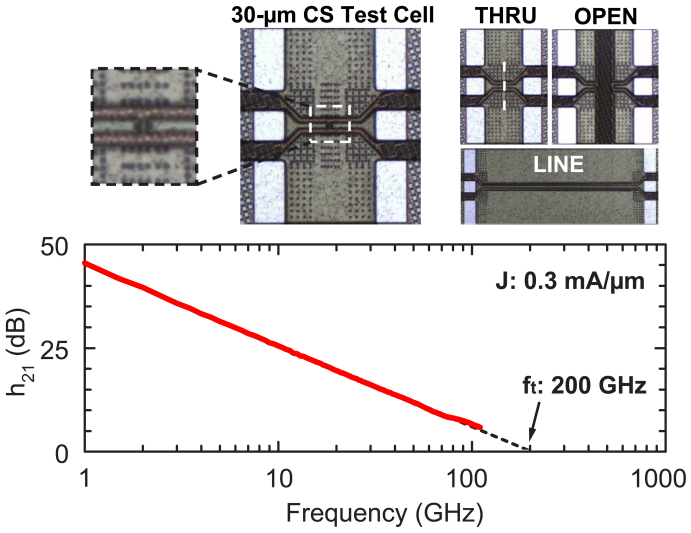


Figure 2.3: Measured f_t of a 30×1-μm common-source transistor using a TRL calibration.

density.

The physical layout of a 30×1-μm transistor is shown in Fig. 2.4. The transistors have dummy polysilicon gates at the outer edges for better device matching. The default transistor model from the IBM library does not fully account for the metal resistances and metal-metal/metal-poly parasitic capacitances since the process is developed for digital and mixed-signal applications. In particular, accurate modeling of the gate resistance is critical for the transistor gain and stability. Therefore, all of the metal and polysilicon layers at the transistor gate and drain are extracted up to M2 using an R/C parasitic extraction tool (Calibre [16]). Also, the source is extracted up to the surrounding M1 ground plane. Since the source connections are not included in the EM model and the parasitic inductances are not captured in the R/C extraction, extensive care is taken in the layout in order to establish a strong ground definition. Several blocks of stacked vias are used to connect the top level grounds (LB and B3 layers) to M1 and a wide M1 plane is used close to transistor source so as to minimize any undesired inductances that can degrade the device performance.

The vertical transition between the LB and M2 metal layers is 8.9 μm, and both gate and drain sections are simulated together to include the parasitic electromagnetic (EM) coupling between them using a 2.5D EM solver (Sonnet [17]). The metal layers from LB down to B1 are modeled using the thick-metal model in Sonnet with multiple number of sheets. More than two sheets are used for the top metal layers, LB in particular, where the vertical thickness is comparable to the trace width. The metal and via resistances are taken into account as specified in the IBM process design manual.

Fig. 2.5 shows the effect of the parasitics on the transistor f_t and noise figure. The simulated peak f_t of the IBM transistor model is 300-340 GHz and decreases to 200–220 GHz at a bias current of 0.3–0.6 mA/μm when all transitions are modeled (Fig. 2.5a-b). The minimum noise figure (NF_{min}) also shows a similar trend when the parasitics are included and the lowest NF_{min} is achieved at 0.1–0.3 mA/μm current density (Fig. 2.5c). The added parasitics slightly change Γ_{opt} away from the *r=1* circle on the Smith chart. As seen in Fig. 2.5b, there is not much improvement in f_t once the current density exceeds 0.3 mA/μm, so the transistor can be biased close to 0.3 mA/μm as a trade-off between high f_t and low noise figure. The measured f_t of the 30×1-μm common-source test cell at 0.2–0.5 mA/μm current density is consistent with simulations.

The unilateral power gain of the transistor is plotted in Fig. 2.6a together with the measured maximum available gain (MAG) and maximum stable gain (MSG). The transistor

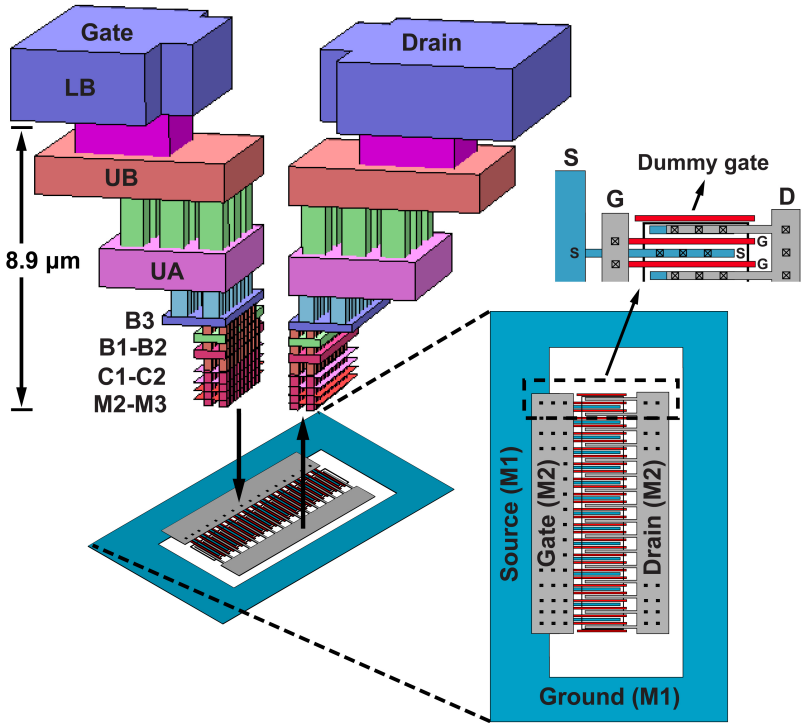


Figure 2.4: Modeling of transition from top metal down to transistor level and simplified layout of a 30×1-μm transistor.

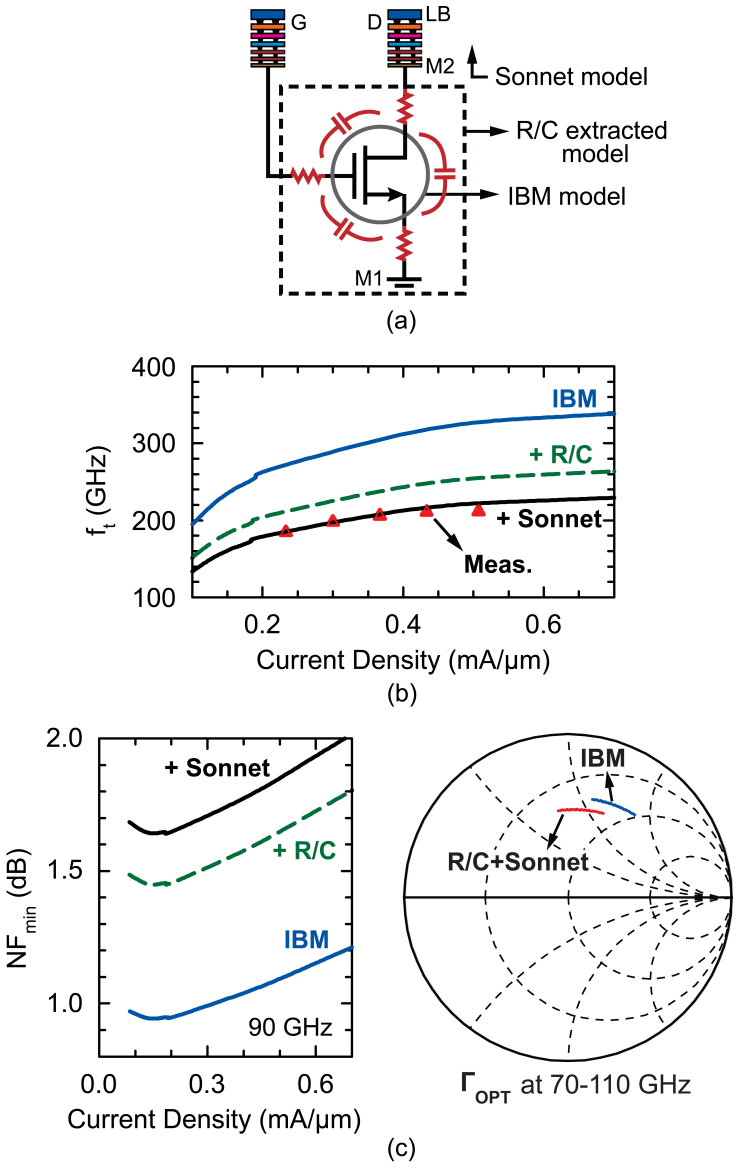


Figure 2.5: (a) Transistor-level modeling of interconnect parasitics. The effect of parasitics (b) on f_t and (c) on NF_{min} and Γ_{OPT} (30×1-μm transistor used).

f_{max} is calculated from the measured unilateral power gain (U) curve and is 200±5 GHz for a current density of 0.2-0.5 mA/μm [18] (Fig. 2.6b). This is lower than the IBM model (referenced to the transistor itself) which predicts an f_{max} of 460–480 GHz at this current density. The MAG and MSG curves show that the transistor becomes unconditionally stable above 90 GHz.

Fig. 2.7a presents the effect of parasitics on the MAG of the same transistor. The measured peak MAG is 9 dB with 0.3 mA/μm current density at 90 GHz, and agrees well with simulations. Fig. 2.7b is the measured MAG versus frequency at different current densities. As the current density increases, the MAG also increases, but it rolls off at a lower frequency. This is the reason for the decrease in MAG once the current density exceeds 0.3 mA/μm. For lower frequencies, the MAG smoothly increases as the current density is increased, and the simulated and measured MAG at 75 GHz is shown in Fig. 2.7c as an example.

Another question that can arise about the transistor modeling is how the level of R/C extraction affect the transistor performance and what happens when all the metals up to the top metal layer are extracted without any Sonnet modeling. Fig. 2.8a-d shows how the f_t, f_{max}, MAG, and the input impedance change for different R/C extraction scenarios, and how they compare to the Sonnet model. In Fig. 2.8a, the green curve is the IBM+R/C extraction up to M2 and the black curve is the Sonnet model applied on top of it. The orange curve is the IBM+R/C extraction up to top metal layer LB, which gives a nearly identical response compared to the Sonnet model. The R/C extraction up to the top metal yields slightly more pessimistic results for f_{max} and MAG (Fig. 2.8b-c). The input impedance is also affected by the level of extraction, and both the Sonnet and top metal R/C extraction are close to the measured impedance at 70-110 GHz (Fig. 2.8d). Based on these analyses, it can be concluded that the R/C extraction is sufficient to model the transitions from the transistor up to the LB metal without any Sonnet modeling.

2.3 W-Band Amplifier

2.3.1 Design

The W-band amplifier is shown in Fig. 2.9 and is based on a three-stage common-source design using floating-body transistors. The first two stages are designed with 30×1-μm transistors and the device size is increased to 40×1-μm at the third stage for high output power. The current density is set to be 0.3 mA/μm for all stages under nominal bias conditions (discussed in Section 2.2).

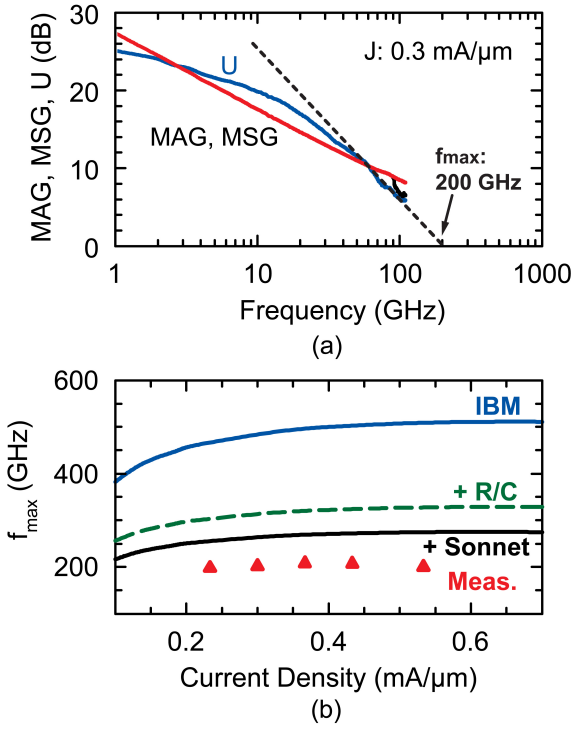


Figure 2.6: (a) Measured U, MAG, and MSG vs. frequency up to 110 GHz, and (b) simulated and measured f_{max} vs. current density.

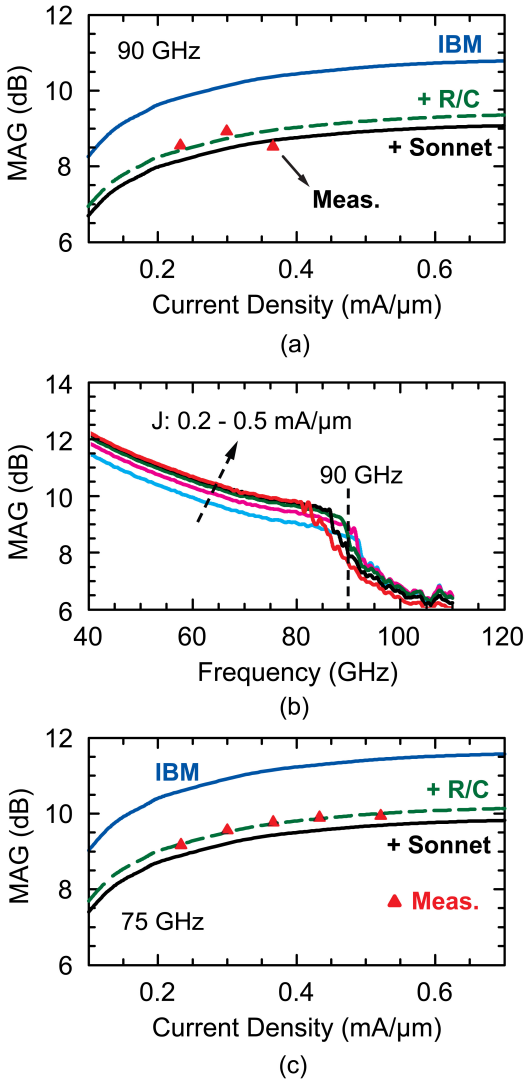


Figure 2.7: (a) The effect of parasitics on the MAG at 90 GHz, (b) measured MAG vs. frequency for different current densities, and (c) measured MAG at 75 GHz.

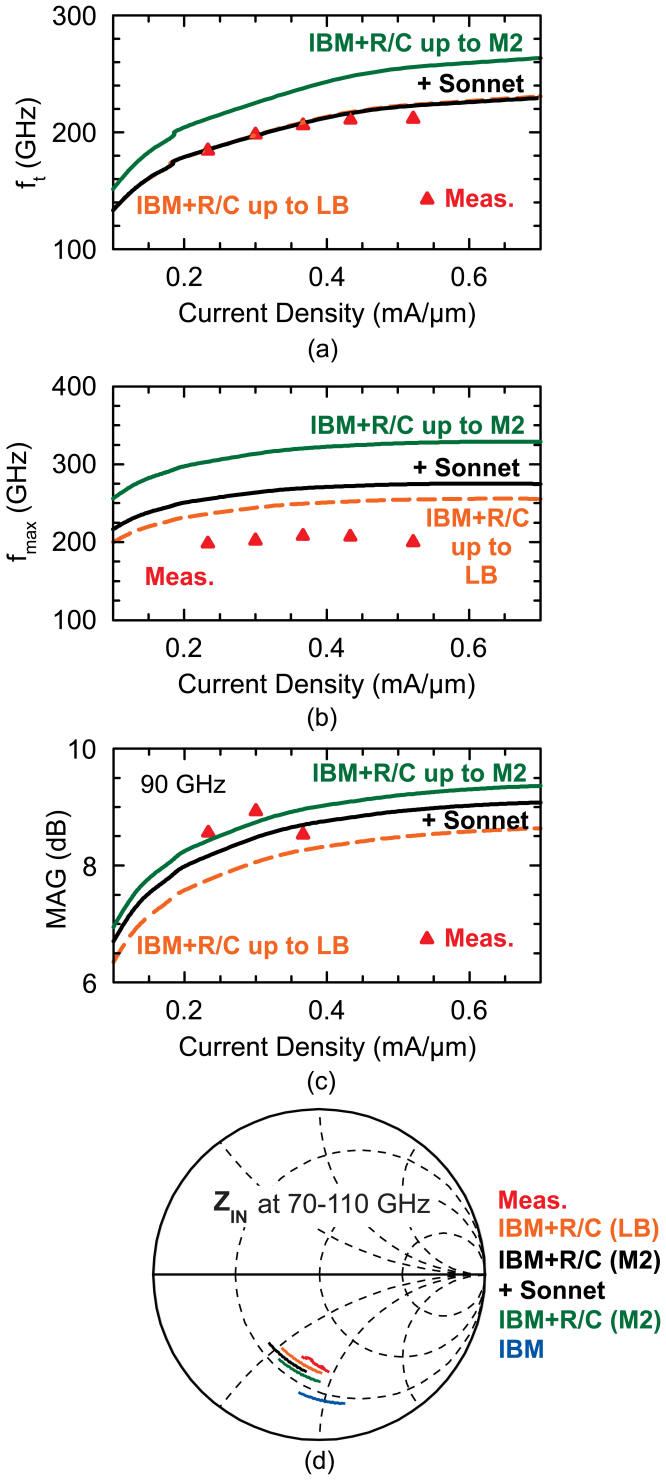


Figure 2.8: The effect of different modeling scenarios on (a) f_t, (b) f_{max}, (c) MAG, and (d) input impedance at 70-110 GHz.

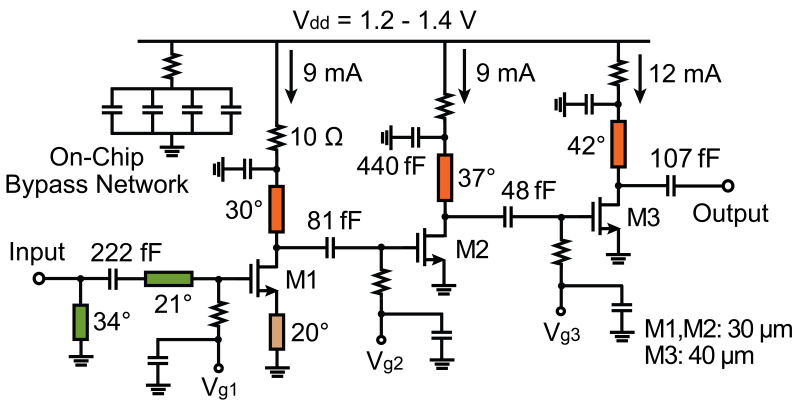


Figure 2.9: Schematic of the W-band amplifier.

All transmission lines and stubs are implemented using the 9-8-9 μm (50 Ω) grounded CPW lines with a loss of 1.1 dB/mm and a Q of 15 at 90–100 GHz according to Sonnet simulations. Shunt 440 fF capacitors, which are close to self-resonance at 90 GHz, are placed at the end of the matching stubs and provide a low impedance to ground at 80–100 GHz. Wideband on-chip bypass networks, composed of a 4 Ω polysilicon resistor in series with 0.3–2 pF thick-oxide capacitor banks, are implemented and connected to the power supply lines to prevent any oscillations due to interstage coupling. Also, 10 Ω resistors are placed in series with the drain matching stubs to further improve the stability at an expense of $\sim$0.1 V at the drain node. These resistors are used as a conservative design measure since this was the first implementation of this process at 90–200 GHz. The gate biasing is done by using a 3 kΩ resistor, and a simple voltage divider is used at the bias pad to provide a high impedance path to ground and also decrease the sensitivity to the applied voltage (not shown).

A shorted stub is used at the source of the first-stage transistor and acts as a degeneration inductor, which increases the real part of the impedance seen at the gate. This results in two beneficial effects on the amplifier's RF performance. First, a wideband input impedance is achieved when combined with the low-Q matching sections at the input ($S_{11} <$ -10 dB at 84–103 GHz). Second, $\Gamma_{\rm opt}$ at the input of the first stage moves toward the 50 Ω region on the Smith chart and results in a simultaneous gain and noise figure match after the input matching network.

The high-pass interstage matching networks are composed of transmission lines at the $V_{\rm dd}$ paths and interstage capacitors. All of the capacitors are implemented using the vertical natural capacitor model (vncap) found in the IBM design kit. The capacitance is formed between the inter-digitated metal fingers composed of C1 to B3 metal layers. The lower metal layers are not used since they result in higher parasitic shunt capacitance per 1 fF of series capacitance,

which degrades the performance at millimeter-wave frequencies.

The simulated gain of the amplifier is 13.5 dB at 90 GHz with a 3-dB bandwidth of 85–101 GHz. The input and output return losses are wideband due to low-Q matching networks (S_{22} < -10 dB at 82 – >110 GHz). The simulated NF is 5.3–4.6 dB at 90–100 GHz. The simulated saturated output power ($P_{\rm sat}$) and compression point ($P_{\rm 1dB}$) at 90 GHz are 8.0 dBm and 5.5 dBm, respectively, with a peak power added efficiency (PAE) of 12% and a 1.4 V supply.

2.3.2 Measurements

The chip microphotograph with an expanded view around the transistors is shown in Fig. 2.10a. The vertical dimension is determined by the input and output 100-μm pitch GSG pads, hence, the transmission lines and stubs are not meandered. The resulting chip size is 0.58×0.55 mm^2 including the pads.

The small-signal measurements of the W-band amplifier is performed using an Agilent network analyzer (PNA E8361A) with 75–110 GHz frequency extenders and 1-mm coaxial cables. The calibration is done up to the probe tips using an SOLT calibration substrate. The measured S-parameters are shown in Fig. 2.10b. The W-band amplifier has 10.7 dB gain at 95 GHz and a 3-dB bandwidth of 92–100 GHz for three different samples. Both input and output return losses are < -10 dB at 87–110 GHz and the measured reverse isolation (S_{12}) is < -35 dB up to 110 GHz (not shown).

The noise figure (NF) is measured using an Agilent E4448A spectrum analyzer with a W-band noise source at the DUT input, and a waveguide amplifier/mixer down-conversion setup at the output port. The measured NF is 6.0 dB at 95 GHz as shown in Fig. 2.11 with nominal biasing (0.3 mA/μm) and is 5.9–6.1 dB over a wide range of bias current. NF measurements at 100 GHz could not be done since the W-band waveguide amplifier operated up to 96 GHz.

The large signal measurements are done with WR-10 waveguide components and a 1-mm coaxial setup. Agilent E8257D signal generator was used with a tripler to generate a W-band signal and a waveguide variable attenuator was used at the input for power sweeps. The measured output $P_{\rm 1dB}$ and $P_{\rm sat}$ at 95 GHz are 5.2 and 7.5 dBm, respectively with a 1.4 V supply and the measured peak PAE is 9.0% at 95 GHz (Fig. 2.12). At $P_{\rm sat}$, the current is 15 mA in the last stage which results in 0.15 V drop across the 10 Ω resistor and a drain voltage of 1.25 V.

The measured $P_{\rm sat}$ versus frequency is shown in Fig. 2.13a and is > 6 dBm at 90–100 GHz with nominal bias conditions. $P_{\rm sat}$ was also measured by varying the supply voltage at 95 GHz (Fig. 2.13b) and it can be increased up to 8 dBm with a 1.4 V supply by optimizing the

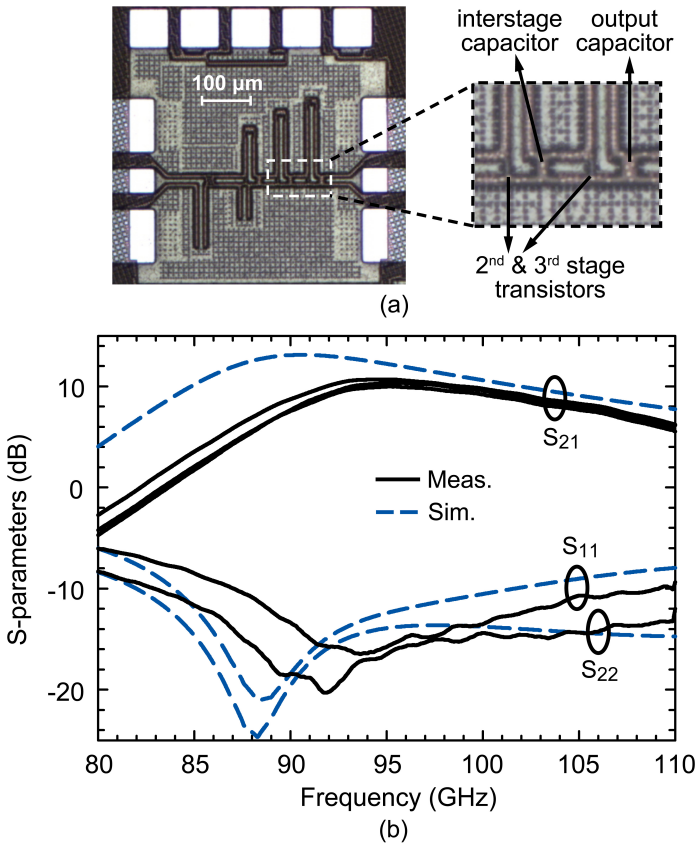


Figure 2.10: (a) Microphotograph of the W-band CMOS amplifier (0.58×0.55 mm^2) and (b) measured S-parameters on three different samples (only S_{21} is shown for the three samples).

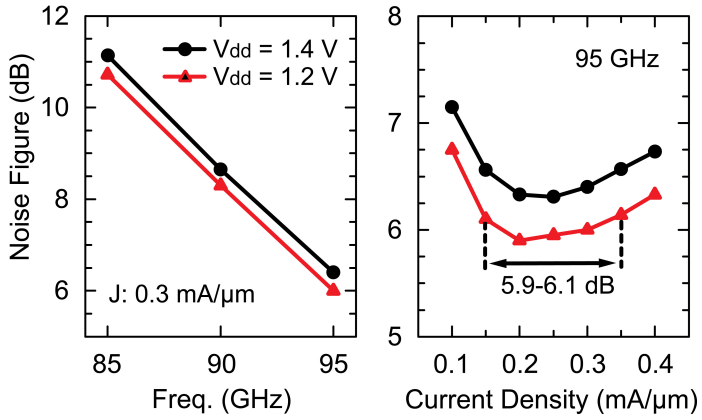


Figure 2.11: Measured noise figure of the amplifier versus frequency and current density.

gate bias points. Two other amplifiers from different dies were also measured and they yielded a P_{sat} above 7.6 dBm with a 1.4 V supply at 95 GHz, showing that the amplifier can generate a high output power even with standard process variations.

2.4 W-to-G-Band Doubler

2.4.1 Design

The doubler is an active balanced design as shown in Fig. 2.14. The single-ended input is converted to a differential signal using a passive balun and fed into the balanced transistor pair. The drain nodes are connected together which creates a broadband short circuit for the fundamental and odd harmonics, but the even harmonics are combined in phase. As the transistor size is increased, the doubler can yield more power, but a higher input power is required. The input power to the doubler is 6–7 dBm (see Section III) and a 30×1-μm transistor is simulated to achieve maximum conversion gain at this input power. Although a smaller finger width can achieve slightly more conversion gain, the finger width of 1 μm is chosen due to stability concerns (Fig. 2.15a). When the transistor is simulated without any parasitic extraction, it becomes unstable for finger widths $\leq$ 1 μm. Since this was the first design trial in this process, a conservative approach is taken and the finger width is limited to 1 μm.

Second harmonic reflectors are used at the transistor inputs to further improve the doubler conversion gain [19, 20]. The 220 fF capacitors at the reflector end operate close to self-resonance, thus providing a very low impedance (0.6 Ω) for the second harmonic at 180 GHz. The position and length of the reflectors are adjusted using EM simulations (Sonnet) to ensure

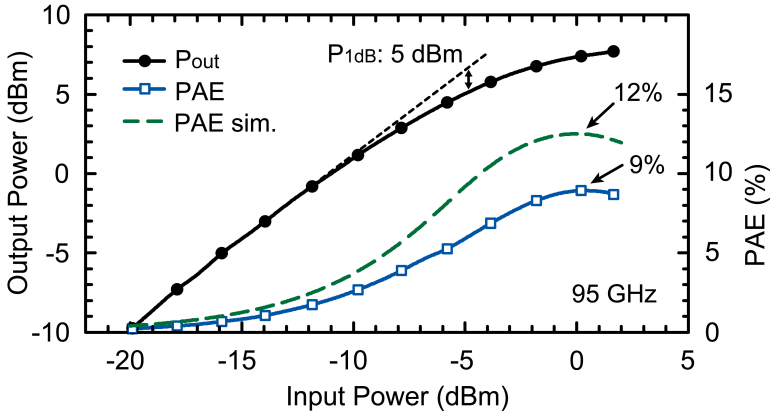


Figure 2.12: Measured output power and PAE versus input power at 95 GHz.

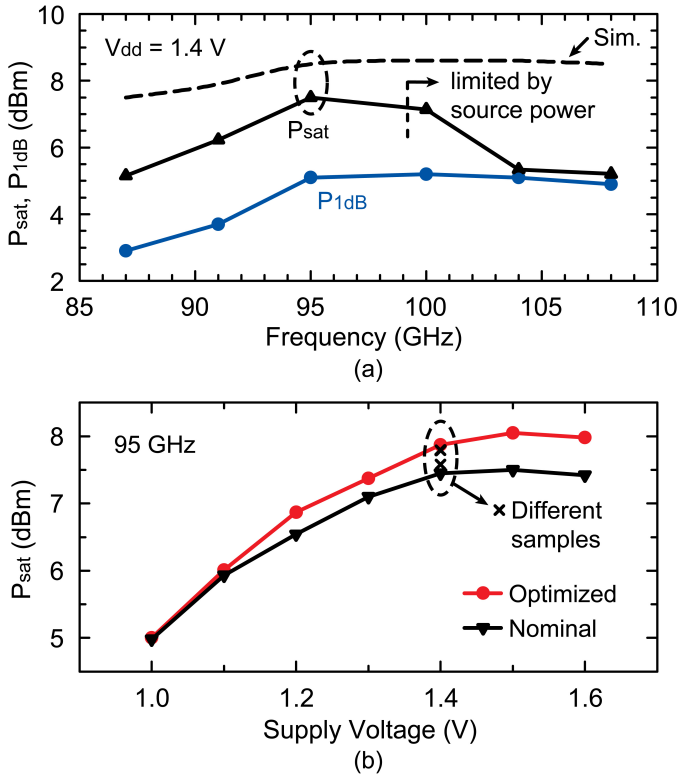


Figure 2.13: Measured (a) Psat and P1dB vs. frequency, (b) Psat vs. supply voltage.

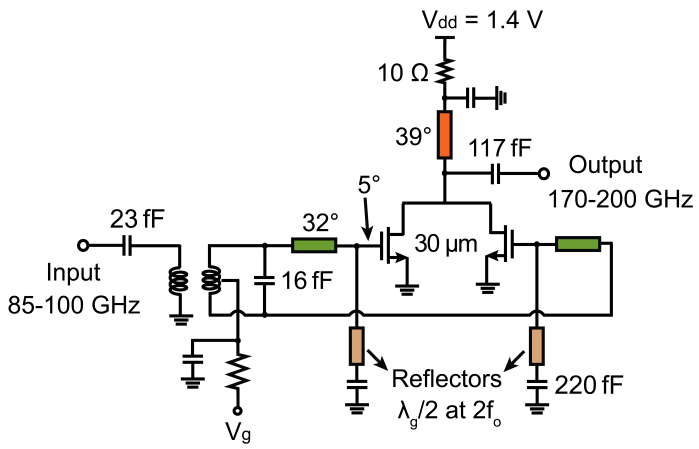


Figure 2.14: Schematic of the W-to-G-band balanced doubler.

a simultaneous short circuit for the second harmonic and a high impedance for the fundamental tone at 90 GHz. Simulations show that the reflectors result in a 2 dB increase in the output power at 170–185 GHz (Fig. 2.15b).

The transistor bias condition is crucial for doubler efficiency since the conduction angle should be set correctly to maximize the second harmonic tone at the output [21]. If the drain current waveform is assumed to be a rectified cosine pulse, it can be represented by Fourier series expansion as:

$$I_{\mathrm{d}}(\mathrm{t}) = \mathrm{I}_0 + \mathrm{I}_1\cos(\omega_1\mathrm{t}) + \mathrm{I}_2\cos(\omega_2\mathrm{t}) + ... \tag{2.1}$$

and the coefficients for n $\geq$ 1 are

$$I_{\mathrm{n}} = \mathrm{I}_{\mathrm{max}}\frac{4\mathrm{t}_0}{\pi\mathrm{T}}\left|\frac{\cos(\mathrm{n}\pi\mathrm{t}_0/\mathrm{T})}{1-(2\mathrm{n}\pi\mathrm{t}_0/\mathrm{T})^2}\right|, \tag{2.2}$$

where $\mathrm{I}_{\mathrm{max}}$ is the maximum drain current, t_0 is the duration of the pulse, and T is the period of fundamental frequency. When (2.2) is solved to maximize I_2, t_0/T = 0.35, which corresponds to a conduction angle of 125°. Therefore, the transistor gates need to be biased below the threshold voltage (V_{th} = 270 mV) for optimum doubler operation and this is shown by the large-signal simulations in Fig. 2.15c.

The input balun is designed using Sonnet (Fig. 2.16). The magnetic coupling occurs vertically between the primary coil designed using the top metal LB and the secondary coil composed of stacked UB and UA metals. The distance to the ground plane is 20 μm on each side and the trace width is 5 μm. A 23 fF series capacitor at the input, the balun, and a 16 fF capacitor at the balun output form a multistage matching network and provide a wideband match at the doubler input (S_{11} < -10 dB at 84–100 GHz). The simulated phase and amplitude

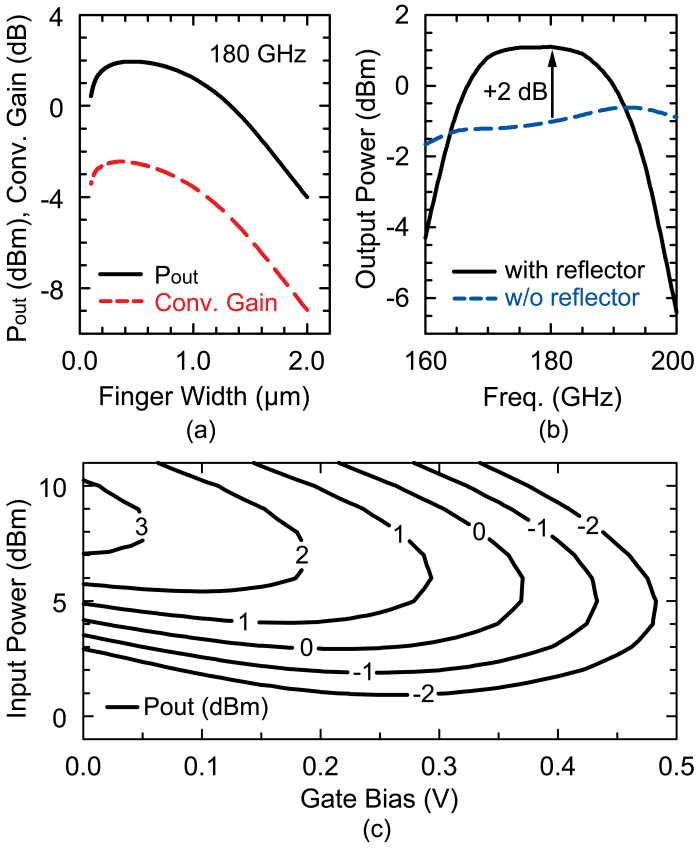


Figure 2.15: Simulations showing (a) output power and conversion gain of the doubler vs. finger width (30-μm wide transistors), (b) effect of reflector on the output power of the doubler, and (c) output power contours for different gate bias voltages and input power levels.

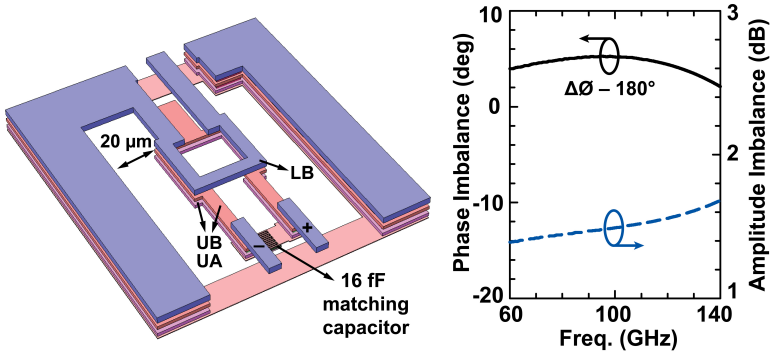


Figure 2.16: 3-D view of the doubler input balun and simulated phase/amplitude imbalance between the differential ports.

imbalance between the differential ports is $< 5^{\circ}$ and $<$ 1.5 dB at 80–100 GHz, respectively.

All the transmission lines and interconnects at the input and output of the doubler are modeled using Sonnet. Due to maximum metal density requirement for the lower metals, the B3 ground plane under the transmission-lines needs to be extensively meshed. Fig. 2.17a shows a shielded CPW line with a ground plane mesh designed for 75% maximum metal density. This effect can be captured in EM simulations and results in 0.1 dB increase in line loss per mm and a Q drop of 10% at 180 GHz. A 600-μm long line was measured at 160–200 GHz, and the effect of the pads and the CPW transition were de-embedded using a GSG thru-section. The measured line loss is 2.2 dB/mm at 180 GHz, which is 0.7 dB higher than simulations (1.5 dB/mm) (Fig. 2.17b). The increase in line loss over simulations has been measured by several groups [10, 22] and is perhaps due to the thin Ta and W adhesion layers used in the fabrication process [23].

2.4.2 Measurements

The chip microphotograph is shown in Fig. 2.18a and the DC bias for the gate and drain nodes is supplied using the top pads. The input and output pads are compatible with both 100-μm and 80-μm pitch GSG probes. The section after the input balun is designed symmetrically to maintain balanced operation and the transistors in the doubler core are placed in close proximity to each other so as to minimize the distance to the common drain node. The second harmonic reflectors are meandered to reduce the chip area and the total size is 0.69$\times$0.49 mm^2 including the pads.

The S-parameter measurements of the doubler requires two different setups since the input and output are at different frequencies. The input return loss is measured with the same setup as the W-band amplifier and is $<$ -10 dB at 86–108 GHz. The output return loss is measured using a 140–220 GHz (G-band) frequency extension setup and is $<$ -10 dB at 153–175 GHz (Fig. 2.18b).

The large signal characterization is performed using a complete waveguide setup with WR-10 and WR-5 sections at the input and output, respectively (Fig. 2.19). All measurements are referenced to the GSG input and output pads. A mechanically tuned Gunn-diode oscillator is used at the input and is followed by a variable attenuator for controlling the input power. The input power is monitored using a 10-dB coupler and an Agilent E4417A power meter, and the output port is directly connected to an Erickson power meter [24]. The measured peak output power is -0.8 dBm at an input power of 6–7 dBm with -8.0 dB conversion gain at 180 GHz with a constant gate bias (V_g) of 0.24 V for all input power levels (Fig. 2.20a). Fig. 2.20b

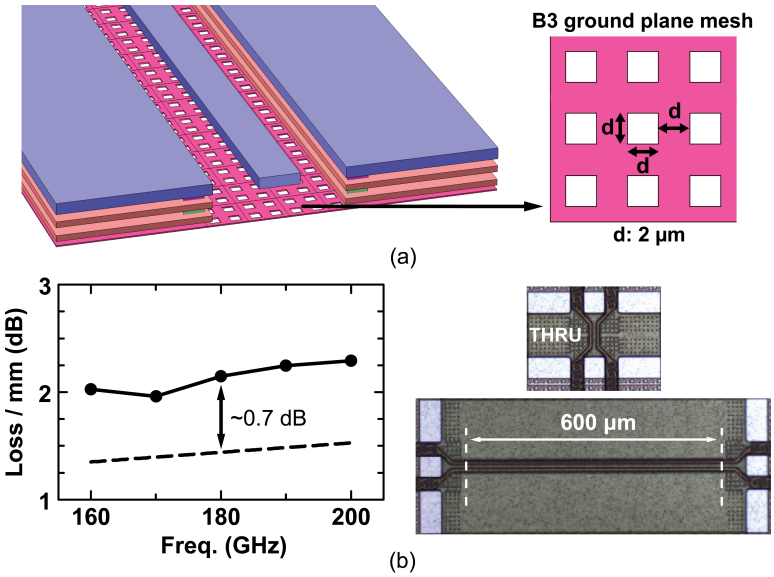


Figure 2.17: (a) CPW transmission line with ground plane meshing. (b) Measured (solid) and simulated (dashed) line loss/mm for a 50 Ω T-line. A 600-μm line and GSG thru pads are used for line loss measurements.

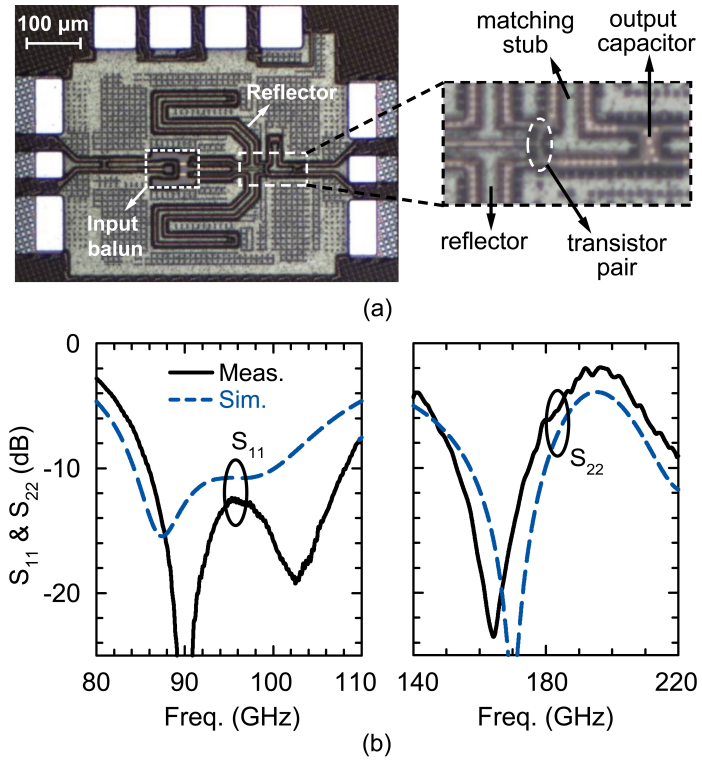


Figure 2.18: (a) Microphotograph of the doubler (0.69×0.49 mm^2) and (b) measured S-parameters.

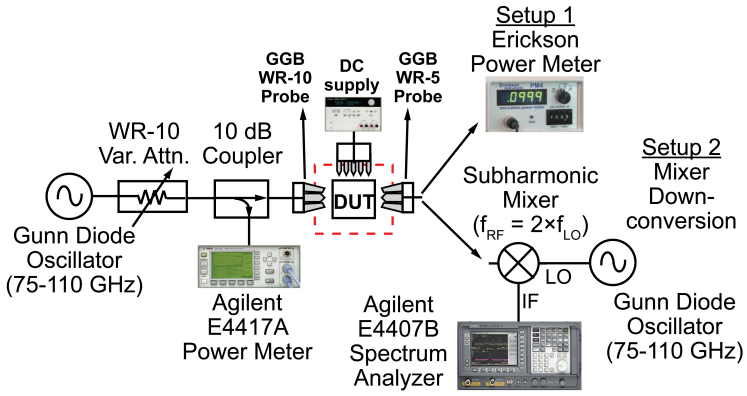


Figure 2.19: Measurement setup for doubler output power and gain characterization. An all-waveguide setup is used for accurate power measurements.

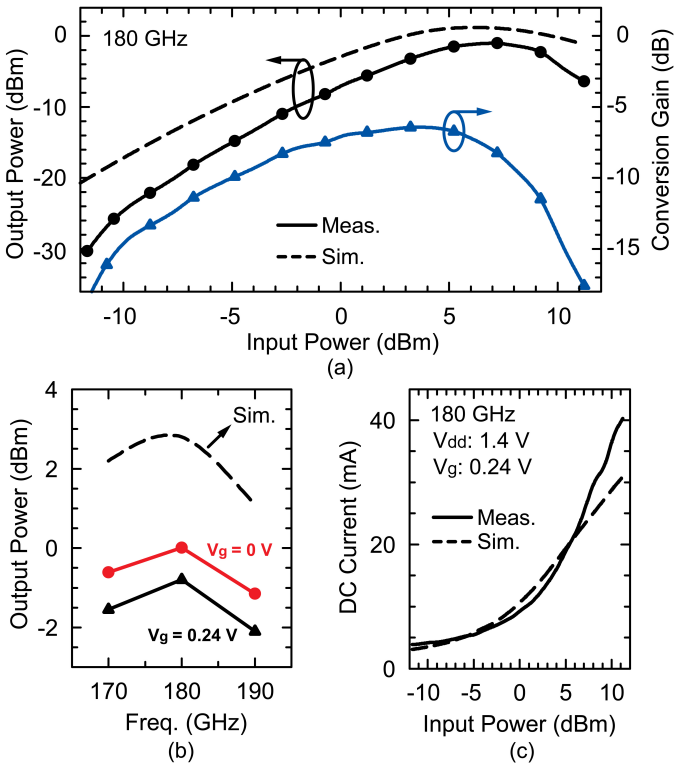


Figure 2.20: Measured (a) output power and gain of the doubler vs. input power at 180 GHz, (b) output power vs. frequency, and (c) DC current vs. input power.

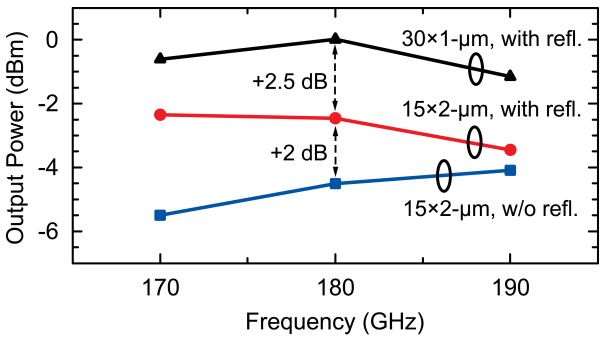


Figure 2.21: Measured peak output power of the G-band doubler versus frequency for different doubler designs.

presents the measured output power at 170–190 GHz at two gate bias points. As the input power is increased, the gate bias needs to be reduced to maintain optimum conduction angle that maximizes the second harmonic generation ($\sim$125°). The output power can be increased to 0 dBm by decreasing the gate bias to 0 V at 180 GHz with 3.0% drain efficiency. The DC current of the doubler is also monitored and is in good agreement with the simulations up to 7 dBm input power (Fig. 2.20c). Note that the 10 Ω resistor in Fig. 2.14 results in 0.2–0.3 V drop for Pin=5–8 dBm, and the drain voltage is $\sim$1.1 V at the peak output power.

Apart from this doubler, two other doubler versions were designed and measured in order to verify the effect of finger width and the 2^{nd} harmonic reflector. Fig. 2.21 shows the measured peak output power versus frequency for the three different designs. The main doubler design, which has 30×1-μm transistors and an input reflector, yields the highest output power. The second version has 15×2-μm transistors and results in 2.5 dB less output power due to increased gate resistance. The third version also uses 15×2-μm transistors, but without the 2^{nd} harmonic reflector. As predicted, the input reflector improves the output power by $\sim$2 dB.

2.5 W-Band Amplifier and G-Band Doubler

The amplifier/doubler is a cascade of the same amplifier and doubler designs discussed in the previous sections. The chip microphotograph is shown in Fig. 2.22a and the total size is 1.0×0.56 mm^2 including the pads. A single V_{dd} and a single ground is used for the entire chip. The S-parameter measurement setup is same as in the case of the doubler. The input return loss is wideband and is the same as the amplifier S_{11} (see Fig. 2.10b). The output return loss is well matched at 160–185 GHz (Fig. 2.22b), and shows a better performance than the doubler (Fig. 2.18b). The W-band amplifier has an effect on the doubler output impedance since it is not a

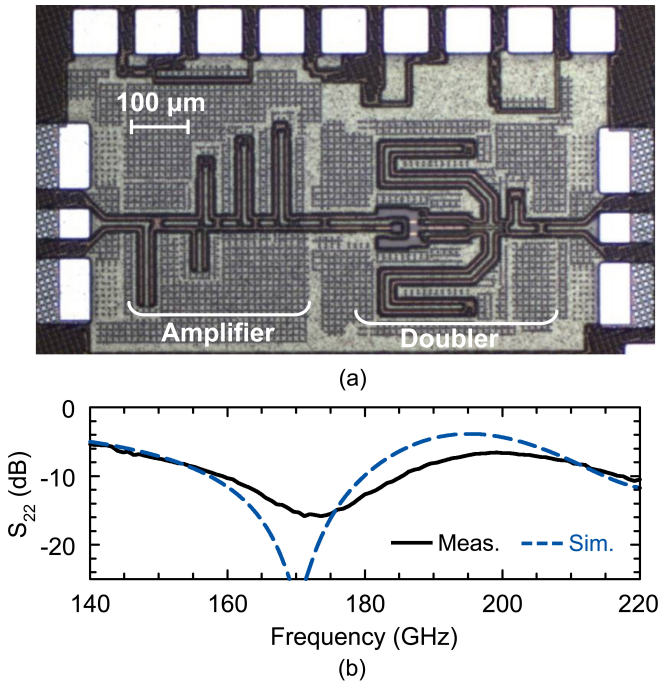


Figure 2.22: (a) Microphotograph of the amplifier/doubler (1.0×0.56 mm^2) and (b) measured output return loss.

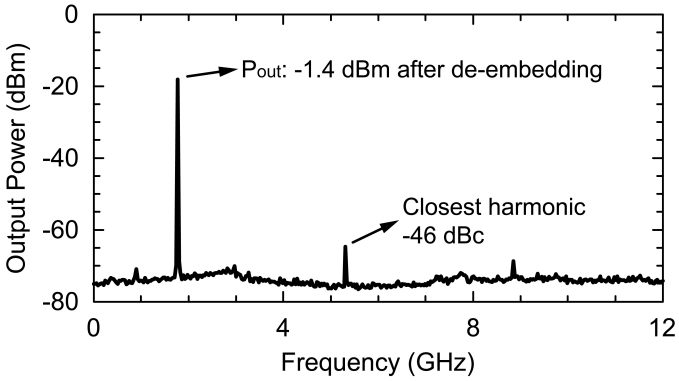


Figure 2.23: Down-converted 180 GHz signal at the output of the amplifier/doubler measured using a spectrum analyzer.

wideband 50 Ω load.

The same measurement setup of Fig. 2.19 is used for large-signal amplifier/doubler measurements. The mixer down-conversion setup is also used for verifying the results obtained by the power meter. The down-converted 180 GHz signal is shown in Fig. 2.23 with an output spectrum up to 12 GHz. The measured output power is -1.4 dBm after de-embedding the losses due to output probe, mixer, and output cable. The highest undesired tone is 46 dB lower with respect to the $2f_o$ output signal and is due to the subharmonic mixer setup.

Fig. 2.24 presents the measured conversion gain and output power of the amplifier/doubler versus input power at 180 and 190 GHz (V_g = 0.24 V). The peak conversion gain is 2–3 dB when the input power is at -7$\pm$2 dBm and drops as the input power is increased. The amplifier/doubler saturates at an input power of -2 dBm since the W-band amplifier is saturated. As a comparison, the output power of the stand-alone doubler is also shown in Fig. 2.24. The stand-alone doubler saturates at a higher input power and the difference between the doubler and amplifier/doubler curves at low input powers is equal to the amplifier gain. The maximum output power generated by both the doubler and amplifier/doubler is nearly identical, indicating that the W-band amplifier is providing at least 6–7 dBm and saturating the doubler sufficiently.

The output power is also measured versus frequency from 170 to 200 GHz with the power meter and mixer setups (Fig. 2.25a). The measured peak output power is 0.0 – -1.2 dBm at 180–190 GHz when V_g = 0 V. Fig. 2.25b shows the measured conversion gain versus frequency at different input power levels. A peak conversion gain of 3.4–5.0 dB with -8 dBm input power is achieved at 190 GHz due to the gain response of the driver amplifier. As the input power is increased, the amplifier saturates and the overall conversion gain decreases. At an input power of 0 dBm, the conversion gain drops to -2 – -1 dB at 180–190 GHz. The amplifier/doubler results in 0.5–1 mW of output power at 170–195 GHz and shows, to our knowledge, the highest power achieved from a CMOS source above 150 GHz.

Table 2.1 presents a summary of W-band CMOS amplifiers. It is seen that the 45-nm SOI CMOS technology results in the lowest NF and with high P_{sat} values. Table 2.2 presents a summary of doublers above 130 GHz. It is seen that the 170-200 GHz CMOS doubler is competitive with the best SiGe results.

2.6 Conclusion

This chapter demonstrated the first use of 45-nm SOI CMOS at W-band and G-band. A significant finding is the reduction of the transistor f_t from 340 GHz to 200 GHz when all the

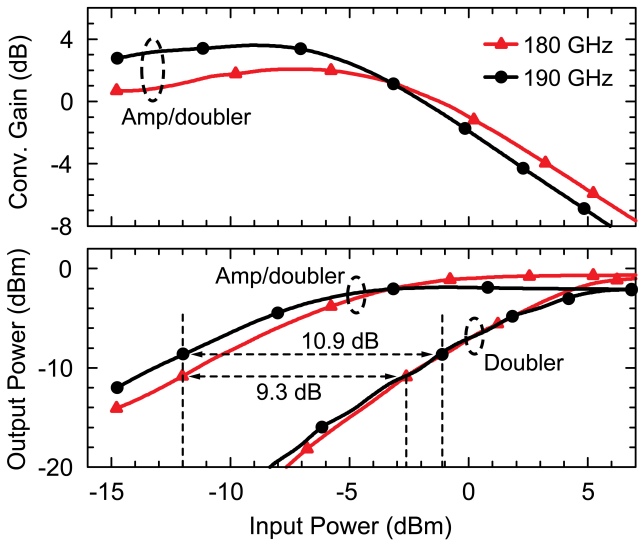


Figure 2.24: Measured conversion gain and output power of the amplifier/doubler at 180 and 190 GHz. Stand-alone doubler output power is also plotted for comparison.

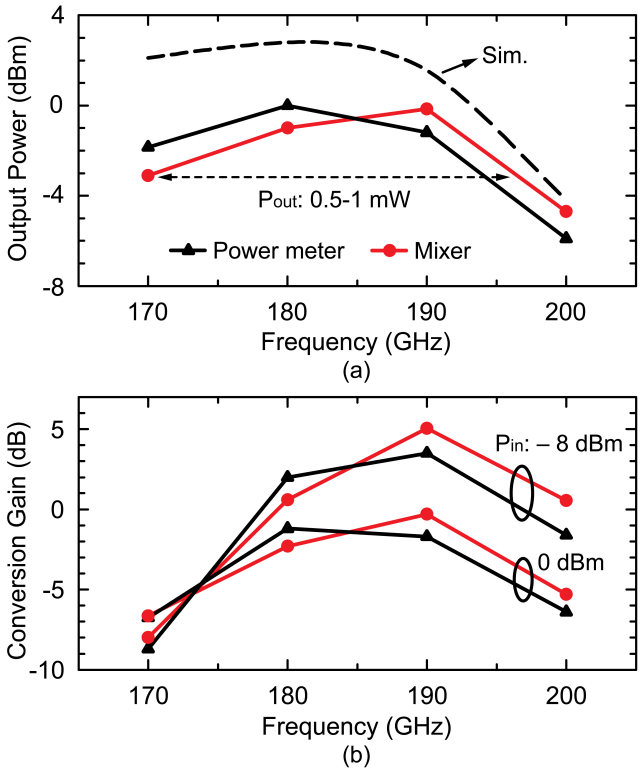


Figure 2.25: (a) Measured peak output power and (b) conversion gain of the amplifier/doubler versus frequency. Measurements done using a power meter and a mixer down-conversion setup.

interconnect parasitics are taken into account. Still, 45-nm CMOS is an excellent candidate for millimeter-wave low-noise amplifiers and submillimeter-wave sources. The technology allows for efficient antennas due to its thick back-end metal layers, and a higher output power can be obtained, both at W-band and at 200 GHz, using free space combining techniques as demonstrated in [5].

2.7 Acknowledgement

The authors thank O. Inac and M. Uzunkol, University of California, San Diego, for technical discussions and for helping in the measurements. The authors thank Prof. Sandy Weinreb, California Institute of Technology, for his advice on 100 GHz amplifier design.

Chapter 2 is mostly a reprint of the material as it is submitted for publishing to IEEE Transactions on Microwave Theory and Techniques, 2011. Berke Cetinoneri; Yusuf A. Atesal; Andy Fung; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Table 2.1: Performance Summary of W-Band CMOS Amplifiers

Freq. (GHz)	**Technology**	**Topology**	**Gain (dB)**	**NF (dB)**	**Psat (dBm)**	**PAE (%)**	**Pdc (mW)**	**Area (mm^2)**	**Ref.**
95	45-nm SOI CMOS	3-stage CS	10.7	6.0	7.5	9.0	52	0.32	This work
85	45-nm SOI CMOS	3-stage CS	13.5	5.7	2.5	–	13	0.32	[15]
100	65-nm CMOS	4-stage CS	13	7.5	10.0	7.3	86	0.33	[11]
88	65-nm CMOS	5-stage Cascode	36	6.4	–	–	60	–	[3]
94	90-nm CMOS	3-stage Cascode (balanced)	15	–	12.0	4.8	208	0.42	[9]

Table 2.2: Performance Summary of Doublers $>$ 130 GHz

Freq. (GHz)	**Techn.**	**Peak P$_{\rm out}$ (dBm)**	**Peak Conv. Gain (dB)**	**P$_{\rm dc}$ (mW)**	**Area (mm^2)**	**Ref.**
170-200	45-nm SOI CMOS	0.0	-6.4 (P$_{\rm in}$= 4 dBm)	39	0.34	This work
170-200	45-nm SOI CMOS	0.0	3.4* (P$_{\rm in}$= -8 dBm)	91	0.56	This work
215-240	0.13-μm SiGe	-1.0	$>$12* (P$_{\rm in}<$ -13 dBm)	–	0.61	[25]
128-138	0.13-μm SiGe	-2.9	-3.2 (P$_{\rm in}$= -1 dBm)	7.2	0.23	[26]

*: including the driver amplifier

Chapter 3

Millimeter-Wave CMOS Switches

3.1 Introduction

Mm-wave CMOS switches are becoming increasingly important for multi-band systems. Of particular importance is the 24 GHz and the 60 GHz frequency range for automotive radars, narrowband ISM and Gbps communication systems [27–30]. Single-pole multiple-throw switches are required for switched-beam antennas, multiple receivers on-chip, built-in-self-test (BIST) circuits and instrumentation systems. Previously, mm-wave SPST and SPDT switches have been demonstrated using 0.13 μm, 90 nm and even 65 nm circuits and have shown wideband performance [31–35]. Also, 60 GHz SPDT and 2:6 switch networks have been demonstrated with excellent performance using metamorphic HEMTs [36]. However, InGaAs technology is expensive and does not lead to co-integration with the mixed signal and digital electronics. A DC-30 GHz SP4T has also been demonstrated using 0.l3-μm CMOS with a 3.1 dB insertion loss at 30 GHz [37]. This switch was based on standard CMOS transistors and therefore suffered from substrate coupling and increased insertion loss. This chapter presents an improved SP4T switch with several key transistor and CMOS technology features such as deep n-well transistors, high substrate contact resistance, and deep trench isolation. The resulting SP4T shows a measured state-of-the-art insertion loss and isolation up to 67 GHz. Apart from the series-shunt SP4T switch, high performance 60 GHz SPDT and SP4T switches are also presented, which are realized in a standard 0.13-μm CMOS technology with high substrate resistance contacts. The resulting switches show state-of-the-art insertion loss and isolation in the 50-70 GHz range.

3.2 Design

3.2.1 DC-70 GHz SP4T Switch

Fig. 3.1 shows the SP4T schematic based on a series-shunt design with input and output matching networks. The SP4T switch is realized using the IBM8HP process and the corresponding transistor models. A cross-section view and circuit model of the series-shunt CMOS transistors are shown in Fig. 3.2. The transistors are based on the deep n-well technology which enables the minimization of the capacitance between the body and the substrate without any latch-up problems. The transistor body and n-well are tied to ground and Vdd, respectively, using Rw = 20 kΩ to eliminate any RF leakage. An optimization was done at 60 GHz to determine the insertion loss and isolation vs. transistor size (Fig. 3.3). The insertion loss is mostly dependent on the series transistor and a FET width of 15 μm (6 fingers) is chosen for a minimum insertion loss of 3.5 dB. Next, the shunt size is chosen based on the required isolation, and a FET width of 21 μm (12 fingers) is chosen for an isolation of 25 dB. Although a wider shunt transistor results in better isolation, the shunt capacitance would limit the switch bandwidth and requires a larger matching inductor which resonates below 70 GHz.

The output matching circuit is implemented using a series 100 pH inductor (L_2 - 60×60 μm^2) and is designed using full-wave EM modeling (Sonnet [17]) with a Q of ∼14

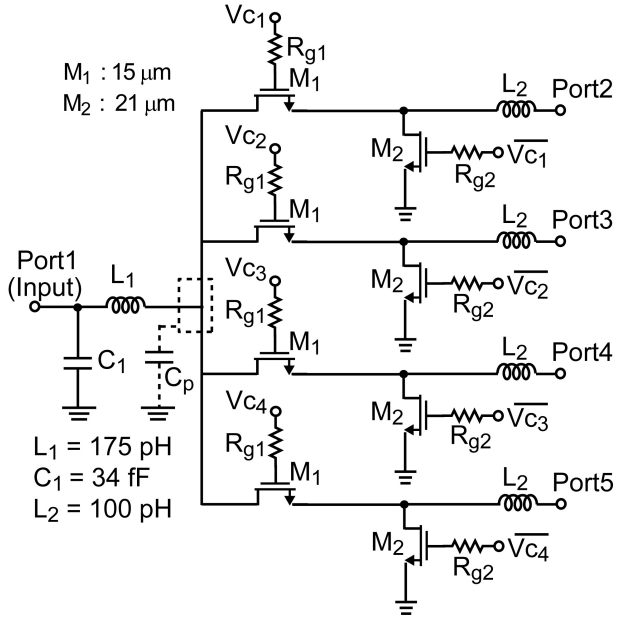


Figure 3.1: Schematic of series-shunt SP4T switch.

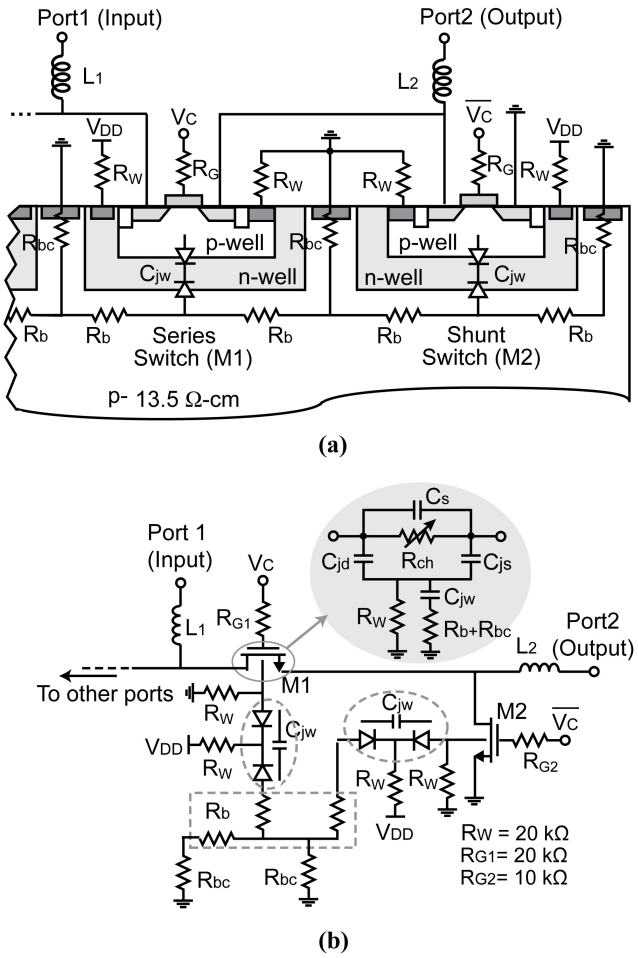


Figure 3.2: (a) Cross sectional view and (b) schematic of the SP4T switch using deep n-well nMOS transistors (only one branch is shown).

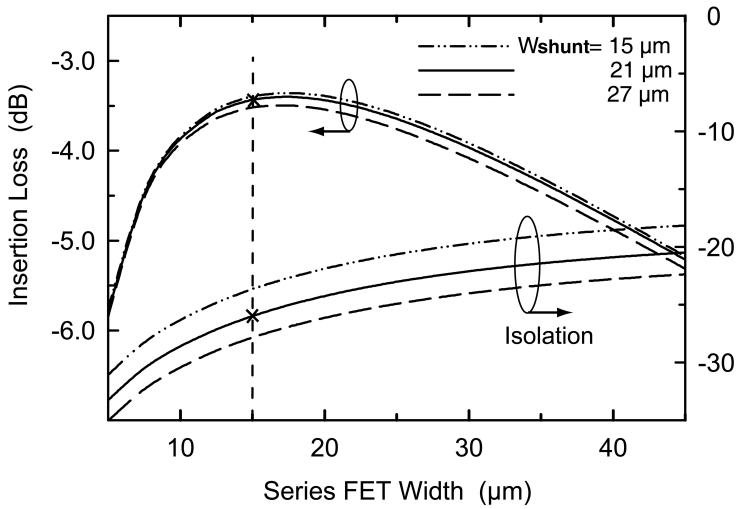


Figure 3.3: Simulated insertion loss and isolation of a series-shunt switch at 60 GHz versus the gate width.

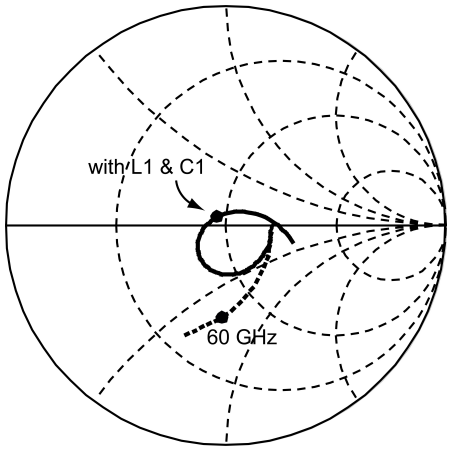


Figure 3.4: The input reflection coefficient at DC-80 GHz at the common node (dashed) and the input port (solid).

at 60 GHz. The capacitance of the common-node at the input matching circuit (simulated using Sonnet) and the capacitance of the three off-state series transistors (IBM model) are matched using a wideband C_p-L_1-C_1 circuit at the input port (Fig. 3.4). In this case, L_1 = 175 pH (80×60 μm^2) with a Q of ∼15 at 60 GHz (designed using Sonnet), C_1 = 34 fF and is implemented using two 70 fF MIM capacitors from the IBM library. The simulated S_{11} and S_{22} are less than -13 dB from DC to greater than 70 GHz for the SP4T switch.

3.2.2 50-70 GHz SPDT and SP4T Switches

Fig. 3.5 presents the SPDT and SP4T schematics based on a tuned λ/4 approach. The SPDT switch is based on a shunt-shunt configuration for added isolation, while SP4T switch is based on a single shunt transistor. In the off- state, the transistor gate (C_S) and junction capacitances (C_J), together with the substrate resistance (R_{SUB}) transform to an equivalent capacitance / resistance network (C_{eq}, R_{eq}). The output matching circuit for the SPDT consists of a $C_{eq}L_1C_{eq}$ network where C_{eq} is the off-state capacitance of the shunt switch. On the other hand, the output matching network of the SP4T consists of a shorted stub which acts as an inductor and creates a parallel resonance with the off-state FET capacitance.

A cross-sectional view of the shunt CMOS transistor is shown in Fig. 3.6. A high substrate resistance of 1 kΩ is used to reduce the RF loss through the junction capacitances, C_J. For a high R_{SUB}, the junction capacitances can be resonated out by adjusting the values of inductors L_1 (SPDT) and L_S (SP4T) [38]. The high R_{SUB} is realized by adopting very small substrate contacts (0.28×5 μm^2) close to the nMOS transistor. The transistors are surrounded with deep trenches and an isolation moat (n-type epitaxial layer) that isolate the transistor active area from the substrate. The deep trench and isolation moat have a depth of 6 μm and 2 μm, respectively, and increase the resistance between the junctions of two nMOS transistors, thus also improving the isolation between the ports.

An optimization was done at 60 GHz to determine the bandwidth and isolation versus transistor size (Fig. 3.7). A FET width of 75 and 150 μm is chosen for an isolation of 40 dB (SPDT) and 27 dB (SP4T), and result in a bandwidth of 42 GHz and 17.5 GHz, respectively. The equivalent capacitances are C_{eq} = 40 fF and 82 fF for the 75 and 150 μm transistors, respectively. L_1 and L_S are 120 and 90 pH for the SPDT and SP4T switches, respectively. L_1 is implemented as a one-turn spiral inductor using full-wave EM modeling (Sonnet [17]) with a simulated Q of 15 at 60 GHz. L_S is synthesized using a shorted CPW stub with impedance of 50 Ω, length of 221 μm (λ_g/11), and a simulated Q of ∼18 at 60 GHz. For the SP4T design, a stub was

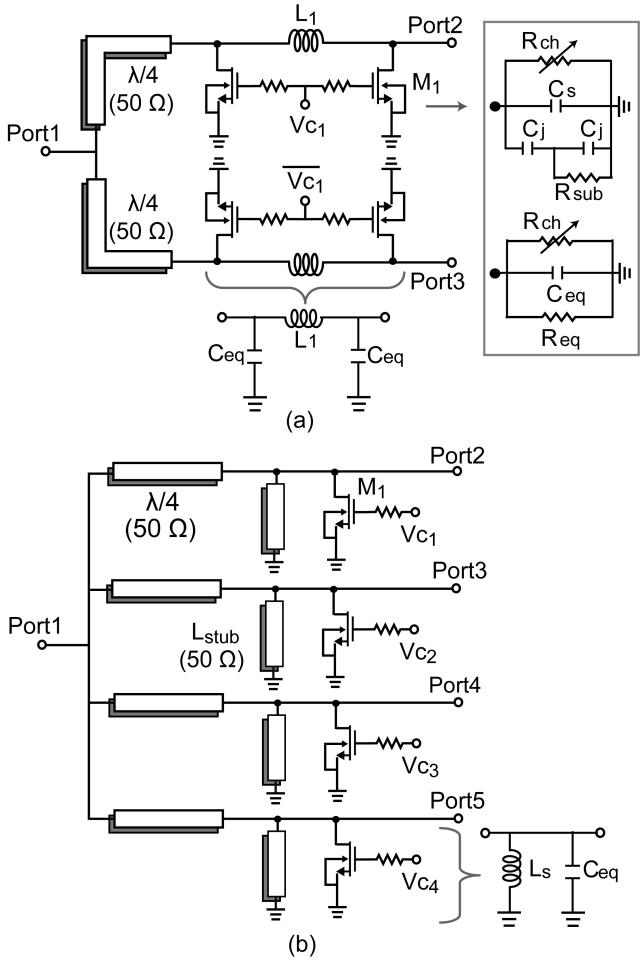


Figure 3.5: Schematic of (a) SPDT and (b) SP4T switches.

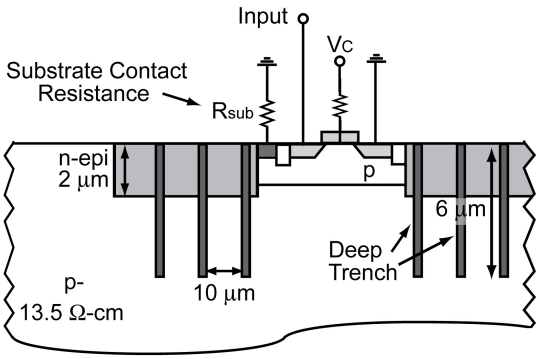


Figure 3.6: Cross sectional view of the shunt CMOS transistor with deep trenches, isolation moat, and high R_{SUB} contacts.

chosen since the shunt inductance determines the LC resonance bandwidth (hence the return and insertion loss), and a precise value is required for resonance at 60 GHz. On the other hand, the SPDT output matching network is a C-L-C network which is less sensitive to the inductor value for impedance match and insertion loss. In both designs, the λ/4 transmission lines are 590 μm long and are implemented using a 11/12/11 μm grounded CPW line with a simulated loss of 0.55 dB/mm at 60 GHz. The common node (Port1) is simulated using Sonnet and its S-parameters are embedded into the λ/4 sections. The mutual coupling between the CPW lines was also simulated in Sonnet and is $<$ -45 dB at 60 GHz. The insertion loss is determined mostly by the inductor (or stub) Q and by the λ/4 transmission line. The simulated switch loss is 1.7 dB and 2.1 dB for the SPDT and SP4T, respectively, with an impedance match better than -10 dB from 50-70 GHz.

3.3 Implementation and Measurements

3.3.1 DC-70 GHz SP4T Switch

Fig. 3.8a shows the fabricated SP4T switch using the IBM8HP process. The switch active area is 0.24$\times$0.23 mm^2, not including the CPW pads. Ports 4 and 5 are terminated internally with 50 Ω for ease of measurements. A detailed view of the switch core is shown in Fig. 3.8b (65$\times$80 μm^2) and the common-node is clearly seen at port 1. A deep-trench isolation perimeter is visible around each series-shunt switch pair which reduces the coupling between the output ports. Another deep-trench perimeter encircles all the SP4T switches so as to isolate them from other active devices on the wafer. A detailed view of the series-shunt switch cell is also presented in Fig. 3.8b.

S-parameter measurements were done using the 67 GHz Agilent E8361A PNA. The

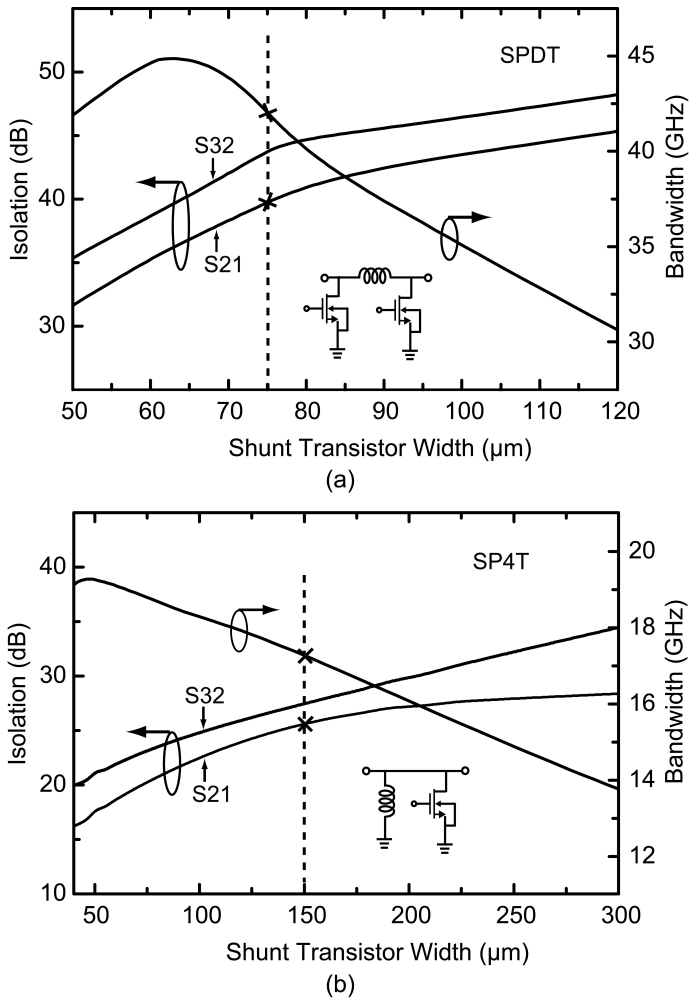


Figure 3.7: Simulated -10 dB return loss matching bandwidth, and isolation versus transistor width of (a) SPDT and (b) SP4T.

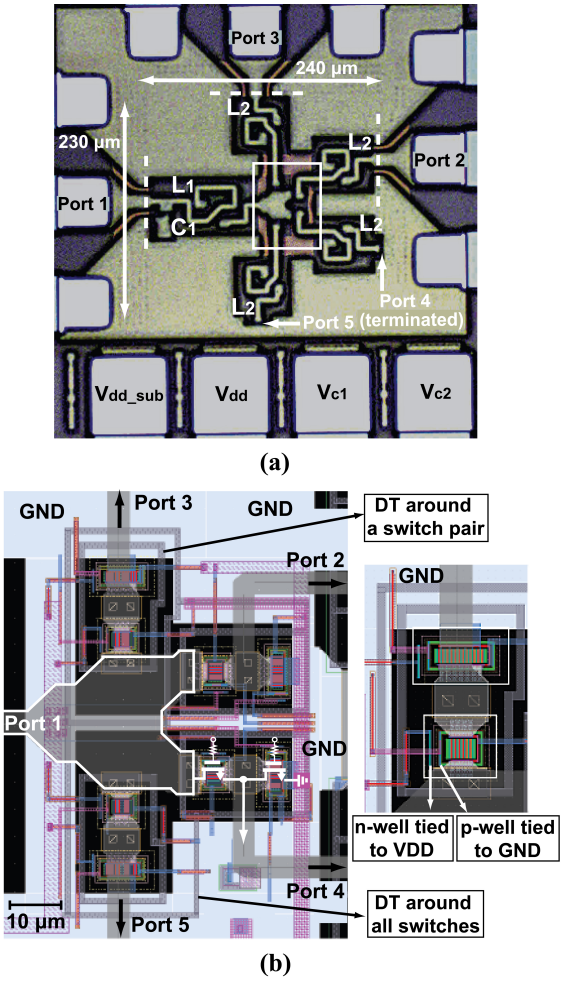


Figure 3.8: Micro-photograph of the series-shunt SP4T switch.

reference planes are shown in Fig. 3.8a, and the pad loss is de-embedded using TRL calibration and pad-to-pad measurements (both result in a loss of 0.1-0.3 dB at 10-60 GHz per pad). The measured insertion loss and reflection coefficient are nearly identical for port 2 and port 3, showing the symmetry of the design, and agree well with simulations (Figs. 3.9, 3.10).

The SP4T results in an insertion loss of 3.5 dB at 60 GHz which is a significant improvement over other wideband SP4T designs [37]. The measured isolation is better than 25 dB up to 60 GHz, and again, both ports result in nearly identical response (Fig. 3.11). The measured isolation between the two output ports is better than 28 dB at 60 GHz and agrees well with simulations. The switch results in a constant P_{1dB} of 9-10 dBm and a constant IIP3 of 20-21 dBm from 10 to 60 GHz as predicted by the IBM models (Fig. 3.12). The power handling is limited by the voltage swing at the gate of the shunt transistor [32]. The simulated switching time is limited by the gate-bias resistors and is 0.3-0.4 ns independent of the RF frequency (Fig. 3.13). The SP4T switch can operate up to 70 GHz with an insertion loss of less than 3.8 dB, and with excellent input and output match.

3.3.2 50-70 GHz SPDT and SP4T Switches

The switches were fabricated in a 0.13-μm SiGe BiCMOS process (IBM 8HP) and are shown in Fig. 3.14. The active chip area is 0.39×0.32 mm^2 (SPDT) and 0.59×0.45 mm^2 (SP4T), and can be made smaller in future designs by folding the $\lambda/4$ transmission-line sections. In the SP4T design, Ports 4 and 5 are terminated internally with 50 Ω for ease of measurements and should have identical results to Ports 2 and 3, due to the symmetry of the design. S-parameter measurements were done using the 67 GHz Agilent E8361A PNA, and the reference planes are shown in Fig. 3.14. The pad loss is de-embedded using TRL calibration and also using back-to-back pad measurements (both methods result in a loss of 0.2-0.3 dB per pad at 50-70 GHz).

Measured SPDT and SP4T insertion loss and reflection coefficients agree well with simulations and are nearly identical for Ports 2 and 3, showing the symmetry of the design (Fig. 3.15). The SPDT results in an insertion loss of 2.0 dB (1.7 dB simulated) and the SP4T results in an insertion loss of 2.3 dB (2.1 dB simulated) at 60 GHz. Insertion loss is < 2.5 dB and < 2.8 dB with a bandwidth of 45-75 GHz and 55-65 GHz for SPDT and SP4T, respectively, showing very wideband performance. These results were achieved on two different chips with $\sim$0.1 dB variation in the measured insertion loss. The measured SPDT and SP4T isolation is > 30 dB and > 20 dB at 50-67 GHz and again both output ports results in nearly identical responses (Fig. 3.16). The measured isolation between the two output ports is 27 dB for both designs, and is

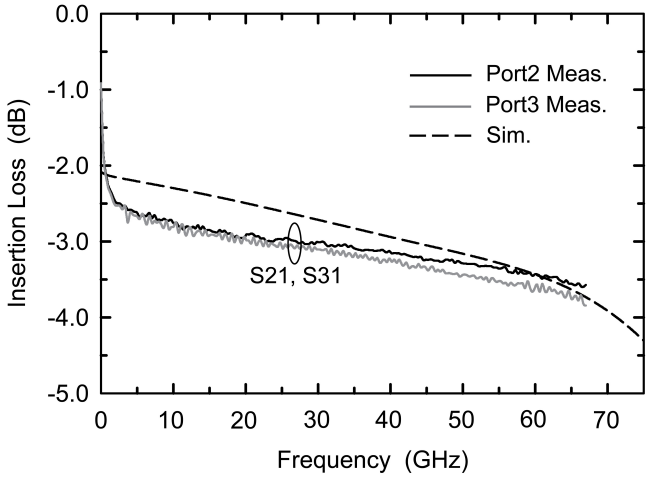


Figure 3.9: Measured and simulated insertion loss of the series-shunt SP4T switch.

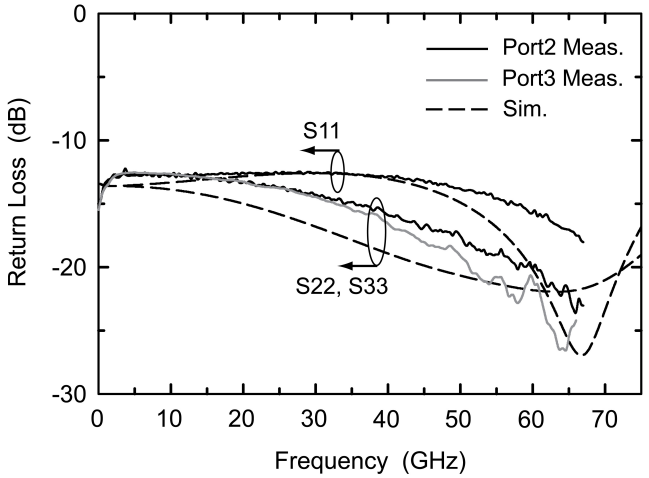


Figure 3.10: Measured and simulated return loss of the series-shunt SP4T switch.

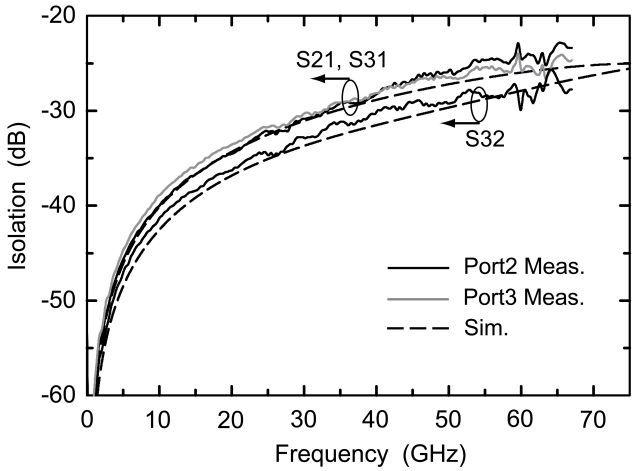


Figure 3.11: Measured and simulated isolation of the series-shunt SP4T switch.

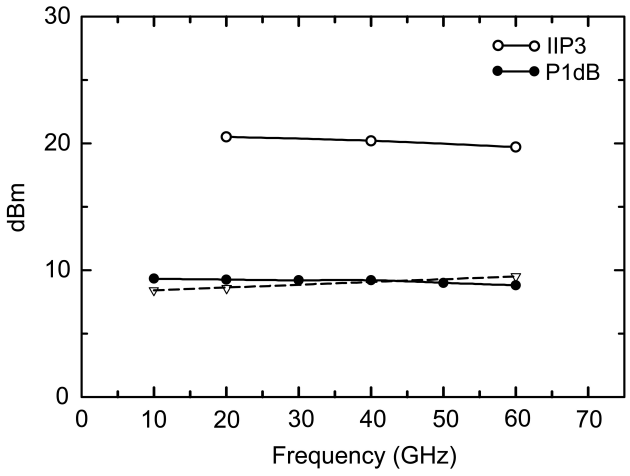


Figure 3.12: Measured (solid) and simulated (dashed) P1dB and IIP3 of the series-shunt SP4T switch.

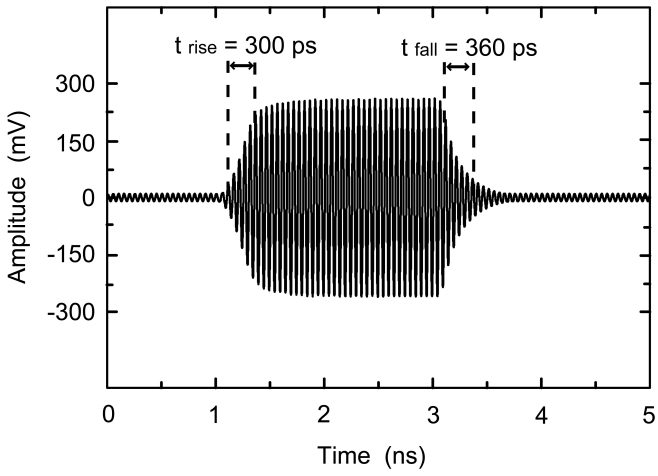


Figure 3.13: Simulated switching time of the series-shunt SP4T switch at 20 GHz. Similar results are achieved at 40 GHz and 60 GHz.

limited mostly by substrate coupling (simulations predict $\sim$37 dB for the SPDT design).

The SPDT and SP4T switches result in a simulated P1dB of 13-14 dBm, but this could not be measured due to power limitations at 60 GHz (compression is not observed up to 10 dBm, Fig. 3.17). The measured IIP3 is 23-24 dBm for both designs and agree well with simulations. Power handling is limited by the voltage swing at the gate of the transistors [32].

3.4 Conclusion

A comparison of wideband CMOS switches are given in Table 3.1. This chapter presented a wideband series-shunt SP4T switch with high isolation between the channels. This is achieved due to the small size of the transistors, deep n-well technology and deep trench isolation between the different ports. The transistor models used are standard foundry models, and EM modeling is used to design input and output matching circuits. The power handling is limited to 10 dBm $\mathrm{P_1dB}$ which makes it ideal for mm-wave (short-distance) communication systems, automotive radars, and wideband instrumentation systems. Wideband SPDT and SP4T switches centered at 60 GHz are also presented with excellent performance. The SPDT loss can be reduced to 1.6 dB if a single shunt transistor is used but at the expense of isolation (24 dB instead of achieved 30 dB). The power handling is limited to 13-14 dBm which is sufficient for most short-range 60 GHz communication systems.

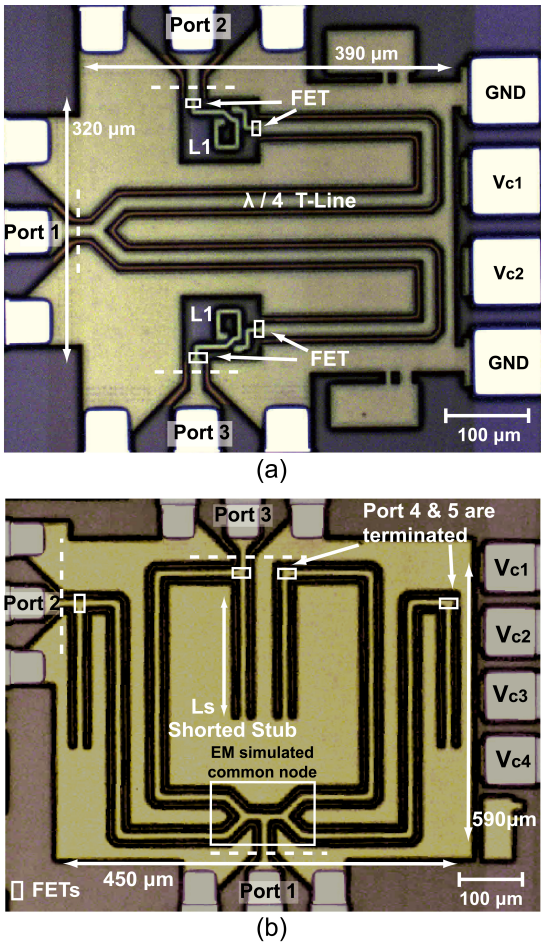


Figure 3.14: Micrograph of (a) SPDT and (b) SP4T switches (figures are not to the same scale).

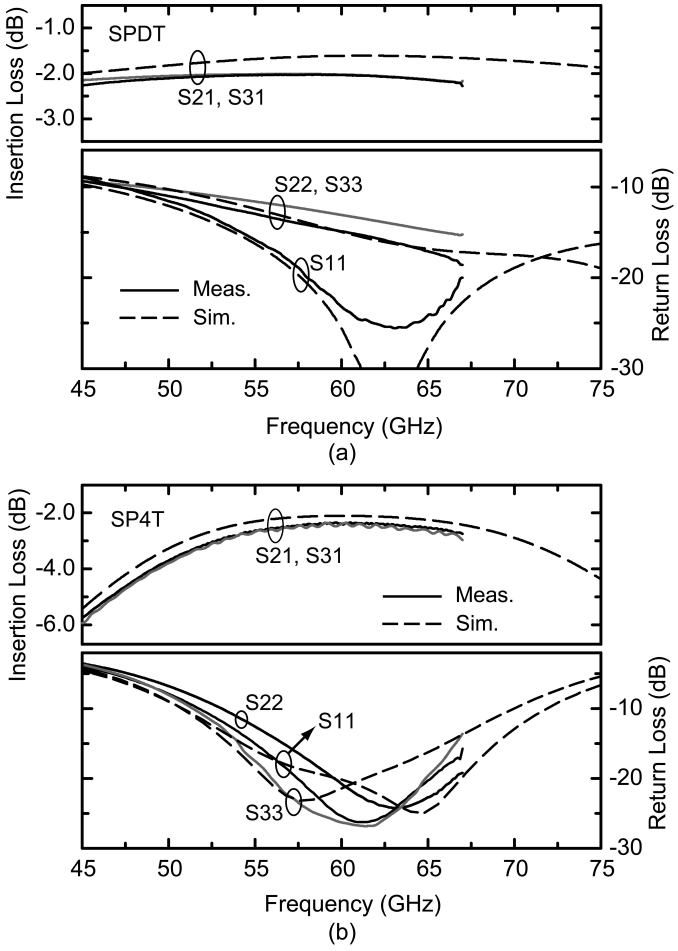


Figure 3.15: Measured and simulated insertion loss and return loss for (a) SPDT and (b) SP4T switches.

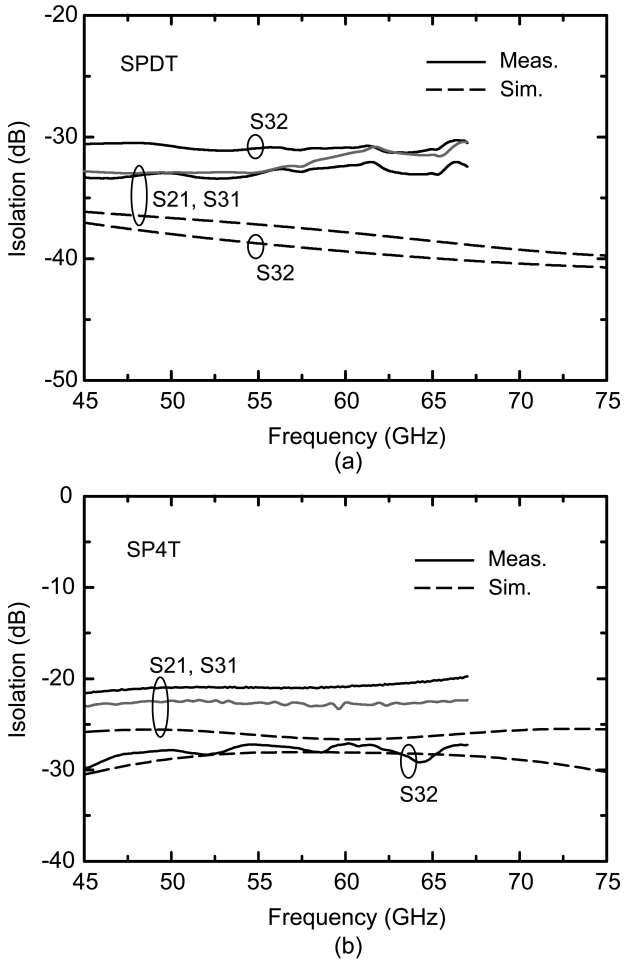


Figure 3.16: Measured and simulated isolation for (a) SPDT and (b) SP4T switches.

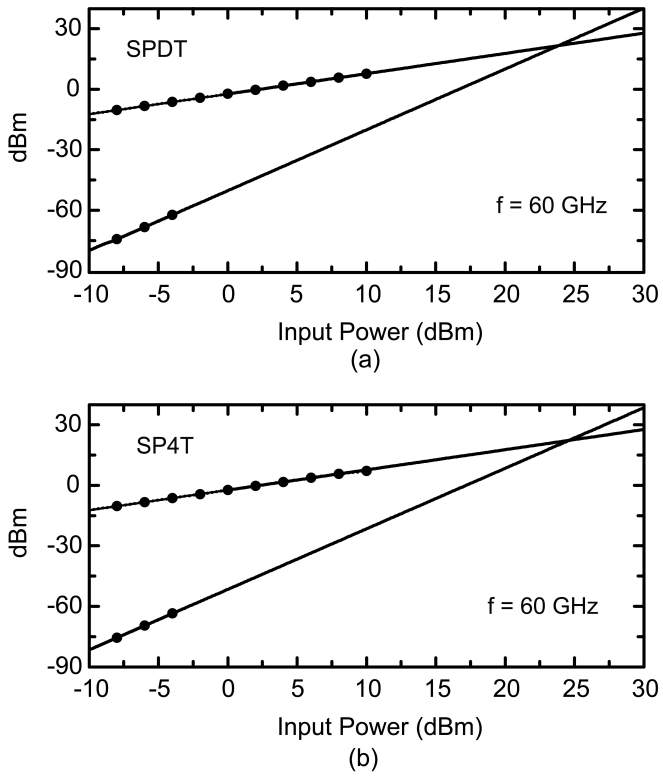


Figure 3.17: Measured IIP3 of (a) SPDT and (b) SP4T switches at 60 GHz.

Table 3.1: Comparison of Wideband Mm-Wave Switches.

$Ref.$	IL (dB)	Iso. (dB)	BW (GHz)	Tech.	Type
[5]	< 2.5	> 25	DC-20	0.18-μm CMOS	SPDT
[8]	< 1.6	> 30	DC-94	65-nm CMOS	SPST
[9]	< 6	> 38	DC-50	0.18-μm CMOS	SPDT
[10]	< 3.1	> 25	DC-30	0.13-μm CMOS	SP4T
This work	< 3.5	> 25	DC-70	0.13-μm CMOS	SP4T

3.5 Acknowledgement

This work was supported in part by INTEL Corporation, Ian Young, and by DARPA, Mark Rosker, program monitors. The authors would like to thank Byung-Wook Min, Qualcomm Inc., for technical discussions.

Chapter 3 is mostly a reprint of the material as it appears in IEEE International Microwave Symposium Digest, 2009 and IEEE Radio Frequency Integrated Circuits Symposium, 2009. Berke Cetinoneri; Yusuf A. Atesal; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 4

8×8 and 4×4 Butler Matrices in 0.13-μm CMOS

4.1 Introduction

In the recent years, phased arrays based on CMOS and SiGe technologies have begun to demonstrate their potential at microwave and millimeter-wave frequencies due to the high density of integration, functionality and reduced cost of a silicon chip [39–47]. Phased arrays have the ability of electronic beam steering as well as nulling an interferer. They also provide fast beam scanning capabilities, which make them ideal for mobile platforms. However, the drawbacks of phased arrays are relatively high power consumption and increased complexity to generate multiple beams (4 or 8 beams).

Kang et al. recently demonstrated a 2-antenna/4-simultaneous beam silicon chip at X/Ku-band- all beams can be at the same frequency and each with $>$ 1 GHz bandwidth [48]. One can also generate multiple beams using digital beam-forming techniques, and Cetinoneri et al. presented a heterodyne Ku-band SiGe digital beamformer with a noise figure of 3.1 dB at 15 GHz [49]. These architectures can scale to 8 simultaneous beams but at a cost of relatively high power consumption.

Butler matrices offer an excellent compromise between multi-beam systems and phased array systems [50–54] (Fig. 4.1). These feed matrices, composed of 90° couplers, transmission lines and fixed phase delays, are passive and bi-directional, and can synthesize N beams from M antennas. The beams cover the whole visible space with $\sim$-3 dB cross-over in the patterns. Butler matrices can either be used in a multiple-input-multiple-output (MIMO) configuration with

M simultaneous receivers, or a single-pole-M-throw (SPMT) switch can be used with a single receiver for switched-beam applications [55, 56]. For an 8-element array, one can also use 2 (or 4) SPNT switches and 4 (or 2) transceivers to obtain multiple independent beam systems. Also, planar Rotman lenses can generate simultaneous beams with low-sidelobes [57–59]. Previously, 4×4 CMOS-based Butler matrices were demonstrated at 2.5 GHz [60], 24 GHz [61], and 60 GHz [62], but the pattern and absolute gain measurements were not completely presented. This chapter presents the first 8×8 Butler matrix at 5 to 6 GHz and a 4×4 Ku-band Butler matrix for multibeam applications. Both designs are based on lumped elements with a very small size and are presented with a full pattern characterization versus frequency.

4.2 8×8 Butler Matrix at 5–6 GHz

4.2.1 Design and Circuit Blocks

Fig. 4.1b illustrates the block diagram of an 8×8 Butler matrix based on 4-port couplers and fixed delay lines. The design consists of twelve 3-dB quadrature couplers, 8 delay cells with phase values of 22.5°, 45°, and 67.5°, and 16 cross-overs. For each beam port, the circuit generates progressive phase shifts at the antenna ports with equal amplitude. Due to the linear characteristic of the Butler matrix, 8 simultaneous beams can be formed in different directions depending on the input (beam) port. The phase distribution and corresponding beam directions are shown in Table 4.1 with $\Delta\Phi$ defined as the element-to-element phase variation.

CMOS Chip Design

There are several designs for lumped 90° couplers, and the circuit shown in Fig. 4.2a results in a low-loss implementation [63]. Both conventional (transmission line based) and lumped element designs are reciprocal, and result in an impedance match at all ports ($S_{\mathrm{nn}}= 0$) and perfect isolation ($S_{31}= S_{42}= 0$) at the design frequency. The main difference between the 90° coupler implemented using transmission lines and lumped-elements is the absolute output phase at ports 2 and 4. For a transmission line coupler, $S_{21}= 0.707e^{-j90^\circ}$ and $S_{41}= 0.707e^{-j180^\circ}$, while for the lumped-element coupler, $S_{21}= 0.707e^{-j90^\circ}$ and $S_{41}= 0.707e^{j0^\circ}$. In order to obtain correct Butler matrix operation for an 8×8 matrix with lumped-element couplers, the 22.5°, 45° and 67.5° fixed delay lines are removed from the straight paths (conventional design, not shown) and inserted in the cross-over paths (Fig. 4.1b). This corrects for the different phase seen at S_{41}.

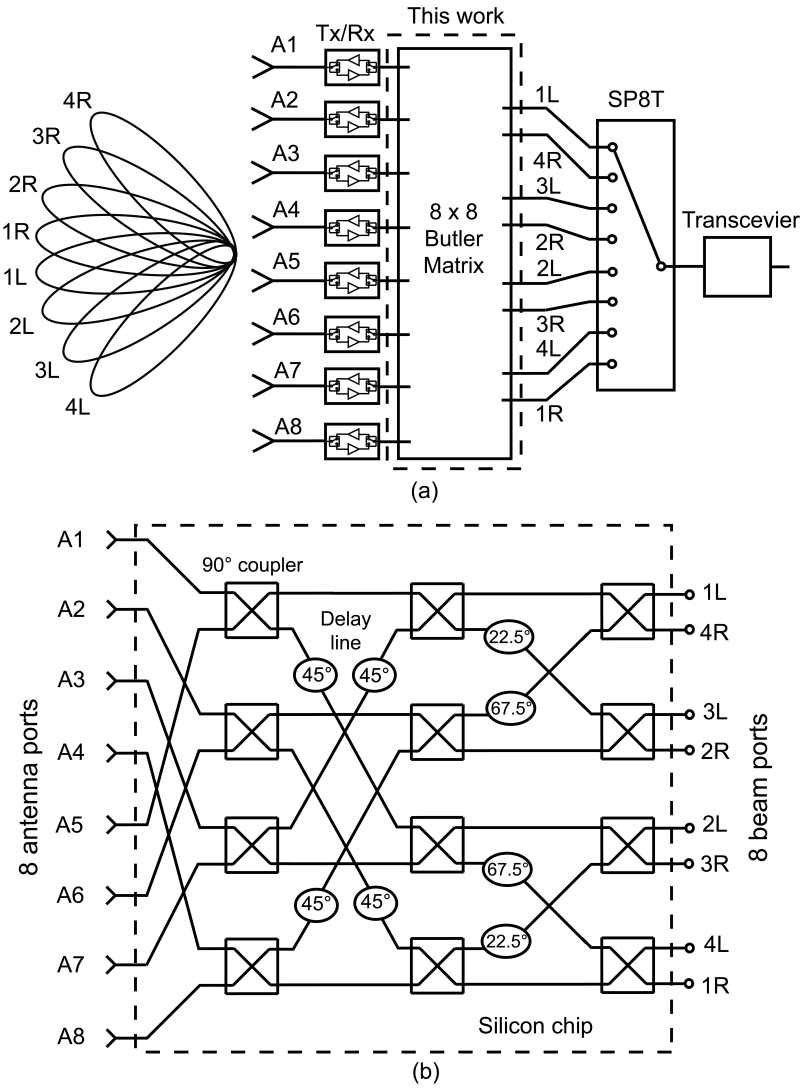


Figure 4.1: (a) Conceptual block diagram of Butler matrix used in a switched-beam system, and (b) circuit diagram of an 8×8 Butler matrix.

Table 4.1: Phase Distribution of an 8×8 Butler Matrix

	Beam Ports							
Ant. Port	**1L**	**4R**	**3L**	**2R**	**2L**	**3R**	**4L**	**1R**
A1	90	-180	157.5	-112.5	135	-135	157.5	-112.5
A2	112.5	22.5	-90	-180	-157.5	112.5	-45	-135
A3	135	-135	22.5	112.5	-90	0	112.5	-157.5
A4	157.5	67.5	135	45	-22.5	-112.5	-90	-180
A5	-180	-90	-112.5	-22.5	45	135	67.5	157.5
A6	-157.5	112.5	0	-90	112.5	22.5	-135	135
A7	-135	-45	112.5	-157.5	-180	-90	22.5	112.5
A8	-112.5	157.5	-135	135	-112.5	157.5	-180	90
$\Delta\Phi$	22.5	-157.5	112.5	-67.5	67.5	-112.5	157.5	-22.5
Beam Angle	-7	+61	-39	+22	-22	+39	-61	+7

*All in degrees

For a 5.5 GHz lumped-element quadrature coupler design, $C_1 = 590$ fF, $C_2 = 240$ fF and $L_1 = 1.0$ nH. The simulated lumped coupler shows an insertion loss of 0.9 dB at 5.5 GHz, and isolation > 17 dB from 5 to 6 GHz.

The required 22.5°, 45°, and 67.5° delay lines are too long to be integrated on-chip at 5-6 GHz. Therefore, the delay cells are implemented using C-L-C π-networks (Fig. 4.2b). At 5.5 GHz $C_{\rm d} = 115, 240, 385$ fF and $L_{\rm d} = 0.55, 1.0, 1.33$ nH for 22.5°, 45° and 67.5° delay cells, respectively. The delay cells have a simulated loss of 0.2-0.5 dB at 5.5 GHz. The 90° coupler and delay cells have a linear phase relationship versus frequency, and therefore result in true-time-delay performance over the 5-6 GHz bandwidth. This ensures that the beams always point in the same direction versus frequency.

The inductor L_1 in the 90° coupler, and the $L_{\rm d}$ in the delay lines are implemented as spiral inductors with a Q of 15 at 5.5 GHz. Capacitors, C_1, C_2 and $C_{\rm d}$ are realized using MIM capacitors in the IBM 8RF process. Transmission lines ($Z_0 = 50\,\Omega$) are used for interconnections between the couplers and the delay cells, and implemented using 12-20-12 μm grounded coplanar waveguide (CPW) lines with the MA and MG layers (Fig. 4.3). The inductors together with the transmission lines are simulated using a full-wave electromagnetic simulator, Sonnet [17], and are tuned so as to obtain the correct phase between the different sub-cells.

Transmission line crossovers are imperative in all Butler matrix implementations, and the on-chip crossover is done using metal layers MA (top metal), E1 and MG (Fig. 4.3). The E1 metal layer acts as a ground island between MA and MG, thereby enhancing the isolation. The crossover isolation is simulated using full-wave electromagnetic analysis (Sonnet) and is > 65 dB at 5-6 GHz.

The complete passive 8×8 matrix has 32 inductors, 72 capacitors and 16 cross-overs, and is shown in Fig. 4.4. The input and output RF pads (8+8) are placed on a 150 μm pitch. The chip is 2.5 mm×1.9 mm including all RF pads. The simulated loss of the CMOS 8×8 Butler matrix is 3.5 dB at 5.5 GHz including the RF pad transitions, and is mostly due to the finite Q of the inductors in the couplers and delay cells. The long transmission lines and cross-overs at the antenna ports (see Fig. 4.4a) contribute ∼0.2 dB of loss at 5.5 GHz.

Board Design

In order to fully characterize the 8×8 Butler matrix and demonstrate its beam-forming capabilities, the chip is connected to an 8-element antenna array. The assembled 8×8 Butler matrix system board is shown in Fig. 4.5a, and is based on a Teflon board with an $\epsilon_{\rm r} = 2.2$,

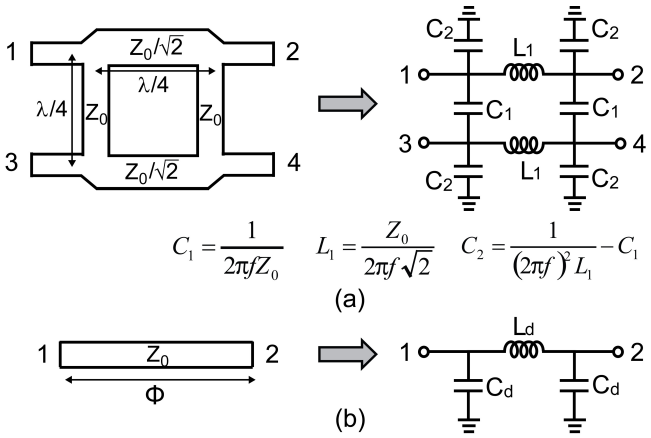


Figure 4.2: Transmission line and lumped element based (a) 90° coupler, and (b) phase delay cell.

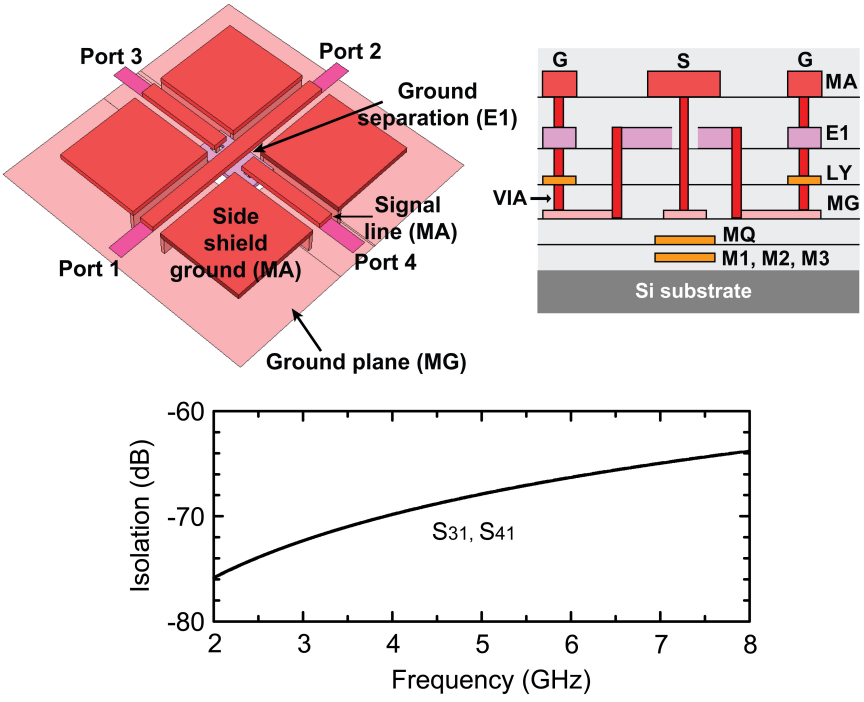
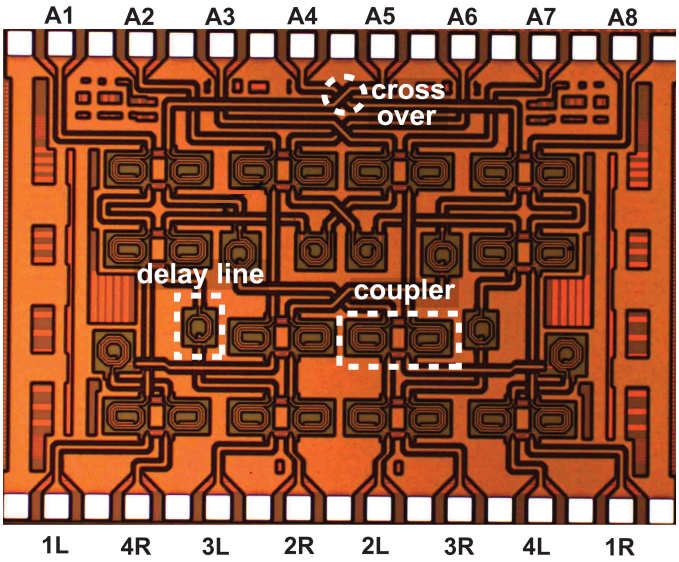
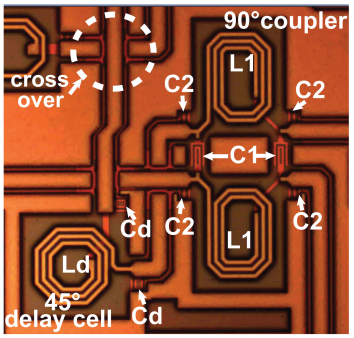


Figure 4.3: On-chip CPW crossover structure: top view, cross-sectional view, and simulated coupling between the ports.



(a)



(b)

Figure 4.4: (a) Microphotograph of the 8×8 Butler matrix (2.5×1.9 mm^2), and (b) a 45° phase delay cell with a 90° coupler.

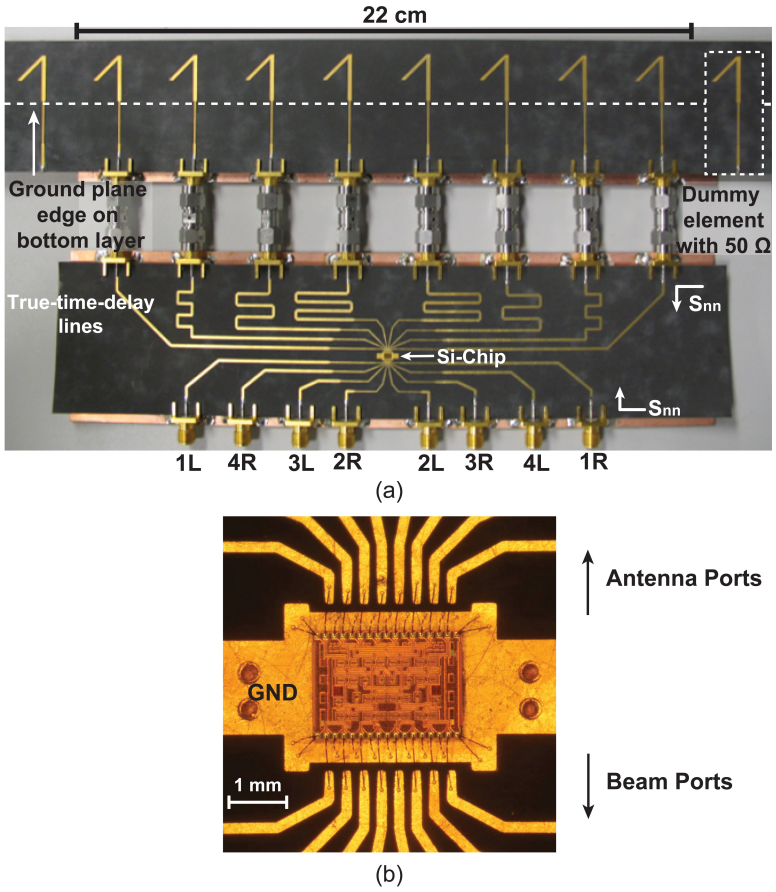


Figure 4.5: (a) Picture of the assembled 8×8 Butler matrix board, and (b) close-up view of the silicon chip on a Teflon board.

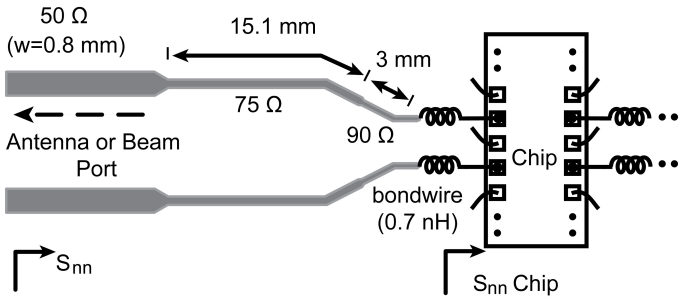


Figure 4.6: Matching network for the 8×8 Butler matrix chip. 8 of them are used on each side of the chip: antenna ports and beam ports.

$h = 10$ mils (Rogers RO5880). The silicon chip is placed on a grounded pedestal and bonded to the RF transmission lines (Fig. 4.5b). Port-to-port coupling due to the bondwires is minimized using grounded bondwires between the RF ports. An RF matching network is designed for each antenna port and beam port so as to compensate for the bondwire effects (Fig. 4.6). The matching circuits quickly diverge in order to minimize the coupling on the Teflon board. The simulated return loss ($S_{\rm nn}$, n=1-8) at the antenna and beam ports is $<$ -10 dB from 5-6 GHz, and the simulated coupling from the silicon chip to the coaxial connectors is $<$ -18 dB at 5-6 GHz. In order to preserve the phase distribution at the antennas, true-time-delay lines are used between the antenna ports of the silicon chip and the dipole antennas (Fig. 4.5a).

The 8-element antenna array is built using angled dipoles with a spacing of $0.5\lambda_0$ at 5.5 GHz (0.45-0.55 λ_0 at 5-6 GHz). The antennas are designed using a 3D electromagnetic solver HFSS [64], and result in $S_{11} <$ -10 dB at 5.0-6.4 GHz, a peak gain of 2 dB, and $<$ -17 dB element-to-element coupling. The antennas have $\sim$120° half-power-beam-width and are suitable for wide angle scanning. Due to the mutual coupling between the antennas in the array environment, there is a 3-dB drop in the antenna element pattern at broadside as shown in Fig. 4.7. This is acceptable since it results in a more uniform gain over the different beams. The H-plane pattern (not shown) has a 3-dB beamwidth of 170° [65].

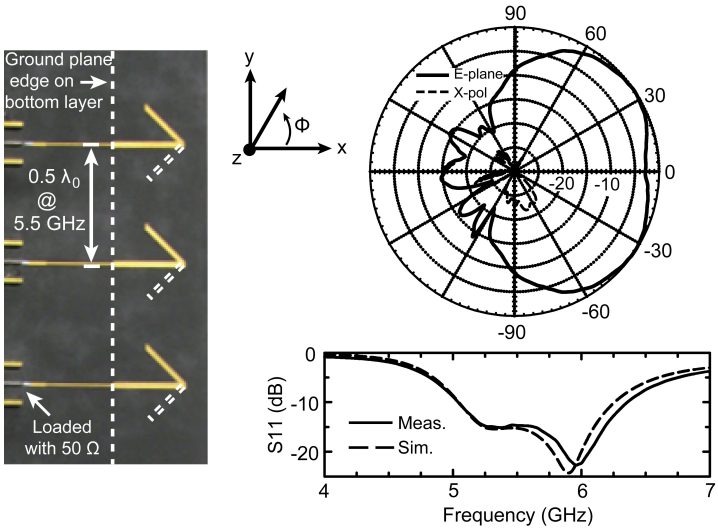


Figure 4.7: 3-element layout of the angled-dipole antenna, the measured pattern at 5.5 GHz and return loss (center element shown).

4.2.2 Measurements

Quadrature Coupler

The silicon chip is fabricated in a standard 0.13-μm CMOS technology (IBM 8RF-DM). The 90° coupler is first characterized with on-chip S-parameter measurements of a test cell. Port-3 of the quadrature coupler test cell is connected to a 50 Ω on-chip load (Fig. 4.8). The coupler results in an insertion loss of 3.8±1 dB at 5-6 GHz with $<$ -10 dB input and output impedance match. The measured absolute quadrature phase error is $<$ 10° and the measured isolation between the output ports is $>$ 16 dB at 5 to 6 GHz (Fig. 4.8).

System Gain and Pattern Measurements

The measured return loss (S_{nn}) of the 8×8 Butler matrix chip is $<$ -10 dB at 5-6 GHz for all 8 beam ports and 8 antenna ports including bondwires, transmission lines and connector effects (Fig. 4.9). The antenna ports are then connected to 8 angled-dipole antennas, and far-field patterns are measured in an anechoic chamber using a standard gain horn antenna. The normalized E-plane patterns of the array at 5.5 GHz are shown in Fig. 4.10a and agree very well with simulations. Eight beams are generated at -61° (4L), -39° (3L), -22° (2L), -7° (1L), +7° (1R), +22° (2R), +39° (3R) and +61° (4R) with $<$ 1° error in the beam direction, and covering the -73° to +73° angular space with $<$ 3 dB variation. The simulations are based on ideal 90° couplers and delay lines (not on the measured S-parameters of the stand-alone components) and the simulated angled-dipole pattern. The beamwidth increases with scan angle: 14° (1L, 1R), 15° (2L, 2R), 16° (3L, 3R), and 23° (4L, 4R), as expected from a scanned linear array [66].

The measured gain is obtained using the Friis transmission method in the receive mode [66]. The received power ($\mathrm{P_R}$) is measured at the coaxial connector at the beam port.

$$\frac{P_R}{P_T} = \left(\frac{\lambda}{4\pi R}\right)^2 G_T G_{DUT} \tag{4.1}$$

where λ is the wavelength, R is the distance between the horn antenna and the 8-element array ($R \approx 3$ m), G_{T}, P_{T} are the gain and power of the transmit horn, respectively, and G_{DUT} is the gain of the 8-element antenna array connected to the Butler matrix. A measured gain of 4.8±1 dB is obtained for all beams and includes the loss of the true-time-delay transmission lines, Butler matrix, connectors and the effect of the angled-dipole pattern (Fig. 4.10b). The predicted gain is 11.0 dB and the difference is attributed to: 1) 3.5 dB simulated on-chip Butler matrix loss, 2) 2.0 dB input/output transmission line loss including the matching networks and

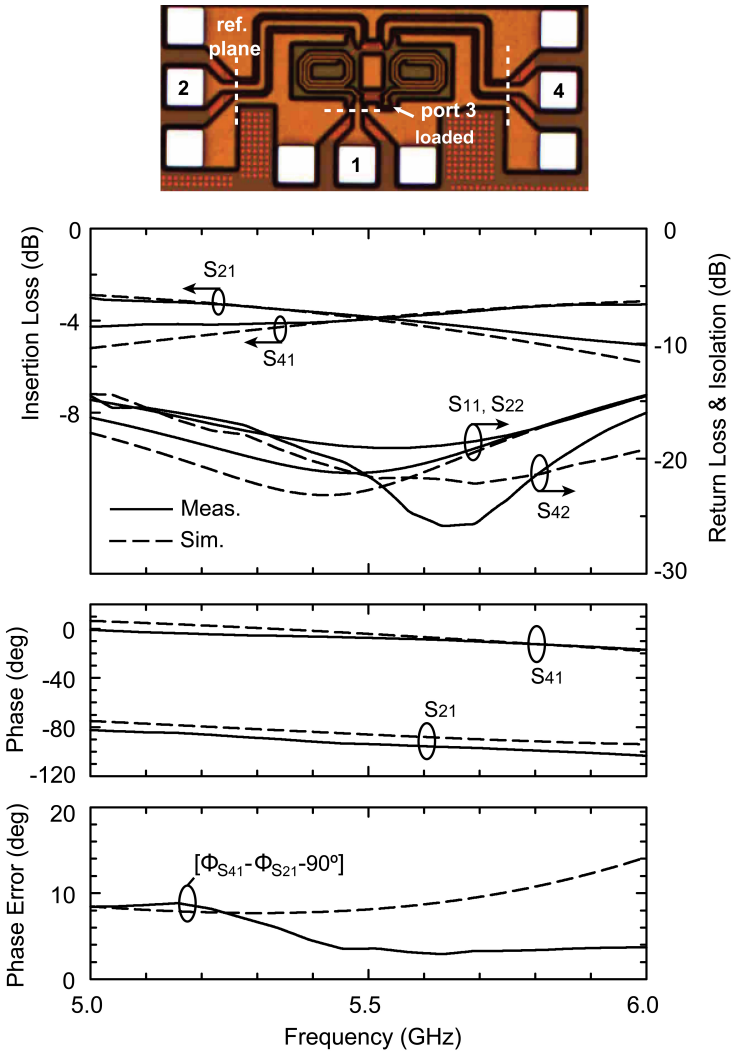


Figure 4.8: Microphotograph and measured S-parameters of the quadrature coupler test cell (Port 3 is loaded on-chip for measurement purposes).

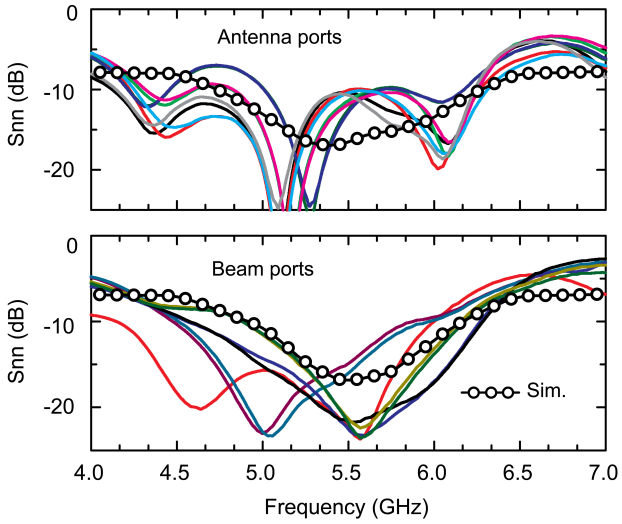


Figure 4.9: Measured return loss: beam ports and antenna ports.

bondwires, 3) 0.7 dB connector loss (Table 4.2). Note that the 3R and 3L beams show ∼1.5 dB higher gain than 1L-1R beams due to the antenna element factor. The 4L and 4R beams show a significant gain reduction below 5.3 GHz due to the large phase variation across the array and mutual coupling effects between the antennas (S_{21}= −15 dB at 5 GHz).

The on-chip loss was measured using three different methods: 1) On-chip CPW probe measurements (see Fig. 4.4a) with an input at port A1 and an output at port 1L or 4R or 3L, etc. and fitting the measured S-parameters to the Butler matrix circuit model with two ports terminated and all other ports left open circuited. S-parameter measurements were also done for an input at port A2 and an output at port 1L or 4R or 3L, etc. resulting in 64 total measurements. The on-chip measurements consistently resulted in a fitted loss of 3.5 dB at 5.5 GHz for all the port combinations. 2) Board level S-parameter measurements with one input port at A1 (or A2, or A3, etc.) and an output at port 1L or 4R or 3L, etc. and all other ports terminated in 50 Ω

Table 4.2: Gain of 8×8 Butler Matrix with Dipole Array at 5.5 GHz

Ideal Gain (dB)		11.0
Simulated Loss (dB)	On chip	3.5
	T-lines	2.0
	Connectors	0.7
Simulated Gain (dB)		4.8
Measured Gain (dB)		4.8±1

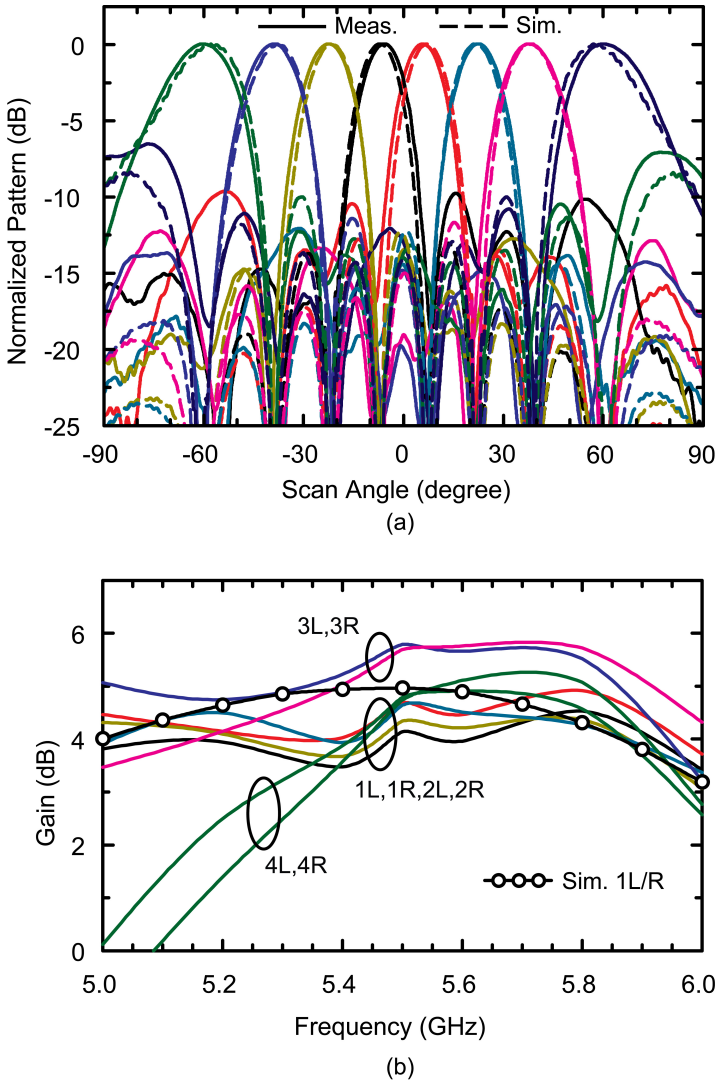


Figure 4.10: (a) Measured normalized beam patterns at 5.5 GHz (4L-3L-2L-1L-1R-2R-3R-4R from left to right), and (b) measured gain vs. frequency.

(see Fig. 4.5a without the antennas and with 50 Ω on all non-measured ports). In this case, the measurements include the transitions in and out of the silicon chip + transmission line loss + connector loss (2.7 dB in total). The measured S-parameters result in $<$ -10 dB return loss at 5.5 GHz for all the measured ports, and a loss of 3.5$\pm$1.5 dB at 5.5 GHz for the on-chip Butler matrix. 3) Antenna-based gain measurements as presented above and with a measured system level gain of 4.8$\pm$1 dB for the 8-element array which translates to a measured on-chip Butler matrix loss of 3.5$\pm$1 dB (see Table 4.2).

The measured patterns vs. frequency at 5-6 GHz are presented in Fig. 4.11 and show no beam steering vs. frequency due to the true-time-delay design of both the Butler matrix chip and the connecting transmission lines. The beamwidths change slightly with frequency and are diffraction limited (given by the array size in wavelengths). Only beams 1R-2R-3R-4R are shown, since the matrix is perfectly symmetrical. Fig. 4.12 presents the measured gains at θ=+7°, θ=+22°, θ=+39° and θ=+61° for all beams. It is clear that the 8$\times$8 Butler matrix results in good beam isolation (low side-lobes) at 5-6 GHz.

4.2.3 Extension to Full-Angle Scanning

The 8$\times$8 Butler matrix of Fig. 4.1 results in fixed beams and -3 dB cross-overs, which can be detrimental to the system link at the cross-over angles. A modified 8$\times$8 Butler matrix is shown in Fig. 4.13, where a progressive phase shift of 22° is applied to each element (-77°, -55°, -33°, -11°, 11°, 33°, 55°, and 77°) resulting a $\sim$7° scan-angle shift for each of the 8-beams. In this case, the visible-space (-80° to +80°) can be covered with $<$ 1-dB cross-overs. The phase delays in the modified Butler matrix can be easily designed using switched CMOS L-C networks [67].

4.3 4$\times$4 Butler Matrix at Ku-Band

4.3.1 Design

Fig. 4.14 illustrates the block diagram of the 4$\times$4 Butler matrix, which is based on 4-port 90° lumped-element couplers and fixed delay lines similar to the 8$\times$8 design. For a 12 GHz design, C_1=266 fF, C_2=120 fF and L_1=470 pH. The 45° delay lines are realized using a CLC π-network composed of C=94 fF, and L is synthesized using a short section of a 70.7 Ω transmission line. In addition, the 94 fF capacitor is absorbed into the shunt capacitor C_2 of the 90° coupler. The on-chip cross-over is done using metal layers MA (top metal) and

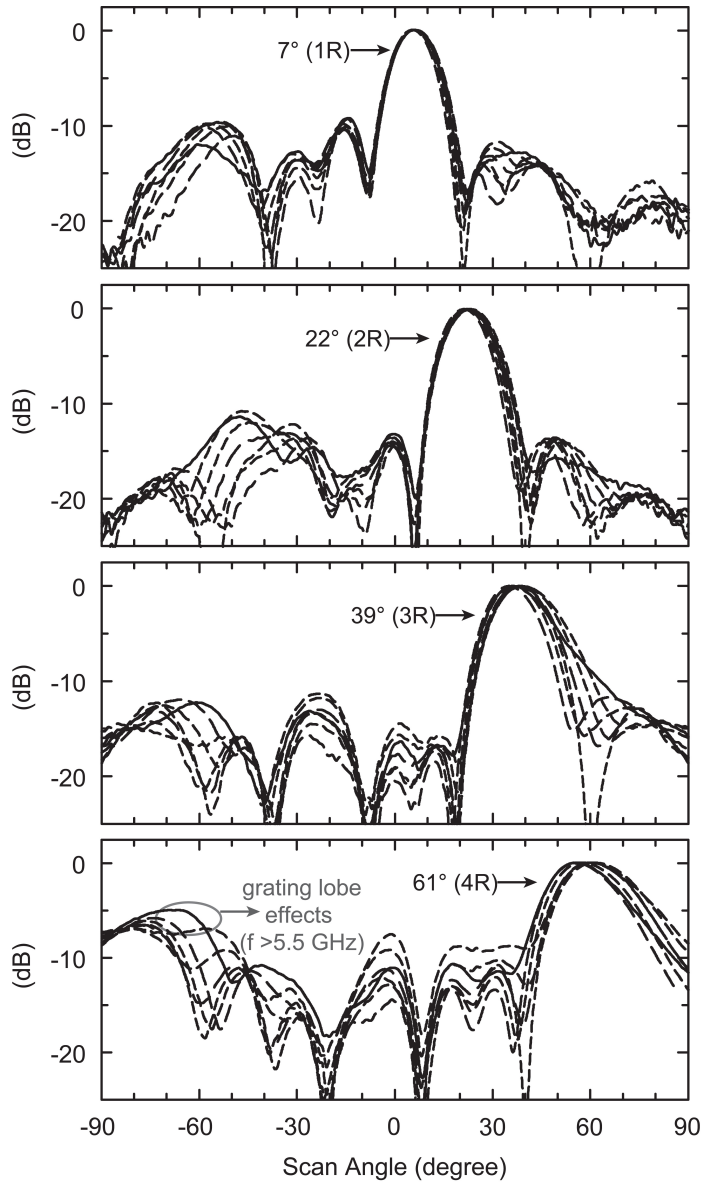


Figure 4.11: Measured normalized pattern for each beam at 5-6 GHz with 0.2 GHz steps. Beams 1L-4L are symmetrical with beams 1R-4R and not shown.

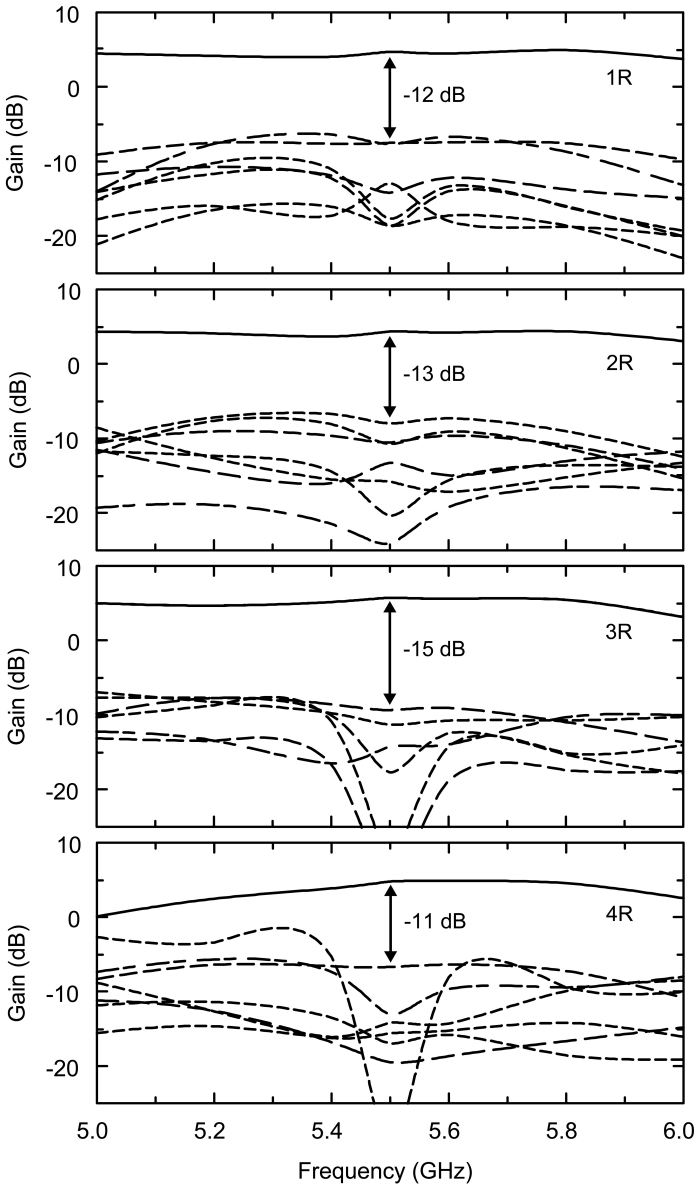


Figure 4.12: Measured gain at 7° (1R), 22° (2R), 39° (3R), and 61° (4R) for different beams resulting from the 8×8 Butler matrix.

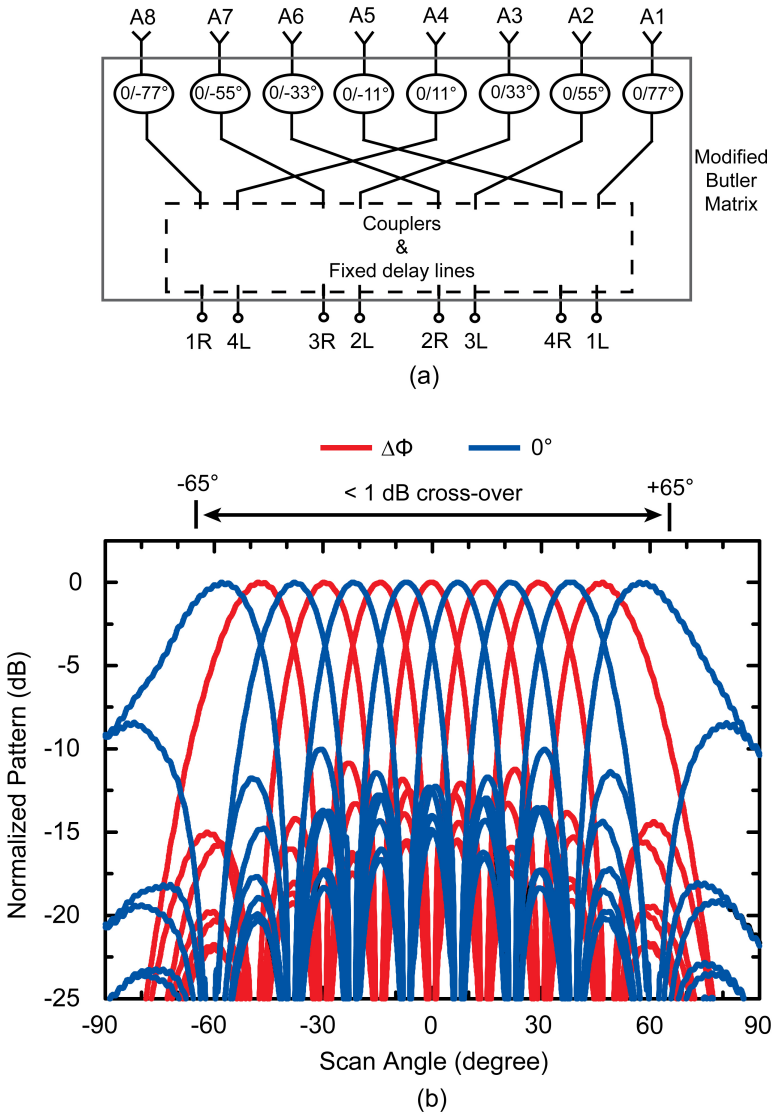


Figure 4.13: (a) Modified Butler matrix block diagram for near continuous angular coverage, and (b) simulated patterns with 0° and $\Delta\Phi$.

E1 (Fig. 4.15). The crossover isolation is simulated using full-wave electromagnetic analysis (Sonnet [17]) and is $>$ 50 dB at 12 GHz.

For a switched-beam implementation it is imperative to integrate an absorptive on-wafer SP4T switch since the impedance connected to the 1L, 1R, 2L, 2R ports must be matched to Z_0 irrespective of the port choice. In this design, a resistively loaded SP4T series-shunt switch with an inductive output match is used. A 30 μm-wide device is chosen for the series and shunt transistors, and results in an insertion loss of $\sim$1.5 dB and an isolation of $\sim$32 dB at 12 GHz. This results in a 4$\times$4 Butler matrix simulated gain of 2.1 dB including coupler, delay line, and SP4T switch losses.

The assembled 4$\times$4 Butler matrix is shown in Fig. 4.16 together with the chip layout. For reduced coupling between the antenna ports and a small silicon chip size, the layout is designed to have two ports on the east and two on the west (Fig. 4.16c). However, this necessitates a cross-over on the Duroid board which is designed using grounded CPW lines for reduced coupling (Fig. 4.17). Simulations show a return loss $<$ -10 dB and an isolation $>$ 30 dB up to 14 GHz (Fig. 4.17).

The board is based on an $\epsilon_{\rm r}$=2.2, h=10 mils Duroid substrate and true-time delay lines are used between the Butler matrix chip and the antennas. The silicon chip is placed on a grounded pedestal and input and output RF matching networks (shown in Fig. 4.18) are designed so as to compensate for the bondwire effects (S_{11} and S_{22} $<$ -10 dB at 10-14 GHz).

The 4-element antenna array is based on an angled dipole design with a spacing of 0.5λ_0 at 12 GHz. The antennas are resonant at 12 GHz with an $S_{11\rm ant}$ $<$ -10 dB at 10.5-14 GHz, a gain of 3 dB, and $<$ -17 dB element-to-element coupling.

4.3.2 Measurements

4$\times$4 Butler Matrix Chip: The silicon chip is fabricated in a standard 0.13-μm CMOS technology (IBM 8RF-DM). The 90° coupler and SP4T switch are first characterized using on-chip S-parameter measurements using stand-alone test cells. The 90° lumped-element coupler results in an insertion loss of 4.2$\pm$0.9 dB at 11-13 GHz with $<$ -10 dB input and output impedance match. The measured absolute phase error between ports 2 and 4 is $<$ 10° from 10.8 GHz to 13.3 GHz. The measured insertion loss and isolation of the absorptive SP4T switch are 2.1$\pm$0.05 dB and 29.5$\pm$1 dB, respectively at 11-13 GHz. The switch is well matched in both the ON and OFF states. The 4$\times$4 Butler matrix was then characterized on-wafer using multiple S-parameter measurements, and resulted in 4.6 dB insertion loss at 11-13 GHz including the

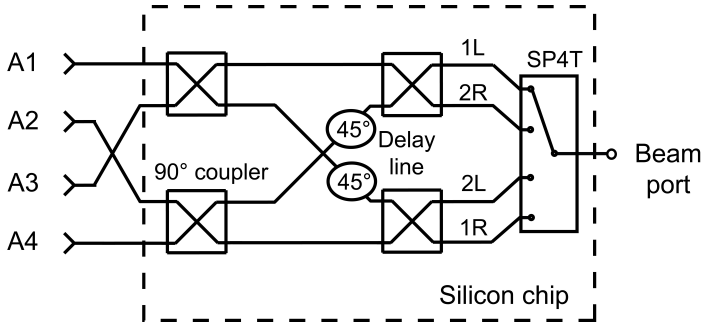


Figure 4.14: Block diagram of 4×4 Butler matrix.

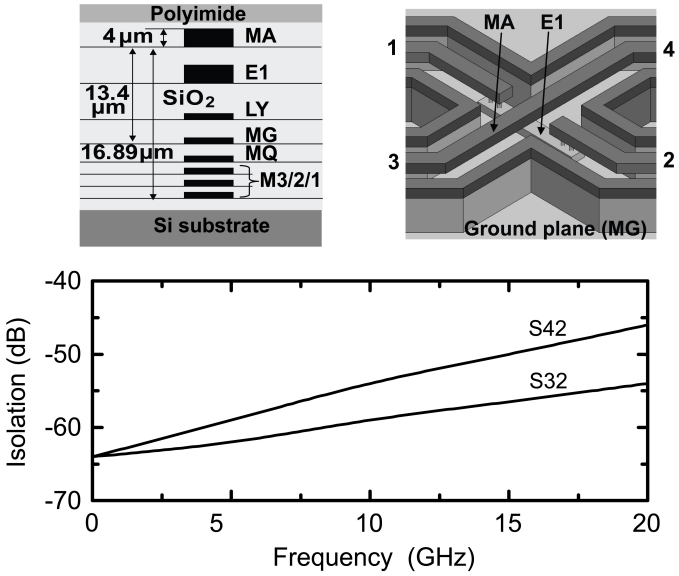


Figure 4.15: IBM 8RF process stack-up, on-chip cross-over layout, and simulated isolation between the different ports.

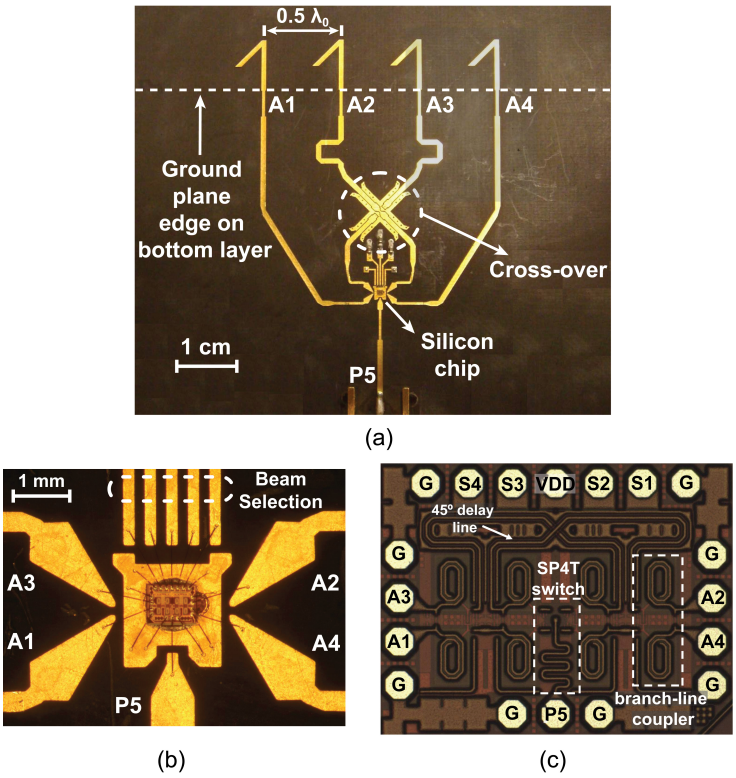


Figure 4.16: (a) Picture of the assembled 4×4 Butler matrix board, (b) close-up view of the silicon chip on board, (c) microphotograph of the 12 GHz 4×4 Butler matrix chip (size: 0.85×0.65 mm^2).

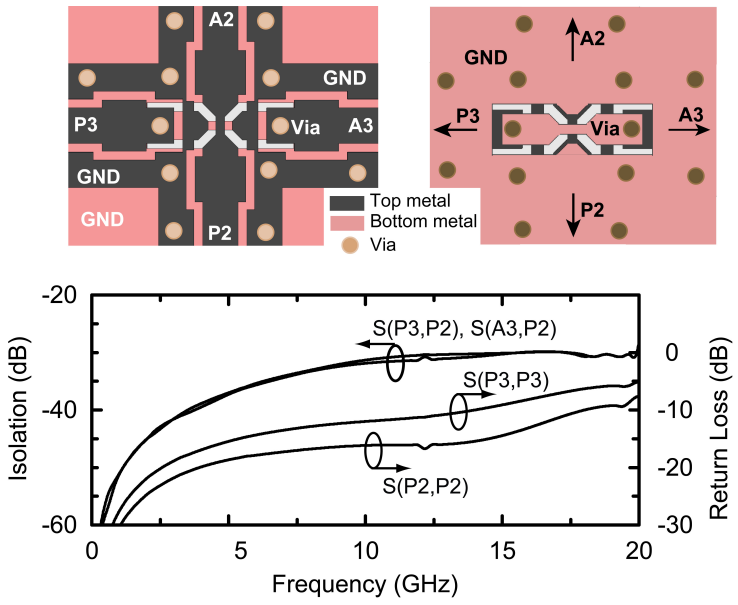


Figure 4.17: Layout and S-parameters of the cross-over on the Duroid board. Excellent isolation is achieved using grounded CPW lines.

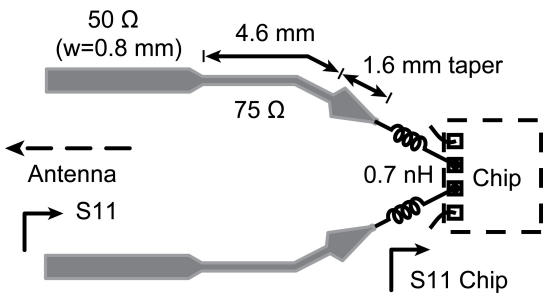


Figure 4.18: Input matching network for the 4×4 Butler matrix. The output matching network is similar and is not shown.

SP4T switch loss (2.4 dB without the switch loss).

4×4 Array Measurements: The measured output S_{22} of the beam-former chip is $<$ -10 dB at 10.5 and 13 GHz for all 4 beams due to the SP4T switch (Fig. 4.19a). The patterns are measured in an anechoic chamber using a standard gain horn antenna, and agree well with simulations with beams at 49° (2L), 15° (1L), +15° (1R), +49° (2R) (Fig. 4.19b). The simulations are based on ideal 90° couplers and delay lines, and not on the measured S-parameters of the stand-alone components. There is a slight deviation in the peak angle of 1L and 1R due to the phase error in the 90° couplers at 12 GHz.

The measured patterns vs. frequency at 11-13 GHz are presented in Fig. 4.20a and show no steering vs. frequency. It is clear that the 4×4 Butler matrix results in true-time delay operation at 12±1 GHz. The measured gain is done using the Friis transmission method and is calculated using P_t from the standard gain horn and P_r at the output of the 4×4 Butler matrix. The gain is 1.2±0.75 dB at 12 GHz for all beams and includes transmission-line, butler matrix, SP4T losses and any mutual coupling effects between the antennas (Fig. 4.20b). The predicted gain is 8.0 dB and the difference is attributed to: 1) 2.4 dB Butler matrix loss, 2) 2.2 dB SP4T loss, 3) 1.1 dB input/output transmission-line loss, 4) 0.2 dB connector loss.

Fig. 4.21 presents the measured gains at θ=49° and θ=15° for all four beams. It is clear that the 4×4 Butler matrix results in good beam isolation (low side-lobes) at 11-13 GHz.

4.4 Conclusion

This chapter demonstrated the first fully integrated 8×8 Butler matrix in 0.13-μm CMOS technology and a CMOS 4×4 Butler matrix at 11-13 GHz together with system-level measurements. The chip design is based on lumped-element couplers and phase-delay cells, occupying a very small area. The chip is assembled on a Teflon board with angled-dipole antennas

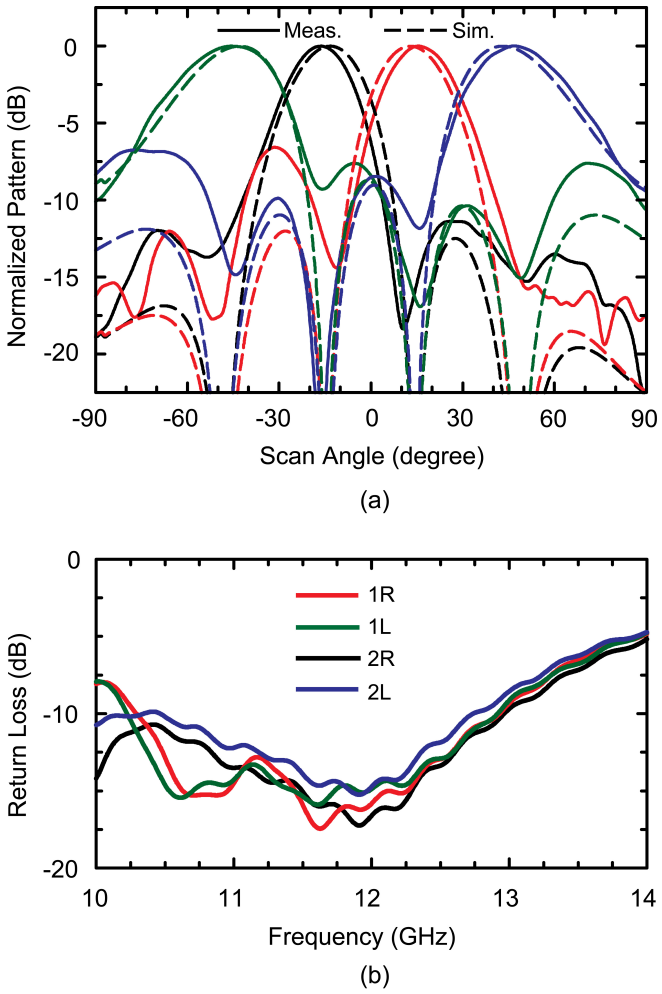


Figure 4.19: (a) Measured beam patterns at 12 GHz, and (b) measured output return loss.

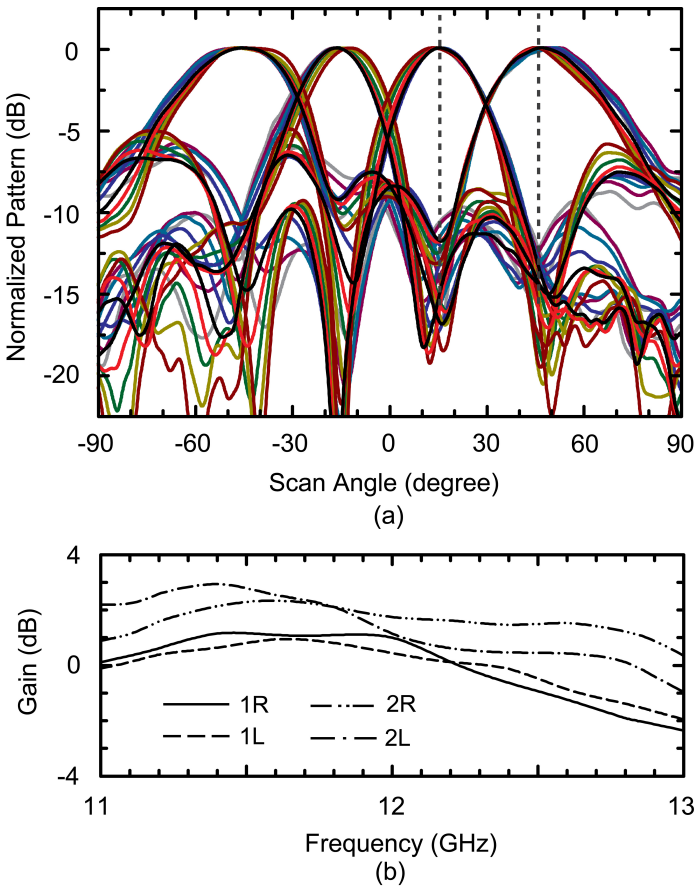


Figure 4.20: (a) Measured patterns at 11-13 GHz and (b) measured gain.

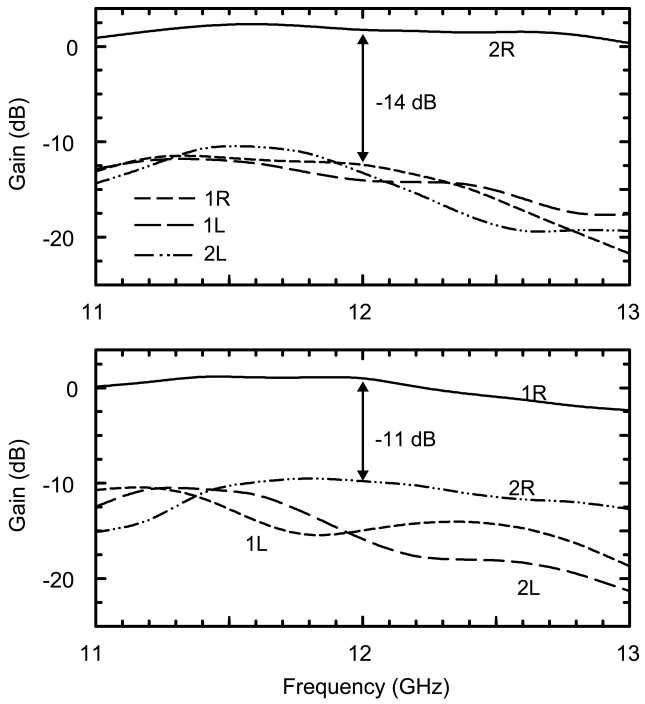


Figure 4.21: Measured gain at (a) 49° (2R), (b) 15° (1R) for the different beams resulting from the 4×4 Butler matrix.

and eight simultaneous beams are synthesized at -61° (4L), -39° (3L), -22° (2L), -7° (1L), 7° (1R), 22° (2R), 39° (3R) and 61° (4R) with less than 1° error in beam direction. The measured patterns and gains are demonstrated with complete characterization versus frequency at 5–6 GHz and 11–13 GHz. The design can be scaled to higher frequencies (24 GHz, 60 GHz, 77 GHz) for switched-beam high data-rate communication systems and automotive radars.

4.5 Acknowledgement

This work was supported by the Intel Corporation, Dr. Ian Young and Dr. Jad Rizk, program monitors.

Chapter 4 is in-part mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques, 2011. Berke Cetinoneri; Yusuf A. Atesal; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 4 is also in-part a reprint of the material as it appears in IEEE International Microwave Symposium Digest, 2010. Berke Cetinoneri; Yusuf A. Atesal; Jeong-Geun Kim; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

Chapter 5

Conclusion

This thesis presented advanced circuits for microwave and millimeter-wave communications using CMOS technology for different range of applications. A low-noise W-band amplifier and mW-level 170–200 GHz output doublers were demonstrated. In addition, high performance single-pole multiple-throw CMOS switches were presented with a measured state-of-the-art insertion loss and isolation up to 67 GHz. To further improve the scanning capabilities of the millimeter-wave systems, 8×8 and 4×4 Butler matrices were presented at 5–6 GHz and at 12 GHz, respectively. Finally, a gamma-ray detector with an operation principle based on microwaves was presented.

Chapter 2 presented a W-band low-noise amplifier with a record noise figure and balanced frequency doublers capable of high output power at 170–200 GHz range. These circuits are fabricated using IBM's 45-nm SOI CMOS technology, which was developed for digital and mixed-signal circuits, but can offer a lot of potential for 90–200 GHz applications with high f_t/f_{max} values. The SOI CMOS technology is analyzed in detail and the measured and simulated transistor-level results were presented. The W-band amplifier shows 11 dB gain at 95 GHz and achieves a noise figure of 6 dB. The large-signal measurements show a saturated output power of 7–8 dBm at 95 GHz with 9% of power-added efficiency. Next, a balanced doubler design is demonstrated with simulations showing the circuit optimization and the measurement results are discussed in detail. The G-band doubler results in an output power of 1 mW at 180 GHz. The amplifier and the doubler designs are eventually cascaded and the measurement results are presented with a peak output power of 0.5–1 mW at 170–195 GHz and a total conversion gain of -2 – -1 dB. The performance summary and comparison tables indicate that the circuits built using 45-nm SOI CMOS technology results in state-of-the-art performance at W-band and G-band.

Chapter 3 demonstrated millimeter-wave single-pole multiple-throw CMOS sw-itches for communication systems. A miniature DC–70 GHz single-pole four-throw (SP4T), 50–70 GHz single-pole double-throw (SPDT), and single-pole four-throw (SP4T) switches are built using 0.13-μm CMOS process. Several key transistor and CMOS technology features such as deep n-well transistors, high substrate contact resistance, and deep trench isolation are discussed. The DC-70 GHz SP4T switch is based on a series-shunt design with deep n-well CMOS transistors to improve the performance and occupies an active chip area of 0.24×0.23 mm^2. The SP4T has a measured insertion loss of less than 3.5 dB up to 67 GHz with greater than 25 dB isolation. The measured P1dB and IIP3 are 9–10 dBm and 20–21 dBm, respectively, and constant versus frequency. When this work was published, it represented the widest bandwidth SP4T switch in any CMOS technology to-date. Next, 50–70 GHz single-pole double-throw (SPDT) and single-pole four-throw (SP4T) switches, which are based on tuned λ/4 designs with output matching networks, are presented. The SPDT and SP4T switches result in a measured insertion loss of 2.0 and 2.3 dB at 60 GHz, with an isolation of $>$ 32 dB and $>$ 22 dB, respectively. When this work was published, it presented the lowest loss 60 GHz SPDT and SP4T switches and also the highest isolation SPDT switch in any CMOS technology to-date.

Chapter 4 presented 5–6 GHz 8×8 and Ku-band 4×4 Butler matrices in 0.13-μm CMOS technology with excellent patterns. The lumped-element design is discussed in detail with an emphasis on how the on-chip cross-overs are realized with good isolation. The fabricated Butler matrix chips are mounted on a Teflon board with 8 or 4 antennas, and the input/output matching networks are designed by considering the bondwire transitions from the chip to the board. Complete pattern and gain measurements versus frequency are presented and the measured patterns agree very well with simulations. The 8×8 design results in an insertion loss of 3.5 dB at 5.5 GHz, with a bandwidth of 5-6 GHz and no power consumption. The chip area is 2.5×1.9 mm^2 including all pads. The measured patterns of the 8×8 matrix show an isolation of $>$ 12 dB at 5-6 GHz. The 4×4 design results in an insertion loss of 2.4 dB at 12 GHz with a bandwidth of 11–13 GHz. The chip area is only 0.85×0.65 mm^2 including all pads, and the power consumption is $\sim$0 mA from a 1.5 V power supply. The pattern isolation is $>$ 11 dB at 11–13 GHz. Finally, A modified 8×8 matrix is also shown with a potential to replace small-element phased array systems with $<$ 1 dB pattern cross-over. CMOS Butler matrices offer a simple and low power alternative to replace 8-element phased-array systems for high gain transceivers. The applications areas are in high data-rate communications at 5–6 GHz and at 57–66 GHz. Also they can be excellent candidates for MIMO systems.

Appendix A demonstrated the first differential gamma-ray detector based on a contactless microwave cavity method at room temperature. The system is developed mainly for homeland security applications in order to detect low-energy gamma-ray photons with high energy resolution and good efficiency. The detection is done using a reflection-type cavity resonator with a detector-grade CZT crystal. Significantly lower noise floor is achieved compared to single-ended design leading to potential detection of low-energy gamma ray photons in the 100 keV – 1 MeV range. Next, new cavity designs, which can achieve higher electric field by applying a high DC voltage, are presented with initial simulation results for detecting low-energy single photons $<$ 100 keV. The proposed microwave-based detection principle may result in an improved performance.

There will be some future work for Chapter 2 and Appendix A. Regarding Chapter 2, a 2$\times$2 CMOS transmit array at 180 GHz was designed by my colleagues Fatih Golcuk and Jen Edwards as an extension of the amplifier/doubler design and this chip is scheduled to arrive on August 2011. The same amplifier/doubler design is used for each element and 4 elements are connected to on-chip slot ring antennas. The expected power generated on-chip will be 6 dBm and the total radiated power will be 3 dBm at 180 GHz, assuming 50 $\%$ antenna efficiency. The effective isotropic radiated power (EIRP) will be 15.6 dBm at 180 GHz. This work will be a demonstration of achieving high output power at sub-millimeter-wave frequencies using free-space power combining.

The future work for Appendix A will be the investigation of how the CZT and the cavity wall interface affects the detection sensitivity. In the current design, the mechanical contact between the CZT column and Aluminum cavity wall (silver plated) creates a Schottky barrier since silver acts as a rectifier. Therefore, there is no ohmic contact between the CZT and the cavity walls, and this can affect the detection performance significantly. This issue can be resolved by using another material, such as Indium, that will create an ohmic contact between the CZT and the cavity walls. Indium can provide an ohmic contact to CZT since its work function (4.12 eV) is approximately the same as the CZT electron affinity (4.3-4.5 eV). The CZT in the current cavity design will be taken out of the cavity and Indium will be evaporated on top and bottom and then finally annealed. The gamma-ray detection experiments will continue once this process is completed.

Appendix A

A Microwave-Based Gamma-Ray Detector

A.1 Introduction

In the recent years, detection of low energy radioactive materials has gained significance especially in the homeland security and material characterization fields. One of the techniques employed in these areas is microwaves, and includes different methods such as reflection, transmission or cavity resonance. Cavity resonance utilizing the microwave cavity perturbation (MCP) has been widely used due to its superior sensitivity and smaller detector-grade sample size [68]. In this method, an external photon changes the conductivity of the detector-grade sample, which in turn, results in a minute change in the quality factor (Q) of the resonant cavity. In order to analyze this excitation, which is in the order of microseconds, the Q of the cavity needs to be monitored in time domain. However, since it is not practical to measure the Q of a cavity in such a small period of time, this small change in Q can be measured using the power reflecting back from the cavity at resonance [69, 70].

The detector-grade sample inside the cavity is a semiconductor crystal and its conductivity changes locally due to photo-excitation of carriers inside this material. $Cd_{1-x}Zn_xTe$ ($x \sim 0.1$) (CZT) is a wide band-gap compound semiconductor and is used as a detector-grade crystal. Due to its favorable physical properties such as wide band-gap and high atomic number, it is a strong candidate to fulfill the requirements for gamma ray spectroscopy applications at room temperature.

Previously, it was shown that high energy X-ray photons (> 5 MeV) can be detected

using a CZT crystal in a microwave cavity at 79 K [71]. In this paper, a differential detection method is proposed with an optimized microwave cavity, and results in improved signal-to-noise ratio (SNR) and sensitivity at room temperature. Analytical calculations are presented, including the effect of close-in phase noise of the RF signal generator.

A.2 Operation Principle

Fig. A.1a shows the conceptual block diagram of a microwave based γ-ray detector using a reflection-type cavity resonator. A γ-ray creates localized free charges inside the detector grade CZT column. The new conductivity in this region (typically $<$ 0.5 mm sphere) can be calculated from:

$$\sigma_{\gamma-\mathrm{ray}} = \mathrm{q}(\mathrm{n}\mu_{\mathrm{n}} + \mathrm{p}\mu_{\mathrm{p}}) \tag{A.1}$$

where n and p are the number of free electrons and holes, and μ_{n}=1000 cm^2/Vs and μ_{p}=100 cm^2/Vs are the corresponding mobilities. The small power lost due to the free charges reduces the Q as:

$$Q' = Q - \Delta Q = \frac{\omega W_{\mathrm{stored}}}{P_{\mathrm{cavity}} + \mathrm{P}_{\gamma-\mathrm{ray}}} \cong Q\left(1 - \frac{P_{\gamma-\mathrm{ray}}}{P_{\mathrm{cavity}}}\right),$$
$$\frac{\Delta Q}{Q} = \frac{P_{\gamma-\mathrm{ray}}}{P_{\mathrm{cavity}}}, \tag{A.2}$$

where Q is the quality factor of the cavity without the γ-ray excitation but with the presence of the CZT column, and

$$P_{\gamma-\mathrm{ray}} = \frac{1}{2}\int \sigma_{\gamma-\mathrm{ray}} \mid \mathrm{E}_0 \mid^2 \mathrm{dV}_{\gamma-\mathrm{ray}} \tag{A.3}$$

The cavity resonator can be modeled as in Fig. A.1b. The decrease in the Q is represented by ΔR where,

$$Q' = \frac{\omega L}{R + \Delta R} \cong Q\left(1 - \frac{\Delta R}{R}\right) \quad \Rightarrow \quad \frac{\Delta R}{R} \cong \frac{\Delta Q}{Q} \tag{A.4}$$

The change in the quality factor results in a change in S_{11} such that:

$$\Delta S_{11} = S'_{11} - \mathrm{S}_{11} = \frac{\Delta \mathrm{R}}{\mathrm{R} + \mathrm{Z}_0} = \frac{\Delta \mathrm{R}}{\mathrm{R}} \frac{(1 + \mid \mathrm{S}_{11} \mid)}{2} \cong \frac{\Delta \mathrm{Q}}{2\mathrm{Q}} \tag{A.5}$$

with $|\mathrm{S}_{11}|$=0 for a critically coupled cavity.

The voltage change, $\Delta \mathrm{V}_{\mathrm{out}}$, due to the change in the reflected power is:

$$\Delta V_{\mathrm{out}} = \sqrt{2P_{\mathrm{in}}\mathrm{R}}\Delta S_{11} \cong \sqrt{2P_{\mathrm{in}}\mathrm{R}}\left(\frac{\Delta Q}{2Q}\right) \tag{A.6}$$

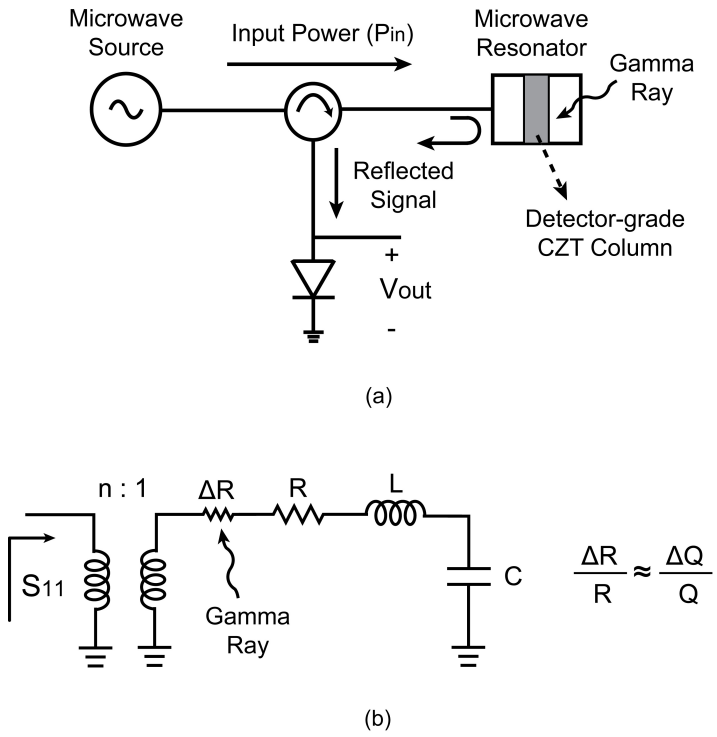


Figure A.1: (a) Conceptual block diagram for a microwave-based γ-ray detector, (b) RLC circuit model.

where $\Delta V_{\rm out}$ is the peak detected voltage in a 50 Ω load and $P_{\rm in}$ is the input power to the cavity. Using (A.2), we find

$$\Delta V_{\rm out} = \sqrt{2P_{\rm in}R}\left(\frac{P_{\gamma-{\rm ray}}}{2P_{\rm cavity}}\right) \tag{A.7}$$

To achieve high $\Delta V_{\rm out}$, one must operate under high input power ($\sim$1 W), and a high Q cavity. The high Q cavity results in a large electric field inside the cavity, which quickly separates electrons and holes inside the CZT column.

A.3 Cylindrical Cavity Design

A cylindrical cavity resonator is designed to resonate at 6 GHz without the CZT column under the TM_{010} mode (Fig. A.2). This results in resonance frequency, f_0, and electric field, E, as:

$$f_0 = \frac{p_{01}}{2\pi a\sqrt{\mu\epsilon}}, \quad E = \hat{z}E_0J_0(k_c r), \quad k_c = \frac{p_{01}}{a}, \tag{A.8}$$

where p_{01} is the first zero of the derivative of the Bessel function J_0 and a is the cavity radius (a=19 mm). In order to maximize the Q and the peak electric field, the height of the cavity should be equal to its radius. However, the CZT detector limited the height to 10 mm for a zero defect sample.

A cylindrical CZT block (ϵ_{r-czt}=11, σ_{czt}=10^{-10} Ω^{-1}cm^{-1}) with a radius of 2.5 mm and a height of 10 mm is then placed in the middle of the cavity. The CZT column does not distort the fields inside the cavity since it provides a tangential boundary condition all along the electric field direction (Fig. A.3). However, the CZT reduced f_0 to 4.5 GHz [72] and the cavity Q is calculated as:

$$Q = \frac{\omega W_{\rm stored}}{P_{\rm cavity}} = \frac{\omega W_{\rm stored}}{P_{\rm loss-wall} + \frac{1}{2}\int \sigma_{\rm czt} \mid E \mid^2 dV_{\rm czt}}, \tag{A.9}$$

where

$$W_{\rm stored} = 2\frac{1}{2}\int \epsilon_{\hat{r}} E_z^2 dV = \frac{1}{2}\epsilon_0 \pi h \mid E_0 \mid^2 J_1^2(p_{01})[\epsilon_{\rm czt} r_{\rm czt}^2 + (a_{\rm cavity}^2 - r_{\rm czt}^2)] \tag{A.10}$$

$$P_{\rm loss-wall} = \frac{1}{2\sigma\delta_s}J_1^2(p_{01})\frac{\epsilon_0}{\mu_0} \mid E_0 \mid^2 (2\pi ah + 2\pi a^2) \tag{A.11}$$

for $\sigma_{\rm czt}$=$10^{-10}\Omega^{-1}$cm^{-1} and $P_{\rm loss-wall} \gg 1/2\int\sigma_{\rm czt}|E|^2 dV_{\rm czt}$.

In order to optimize the detected voltage, a critically coupled cavity (S_{11}=0) is used. The coupling is achieved using an E-plane coupling rod, and as shown in [73], the distance of the coupling probe from the center, the length and diameter of the probe should be optimized. In addition, a tuning screw is implemented in order to manually tune the resonant frequency.

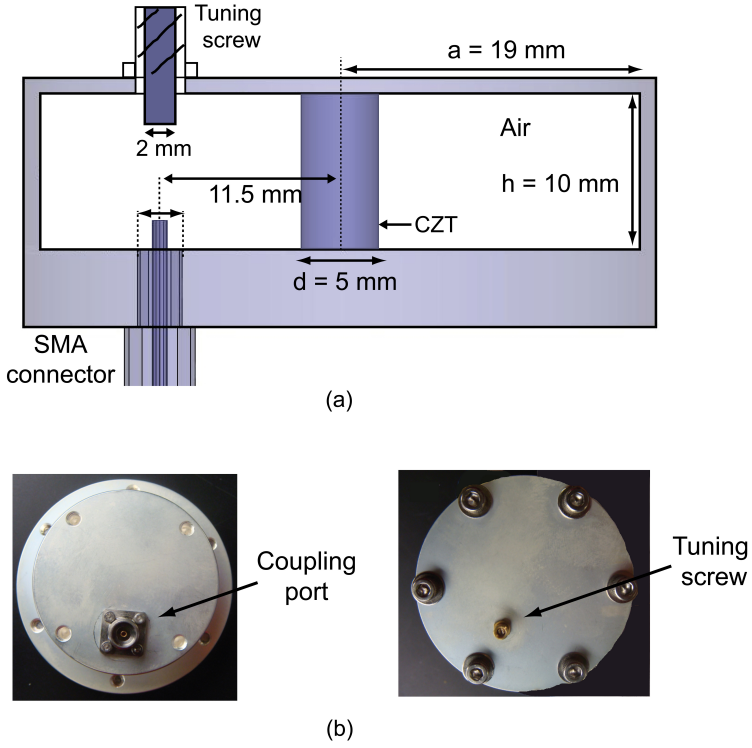


Figure A.2: (a) Cross-sectional diagram and (b) top/bottom view of the fabricated 4.5 GHz cavity.

The cavity design and optimization is done using HFSS^{TM}. The cavity is coated with a 7.6 μm thick silver layer (σ=63$\times$10^6 S/m). Fig. A.4 shows the simulated and measured S_{11} for two different cavities. For a critically coupled cavity, $Q_{loaded} \cong Q_{unloaded}/2$, and the measured unloaded Q is $\sim$3000 at 4.51 GHz.

A 1 MeV γ-ray creates 1.4$\times$10^5 free charges inside the CZT column. Using (A.11) and Q=3000, P_{cavity}=13.7$\times 10^{-11}|E_0|^2$ (m$^2/\Omega$), W_{stored}=1.6$\times 10^{-17}|E_0|^2$ (m^{2}s/Ω). Using the number of free charges and (A.3), $P_{\gamma-ray}$=1.23$\times 10^{-15}|E_0|^2$.

For an input power of 1 W, $|E_0|$=840 V/cm, W_{stored}=113 nJ, P_{cavity}=1 W (since S_{11}=0) and $P_{\gamma-ray}$=8.67 μW. This corresponds to $\Delta Q/Q \approx 10^{-5}$, ΔS_{11}=5$\times 10^{-6}$, and ΔV_{out} =50 μV in a 50 Ω load. The detection bandwidth should be at least 1-2 MHz to clearly detect a sharp instantaneous rise and a 2-4 μs decay. This results in a reflected power change of 25$\times 10^{-12}$ W (25 pW) in a 2 MHz bandwidth (or 12.5$\times 10^{-18}$ W/Hz) which is much larger than the receiver noise floor (NF of 10-15 dB). The minimum detectable signal is therefore dominated by the RF source 1/f noise combined with the S_{11} as shown in the next section.

A.4 Detector Design

Fig. A.5 shows the block diagram of the microwave γ-ray detector. A differential system with two different cavities is used so as to reduce the 1/f noise contribution. A circulator followed by mixer down-converts the reflected power from the cavity using a zero-IF (homodyne) technique. The LO path is aligned in phase with RF path using a phase shifter to result in a maximum output signal. The down-converted signal is then amplified with a gain of $\sim$30 dB and shaped with a 50 kHz - 2 MHz band-pass filter. The bandwidth of the amplifier-filter is determined according to the recombination time of the charges inside the CZT.

Noise Considerations: Fig. A.6 shows the effect of cavity reflection coefficient on the input signal. The reflected power demonstrates a sharp increase in its 1/f noise spectrum due to the rapid change in $|S_{11}|$ vs. frequency (high-Q design). In effect, the cavity absorbs the signal by 20 dB (S_{11}=-20 dB), but reflects all the associated close-in phase noise. This is clearly seen in Fig. A.6 and a 20 dB S/N degradation is measured at $\Delta f > 0.5$ MHz.

The 1/f noise which is reflected back from the cavity is then integrated over the detection bandwidth of 2 MHz in the homodyne mixer. The output noise can be found by:

$$V_{noise}^2 = \frac{G_{dwn}}{R_l} \int_0^{f_b} \frac{P_{in}}{PN} df \tag{A.12}$$

where G_{dwn} is the gain of the down-converter including the mixer and IF amplifiers, R_l is the

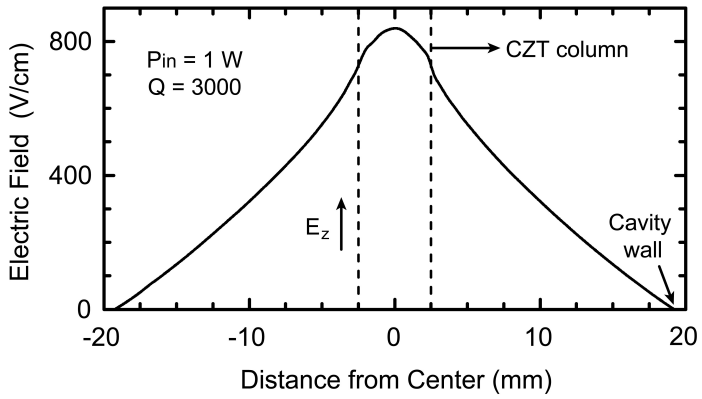


Figure A.3: Simulated E-field inside the cavity for TM_{010} mode. Note the discontinuity in the E-field slope at the air-CZT interface.

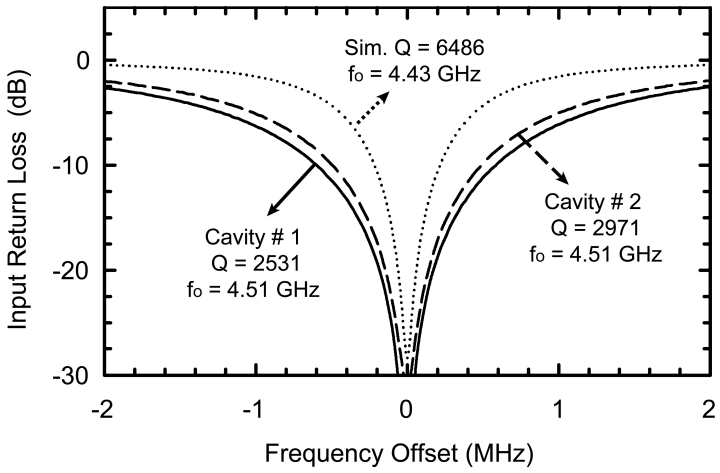


Figure A.4: Measured resonance frequency (f_0) and Q for two different cavities after manual tuning.

load resistance, PN is the phase noise (with respect to carrier) of the RF signal reflected back from the cavity, and f_b is the detection bandwidth. For P_{in}=1 W, G_{dwn}=28 dB, R_l=50 Ω and f_b=2 MHz, the measured and calculated output noise level is 6 mV_{rms} (V_{ppk} ∼30 mV) with a single-ended setup. The noise contributed by the downconverter block alone is much less (∼0.3 mV_{rms}) than the noise contributed by the RF source/cavity setup.

In order to achieve a better SNR at the output, a differential topology has been implemented (Fig. A.5). First, the input signal is divided into half and fed into two identical cavity resonators. The phase of the signal in one of the reflection paths is shifted by 180° and destructively combined with the signal from the other reflection path. As a result, both the signal and the associated noise are effectively canceled. The differential design has no effect on the probability of γ-ray detection since the γ-ray will always hit only one cavity at a time. Therefore, no coherent cancelation will occur for γ-rays.

Note that the detected output voltage will be 3 dB less than the single cavity detector due to the Wilkinson combiner properties. In theory, the differential setup with the cavities/mixer/IF amplifier should result in the ∼0.3 mV_{rms} noise (no noise due to RF source /cavities), but in practice, the two cavities are not identical and the Wilkinson coupler has - 17 dB rejection for 0/180° inputs. The measured output noise level was reduced to 0.8 mV_{rms} (V_{ppk} $>$ 5 mV) using the differential system. Therefore, the differential system provides 15 dB better S/N ratio than a single-ended one.

A.5 Measurements

Optional Test Path: An optional test path is implemented to measure the sensitivity of the detection circuit (Fig. A.5). An RF signal is coupled before the cavity using a 20 dB coupler. The signal is then either connected to 50 Ω or reflected back and injected to the system using an SPST switch. This results in a change in S_{11} (ΔS_{11}) which is equivalent to an external γ-ray excitation. Fig. A.7 shows the detected output voltages for injected power levels of 100 nW, 1 nW, 250 pW and 63 pW.

Gamma-Ray: A linear particle accelerator is used as the source to radiate bursts of γ-rays towards the cavities connected to the γ-ray detector. Lead blocks are used between the cavities and the γ-ray source in order to decrease the γ-ray energy level. As shown in Fig. A.8, additional lead blocks are used for one of the cavities such that only one cavity is hit by a higher energy γ-ray (configurations ”A” and ”B”). As a result of the differential system, the polarity of the detected signal changes for configuration A and B. The system is also tested for two

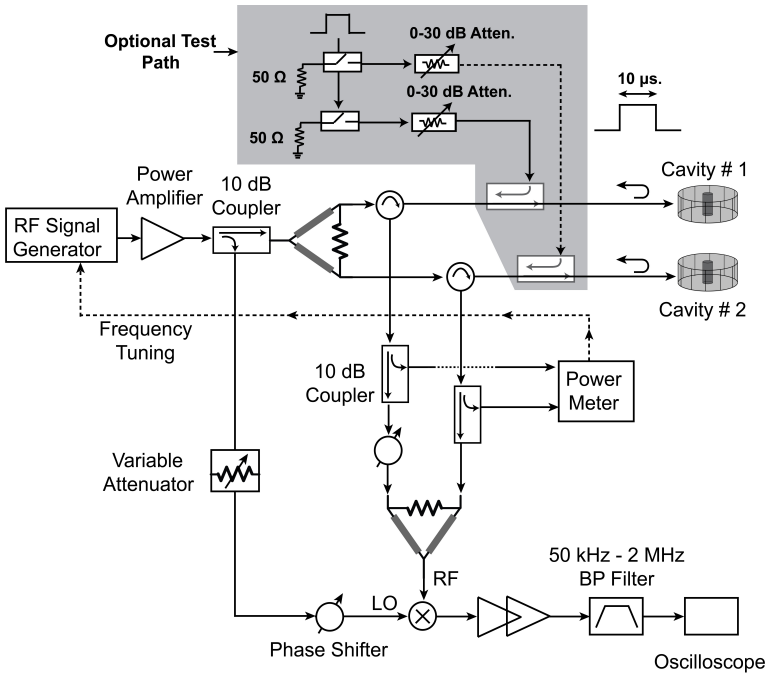


Figure A.5: Block diagram of the differential gamma-ray detector with optional test path.

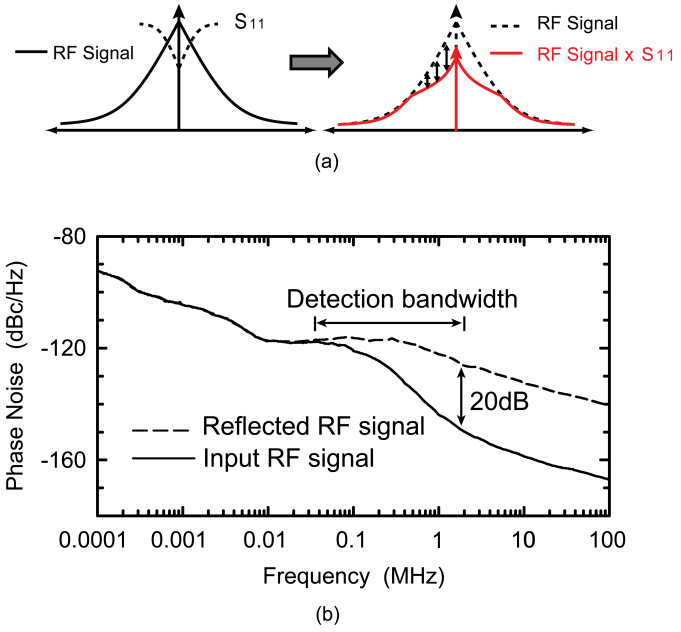


Figure A.6: (a) Conceptual diagram of the close-in phase noise degradation due to cavity S_{11}. (b) Measured RF signal phase noise before and after reflection from the high-Q cavity.

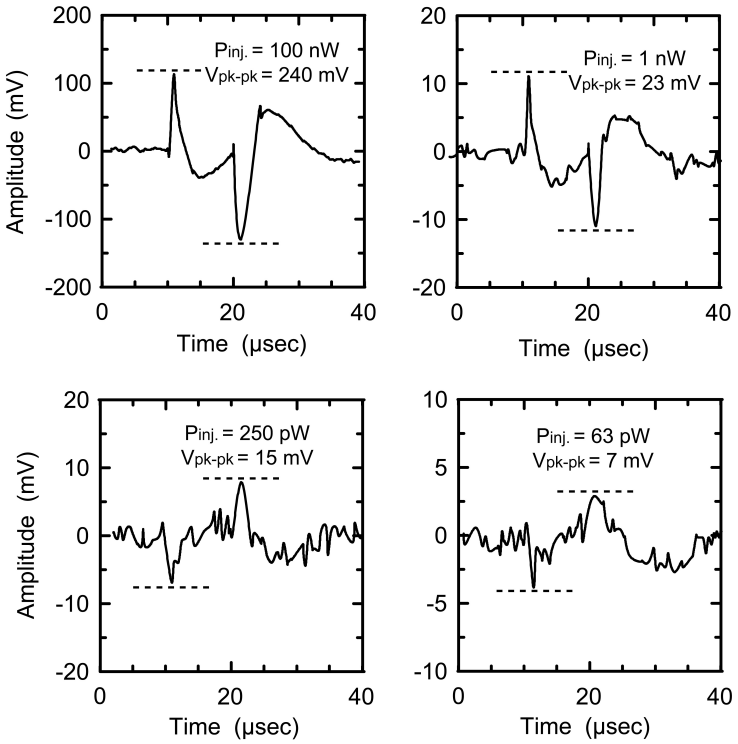


Figure A.7: Injected power (10 μs pulse) using matched switches and corresponding measured signal at the scope.

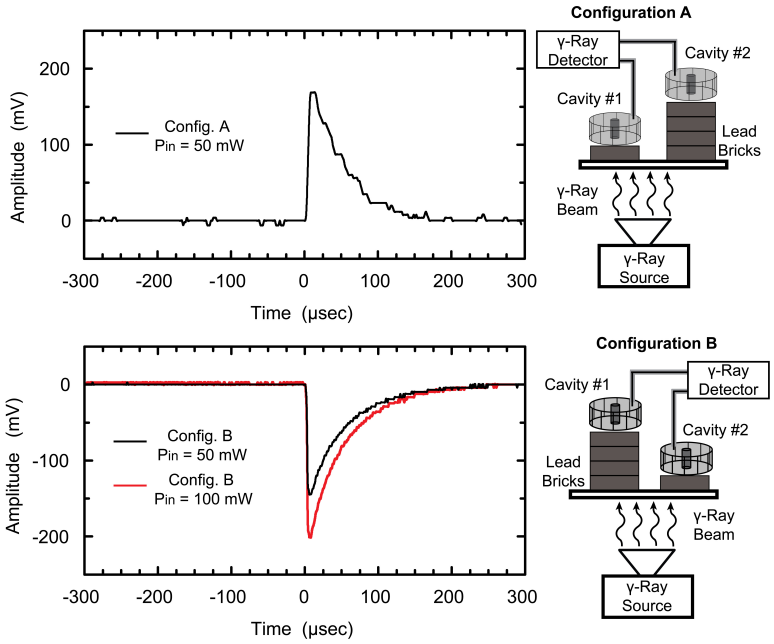


Figure A.8: Test setup and measured response for the γ-ray detector.

different power levels: 50 mW and 100 mW, and as expected, the detected signal level increased by a factor of $\sqrt{2}$. The decay time for the measured signals is 100 μs due to interaction of multiple photons within the CZT and having a much longer decay time as a result of large dose of γ-rays.

A.6 Cavity Designs for Improved Detection

A new approach is necessary in order to detect single γ-ray photons with less than 1 MeV energy. One way is to apply a high DC voltage to increase the electric field in the cavity resonator, which will prolong the electron-hole recombination time in CZT. Therefore, the lifetime of free charges will increase and the measurement sensitivity will be improved. In order to realize this idea, two cavity resonators, which are the same as the existing cavity design, are connected back-to-back as shown in Fig. A.9a. In this design, the high voltage (HV) is applied to the center plate shared by both cavities and the outer plates are connected to a common ground. As a result, a high electric field is generated along the vertical ($\hat{z}$) axis of the cavities. A 2-mil thick insulating spacer (Kapton film) is used to electrically isolate the high voltage wall of the cavity from the grounded parts.

The RF performance of the fabricated dual-cavity structure (Fig. A.9a) is tested in the

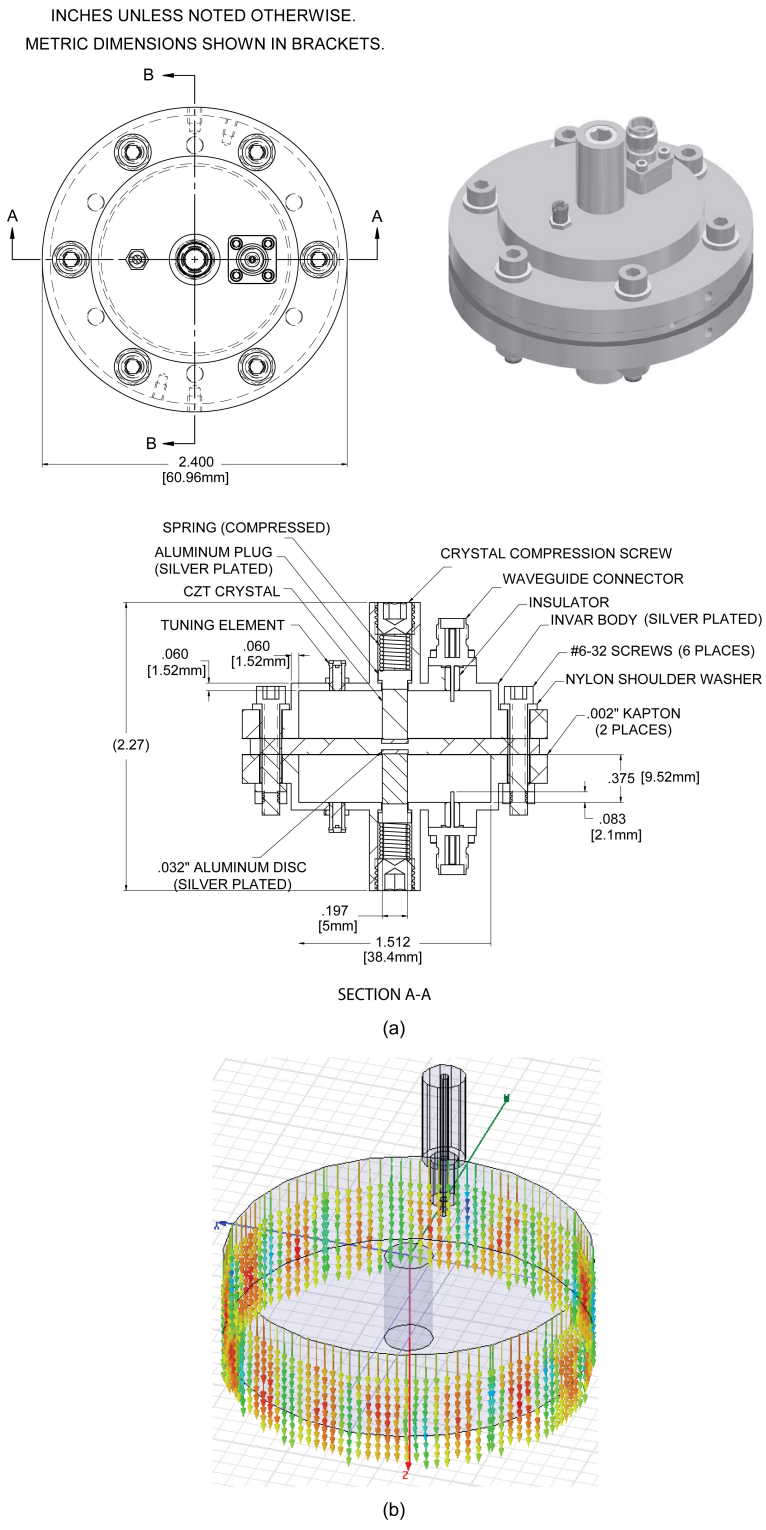


Figure A.9: (a) Initial dual-cavity design, (b) current distribution on the cavity walls.

lab before applying a high voltage. In the measurements, the measured Q of the cavity resonators was less than 400, whereas previously both of the cavities have Q's around 3200. The reason for the reduced Q in this new design is due to the insulating Kapton film, which creates a 2-mil gap on the cavity walls. Fig. A.9b shows the current distribution on the walls for a single cavity. The RF current oscillates along the cavity walls between the top and the bottom plates. When the Kapton film is placed between the middle plate and the walls, the RF current flow is disturbed and it leads to a dramatic decrease in Q. This can also be viewed as a result of the small gap at the middle plate and wall intersection, where the energy inside the cavity leaks out through this radial gap and contributes to the power loss, eventually degrading the Q.

In order to apply high voltage without a Q reduction, a new cavity design was developed. The high impedance caused by the Kapton film gap must be reduced in order to attain high Q values. This is achieved by impedance transformation through a quarter-wave section as seen in Fig. A.10a. The high impedance at the outer section of the cavity is transformed into a low impedance at the wall-middle plate intersection. Based on HFSS simulations, the required length of the transformer section yielding the highest Q is 7 mm and the simulated Q of the new cavity is 4300. The use of a quarter-wave section also enabled increasing the thickness of the Kapton film to 5 mils for enhanced material durability.

Another issue that needs to be taken into consideration is the dielectric breakdown that can occur between the HV middle plate and the grounded sections. The insulating Kapton film should be able to handle the applied HV, which is expected to be on the order of 3 kV DC. The 5-mil thick Kapton film has a dielectric breakdown of 3 kV/mil and therefore, prevents the dielectric breakdown across the metal plates. Once a sufficient isolation through the Kapton film is ensured, the new cavity structure is simulated using Ansoft's Maxwell 2D electromagnetic field simulator [74] and the simulation results can be seen in Fig. A.10b. The simulated electric field is on the order of 13 kV/mm, which is much lower then 3 kV/mil (120 kV/mm) breakdown limit of the Kapton film. The attention needs to be directed to the outer sides of the cavity, where the Kapton film ends. There is still a significant amount of electric field across the HV and grounded sections through the air, which has a dielectric breakdown of only 3 kV/mm. For this reason, a 2 mm $\times$ 4 mm notch section was created at the outer HV-ground boundary as seen in Fig. Fig. A.10. The static E-field simulations show that no breakdown occurs when there is Kapton film and the 2 mm $\times$ 4 mm opening.

Based on maintaining high Q with high voltage tolerance, a new dual-cavity resonator prototype was manufactured and the dimensions are shown in Fig. A.11. The measured input

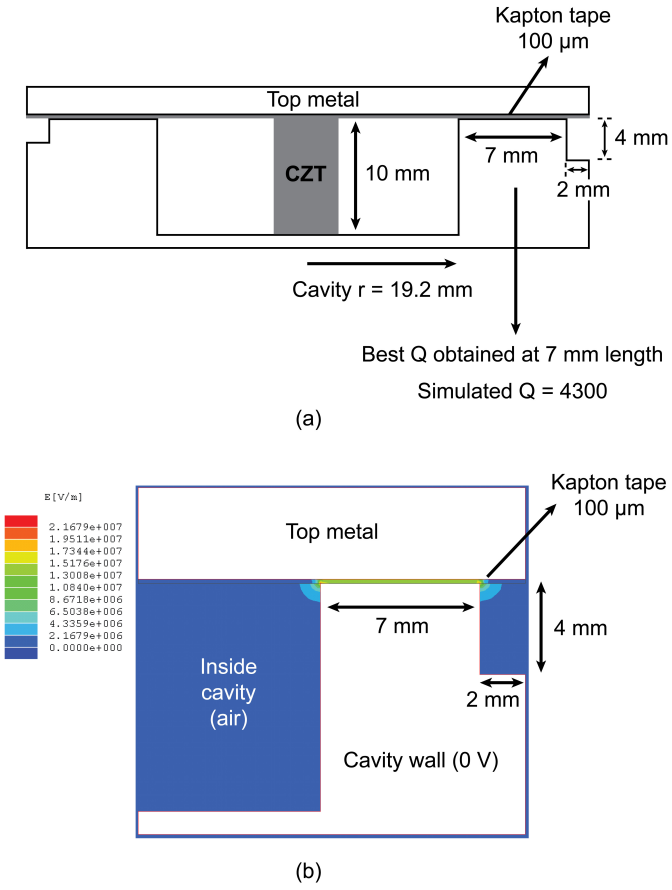


Figure A.10: (a) Cavity design with low-impedance quarter-wave matching. (b) Simulation of the electric field distribution between the top and the bottom metals of the cavity.

return loss of both cavities are shown in Fig. A.12. Good return loss and resonance frequency alignment is achieved for both cavities after a minor adjustment with the tuning element on the cavities. The resonance frequency is close to 4.5 GHz and agrees well with simulations. The measured Q of the cavities is around 1700 and should still be good enough for gamma ray detection. The difference between the measured and simulated Q factors is a result of extra loss in the fabricated cavity.

A.7 Conclusion

This appendix chapter demonstrated the first differential γ-ray detector based on a contactless microwave cavity method. Significant reduction in noise floor is achieved, reducing the sensitivity level of the system in order to detect low energy gamma-ray photons. The current system sensitivity is $<$ 100 keV, and the recent work was done to reduce it to $<$ 20 keV to ultimately detect single gamma-ray photons at room temperature. The system is currently being improved to increase the detection sensitivity.

A.8 Acknowledgement

This work is supported by U. S. Department of Homeland Security, Domestic Nuclear Detection Office.

This appendix chapter is in-part mostly a reprint of the material as it appears in IEEE International Microwave Symposium Digest, 2010. Berke Cetinoneri; Yusuf A. Atesal; Richard A. Kroeger; Gary Tepper; Jon Losee; Charles Hicks; Marc Rasmussen; Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

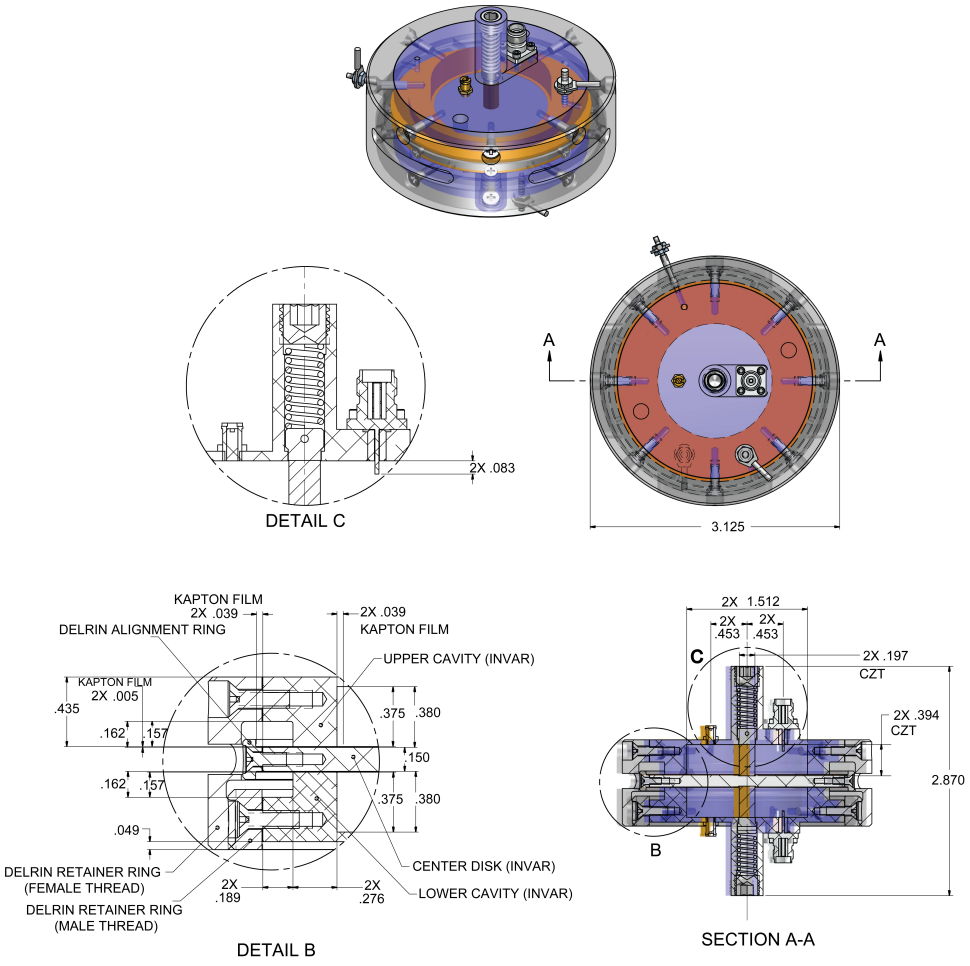


Figure A.11: Proposed dual-cavity resonator prototype for high Q and high voltage.

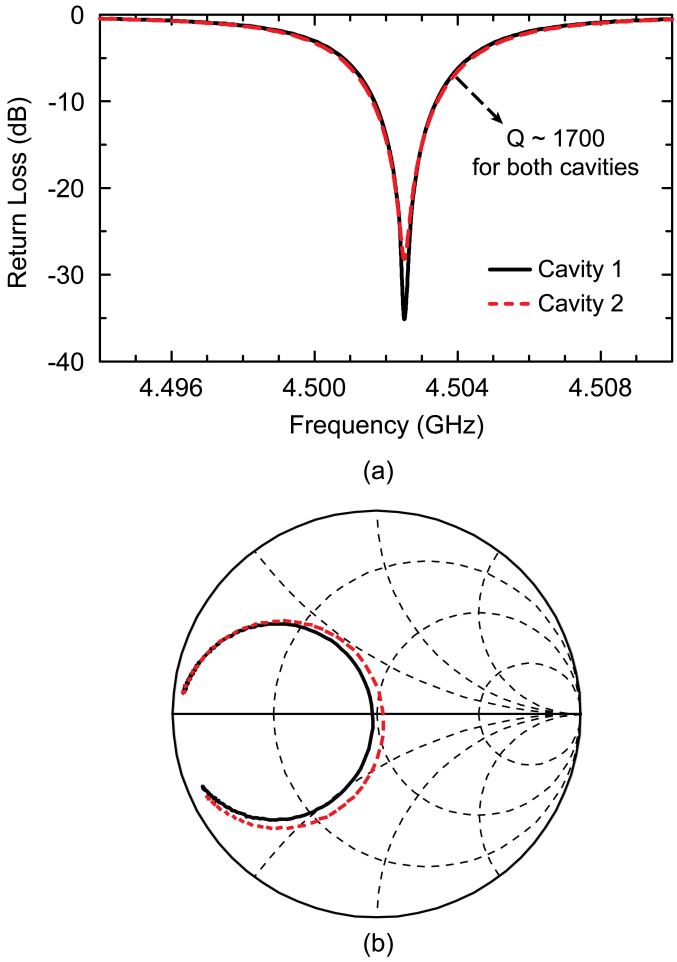


Figure A.12: Measured return loss of both cavity resonators (a) on dB scale and (b) on the Smith chart.

Bibliography

[1] J. W. May and G. M. Rebeiz, "Design and characterization of W-band SiGe RFICs for passive millimeter-wave imaging," *IEEE Trans. Microw. Theory and Tech.*, vol. 58, pp. 1420–1430, May 2010.

[2] L. Zhou, C.-C. Wang, Z. Chen, and P. Heydari, "A W-band CMOS receiver chipset for millimeter-wave radiometer systems," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 378–391, February 2011.

[3] A. Tomkins, P. Garcia, and S. P. Voinigescu, "A passive W-band imaging receiver in 65-nm bulk CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 1981–1991, October 2010.

[4] J. W. May, R. A. Alhalabi, and G. M. Rebeiz, "A 3 G-bit/s W-band SiGe ASK receiver with a high-efficiency on-chip electromagnetically-coupled antenna," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2010, pp. 87–90.

[5] Y. A. Atesal, B. Cetinoneri, M. Chang, R. A. Alhalabi, and G. M. Rebeiz, "Millimeter-wave wafer-scale silicon BiCMOS power amplifiers using free-space power combining," *IEEE Trans. Microw. Theory and Tech.*, vol. 59, pp. 954–965, April 2011.

[6] U. R. Pfeifer, E. Ojefors, and Y. Zhao, "A SiGe quadrature transmitter and receiver chipset for emerging high-frequency applications at 160GHz," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, February 2010, pp. 416–417.

[7] E. Laskin, P. Chevalier, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "165-GHz transceiver in SiGe technology," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 1087–1100, May 2008.

[8] E. Laskin, M. Khanpour, S. T. Nicolson, A. Tomkins, P. Garcia, A. Cathelin, D. Belot, and S. P. Voinigescu, "Nanoscale CMOS transceiver design in the 90-170-GHz range," *IEEE Trans. Microw. Theory and Tech.*, vol. 57, pp. 3477–3490, December 2009.

[9] Y.-S. Jiang, J.-H. Tsai, and H. Wang, "A W-band medium power amplifier in 90 nm CMOS," *IEEE Microwave and Wireless Comp. Lett.*, vol. 18, pp. 818–820, December 2008.

[10] M. Seo, B. Jagannathan, C. Carta, J. Pekarik, L. Chen, C. P. Yue, and M. Rodwell, "A 1.1V 150GHz amplifier with 8dB gain and +6dBm saturated output power in standard digital 65nm CMOS using dummy-prefilled microstrip lines," February 2009, pp. 484–485.

[11] D. Sandstrom, M. Varonen, M. Karkkainen, and K. A. I. Halonen, "W-band CMOS amplifiers achieving +10 dBm saturated output power and 7.5 dB NF," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 3403–3409, December 2009.

[12] O. Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: a systematic approach," *IEEE Journal of Solid-State Circuits*, vol. 46, pp. 583–597, March 2011.

[13] E. Seok, C. Cao, D. Shim, D. J. Arenas, D. B. Tanner, C.-M. Hung, and K. K. O, "A 410GHz CMOS push-push oscillator with an on-chip patch antenna," February 2008, pp. 472–473.

[14] S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, "Record RF performance of 45-nm SOI CMOS technology," December 2007, pp. 255–258.

[15] O. Inac, M. Uzunkol, and G. M. Rebeiz, "45 nm CMOS SOI technology for low-noise millimeter-wave amplifiers," *IEEE Trans. Microw. Theory and Tech.*, submitted for publication, May 2011.

[16] *Calibre, ver. 9.3.1.1*, www.mentor.com, Mentor Graphics Corp., Wilsonville, OR.

[17] *Sonnet v12*, www.sonnetsoftware.com, Sonnet Software Inc., Syracuse, NY.

[18] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. New Jersey: Wiley, 2005.

[19] D. G. Thomas and G. R. Branner, "Single-ended HEMT multiplier design using reflector networks," *IEEE Trans. Microw. Theory and Tech.*, vol. 49, pp. 990–993, May 2001.

[20] J.-J. Hung, T. M. Hancock, and G. M. Rebeiz, "High-power high-efficiency SiGe Ku- and Ka-band balanced frequency doublers," *IEEE Trans. Microw. Theory and Tech.*, vol. 53, pp. 754–761, February 2005.

[21] S. A. Maas, *Nonlinear microwave and RF circuits*. Massachusetts: Artech House, 2003.

[22] K. Yau, I. Sarkas, A. Tomkins, P. Chevalier, and S. P. Voinigescu, "On-wafer S-parameter de-embedding of silicon active and passive devices up to 170 GHz," in *IEEE Int. Microwave Symp. Dig.*, May 2010, pp. 600–603.

[23] *CMOS 12S0 (SOI12S0) Technology Design Manual*, www.ibm.com, IBM Corp., Hopewell Junction, NY.

[24] *Erickson Power Meter PM4*, www.vadiodes.com, Virginia Diodes, Inc., Charlottesville, VA.

[25] E. Ojefors, B. Heinemann, and U. R. Pfeiffer, "Active 220- and 325-GHz frequency multiplier chains in an SiGe HBT technology," *IEEE Trans. Microw. Theory and Tech.*, vol. -, p. IEEE early access, May 2011.

[26] L. Wang, Y.-Z. Xiong, B. Zhang, S.-M. Hu, and T.-G. Lim, "Millimeter-wave frequency doubler with transistor grounded-shielding structure in 0.13-μm SiGe BiCMOS technology," *IEEE Trans. Microw. Theory and Tech.*, vol. -, p. IEEE early access, May 2011.

[27] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60 GHz receiver and transmitter chipset for broadband communications," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2820–2831, December 2006.

[28] Y. Jain, S. Sundararaman, and P. Heydari, "A CMOS 22-29 GHz receiver front-end for UWB automotive pulse-radars," in *IEEE CICC*, September 2007, pp. 757–760.

[29] T. Mitomo, R. Fujimoto, N. Ono, R. Tachibana, H. Hoshino, Y. Yoshihara, Y. Tsutsumi, and I. Seto, "A 60-GHz CMOS receiver front-end with frequency synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 1030–1037, April 2008.

[30] I. Gresham, N. Kinayman, A. Jenkins, R. Point, A. Street, Y. Lu, A. Khalil, R. Ito, and R. Anderson, "A fully integrated 24 GHz SiGe receiver chip in a low-cost QFN plastic package," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2006, pp. 371–374.

[31] Y. Jin and C. Nguyen, "Ultra-compact high-linearity high-power fully integrated DC-20-GHz 0.18-μm CMOS T/R switch," *IEEE Trans. Microw. Theory and Tech.*, vol. 55, pp. 30–36, January 2007.

[32] B.-W. Min and G. M. Rebeiz, "Ka-band low-loss and high-isolation switch design in 0.13-μm CMOS," *IEEE Trans. Microw. Theory and Tech.*, vol. 56, pp. 1364–1371, June 2008.

[33] S.-F. Chao, H.-W. Wang, C.-Y. Su, and J. G. J. Chern, "A 50-94 GHz CMOS SPDT switch using traveling-wave concept," *IEEE Microwave and Wireless Comp. Lett.*, vol. 17, pp. 130–132, February 2007.

[34] A. Tomkins, P. Garcia, and S. Voinigescu, "A 94 GHz SPST switch in 65 nm bulk CMOS," in *IEEE CSICS Digest*, October 2008, pp. 139–142.

[35] M.-C. Yeh, Z.-M. Tsai, and H. Wang, "A miniature DC-to-50 GHz CMOS SPDT distributed switch," in *IEEE EGAAS*, October 2005, pp. 665–668.

[36] I. Kallfass, S. Diebold, H. Massler, S. Koch, M. S. Eggebert, and A. Leuther, "Multiple-throw millimeter-wave FET switches for frequencies from 60 up to 120 GHz," in *IEEE European Microwave Conference*, October 2008, pp. 1453–1456.

[37] B.-W. Min and G. M. Rebeiz, "A compact DC-30 GHz 0.13-μm CMOS SP4T switch," in *IEEE SiRF*, January 2009, pp. 1–4.

[38] ——, "Ka-band low-loss and high-isolation 0.13-μm CMOS SPST/SPDT switches using high substrate resistance," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2007, pp. 569–572.

[39] A. Tomkins, R. A. Aroca, T. Yamamoto, S. T. Nicolson, Y. Doi, and S. P. Voinigescu, "A Zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2085–2099, August 2009.

[40] K. Koh, J. W. May, and G. M. Rebeiz, "A millimeter-Wave (40-45 GHz) SiGe BiCMOS 16-element phased-array transmitter," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 1498–1509, May 2009.

[41] Y. Yu, P. Baltus, A. van Roermund, A. de Graauw, and E. V. der Heijden, "A 60 GHz digitally controlled RF-beamforming," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2009, pp. 211–214.

[42] T. Yu and G. M. Rebeiz, "A 22-24 GHz 4-element CMOS phased array with on-chip coupling characterization," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 2134–2143, September 2008.

[43] M.-D. Tsai and A. Natarajan, "60 GHz passive and active RF-path phase shifters in silicon," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2009, pp. 223–226.

[44] D.-W. Kang, J.-G. Kim, B.-W. Min, and G. Rebeiz, "Single and 4-element Ka-band transmit/receive phased-array silicon RFICs with 5-bit amplitude and phase control," *IEEE Trans. Microw. Theory and Tech.*, vol. 57, pp. 3534–3543, December 2009.

[45] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four element phased-array at 60 GHz with RF-IF conversion block in 90nm CMOS process," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2009, pp. 207–210.

[46] S. Kishimoto, N. Orihashi, Y. Hamada, M. Ito, and K. Maruhashi, "A 60-GHz band CMOS phased array transmitter utilizing compact baseband phase shifters," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2009, pp. 215–218.

[47] K. Koh and G. M. Rebeiz, "An X- and Ku-band 8-element phased-array receiver in 0.18-μm SiGe BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 1360–1371, June 2008.

[48] D.-W. Kang, K.-J. Koh, and G. M. Rebeiz, "A Ku-band 2-antenna 4-simultaneous beams SiGe BiCMOS phased array receiver," *IEEE Trans. Microw. Theory and Tech.*, vol. 58, pp. 771–780, April 2010.

[49] B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A two-channel Ku-band BiCMOS digital beam-forming receiver for polarization-agile phased-array applications," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2009, pp. 127–130.

[50] J. Butler and R. Howe, "Beamforming matrix simplifies design of electronically scanned antennas," in *Electronic Design*, April 1961, pp. 170–173.

[51] J. P. Shelton and J. K. Hsiao, "Reflective Butler matrices," *IEEE Trans. Antennas and Propagation*, vol. 27, pp. 651–659, September 1979.

[52] G. Tudosie, H. Barth, and R. Vahldieck, "A compact LTCC Butler matrix realization for phased array applications," in *IEEE Int. Microwave Symp. Dig.*, June 2006, pp. 441–444.

[53] M. Bona, L. Manholm, J. P. Starski, and B. Svensson, "Low-loss compact Butler matrix for a microstrip antenna," *IEEE Trans. Microw. Theory and Tech.*, vol. 50, pp. 2069–2075, September 2002.

[54] C.-H. Tseng, C.-J. Chen, and T.-H. Chu, "A low-cost 60-GHz switched-beam patch antenna array with Butler matrix network," *IEEE Antennas and Wireless Prop. Lett.*, vol. 7, pp. 432–435, 2008.

[55] B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A miniature DC-70 GHz SP4T switch in 0.13-μm CMOS," in *IEEE Int. Microwave Symp. Dig.*, June 2009, pp. 1093–1096.

[56] Y. A. Atesal, B. Cetinoneri, and G. M. Rebeiz, "Low-loss 0.13-μm CMOS 50–70 GHz SPDT and SP4T switches," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2009, pp. 43–46.

[57] L. Schulwitz and A. Mortazawi, "A compact dual-polarized multibeam phased-array architecture for millimeter-wave radar," *IEEE Trans. Microw. Theory and Tech.*, vol. 53, pp. 3588–3594, November 2005.

[58] ——, "A new low loss Rotman lens design using a graded dielectric substrate," *IEEE Trans. Microw. Theory and Tech.*, vol. 56, pp. 2734–2741, December 2008.

[59] S. Lee, S. Song, Y. Kim, J. Lee, C.-Y. Cheon, K.-S. Seo, and Y. Kwon, "A V-band beam-steering antenna on a thin-film substrate with a flip-chip interconnection," *IEEE Microwave and Wireless Comp. Lett.*, vol. 18, pp. 287–289, April 2008.

[60] C. Chang, T. Chin, J. Wu, and S. Chang, "Novel design of a 2.5-GHz fully integrated CMOS Butler matrix for smart-antenna systems," *IEEE Trans. Microw. Theory and Tech.*, vol. 56, pp. 1757–1763, August 2008.

[61] T. Chin, S. Chang, C. Chang, and J. Wu, "A 24 GHz CMOS Butler matrix MMIC for multi-beam smart antenna systems," in *IEEE Radio Frequency Integrated Circuits Symp.*, June 2008, pp. 633–636.

[62] K. Park, W. Choi, Y. Kim, K. Kim, and Y. Kwon, "A V-band switched beam-forming network using absorptive SP4T switch integrated with 4×4 Butler matrix in 0.13-μm CMOS," in *IEEE Int. Microwave Symp. Dig.*, May 2010, pp. 73–76.

[63] D. M. Pozar, *Microwave Engineering*, 2nd ed. New York: Wiley, 1998.

[64] *Ansoft HFSS v11*, www.ansoft.com, ANSYS Inc., Canonsburg, PA.

[65] R. A. Alhalabi and G. M. Rebeiz, "High-efficiency angled-dipole antennas for millimeter-wave phased array applications," *IEEE Trans. Antennas and Propagation*, vol. 56, pp. 3136–3142, October 2008.

[66] C. A. Balanis, *Antenna Theory: Analysis and Design*, 3rd ed. New Jersey: Wiley, 2005.

[67] B.-W. Min and G. M. Rebeiz, "Single-ended and differential Ka-band BiCMOS phased array front-ends," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 2239–2250, October 2008.

[68] V. Subramanian, V. R. K. Murthy, and J. Sobhanadri, "Sensitivity analysis of transient measurements using the microwave cavity perturbation technique," *AIP Journal of Applied Physics*, vol. 83, pp. 837–842, January 1998.

[69] V. Subramanian and J. Sobhanadri, "New approach of measuring the Q factor of a microwave cavity using the cavity perturbation technique," *AIP Review of Scientific Instruments*, vol. 65, pp. 453–455, January 1994.

[70] K. R. Richter, "Measurement of short time changes of cavity Q and resonant frequency," *IEEE Trans. Microw. Theory and Tech.*, vol. 17, pp. 339–344, June 1969.

[71] G. Tepper and J. Losee, "A contactless, microwave-based radiation detector," *Nuclear Instruments and Methods in Physics Research*, vol. 458, pp. 472–477, February 2001.

[72] R. Lech and J. Mazur, "Analysis of circular cavity with cylindrical objects," *IEEE Trans. Microw. Theory and Tech.*, vol. 55, pp. 2115–2123, October 2007.

[73] D. Kajfez and P. Guillon, *Dielectric Resonators*. Massachusetts: Artech House, 1986.

[74] *Maxwell 2D SV*, www.ansoft.com, Ansoft Corp., Pittsburgh, PA.