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Characterization and Write Error Rates of Magnetic Tunnel Junctions

A thesis submitted in partial satisfaction  
of the requirements for the degree of Master of Science  
in Electrical Engineering

by

Xueqing Cai

2014

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## ABSTRACT OF THE THESIS

### Characterization and Write Error Rates of Magnetic Tunnel Junctions

by

Xueqing Cai

Master of Science in Electrical Engineering

University of California, Los Angeles, 2014

Professor Kang L. Wang, Chair

There are many parameters necessary for magnetic tunnel junctions (MTJs) to be commercially competitive with established CMOS memory technologies, and one is the reliability of switching, characterized by the write error rate (WER) parameter. WER is a key requirement particularly for magnetoresistive random access memory (MRAM) applications. For lower energy consumption, better bit density, and higher endurance, electric field controlled devices can be used instead of current controlled spin-torque transfer (STT) switching. This thesis experimentally investigates low WER of voltage controlled MTJs using a large number of write trials. In addition, other parameters of MTJ performance are characterized and investigated, including perpendicular magnetic anisotropy (PMA), the voltage-controlled magnetic anisotropy (VCMA) effect, and critical switching voltage at different device sizes. Experimental WER results for our presently fabricated devices are presented and analyzed. Methods are proposed to further reduce the WER by reducing switching speed, as well as materials optimization of the MTJ to reduce damping factor.

The thesis of Xueqing Cai is approved.

Puneet Gupta

Oscar Stafsudd

Kang L. Wang, Committee Chair

University of California, Los Angeles

2014

## Dedication

I would like to express heartfelt gratitude to everyone who helped me through the two years of graduate school at UCLA, especially my mentor Juan G. Alzate for his patient help in teaching me everything magnetic almost from scratch; Farbod Ebrahimi who made indispensable contributions to the experiment setup through programming; Professor Pedram Khalili Amiri for his invaluable experience in directing the focus of my research; and last but not least Professor Kang L. Wang for his support and guidance of my academic career as a whole. Secondly I want to thank friends (a giant overlap with the first group) who've made my stay at UCLA so pleasant that it feels like two years have gone by in a flash. Finally I dedicate this thesis to my parents, without whom I wouldn't be here today.

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## Chapter 1: Introduction and Motivation

The information age is fully upon us: electronic devices are more and more ubiquitous in daily life, and electronic data is being generated in larger and larger densities. It is a race to provide fast, reliable, energy efficient, and dense electronic memory storage to keep pace with data storage needs. Currently, long term data is stored in non-volatile memory, which is named such because it can retain information without external power. Current commercial non-volatile memories include NAND or NOR flash, which rely on floating gate CMOS transistors to store electric charge. For short-term memory applications, and applications like CPU cache for which speed is important, volatile memory is used. These devices need external power to retain information, so it is called volatile memory. DRAM (dynamic random access memory) and SRAM (static random access memory) are the two popular ones, and DRAM in particular is used for high speed and high density applications.

However these CMOS based memories are meeting increasingly serious difficulties in scaling, posed by fabrication hurdles such as the cost and complexity of lithography and optical proximity correction (OPC) for feature sizes of under 20nm, for example. Additionally, performance degradation of the devices themselves as they are scaled also sets limitations. Large leakage current, for example through the gate as caused by GIDL, and increased subthreshold source-drain leakage caused by for example a lower threshold voltages due to voltage scaling, will result in high power consumption even in the off-state. The leakage currents combined with the closely packed transistors also generate excess heat. More power must be put into dispelling the heat, as increased temperature further degrades transistor performance. It is clear that continuing to scale CMOS-based memories is bringing diminishing returns in power reduction, performance, and average cost per gigabyte.

As a result much research focus has been on finding replacement memory technologies that are fast, dense, reliable, and non-volatile. Emerging memory devices include resistive RAM (RRAM) which stores information in changing the resistance of some dielectric material, and phase change memory (PCM) which changes the lattice structure of the material, for example from amorphous to crystalline. This thesis focuses on magnetoresistive RAM (MRAM), which uses the magnetization direction of a material, relative to a fixed direction, to store information. The speed of reading and writing, as well as the low power consumption make it a good candidate for a future ‘universal memory’.

If such an ideal ‘universal memory’ technology can be found, not only will the storage capacity of all devices become much larger, changes even to computing architecture can be pursued. For example, ‘normally-off’ computing is where power is only consumed when the CPU reads or writes to the cache, and such a computer would be able to instantly boot up into the last known state. An even further direction for the evolution of computing is a neuromorphic style which copies the human brain, in having many more devices dedicated to memory than computation. Most information would be stored and retrieved quickly as needed, without much computation which can be energy inefficient. Entirely revolutionizing the current Von Neumann architecture for faster and energy efficient computation could be a possibility if one of the emerging memories can be realized.

## Chapter 1.1: Magnetism, Ferromagnets, and Ferromagnetic Thin Films

This chapter covers the very basics of magnetism, and ferromagnets in bulk and thin film morphology. This knowledge forms the basis of magnetic tunnel junctions and how they operate, which will be introduced in Chapter 1.2. As it would be redundant to cite every basic equation and statement to essentially the same sources, they are listed here in order of level of reference. If an equation or conclusion is not specifically noted to be from a paper, they were taken from one or more of the following sources: lecture notes used during the 2013 and 2014 IEEE Magnetics Society Summer School, *Hitchhiker's Guide to Magnetism* written by Bruce M. Moskowitz [1], and Chapter 20 of *Materials Science and Engineering, an Introduction*, Seventh Edition, written by William D. Callister Jr. [2].

### Section 1.1.1: Magnetism Background

The origin of magnetism in materials originates from the spin of electrons, which gives them angular momentum, and the orbital motion of electrons around atomic nuclei of the material, which gives them orbital angular momentum  $L$  [Nms]. The magnetic moment  $m$  [Am<sup>2</sup>] of a bulk material is a vector parameter intrinsic to it, and is affected by the atomic orbital configuration and arrangement of atoms in the material. The magnetic moment has a magnitude and a direction. It will feel a torque in an external magnetic field  $H$  [A/m]:  $\Gamma = m \times H$ , which is a vector cross product of the magnetic moment and the magnetic field. The total magnetization  $M$  [A/m] of a piece of material is defined as the magnetic moment per unit volume of material:  $M = m/V$ , where  $V$  is the total volume of the material.

The total magnetization of the material is what is referred to when magnets are being talked about. A non-magnetic material is not affected by magnetic fields, and has no magnetization. A magnetic material will have a net magnetization only when an external magnetic field is applied, but not otherwise. Materials fitting this kind of description can be further split into diamagnets and paramagnets, differing only in whether the induced magnetization opposes or aligns in the same direction as the applied magnetic field. A permanent magnet can retain a net magnetization even when not in the presence of an external magnetic field. This kind of material can be split into ferromagnets, anti-ferromagnets, and ferrimagnets. The difference is the alignment of the magnetic moments inside the material.

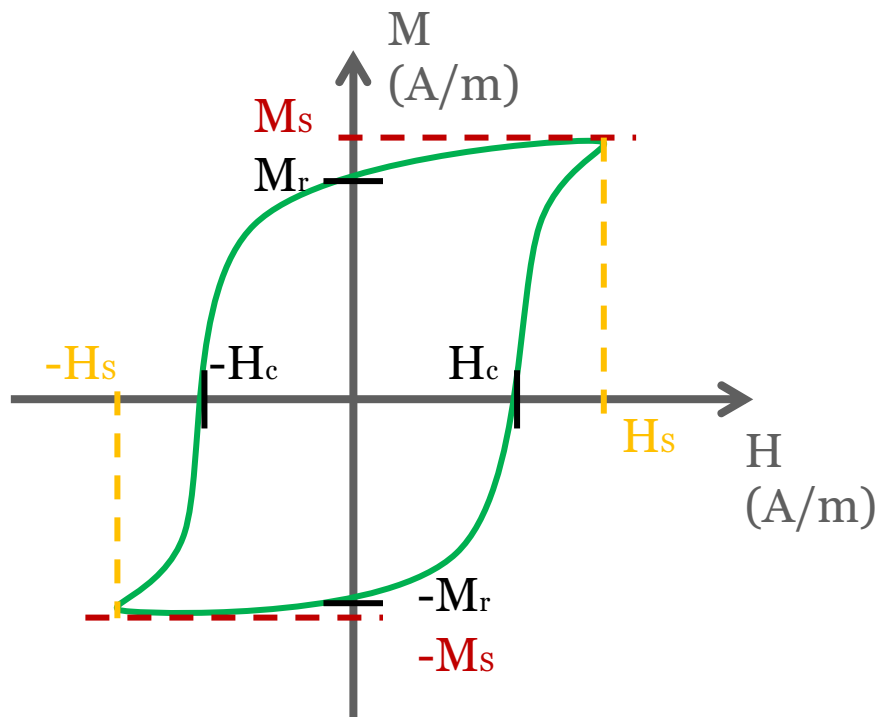
### **Section 1.1.2: Ferromagnets**

The magnetic moments in a ferromagnet all align in the same direction, within the same magnetic domain, due to exchange interactions between different magnetic moments. Different domains can have the magnetization point in a different direction from its neighbors, and they form because it is energetically more favorable to do so for large numbers of atoms. The region between different domains is called a domain wall, and features a smooth progression of magnetic moment direction from one domain to the other.

The magnetization of a bulk ferromagnet at zero applied magnetic field may be composed of many different domains pointing in slightly different directions, some of which can cancel each other out. So even though there is a net magnetization under zero field, it is often not the maximum magnetization that the ferromagnet can achieve. The saturation magnetization,  $M_s$ , describes the maximum magnetization that a ferromagnet can reach after a magnetic field larger or equal to the saturation magnetic field  $H_s$  is applied to the ferromagnet, to align all of the

magnetization of the domains in the same direction as the applied field. These parameters are intrinsic to the ferromagnet, and can be altered by changing the composition or morphology of the material.

The change of the magnetization of a ferromagnet, as it is subject to a magnetic field which is swept between  $\pm H_s$ , is called the magnetization-field (MH) curve of the material, or also as the hysteresis loop. An example curve is shown in Figure 1. Notice that the ferromagnet can have two different remanent magnetization directions  $M_R$  at zero field, depending on which direction the field has been swept from,  $+H_s$  or  $-H_s$ . This hysteresis phenomenon is the basis for using ferromagnets as a memory element, because the information can be stored in the direction of the magnetization.

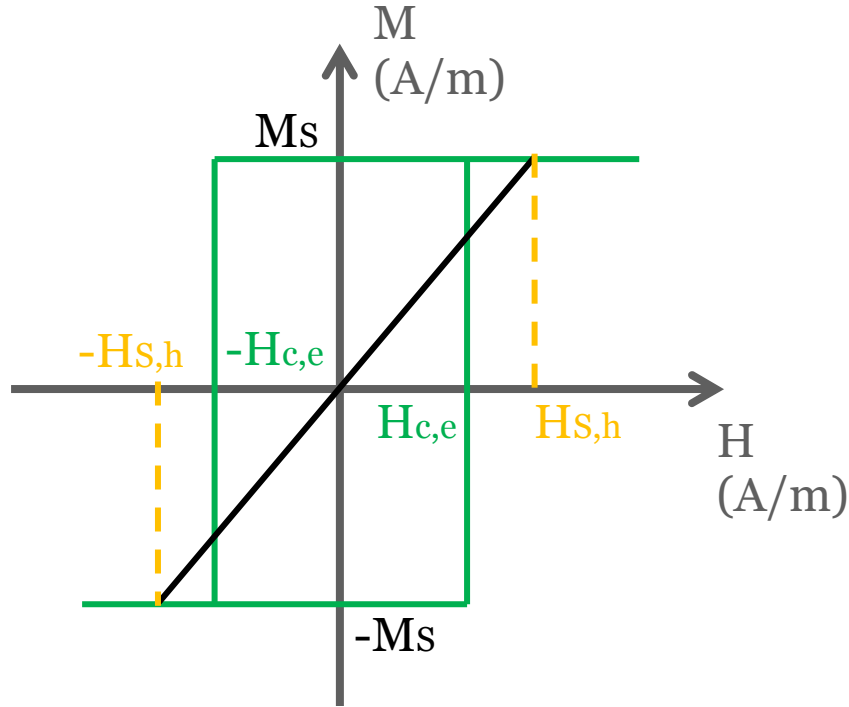


**Figure 1 shows a representative hysteresis curve for a ferromagnet. The parameters of saturation magnetization  $M_s$ , remanent magnetization  $M_r$ , coercivity  $H_c$ , and saturation field  $H_s$  are shown.**



The two fields at which the magnetization is reduced to zero is called the coercivity  $H_C$ . A magnetically soft material will have a smaller coercivity, meaning it is relatively easy to demagnetize a soft material. Conversely, a magnetically hard material will have a larger coercivity, and be harder to demagnetize. The area inside the hysteresis curve is a reflection of the magnetic energy loss per unit volume which the external magnetic field provides, every time the magnet is magnetized from an initial saturation magnetization direction, into the other direction, and back. This energy can be converted into heat, which may cause the temperature of the ferromagnet to rise.

The hysteresis curve of ferromagnets subject to magnetic fields applied in different directions can be different. This is caused by the magnetic moments requiring different amounts of magnetic energy to align in different directions. This phenomenon is called magnetic anisotropy, and is influenced by many things, including the crystalline lattice structure of the ferromagnet, its physical shape, if there is any stress on the material, or if there are any interactions with other materials the ferromagnet is in contact with. These are all different forms of magnetic anisotropy, and contribute to an overall effective magnetic anisotropy of the material. The saturation magnetization is the same for every direction, since that is an intrinsic property of the ferromagnet. However the saturation field can be different for different directions. The easy magnetization axis is defined as the direction along which if a field is applied, the saturation field of the material is small. It is so named because it is easy to saturate the material in this direction. The hard magnetization axis is then the direction along which the saturation field is large. Easy and hard axis hysteresis loops for an ideal ferromagnet is shown in Figure 2, where it can be seen that the saturation field  $H_{S,h}$  for the hard axis loop is larger than  $H_{S,e}$  for the easy axis loop.

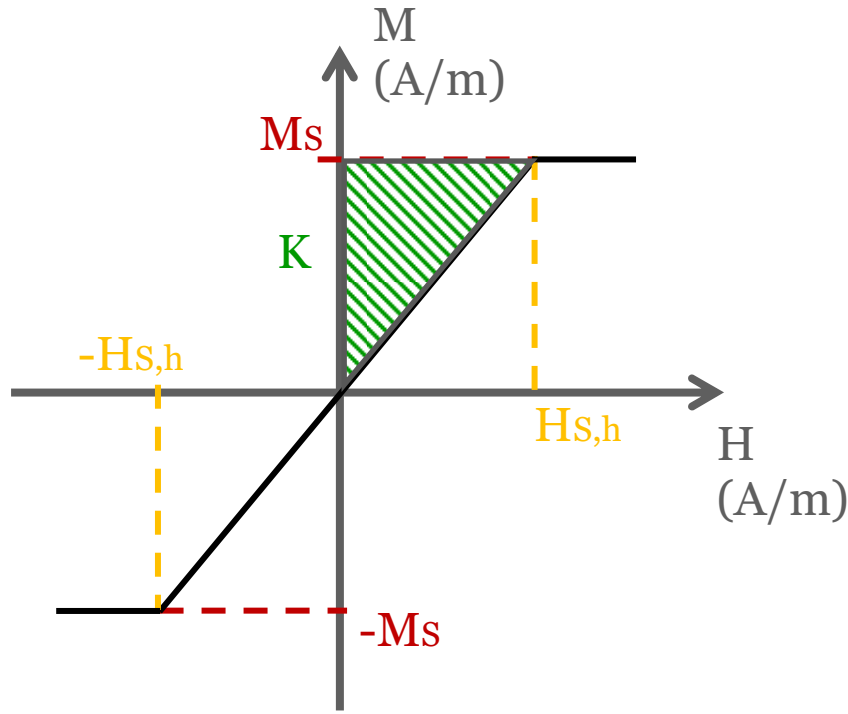


**Figure 2 shows the hard and easy axis hysteresis loops for an ideal ferromagnet. The black line is the hard axis curve, and the green rectangle is the easy axis loop. The saturation fields for the easy and hard axis loops are  $H_{S,e}$  and  $H_{S,h}$  respectively.**

A ferromagnetic material can have one easy axis direction, or many, and the same is true for hard axis directions. Materials with one easy axis are said to have uniaxial anisotropy, and the hard axis is a plane perpendicular to the easy axis. Materials with two easy axes perpendicular to each other have biaxial anisotropy. Three or four easy axes are also possible.

The magnetic anisotropy energy (MAE) of the material is defined as the energy needed to be provided to a magnetic moment in an easy axis direction so that it can align in a hard axis direction [3]. It is the difference between the total anisotropy energies for the two orientations. For aligning the total magnetization of a material from the easy to the hard axis direction, the magnetic anisotropy energy density  $K$  is defined, which is the MAE per unit volume.

On the hard axis hysteresis loop, the magnitude of the magnetic anisotropy energy density is the area of the triangular green shaded area shown in Figure 3, which is the energy per unit volume that the applied field must provide to align the magnetization from an easy axis direction to a hard axis direction. This is to say, starting at zero field, where the magnetization is zero along the hard axis direction, to the saturation field, where the magnetization is fully saturated along the hard axis direction. For an ideal curve such as the one shown, the MAE is simply the area of the shaded triangle, and can be calculated by:  $K = H_{s,h}M_S/2$ .



**Figure 3 shows the calculation of the magnetic anisotropy energy density  $K$  of an ideal ferromagnet, from its hard axis hysteresis loop. It is equal to the area of the green shaded region.**

In uniaxial anisotropy ferromagnets, the energy that the magnetization must acquire to switch from one direction along the easy axis, over the hard plane, to the other easy axis direction, is defined as the energy barrier  $E_B = KV = H_S M_S V / 2$ , where  $V$  is the volume of the ferromagnet. In

ferromagnets with more than one easy or hard axes, there can be more than one energy barrier, for switching to and from different orientations. The energy barrier in this case is still the minimum energy required to make this magnetization direction switch. From the energy barrier equation it is clear that as the ferromagnet volume is decreased, the energy barrier height also decreases, and changing the magnetization direction requires less energy.

When a ferromagnet is at a non-zero ambient temperature, the magnetic moments will experience thermal fluctuations, which will give energy to the magnetic moments. Thermal noise like this is random in direction and amplitude, and is proportional to the temperature. The thermal stability  $\Delta$  of a ferromagnet describes how well the magnetization direction keeps its initial direction, against disturbances from thermal noise:  $\Delta = E_B/(k_B T) = H_S M_S V / (2k_B T)$ . When the temperature increases, the thermal noise will increasingly become more and more comparable to the energy barrier height, and the possibility of a random switch of magnetization direction becomes more likely. Similarly, as the volume of the material decreases, the magnetization direction requires less energy to change, and the thermal stability also decreases.

The statistically average time that the magnetization will take to ‘relax’ from an initial state into another easy axis direction is called the relaxation time. A ferromagnet with a larger thermal stability will have a larger relaxation time, due to the fact that the energy barrier is larger, and the probability that thermal fluctuations will randomly provide large energies is lower. The relaxation time  $t$  can be related to the thermal stability  $\Delta$  using the Néel-Brown model [4] [5]:  $t = \tau_0 \exp(\Delta)$ , where  $\tau_0$  is the attempt time, a parameter that is related to the gyromagnetic resonance frequency of the magnetic moments in a material.

Electrons have an intrinsic spin, which gives them an angular momentum, with a magnitude and direction. The magnetization of ferromagnets can interact with electrons and vice versa, due to them both having magnetic moments which generate magnetic fields. Due to exchange

splitting which displaces the spin sub-bands, electrons with different spin directions have different density of states at the Fermi level inside a ferromagnet. Electrons with spins in the same direction as the ferromagnet magnetization are called the minority spin electrons, because while there are more of them, the density of states is smaller. The majority spin electrons have a spin opposite to the ferromagnet magnetization, but the density of states is larger.

Ferromagnets can interact with a current comprised of electrons with spins in random directions, by ‘spin polarizing’ some of them as they pass through the ferromagnet, causing some of the electrons to point in the same direction as the ferromagnet magnetization direction [6] [7]. This is due to the density of states difference, which causes electrons with parallel spins to pass through the ferromagnet easier than electrons with antiparallel spins. The degree to which a ferromagnet can spin polarize current passing through it is related to the density of states difference between the parallel and antiparallel spins, which is described by the spin polarization  $P$  of the ferromagnet. An extreme case would be a half-metallic ferromagnet, which would have no density of states for the majority spins at the Fermi level, and would have a spin polarization of 1.

The electron spins also act on the ferromagnet magnetization, similar to the law of action and reaction in classical physics. The electron spins will exert a torque on the ferromagnet magnetic moments, and transfer angular momentum to the system [8] [9]. With enough electrons and angular momentum, the magnetization direction can be induced to switch from one easy axis direction to another. Spin-torque transfer (STT) MRAM uses this phenomenon to switch the magnetization direction of a ferromagnet.

### **Section 1.1.3: Ferromagnetic Thin Films**

Ferromagnets are integrated into magnetic tunnel junction devices as thin films, sandwiched between other films which may affect its parameters and behavior [10]. One effect is called interface anisotropy, which also contributes to the effective anisotropy of the ferromagnet in addition to the other bulk anisotropy sources already mentioned. Interface anisotropy arises from the interaction of the ferromagnet atoms with atoms of another material, at the interface of the two materials.

The interface anisotropy contribution can overwhelm the bulk contribution to the total effective anisotropy, causing the easy axis to be perpendicular to the film plane. For bulk materials where interface anisotropy is small, the easy axis is usually in-plane. The interface anisotropy contribution is inversely proportional to the film thickness:  $K_{eff} = K_v + K_i/t$ , where  $t$  is the thickness of the ferromagnetic film,  $K_{eff}$  is the total effective magnetic anisotropy energy density of the material,  $K_v$  is the bulk volume contribution, and  $K_i$  is the interface contribution. The bulk contribution is negative, so that a thin film with an in-plane easy axis has negative effective anisotropy energy. The interface contribution is positive, so a thin film with perpendicular easy axis has positive  $K_{eff}$ .

## **Chapter 1.2: Magnetic Tunnel Junctions**

In this chapter a general overview of the magnetic tunnel junction device is presented, together with some important performance parameters.

### **Section 1.2.1: Physical structure and operation**

The core of a magnetic tunnel junction (MTJ) device is physically comprised of two ferromagnetic layers sandwiching an insulating layer. The relative directions of the magnetization of the two ferromagnetic layers store the information. The orientation can be in the same direction, called the parallel (P) state of the device, or it can be in the opposite direction, called the anti-parallel (AP) state. Usually one layer is designated the reference, or fixed layer, and during normal operation the magnetization direction of this layer does not change. The other layer is called the free layer, because this layer is the one that changes direction to alter the device state between P and AP.

The device state is converted to electrical resistivity through the tunneling magnetoresistance (TMR) effect [6] [7] [11] [12], which is related to the ability of ferromagnets to be spin polarizers. Assuming identical ferromagnets sandwiching an insulator, in the parallel state the density of states for the majority and minority spins for each layer will be the same, leading to large conduction and low electrical resistance. In the antiparallel state the majority and minority spins for each layer is directly opposite, so for each spin direction there is always one layer with less density of states, leading to small conduction and large electrical resistance. Thus reading the state of an MTJ is as easy as reading the electrical resistance of the device, and the relative orientations of the fixed and free layer magnetization directions can be known.

Writing information to the device means changing the magnetization direction of the free layer, from one direction of the easy axis, to the other. To do this, sufficient energy must be provided to the magnetization to overcome the energy barrier between the easy axis directions. To make switching easier, methods can be found to lower the energy barrier before writing, then restoring it after writing is done, to protect the information against thermal agitation.

### **Section 1.2.2: Device Parameters**

The most basic device parameter is the P and AP resistance values. From these two the tunneling magnetoresistance ratio (TMR) can be calculated:  $TMR = (R_{AP} - R_P)/R_P = (G_P - G_{AP})/G_{AP}$ , where R and G stand for electrical resistance and conductance, respectively, in the P and AP states. The resistance of the MTJ device has an impact on the RCL delay of any control circuits that it will be connected to. Since smaller area devices with otherwise identical structures will have larger resistance, a uniform way of isolating the resistance of the device structure independent of device area is the Resistance-Area (RA) product, which is the product of the resistance and the device area, and is usually in units of  $\Omega \cdot \mu\text{m}^2$ .

The fixed and free layers must have the same direction of easy axis, to achieve maximum TMR for the device. This direction can be in the same plane as the free layer film, or perpendicular to it. The magnetic anisotropy energy density and the energy barrier between the easy axis directions are important parameters for MTJ devices. To ensure that the fixed layer magnetization direction remains constant, the energy barrier must be extremely large to prevent switching caused by thermal noise or any disturbances from switching the free layer. Secondly and more importantly, the thermal stability of the device, or more generally its data retention ability, is decided entirely by the thermal stability of the free layer. A thermally stable device is



necessary for long term data retention. However a large energy barrier will also require more energy to write to the device. As devices are scaled, the volume of the free layer decreases and the thermal stability of the device will decrease, which is a problem for long-term electronic storage applications.

The coercivity of the MTJ device is really the coercivity of the free layer, since the fixed layer is assumed to hold a constant direction of magnetization during normal operation. A larger coercivity reflects a larger  $K_{\text{eff}}$ , which means the free layer will have a larger energy barrier. Due to the free layer being in a stack, and subject to dipole stray fields especially from the fixed layer close to it, the hysteresis loop is often offset from zero field by an amount  $H_{\text{offset}}$ , which is necessary to counteract the stray fields on the free layer.

The resistance, TMR, coercivity  $H_C$  and offset field  $H_{\text{offset}}$  can be measured for a device by measuring the resistance-field (RH) plot. The easy axis RH loop is measured by monitoring the device resistance as a magnetic field along the easy axis direction is swept. The hard axis RH loop is the same except a magnetic field along the hard axis direction is applied. From the hard axis RH loop the MAE of the free layer can be calculated, if the free layer can be completely saturated in the hard axis direction. The P and AP resistances can be assumed to be the resistance of the free layer in each easy axis saturation magnetization direction, relative to the fixed layer. For magnetization directions of the free layer which is not fully parallel or antiparallel to the fixed layer, the resistance of the device takes on intermediate values between  $R_P$  and  $R_{AP}$  which are proportional to the angle  $\theta$  between the free and fixed layer magnetization directions:  $G(\theta) = G_S[1 + P_F^2 \cos(\theta)]$ , where  $G_S$  is a constant representing the mean surface conductance,  $P_F$  is the effective spin polarization of the tunneling electrons [13]. Thus, it is possible to deduce the parameters of the free layer in the stack with information attained from RH loops.

The switching mechanism of the device determines its switching speed, energy, and success rate. Listed in order of increasing switching speed, some of the methods under study now to switch the magnetization include thermal assisted switching, STT switching, and precessional switching. Thermal assisted switching uses thermal noise together with a lowered energy barrier, so that the energy from thermal noise can overcome the lowered energy barrier and switch the magnetization direction. With STT switching, a large current is passed through the device to transfer angular momentum to the free layer, to switch its direction. Precessional switching makes the magnetization precess around a field perpendicular to it, for half of a precessional period, before stopping the precession.

The switching energy of the thermal assisted method is used to lower the energy barrier height, using whatever method. For STT, it is the amount of angular momentum which must be transferred, and is described by the switching efficiency. Precessional switching requires energy to destroy the old easy axis, so that the magnetization can precess, for example around an effective field generated by the other anisotropy terms.

For precessional switching, one way to destroy the old easy axis is to use the voltage-controlled magnetic anisotropy (VCMA) effect, in which a voltage applied across the insulator barrier will change the perpendicular magnetic anisotropy (PMA) of the ferromagnetic layers [14] [15] [16] [17] [18]. This is either due to accumulation or depletion of electrons in select orbitals of ferromagnetic atoms along the interface, or through Rashba interaction. The degree of control that electric field in the insulator has on the PMA of the free layer is described by the VCMA coefficient  $\xi$  [fJ/Vm], defined as the amount of interface magnetic anisotropy energy density change per change in electric field:  $\xi = \Delta K_i / \Delta E = \Delta K_i / (\Delta V / t)$ , where  $K_i$  is the interface magnetic anisotropy energy density, and  $V$  here is the applied voltage across an insulator of thickness  $t$  [19].

The switching rate describes how reliable the switching method is at switching the magnetization direction, when a write attempt is made to the device: *switching rate* = *successful write attempts*/*total write attempts*. The write error rate is complementary to the switching rate: *write error rate* = *failed write attempts*/*total write attempts*.

### **Section 1.2.3: Magnetization Switching**

The easiest way to switch the magnetization of the free layer is to apply an external magnetic field. However, the difficulty of generating large but localized magnetic fields, using current passed through a cylindrical coil, given by  $H = \frac{NI}{L}$  where  $N$  is the number of coil turns,  $I$  is the current, and  $L$  is the length of the cylindrical coil, poses a hard limit on the ultimate device density which uses this kind of magnetization switching.

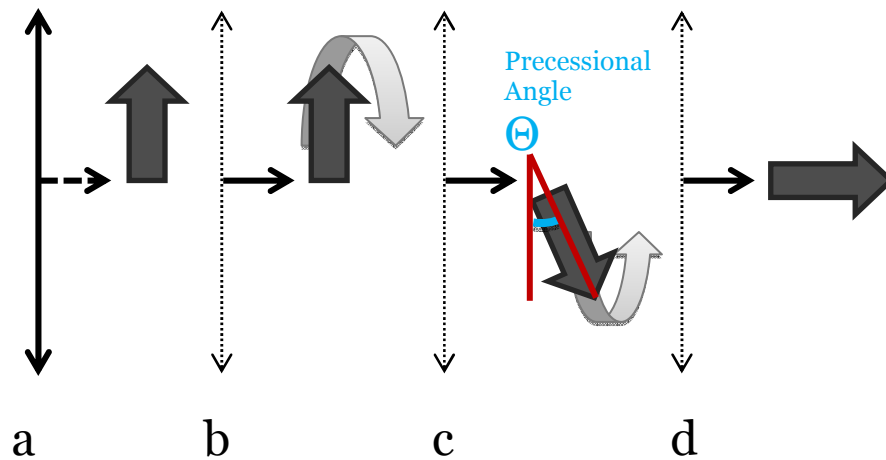
Modern circuits use electric currents to transfer information, and it was demonstrated that spin-torque transfer (STT) could be used to change the magnetization orientation of the free layer [20]. The principle is that the electron spin from conduction electrons can transfer their angular momentum to the magnetic moments of a ferromagnet, and also vice versa. However power consumption, speed, and scaling difficulties are present in this method. A certain number of electrons are needed to switch the magnetization direction, meaning that the critical switching current is large, posing problems for power consumption and the lifetime of the device. To achieve fast switching below 10ns, even larger currents must be applied. This is because as the current pulse length is decreased to below 10ns, the switching mechanism changes from thermal activation to a precessional model, which requires a critical switching current that increases exponentially as the pulse length is scaled [21] [22].

The power consumption of an STT device is proportional to the applied voltage and switching current amplitude, which can further be related to the device resistance. Scaling the device area will cause the resistance to increase, slowing down the ultimate speed of STT devices in a memory circuit. GHz speed operation will also require methods to decrease the switching current amplitude at short current lengths for these smaller devices.

In addition to all those issues against fast operation for STT-switched devices, spin torque also has an incubation time  $\tau_i$  between the application of the current pulse, and the start of the magnetization switching [23]. It is dependent on the applied current  $I$ :  $\tau_i = \tau_0 \exp \left[ \Delta \left( 1 - \frac{I}{I_{c0}} \right) \right] = \tau_0 \exp \left[ \frac{E_b}{k_B T} \left( 1 - \frac{I}{I_{c0}} \right) \right]$ , and is a reflection of the time it takes for the magnetization to climb the energy barrier  $E_b$  [24]. Thus additional challenges arise of balancing high device thermal stability with fast operation.

A third method was found to switch the magnetization, whereby applying an electric field at the interface of the ferromagnet and an insulator, the interface anisotropy would change [15] [16] [18]. This phenomenon is called the voltage-controlled magnetic anisotropy (VCMA) effect. For the CoFeB/MgO interface, decreasing the electron concentration at the interface will increase PMA, and accumulating electrons will decrease PMA [25]. Methods were designed to use an electric field to lower the energy barrier between perpendicular easy axis directions, then use STT, thermal, or precessional methods to easily switch the device with less energy [26]. Thermal switching [27] is the process where the perpendicular anisotropy is reduced to low enough, so that thermal fluctuations have a chance of nudging the magnetization out of one state and into the other. This is a statistical process which is proportional to the thermal energy in the system. The attempt time is on the order of 1ns, but the strength and direction is random, so the effective thermal switching time is around the range of 10ns.

Besides thermal assisted switching, a second method using VCMA is called precessional switching [28], and utilizes the fact that the magnetization will precess around a field which is applied perpendicular to its original direction, because the torque  $\vec{\Gamma}$  exerted on magnetic moment  $\vec{m}$  by a field  $\vec{H}$  is  $\vec{\Gamma} = \vec{m} \times \vec{H}$ . It is possible to destroy the perpendicular anisotropy and create an in-plane effective field, which will cause the originally out of plane magnetization to precess around the in-plane field. This process is illustrated in Figure 4a and Figure 4b for a perpendicular uniaxial easy axis ferromagnet. If there is no damping, the precessional angle  $\theta$ , defined as the angle between the magnetization direction and the perpendicular easy axis direction, would always be zero. The magnetization will continue precessing forever, passing through the original perpendicular axis every half of the precessional period. Reintroducing the perpendicular anisotropy will cause the magnetization to try to align to an out-of-plane direction closest to it, again through precession. If the reintroduction is timed correctly, one can cause an originally ‘up’ magnetization to precess to the ‘down’ direction, or vice-versa. However, Gilbert damping [29] [30] [31] [32] exists in real systems, and the damping factor  $\alpha$  is anywhere from 0.01 to 0.3, which causes the magnetization to slowly lose energy to the lattice, and eventually to align with the in-plane effective field, as shown in Figure 4d.



**Figure 4 illustrates part of the precessional switching process. The thin arrows are perpendicular and in-plane easy axis directions, respectively. The thick arrow is**

**the magnetization vector. In a), the perpendicular magnetic anisotropy (PMA) is dominant, so the easy axis is in the perpendicular direction. In b), the PMA has been destroyed by an applied voltage, so the in-plane magnetic anisotropy dominates. The magnetization starts to precess due to torque. In c), the magnetization has precessed for half of a period. Due to damping the magnetization loses energy to the lattice and the precessional angle  $\theta$  starts to increase from zero. If the PMA is reintroduced at this step, the magnetization has a large chance of aligning to the ‘down’ direction of the easy axis, completing a successful switch from the ‘up’ direction. If the magnetization is allowed to precess until it loses all of its energy, it will align with the in-plane axis, as shown in d).**

The precessional period is inversely proportional to the magnitude of the in-plane effective field [33], so a larger in-plane field will cause faster precession.

$$t_{precess} = \frac{2\pi(1 + \alpha^2)}{\gamma H_{ext}}$$

Where  $\alpha$  is the Gilbert damping parameter, and  $\gamma$  is the gyromagnetic ratio.

Magnetization dynamics can be modeled using the zero temperature Landau-Lifshitz-Gilbert (LLG) equation to gain further insight [34] [35] [36]:

$$\frac{d\vec{m}}{dt} = -\gamma\vec{m} \times (\vec{H}_{eff} + \vec{h}_T) + \alpha\vec{m} \times \frac{d\vec{m}}{dt}$$

Here the thermal noise is incorporated by modeling it as a random vector field  $h_T$  with zero mean and a standard deviation of  $\sqrt{\frac{2\alpha k_B T}{\gamma \mu_0 M_s V \delta t}}$ .  $\vec{m}$  is the magnetic moment vector normalized by the saturation magnetization,  $H_{eff}$  is the total effective field which is the vector sum of the anisotropy field and externally applied fields.

The Fokker-Planck equation [4] [5] can also be used to study the effect of thermal noise on magnetization switching, and the thermal noise is similarly modeled as a random field with a Gaussian distribution. This approach calculates the time dependent probability density

distribution of the magnetization after some applied pulse, and can be used to simulate switching probabilities [33].

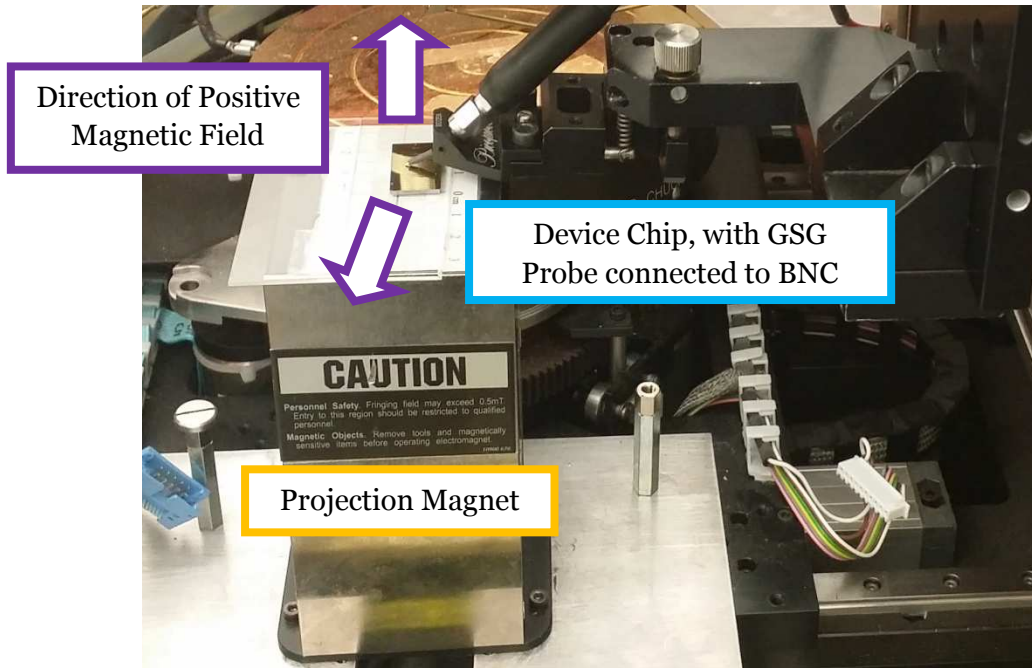
## **Chapter 2: Experimental Setup and Methodology**

This section presents the hardware experimental setup for characterizing MTJ devices, and the methodology for doing so. Basic characterization includes the measurement of RH loops, estimation of the energy barrier, and the calculation of the VCMA coefficient. Also, the setup for quickly writing to the device and reading the state is described, which is the basis for switching voltage and write error rate experiments. All experimental equipment is controlled through the LabVIEW program, with commands being sent through GPIB.

### **Chapter 2.1: RH Loops and Dwell Time**

A single setup can be used to measure both RH loops and the dwell time. A projection magnet (Magnet GMW, Model 5201) was used to provide the external magnetic field, and a Keithley 2612 Sourcemeter to monitor the device resistance as the field is swept. The device is placed directly on top of the magnet, as shown in Figure 5, and the angle of the field can be controlled by changing the position of the device on the magnet. The magnetic field magnitude and angle were calibrated using a gauss meter placed directly on top of the magnet, where the devices would be during operation. For this thesis, the convention of magnetic field sign is as follows: a perpendicular magnetic field pointing up from the magnet is defined as positive out-of-plane field, and positive in plane field is the direction pointing toward the use of the probestation, when facing the magnet. This is also shown in Figure 5 with purple arrows. When an angle is mentioned in the experimental results section in Chapter 3, it refers to the angle between the total magnetic field and the out-of plane, vertical direction.





**Figure 5 shows the setup for the projection magnet, and the definition of the positive direction of the magnetic field: up from the magnet for out-of plane fields, pointing to the probe station user for in-plane fields. The sample is placed directly on the magnet, and the angle of the total magnetic field applied to the device can be controlled by moving the device on the magnet. The connection between the devices and the rest of the measurement circuit is made through point probes (not shown) for DC measurements, or a Picoprobe GSG microwave RF probe, connected through a BNC cable, for high frequency write pulses.**

Once the MTJ device is connected to the circuit through either point probes or a Picoprobe GSG microwave RF probe, the RH loop measurement can begin. The magnet is set to bias the device under a certain magnetic field, and a measurement of the resistance is taken after a certain amount of wait time, usually 350ms to 500ms or more. Then magnet is set to the next bias field, typically 10Oe or 20Oe larger or smaller, and the resistance taking procedure is repeated. The wait time of at least 350ms is to give the magnetic field a chance to settle to its final value after being changed. An average of 3 RH loops are typically measured to compensate for the statistical nature of the relaxation of the ferromagnet under an external field. This yields a more reliable value for the coercivity of the free layer, because the coercivity of each loop is not guaranteed to

be the same. A smaller wait time would yield larger loops, because the device would appear to switch at bias fields where the dwell time is smaller, and a larger wait time would yield smaller loops, for the same reason. For all the RH loops shown here, 350ms wait time is used, and the coercivity is taken as half of the average of the fields where the device switches from AP to P and P to AP.

The dwell time is measured by first setting the device in a certain state, for example the P state, then applying an external magnetic field near the edge of the RH loop where the device switches from P to AP. The time necessary for the device to relax to the AP state is taken to be the dwell time at that external bias magnetic field. 50 dwell times are measured for each bias field in this way, and the average is taken. At least three, usually four to seven bias fields near the corners of the coercivity loop are measured. These dwell times corresponding to different bias fields can then be fitted to the exponential equation that the Néel-Brown model [4] describes, to estimate the energy barrier height for different switching directions, at different bias fields.

$$t_{dwell} = \tau_0 \exp\left(\frac{E_b}{k_B T}\right)$$

From RH loops it is possible to calculate the saturation magnetization and field. From these numbers the perpendicular magnetic anisotropy energy can be calculated. If PMA energy is calculated for several different voltages, the VCMA coefficient of the fixed and free layers can be estimated. The prerequisite is that the free layer of a suitable device is able to be saturated in the hard axis direction, while the fixed layer is assumed to be relatively constant. These two requirements are necessary for an accurate conversion between RH loops and magnetization-field (MH) loops.

Once an RH loop has been measured for a certain voltage, it can be converted to a MH curve using the linear relationship between the conductance of the MTJ and the angle between the

fixed and free layer magnetizations. The MH curve should be normalized by  $M_s$ , so that it is between  $\pm 1$ . Then by integrating the area formed between the zero magnetization and the saturation magnetization, together with the zero field (derived using total applied field minus the offset field) to the saturation field.

This is done for several different voltages, to get a series of PMA energies of the free layer at each voltage. If the insulator barrier thickness is known, the electric field across the insulator can be calculated by dividing the voltage by the thickness. The VCMA coefficient is then the change in perpendicular magnetic anisotropy energy per change in electric field across the insulator.

The properties of the fixed layer can be investigated in a similar procedure, however special care must be taken to ensure that the free layer does not rotate during testing. This can be done for example by choosing a device with in-plane free layer and out of plane fixed layer, then applying an in-plane field to saturate the fixed layer in two directions.

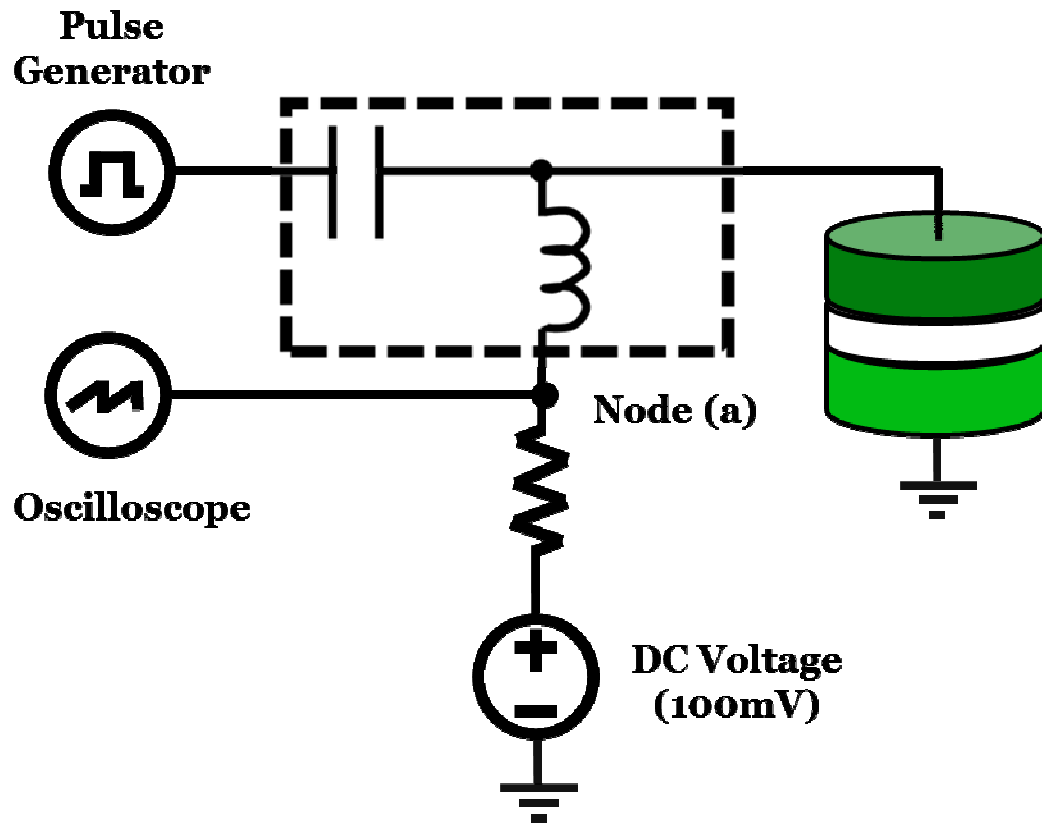
## Chapter 2.2: Write Error Rates

The setup we devised for conducting write error rate experiments is able to conduct write and read functions consecutively and at high speed to a device. This speed is necessary to conduct large numbers of switching experiments in a reasonable timeframe. Many trials are needed to characterize low write error rates: from statistical sampling theory, in random sampling the margin of error is smaller as the sampling size is increased. For switching experiments, the success or failure of each write trial at a certain set of variables is just one sample of the actual switching rate, so the more write trials that are conducted, the smaller the sampling error there is regarding the measured switching rate, for the device at a certain set of variables. For testing write error rates of  $10^{-3}$  and below, altogether more than  $10^6$  trials must be run on the device, under different field and pulse conditions to find the optimum point.

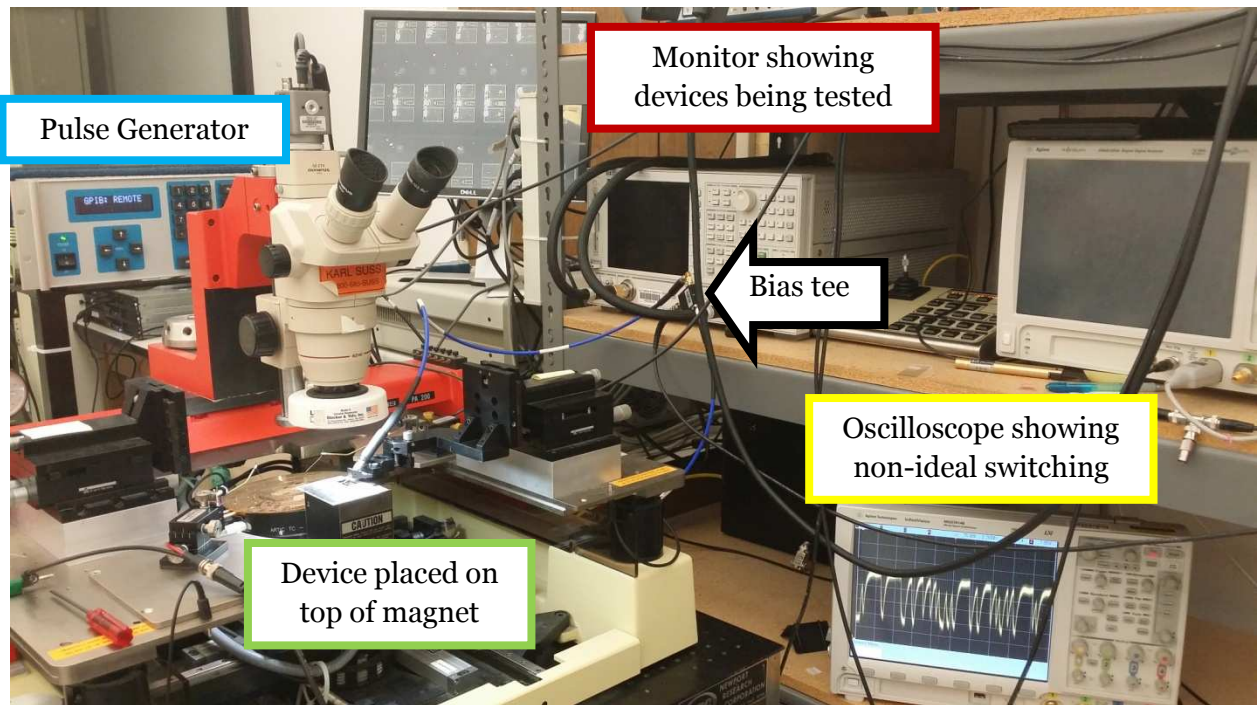
The Picosecond 10,070 pulse generator was used to send write pulses at 100KHz (a period of 10 $\mu$ s), with calibrated pulsewidths between 0.07ns to 9.8ns, and a rise and fall time on average of 120ps and 180ps respectively. The pulse generator output has a -3dB attenuator installed to decrease the amplitude of any frequencies reflected into the output of the pulse generator, which is very sensitive. Due to impedance mismatch at the MTJ, when the attenuated pulse first reaches the device, the amplitude is effectively doubled, so that the MTJ feels approximately the same voltage amplitude as the pulse generator sends. Of course the real amplitude has been calibrated using a wide bandwidth oscilloscope with high channel impedance.

To read the MTJ state, a sourcemeter would take around 10ms through GPIB. Compared with the fastest possible trial period of 10 $\mu$ s, this would become the main bottleneck. So instead we decided to use an oscilloscope to record the voltage across the MTJ which is in series with a fixed resistor, forming a voltage divider. Figure 6 shows a schematic of the circuit. By applying a

100mV DC voltage across the voltage divider, and connecting the oscilloscope channel to Node (a) between the resistor and the MTJ, the MTJ state changes can be converted into a voltage waveform on the oscilloscope. A picture of the physical setup is shown in Figure 7, with the oscilloscope and bias tee labeled.

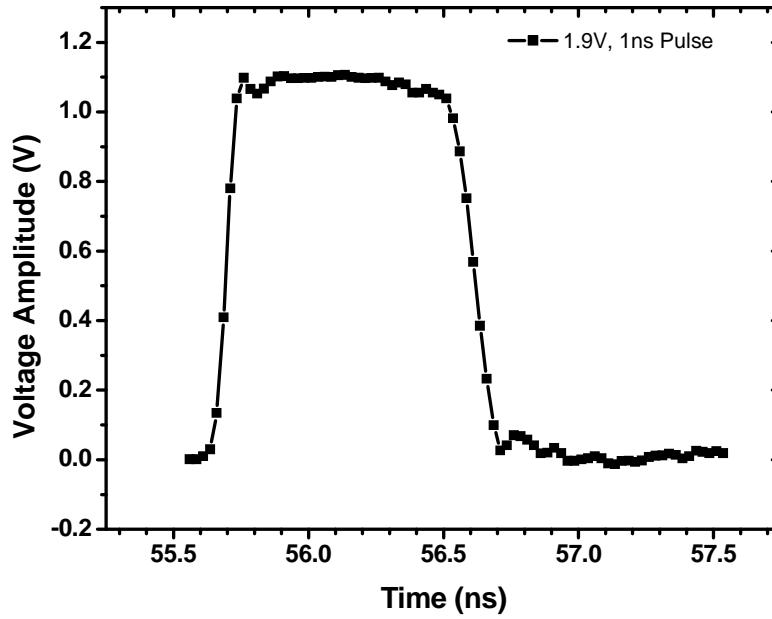


**Figure 6 showing the schematic of the write error rate setup. Node (a) of the voltage divider which is formed by the fixed resistor and the MTJ is connected to the oscilloscope. The pulse generator sends high frequency pulses through the RF arm of the bias tee, delineated in dotted lines, to the MTJ on the right side of the figure.**

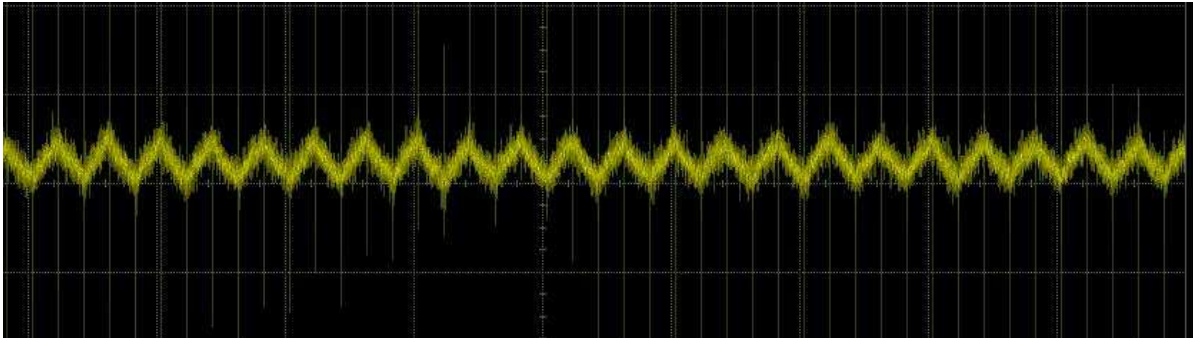


**Figure 7 shows the setup for the write error rate measurement. The GSG probe must be used because the write pulses have frequency components above 10GHz.**

Figure 8a shows the shape of the pulse sent from the pulse generator, and 8b shows the voltage at Node (a), as displayed on the oscilloscope. For ideal 100% switching at every write pulse, the oscilloscope waveform would be a square wave, alternating between the voltages that the voltage divider gives for the P and AP states of the MTJ. However the circuit has RCL components that add a time constant which turns the waveform into the saw-tooth wave seen in Figure 8b. The thin spikes of pulses at each point of the saw-tooth wave are low frequencies of the write pulse which were reflected back from the MTJ through the DC arm of the bias tee.



a)



b)

**Figure 8a)** shows the pulse shape as seen on the oscilloscope, for a nominal 1ns pulse at 1.9V amplitude. The pulse shape looks close to ideal, for long pulsewidths such as 1ns. For shorter pulsewidths of less than 0.3ns the maximum amplitude begins to decrease from the nominal amplitude, due to rise/fall time limitations. **Figure 2b)** shows a section of ideal switching waveform captured by the oscilloscope. It is not a square wave due to the RCL components in the circuit. The x-axis of both figures is time, and the y-axis is voltage amplitude. Every peak of the sawtooth waveform is the MTJ switching states. The vertical lines at the peaks are low frequency components of the write pulse leaking through the inductor of the bias tee.

The DC voltage and high-frequency pulses are combined by a bias tee, shown by a dotted rectangle in Figure 6, which unfortunately also introduces some CL components into the circuit.

Thus the choice of bias tee is also a consideration: the high frequency cutoff must be high

enough to pass at least the first two harmonics of the shortest pulses we want to send (around 0.1ns). We have been using 26.5GHz. However the inductor, which determines the low frequency cutoff, should be small so that the RL constant is not too large, but at the same time be large enough to still pass the longest pulsewidths (~10ns) on the RF side. The bias tee we use for measurements is a Picosecond Pulse Labs Model 5541A Bias Tee, shown in Figure 7.

In using the voltage divider method together with the oscilloscope, the device changing states has been converted into voltage signals on the oscilloscope. This oscilloscope data is further processed to count the switching events and generate the switching probability and write error rate. A separate C program was written for this purpose.

For the oscilloscope, at first we used an Agilent MSO 7014B Mixed Signal Oscilloscope with a memory depth of 8M points, a maximum sampling rate of 2G samples/s, and a bandwidth of 100MHz. Later we used the Agilent DSA91204A, which has a deeper memory depth per channel (50M points), but more importantly the ability to run Matlab script directly on the data in the deep memory of the scope, eliminating the major speed bottleneck of loading the data onto computer RAM. This more powerful oscilloscope sped up the data acquisition by more than 100 times, to ~2secs for a data point containing 10K trials.

In addition to investigating low write error rates, this setup was also used to conduct experiments for switching voltage as a function of device area. The switching voltage was defined as the smallest voltage amplitude at which the switching probability of the device for one direction is over 50%, for any pulse width. The magnetic field applied is the calculated field at which the energy barrier heights for the P and AP directions are the same, as estimated from the dwell times measured at the edge of the coercivity loop.

However in real applications the current through the device may affect offset the hysteresis loop, by contributing significant amounts of angular momentum to the free layer magnetization. This



effect is generally more pronounced for devices with smaller resistances, simply due to Ohm's law. Due to this, the equal energy barrier field measured for 100mV is usually offset by a few tens of Oersteds, from the magnetic field where the energy barrier is the same for both directions as switching voltages of between 1V to 3V are applied. This is indicated by a balanced switching rate from the P to AP, and AP to P directions.

Due to the effect that the current through the device has on the free layer, including STT effects, the switching rate at the equal energy barrier field measured at 100mV usually is very bad for one direction, but very good for another. The switching rate is then defined as the lowest voltage amplitude for which at least 50% switching is attained for the direction with bad switching.

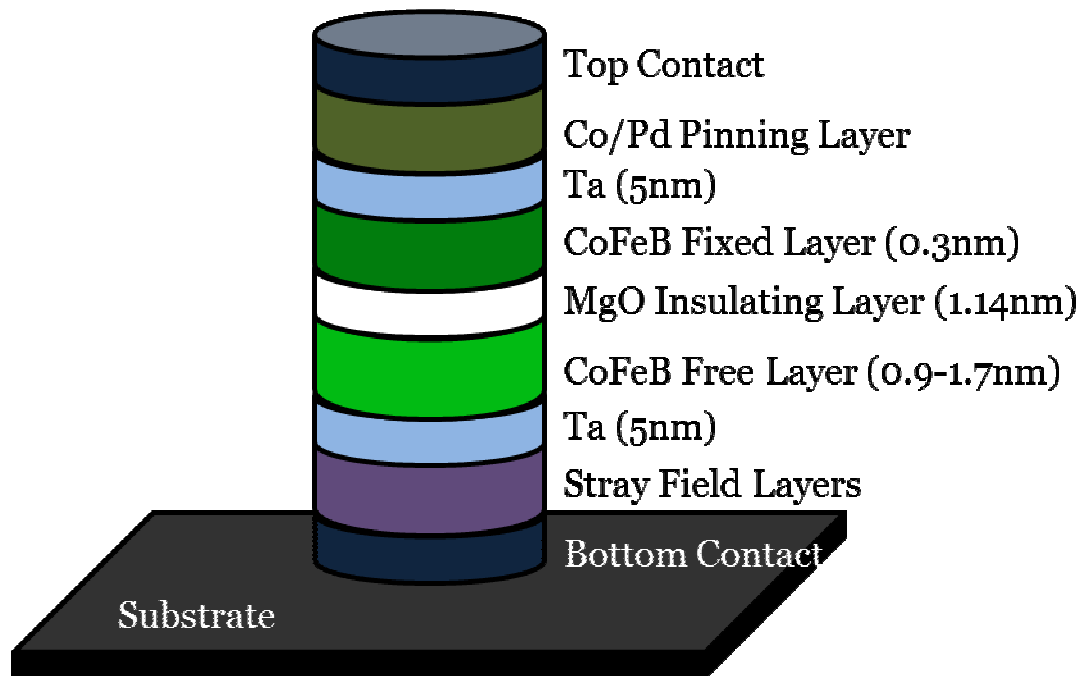
Endurance tests used a modified of this setup, just with the pulse generator and the sourcemeter. The pulse generator was set to run at 100KHz, and a timer in the LabVIEW program estimates the total number of trials by recording the amount of time the pulse generator was running. The sourcemeter is used to monitor the device resistance so that the LabVIEW program can be stopped in the event that the device shorted or opened. At the trial frequency of 100KHz,  $10^{10}$  trials can be reached in 27.7 hours, and  $10^{11}$  trials in 11.5 days of continuous testing.

## **Chapter 3: Experimental Results and Discussion**

This chapter includes the experimental measurement results of two different device structures, one with tantalum seed layer, and one with hafnium seed layer. The basic characterization results including resistance, TMR, and coercivity across the wafer is presented. Switching voltage scaling, VCMA coefficient, and write error rate results are also presented where available and discussed with the help of theoretical analysis.

### **Chapter 3.1: Tantalum Seed Layer Devices**

Tantalum seed layers close to the free layer has been shown to increase the TMR of the device, so devices with Ta layers were fabricated. The stack structure is shown in Figure 9. Positive voltage is defined as being applied at the top contact, with the bottom contact grounded. The pinning layer on top of the fixed layer is used to provide a dipole field on the magnetization of the fixed layer, shifting the hysteresis loop and making it harder to switch during normal operation. The 5nm Ta layers next to the fixed and free layers are to increase the perpendicular magnetic anisotropy of the ferromagnet layers, by absorbing some of the oxygen during annealing. These devices feature a stray field layer below the MTJ, the purpose of which was to provide an in-plane field for the magnetization to precess around. However in practice the field from this layer was too small to achieve uniform switching, so an external field was necessary during testing to help precession. This is why some of the results presented here will have the magnetic field at an angle to the perpendicular direction, with an in-plane component.

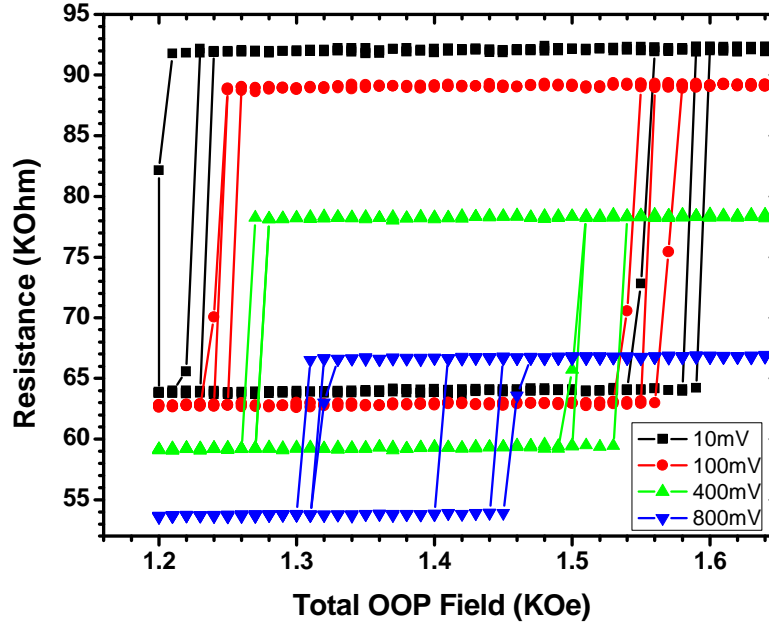


**Figure 9 shows the device stack structure of the Ta seed layer devices. Notice the wedge for the CoFeB free layer thickness across the wafer, which allows optimization of the free layer thickness for best performance. A stray field layer is also incorporated, aiming to provide an in-plane stray field on the free layer for it to precess around.**

Across the entire wafer there are two perpendicular wedges, one for the free layer thickness, and the second for one of the CoFeB layers in the stray field stack. The wedge allows optimization of the free layer thickness, for a suitable perpendicular magnetic anisotropy. Because the transition thickness was around 1.75nm for this stack, for our experiments we used a free layer thickness of between 1.1nm to 1.6nm, for a good range of perpendicular anisotropy that produced a thermally stable free layer, but did not require too much voltage to decrease. Devices in the same column have the same device size and the same free layer thickness. Devices in the same row have the same stray field layer CoFeB layer thickness. The MgO thickness is nominally 1.14nm across the whole wafer.

### Section 3.1.1: General Device Parameters

Representative RH loops conducted at different applied voltages for a 60nm diameter device with a nominal free layer thickness of 1.117nm is shown in Figure 10 below.



**Figure 10 shows RH loops at different applied voltages for a 60nm diameter Ta seed layer device with nominal free layer thickness of 1.117nm. The VCMA effect is apparent, as is the bias voltage dependence of the MTJ resistance. The TMR, coercivity, and offset field parameters for this device can be extracted from this plot.**

The P resistance is around 64 KΩ, and together with the nominal device diameter of 60nm yields a RA of around 181 Ω·μm<sup>2</sup>. The AP resistance is around 92 KΩ, which gives a tunneling magnetoresistance ratio of  $TMR = (R_{AP} - R_P)/R_P = 43.75\%$ , for a bias voltage of 10mV.

The decrease in P and AP state resistivity, and the resulting TMR of the device, shows a dependence of the resistance on bias voltage. Many theories have been proposed to explain and

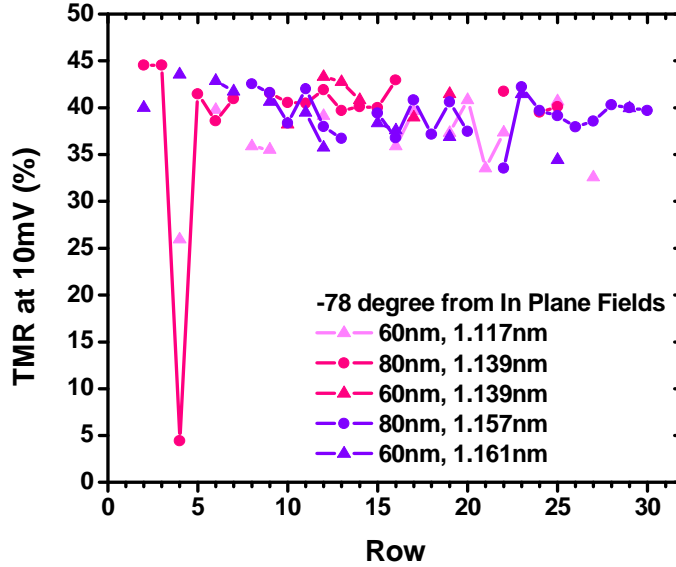
model this phenomenon [37] [38] [39], including spin excitation [40] or magnon excitation [41] at the interface.

The VCMA effect can be seen in the decrease of coercivity at higher applied fields, which corresponds to a decrease of perpendicular magnetic anisotropy with the accumulation of electrons at the free layer interface with MgO, consistent with previous reports [25]. The coercivity at 10mV is quite large, around 170 Oe. This implies that the device has a lot of perpendicular magnetic anisotropy, which is to be expected for thinner free layer devices. The offset field is around 1400 Oe when 10mV is applied, while it is slightly lower for larger applied voltages, due to the increased current flowing through the device, providing spin-torque effects.

Using the same method as above for other devices in the region of the suitable free layer thickness, the average measured TMR is 40%, with minimums at 35% and maximums approaching 45%. A plot is shown in Figure 11. The TMR is independent of device size and free layer thickness, for these devices. It seems to drop off as the row number increases, in which direction the stray field layer CoFeB has nominally decreased from 1.289nm to 1.209nm. It is possible that the thinner stray field layer which applies larger in-plane dipole fields on the free layer, tilting the magnetization slightly out of perpendicular, so that the maximum TMR is not measured. Another reason could be due to differences in the free layer interface due to fabrication, for example if the sputtering target was at an angle.

The distribution of TMR could be attributed to fabrication variations, for example sidewall residue left on the device which could add a large constant resistance in parallel with the MTJ stack, different for every device, which would yield slightly different TMR for essentially the same MTJ.

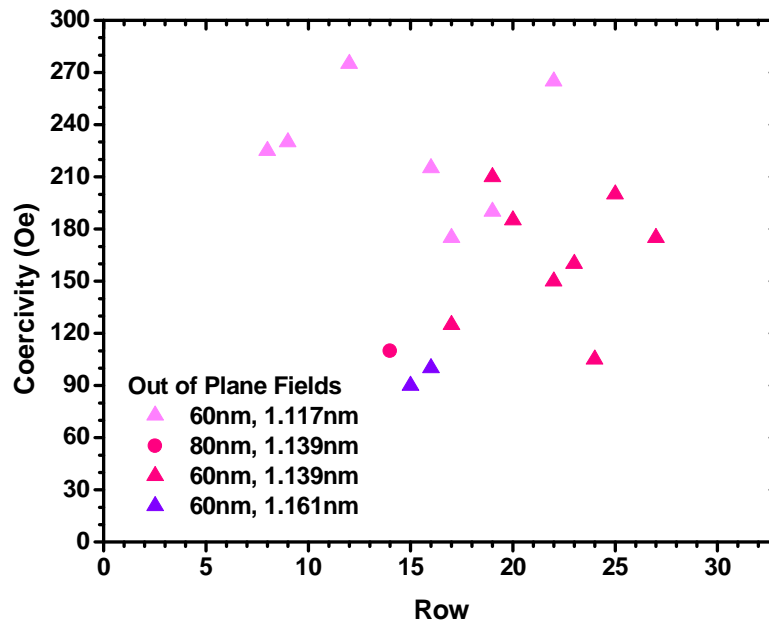
It can also be seen that the yield is also quite high, as all devices which were not shorted or opened were measured for their TMR. The two low TMR devices are both concentrated on Row 4, hinting at fabrication issues.



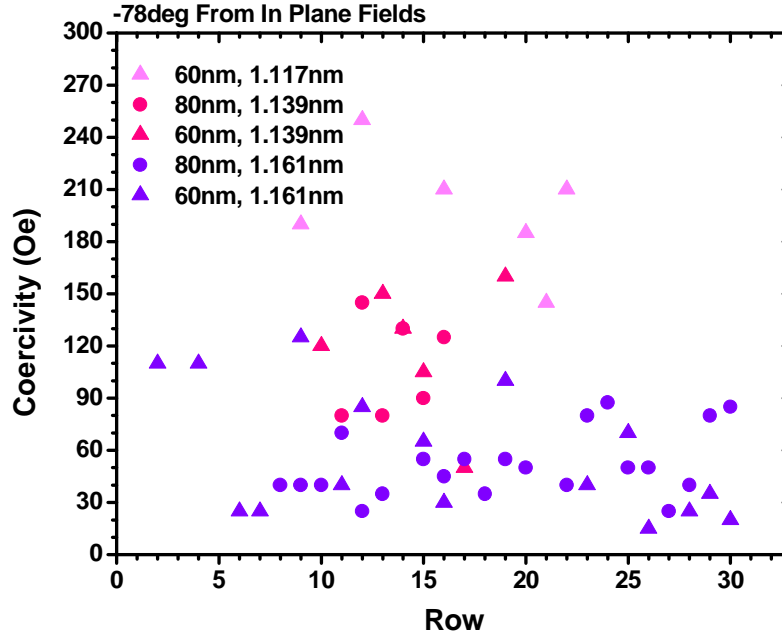
**Figure 11 shows the TMR for different sized devices, and at different free layer thicknesses. For different rows the stray field layer thickness is different, with larger rows having thinner CoFeB stray field layers. The TMR is quite uniform across different sizes and free layer thicknesses.**

A summary of device coercivities is plotted in Figure 12 and 13. Data points for Figure 12 was measured under pure out-of-plane fields, and Figure 13 was measured using an angled magnetic field, of  $22.9^\circ$  with the perpendicular direction. As expected, devices with thinner free layer have larger coercivities, due to larger perpendicular anisotropy energy. The large spread of coercivities can be attributed to the unreliability of calculating coercivities using only 3 RH loops. With this uncertainty, the expected coercivity difference between devices of different sizes is not obvious from the plot. Due to the nominal free layer thickness which should be constant for the same size devices, the free layer volume is decided by the device size, and the

perpendicular anisotropy energy is proportional to volume. It is then expected that devices with larger area will have proportionally larger coercivity. Between 60nm diameter devices and 80nm diameter devices at the same free layer thickness, the perpendicular anisotropy is expected to approach a ratio of 3:5.



**Figure 12 shows the coercivities for different sized devices, at different free layer thicknesses, measured when a purely out-of plane magnetic field is applied. As is expected, the coercivity is smaller for devices with thicker free layer.**

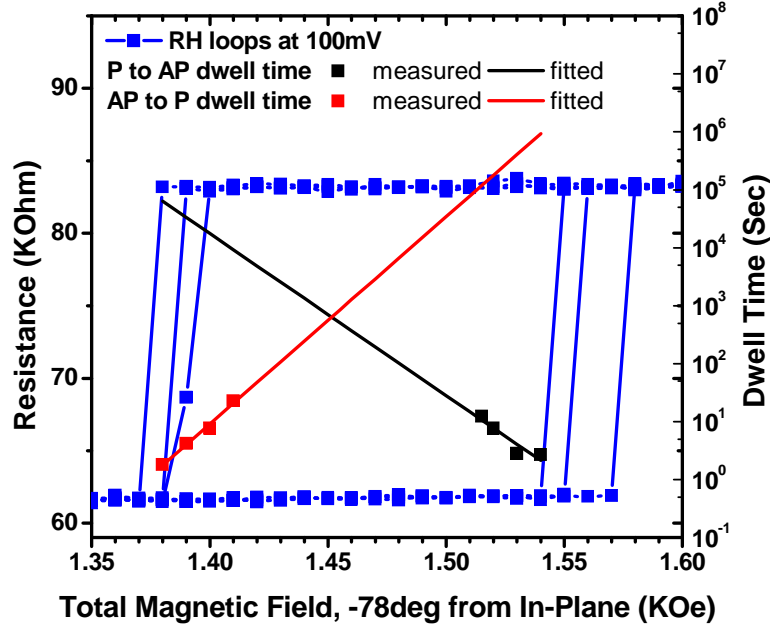


**Figure 13** shows the coercivities of the same devices, but measured at a field with an in-plane component.

The decrease in coercivity seen between Figure 12 and 13, when a non-zero in-plane field is applied to the device, is due to the free layer tilting out of the fully perpendicular direction, thus requiring less out of plane field to switch. Due to the same tilting effect, the TMR of the devices are also decreased, by a few percent, under an applied field which is  $22.1^\circ$  to the perpendicular direction.

### Section 3.1.2: Dwell Time





**Figure 14 shows an RH loop referenced to the left axis, together with the dwell time measurements and fits referenced to the right axis, for the estimation of the energy barrier height. The total field applied has an in-plane component in addition to the out-of plane component.**

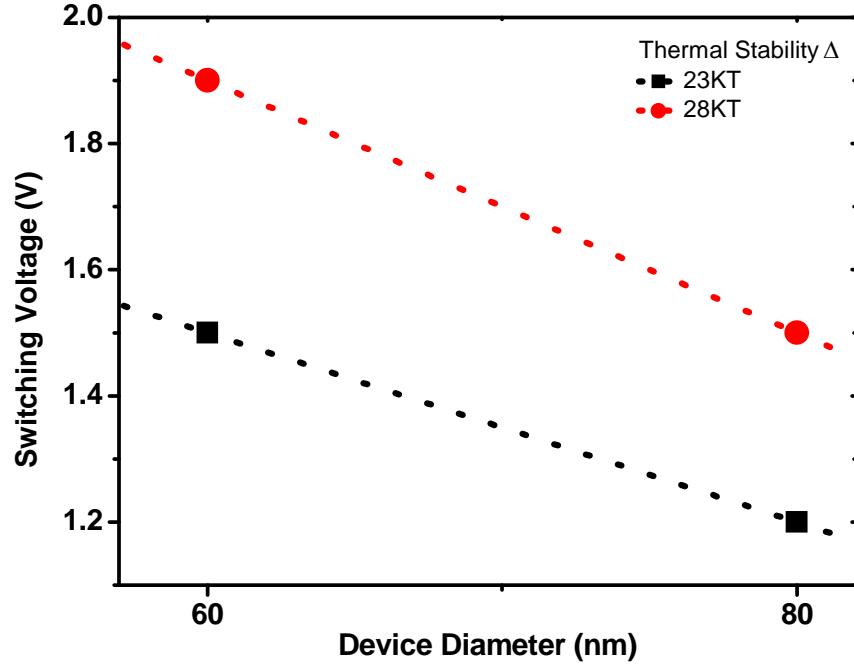
Figure 14 shows a representative RH loop, plotted together with the measured dwell times at the edge of the loop. For this device, the edge is at around 1370 Oe for the AP to P direction, and 1560 Oe for the P to AP direction. At fields close to these, the dwell time is measured using bias fields chosen near these two fields, shown in dots on Figure 14. The measured dwell times are fitted using the exponential dependence that the dwell time has on the bias field [42], shown by straight lines in Figure 14. The energy barrier height at the field where the dwell times are equal, here taken to be around 1450 Oe, is calculated using the Néel-Brown relaxation formula. For the devices investigated, the energy barrier height  $E_b$  is between  $20k_B T$ , up to  $30k_B T$ . This ensures a reasonable thermal stability when no voltages are being applied to the device. The RH loop and dwell times were both conducted at 100mV, because that is closer to the actual DC bias voltage the devices will feel when switching experiments are being conducted. Thus the energy barrier

calculated here can more accurately account for any current effects through the device due to the DC current.

The VCMA coefficient of the free layer of this wafer is assumed to be around  $30 \text{ fJ}/(\text{Vm})$ , as it is similar to another Ta seed layer wafer for which the VCMA coefficient was measured the conventional way; that is, measuring the RH curve, converting it to MH and then calculating the area between the curve, the saturation magnetization, and zero field. It was not possible to directly measure the VCMA for this wafer, because of the limitation of the projection magnet field strength for out of plane fields. The maximum field was not able to saturate the in-plane magnetization, due to its high  $H_s$ . In addition to the magnetic field not being large enough to saturate the magnetization, the magnetization itself was actually not completely in plane, and exhibited switching and coercivity when an out of plane field was swept. We did not apply an in-plane field to out of plane free layers, because the fixed layer also rotated under the external field, leading to inaccurate conversion to conductivity, which can yield an inaccurate magnetization  $M$ .

### **Section 3.1.3: Switching Voltage**

The minimum switching voltage for devices with diameter 60nm and 80nm were studied. Larger devices were not investigated due to their low device resistances, of around 12 KOhm and 20 KOhm in the P state respectively, which caused a large current to flow through the device during switching. Effects from the large current would have been hard to distinguish from pure VCMA-induced precessional switching, which is what we want to study. Additionally, the larger devices have a higher possibility of being multi-domain, thus invalidating the macrospin approximation.



**Figure 15** show preliminary switching voltage results for devices with different diameters, 60nm and 80nm. The thermal stability is kept constant between the different device diameters.

Preliminary results for the minimum switching voltage for otherwise identical devices with different areas are shown in Figure 15. It can be seen that the switching voltage increases quite uniformly as the device area is decreased, for different thermal stability values. This is due to the increased perpendicular anisotropy  $K_i$  which is necessary to retain the thermal stability as the device volume is decreased. The higher  $K_i$  requires more voltage to manipulate, for a constant VCMA coefficient. Further experiments are ongoing to verify the trend and slope of the voltage increase with more devices at more thermal stabilities.

Theoretically, a figure of merit for the ratio of the critical switching voltage divided by the thermal stability can be found. Recall the equations for the thermal stability and the energy barrier:

$$\Delta = \frac{E_b}{k_B T}$$

$$E_b = K_i(V)A = \frac{H_i(V)M_s A}{2}$$

The interface anisotropy is modulated by the applied voltage, proportional to the VCMA coefficient.

$$K_i(V_{app}) = K_i - \xi \frac{V_{app}}{d_{MgO}} = K_i - \xi E$$

The critical switching voltage  $V_c$  is defined as the applied voltage which decreases the interfacial anisotropy energy to zero. It is easy to see that for the same VCMA coefficient  $\xi$ , smaller area  $A$  will require larger critical switching voltages.

By rearranging the equations, the ratio of critical switching voltage to the thermal stability  $\Delta$  can be expressed as

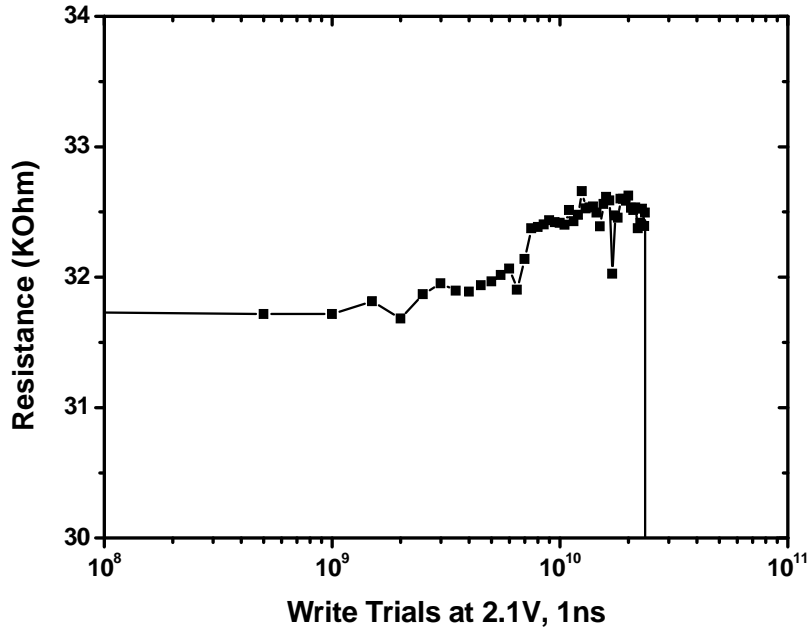
$$\frac{V_c}{\Delta} = \frac{k_B T d_{MgO}}{\xi A}$$

The figure of merit ratio should increase proportionally to the inverse of the area, if  $\xi$  is kept constant. The MgO thickness is usually not a variable, as it is decided more by the RA and endurance requirements of the device.

### **Section 3.1.4: Endurance and Breakdown**

The breakdown voltage for the 60nm and 80nm diameter devices was measured to be as high as 3.4V, which the devices would pass a few thousand pulses of before shorting. For voltages closer to the switching voltage around 2V, the endurance has been measured to be up to  $2.4 \cdot 10^{10}$  write

trials at 1ns pulsewidth, for 2.1V of write amplitude, and a pulsewidth of 1ns. Figure 16 shows the resistance change of an 80nm diameter device as write trials are successively applied. A small increase in resistance can be observed near the end of the lifetime of the device, before it shorts. This shift in resistance has so far not been observed for the other device under test at 1.5V, so it's possible that it is due to the larger applied voltage, for example charge accumulation effects in the MgO. For pulses with voltage amplitude of 1.5V and pulse width of 1ns, the endurance for a similar structure 80nm diameter device was measured up to  $1.2 \cdot 10^{11}$  trials, before the device shorted. In fact it is likely the device was shorted due to non-standard measurement procedures which may have introduced a voltage spike to the device. This is the difficulty with endurance tests: not only do they require a large time frame, but one must be extremely careful to avoid any kind of disturbance, as it is not possible to tell what exactly causes a short or open device after it has happened. Further measurements at other write voltages are ongoing.



**Figure 16 shows the resistance evolution of an 80nm diameter device with a nominal MgO thickness of 1.14nm. After around 2.4E10 trials the device shorted, after showing a slight increase in resistance.**

The breakdown voltage for larger devices, of diameter 100nm to 120nm, is much smaller, at 1.9V. At least 3 devices with diameter 120nm have shorted consistently at this voltage after just a few hundred write trials. This lowered endurance can be attributed to the larger tunneling current that is passing through the larger devices for the same applied voltage. The 120nm diameter devices have an average P state resistance of around 12 KOhms, while the 80nm diameter devices have an average resistance of around 40 KOhms. This implies a current of around 0.158mA for the large devices, and only 0.085 mA through the smaller devices, at their respective breakdown voltages. The current density for the two is respectively  $1.4 \cdot 10^{10} \text{ A/m}^2$  and  $1.69 \cdot 10^{10} \text{ A/m}^2$ . From this it seems that the maximum current density that an MTJ with nominal MgO thickness of 1.14nm can withstand for more than 10K write trials is around  $1.5 \cdot 10^{10} \text{ A/m}^2$ .

Since the nominal MgO thickness is uniform for all sized devices, having a maximum current density rather than a breakdown voltage amplitude implies that the breakdown mechanism for these MTJ devices is dominated by tunneling electrons forming a percolation path through the MgO and ultimately shorting the tunneling barrier. The voltage which generates this maximum current is below the voltage at which the electric field across the MgO approaches the breakdown electric field.

That the dielectric breakdown is dominated by percolation paths at lower applied voltages, instead of hard breakdown due to the application of a critical breakdown electric field across the insulator, could be because the MgO initially has some leaky spots which aids the formation of leakage paths. If this is caused by fabrication, then the deposition/sputtering method can be better optimized for higher endurance. It is also possible that for the MgO layers between 1nm and 2nm that are being used in MTJs, this is the best quality that can be achieved for sputtering. Nevertheless, more research and process optimization is needed.

Two papers which discuss percolation path [43], and critical electric field [44], dominating the breakdown process, come to conflicting conclusions. This discrepancy could be attributed to the different MgO thicknesses studied, with the leaky percolation paths paper using 1nm, and the hard breakdown paper using thicknesses between 0.7nm and 0.85nm. Both used magnetron sputtering to deposit the MgO, however the critical field paper uses high-vacuum deposition, while this is not mentioned in the leaky percolation paths paper. If thinner MgO means more defects, then the latter paper should not have seen hard breakdown. However at thinner insulating barriers the field across the barrier is higher for the same applied voltage, and at the same time the current is larger.

To reconcile these different findings will require more research, and dedicated time to dielectric breakdown (TTDB) tests.

### Section 3.1.5: Write Error Rates

For the precessional switching that we are interested in, which is initiated by the VCMA effect, reliable switching depends heavily on the free layer magnetization precessing in a predictable and coherent way. If the applied voltage pulse is timed to be exactly half the precession period, the magnetization will precess smoothly to the opposite easy axis direction, then align to it, for a successful switch. Please refer to Figure 4 for a diagram and explanation of precessional motion. Anything that disturbs this precession will cause switching errors, for example thermal fluctuations, spin torque, heating, or multi-domain effects which can include subvolume excitation [45].

Before the experimental results are presented, some of the parameters relevant to write error rates are discussed theoretically. Due to time and energy constraints, not all of these factors could be studied experimentally. The contribution of these parameters, as well as other factors, to switching errors is discussed. A brief overview of experimental investigations into write error rates that have been conducted is presented as the motivation for our method of investigating write error rates.

Precessional switching parameters which are external to the device include the externally applied in-plane field magnitude  $H_{ext}$ , the voltage pulse length  $t_{pulse}$ , and the voltage pulse amplitude  $v_{pulse}$ . Internal parameters include the Gilbert damping parameter  $\alpha$ , and the thermal stability, which is determined by the perpendicular magnetic anisotropy field  $H_K$ , saturation magnetization  $M_s$ , and the switching volume  $V$ :  $\Delta = \frac{H_K M_s V}{2k_B T} = \frac{E_b}{k_B T}$  [33], where  $E_b$  is the anisotropy energy barrier height between the two perpendicular easy axis directions.



The voltage pulse length  $t_{pulse}$  should theoretically be timed to be half the precession period, so that the perpendicular easy axis can be reintroduced just as the magnetization swings around to the other side of the original direction. However if STT effects are taken into account, where the current through the device is different for AP and P states, the best switching rate for AP->P and P->AP directions is actually at different pulse widths [46]. This is because the polarized electron spins will help or hinder the precession depending on which way the magnetization is trying to precess to. For example, if the free layer is below the fixed layer in the device stack, and a positive voltage is applied to the top of the stack, the current will always pass from the fixed to the free layer. Thus, AP to P direction switching will be favored by STT, over P to AP switching. Effectively, the field-like torque exerted on the free layer by the electron current shifts the minor RH curve closer to zero field, and this changes both the optimum in-plane field and pulsewidth to different values for the two directions of P and AP switching. The pulsewidth is changed as well, because STT effects change the effective field acting on the magnetization, which changes the precession period. To decrease these unwanted STT effects, the device resistance should be increased, by increasing MgO thickness. However, large device resistance, especially when the area is scaled as well, will increase the RCL delay of any control circuits that are connected, which slows down the read/write speed. The MgO thickness can also change the anisotropy of the ferromagnetic layers, by altering interactions between the fixed and free layers. For our devices, thicker MgO at the same fixed and free layer thicknesses increased the fixed layer coercivity. This could have been due to fabrication process variations incidental to depositing thicker MgO, or to decrease of interactions.

The voltage pulse amplitude  $v_{pulse}$  should be large enough to reduce the perpendicular anisotropy enough so that the effective field is in plane. But applying large voltages, especially approaching the breakdown voltage, would reduce the lifetime of the device. The STT effects discussed earlier in this section will also become more pronounced due to the increased current.

The pulse amplitude is directly related to the write energy consumption of the MTJ, assuming a capacitor across the insulator:  $E_{write} = \frac{1}{2} CV^2 = \frac{\epsilon AV^2}{2d_{MgO}}$  where  $\epsilon$  is the permittivity of MgO. For more energy efficient operation, the voltage amplitude needs to decrease through an increase of the VCMA coefficient.

For the Gilbert damping parameter  $\alpha$ , simulations show that devices with low damping can achieve high switching rates [33] [36]. The reason for this is explained as, for low damping materials the standard deviation of the thermal agitation term is proportional to the damping, so lower damping means less thermal noise. The thermal agitation term  $k$  in the Fokker-Planck equation is of the form:  $k = k_B Th/V$ , where  $h = (\alpha\gamma)/(M_s + M_s\alpha^2)$ ,  $V$  is the ferromagnet volume, and  $\gamma$  is the gyromagnetic ratio. From the same logic, other methods of decreasing the thermal noise is to increase the saturation magnetization  $M_s$  or the volume  $V$ . Low damping also means that the magnetization stays closer to the perpendicular easy axis as it precesses around the effective in-plane field, the precessional angle  $\theta$  between the effective in-plane field and the magnetization decreases slower. This smaller precessional angle means that the magnetization has a larger chance of aligning to the opposite perpendicular easy axis direction when the PMA is reintroduced. Please refer to Figure 4 for a better picture of precessional dynamics.

The thermal stability  $\Delta$  of the device, partially determined by the perpendicular anisotropy, also affects the switching rate. With a large thermal stability, the probability is higher that the magnetization starts out in a smaller region more concentrated around the perpendicular axis. After precessing for half of the precession period, assuming a perfect precessional movement of the single domain magnetization, the probability is also higher that the magnetization will be close to the perpendicular easy axis in the opposite direction, and this will result in a larger switching probability [46]. Larger thermal stability also decreases the probability of switchback; this is the phenomenon where the magnetization jumps out of its current state and into the

opposite state due to thermal fluctuations, even without an applied voltage pulse. This usually happens for very low thermal stability cases only, where the energy barrier between the easy axis directions is comparatively low, compared to the thermal energy  $k_B T$ . For commercial applications, the thermal stability for single bits must be high enough to be able to retain information for 10 years. For single bits this implies a thermal stability of 40, but for arrays of long-term memory the requirement is higher.

Subvolume excitation can also cause switching errors. This refers to magnetic excitation which is not single domain, that is, macrospin; where the free layer is split into many subdomains which switch semi-independently, thus decreasing switching efficiency [45]. The subvolume is usually smaller than the actual physical volume of the material, and is proportional to the exchange length of the thin film. For the CoFeB material in the cited study the diameter of the domains is around 40nm. When the device is larger than this subvolume size, and when spin wave excitation which is non uniform becomes dominant, non-macrospin effects start to become prominent. In device parameters, subvolumes can show up as a much higher damping constant than predicted, and could possibly be what is being seen for our devices. To decrease these subvolume effects, the physical size of the device can be decreased to be around the subvolume size, or the internal exchange strength of the material can be improved [47].

In summary, thermal noise and non-single-domain switching dynamics can prevent MTJ devices from achieving high switching rates. Further theoretical and experimental investigation into the causes of decoherence, and methods of decreasing it is needed. Methods to decrease the effect of thermal noise without increasing switching voltage unreasonably is also an important area. So far, most experimental investigations, including into STT-RAM switching rates, have been limited to low trial numbers in the hundreds [36] [26] [22] [48]. While these techniques are acceptable for replicating the general trend of the switching behavior at different biasing conditions, it is not suitable for investigating the extremely high switching rates that theoretical

studies have been predicting. Other methods have used arrays of devices to get a single switching rate for each device [49]; this method assumes that all the devices in the array are physically identical and behave the same way, which is debatable for smaller devices due to fabrication process variations. Other papers have integrated the MTJ devices into CMOS logic circuits, which presumably can latch and convert the MTJ state into logic signals for fast processing of write trial results [50] [51]. While this method has the potential to greatly simplify the experimental hardware setup, the design and fabrication of such circuits is more complicated. For optimizing the stack materials and fabrication process this process is not as flexible as only having stand-alone MTJ devices. However something can be said for this method also testing the CMOS integration of MTJs at this stage. Simulations of switching rates are usually limited to solving for the probability density function of the magnetization direction using the Fokker-Planck equation, or solving the LLG equation for a small number of trials. While this does yield valuable insight into how various parameters affect switching performance, experimental confirmation is needed.

In terms of other methods to switch the MTJ device, there have been investigations in using spin-orbit interactions to decrease the energy barrier rather than using electric field [52]. This method turns the MTJ into a three terminal device, with a heavy metal connect directly under the MTJ stack, in contact with the free layer. A spin-polarized current flows through this metal connect, and due to the spin hall effect, spins will gather near the free layer and effectively lower the energy barrier. This can decrease the needed critical current through the MTJ and increase device lifetime, but on the other hand, as of now a large current is needed to pass through the metal connect. Other switching methods generally involve combinations of thermal activation or precession, used in conjunction with different ways of lowering the energy barrier to allow that to happen; for example heat, anisotropy-graded and exchange-coupled media, or exploiting the behavior of multiferroics with strain.

In this section the write error rate results for Ta seed layer devices is presented. In summary, write error rates of down to  $10^{-3}$  and  $10^{-4}$  respectively, for the P→AP direction switching and AP→P switching were found. We investigated the effect of free layer thickness, or effectively switching voltage pulse width, and external field strength on the switching probability.

#### ***Subsection 3.1.5.1: Free Layer CoFeB Thickness***

Decreasing the free layer thickness will increase the PMA, and increase the energy barrier between the stable states, and thus the thermal stability. However this also increases the switching voltage for a constant VCMA coefficient, which is assumed to be true across all the devices. In order to not have extremely high switching voltages which would decrease the endurance of the device, a high in-plane field is applied to tilt the magnetization (and thus the energy wells) to decrease the energy barrier. With a high in-plane field applied, the precession speed increases, and the optimum pulsewidth decreases. Thus to keep the switching voltage generally constant and under the breakdown voltage of 2.6V, changing free layer thickness effectively meant changing optimum pulsewidth, which is closely related to the in-plane field.

Figure 17 and 18 below show representative write error rate curves for a total of 1K trials per data point, and 50K trials per data point respectively. The device is a 60nm diameter device with nominal free layer thickness of 1.117nm. The total applied magnetic field was 1720 Oe, with 1440 Oe out-of-plane component, and 940 Oe in-plane field component. In Figure 17 the data points cut off at  $10^{-3}$  because no errors in 1K trials were found during that set of tests. There is also a large noise present in the results. However the noise is much lower for the 50K trials in Figure 18, illustrating the need for large trial numbers to properly investigate low write error rates.

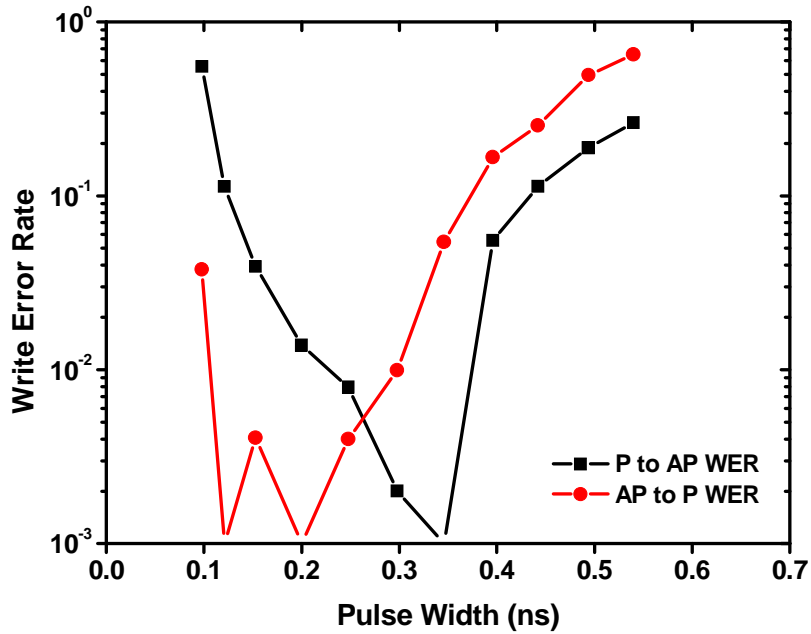


Figure 17 shows a write error rate plot for different pulse widths, with 1K trials per data point. The curve cuts off in three places near E-3 due to no errors being detected during that trial run. Noise is quite prominent.

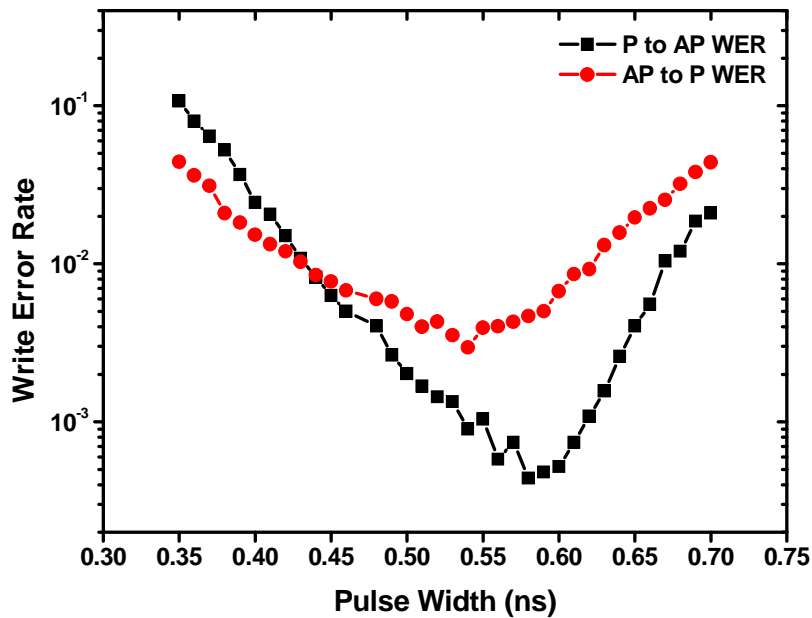


Figure 18 shows a write error rate plot for the same device, except with 50K write trials per data point. The noise is much smaller, and the curve appears to smooth out near 2E-4 WER for the P to AP direction.

Figure 18 also shows that for devices with thin free layer, balanced write error rates did not decrease beyond  $10^{-4}$ , at optimum pulsewidths of between 0.4ns and 0.6nm, which varies between devices. It is possible the precession is too fast, due to the large in-plane field which was applied to tilt the magnetizations of devices with thin free layer. Nonuniform precession could have been compounded by a non-ideal pulse shape being applied across the MTJ, either due to the pulse generator itself, or distortions introduced by the test circuit.

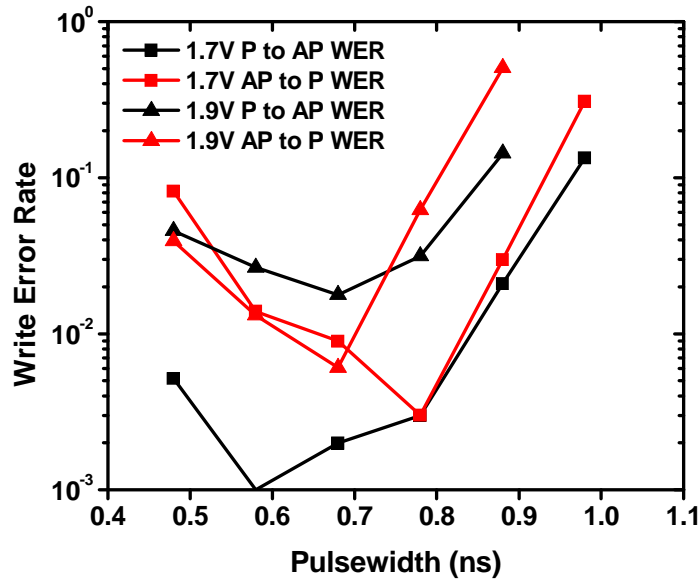
Recent simulations have been able to accurately reproduce the switching data by using a damping factor of  $\alpha=0.27$ , which is 10 times larger than what usually is predicted for actual devices. For such high damping the precessional angle between the magnetization and the in-plane effective field would increase extremely fast, which would explain why the switching is only be good at extremely short pulsewidths, with large in-plane fields applied. For slower precession the magnetization would almost be in-plane by the half the precessional period. Since the damping factor is intrinsic to the device, or more accurately to the free layer, it could be possible that switching could be bad across the entire wafer. But it's reasonable to assume that the damping factor could decrease as the free layer thickness is increased, due to smaller edge effects.

The larger damping factor could also be a symptom of subvolume excitation, namely that the switching volume is smaller than the actual volume of the free layer, and single-domain macrospin models no longer accurately predict the switching behavior. Further simulations will be needed to verify if this is the cause of bad switching.

If the damping factor is not due to multidomain effects, it may be worthwhile to optimize the composition of the CoFeB layers, since all three materials have different damping factors. In addition, due to the presence of an interface with the insulator, an additional damping factor

may be introduced [30] in the ferromagnet, so interface engineering can also be a possibility to reduce the damping factor.

As the free layer thickness is increased, the required in-plane field is smaller due to the smaller PMA, and thus the precession is slower. From the lowered switching voltages it can be inferred that the energy barrier/thermal stability is lower as well. Figure 19 shows a representative write error rate plot for a 60nm diameter device with nominal free layer thickness of 1.161nm, done with 1K trials at each point. It can be seen that the switching at 1.9V is better than at 1.7V, being able to achieve lower WER. However there still seems to be significant noise in the results, so further experiments are ongoing using more write trials, to decrease the noise in the results.



**Figure 19 shows the write error rate plot for a 60nm diameter device with nominal free layer of 1.161nm, for two different write voltage amplitudes, 1.7V and 1.9V.**

Theoretically, the switching behavior at thicker free layers should be a trade-off between lower thermal stability devices that are more susceptible to thermal noise, competing with slower switching which would spend more time around the opposite direction. There should be an



optimum tradeoff point between the two effects, where slower and more coherent switching would lose to increased thermal noise effects and lower thermal stability, and show decreased switching rate.

### ***Subsection 3.1.5.2: In-Plane Magnetic Field***

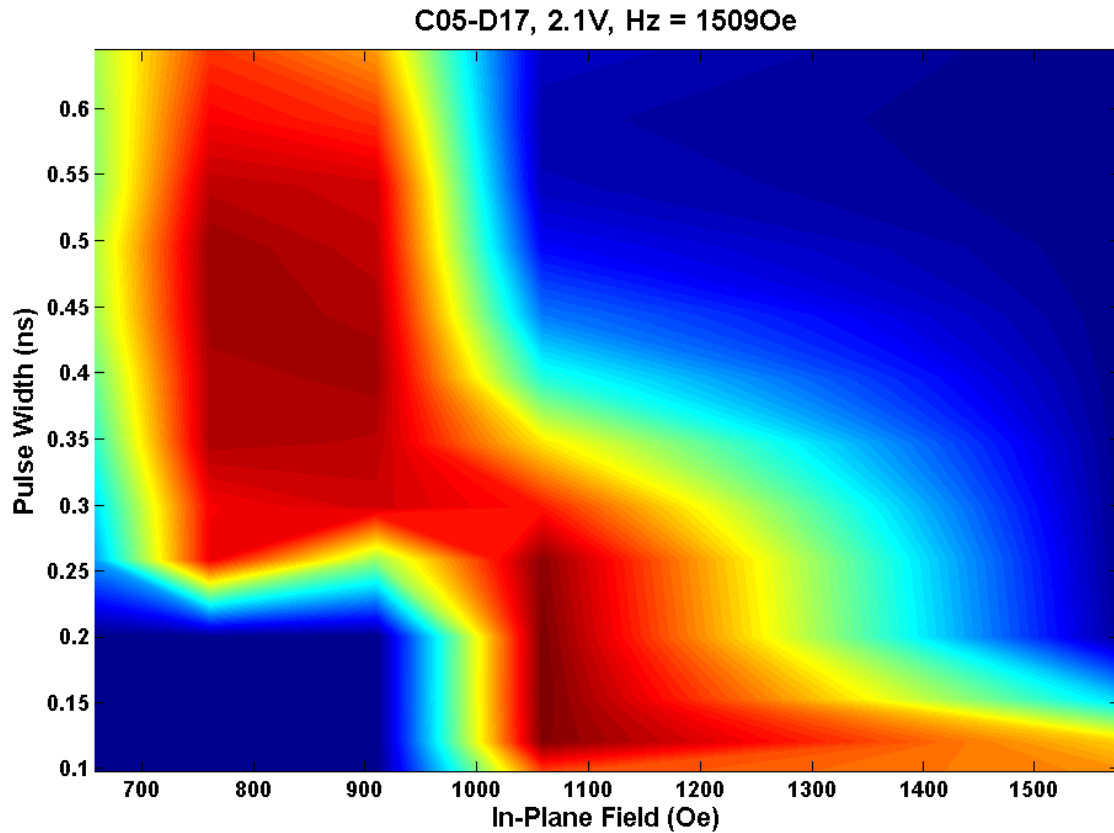
The external applied field  $H_{ext}$  provides an effective in-plane field for the magnetizations to precess around. It should not be too large or too small [33] [48]. Too large in-plane effective field increases both the precession angle  $\theta$  (the angle between the magnetization and the plane perpendicular to the in-plane effective field, as illustrated in Figure 4) and the precession frequency. A large precession angle means that once the perpendicular anisotropy is reinstated with the removal of the voltage pulse, the magnetization has a larger chance of realigning to the original direction, resulting in a failed switch attempt. The magnetization is also more susceptible to thermal fluctuations pushing it back to the original direction, when the magnetization is farther away from the perpendicular easy axis, because it has to precess for a longer time to realign in the perpendicular direction. Faster precession may also encourage multi-domains or other non-coherence in the precession, effectively reducing the single-domain switching volume. If the in-plane field is too small, the precession will be slow, and during the longer precession time it is subject to more thermal fluctuations. It is also possible that if the applied voltage is not enough, the perpendicular anisotropy field may be comparable to the externally applied field, causing the  $H_{eff}$  to not be fully in-plane. A precession around an effective field which is not really perpendicular to the original direction of the magnetization will not be uniform, and will not pass predictably through the opposite perpendicular direction, causing bad switching rates.

In the MTJ devices that are investigated here, there is also a dipole field from the fixed layer which must be cancelled by an externally applied field in the perpendicular direction. Slight over or under-compensation of this field will result in one state being favored over the other. Extreme over or under-compensation will pin the magnetization in a certain direction, and be extremely hard to switch in the other direction. There is only one optimum out-of-plane field for good switching rates. To get rid of the need for an external applied field, as would be required in a commercial device, a layer near the free layer can be inserted that applies a dipole field in the opposite direction to the fixed layer. Due to the sensitivity of this compensation, the field this layer applies must be controlled carefully, so care must be taken during.

The in-plane field is to give the magnetization an effective in-plane axis to precess around. It helps the magnetizations precess smoothly, because the devices are circular, so in the in-plane direction there is no preferred direction. Once the perpendicular anisotropy is destroyed with the applied voltage pulse, it helps to have an in-plane axis for the magnetizations to precess around, without the magnetizations doing some weird motions which may also be more susceptible to thermal fluctuations. The added in-plane field also helps speed up precession. From the chart you can see that as the in-plane field decreases, the precession period increases, and larger in-plane fields have better switching at smaller pulse widths. However there is an optimum in-plane field, too large (narrower optimum pulse width range is harder to find, decreased thermal stability) or too small (increased thermal fluctuations) both will give lower switching rates.

Figure 20 shows a phase map of the combined AP→P and P→AP direction switching rate, which is multiplied together. The red regions show 'hot spots' for low write error rates, and the blue regions show high write error rates. For this device, the applied write voltage has amplitude of 2.1V and an out of plane field of 1509 Oe, which compensates for the dipole fields well. For low in-plane fields, the optimum pulsewidth for good switching is at longer pulsewidths than for

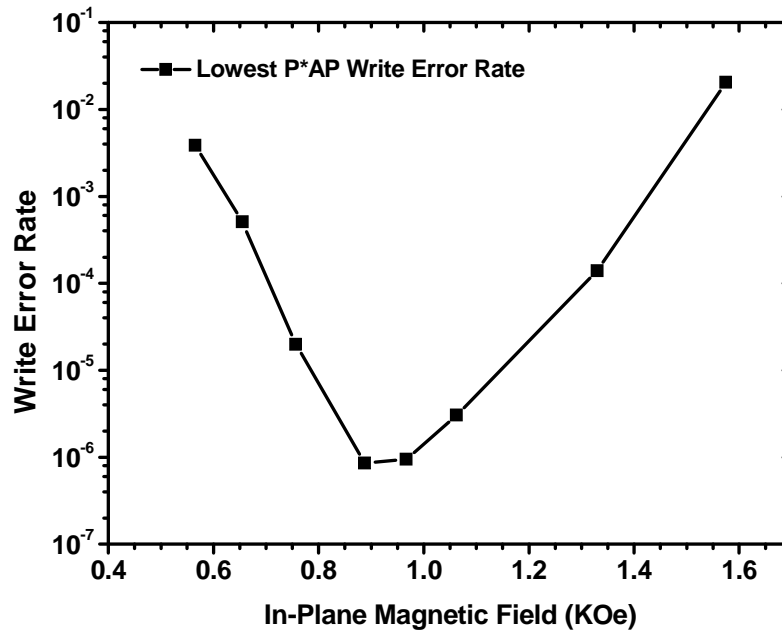
higher in-plane fields. This confirms the dependence of the precessional period on the applied in-plane field. This phase map was plotted using 5K write trials for each data point, so ideally 2.5K trials for each side.



**Figure 20 shows a phase map of the combined P to AP switching rate, multiplied by the AP to P switching rate, for different in-plane fields and pulse widths. The write amplitude is 2.1V, and the out-of plane field is 1509 Oe. Red regions denote small write error rates, blue regions denote large write error rates.**

In Figures 21 and 22, the lowest write error rate for each field magnitude and pulse width was found and plotted for the same device. The trial numbers for these plots are higher than that used in the phase map, reaching 100K for the lowest write error rates. At this many trials both the write error rate noise and field and pulsewidth variation should be minimal. Figure 21 shows the optimum in-plane field for write error rates is between 900 Oe to 1000 Oe. Figure 22 plots

the other parameters that contribute to the low error rate at those in-plane fields. The optimum write pulse width is between 0.25ns to 0.3ns, and the optimum out of plane field component is relatively constant at around 1500 Oe.



**Figure 21 plots the lowest combined write error rate against the in-plane field for which it is found. The pulse width and out of plane fields were optimized to find the best write error rate for each in-plane magnetic field.**

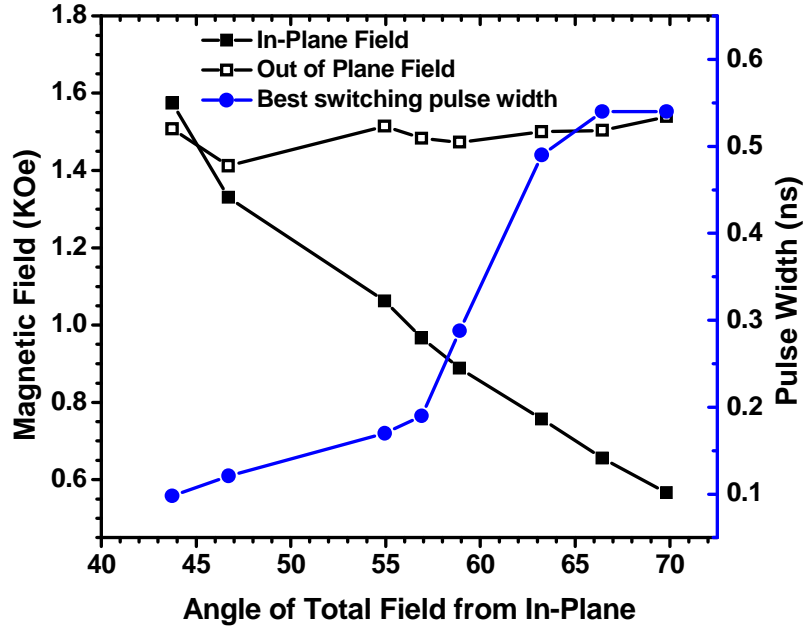
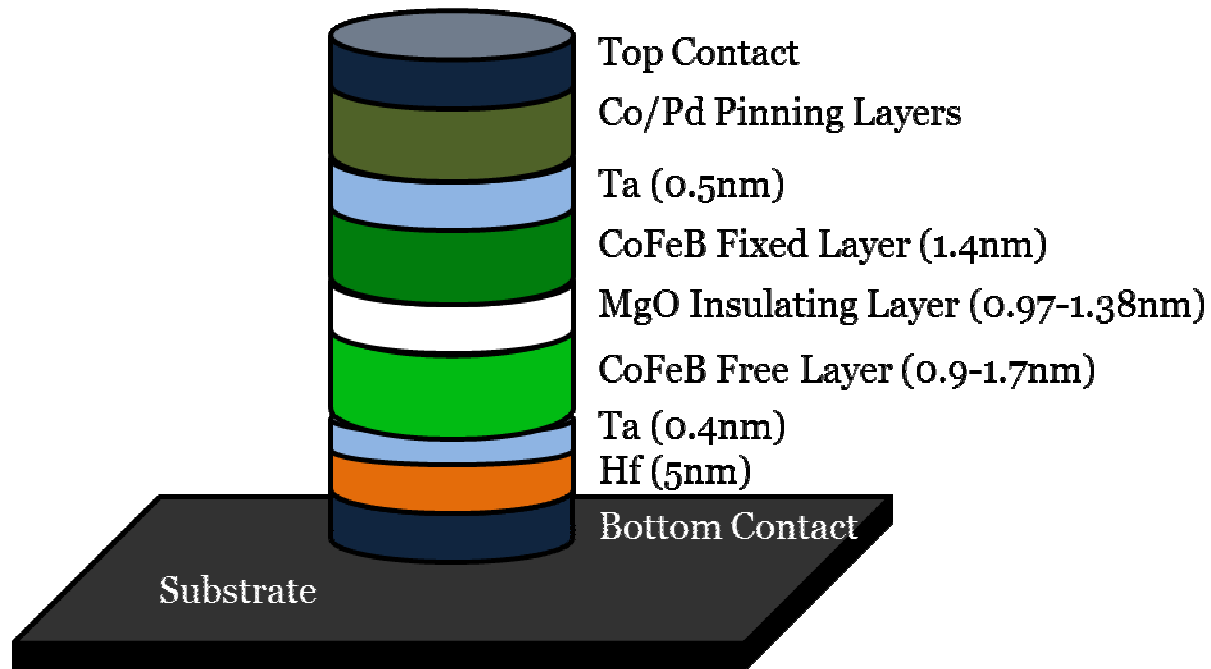


Figure 22 plots the in-plane field, out of plane field, and pulse width, against the magnetic field angle from the in-plane direction, for which the lowest write error rate was found. The magnetic field is referenced to the left y-axis, and the pulse width is referenced to the right y-axis. The x-axis is the angle of the applied magnetic field, measured from the in-plane direction. As is expected, the optimum out of plane field is relatively constant. The optimum in-plane field decreases as the magnetic field angle is increased, and with the decrease of in-plane field, the precession slows down so the optimum switching pulsewidth increases.

## Chapter 3.2: Hafnium Seed Layer Devices



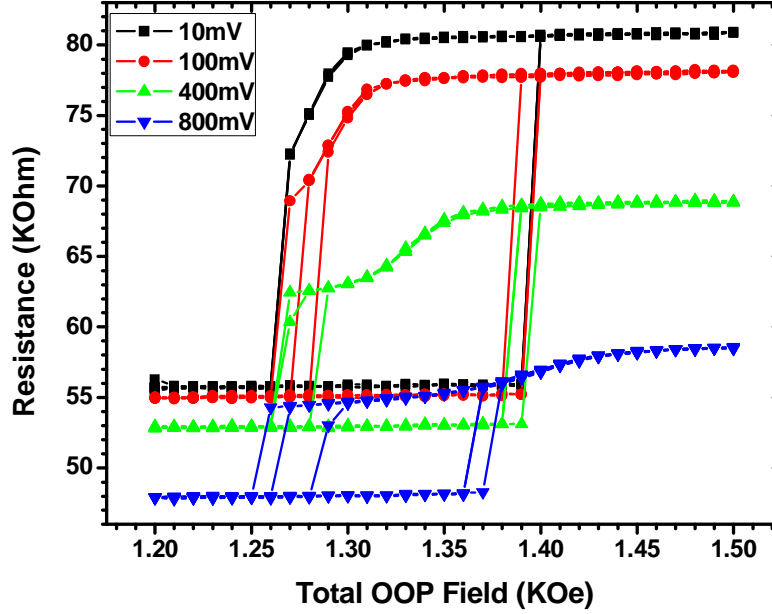
**Figure 23 shows the device stack structure of the Hf seed layer devices. Notice the two perpendicular wedges across the wafer, one for the MgO insulating layer, and the second for the CoFeB free layer. These wedges allow us to pick the thickness with the best performance.**

Hafnium seed layer has been shown to increase the PMA of the free layer [53]. It was hoped that the VCMA coefficient would similarly be improved for these devices, so that switching voltages do not increase too much. For these devices a 0.5nm buffer layer of Ta is inserted between the Hf to encourage a smooth interface with the CoFeB. Devices of diameter between 50nm to 100nm were fabricated to continue investigation into nanoscale MTJ devices which should have a minimum of multidomain effects.

The device structure is shown in Figure 23. Across the wafer of this chip there are two wedges perpendicular to each other, one for the free layer, and the second for the MgO insulator layer.

### Section 3.2.1: General Device Parameters

A representative RH loop for an 80nm diameter device with nominal free layer thickness of 1.31nm, and MgO thickness of 1.28nm is shown in Figure 24.



**Figure 24 shows RH loops for a representative 80nm Hf seed layer device with a nominal free layer thickness of 1.31nm, and MgO thickness of 1.28 nm.**

The transition thickness between perpendicular easy axis and in-plane easy axis is on average around 1.33nm across the wafer, so this is just on the perpendicular side. For the 10mV RH loop, a slow rotation of the magnetization near the AP→P edge of the RH loop can be seen, before the magnetization switches abruptly to the P state. This indicates that the free layer at this thickness is still not fully perpendicular for this device. This phenomenon becomes less pronounced at higher applied voltages, but the reason is not clear. One reason could be that it is simply not as noticeable due to the lowered resistances and TMR ratio.

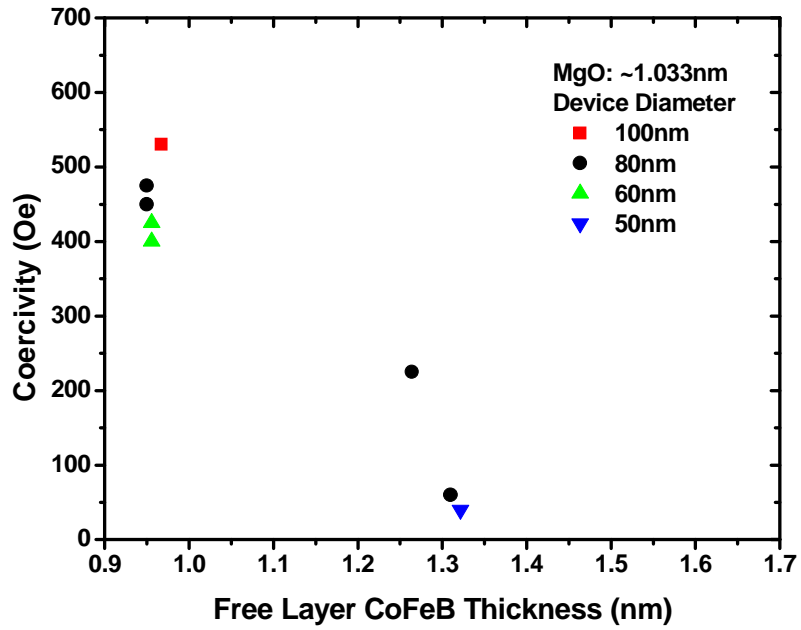


Figure 25 shows the coercivity of devices with different sizes and free layer thicknesses, for MgO thickness of around 1.033nm.

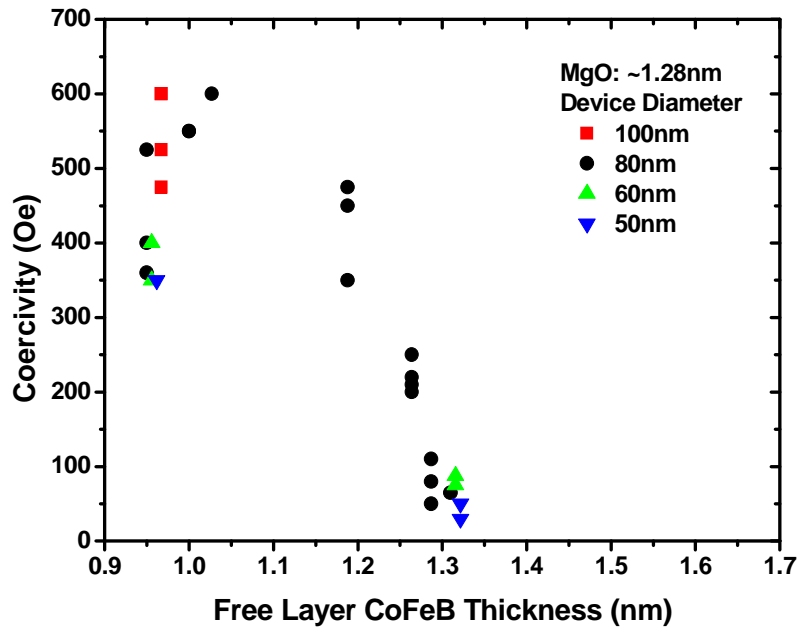


Figure 26 shows the coercivity for devices with different sizes and free layer thicknesses, for MgO thickness of around 1.28nm.



Figure 25 shows the coercivity of devices for MgO thickness of around 1.033nm, and Figure 26 shows the coercivity for devices with MgO thickness of around 1.26nm. The coercivity shows a non-linearity as the free layer thickness is decreased: first increasing, and then decreasing to zero close to the transition point. This nonlinear behavior of the coercivity is expected, as it has been seen previously for other ultrathin ferromagnetic films, and can be attributed to the demagnetization field overpowering the interface anisotropy, or equivalently to a decreasing  $H_K$  [10] The large distribution of coercivity for devices with nominally the same area, free layer thickness, and MgO thickness, could be a compound of measurement error and fabrication unevenness. Due to the MgO wedge, each device with the same free layer thickness does have a different MgO layer, but according to the wedge calibration from the film deposition company, the slope is 0.015nm per every 5mm across the wafer, and as the spacing between each device is around 0.8mm, that translates to 0.0024nm MgO thickness difference between each neighboring device. Since the coercivity measurements are generally taken for devices right next to each other, skipping shorted or opened devices, the MgO variation should not be this large.

For devices around 1.1nm no data could be gathered, because out of plane fields of  $\pm 2000\text{Oe}$  was not even able to switch the free layer, likely caused by a high offset field of above  $1500\text{Oe}$ , combined with a coercivity field larger than  $600\text{Oe}$ .

The devices exhibit two offset fields depending on the fixed layer orientation as the minor loop is measured, as shown in the major loops for two different devices in Figure 27 and 28. Figure 27 shows a device with an offset field of  $+1500\text{Oe}$  and  $-500\text{Oe}$ , and Figure 28 shows a device with an offset field of  $-1500\text{Oe}$  and  $+500\text{Oe}$ . Figure 28 also shows the minor loops of the device, for 10mV and 100mV voltages applied. Thus in absolute value, the offset field is roughly  $1500\text{Oe}$  and  $500\text{Oe}$ . This shift of  $500\text{Oe}$ , which causes the offset field to not be exactly  $\pm 1000\text{Oe}$  on both sides, probably originates from other layers in the stack, like the pinning layer giving an offset, the exact sign of which depends on the orientation of the pinning layer.

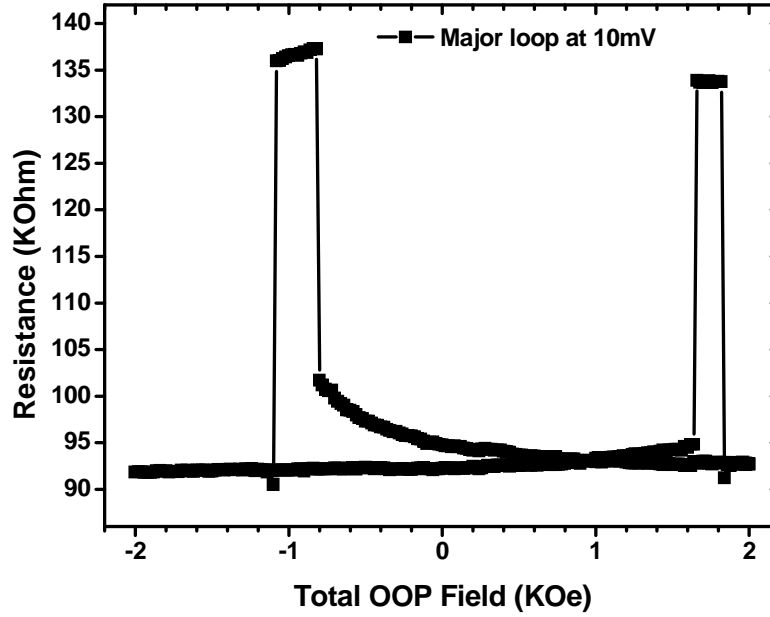


Figure 27 shows the major RH loop of a 60nm device with offset fields at -500 Oe and +1500 Oe, respectively. The major RH loop switches the fixed and free layer magnetizations.

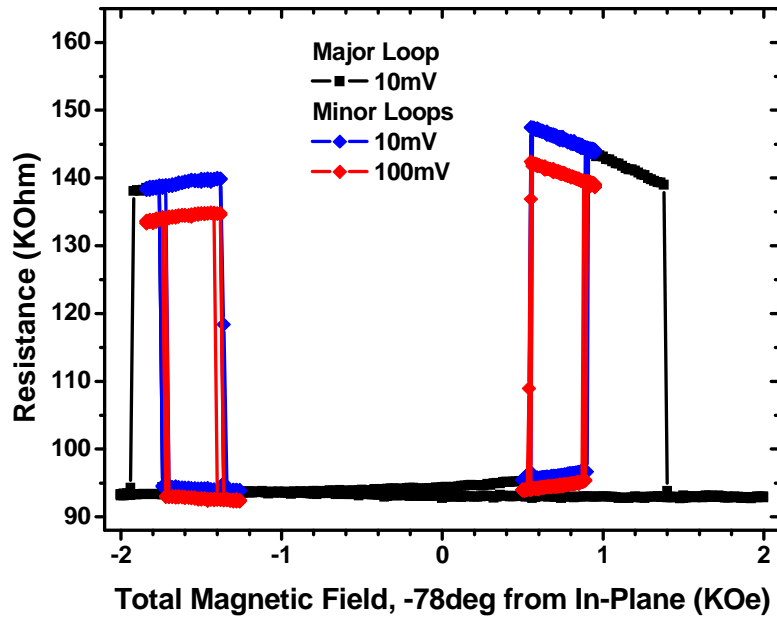


Figure 28 shows a representative major and minor RH loops for a 60nm device with offset fields of -1500 Oe and +500Oe. The reason for the resistance change in the AP state, for both the major and minor curves, is not clear.

The major loops also show a strange decrease of resistance while the device is in the AP state, as is more obvious in Figure 28. This phenomenon is also more pronounced in the smaller side of the offset field. The reason for this is not clear. Because the major RH loop switches both the free and fixed layer magnetization directions, the only reason the resistance is decreasing like that is if one of the layers is rotating slowly under the external magnetic field, before switching abruptly. From zero field, the first jump to AP state is the free layer switching, because it has been engineered to have a smaller coercivity. The second jump to P state at even higher fields is due to the fixed layer switching to align with the external field as well. Using this analysis, the resistance change in the AP state can only be caused by the fixed layer slowly rotating before switching abruptly.

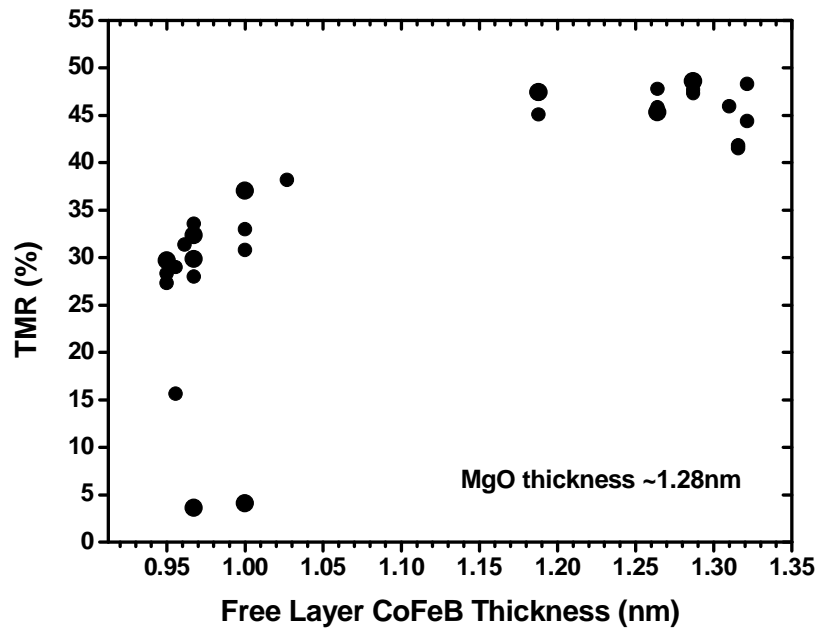
However this should not be the case, as the fixed layer should be extremely perpendicular, even more so than the free layer. It should be able to switch abruptly, instead of rotating. However it is true that in Figure 28 the resistance change in the AP state is more pronounced, and the field at which those measurements were taken is not strictly out-of plane, there is an in-plane component. Nevertheless, for an extremely perpendicular fixed layer, an in-plane field component on the magnitude where the measurements were taken should not have caused it to rotate.

The minor loops also show the resistance change in the AP state. Using a similar analysis procedure as the major loops, it can be deduced that it is also the fixed layer rotating slowly under the external applied magnetic field.

Even though it does not make much sense, it seems that one possible reason for the resistance change in the AP state is caused by a not fully perpendicular fixed layer.

The TMR of devices with MgO thicknesses of around 1.28nm were measured and plotted in Figure 29. Across the wafer the TMR was found to be on par with, if not even higher than the Ta

seed layer devices. The highest TMR reached almost 50% for devices with thicker free layers, but dropped to around 30% for devices with thin free layers. This could be due to the fact that the free layer CoFeB is smoother when it is thicker, leading to better TMR. The RA of these devices increased as the device size decreased as well, from  $100 \Omega \cdot \mu\text{m}^2$  up to  $140 \Omega \cdot \mu\text{m}^2$ , for devices with diameter from 100nm to 50nm. This however could be attributed to fabrication variations, where it is harder to control the precise area of smaller devices.



as the magnetic field was swept. The shorting could have been caused by inter-diffusion of metals into the MgO, lowering the resistance and basically eliminating any TMR.

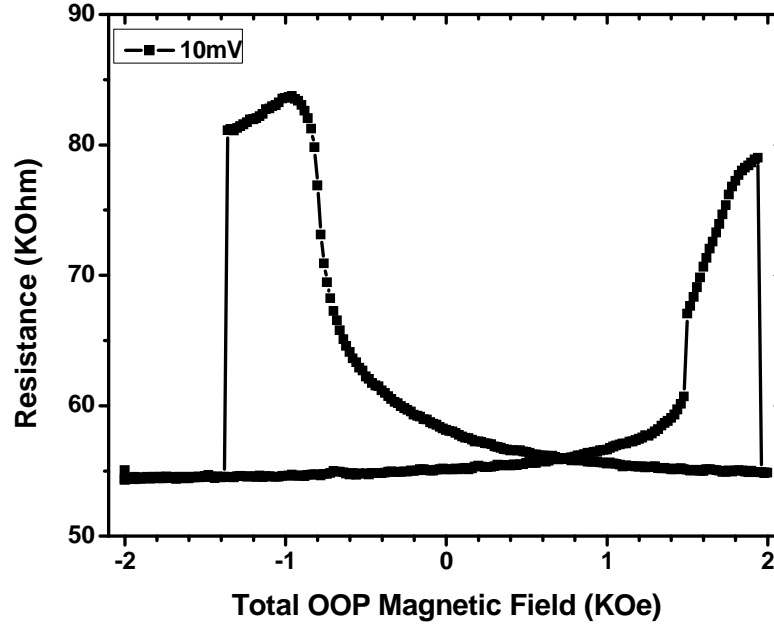
Switching experiments were attempted on these devices, and it was found that the breakdown voltage was as low as 2.4V, and shorts could even happen for just a few pulses at 2.1V, and one device actually shorted after a few pulses at 1.5V. The MgO thickness for the devices was around 1.28nm, a little thicker than the Ta devices, making the RA of these devices higher than that of the Ta devices, around  $255 \Omega \cdot \mu\text{m}^2$  for 60nm diameter devices, and  $276 \Omega \cdot \mu\text{m}^2$  for 80nm diameter devices. That should only have made the devices less susceptible to breakdown, due to less current running through the device, since the MgO was sputtered in the same method. The critical breakdown current density is only around  $7.6 \cdot 10^{-9} \text{ A/m}^2$ , for the 80nm devices. The exact reason for this much lowered critical breakdown current still requires more investigation.

Because breakdown voltage is so low, only voltages under 2V can be reliably used for switching. With the larger PMA, switching voltage is expected to be larger than that of Ta, thus it's predicted that switching will be very bad because the voltage is not high enough. Actual switching experiments have demonstrated what was expected, bad switching before breaking down.

### **Section 3.2.2: VCMA Coefficient**

VCMA was measured by choosing devices past the transition thickness which had free layers which are mostly in-plane, and applying an out of plane field to saturate it in P or AP direction. The magnetic field could only saturate the magnetization in one direction, if an out of plane magnetic field opposite to the direction of the fixed layer, it was likely to switch as well. Figure 30 shows a representative major RH loop of a device chosen for VCMA coefficient experiments.

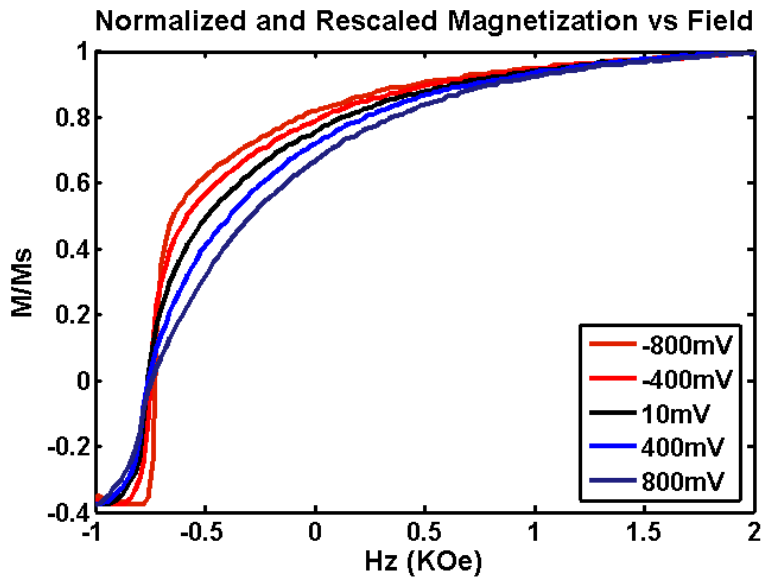
The same resistance change in the AP state is apparent in this device as in the perpendicular devices. We can only assume that it is also due to the fixed layer rotating before abruptly switching.



**Figure 30 shows a representative RH loop for an in-plane free layer device for the calculation of the VCMA coefficient. The change in resistance in the AP state is exhibited in these devices as well, further proof that it is the fixed layer that is rotating. On the positive applied field, the free layer shows a small switch near 1500 Oe instead of rotating smoothly, indicating that it is still not fully in-plane.**

After converting the RH loops to conductance-field (GH) and finally magnetization  $M_z$ /M-field, we normalized the magnetization by taking the magnetization at which the curve intersects for different voltages as  $M_z/M=0$ , and calculated the area starting there. This process is shown in Figure 31. Each curve represents data collected at a different applied voltage. From the figure it is apparent that the intersection point of the curves at different voltages is not zero. This could mean that the free layer magnetization is not fully in-plane at the average of the normalized magnetization, or possibly that the fixed layer is somehow rotating under an out-of plane field, which was also hypothesized to be the cause of the AP resistance change in the major RH loops.

However the exact origin of this offset is still under discussion. By taking a general average of the ‘origin’, this device yielded values of around  $30 \text{ fJ}/(\text{Vm})$ , comparable to the VCMA of Ta seed devices.



**Figure 31 shows the normalized MH curves used for the calculation of the VCMA coefficient. The magnetic anisotropy energy is the area between the curve, the saturation magnetization, and the field at which the curves intersect.**

## Chapter 4: Conclusion and Further Work

In summary, two device stacks were characterized, one with Ta and the second with Hf seed layers, with an emphasis on the write error rates of the Ta devices. An experimental setup for quickly recording switching trial results was built and coded. For devices with Ta seed layers, the write error rates were found to be limited to above  $10^{-4}$ , possibly due to internal factors like low thermal stability, high damping factor, or external factors like too high in-plane field. That caused the precession period to decrease, which may have caused additional decoherence in the free layer. The Hf seed layer improved the PMA compared to the Ta devices, as expected, but the combination of comparable VCMA coefficient to Ta devices, as well as an extremely low breakdown voltage of around 2V, switching experiments were not possible for these devices. However the TMR of Hf devices surpassed Ta, and the high PMA leaves room for more improvement with further annealing.

Areas of further work include the continued characterization of write error rates of Ta devices with thicker free layer, as well as continued experiments for the switching voltage of devices at different sizes, to confirm the trend predicted theoretically. Other questions include the strange rotation of the fixed layer in an external magnetic field, when it should be extremely perpendicular. It could also be interesting to look into the reason for the 500 Oe offset of the offset fields in the Hf devices.

From a bigger picture, new methods of switching the free layer magnetization reliably and with low energy should always be a priority. Materials engineering to improve the TMR and PMA of MTJs would be extremely helpful for magnetic memories, no matter what switching mechanism.



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