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Computational Model of Graphenen-Based Logic Gates and Architectures

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Computational Model of Graphenen-Based Logic Gates and Architectures

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ABSTRACT OF THE THESIS

Computational Model of Graphenen-Based Logic Gates and Architectures

by

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Dr. Alexander Balandin, Chairperson

Depend on a number of unique properties, graphene is beneficial for microelectronic devices. To design logical gates using graphene without bandgap is a chanllenge. As a result, "conventional" design for construction is required to make this breakthrough. The theory of negative differential resistance is used in this design to build logical gate with gapless graphene. The absence of a band gap makes graphene utilization in digital logic circuits problematic due to the power dissipation issue. On the other hand, the unique properties of graphene-based devices such as a high mobility and non-linear output characteristics may be utilized in non-Boolean logic circuits for special task data processing. It would be of great practical benefit to develop graphene-based analog logic circuits able to complement of complementary metal-oxide semiconductor (CMOS) technology in doing specific operations, which require enormous resources for the conventional digital counterparts (i.e. image recognition and image processing). In this

Section, we propose and discuss several special task grpahene-based logic circuits and illustrate their operation by numerical modeling.

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INTRODUCTION

1.1 Introduction

1.1.1 Graphene

As shows in figure 1.1, graphene is one of the crystalline forms of carbon, besides diamond, graphite, carbon nanotubes and fullerenes. In graphene, carbon atoms are arranged in flat two dimensional hexagonal patterns. Graphene can be described as a one-atom thick layer graphite which usually 0.5 nm. High quality graphene is very strong, light, nearly transparent, an excellent conductor of heat and electricity. Its inherently two-dimensional nature and carbon properties produce unique properties [1].

Many researchers studying carbon nanotubes were already well familiar with the composition, structure and properties of graphene which had been calculated decades earlier. The combination of familiarity, extraordinary properties and surprising ease of isolation enabled an explosion in graphene research. The Nobel Prize in Physics for 2010 was awarded to Andre Geim and Konstantin Novoselov at the University of Manchester "for groundbreaking experiments regarding the two-dimensional material graphene" [2].

Graphene differs from most conventional three-dimensional materials. Intrinsic graphene is a semi-metal or zero-gap semiconductor [1]. Understanding the electronic structure of graphene is the starting point for finding the band structure of graphite. It was realized as early as 1947 by P. R. Wallace [3]. that the energy-momentum relation (dispersion relation) is linear for low energies near the six corners of the two-dimensional hexagonal Brillouin zone, leading to zero effective mass for electrons and holes [4]. Due to this linear (or “conical") dispersion relation at low energies, electrons and holes near these six points, two of which are inequivalent, behave like relativistic particles described by the Dirac equation for spin-1/2 particles [5][6]. Hence, the electrons and holes are called Dirac fermions and the six corners of the Brillouin zone are called the Dirac points [5]. The equation describing the electrons' linear dispersion relation is

$$E=\hbar vf\sqrt{k_x^2+k_y^2} \qquad (1)$$

where the Fermi velocity is vF ~ 106 m/s, and the wave vector k is measured from the Dirac points (the zero of energy is chosen here to coincide with the Dirac points) [6].

Experimental results from transport measurements show that graphene has a remarkably high electron mobility at room temperature, with reported values in excess of 15,000 cm2·V−1·s−1 [1]. Additionally, the symmetry of the experimentally measured conductance indicates that the mobilities for holes and electrons should be nearly the same [4]. The mobility is nearly independent of temperature between 10 K and 100 K [7][8][9] which implies that the dominant scattering mechanism is defect scattering. Scattering by the acoustic phonons of graphene places intrinsic limits on the room temperature mobility to 200,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at a carrier density of 1012 cm^{-2} [9][10]. The corresponding resistivity of the graphene sheet would be 10^{-6} $\Omega \cdot cm$. This is less than the resistivity of silver, the lowest resistivity substance known at room temperature [11]. However, for graphene on SiO2 substrates, scattering of electrons by optical phonons of the substrate is a larger effect at room temperature than scattering by graphene's own phonons. This limits the mobility to 40,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [9].

Despite the zero carrier density near the Dirac points, graphene exhibits a minimum conductivity on the order of 4e2/h [1]. The exact minimum conductivity is unrevealed. However, rippling of the graphene sheet or ionized impurities in the SiO2 substrate may lead to local puddles of carriers that allow conduction [4]Several theories suggest that the minimum conductivity should be 4e2/πh); however, most measurements are of order 4e2/h or greater [1]. and depend on impurity concentration [12].

Recent experiments have probed the influence of chemical dopants on the carrier mobility in graphene [12][13] Schedin et al. doped graphene with various gaseous species (some acceptors, some donors), and found the initial undoped state of a graphene structure can be recovered by gently heating the graphene in vacuum. They reported that even for chemical dopant concentrations in excess of 1012 cm^2

there is no observable change in the carrier mobility [13]. Chen, et al. doped graphene with potassium in ultra-high vacuum at low temperature. They found that potassium ions act as expected for charged impurities in graphene [14]. and can reduce the mobility 20-fold [12]. The mobility reduction is reversible on heating the graphene to remove the potassium [1].

Due to its two-dimensional property, charge fractionalization (where the apparent charge of individual pseudoparticles in low-dimensional systems is less than a single quantum[15]) is thought to occur in graphene. It may therefore be a suitable material for the construction of quantum computers [16]. using anyonic circuits [17][18].

1.1.2 **Graphene-based electronic device**

Modern digital logic is based on Boolean algebra implemented in semiconductor switch-based circuits [19]. For more than fifty years, silicon complementary-metal-oxide semiconductor technology (CMOS) becomes more and more small on scale, and leads to increase performance of chips to improve information technology. However, as the electronic industry leaders are working on the sub 10-nm technology node, it is widely expected that the downscaling of Si CMOS technology will not last much further beyond 2020 [20]. The problem of heat dissipation and physical limitations of silicon are expected to end the “era of silicon” computer chips, which enabled progress in information technologies [19]. This fact motivates a search for alternative materials and computational paradigms that can, if not replace Si CMOS, then complement it in special-task information processing [19, 21, 22].

Since its first mechanical exfoliation [23] and discovery of its extraordinary high mobility at room temperature (RT) [24], graphene attracted attention as a potential candidate for future electronics. In addition to its high mobility, graphene reveals exceptional heat conduction properties [25], high saturation velocity [26], convenient planar geometry and capability for integration with virtually any substrate [27]. However, the absence of the energy band-gap, EG, in graphene means that graphene device cannot be switched off resulting in the high leakage currents and prohibitive energy dissipation [19]. A large number of research groups have attempted to solve this problem via application of an electric field [28, 29], quantum confinement of carriers in nanometer-scale ribbons [30], surface functionalization with various atoms [31, 32] and strain engineering [33, 34]. The outcome of these efforts was a modest band gap opening of few-hundred meV, which often came at the expense of strongly degraded electron mobility [19]. Practical applications of graphene in digital circuits would require a band-gap on the order of 1 eV at room temperature (RT) [19].

1.1.3 Negative differential resistance

Negative differential resistance (NDR) devices are electronic components with nonohmic current-voltage characteristics and are used in a wide array of applications including frequency multipliers, memory, fast switches, and most importantly, high-frequency oscillators up to the THz range [19]. Graphene field-effect transistors of “conventional” design as NDR device allows for construction of viable non-Boolean computational architectures with the gap-less graphene [19]. The negative differential resistance – observed under certain biasing schemes – is an intrinsic property of graphene resulting from its symmetric band structure [20].

The NDR effect in the dual-gate graphene field-effect transistors (G-FETs) and the means of controlling are its strength. The devices for this study are fabricated from mechanically exfoliated graphene on a Si/SiO2 substrate [35, 36]. Micro-Raman spectroscopy is the method to identify the samples of single layer graphene (SLG). The details of our micro-Raman procedures for graphene quality control were reported elsewhere [37, 38]. The source, drain, and gate regions made of Ti and Au are defined by the electron-beam lithography (EBL). The top-gate oxide is deposited using the two-layer method. The first layer is a thin film of evaporated Al, which is oxidized in air [19, 39]. The second layer is grown by ALD. The heavily doped Si substrate acts as the back-gate. Figure 1.2 shows a typical scheme image of the dual-gate G-FET. The NDR effect tuned by back gate voltage strength is shown in Figure 1.3.

1.1.4 **XOR gate**

A logic gate is an idealized or physical device implementing a Boolean function, that is, it performs a logical operation on one or more logical inputs, and produces a single logical output [40]. Therefore, an ideal or non-ideal physical logic gate can be built depend on the difference of the instant time.

In this work, I choose XOR gate as example to design circuit. Usually we need eight semiconductor diodes to build an XOR gate, but in this design we just need three graphene-based devices to achieve the equal gate. And serious connect 5 XOR gates to calculate hamming distance to show the possible outputs of the circuit.

The XOR gate (sometimes EOR gate, or EXOR gate) is a digital logic gate that implements an exclusive or; that is, a true output (1) results if one, and only one, of the inputs to the gate is true (1). If both inputs are false (0) or both are true (1), a false output (0) results. Its behavior is summarized in the truth table shown on the right. A way to remember XOR is "one or the other but not both" [40].

XOR represents the inequality function, i.e., the output is HIGH (1) if the inputs are not alike otherwise the output is LOW (0). XOR can also be viewed as addition modulo 2 [40]. As a result, XOR gates can be used as binary adder in computers.

1.1.5 **Matlab modeling**

MATLAB is a high-level language and interactive environment for numerical computation, visualization, and programming. Using MATLAB, you can analyze data, develop algorithms, and create models and applications [41]. The language, tools, and built-in math functions enable you to explore multiple approaches and reach a solution faster than with spreadsheets or traditional programming languages, such as C/C++ or Java™ [41].

Maybe Matlab is not the fastest execution program for your code, but in the process of doing a simulation; the bottle neck is the programming time. You need a program language can fast be coded. Matlab is famous for embedding numerous math functions and methods including Interpolation and regression, Differentiation and integration, Linear system and equation, Fourier analysis, Eigenvalues and singular values, Ordinary differential equations, and Sparse matrices. Moreover, the plot tool of Matlab is much better than other language, such as Python. One of the example is Python can only plot figures only once per script. At last, Matlab has almost 106 licensed users worldwide, and increase rapidly.

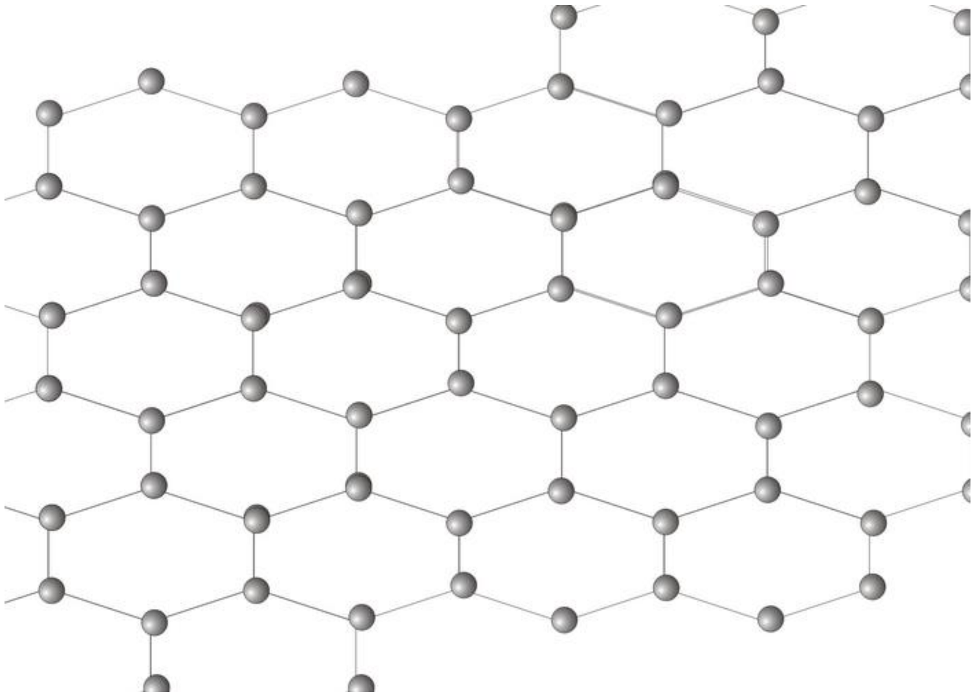

Figure 1.1 Graphene Crystal Structure.

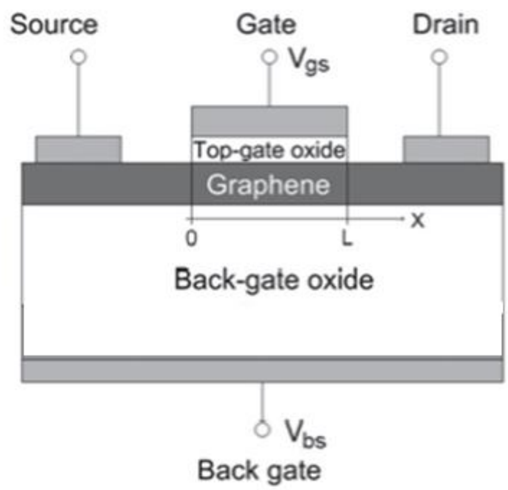

Figure 1.2 Structure of the dual-gate G-FET.

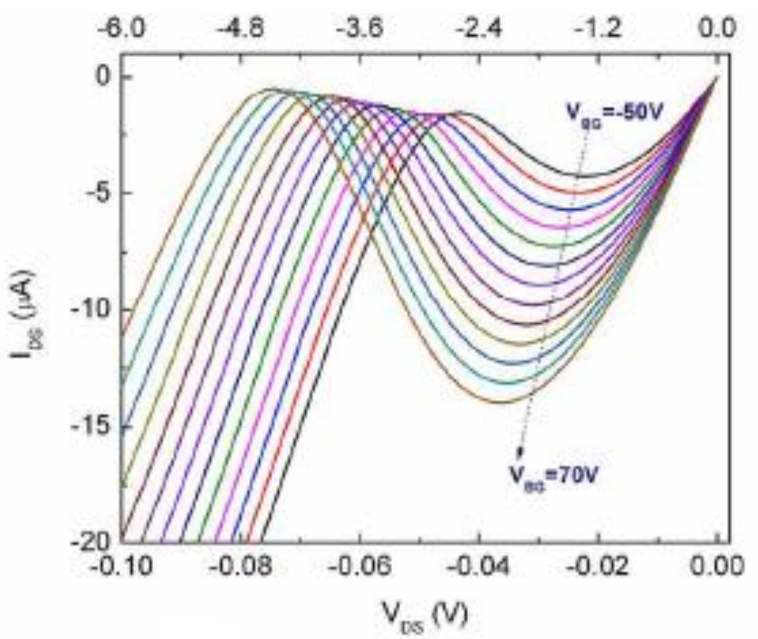

Figure 1.3 N-shape NDR in the dual-gate G-FET at the VBG=70V. (Liu, G. et al. (2013) " Graphene-Based Non-Boolean Logic Circuit". arXiv: 1308.2931.)

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2 Chapter 2

The Property of Graphene-Based Device, Logical Gates, and Architectures

2.1 Abstract

Granphene field effective transistor has been popular recently. Based on the numerous researches on the material, fabrication, and theory, we can achieve better and better device. As a result, the next step logical gates of the device application become useful grandly. Logical gates are the foundation of the binary computation, and semiconductor is used for transistor for decades' years. However the thermal conductivity and electrical property limit the improvement of the large scale transistor circuit. On the other hand, graphene transistor will be better replacement based on its better thermal conductivity and electrical property. We can use fewer cells to fabricate more complicated logical gates with better thermal property. Here I module logical gates and pattern circuit simulation with classical grapheme field effect transistor theory to show the computational results.

2.2 Introduction

The absence of a band gap makes graphene utilization in digital logic circuits problematic due to the power dissipation issue. On the other hand, the unique properties of graphene-based devices such as a high mobility and non-linear output characteristics may be utilized in non-Boolean logic circuits for special task data processing. It would be of great practical benefit to develop graphene-based analog logic circuits able to complement of complementary metal-oxide semiconductor (CMOS) technology in doing specific operations, which require enormous resources for the conventional digital counterparts (i.e. image recognition and image processing). Pattern matching is one of the examples, which is widely-used for database search, spell checking and signal processing tasks. The essence of the pattern matching operation is the checking if the stream of input data matches a reference one. The main challenge for this application is to perform high throughput operation to match the speed of the gigabit network. The inevitable development of 100 Gbps-scale data networks would make real time network intrusion detection impossible [1]. even using the most optimistic assumptions for scaling CMOS [2]. That is one of the cases where unique properties of graphene may be utilized to complement the existing technology. In this Section, we propose and discuss several special task grpahene-based logic circuits and illustrate their operation by numerical modeling [3,20]

2.3 Simulation

2.3.1 I_{DS}-V_{DS} characteristics of the diode connected graphene transistor

The experimentally observed NDR effect can be explained in relatively simple terms using the drift-diffusion model for current conduction in graphene. We define V_{DS} and V_{TG} to sweep zero simultaneously with a different step size M, $V_{TG} = MV_{DS} = V$. Since we observed that the NDR effects happens close to the Dirac point where the ns is roughly proportional to V_{TG}, we can write that $n_{TG}=C_{TG}(-V_{TG}+ V^0_{TG})/e$, where e is the elementary charge, C_{TG} is the capacitance of the top-gate. We choose here the p-type branch of graphene since this is the region where NDR appears. Thus, we use $(-V_{TG}+ V^0_{TG})$, where V^0_{TG} is the top-gate voltage at the Dirac point under a certain back-gate bias. We can write for the current I= $\frac{W}{L}[\sigma_s + \sigma_0]V_{DS}$, where $\sigma_s = \mu e n_{TG}$ is the conductivity controlled by the gate and σ_0 is the conductivity at the Dirac point. Thus, one

arrives with the following equation:

$$I=\frac{W}{L}[uC_{TG}(-V_{TG}+ V^0_{TG})+ \sigma_0]V_{DS} \qquad (2)$$

Plugging in the common values for our dual gate graphene devices, σ_0= 1/ 6kΩ, u=1000cm^2 /Vs CTG =0.94 uF / cm^2 for ~12 nm AlOx/HfO2 oxide stack and $V^0_{TG} = -2V$. [20]

In figure 2.1, there are shown three approximate I-V curves of the diode-connected graphene transistor at three different back gate voltages. In numerical simulations, we use the analytical expressions for IDS= $\frac{V}{\sqrt{{n_0}^2+(C_{back}(V_{bg}-V_{bg0})+C_{top}(V_0-V_{tg})}}$.

Without loss of generality, we assumed Cback=0.5Ctop and introduced a linear shift for the V_{tgs}^{0} as follows: V_{tgs}^{0} =1-0.5Vbgs. The current is shown in normalized units I0, where $I_0 = \frac{W}{2L}\mu e n_0 V_{bgs}^{0}$. There are two general trends in of I-V response to the back gate to capture: (i) the NDR regions shifts to the left with the increase of the back gate voltage, and (ii) the NDR regions shrinks as the back gate voltage increases. [3, 20]

2.3.2 Three terminal device

As a building block for logic gate construction, we consider a circuit combining two graphene transistors connected in series as shown in figure 2.2. It is a three terminal device, where the two back gates serve as the input terminals, and the common top gate serves as the output terminal. The output voltage depends on three parameters: Vdd, Vbg1, and Vbg2, which can be controlled independently. There may be one or two stable outputs depending on the combination of the control voltages. In figure 2.2(B), it is shown a color map of the possible output voltages depending on the two back-gate voltages Vbg1 and Vbg2 at fixed Vdd. The red color depicts the region in the 2D space where the output has two stable values. The dark blue and the light-blue color depict the regions of single-value output (e.g. blue color shows the “low” output Vout<0.5Vdd, or the “high” output Vout>0.5Vdd). The graphs in figure2.2(C) illustrate the possible scenarios for two I-V curves intersection leading to the single- or bi- stable output.

The device shown in figure 2.2(a) is a four terminal device two back gate inputs, control gate (Vdd) and the output. Such a multi-terminal device can be used as a base block for building a variety of logic gates. It should be noted that a double gate transistor itself is a powerful a tool for circuit engineering, which has been attracting great interest from the early days of semiconductor devices (e.g. the “Unipolar ‘Field Effect’ Transistor” proposed by Shockley in 1952 [3]). The independent control of two gates allows for significant increase of the logic functionality per transistor and overall logic density per area enhancement. For example, NAND and NOT gates can be implemented within a one transistor circuit and more complicated logic circuits (e.g. bit-adders) can be realized with a fewer number of elements than required for standard CMOS-technology [4]. In case of the multi-gate graphene device, AND and OR gates can be realized by the proper choice of the input voltages V1 and V2 applied to the back gates as well as by the choice of the Vdd as illustrated in figure 2.2(b).

With different back voltage combination, we can get single, bi stable state. Even tri-stable state, but the third stable state cannot stay stable for long time. We can see, the single-stable (figure 2.3) and bi-stable (figure 2.4) perform well robust. But the tri-stable state (figure 2.5) will transfer to bi-stable after few seconds. The different type of state can be localized in the figure 2.2(b).

2.3.3 XOR gate

More promising is the implementation of the graphene multi-gate device for complex logic circuits such as XOR gate, which requires minimum eight transistors in CMOS. This gate can be constructed with just three graphene transistors as shown in figure 2.6. Two input voltages V1 and V2 are applied to the back gates of the first stage transistors, where V1 and V2 correspond to logic 0 and 1 respectively. It is possible to find a pair of voltages providing the same output Vout if and only if V1= V2 (logic inputs 00 and 11). Then, the output voltage is applied to the back gate of the second stage graphene transistor. The output voltage corresponding to 00 and 11 states is matched to the Dirac point providing minimum conductivity. Overall, such a device provides minimum current if and only if two input signals coincide. In order to do pattern matching, the number of such devices can be connected in series as shown in figure 2.6. The two inputs of each device are aimed to receive input voltages corresponding to the input and the reference data string (i.e. all odd inputs receive input data and all even inputs receive the reference data). The upper transistor is in the Off state if the input and reference data are the same and the upper transistor is in the On state otherwise. The current flowing through the upper transistors decreases with the decrease of the Hamming distance among the input and reference data strings. It has absolute minimum in the case of the perfect match where zeros and ones of the input data matches zeros and ones of the reference data.

The graphene-based pattern matching circuit shown in figure 2.6 has several important advantages in terms of area, speed and overall functional throughput over the existing circuits. One hand, the elementary XOR gate requires only three transistors, where the area per graphene transistor can be as small as 10nm×40nm [5]. All XOR gates are connected in series to the common sensing line allowing for parallel data read-in. On the other hand, the operation frequency of the graphene transistor can be as high as 427GHz [6]. The maximum pattern matching throughput defined as Nbitsfmax/Acell may exceed 1021bits/s/cm2 , which is orders of magnitude higher than any reported or even projected scaled circuits [2]. This example illustrates the possibility of building special task analog logic circuits which can significantly outperform CMOS in one specific application.

2.3.4 XOR gate circuit

In the figure 2.7, we map the total possible value for all combination of input1 and input2. In the red region, the value is high to 50 more. And in the blue region, the value starts from -10. To achieve a good performance of XOR, we try to find 4 points (00, 01, 10, 11) to form a square which two points have the same value (V00=V11< V01=V10). Unfortunately, it is hard to find those perfect 4 points to make a XOR gate. As a result, V00=V11< V01<V10 were chosen instead of V00=V11< V01=V10. The exact value of the 4 points was shown in the table.

After set value for the XOR gate, a pattern circuit including 5 XOR gates was series connected together to calculate the hamming distance in the simulation. The result shows in the figure 2.9. In the figure, there are multiple points appear around some values, because of the slight difference between V00 and V11.

2.3.5 Non-Boolean logic architectures

Bi-stability is another property of the graphene transistor with NDR, which is of great potential of building non-Boolean logic architectures (e.g. non-linear networks). The concept of non-linear network based on the devices with RTD [7]. is well-known example of a non-Boolean approach. However, the most interest so far has been focused on the tunneling diodes, which are two-terminal devices. The utilization of the diode-connected graphene transistor offers a three-terminal device with RTD. The latter opens a new horizon for building non-linear networks with enhanced logic capabilities. In this work, we present an example of a non-linear network exploiting the unique characteristics of the graphene transistor. In Fig.4(A), it is shown a circuit combining three layers (stages) of graphene transistors, where each layer consists of two graphene transistors connected in series. Each stage is biased by a separate Vdd, which value may vary from stage to stage. The input voltages are applied to the back gates of the transistors. The top gates of each stage are connected to the one of the back gates of the next stage as shown in figure 2.8. The main idea is to make use of the bi-stable outputs provided by each stage and to build a multi-valued logic unit. The results of numerical modeling in figure 2.10-2.12 illustrate the output values (black markers) after each stage as well as the ensemble of output values after the last stage. In this example, all inputs are chosen to have either 0.5V0 or 1.9V0 (this combination leads to the bi-stable output at Vdd=3.0V as shown in Fig.2(C)). Thus, the output of Stage 1 may have 5 possible stable values for four possible input combinations. The number of possible output values depends on the inputs as well on the Stage bias voltage Vdd. The results of numerical modeling in Fig.4(B-D) illustrate three evolution trees for different combinations of the stage Vdd. We intentionally use the input and Vdd values leading to the increase number of the output states. At some point, the patterns shown in Fig.4 resemble the operation of the cellular automata [8], where the existence or absence of the stable output in the certain value interval is analogous to the logic 0 or 1. The presented network built of graphene transistors can be evolved in a number of ways (e.g. by increasing the number of transistors per stage, by introducing a time-varying bias voltage Vdd(t), by increasing the number of interconnects among the stages, etc.) Without any doubt, a three-terminal device with RTD is a powerful building block for non-linear network construction. Image recognition, data encryption, database search are among the most urgent applications to benefit from the CNN implementation.

2.4 Conclusions

In conclusion, we demonstrated that the negative differential resistance experimentally observed in graphene field-effect transistors allows for construction of viable non-Boolean computational architectures. The proposed approach overcomes the absence of the energy band gap in graphene. The negative differential resistance appears not only in the large scale grapheme transistors but also in the downscaled devices operating in the ballistic transport regime. Our results may lead to a conceptual change in graphene research proving an alternative route for graphene's applications in information processing.

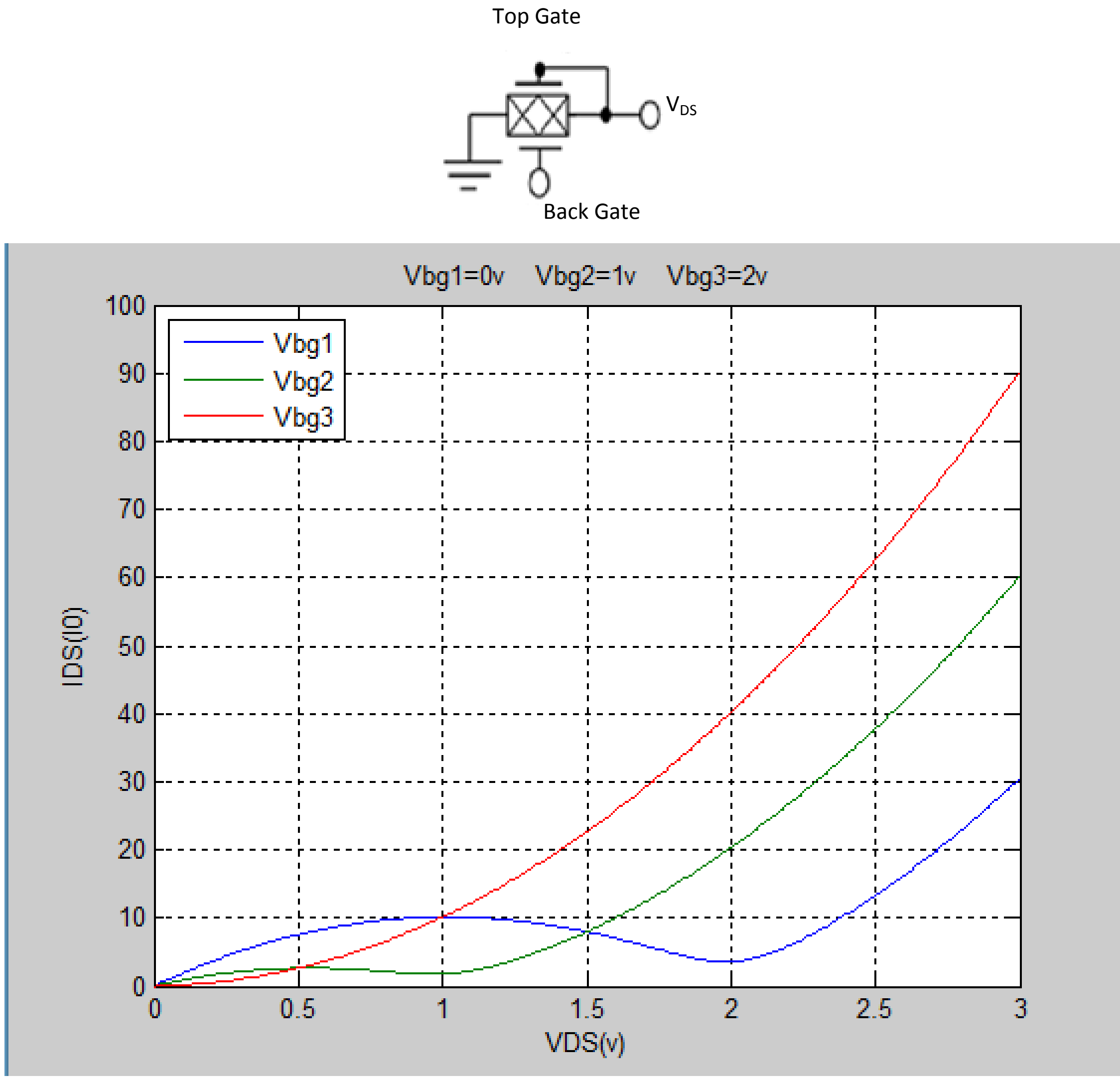


Figure 2.1 Approximate I_{DS}-V_{DS} characteristics of the diode-connected graphene transistor under different VBG. The increase of the back gate voltage shrinks the NDR region and shifts it to the left.

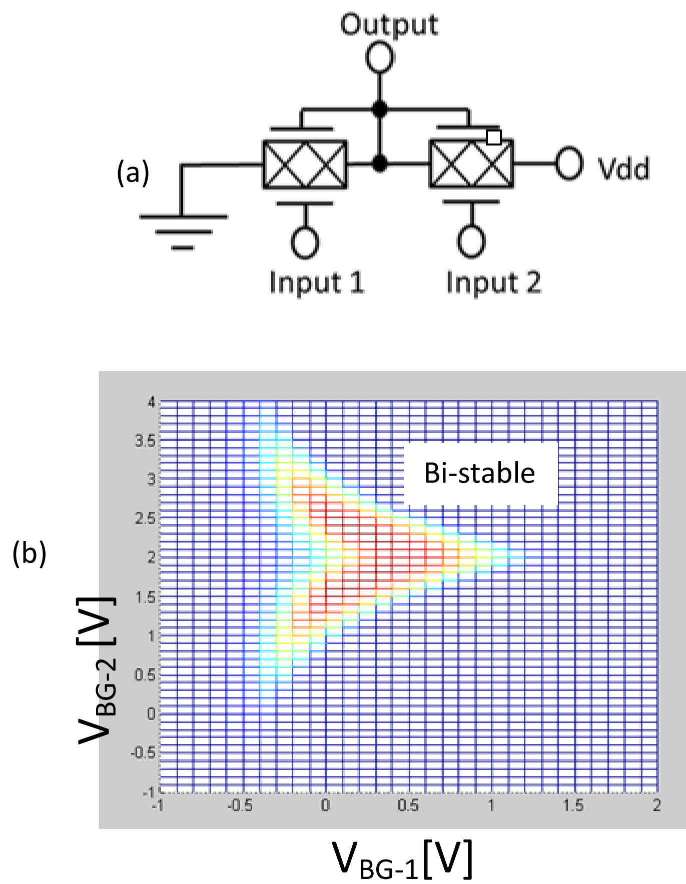
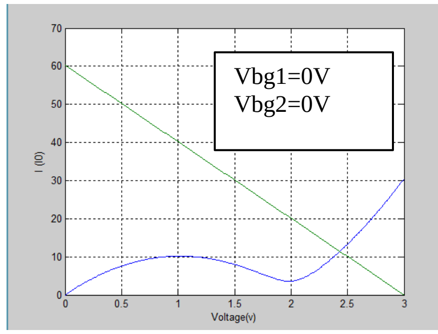


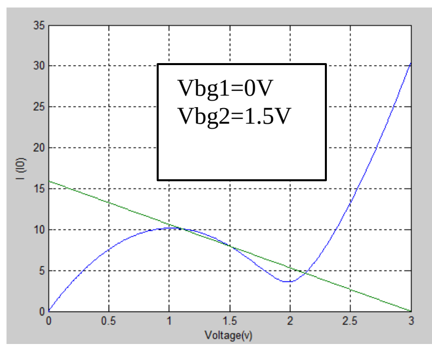
Figure 2.2 (a) Schematics of the circuit compromising two grapheme transistors. The back gates serve as the input terminals, and the top gate serves as the output terminal. (b) Results of numerical simulations: the color map of the output for different back-gate voltage VBG-1 and VBG-2 at fixed Vdd. The red and the blue regions depict the bi-valued and single-valued output, respectively. The blue color show “low” or “high” output (Vout<0.5Vdd or Vout>0.5Vdd).

(c)

Single
State



Bi-stable
State



Single
State

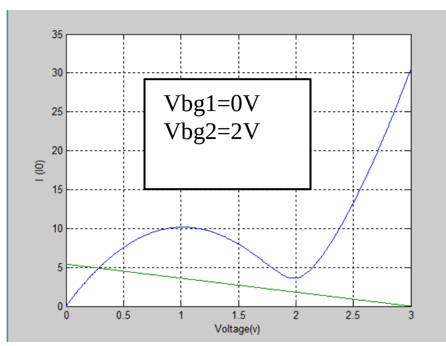


Figure 2.3 (c) Possible combinations of the input voltages V_{BG-1} and V_{BG-2} leading to the single- and bi- stable output. The single-valued regions can be used for Boolean logic gate construction, while the bi-valued regions are of great promise for non-Boolean logic circuitry (e.g. cellular non-linear network).

Table 2.1 Table of Graphene-Based XOR Gate

Input1	Input2	Output-Current	(A)
0	0	Low	6.3
0	1	High	30
1	0	High	13
1	1	Low	5.4

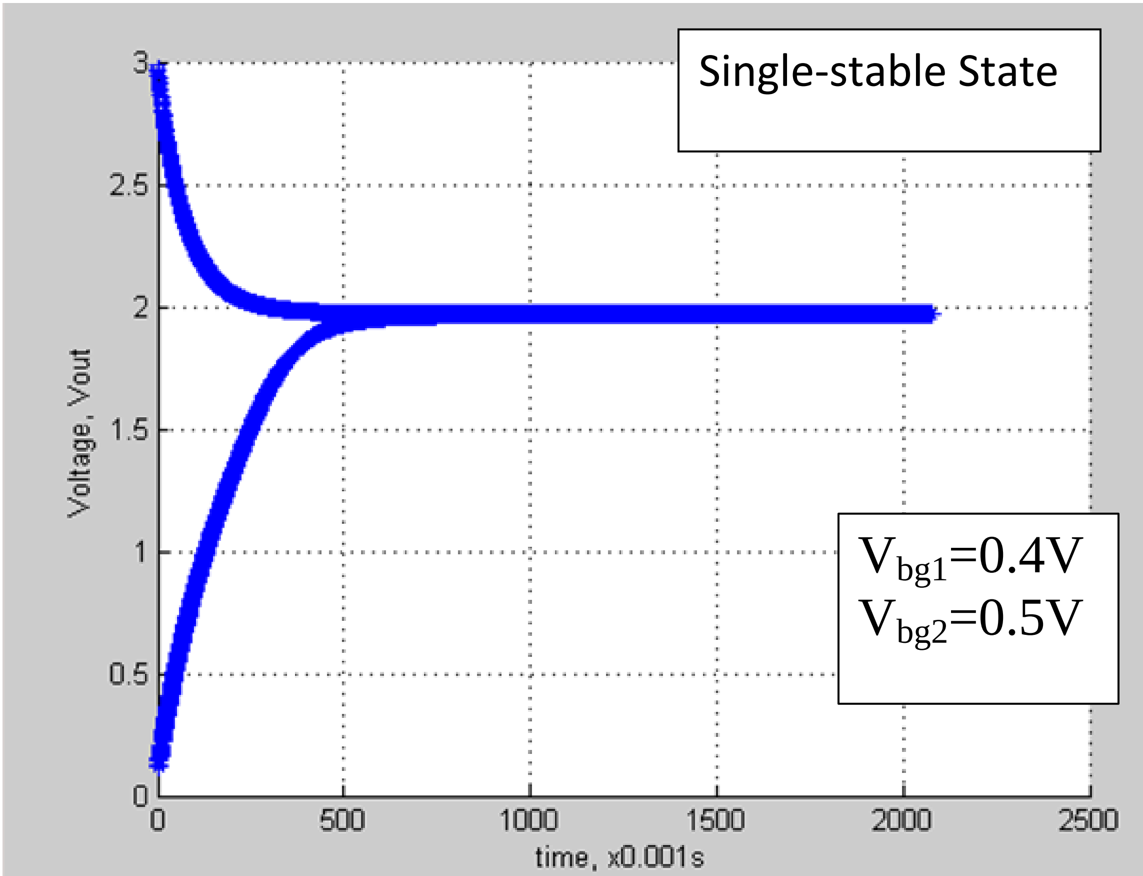


Figure 2.4 Single-stable State with V_{bg1}=0.4V and V_{bg2}=0.5V.

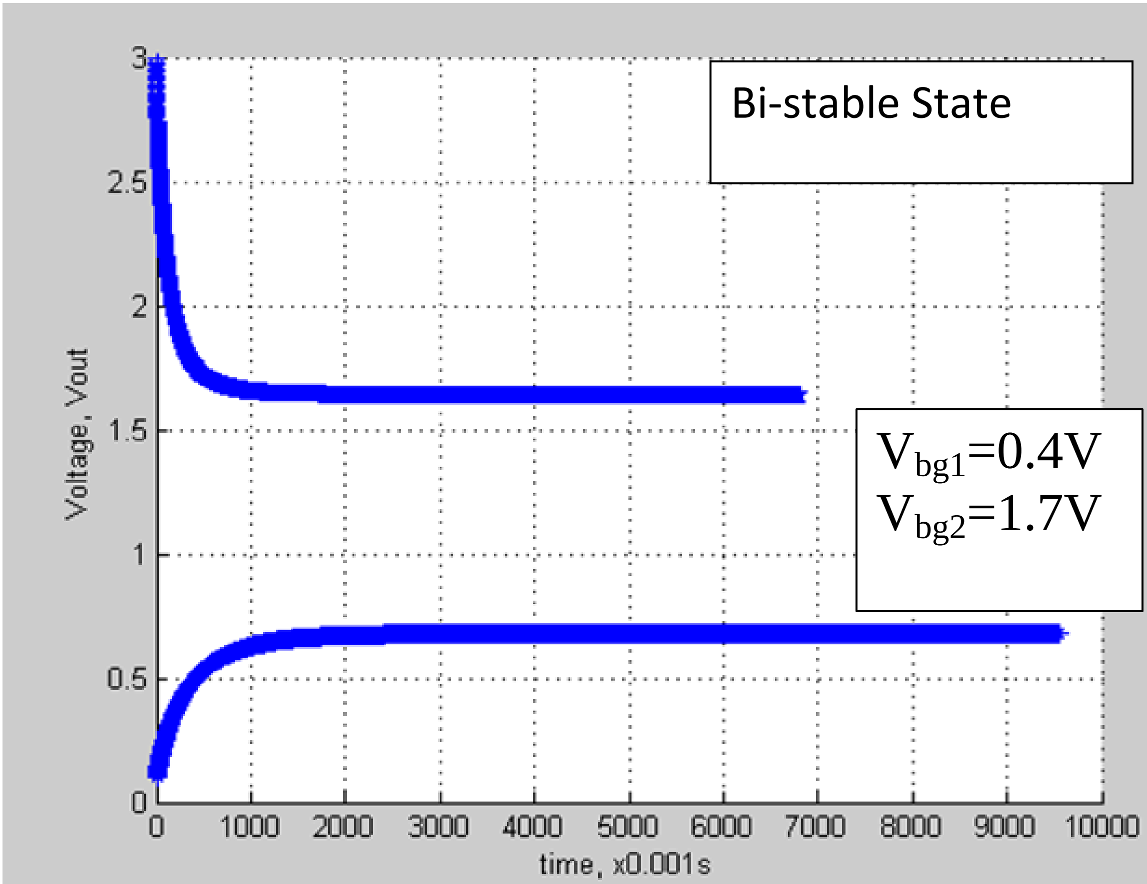


Figure 2.5 Bi-stable State with V_{bg1}=0.4V and V_{bg2}=1.7V.

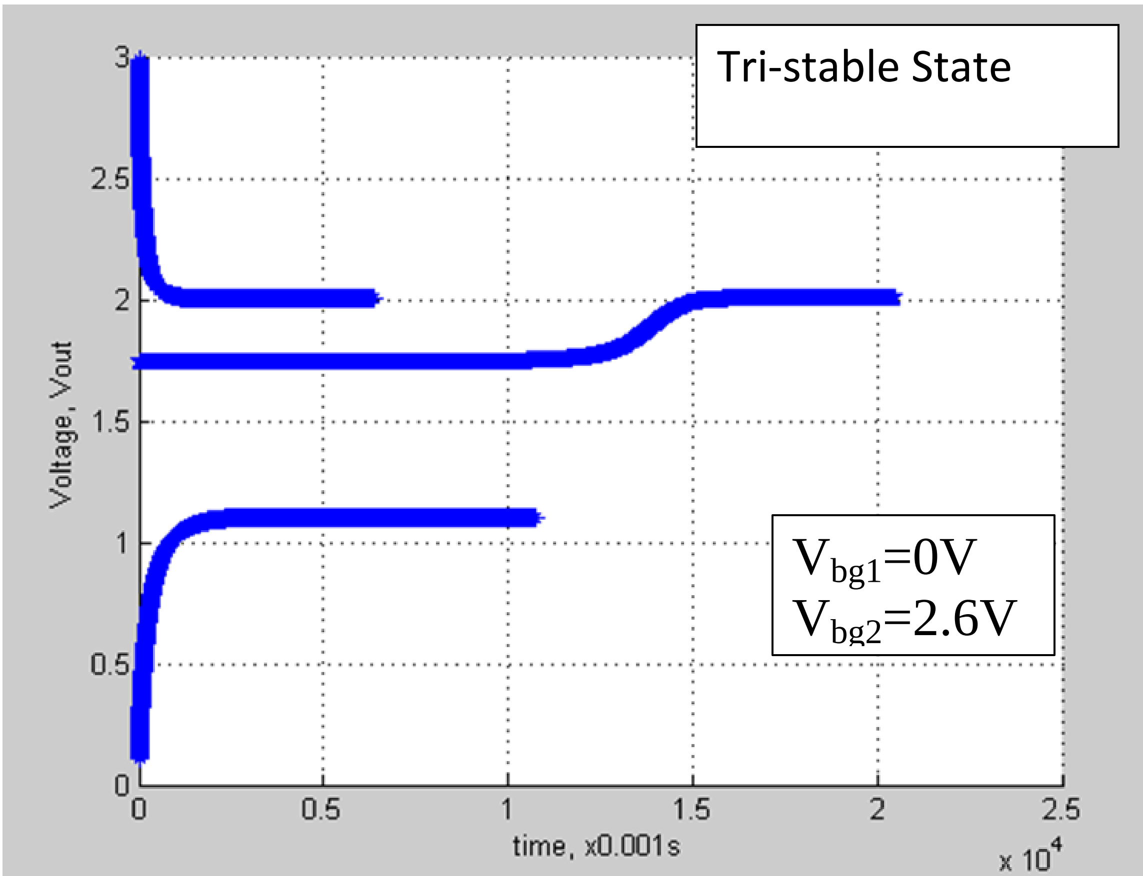


Figure 2.6 Tri-stable State with V_{bg1}=0V and V_{bg2}=2.6V.

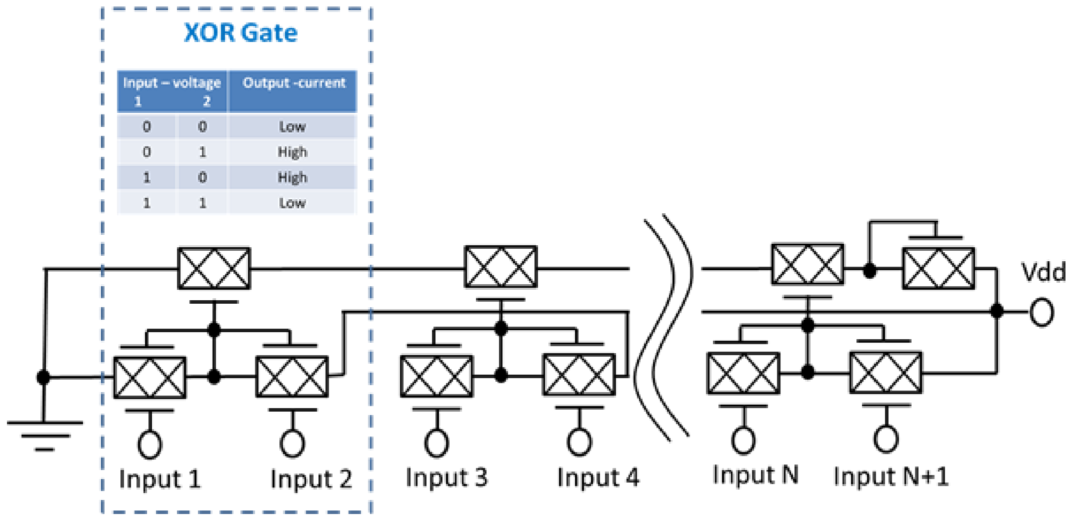


Figure 2.7 Schematics of the pattern matching circuit built of grapheme transistors. An elementary cell consists of three grapheme transistors arranged in a two stage circuit. The input data are applied to the two inputs of the first stage transistors. The input Voltage V_1 and V_2 represent two logic states 0 and 1. The values of the input voltages are found to provide the same output if and only if $V_1 = V_2$ (logic states 00 and 11). The output voltage of the first stage is then applied to the back gate of the second stage transistor. The output voltage corresponding to 00 and 11 states is matched to the Dirac point providing minimum conductivity. Overall, the elementary cell acts as a XOR gate providing minimum current for 00 and 11 inputs. The circuit consists of a number of cells, where each cell receives one bit of the input data and one bit of the reference data.

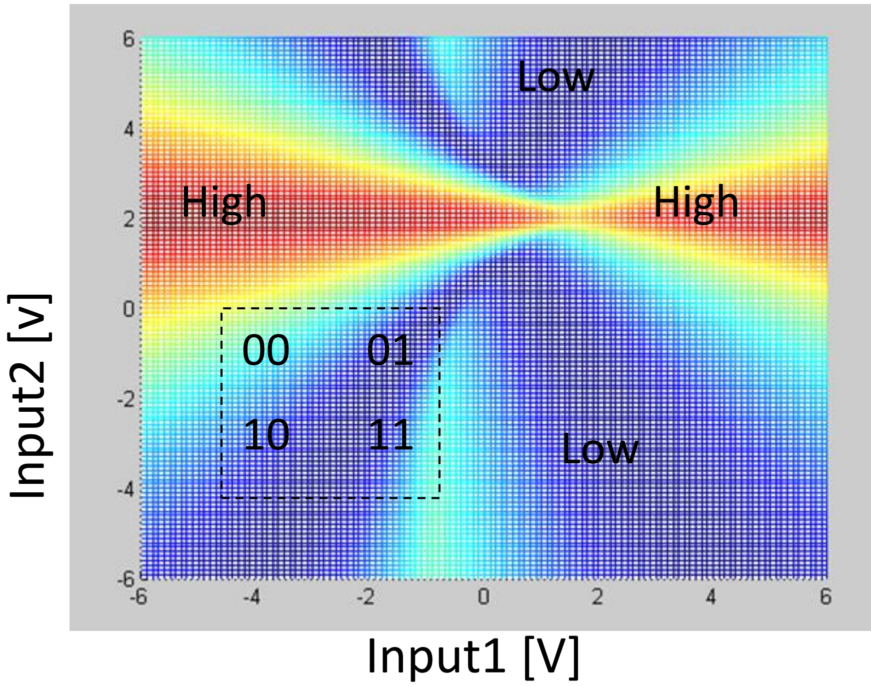


Figure 2.8 The color contour is mapping the Output value of the XOR Gate.

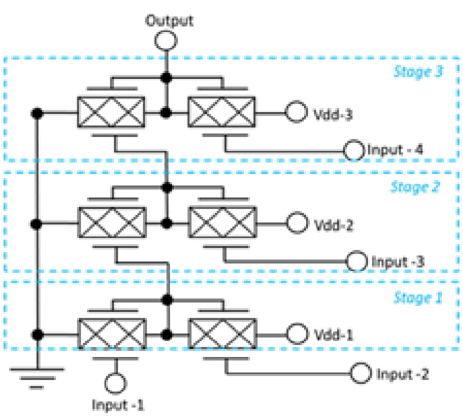


Figure 2.9 Network consisting of three stages of grapheme transistors. Each stage is biased by a separate Vdd. The input voltages are applied to the back gates of the transistors. The top gates of each stage are connected to the one of the back gates of the next stage. (Liu, G. et al. (2013) " Graphene-Based Non-Boolean Logic Circuit". arXiv: 1308.2931.)

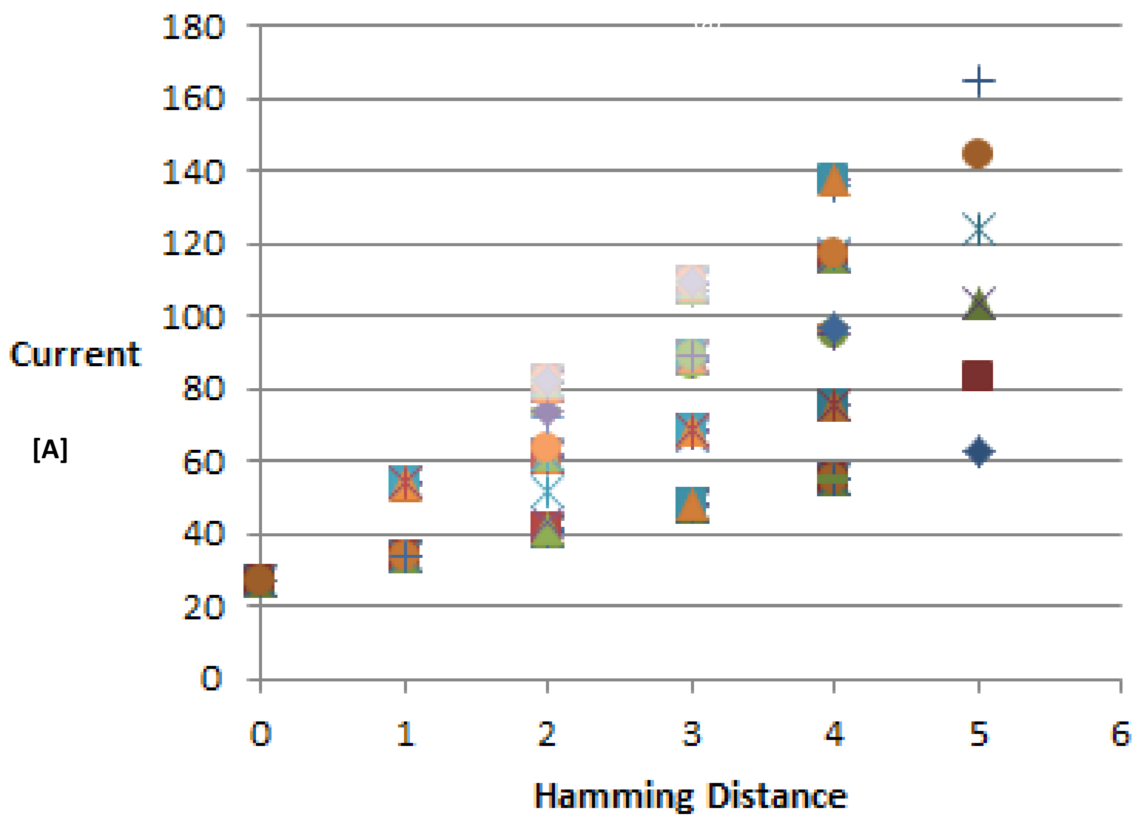
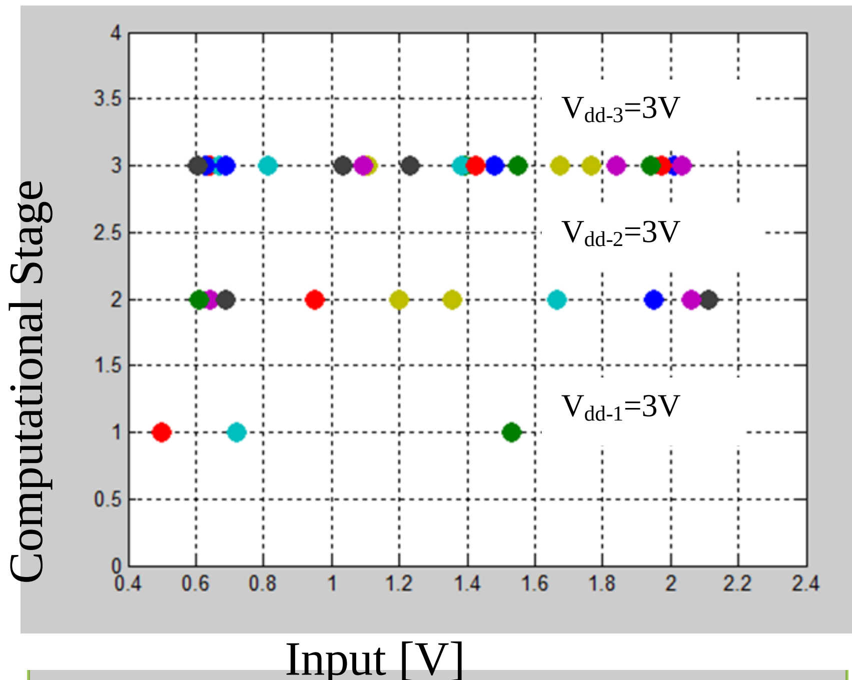


Figure 2.10 Hamming distance of the 5 series connected graphene XOR gates.

(a)



(b)

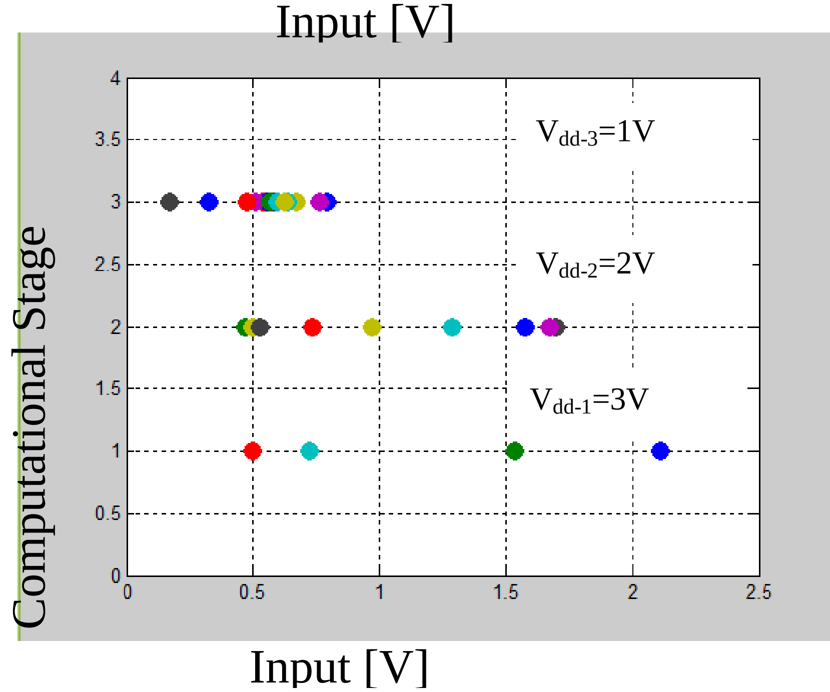


Figure 2.11 Result of numerical modeling illustrating the evaluation trees for output voltage at combinations of the stage V_{dd} (a) and (b).

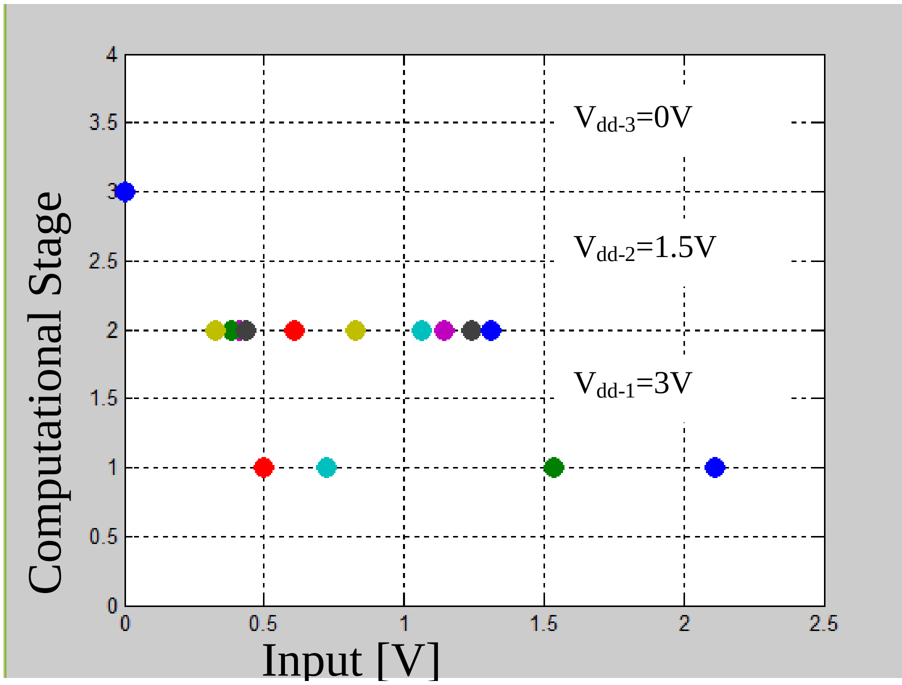
(c) 

Figure 2.12 Result of numerical modeling illustrating the evaluation trees for output voltage at combinations of the stage V_{dd} (c).

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Chapter 3 (Appendix)

Code and Explaination

3.1 Abstract

To make this matlab simulation, I started from writing code of the double gate graphene device. And then I connected two devices together to get the NDR region. In the process, I use nonlinear method to calculate the current through the two devices with certain source-drain voltage and gate voltage. I set time step to adjust the feedback until the current difference of the two device smaller than 0.000001 A. Based on the two device circuit, another single gate graphene device was added to model a XOR gate. With the computational property of the XOR gate, 5 XOR gate cells were series connected to build up the pattern circuit. I will explain every step of the simulation with my matlab code.

3.2 Introduction

The following explanation and code include the NDR region, stable states, XOR gate, hamming distance, and stage tree evaluation.

3.3 Simulation Details

3.3.1 NDR of diode-connected graphene

The code of diode-connected graphene NDR showed in the figure 2.1.

```
V1=3

V0=0:0.01:V1;

Vdd=0:0.01:V1;

Vbg1=0;

Vbg2=2;

Vbg3=1;

Vbg4=2;

Cb=5;

Ct=10;

V111=0.01;
```

```
Csum=1/((1/Cb)+(1/Ct));

a1=1.8^2+(Cb.*(Vbg1-2)+Ct.*(V0-(1-0.5*Vbg1))).^2;

a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V0-V0)-(1-0.5*Vbg2))).^2;

I11=((a1.^(0.5))).*(V0);

I22=((a2.^(0.5))).*(V1-V0);

a3=1.8^2+(Cb.*(Vbg3-2)+Ct.*(V0-(1-0.5*Vbg3))).^2;

I33=((a3.^(0.5))).*(V0);

a4=1.8^2+(Cb.*(Vbg4-2)+Ct.*(V0-(1-0.5*Vbg4))).^2;

I44=((a4.^(0.5))).*(V0);

plot(Vdd,I11,Vdd,I33,Vdd,I44)

xlabel('Voltage(v)')

ylabel('I (I0)')

grid on
```

3.3.2 Bi-stable state color map

The code of Bi-stable state color map showed in the figure 2.2 (b).

```
M=1

N=1;

V0=0.1

V1=3

Vdd=2.5;

Vbg1=-6:0.1:6;

Vbg2=-6:0.1:6;

[x,y]=meshgrid(Vbg1,Vbg2)

Cb=5;

Ct=10;

Csum=1/((1/Cb)+(1/Ct));

a1=1.8^2+(Cb.*(x-2)+Ct.*(V0-(1-0.5 .*x))).^2;

a2=1.8^2+(Cb.*(y-2)+Ct.*((V0-V0)-(1-0.5 .*y))).^2;

I11=((a1.^(0.5))).*(V0);

I22=((a2.^(0.5))).*(Vdd-V0);

Isum=-I11+I22
```

```
dV=Isum./Csum;

f=(dV.^2).^0.5;

 dt=0.00001

 V0=V0+dV*dt;

f=0.01

while f>0.0000001

a1=1.8^2+(Cb.*(x-2)+Ct.*(V0-(1-0.5 .*x))).^2;

a2=1.8^2+(Cb.*(y-2)+Ct.*((V0-V0)-(1-0.5 .*y))).^2;

I11=((a1.^(0.5))).*(V0);

I22=((a2.^(0.5))).*(-V0+Vdd);

Isum=-I11+I22;

dV=Isum./Csum;

f=(dV.^2).^0.5;

V0=V0+dV*dt;

M=M+1;

end
```

```
M=1

a1=1.8^2+(Cb.*(x-2)+Ct.*(V1-(1-0.5 .*x))).^2;

a2=1.8^2+(Cb.*(y-2)+Ct.*((V1-V1)-(1-0.5 .*y))).^2;

I11=((a1.^(0.5))).*(V1);

I22=((a2.^(0.5))).*(Vdd-V1);

Isum=-I11+I22;

dV=Isum./Csum;

f=(dV.^2).^0.5;

 dt1=0.00001

 V1=V1+dV*dt;

ff=0.001

while ff>0.000001

a11=1.8^2+(Cb.*(x-2)+Ct.*(V1-(1-0.5 .*x))).^2;

a22=1.8^2+(Cb.*(y-2)+Ct.*((V1-V1)-(1-0.5 .*y))).^2;

I1=((a1.^(0.5))).*(V1);

I2=((a2.^(0.5))).*(-V1+Vdd);
```

```
Is=-I1+I2;

dV1=Is./Csum;

ff=(dV1.^2).^0.5;

V1=V1+dV1*dt1;

N=N+1;

end

z=((-V0+V1).^2).^0.5

mesh(Vbg1,Vbg2,V0)
```

3.3.3 Stable states

The code of single- or Bi-stable states showed in figure 2.3, 2.4, and 2.5.

```
V0=0.1

V1=3

Vdd=2.5

Vbg1=1;

Vbg2=2;

Cb=5;
```

```
Ct=10;

Csum=1/((1/Cb)+(1/Ct));

a1=1.8^2+(Cb.*(Vbg1-2)+Ct.*(V0-(1-0.5 .*Vbg1))).^2;

a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V0-V0)-(1-0.5 .*Vbg2))).^2;

I11=((a1.^(0.5))).*(V0);

I22=((a2.^(0.5))).*(Vdd-V0);

Isum=-I11+I22

dV=Isum./Csum;

f=(dV.^2).^0.5;

 dt=0.001

V0=V0+dV*dt;

while f>0.0000001

a1=1.8^2+(Cb.*(Vbg1-2)+Ct.*(V0-(1-0.5*Vbg1))).^2;

a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V0-V0)-(1-0.5*Vbg2))).^2;

I11=((a1.^(0.5))).*(V0);

I22=((a2.^(0.5))).*(-V0+Vdd);
```

```
Isum=-I11+I22;

dV=Isum./Csum;

f=(dV.^2).^0.5;

V0=V0+dV*dt;

M=M+1;

   % end

 hold on

 plot(M,V0)

end

a1=1.8^2+(Cb.*(Vbg1-2)+Ct.*(V1-(1-0.5 .*Vbg1))).^2;

a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V1-V1)-(1-0.5 .*Vbg2))).^2;

I11=((a1.^(0.5))).*(V1);

I22=((a2.^(0.5))).*(Vdd-V1);




Isum=-I11+I22;
```

```
dV=Isum./Csum;

f=(dV.^2).^0.5;

M=1

 dt=0.001

V1=V1+dV*dt;

while f>0.0000001

a1=1.8^2+(Cb.*(Vbg1-2)+Ct.*(V1-(1-0.5*Vbg1))).^2;

a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V1-V1)-(1-0.5*Vbg2))).^2;

I11=((a1.^(0.5))).*(V1);

I22=((a2.^(0.5))).*(-V1+Vdd);

Isum=-I11+I22;

dV=Isum./Csum;

f=(dV.^2).^0.5;

V1=V1+dV*dt;

M=M+1;

   % end
```

```
  hold on

  plot(M,V1)

end
```

3.3.4 The color contour of the output value of the XOR gate

The code in fact is 3-D model of the output value of the XOR gate, the figure 2.7 is the top view of the 3-D model

```
Input1=0

Input2=6

Vbg1=-7.5:0.1:4.5;

Vbg2=-6:0.1:6;

[x,y]=meshgrid(Vbg1,Vbg2)

Vdd=3

V0=0.1

Cb=5;

Ct=10;

Csum=1/((1/Cb)+(1/Ct));
```

```
M=1

dt=0.001

a1=1.8^2+(Cb.*(x-2)+Ct.*(V0-(1-0.5 .*x))).^2;

a2=1.8^2+(Cb.*(y-2)+Ct.*((V0-V0)-(1-0.5 .*y))).^2;

I1=((a1.^(0.5))).*(V0);

I2=((a2.^(0.5))).*(Vdd-V0);

Isum1=-I1+I2;

dV1=Isum1./Csum;

f1=(dV1.^2).^0.5;

V0=V0+dV1*dt;

while f1>=0.00000001

a1=1.8^2+(Cb.*(x-2)+Ct.*(V0-(1-0.5 .*x))).^2;

a2=1.8^2+(Cb.*(y-2)+Ct.*((V0-V0)-(1-0.5 .*y))).^2;

I1=((a1.^(0.5))).*(V0);

I2=((a2.^(0.5))).*(-V0+Vdd);

Isum1=-I1+I2;
```

```
dV1=Isum1./Csum;

f1=(dV1.^2).^0.5;

V0=V0+dV1*dt;

M=M+1;

end

Vbg=V0

a=1.8^2+(Cb.*(Vbg-2)+Ct.*(0-(1-0.5*Vbg))).^2;

I=((a.^(0.5))).*(Vdd);

mesh(Vbg1,Vbg2,I)
```

3.3.5 The hamming distance of the circuit

The most difficult part in the simulation is the hamming distance. The complication comes from the multiple matrix input. The following code is the simulation of figure 2.9. For application, i is the value of hamming distance. Set the i to achieve the value you want.

```
Input1=[0.659,-2]

Input2=[-2,0.659]
```

```
Input=0.659-2

Vdd=3

V0=0.1

z=0

Cb=5;

Ct=10;

Csum=1/((1/Cb)+(1/Ct));

M=1

dt=0.001

Vbg1=[Input1,Input1,Input1,Input1,Input1,Input2;
   Input1,Input1,Input1,Input1,Input2,Input2;
   Input1,Input1,Input1,Input2,Input2,Input2;
   Input1,Input1,Input2,Input2,Input2,Input2;
   Input1,Input2,Input2,Input2,Input2,Input2];

Vbg2=Vbg1

for i=1:3
```

```
Vbg2(i,:)=Input-Vbg1(i,:)

a1=1.8^2+(Cb.*(Vbg1-2)+Ct.*(V0-(1-0.5*Vbg1))).^2;

a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V0-V0)-(1-0.5*Vbg2))).^2;

I1=((a1.^(0.5))).*(V0);

I2=((a2.^(0.5))).*(Vdd-V0);

Isum1=-I1+I2;

dV1=Isum1./Csum;

f1=(dV1.^2).^0.5;

V0=V0+dV1*dt;

    while f1>=0.00000001

       a1=1.8^2+(Cb.*(Vbg1-2)+Ct.*(V0-(1-0.5*Vbg1))).^2;

        a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V0-V0)-(1-0.5*Vbg2))).^2;

          I1=((a1.^(0.5))).*(V0);

           I2=((a2.^(0.5))).*(-V0+Vdd);

             Isum1=-I1+I2;

            dV1=Isum1./Csum;
```

```
            f1=(dV1.^2).^0.5;
           V0=V0+dV1*dt;
         end
Vbg=V0
a=1.8^2+(Cb.*(Vbg-2)+Ct.*(0-(1-0.5*Vbg))).^2;
R=1./(a.^(0.5));
RR=sum (R)
I=((a.^(0.5))).*(Vdd);
II=sum(I)
z=z+1
g{z}=Vbg2
c(z,:)=II
f(z,:)=II
Vbg2=Vbg1
end
  c=reshape(c',1,prod(size(c)))
```

```
c=unique(c)
```

3.3.6 Stage evaluation tree

The code is the result of numerical modeling illustrating the evaluation trees for output voltage at combinations of the stage Vdd, showed in figure 2.10.

```
Input1=0.5;

Input2=1.9;

Input3=2.2;

Input4=2.2;

Vdd1=3;

Vdd2=1.5;

Vdd3=0;

V0=0.1%[0.1,0.1,0.1,0.1,3,3,3,3];

V1=0.1%[0.1,0.1,3,3,0.1,0.1,3,3];

V2=0.1%[0.1,3,0.1,3,0.1,3,0.1,3];
```

```
N=0

Cb=5;

Ct=10;

Csum=1/((1/Cb)+(1/Ct));

M=1

dt=0.001



i=1;

Vbg1=[Input1,Input2,Input1,Input2];

Vbg2=[Input1,Input1,Input2,Input2];

a1=1.^2+(Cb.*(Vbg1-2)+Ct.*(V0-(1-0.5*Vbg1))).^2;

a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V0-V0)-(1-0.5*Vbg2))).^2;

I1=((a1.^(0.5))).*(V0);

I2=((a2.^(0.5))).*(Vdd1-V0);

Isum1=-I1+I2;

dV1=Isum1./Csum;
```

```
f1=(dV1.^2).^0.5;

V0=V0+dV1*dt;

while f1>=0.00000001

a1=1.8^2+(Cb.*(Vbg1-2)+Ct.*(V0-(1-0.5*Vbg1))).^2;

a2=1.8^2+(Cb.*(Vbg2-2)+Ct.*((V0-V0)-(1-0.5*Vbg2))).^2;

I1=((a1.^(0.5))).*(V0);

I2=((a2.^(0.5))).*(-V0+Vdd1);

Isum1=-I1+I2;

dV1=Isum1./Csum;

f1=(dV1.^2).^0.5;

V0=V0+dV1*dt;

M=M+1;

%    hold on

%    plot(M,V0)

end

j=2;
```

```
Vbg3=[V0,Input3,V0,Input3];

Vbg4=[V0,V0,Input3,Input3];

a3=1.8^2+(Cb.*(Vbg3-2)+Ct.*(V1-(1-0.5*Vbg3))).^2;

a4=1.8^2+(Cb.*(Vbg4-2)+Ct.*((V1-V1)-(1-0.5*Vbg4))).^2;

I3=((a3.^(0.5))).*(V1);

I4=((a4.^(0.5))).*(Vdd2-V1);

Isum2=-I3+I4;

dV2=Isum2./Csum;

f2=(dV2.^2).^0.5;

V1=V1+dV2*dt;

while f2>=0.00000001

a3=1.8^2+(Cb.*(Vbg3-2)+Ct.*(V1-(1-0.5*Vbg3))).^2;

a4=1.8^2+(Cb.*(Vbg4-2)+Ct.*((V1-V1)-(1-0.5*Vbg4))).^2;

I3=((a3.^(0.5))).*(V1);

I4=((a4.^(0.5))).*(-V1+Vdd2);

Isum2=-I3+I4;
```

```
dV2=Isum2./Csum;

f2=(dV2.^2).^0.5;

V1=V1+dV2*dt;

M=M+1;

%    hold on

%    plot(M,V1)

end

N=3

Vbg5=[V1,Input4,V1,Input4];

Vbg6=[V1,V1,Input4,Input4];

a5=1.8^2+(Cb.*(Vbg5-2)+Ct.*(V2-(1-0.5*Vbg5))).^2;

a6=1.8^2+(Cb.*(Vbg6-2)+Ct.*((V2-V2)-(1-0.5*Vbg6))).^2;

I5=((a5.^(0.5))).*(V2);

I6=((a6.^(0.5))).*(Vdd3-V2);

Isum3=-I5+I6;

dV3=Isum3./Csum;
```

```
f3=(dV3.^2).^0.5;

V2=V2+dV3*dt;

while f3>=0.00000001

a5=1.8^2+(Cb.*(Vbg5-2)+Ct.*(V2-(1-0.5*Vbg5))).^2;

a6=1.8^2+(Cb.*(Vbg6-2)+Ct.*((V2-V2)-(1-0.5*Vbg6))).^2;

I5=((a5.^(0.5))).*(V2);

I6=((a6.^(0.5))).*(Vdd3-V2);

Isum3=-I5+I6;

dV3=Isum3./Csum;

f3=(dV3.^2).^0.5;

V2=V2+dV3*dt;

M=M+1;

%    hold on

%    plot(M,V2)

end

plot(V0,i,'.',V1,j,'.',V2,N,'.','MarkerFaceColor','g','MarkerSize',30)
```

```
ylim([0,4])

grid on
```

3.4 Conclusions

Usually the author does not offer the exact code for their simulation. But the other researcher will waste extra time for next step research on repeat the former work. I would like to offer my code to help other people to research in this area.