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Large Signal Analysis on Variations of the Hybridized Dickson Switched-Capacitor Converter

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***Abstract*— Dickson-type DC-DC converters have gained renewed interest in recent years due to their best-in-class volt-amp switch utilization. In addition, "hybrid" switched-capacitor (HSC) structures increase passive component utilization while avoiding the slow-switching limit (SSL), and yet, most HSC work to date has done little to assess large signal voltage ripple behavior and subsequent passive utilization limits. This work contributes a comprehensive review of contemporary Dickson-type HSC converters before introducing eight fundamental reduced HSC Dickson structures, including three that are proposed here. Analysis allowing characterization of large signal operating points, capacitor sizing regimes, switching schemes, and maximum allowable power throughput is introduced. The analysis for "split-phase" switching is also presented in detail, without making small ripple approximations. Furthermore, an expression for large ripple flying capacitor energy density utilization is derived, assisting with optimal topology selection and revealing that split-phase operation may be preferable for conversion ratios greater than 6:1. All analysis is verified in simulation, with an additional discrete hardware prototype further validating a complex case of resonant split-phase timing. The analytical results of seventeen distinct Dickson variations are recorded, assisting with topology selection and design.**

***Index Terms*—DC-DC power conversion, switched capacitor circuits, resonant power conversion.**

I. Introduction

STRATEGICALLY introducing inductors into switched-capacitor power converter topologies has been shown to enable elimination of the steady-state transient inrush currents which would otherwise occur due to flying capacitor voltage mismatch. This technique, termed here as "hybridization", avoids the slow-switching limit (SSL) [1] and allows inductively-assisted capacitor networks to act as highly effective soft-charged energy transfer elements, leading to state-of-the-art power densities being reported in recent years (e.g. [2]–[5]). As hybridized switched-capacitor (HSC) power converters gain popularity, a significant body of work has emerged which describes SSL mitigation in a variety of topologies, with additional work applying zero-voltage/current switching (ZVS/ZCS) [4], [5], [8], [12]–[14] and advanced gate-drive structures [15]–[19] for further improved switching performance. Previous work has proposed general analytical methods by which switched-capacitor topologies can be assessed as to their eligibility for hybridization, with com-

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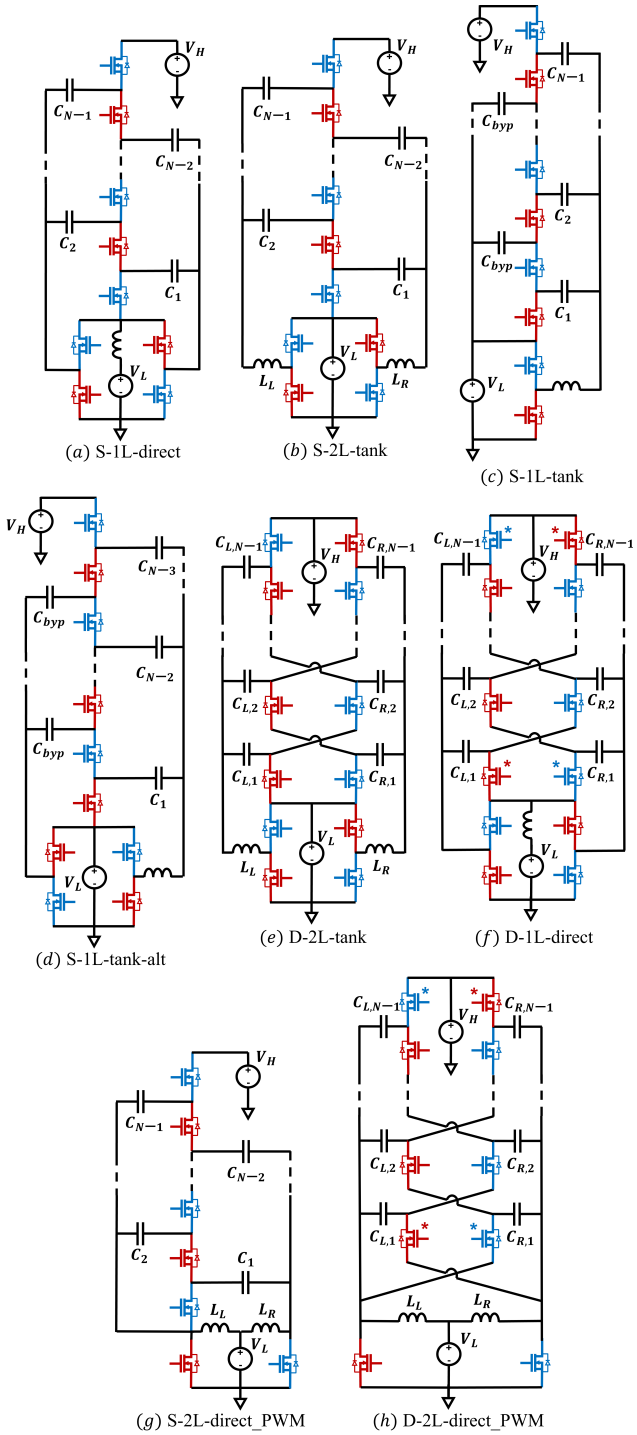

Figure 1. Eight fundamental variations of the HSC Dickson converter using either one or two inductors to achieve complete SSL mitigation. (a), (b), (c), (g) and (h) are discussed in [6], [7], [8], {[9], [10]} and [11] respectively, while (d), (e), and (f) are proposed here. Red and blue coloring indicates switches active during the primary two phases. Asterisk (*) denotes switches requiring split-phase operation within a primary phase.

plementary work addressing revised optimal device sizings, in addition to performing comparative demonstrations which illustrate significant improvements in efficiency and power density [20]–[28].

To date, new topologies and clocking schemes continue to emerge as both academia and industry attempt to assess and quantify topology performance in this rapidly developing converter landscape. This task is made more difficult with the simultaneous development and commercialization of high performance passives and wide band-gap semiconductor devices, including gallium nitride and silicon carbide. Subsequently, general analytical methods and comparison frameworks have maintained significance due to their ability to account for evolving device performance metrics.

Many previous attempts at analyzing HSC power converters have used a classical DC operating point approach and assumed negligible current ripple in inductors and/or negligible voltage ripple in flying capacitors for simplicity. However, we note that the fundamental motivation behind HSC topologies in general is their ability to effectively increase the dynamic range of passive components' large signal behavior [29]–[31]. In particular, flying capacitors can deliberately operate with greatly increased voltage ripple, improving component energy density utilization and further reducing passive element size. Under these extremes of operation, where converter performance reaches its limit, such simplifying assumptions may significantly detract from a comprehensive analysis. In this work, we contribute a comprehensive large signal topological analysis of HSC converters with few assumptions aside from modeling components as ideal[1].

Section II explores the design space encompassing a number of recent state-of-the-art HSC variations on the Dickson topology — a structure recognized as having a best-in-class switch utilization, matching that of the Cockcroft-Walton/Greinacher (CW) or Ladder topologies [28] — while Section III provides a technical commentary on the eight fundamental reduced variations of the HSC Dickson converter depicted in Fig. 1, with topologies (d), (e), and (f) proposed here. Section IV outlines a methodology that allows large-signal steady-state operating points to be derived, in addition to contributing example derivations of an appropriate capacitor sizing regime, clocking scheme, and maximum allowable output power. The expressions derived here — and throughout the remainder of this work — account for large ripple conditions and are constrained to maintain complete SSL mitigation, synonymous with full "hybridization" or soft-charging of all flying capacitors. Section V uses the preceding analysis to derive the energy density utilization, η, of all flying capacitors as a function of load. Furthermore, switch-imposed constraints are used to determine the minimum achievable capacitor volume at a given power level. Section VI addresses split-phase switching – a modified clocking scheme that maintains full SSL mitigation in topologies that yield no capacitor sizing solution as per the analysis presented in Section IV. Here we contribute a new large signal analysis that accounts for both inductor and flying capacitor ripple simultaneously. Accurate expressions for load-dependent bias points, split-phase timing, and both maximum power and capacitor utilization are all derived. Section VII validates the analysis of Section VI using a discrete hardware prototype. Section VIII documents the result of similar analysis applied to seventeen distinct variations on the eight fundamental Dickson structures depicted in Fig. 1. Maximum flying capacitor utilization is also plotted versus conversion ratio, revealing that split-phase approaches offer improved capacitor utilization for conversion ratios larger than 6:1. Section IX concludes this work.

II. Contemporary Dickson Converters

While the analysis presented in the following sections may be extended to other HSC structures, in this work we choose to focus on hybridized topologies that have capacitor network structures akin to that published by J.F. Dickson in 1976 [33]. While the original Dickson topology was described as a DC-DC topology with a single switch column and two interleaved capacitor networks, here we define a Dickson-type converter as any switched-capacitor topology that contains one or more grouped capacitor networks that are organized such that all capacitors within each network share a common bottom-plate connection, as is the case for all variants depicted in Fig 1.

Upon its initial publication as a purely capacitor-based non-hybridized topology, the Dickson converter received interest due to its ability to effectively drive the non-ideal bottom-plate substrate capacitance of all of its flying capacitors when implemented as a fully integrated system on-chip. However, this structure has gained renewed interest in recent years for discrete converter implementations as a result of it achieving the lowest switch V-A rating in its class, thereby requiring the smallest total die area [1], [25]–[28]. Conversely, its passive utilization is less favorable, and so several recent works have proposed various switching techniques and topological modifications that allow for increased capacitor ripple for improved passive energy density utilization, while simultaneously ensuring that SSL-mitigating HSC criteria are met.

For example, [20] concluded that the even order single-column single-inductor direct[2] variant (S-1L-direct), depicted in Fig. 1 (a), could only approach full SSL mitigation under a two-phase switching regime as specific capacitor values impractically tended towards infinity, leading to poor utilization in practice. Subsequent work resolved this by proposing a split-phase switching scheme [6] which enables the S-1L-direct variant of both Dickson and Cockcroft-Walton (CW) topologies [5] to achieve complete SSL mitigation by introducing tertiary switching phases that emulate the natural zero-voltage switching (ZVS) behaviour of diodes. Expanding upon this concept, split-phase switching was first demonstrated for a step-down converter in [10]. However, here voltage ripple was severely limited to be less than the reverse blocking voltage of the switches ($\sim$ 1V). Improving upon this, [35] demonstrated that by applying an inverted form of split-phase switching in

[1]Extended analysis accounting for component loss ([24], [27], [31], [32]) often has minimal impact on large signal dynamic behaviour in high efficiency designs, and so is omitted here for simplicity.

[2]The terminology "direct" and "indirect" was used in [34] to describe converters whose inductor(s) are placed either in series with the low-side port or as part of an internal tank structure respectively.

step-down applications this limitation may be overcome with greatly increased voltage ripple and capacitor utilization.

Alternative multi-phase approaches, such as those introduced in [36]–[38], have also demonstrated complete SSL mitigation, often using identical hardware, albeit with further reduced VA switch utilization. However, the reduced switching activity of these multi-phase techniques yields improved light-load performance where switching losses dominate. As a result, a converter's efficiency range may be maximized by employing either split-phase or multi-phase switching depending on the converter's operating point [5]. Moreover, classical pulse frequency modulation techniques (PFM), or dynamic off-time modulation (DOTM) in [39], [40], may also be used independently or in conjunction with multi-phase approaches to extend light load efficiency further.

Tank-based or "indirect" variations (e.g. Fig. 1(b)-(e)) have also shown promise, with flying capacitor voltage ripple largely hidden from adjacent switches, leading to reduced switch size in practice [31]. As a result, these structures allow for very large ripple, with [7] demonstrating flying capacitors being exercised over almost their entire dielectric range. In addition, the dielectric barrier of resonant tanks may find a two-fold use in capacitively isolated designs [41], [42]. Regulation may often be achieved using phase shifted-operation while preserving ZVS over a known operating range [41], or by modulating the converters output impedance using DOTM [40]. Another example is Google's "switched-tank" converter (STC) [43], depicted in Fig. 2(a), which has been acknowledged as a versatile modular approach similar to the modular multilevel switched-capacitor resonant converter (MMSCRC) in [44] which demonstrated regulation and full ZVS. Extending this, [45] demonstrated adaptive control for further refinement and optimized operation. However, the inductor(s) in tank-based topologies must conduct bi-directional current flow, dissimilar to "direct" converters with inductor(s) at the output, and so often have poorer magnetic losses [31]. In addition, the STC requires a linearly increasing number of inductors with conversion ratio[3], without significantly benefiting from coupled magnetics [50], [51]. Therefore, the STC may not scale as favorably as consolidated core designs [52]. Conversely, an increased inductor count provides a degree of capacitor mismatch immunity and allows for straightforward use of Class II MLCC dielectrics with poor tolerances and derating with age, bias and temperature [53]. The series-capacitor buck (SCB) [54]–[56] depicted in Fig 2(b) similarly benefits, with an inductor always present in every KVL loop.

While several of the aforementioned topologies contain multiple inductors, for the remainder of this work we can limit consideration to topologies containing one or two flying capacitor networks and either one or two inductors. Many higher inductor count topologies can be reduced to an equivalent Dickson variant depicted in Fig. 1 by combining redundant switches and lumping parallel current paths [48]. For example, the STC in Fig. 2(a) is equivalent to the S-1L-tank-alt (Fig. 1(d)), while the SCB in Fig. 2(b) may be mapped onto

[3]To reduce inductor count and associated cost, more recent work has suggested harnessing parasitic trace inductance while switching at higher frequencies [46]–[49].

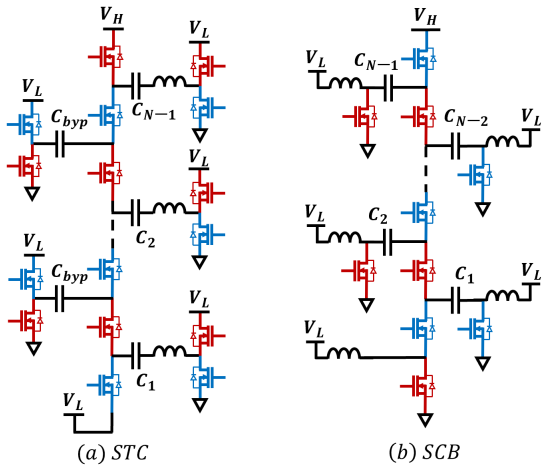

Figure 2. Example multi-inductor Dickson variants: (a) one instantiation of the switched tank converter (STC) [43], (b) series-capacitor buck (SCB) converter [54]–[56]. Assuming appropriate passive values, both the depicted STC and SCB may be simplified into the S-1L-tank-alt (Fig. 1 (d)) and S-2L-direct_PWM (Fig. 1 (g)) respectively by consolidating switches and lumping passive elements.

the S-2L-direct_PWM (Fig. 1(g)). These simplifications result in equivalent solutions with lower overall component count and often improved magnetic performance when interleaved coupled magnetic structures are not used [51], [52], albeit at the cost of decreased modularity and immunity to component mismatch. Furthermore, we focus on independent fundamental topological structures and omit merged composite HSC structures [29], [30], such as the LEGO converter [3], which can be analyzed in sections since its Dickson networks are soft-charged using adjacent buck stages[4].

III. Fundamental HSC Dickson Structures

While the literature on Dickson-type topologies continues to grow, a comparative study of its hybridized variations' large signal characteristics and SSL-mitigating criteria has been lacking. To address this gap, first we summarize each of the eight reduced Dickson structures depicted in Fig. 1, describing their origins — or inspiration in the case of the three variants proposed here — and emphasizing key properties. A comprehensive list of properties is summarized in Table IV of Section VIII.

(a) S-1L-direct. Mentioned previously, this HSC Dickson variant has recently been used to demonstrate split-phase switching [6]. While split-phase switching was required for even conversion ratios in [6], Section IV of this work demonstrates that for odd conversion ratios the S-1L-direct topology can use simplified 2-phase control, provided that specific relative capacitor sizing relationships are satisfied.

As a "direct" topology, the flying capacitor's load dependent voltage ripple is directly imposed on its switches [31], resulting in a well defined limit to the effective energy density utilization of the flying capacitors, as will be examined in Section V. However, it is possible for the inductor to maintain continuous forward conduction while regulating its output through the addition of tertiary pulse-width modulated (PWM) regulation phases [57], [58]. Additionally, the inductor acts as

[4]Due to their two-stage structure, these composite variants may use independently optimized switching frequencies for each stage.

a high frequency choke effectively shielding the low-side port from switching noise and conducted EMI.

(b) S-2L-tank. Recently introduced in [7], this variant is the reduced form of the MMSCRC [44]. Two-phase switching is achievable only at odd conversion ratios, however, the second inductor provides an additional degree of freedom that allows all flying capacitors to be equal in value while also enabling a convenient 50 % duty cycle. As an indirect tank structure, voltage ripple is largely hidden from adjacent switches, allowing for large flying capacitor ripple and very high energy density utilization in practice. As noted in [7], high dv/dt ringing may occur during one of the phases due to the absence of a low impedance path to ground. If component mismatch or unwanted parasitics inhibit complete SSL mitigation, an increased switching frequency and phase-shifted operation similar to [4], [8] may achieve complete soft-charging in addition to ZVS, at the expense of increased circulating currents and reverse conduction losses.

(c) S-1L-tank (Stacked-Ladder). Recently published in [8], this topology offers several desirable traits: it can achieve complete two-phase SSL mitigation at odd or even conversion ratios using a single inductor with a 50 % duty cycle and with all flying capacitors equal in size. As an indirect structure, tank ripple can be large, leading to effective energy density utilization. However, the left side capacitors depicted in Fig. 1 (c) make up a bypass capacitor network and achieves complete SSL mitigation only in the limit of infinite capacitance. This requirement can be approximated using capacitors with high energy density dielectrics, such as Class-II MLCC capacitors since precise matching is not required. Alternatively two interleaved S-1L-tank converters with a 180° phase shift can draw and feed charge from the same shared bypass capacitor column, allowing the capacitors to be greatly reduced [8], [59].

(d) S-1L-tank-alt [Proposed here]. For even conversion ratios only, the static bypass capacitor column of the S-1L-tank may instead be switched, effectively doubling the converter's conversion ratio, albeit with a commensurate increase in switch stress. While not indicated in Fig. 1(d), finite capacitor values may alternatively be used, but split-phase switching requirements are introduced as a result.

(e) D-2L-tank [Proposed here]. Since the shared bypass capacitor column in a dual interleaved S-1L-tank converter is not strictly necessary, it can be removed entirely with further equivalent switch manipulation and consolidation yielding the D-2L-tank converter. This topology retains all of the S-1L-tank topology's desirable attributes in addition to exhibiting a dual interleaved high-side port for reduced bypass capacitance. The D-2L-tank has almost half the number of switches for a given conversion ratio, although both approaches have equivalent VA switch utilization.

(f) D-1L-direct [Proposed here]. Analyzed further in Section VI, this topology is fundamentally incapable of conventional two-phase operation and requires split-phase operation on the four switches marked with an asterisk in Fig. 1(f) provided that all flying capacitors are sized equally. However, it exhibits a dual-interleaved high-side port for reduced decoupling requirements, despite using a single inductor. Since the four mentioned switches only conduct half of the greatly reduced high-side current, it may be desirable to replace them with diodes in step-up applications, relaxing clocking complexity significantly while introducing minimal diode forward voltage drops. All other switches can operate with a 50 % duty cycle. Similar to the S-1L-direct, the inductor provides low-side filtering benefits and allows for continuous conduction and optional regulation with added tertiary phases.

(g) S-2L-direct_PWM. Distinct from the fixed-ratio topologies discussed so far, the low-side connected inductors of the S-2L-direct_PWM topology are subjected to a chopped voltage waveform and switches may easily be controlled to effect PWM for regulation. However, the inductors experience increased volt-seconds relative to fixed-ratio topologies resulting in increased size, albeit still much smaller than a direct buck/boost solution [28]. Reminiscent of the diode-based step-up variants demonstrated in [60], [61], the S-2L-direct_PWM was demonstrated as a synchronous step-down topology in [9] and [10] where it was shown that its low switch VA rating and PWM regulation capability make it a strong candidate for high conversion ratio point-of-load applications. For odd order capacitor networks, two-phase operation can be achieved using specific capacitor sizings, similar to the S-1L-direct variant, but inductors experience unequal current distribution making component selection more challenging. For even order networks, where no two-phase capacitor sizing regime exists, complete SSL mitigation can instead be achieved using split-phase clocking.

(h) D-2L-direct_PWM. Presented in [11], this topology results from converting the S-2L-direct_PWM topology into its dual switch column variant, similar to the transformation from S-2L-tank into D-2L-tank. By doing so current is now symmetrically balanced among all components at both even and odd conversion ratios, with equal flying capacitor values being preferred. However, similar to the D-1L-direct, this topology requires split-phase switching on four of its switching elements. Step-up instantiations using either Dickson or CW networks were presented in [61] and [62] respectively where no consideration was given to either capacitor sizing or split-phase operation due to the use of diodes. Conversely, the modern synchronous variant described in [11] achieves bi-directional regulation capability with 2-phase operation on all switches bar the four mentioned.

IV. Example Two-Phase Analysis (S-1L-Direct)

Building on [1], [20] describes a method by which a switched-capacitor network can be assessed as to its eligibility for hybridization using a single inductor at its low-side input/output ("V_L" here). That is, whether a converter can achieve complete SSL mitigation as a "1L-direct" topology. This analysis begins by assuming a purely capacitor-based design and obtaining an associated system of inconsistent KVL equations, implying the presence of expected SSL losses. Then, V_L is removed as a state variable, signifying the insertion of an inductor and the removal of associated KVL loop constraints. Two-phase HSC eligibility is then ascertained

through the resulting capacitor sizing constraints.

However, this approach becomes non-trivial should inductor(s) be introduced in alternative locations where a single state variable may not exclusively capture all of a given inductor's influence. As such, here we present a sequential approach whereby arbitrary inductor placement is decided initially and appropriate KVL equations are derived directly and intuitively. By progressing in this manner any ambiguities surrounding the transition to a hybridized structure are resolved. Building on this further, we present the derivation of capacitor sizing constraints, resonant timings, and maximum power throughput. Ideal components, large input and output bypass capacitance [63], and zero switch on-resistance are assumed for simplicity.

A. Large Signal Analysis

Here we demonstrate the proposed analytical approach using the S-1L-direct topology depicted in Fig. 3 as an example. First, the method[5] described in [1] is applied to obtain the periodic charge flow through the converter, using the charge quantity conducted by the high-side port, q_H, as a reference quantity: the sequence of steps is annotated $\{1\} \rightarrow \{10\}$ in Fig. 3 and reveals that $q_L = 7 \times q_H$, implying a 1:7 conversion ratio ($N = 7$).

Subsequently, the charge flow through the i^{th} capacitor can be expressed relative to q_H using coefficient a_i, where

$$q_i = q_H a_i \tag{1}$$

For this S-1L-direct example the charge flow coefficients are

$$a_i = 1 \qquad \text{for} \quad 1 \leq i \leq 6 \tag{2}$$

Each flying capacitor's mid-range DC voltage may similarly be expressed in relation to the high-side voltage V_H, using the lowercase coefficient v_i.

$$V_i = \frac{V_{i,max} + V_{i,min}}{2} = V_H v_i \tag{3}$$

Additionally, each capacitor exhibits a voltage ripple contained within the range $V_i \pm \Delta_i$ where the i^{th} capacitor's peak-to-peak voltage ripple, $2\Delta_i$, is described by

$$2\Delta_i = \frac{q_i}{C_i} = \frac{q_H a_i}{C_0 c_i} \tag{4}$$

and where normalized capacitor notation is introduced with arbitrary capacitance C_0.

The scaling coefficients a_i, v_i, and c_i define the given HSC structure and describe the *relative* values of charge, voltage and capacitance respectively. That is, they are independent of power level, voltage or switching frequency. Specific values for q_H, V_H and C_0 define a particular operating point and converter realization and are left as variables for generality.

Having already obtained values for a_i, next we solve for v_i and c_i. Care is taken to record the polarity of the AC ripple on each flying capacitor both at the start *and* end of each phase, as deduced from the direction of charge flow q_i. In Fig. 3 this distinction is denoted by '$\pm$' and '$\mp$' for decreasing and increasing voltage ripple respectively within each phase[6]. The following KVL loops that capture the large signal effect of a non-zero Δ_i voltage ripple may then be recorded.

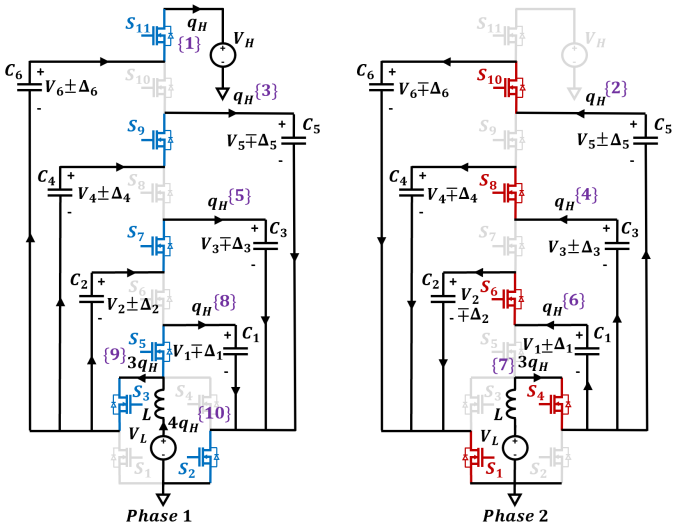

Figure 3. Phase configurations for the 1:7 S-1L-direct Dickson. The steps for deducing normalized steady-state charge flow quantities are annotated sequentially $\{1\} \rightarrow \{10\}$. The i^{th} capacitor undergoes a $2\Delta_i$ voltage transition about its mid-range bias voltage, V_i, with "$\pm$" indicating a positive to negative transition and vice versa.

Start of Phase 1:

$$(V_1 - \Delta_1) + (V_2 + \Delta_2) - (V_3 - \Delta_3) = 0 \tag{5}$$

$$(V_1 - \Delta_1) + (V_4 + \Delta_4) - (V_5 - \Delta_5) = 0 \tag{6}$$

$$(V_1 - \Delta_1) + (V_6 + \Delta_6) = V_H \tag{7}$$

End of Phase 1:

$$(V_1 + \Delta_1) + (V_2 - \Delta_2) - (V_3 + \Delta_3) = 0 \tag{8}$$

$$(V_1 + \Delta_1) + (V_4 - \Delta_4) - (V_5 + \Delta_5) = 0 \tag{9}$$

$$(V_1 + \Delta_1) + (V_6 - \Delta_6) = V_H \tag{10}$$

Start of Phase 2:

$$(V_1 + \Delta_1) - (V_2 - \Delta_2) + (V_4 - \Delta_4) - (V_3 + \Delta_3) = 0 \tag{11}$$

$$(V_1 + \Delta_1) - (V_2 - \Delta_2) + (V_6 - \Delta_6) - (V_5 + \Delta_5) = 0 \tag{12}$$

End of Phase 2:

$$(V_1 - \Delta_1) - (V_2 + \Delta_2) + (V_4 + \Delta_4) - (V_3 - \Delta_3) = 0 \tag{13}$$

$$(V_1 - \Delta_1) - (V_2 + \Delta_2) + (V_6 + \Delta_6) - (V_5 - \Delta_5) = 0 \tag{14}$$

For these ten equations there are twelve unknowns; V_1-V_6 and Δ_1-Δ_6. However, by combining similar expressions from the start and end of each phase, the DC and AC terms can be decoupled and solved independently.

For the DC terms, substituting in (3) during Phase 1 yields:

$$v_1 + v_2 - v_3 = 0 \tag{15}$$

$$v_1 + v_4 - v_5 = 0 \tag{16}$$

$$v_1 + v_6 = 1 \tag{17}$$

[5]Applies the constraint of zero net charge conducted through a capacitor in periodic steady-state.

[6]This notation is used here for compactness. Alternatively, all four boundary circuit states may be drawn out, similar to Fig. 5.

Similarly for Phase 2:

$$v_1 - v_2 - v_3 + v_4 = 0 \tag{18}$$

$$v_1 - v_2 - v_5 + v_6 = 0 \tag{19}$$

Equations (15)-(19) are underdetermined and one further constraint must be obtained relating to the inductor and V_L. How this is achieved is different for fixed-ratio versus chopped PWM topologies, but for fixed-ratio 2-phase converters it can be shown that the inductor must experience zero volt-seconds within each phase[7]. Therefore, inspecting Phase 1 (Fig. 3) we conclude that the mid-range voltage on C_1 is equal to $V_1 = V_L$, where $V_H = NV_L$. Subsequently we can solve for the mid-range DC voltage coefficients

$$v_i = \frac{i}{N} \qquad \text{for} \quad 1 \le i \le 6 \tag{20}$$

Regarding the AC terms, during Phase 1 we obtain:

$$-\Delta_1 + \Delta_2 + \Delta_3 = 0 \tag{21}$$

$$-\Delta_1 + \Delta_4 + \Delta_5 = 0 \tag{22}$$

$$-\Delta_1 + \Delta_6 = 0 \tag{23}$$

and for Phase 2:

$$\Delta_1 + \Delta_2 - \Delta_3 - \Delta_4 = 0 \tag{24}$$

$$\Delta_1 + \Delta_2 - \Delta_5 - \Delta_6 = 0 \tag{25}$$

As is, the set of equations (21)-(25) are under-determined, but an additional normalizing equality, such as $c_1 = 1$, can be introduced to give C_0 a point of reference. Equations (2) and (4) can then be substituted into (21)-(25) with common terms q_H and C_0 canceling. The result is a unique relative sizing solution for all flying capacitors which ensures complete SSL mitigation with two-phase operation:

$$\vec{\boldsymbol{c}} = [1 \quad 3 \quad 1.5 \quad 1.5 \quad 3 \quad 1]^\top \tag{26}$$

This sizing scheme results in all parallel capacitor paths expressing an identical lumped capacitance during each phase. Having the same impedance, charge flow dynamics in each path are identical, causing each branch to terminate conduction at the same time, thereby facilitating two-phase operation without the need for split-phase switching.

This sizing scheme can be generalized for a 1:N S-1L-direct converter, for odd N, giving the same sizing scheme as that noted in [9] for the S-2L-direct_PWM topology. Capacitor sizing for the i^{th} flying capacitor can be described as

$$c_{i,odd} = \frac{N-1}{N-i} \tag{27}$$

$$c_{i,even} = \frac{N-1}{i} \tag{28}$$

In summary, this same approach can be used to solve for specific capacitor sizing solutions that allow for complete soft-charging with two-phase operation in a number of converters. However, in many cases no such sizing solution exists, and split-phase switching, discussed in Section VI, may be necessary to avoid SSL losses and retain complete soft-charging of all flying capacitors.

[7]This constraint is modified when accounting for finite dead-time and parasitics such as switch output capacitance C_{OSS} [4], [12], [64].

B. Duty Cycle and Switching Frequency

To define the required phase durations that satisfy our earlier assumption of zero volt-seconds across the inductor within each phase, in addition to calculating the converter's natural resonant frequency, next we calculate the equivalent capacitance presented to the inductor during each phase. To do so DC sources are short-circuited and flying capacitors are lumped together as an effective capacitance, C_ϕ. Continuing with our S-1L-direct example, during phase 1

$$C_{\phi 1} = C_0 c_1 + \sum_{i=2,4,\ldots}^{N-3} \frac{C_0 c_i c_{i+1}}{c_i + c_{i+1}} + C_0 c_{N-1} = \frac{C_0}{2}(N+1) \tag{29}$$

and during phase 2

$$C_{\phi 2} = \sum_{i=1,3,\ldots}^{N-2} \frac{C_0 c_i c_{i+1}}{c_i + c_{i+1}} = \frac{C_0}{2}\frac{(N-1)^2}{(N+1)} \tag{30}$$

Since the same inductor is used for both phases, when operating with resonant ZCS, the switching frequency of the converter can be calculated as

$$f_{SW,RES} = \frac{1}{\pi(\sqrt{LC_{\phi 1}} + \sqrt{LC_{\phi 2}})} \tag{31}$$

Similarly the relative phase duration, or duty cycle, required to achieve ZCS can be calculated as

$$D = \frac{\sqrt{LC_{\phi 1}}}{\sqrt{LC_{\phi 1}} + \sqrt{LC_{\phi 2}}} = \frac{N+1}{2N} \tag{32}$$

Additionally it can be proven that (32) holds true for switching frequencies above resonance where the inductor enters continuous conduction with a decreasing current ripple. We note that the non-50 % duty cycle of the S-1L-direct topology may be considered a drawback for practical clock implementation.

C. Maximum Power Throughput

A maximum load condition can be determined by assessing the point at which increasing internal voltage ripple causes disabled switches to undergo a reverse bias, causing unintended reverse conduction. Here, this first occurs during Phase 2 when S_2 and S_3 simultaneously limit operation. As such, the active constraint is described by:

$$(V_2 - \Delta_2) - (V_1 + \Delta_1) \ge 0\,\text{V} \tag{33}$$

Evaluating this constraint at its boundary, and including (2), (3), (4) and (20), yields a maximum allowable charge conducted per period:

$$q_{H,\max} = \frac{2V_H C_0}{N}\left(\frac{c_1 c_2}{c_1 + c_2}\right) = V_H C_0 \frac{2\,(N-1)}{N\,(N+1)} \tag{34}$$

Subsequently, $q_{H,\max}$ can be related to maximum allowable output power using f_{SW}:

$$P_{max} = V_H q_{H,\max} f_{SW} = V_H^2 C_0 \left(\frac{2\,(N-1)}{N\,(N+1)}\right) f_{SW} \tag{35}$$

where at resonance f_{SW} is a function of both C_0 and L as per (29), (30), and (31).

V. Capacitor Energy Density Utilization

One metric that may be used to assess a topology's performance is passive energy density utilization. Since passives generally consume the majority of a converter's volume, an improvement in this metric directly translates to a reduction in size. For a given power level, by doubling the utilization, the passive volume is halved.

In this Section we use the scaling coefficients, a_i, v_i and c_i, to arrive at general expressions for the peak energy storage and total energy density utilization of the flying capacitors[8], without needing to perform integrals on time-varying power curves, as presented in [28]. Furthermore, for direct topologies with switch-imposed ripple limitations, we obtain a constrained maximum capacitor utilization.

Here the total capacitor energy density utilization of a converter, η, is defined as the sum of energy transmitted through all flying capacitors divided by twice the total energy storage capability of all flying capacitors given the peak voltage that they each experience. The storage capability is doubled to account for the possibility of bi-directional biasing (e.g. [7]), avoiding the possibility of >100% utilization. Linear capacitors are assumed for simplicity, which is an accurate representation for low-loss Class I MLCC dielectrics.

$$\eta = \frac{E_{\text{util,tot}}}{2E_{\text{pk,tot}}} \times 100\% \tag{36}$$

Assuming capacitor voltages do not become negative[9], the transmitted energy, or total energy utilized, across all flying capacitors is described by

$$E_{\text{util,tot}} = \sum_i E_{\text{util},i} = \sum_i \left(V_H v_i\right)\left(q_H a_i\right) \tag{37}$$

while the peak total energy storage capability of all flying capacitors is described by

$$E_{\text{pk,tot}} = \sum_i E_{\text{pk},i} = \sum_i \frac{1}{2} C_0 c_i \left(V_H v_i + \frac{q_H a_i}{2C_0 c_i}\right)^2 \tag{38}$$

Substituting (37) and (38) into (36) yields

$$\eta = \frac{V_H q_H \beta}{C_0 V_H^2 \alpha + V_H q_H \beta + \frac{q_H^2}{4C_0}\gamma} \times 100\% \tag{39}$$

where

$$\alpha = \sum_i c_i v_i^2 \tag{40}$$

$$\beta = \sum_i v_i a_i \tag{41}$$

$$\gamma = \sum_i \frac{a_i^2}{c_i} \tag{42}$$

The expression for η in (39) is general and a function of topology dependent scaling coefficients (a_i v_i, and c_i) and specific operating point and component selection (V_H, q_H, C_0). As such, η may be used to characterize the large signal capacitor utilization of any HSC, provided the assumptions of linear capacitance and consistent positive bias are valid.

A. Example: Constrained Capacitor Utilization

Using $q_{H,max}$ from Eqn. (34), we can calculate the maximum achievable capacitor utilization, η_{max}, for the two-phase S-1L-direct topology discussed in Section IV. First α, β, and γ are solved for using the expressions for a_i, v_i, and c_i, in (2), (20) and (27-28), respectively.

$$\begin{aligned}\alpha &= \sum_{i,\text{even}} c_{i,\text{even}} v_i^2 \quad + \quad \sum_{i,\text{odd}} c_{i,\text{odd}} v_i^2 \\ &= \sum_{i=1}^{\frac{N-1}{2}} \frac{N-1}{2i}\left(\frac{2i}{N}\right)^2 + \sum_{i=1}^{\frac{N-1}{2}} \frac{(N-1)}{N-(2i-1)}\left(\frac{2i-1}{N}\right)^2 \\ &= \frac{(N+1)(N-1)^2}{4N^2} + \frac{N-1}{N^2}\sum_{i=1}^{\frac{N-1}{2}} \frac{(1-2i)^2}{N+1-2i}\end{aligned} \tag{43}$$

$$\beta = \sum_{i=1}^{N-1} \frac{i}{N} = \frac{N-1}{2} \tag{44}$$

$$\gamma = 2\sum_{i=1}^{(N-1)/2} \frac{2i}{N-1} = \frac{N+1}{2} \tag{45}$$

Here, the unique equations for even and odd capacitor sizes given in (27) and (28) result in an α comprised of two parts. An expression for η_{max} is then obtained by combining (34), (39), and (43)-(45).

$$\eta_{max} = \frac{4N}{N^2+6N+3+\frac{4(N+1)}{(N-1)}\sum_{i=1}^{(N-1)/2}\frac{(2i-1)^2}{N+1-2i}} \times 100\% \tag{46}$$

This result is a direct measure of how well the flying capacitors may be utilized, as a function of conversion ratio N. In Section VIII we compare this metric against several other HSC Dickson solutions.

B. Example: Validation by Simulation

Equation (46) was validated through simulation in LTSpice using $N = 7$, $V_L = 10\,\text{V}$, $C_0 = 100\,\text{nF}$ and $L = 82.71\,\text{nH}$. Capacitor values for C_{1-6} are found to be 100 nF, 300 nF, 150 nF, 150 nF, 300 nF and 100 nF respectively, as per (27) and (28). Using (29)-(32), the switching frequency is determined to be 1 MHz with a duty cycle of 57.14 %. A critical load resistance of 46.6 Ω is found using (34), representing the point at which switches S_2 and S_3 will begin to undergo a reverse bias if load current is increased further. This is confirmed in simulation by observing that the voltage on the node connecting the inductor to switches S_3, S_4 and S_5, (labeled V_{SW} in Fig. 4) transitions to its minimum allowable voltage of 0 V upon commencement of phase 2. Furthermore, symmetric oscillation of V_{SW} about V_L within each phase validates the added zero volt-second constraint stated in Section IV-A.

The peak energy storage for each capacitor was calculated using $0.5 \times C_i V_{max,i}^2$ where the maximum voltage observed across each capacitor was taken from simulated steady-state

[8]While magnetics may also be considered as part of a comprehensive assessment of a converter's passives, their large signal behavior in HSC designs is dependent on — and results from — the analysis presented here and will be addressed in a future extension of this work. Moreover, there are several scenarios in which capacitor utilization may wish to be considered in isolation, such as when integrating flying capacitors on-chip.

[9]Should a capacitor's ripple cause a temporary polarity reversal, a non-linear term is introduced and equation (38) will need to be modified.

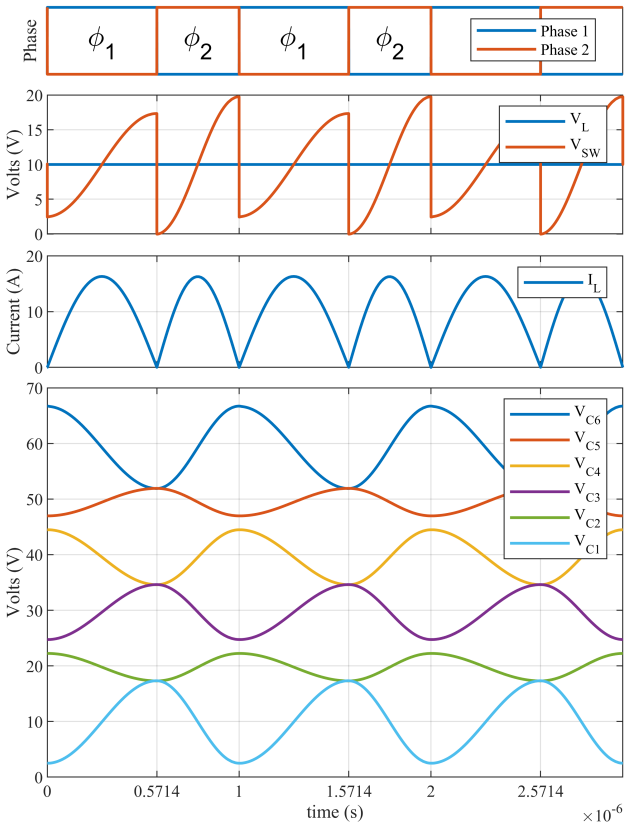

Figure 4. Simulated LTSpice waveforms of a 2-Phase 1:7 S-1L-direct converter operating with maximum allowable charge conduction, $q_{H,max}$. Phase 2 (ϕ_2) commences with $V_{SW} = 0$V, signifying that a further load increase would result in unintended reverse conduction in switches S_2 and S_3.

Table I
SIMULATED STEADY-STATE VOLTAGE RIPPLE FOR 2PH 1:7 S-1L-DIRECT.

	C1	C2	C3	C4	C5	C6
V max (V)	17.33	22.24	34.62	44.47	51.92	66.71
V min (V)	2.50	17.30	24.74	34.59	46.98	51.89

(recorded in Table I). Likewise the energy utilized by each capacitor was calculated by subtracting the minimum energy stored from the maximum energy stored. Total peak flying capacitor energy and energy utilized was determined by summing across all capacitors respectively. Percent energy utilization, calculated using (36), yields a maximum 16.13 % capacitor utilization in this case. This result is identical to that calculated using (46), validating its derivation, and is contextualized against other variations in Fig. 10.

VI. SPLIT-PHASE ANALYSIS

"Split-phase" switching ([6]) uses a more complicated clocking scheme in which specific flying capacitors are only allowed to conduct charge during a sub-interval of a primary switching phase. For topologies with specific conversion ratios and/or capacitor sizes where no analytical two-phase soft-charging solution exists, split-phase switching can ensure that KVL is satisfied at all switching transitions, implying complete SSL mitigation and soft-charging of all flying capacitors. Moreover, [35] demonstrates that in general it is preferable to have the split-phase capacitors conduct towards the end of a primary phase in step-up converters, and towards the beginning of a primary phase in step-down applications. While both temporal placements are theoretically acceptable in either application, adhering to this heuristic avoids the restrictive reverse conduction limits encountered in [10].

Two key elements are required to enable this technique: knowledge of which capacitors to include/omit, and — more challenging — the precise duration of these added sub-intervals, as any timing errors will reintroduce hard-charging losses. When first introduced, [6] assumed zero inductor current ripple when calculating the timing of these sub-intervals, and while [10] improved upon the zero-ripple approach by adding corrective linearized inductor ripple terms, until now, no full large signal analysis has been presented that accounts for large ripple in both flying capacitors and inductors. Here, capacitor ripple only is assessed first, serving as the complement to [10]. Then both capacitor and inductor ripple are assessed simultaneously for the case of resonant operation, yielding an accurate large signal result that is verified experimentally in Section VII. This analysis may be extended to account for capacitor and inductor ripple at finite frequencies above resonance, but is omitted here for conciseness.

To define split-phase operation, now using a D-1L-direct Dickson as an example (Fig. 5), we begin again by applying charge flow analysis, assuming two conventional phases of operation. This reveals that all capacitors must conduct equal charge in steady-state, equal to $q_H/2$, where the total periodic high-side charge, q_H, is again used as a reference quantity. Applying the previously discussed methods, no appropriate capacitor sizings for conventional two-phase operation can be found, indicating the requirement for split-phase switching in order to avoid hard-charging losses. Given this requirement, one straightforward solution is to size all flying capacitors equal to C_0. As will be shown, this choice results in only two switches per phase requiring identical modified clocking schemes.

To deduce which branches must undergo split-phase switching, consider the following: since all flying capacitors are sized equally and must conduct the same quantity of charge, $q_H/2$, they all express the same 2Δ peak-to-peak voltage ripple within a phase (Eqn. (4)), as annotated in Fig. 5. As a result, parallel branches that contain two flying capacitors in series will undergo twice the overall voltage ripple relative to branches that contain a single flying capacitor. Thus, in order to satisfy KVL, any single capacitor branch must only be connected in parallel with series-connected branches for a sub-interval of the latter's conduction window: in this case, for half of the two-capacitor branch's voltage deviation. This does not however imply half the conduction time because the step change in impedance presented to the inductor alters dv/dt, in addition to time-varying charge delivery with non-zero inductor ripple. Figure 5 shades out the capacitor branches that begin each phase disconnected, with their delayed introduction dependent on ZVS conditions being satisfied as each phase progresses.

Figure 5 is also annotated with the large signal voltages present on all flying capacitors both at the beginning and end of each phase. In this case the converter is left and right-sided

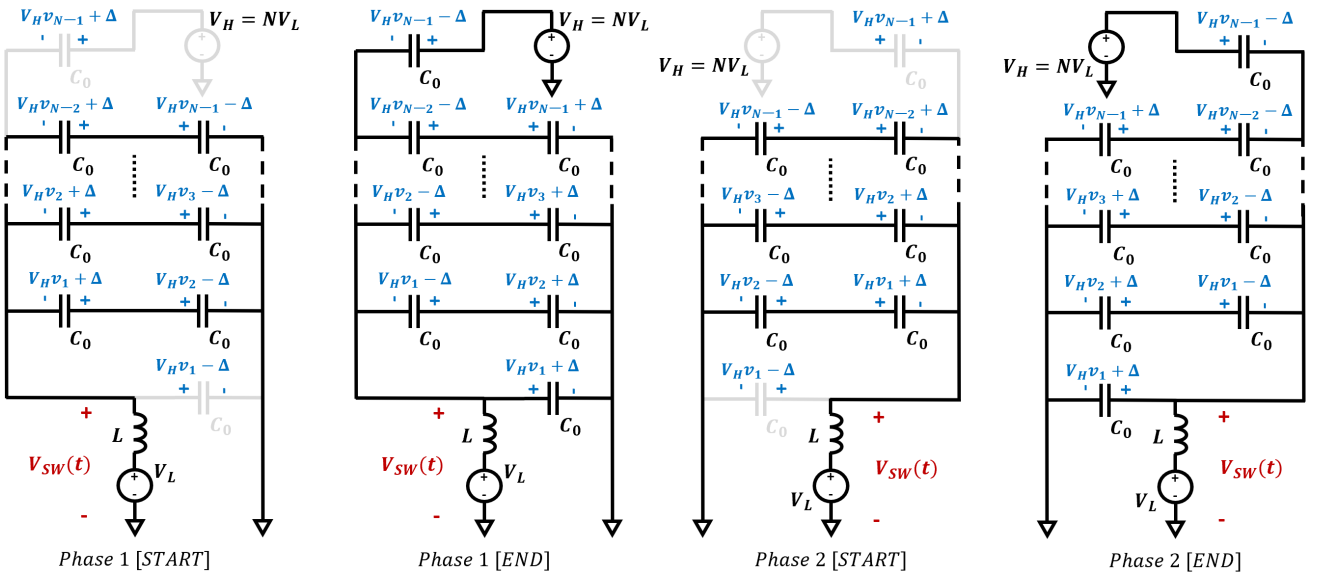

Figure 5. Phase progression for the generalized 1:N D-1L-direct converter undergoing step-up split-phase operation with all flying capacitors set equal. Circuit configurations and flying capacitor voltages (left and right side symmetric) are depicted for both the start and end of each phase.

symmetric which serves to simplify our analysis: constraints satisfying only one phase need be assessed, with the resulting equations being sufficiently bounded such that an additional volt-second constraint need not be considered. For a 1:N D-1L-direct topology, the following equations are obtained through KVL at the end of either phase:

$$2V_H v_1 - V_H v_2 - \Delta = 0 \tag{47}$$

$$V_H v_1 + V_H v_{N-1} = V_H \tag{48}$$

$$2V_H v_i = V_H v_{i-1} + V_H v_{i+1} \qquad \text{for } 1 < i < N-1 \tag{49}$$

Equations (47)-(49) can be solved to yield

$$v_i = \frac{i}{N} + \frac{\Delta}{V_H}\left(\frac{N-2i}{N}\right) \tag{50}$$

where equation (50) defines the mid-range voltage of each flying capacitor and is a function of load, as can be related to Δ using (4).

Next, the timing of appropriate switch activation is examined for two extreme cases. The first idealizes the deep continuous conduction regime where at switching frequencies much higher than resonance, the inductor current appears approximately constant with assumed zero ripple. The second case does not simplify capacitor or inductor behaviour and instead examines large signal resonant operation with ZCS observed on each phase transition.

A. Split-Phase Timing: Constant Current

At frequencies much higher than the converter's natural resonant frequency, the low-side inductor can be regarded as a constant current source, as shown in Fig. 6 (a). Subsequently capacitor voltages change linearly. Additionally, both capacitors shaded in Fig. 5 (phase 1 or phase 2) remain isolated until critical time t_k is reached. As such, the lumped effective capacitance seen by the inductor is different during

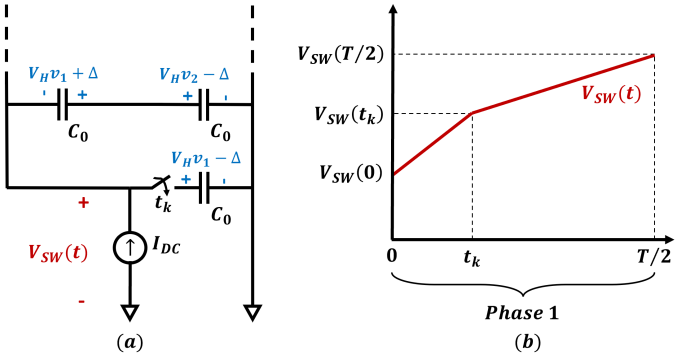

Figure 6. (a) schematic at $t = 0$, and (b) switch node waveform V_{SW} illustrating split-phase timing. Since the inductor is assumed to have zero current ripple it can be replaced with an ideal current source. Single capacitor branches must be inserted into the primary power path upon realizing ZVS conditions if SSL losses are to be avoided.

time intervals $\{0 \to t_k\}$ and $\{t_k \to T/2\}$, modifying the slope of switch node waveform $V_{SW}(t)$, as depicted in Fig. 6 (b).

$$C_{eff,\{0\to t_k\}} = C_0\left(\frac{N-2}{2}\right) \tag{51}$$

$$C_{eff,\{t_k\to T/2\}} = C_0\left(\frac{N+2}{2}\right) \tag{52}$$

Furthermore, V_{SW} can be defined as follows using KVL:

$$V_{SW}(0) = V_H v_2 - V_H v_1 - 2\Delta \tag{53}$$

$$V_{SW}(t_k) = V_H v_1 - \Delta \tag{54}$$

$$V_{SW}(T/2) = V_H v_1 + \Delta \tag{55}$$

Subsequently t_k and $T/2$ can be expressed as

$$t_k = \frac{C_0\left(\frac{N-2}{2}\right)\left(V_{SW}(t_k) - V_{SW}(0)\right)}{I_{DC}} \tag{56}$$

$$\frac{T}{2} = t_k + \frac{C_0\left(\frac{N+2}{2}\right)\left(V_{SW}(T/2) - V_{SW}(t_k)\right)}{I_{DC}} \tag{57}$$

Finally, combining (47), (53-57), the split-phase duty cycle is obtained, expressed as a fraction of phase duration.

$$D_{SOFT} = \frac{t_k}{T/2} = \frac{N-2}{2N} \tag{58}$$

Here we observe that D_{SOFT} is a function of conversion ratio only, with no load dependence. Given the assumption of constant inductor current with no ripple, this result is similar to that described in [6].

B. Split-Phase Timing: Resonant Mode

In resonant mode, each phase transition occurs once the inductor current has returned to 0 A, thereby effecting ZCS. Although sinusoidal voltage and current behavior is expected, the introduction/omission of split-phase branches partway through a primary phase results in resonant dynamics that change mid-phase, similar to the change in slope observed in Fig. 6. The bounding voltage ripple constraints defined in (53)-(55) are still applicable here, with resonant dynamics modifying only the rate at which charge is conducted, and not the net quantity which is still normalized around q_H.

During the initial time interval $\{0 \rightarrow t_k'\}$, and before the additional capacitors have been included, the converter operates with a natural resonant frequency of

$$f_1 = \frac{1}{2\pi\sqrt{LC_0\dfrac{N-2}{2}}} \tag{59}$$

and $V_{SW}(t)$ is described by

$$V_{SW}(t) = V_L + (V_{SW}(0) - V_L)\cos(2\pi f_1 t). \tag{60}$$

Conversely, during interval $\{t_k' \rightarrow T/2\}$, both the natural resonant frequency and $V_{SW}(t)$ are modified to

$$f_2 = \frac{1}{2\pi\sqrt{LC_0\dfrac{N+2}{2}}}. \tag{61}$$

$$V_{SW}(t) = V_L + (V_{SW}(T/2) - V_L)\cos(2\pi f_2 (t - T/2)). \tag{62}$$

Evaluating both (60) and (62) at $t = t_k'$ and combining the result with (47), (53)-(55), (59), and (61) yields this topology's resonant split-phase duty cycle:

$$D_{RES} = \frac{t_k'}{T/2} = \frac{1}{1 + \frac{\sqrt{N+2}}{\sqrt{N-2}}\frac{\cos^{-1}\left(\frac{1}{1-N}\right)}{\cos^{-1}\left(\frac{1}{1+N}\right)}} \tag{63}$$

Furthermore, calculation of this topology's resonant switching frequency, maximum power throughput, and constrained capacitor utilization is straightforward using the steps described in Sections IV and V. For reference, the D-1L-direct topology's resonant switching frequency is found to be

$$f_{SW,RES} = \frac{1}{2\sqrt{LC_0}\left(\sqrt{\frac{N-2}{2}}\cos^{-1}\left(\frac{1}{1+N}\right) + \sqrt{\frac{N+2}{2}}\cos^{-1}\left(\frac{1}{1-N}\right)\right)} \tag{64}$$

the constrained maximum normalized charge quantity is

$$q_{H,max} = V_H C_0 \left(\frac{2}{N+1}\right), \tag{65}$$

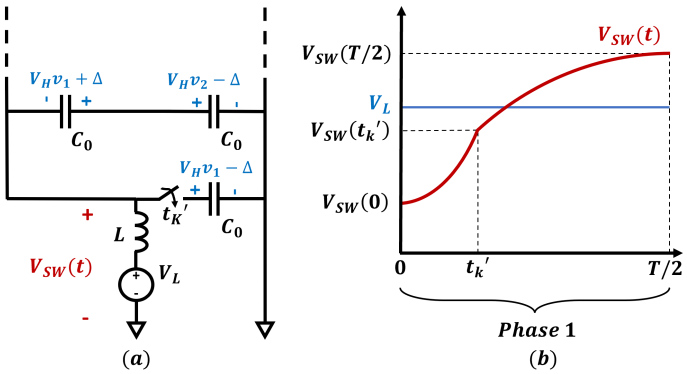

Figure 7. (a) schematic at $t = 0$, and (b) switch node waveform V_{SW} illustrating resonant split-phase operation. Similar to Fig. 6, select capacitors must be inserted into the primary power path upon realizing ZVS conditions if SSL losses are to be avoided.

and the theoretical maximum percent capacitor utilization of the D-1L-direct, for all conversion ratios N, is described by

$$\eta_{max} = \frac{3(N+1)}{2N^2+5N+6} \times 100\%. \tag{66}$$

Maximum power throughput at resonance can be obtained from (64) and (65) (similar to (35)) or alternatively this limit may be extended by operating above resonance. These equations are all validated with measured results using a discrete prototype described in Section VII.

VII. Discrete Prototype

A discrete 1:7 (N=7) D-1L-direct converter prototype, depicted in Fig. 8, was constructed to validate the derivation of (63), (64), (65), and (66). The primary components of the power stage are listed in Table II, where these values dictate both the resonant switching frequency (64) and $q_{H,max}$ (65). Figure 9 plots measured waveforms with a 10 V input, resonant switching frequency of 296 kHz, and a predicted maximum load of 0.41 A. Each phase initializes with $V_{SW} \simeq 0V$ illustrating expected operation at $q_{H,max}$.

Here, diodes are used for the majority of high-side switches to demonstrate this converter's unforced adherence to the expected split-phase switching regime: in step-up converters, split-phase switching may be viewed as an active emulation of how diodes behave naturally [35]. Here the diodes serve to validate the intended clocking scheme by precisely aligning their conduction intervals with the derived timing sequence, an effect that may be masked by a forced transition using synchronous switches.

Figure 9 illustrates that the split-phase switches – $\{S_{R3}$,$S_{L9}\}$ in Phase 1, and $\{S_{L3}$,$S_{R9}\}$ in Phase 2 – naturally undergo a ZVS transition and turn ON once the calculated time duration t_k' has elapsed, validating the derivation of (63) with an observed split-phase duty cycle of 0.38. At this moment, flying capacitors $\{C_{R1}$,$C_{L6}\}$ (Phase 1) and $\{C_{L1}$,$C_{R6}\}$ (Phase 2) are inserted and their voltage begins to change. Note that the lack of any abrupt voltage transitions on any flying capacitor demonstrates complete soft-charging and correct HSC operation.

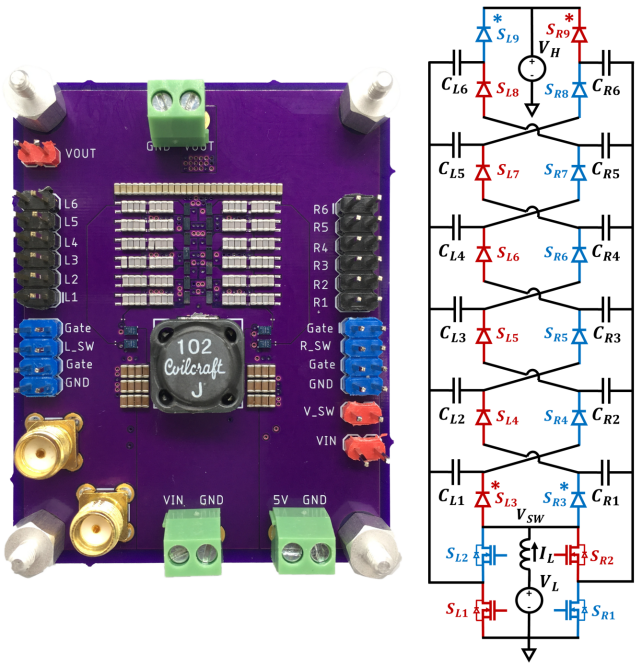

Figure 8. A discrete hardware prototype (left) demonstrating the D-1L-direct variant from Fig. 1(f) with a 1:7 conversion ratio (right). Diodes are used for most of the high-side switches both for simplicity and to validate the preceding analysis through their automatic unforced adherence to the calculated split-phase timings. The component placement in the prototype matches the schematic.

Table II
COMPONENT DETAILS

Components	Details	Part Number
$C_{LX} = C_{RX} = C_0$	8× 10 nF, 50 V, C0G, 0603	GRM1885C1H103JA01D
L	1 μH, 6 mΩ, 20 A	MSS1260-102NL
$S_{X,1\text{-}2}$	16 mΩ, 40 V, NMOS	EPC2014C
$S_{X,3\text{-}9}$	2 A, 30 V, Schottky	NSR20F30NXT5G

Despite a nominal 1:7 conversion ratio, the output voltage is decreased to $V_H = 65.4$ V, primarily as a result of successive diode forward voltage drops. However, synchronous switches may be substituted in for improved performance, provided they are controlled in adherence with the derived timing scheme.

Table III compares measured flying capacitor voltages with that predicted by (50), in addition to two simulated cases: ideal, and with realistic diode losses included. All cases give a capacitor utilization η that matches within 0.4%.

VIII. SUMMARY OF HYBRID DICKSON VARIANTS

Analysis similar to that presented in previous sections was performed on seventeen permutations of all eight Dickson variants depicted in Fig. 1 for a generalized switched capacitor conversion ratio, N. Convenient capacitor sizing regimes were selected: either those that yield two-phase operation, or all flying capacitors set equal for minimized split-phase switching complexity. The resultant duty cycles, mid-range voltages, maximum charge throughput per period, and maximum flying capacitor utilization for all topologies considered are documented in Table IV. Maximum allowable power may be obtained from the listed $q_{H,max}$ expressions, as demonstrated in (35). We also note an asymmetry in inductor currents for Dickson variants (b) and (f) at even and odd conversion ratios respectively, a consideration that may complicate component selection.

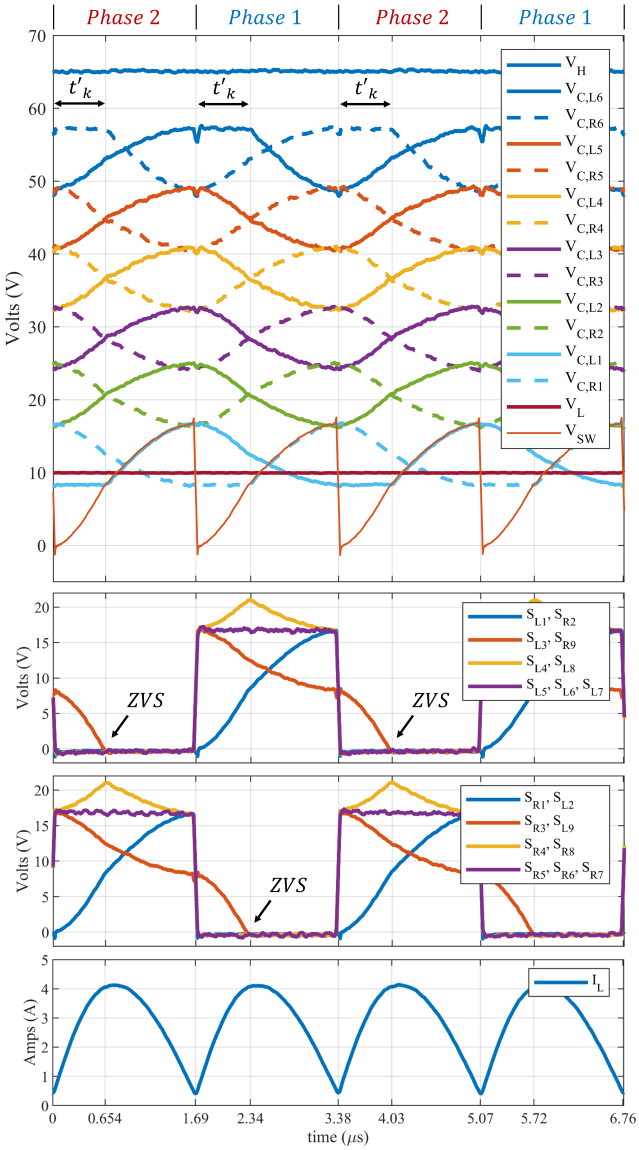

Figure 9. Measured voltage and current waveforms of a 1:7 resonant instantiation of the D-1L-direct split-phase Dickson variant analyzed in Section VI. With $V_L = 10$ V, these results validate the derivation of (63), (64), (65), and (66).

Table III
COMPARISON: MAXIMUM CAPACITOR UTILIZATION

	Theoretical		Simulated (ideal)		Simulated (w/ Loss)		Measured	
	Min (V)	Max (V)	Min (V)	Max (V)	Min (V)	Max (V)	Min (V)	Max (V)
$C_{L1,R1}$	8.75	17.5	8.75	17.49	8.21	16.64	8.39	16.85
$C_{L2,R2}$	17.5	26.25	17.5	26.24	16.39	24.8	16.62	25
$C_{L3,R3}$	26.25	35	26.25	34.99	24.54	32.94	24.52	32.68
$C_{L4,R4}$	35	43.75	34.99	43.74	32.68	41.08	32.67	40.94
$C_{L5,R5}$	43.75	52.5	43.74	52.49	40.82	49.23	40.92	49.14
$C_{L6,R6}$	52.5	61.25	52.49	61.24	48.98	57.42	48.97	57.42
η	17.27%		17.26%		17.65%		17.50%	

Table IV reiterates that indirect or tank-based topologies exhibit switch voltage stress that is largely independent of load-induced flying capacitor voltage ripple, provided switch resistance remains small.

Figure 10 plots the three distinct maximum flying capacitor utilization equations (η_{max} [A]-[C] in Table IV) and demonstrates the extent to which each of these groupings can utilize a specified total capacitor energy or size [65]. When confined to direct (non-tank) structures, split-phase approaches are

Table IV
CHARACTERISTICS OF SEVENTEEN DISTINCT DICKSON VARIATIONS.

Topology	N	Capacitor Sizing ($C_i = c_i C_0$)	Switching Scheme	Duty Cycle	Mid-range Voltages ($V_i = V_H v_i$)	$q_{H,max}$	η_{max} (Constrained by Reverse Conduction)	Switch Stress Indep. of Load
(a) S-1L-Direct	Odd	$c_{i,Odd} = \frac{N-1}{N-i}$	2-Phase	$\frac{N+1}{2N}$	$v_i = \frac{i}{N}$	$V_H C_0 \frac{2(N-1)}{N(N+1)}$	$\frac{4N}{N^2+6N+3+\frac{4(N+1)}{N-1}\sum_{i=1}^{(N-1)/2}\frac{(1-2i)^2}{N+1-2i}}$ [A]	No
(g) S-2L-Direct_PWM		$c_{i,Even} = \frac{N-1}{i}$		50% ($I_L \neq I_R$)				
(a) S-1L-Direct		$c_i = 1$ for all i		$\frac{N+1}{2N}$	$v_i = \frac{i}{N} + \frac{\Delta}{V_H}\left(\frac{N-2i+(-1)^i}{N+1}\right)$	$V_H C_0 \frac{N+1}{N(N+3)}$	$\frac{3N(N^2+4N+3)}{2N^4+13N^3+25N^2+11N+9}$ [B]	
(g) S-2L-Direct_PWM				50% ($I_L \neq I_R$)				
(a) S-1L-Direct	Even		Split-Phase	50%	$v_i = \frac{i}{N} + \frac{\Delta}{V_H}\left(\frac{N-2i}{N}\right)$	$V_H C_0 \frac{1}{N+1}$	$\frac{3(N+1)}{2N^2+5N+6}$ [C]	
(g) S-2L-Direct_PWM								
(f) D-1L-Direct						$V_H C_0 \frac{2}{N+1}$		
(f) D-1L-Direct	Odd							
(h) D-2L-Direct_PWM	Even							
(h) D-2L-Direct_PWM	Odd							
(b) S-2L-tank		$c_i = x$ for all i Even $c_i = y$ for all i Odd						
(b) S-2L-tank	Even	$L_L \sum_{i,Even} c_i = L_R \sum_{i,Odd} c_i$		50% ($I_L \neq I_R$)				
(e) D-2L-tank	Odd	$c_{L,i} = x$ for all i $c_{R,i} = y$ for all i			$v_i = \frac{i}{N}$	Weakly Bounded	$\lim_{\Delta\to\infty} \eta_{max} = 1$	Yes
(e) D-2L-tank	Even	$L_L \sum_i c_{L,i} = L_R \sum_i c_{R,i}$		50%				
(c) S-1L-tank		$c_i = 1$ for all i						
(c) S-1L-tank	Odd							
(d) S-1L-tank-alt					$v_i = \frac{2i-1}{N}$			

expected to achieve superior flying capacitor utilization at high conversion ratios, leading to smaller capacitor volume/area in practice, with a 43% increase in capacitor utilization observed at $N = 15$. Conversely, simpler 2-phase approaches may be preferable for $N < 6$.

IX. CONCLUSION

This paper describes recent hybridized variations of the Dickson power converter, a topology recognized as having best-in-class switch utilization. Eight fundamental reduced structures are described, three of which proposed here, with their evolution and key attributes highlighted. Sections IV-VI demonstrate a large signal analytical approach that may be used to obtain capacitor sizing relationships, resonant switching frequency, relative phase durations, switch-constrained maximum power throughput, and maximum flying capacitor utilization. Furthermore, we note that this is the first work to present accurate analysis for split-phase timings that account for large signal ripple in both inductors and flying capacitors. Section VII validates the preceding analysis through experimental characterization of a discrete hardware prototype that illustrates a complex case of resonant split-phase switching operating at its maximum power point.

We note that the techniques described herein can be applied to all HSC converters in general with minor adaptation, including all of the Dickson variants depicted in Fig. 1. As such, Section VIII records the analytical outcomes for seventeen permutations of the eight Dickson variants discussed, revealing that split-phase switching may be a preferable control technique at conversion ratios greater than 6:1.

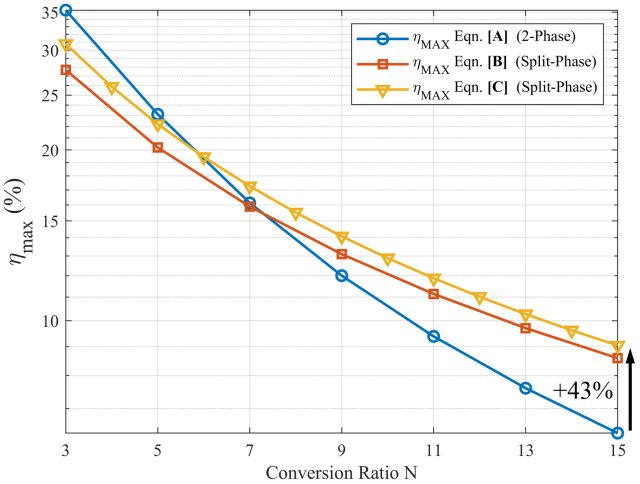

Figure 10. Maximum allowable flying capacitor energy utilization, η_{max}, plotted versus conversion ratio N for governing equations [A], [B], and [C] whose equations are listed in Table IV. Split-phase schemes see up to a 43% increase in capacitor utilization at $N = 15$, while 2-phase approaches may be superior for $N \leq 6$.

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