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UNIVERSITY OF CALIFORNIA
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Graphene Synthesis by Thermal Cracker Enhanced Gas Source Molecular Beam Epitaxy
and Its Applications in Flash Memory

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Ning Zhan

December 2011

Dissertation Committee:

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Special thank to my wife, she was always there to provide support and encouragement. She was a powerful source of inspiration and energy through my Ph.D study.

ABSTRACT OF THE DISSERTATION

Graphene Synthesis by Thermal Cracker Enhanced Gas Source Molecular Beam
Epitaxy and Its Applications in Flash Memory
by

Ning Zhan

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, December 2011
Dr. Jianlin Liu, Chairperson

Because of its unique properties, such as extremely high mobility, high mechanical strength, good optical transparency and high chemical stability, graphene has attracted vast interests in nanotechnology communities, condensed matter physics, and chemistry. The method of synthesizing large-area graphene with good quality is critical for its potential applications. This dissertation reports a new synthesis method of using a home built thermal cracker enhanced gas source molecular beam epitaxy (GSMBE) system. Chapter 2 discusses graphene growth using nickel substrate in the GSMBE system. Hydrocarbon gas molecules were broken by thermal cracker at very high temperature of 1200 °C and then impinged on a nickel substrate. High-quality, large-area graphene films were achieved at 800 °C, and this was confirmed by both Raman spectroscopy and transmission electron microscopy. A rapid cooling rate was not required for few-layer graphene growth in this method, and a high-percentage single layer and bilayer graphene

films were grown by controlling the growth time. The results suggest that in this method, carbon atoms migrate on the nickel surface and bond with each other to form graphene. Few-layer graphene is formed by subsequent growth of carbon layers on top of existing graphene layers. This is completely different from graphene formation through carbon dissolving in nickel and then precipitating from the nickel during rapid substrate cooling in the chemical vapor deposition method. Chapter 3 further discusses using cobalt as graphene growth substrate. Growth conditions including growth temperature and growth time play important roles in the resulting morphology of as-grown films. A narrow growth time window was found for different growth temperatures. Carbon absorption and desorption phenomena were responsible for temperature-dependent and growth time-dependent graphene morphology. Fast cooling rate was not required in this process due to direct growth mechanism under atomic carbon growth condition. Large-area graphene films with high single-layer and bi-layer coverage of 93% were confirmed by Raman spectroscopy and transmission electron microscopy.

Graphene based flash memory was demonstrated by using nickel nanocrystals as storage nodes in chapter 4. First, the graphene channel with a dimension of a $20\ \mu\text{m} \times 5\ \mu\text{m}$ was acquired by photolithography and oxygen plasma etching. Then, the gate stack formed by the deposition of tunneling oxide, nickel nanocrystal and block oxide. On/off operation of the transistor memory was acquired by static pulse response measurement. The memory window of the device was found up to be 23.1 V by back gate sweep. This memory effect is attributed to charging/discharging of nanocrystals. Furthermore, excellent retention and endurance performance were achieved. Chapter 5 demonstrated a

memory capacitor with an embedded graphene nano dots structure. Graphene nano dots were successfully fabricated by using nickel nano crystals as etching masks. By tuning the etching parameters, graphene dots with the size of 10 nm to 100 nm can be acquired. Raman spectra confirms the defects and the edges effect of nano dots. A memory capacitor using a SiO_2 /graphene dots/ Al_2O_3 sandwich structure was fabricated. A hysteresis from the C-V sweep proves the memory capability of the as-fabricated capacitor.

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Chapter 1: Introduction

1.1 Graphene

1.1.1 What's graphene

Graphene, a two dimensional form of carbon atoms arranged in a honeycomb lattice, consists of two inequivalent carbon atoms A and B in one unit cell. The vectors \vec{a}_1 , \vec{a}_2 are primitive vectors and form as the rhombus shape which presents as unit cell of single layer graphene in real space as shown in Figure 1-1 [1]. The carbon-carbon bond length in graphene is about 0.142 nm, making a strong bonding between each atom. For few layer graphene, the interlayer distance is 0.335 nm which leads to relative weaker interlayer bonding. Graphene is the 2-D building block for carbon materials of all other dimensionalities. Its sp^2 -bonded carbon atoms are densely packed into a one-atom-thick planar sheet. It can be wrapped up into 0D fullerenes, rolled into 1D nanotube or stacked into 3D graphite (Figure 1-2) [2].

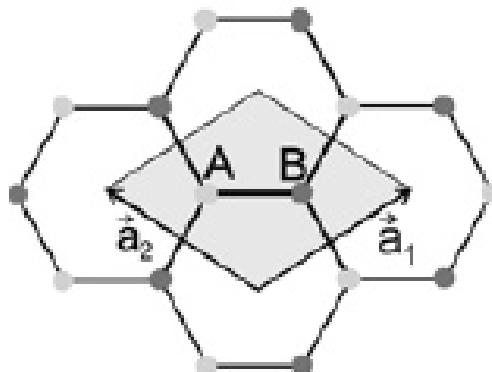


Figure 1-1 A top view of graphene showing the atoms A and B in a unit cell and unit vectors a_1 and a_2 .

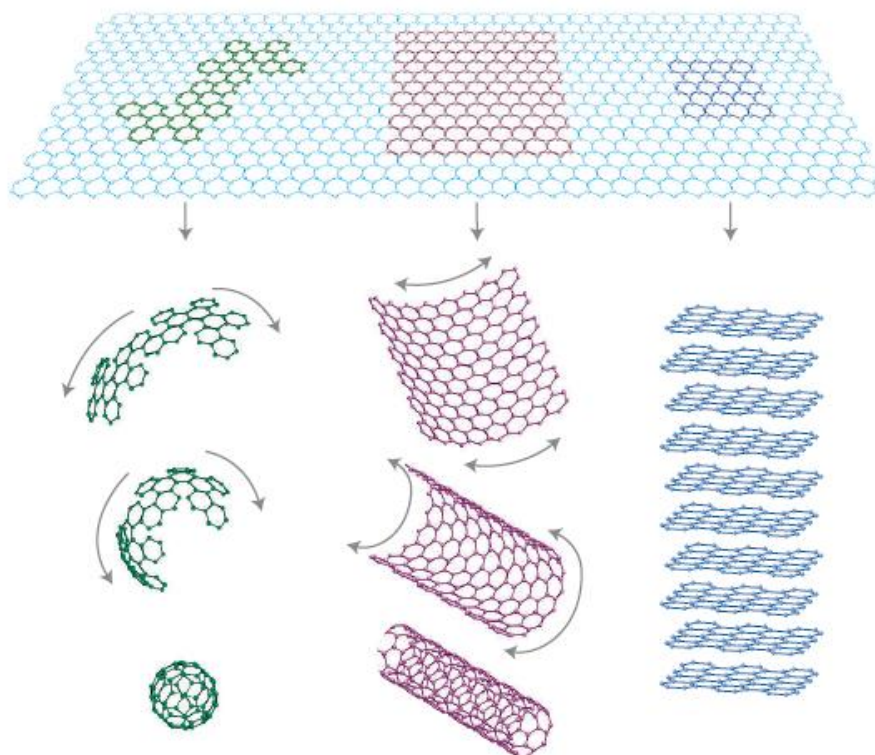


Figure 1-2 Mother of all graphitic forms. Graphene is a 2D building material for carbon materials of all other dimensionalities.

1.1.2. Graphene properties

Graphene is a semi-metal or zero-gap semiconductor which is quite different from most conventional three-dimensional materials. It was found that the E-k relation is linear for low energies near the six corners of the two-dimensional hexagonal Brillouin zone, leading to zero effective mass for electrons and holes. Secondly, because of its ballistic transport at room temperature, graphene shows remarkable high electron mobility both experimentally and theoretically. Novoselov, K. S. *et al.* reported values in excess of $15,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ even under ambient conditions [2] which is much higher than mobility of silicon ($1,400 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$). The measured mobility is nearly independent with temperature in certain range [3-4], meaning the dominant scattering mechanism is defect scattering. Due to the intrinsic scattering between acoustic phonons and electrons, the mobility is limited to $200,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at a carrier density of 10^{12} cm^{-2} [5]. Additionally, the symmetry of measured transfer curves indicates that the mobilities for holes and electrons should be nearly the same, which can also be explained by the symmetric band structures for these two carriers. Combined with the scalability of graphene device due to its 2 dimensional structure, the high electron mobility makes graphene one of the most promising candidates for post-silicon materials. Another exceptional feature of graphene is that its mobility remains the same even at high electric-field-induced concentrations, and seems to be little affected by chemical doping [6].

The linear dispersion at low energies also makes electrons and holes in graphene mimic relativistic particles that are described by the Dirac relativistic equation for particles with spin 1/2, which are usually referred to as Dirac Fermions [7]. Because of

these Dirac electrons in graphene, their spectrum show a Landau level with energy precisely at the Dirac point [8], bringing a $\frac{1}{2}$ shift in the Hall conductivity. Therefore, graphene displays an anomalous quantum Hall effect with the sequence of steps shifted by $\frac{1}{2}$ with respect to the standard sequence [9].

Graphite has been known as a high thermal conductive material (thermal conductivity of 2000 W/mK) for a long time [10]. Ever since its discovery, graphene has been considered to achieve higher thermal conductivity than that of graphite, because it shows almost zero defect and boundary scattering in theory. Recently, a thermal conductivity as high as 5000 W/mK to 10000 W/mK has been found [11-12]. It provides a promising approach for heat removing in semiconductor industry. Graphene also has other properties, such as optical transparence, chemical and mechanical stability. All the above mentioned properties of graphene make it widely researched by people in different fields.

1.1.3 Graphene production methods

In order to use graphene for applications in nano-electronics and condensed matter physics, large area graphene production method is needed. At present, three major categories are proposed in literature.

1.1.3.1 Mechanical exfoliation

The first category was invented by K. S. Novoselov, *et al.* in Science [13]. He used nano-mechanical exfoliation method to produce small area films. In his paper, 1-mm-thick platelets of highly-oriented pyrolytic graphite (HOPG) were used as starting materials. After dry etching in oxygen plasma, they obtained 5 μm -deep mesas on top of the platelets. The structure surface was then pressed against a layer of a fresh wet photoresist spun over a glass substrate. The mesas became attached to the photoresist layer after curing; the rest of the HOPG sample was cleaved off. Then, by using scotch tape, people started repeatedly peeling flakes of graphite off the mesas. Thin flakes left in the photoresist were released by acetone. Then, a Si wafer was dipped in the solution and in plenty of water, graphene flakes became captured by the wafer's surface (Si substrate with 300 nm SiO_2 on top). After Novoselov's first discovery, researchers improved this method based on his original one. Scotch tape was directly pressed against HOPG, after firmly adhering, it was peeled off and pressed on SiO_2 (300nm)/ Si. The graphene flake was left on top of SiO_2 substrate by peeling off the tape again. This mechanical exfoliation approach can provide graphene with highest mobility compared to all other production methods, but it typically only produces films on the order of a few tens of micrometers, which is not suitable for practical application.

1.1.3.2 SiC graphitization

The second category has been reported as graphitization of single crystal SiC [14][15]. In this method, ultrathin epitaxial graphite films were produced on the SiC by thermal desorption of Si. After surface preparation and cleaning, SiC substrate was transferred into ultrahigh vacuum (base pressure: 1×10^{-10} Torr), and then was heated up to temperatures ranging from 1250 °C to 1450 °C for 1-20 min. At these temperatures, thin graphite layers formed while silicon atoms desorbed from the substrate, with the layer thickness determined predominantly by the temperature. This process produces wafer-size graphene, however, does not easily get electrically isolated mono- or bilayer graphene for device applications. Also, graphene produced by this method usually is very fragile and contains many defects due to the large lattice mismatch between the SiC substrate and graphene itself. Additionally, large area production is also limited by expensive SiC substrate.

1.1.3.3 Chemical synthesis

The third category is using hydrocarbon gas or organic chemical to form graphene on metal surface. It has been known for decades that hydrocarbon gas can be decomposed on certain metals in Chemical Vapor Deposition (CVD) system [16]. But only from recent years did people start to use this mechanism to synthesize graphene. Previous works show that well defined graphite layer can be achieved by carbon segregation from metal substrates and metal carbides held at high temperature in an

equilibrium segregation process. However, the number of segregated graphene layers cannot be preserved at room temperature due to non equilibrium phase while cooling the sample. Therefore, research on how to control graphene segregation during cooling process is necessary for synthesizing good quality graphene by carbon segregation. Q.Yu first reported using nickel foil as substrate to grow graphene [17]. In his paper, Ni foil was placed in a chamber at high temperature (1000 °C) with inert gas protection. Then, methane was introduced into the chamber providing carbon source. The Ni substrate broke the attached hydrocarbon gas molecular and functioned as catalyst here. Carbon atoms dissolved into Ni substrate afterwards. Also, the concentration of carbon decreased exponentially from the surface into the bulk. This growth step was kept within a short time to keep a low carbon concentration. After the carbon dissolution, the system started to cool down, leading to carbon segregation on Ni surface. Different cooling rates were tried and led to different segregation behaviors. In this case, when the cooling rate is extremely fast (>20 °C/S), the dissolved carbon atoms lose the mobility before they can diffuse resulting in no carbon growth on surface. With a wide range of medium cooling rates, a finite amount of carbon can segregate at the surface leading to graphite or few layer graphene growth. When the cooling rate keeps further lowering, carbon atoms will have enough time to diffuse into the bulk, so there will not be enough carbon segregated at the surface to form graphene either [17]. With tuning the growth conditions, graphene films with reasonable quality can be achieved, this is the first systematical research on using non equilibrium carbon segregation to synthesize graphene.

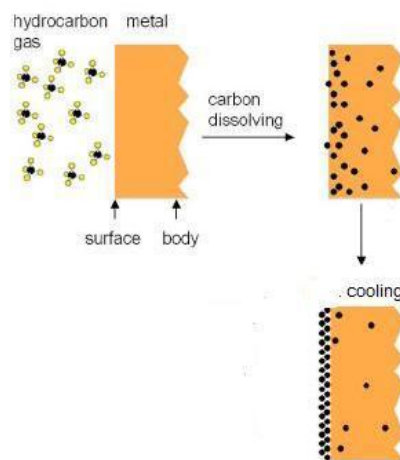


Figure 1-3 Illustration of carbon segregation at metal surface.

Because large amount of dissolved carbon atoms in metal foil tend to form thick graphite, A. Reina [18] proposed to use thin nickel layer (~300nm) for graphene growth substrate. Ni films are usually placed in a CVD chamber and heated up to high temperature (1000 °C). Then hydrocarbon gas (CH_4 , C_2H_4 or C_2H_2) mixed with Argon and Hydrogen flows through the chamber. During gas flowing, the hydrocarbon gas is decomposed by the metal, and carbon dissolves into metal film, as shown in Figure 1-3 [17]. After incorporating gas, the chamber is cooled down. Because the solubility of carbon in Ni decreases with the decrease of temperature, the oversaturated carbon tends to segregate onto surface and form as graphene. Researchers claim that this cooling rate is also very critical for few-layer graphene synthesis [19-20]. In order to get single layer or few-layer graphene, rapid cooling rate is necessary to suppress multilayer information. If the system is cooled very slowly, large part of the dissolved carbon will have enough time to segregate onto surface. Unlike a medium cooling rate is required to form good quality graphene films in Yu's paper, a rapid cooling is necessary for graphene synthesis

in references [19-20]. The reason is 300nm Ni film instead of Ni foil was used as growth substrate. Therefore, carbon atoms cannot dissolve too deeply into bulk, which makes it possible for carbon segregating onto surface with a rapid cooling. Additionally, thin layer of Ni film also limits the overall amount of carbon, bringing better controllability of carbon segregation. Besides nickel, other metals have also been tried for graphene synthesis, such as Ru [21], Co [22-24] and Ir [25] which have very similar growth mechanism as Ni. Due to the requirement of rapid cooling rate, the morphology of as-grown graphene films can easily be affected during cooling period, to solve this problem, we proposed to use our thermal cracker enhanced gas source molecular beam epitaxy system (GSMBE) for graphene growth, more details are given later.

Another widely used metal for graphene synthesis is Cu. It was first discovered by Li et al. [26]. Besides that Cu has wafer-scale production ability as Ni does, it was found that Cu can also provide a good control on the uniformity of as-grown films due to a different mechanism. Carbon was found to adsorb on copper surface rather than dissolve into Ni first then precipitate to surface [27]. Li et al used carbon isotope labeling to track carbon growths for Ni and Cu cases. They took advantage of the separation of the ^{12}C and ^{13}C Raman modes to observe the spatial distribution of graphene domains. The ^{12}C -graphene and ^{13}C -graphene have different G peak locations as shown in Figure 1-4, and these two G peaks Raman mapping were used to track the distributions of ^{12}C and ^{13}C . Then, to understand the carbon growth mechanisms for these two cases, a sequential dosing of $^{12}\text{CH}_4$ and $^{13}\text{CH}_4$ was introduced into system as carbon source. For the graphene growth using Ni as substrate, a uniform distribution of ^{12}C and ^{13}C was found all over the

as-grown films while separated isotopes were shown on Cu sample (Figure 1-5). The reason for the even distribution of ^{12}C and ^{13}C isotopes in Ni case is given as follows. Both $^{12}\text{CH}_4$ and $^{13}\text{CH}_4$ were broken by Ni surface, and carbon atoms dissolved into metals at the time when the gas was introduced. ^{12}C and ^{13}C were evenly mixed together at high temperature and precipitated to metal surface while cooling down. For Cu synthesized graphene, because of much lower solubility of C in Cu as compared to that in Ni, only a small amount of carbon can be dissolved in Cu, and the carbon source for graphene growth is mainly from the CH_4 that is catalytically decomposed on the Cu surface. As a result, once the surface is fully covered with graphene, the Cu catalyst is no longer able to react with further CH_4 molecules, leading to the termination of carbon growth. Carbon atoms grow more easily at areas with imperfectness and boundary working as nucleation sites while slower at others, which contribute to the separated isotopes mapping as in Figure 1-5.

After synthesis, the graphene film strongly attaches to the metal surface. Since these metals are conductive materials, graphene cannot be placed on top of them for the purpose of potential electrical applications. Researchers use acidic solutions (HCl or FeCl_3) to etch underneath metal film. A layer of ethyl-methacrylate (PMMA) is spun on as-grown sample first, and then the whole sample is dipped into acidic solution. After several hours, the solution etches the underneath metal film, making PMMA/Graphene film floating. Arbitrary substrates can be used to take out the floating film, and then the PMMA is dissolved by acetone rinse. In summary, this synthesis method can provide up to 30 inch graphene film production, which was demonstrated by Samsung [28]. The

quality of as-grown films can be easily controlled by growth conditions. And inexpensive metal substrate also makes this synthesis method possible for mass production.

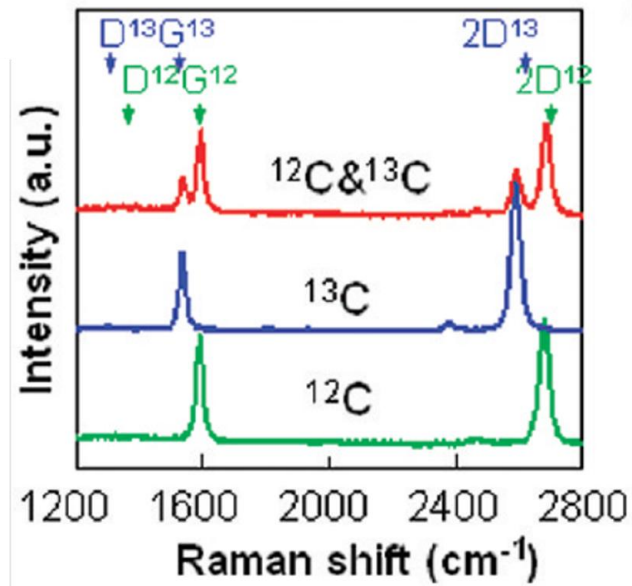


Figure 1-4 Raman spectra from ¹²C-graphene (green), ¹³C-graphene (blue), and the junction of ¹²C- and ¹³C-graphene (red), respectively [27].

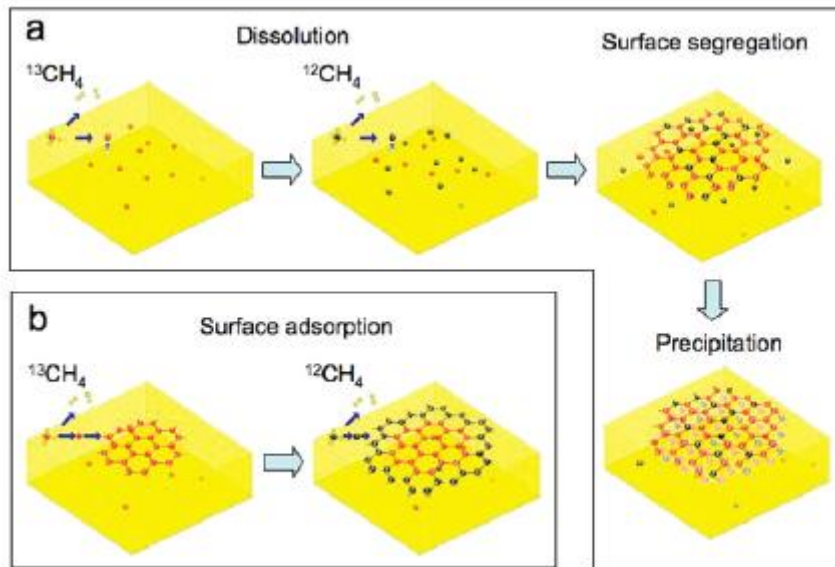


Figure 1-5 Schematic diagrams of the possible distribution of C isotopes in graphene films based on different growth mechanisms for sequential input of C isotopes. (a) Graphene with randomly mixed isotopes such as might occur from surface segregation and/or precipitation. (b) Graphene with separated isotopes such as might occur by surface adsorption [27].

1.1.4. Graphene devices

1.1.4.1 Flexible devices

Graphene has been implemented into various types of device since it was first discovered. Because of its good optical transparency, outstanding electrical, mechanical and chemical properties of graphene, it has attracted tremendous attention in flexible electronics. A group from Korea has achieved 30 inch graphene sheet with 97.4% optical

transmittance. The graphene film was grown with copper roll-to-roll method [28]. First, an 8-inch-wide tubular quartz reactor was used in the CVD system, and a roll of copper foil with dimensions as large as 30 inches was wrapped around the tube. The temperature gradient was well controlled to prevent the inhomogeneous graphene growth at different locations. As in other graphene synthesis methods, the roll of copper foil was heated to 1000 °C in hydrogen for 30 min to pre-clean copper surface. This pre-annealing process was also found to be able to increase copper boundary sizes. As reported in references [19-20, 27], the as-grown graphene boundary size is proportional to the size of the copper substrate. Hence, this pre-annealing process is necessary for good quality graphene growth. After pre-cleaning, a mixture of hydrocarbon gas and hydrogen were introduced into CVD for carbon growth, and the chamber was then cooled to room temperature after that. A thermal release type was attached to as-grown sample and transferred graphene to polyethylene terephthalate (PET) substrate after copper was etched [28].

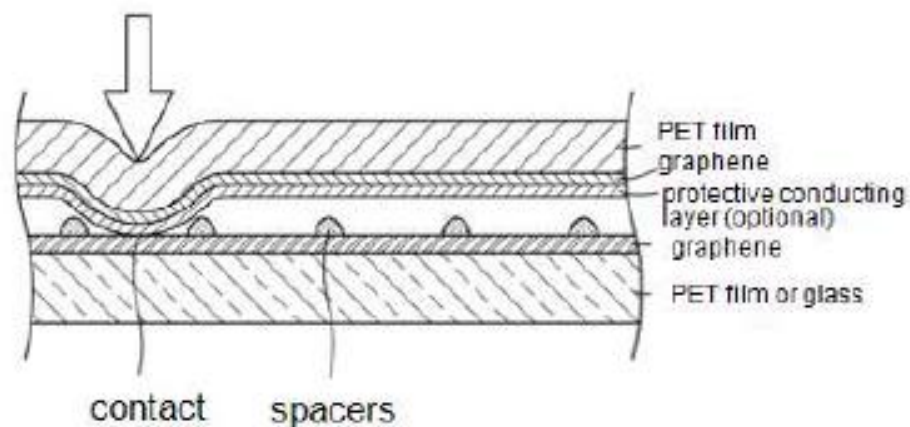


Figure 1-6 The structure of graphene based touch screen devices [28].

The major component of traditional transparent electrode is indium tin oxide (ITO) which has excellent sheet resistance of less than 100 Ω per square and optical transparency of 90%. ITO is widely used in solar cells, touch sensors and flat panel displays. To replace ITO with graphene for applications in flexible electronics, sheet resistance and optical transparency are two critical parameters. After graphene was transferred on PET substrate, a touch screen structure was fabricated as shown in Figure 1-6. The sheet resistance was tested as 125 Ω per square which is very close to that of ITO. The optical transparency was measured as 97.4% by UV-vis spectra [28]. The resistance can be further decreased to 50 Ω per square by doping the films at the expense of lowering the optical transparency to 90%, which is superior to commercial ITO electrode. With the lower manufacture price and also unlimited scalability, graphene replacement over ITO in flexible electronics can be realized in the near future.

1.1.4.2 Radio frequency devices

The most attractive property for graphene is its potential application as post silicon materials in semiconductor industry. Because of high carrier mobility, graphene MOSFET with gigahertz capability has been reported by IBM [29]. Few-layer graphene was made by SiC graphitization method. To form the gate stack, an interfacial polymer layer made of a derivative of poly-hydroxystyrene was spin-coated on the graphene before dielectric deposition. The reason for doing so is to prevent defects and interface scattering between the graphene channel and the dielectric film. Then, a 10-nm-thick HfO_2 was deposited on the graphene as gate dielectric with two gate lengths of 550 nm and 240 nm. The field effect mobility was tested between 800 $\text{cm}^2 \text{V}^{-1}\text{s}^{-1}$ and 1500 $\text{cm}^2 \text{V}^{-1}\text{s}^{-1}$.

s^{-1} . To assess RF characteristics of the graphene FET, on-chip microwave measurements vector network analyzer was used with ground signal-ground (GSG) coplanar probes. After transferring the measured S parameters to H parameters, the current gain for all devices shows the $1/f$ dependence, from which a well-defined cut-off frequency f_T can be defined. As we know, cut-off frequency is reversely proportional to gate length. The device with the gate length of 550nm shows a f_T of 53 GHz, while 240nm gated device has the highest f_T of 100 GHz (Figure 1-7) [29], which is higher than that of a silicon MOSFET with a similar gate length.

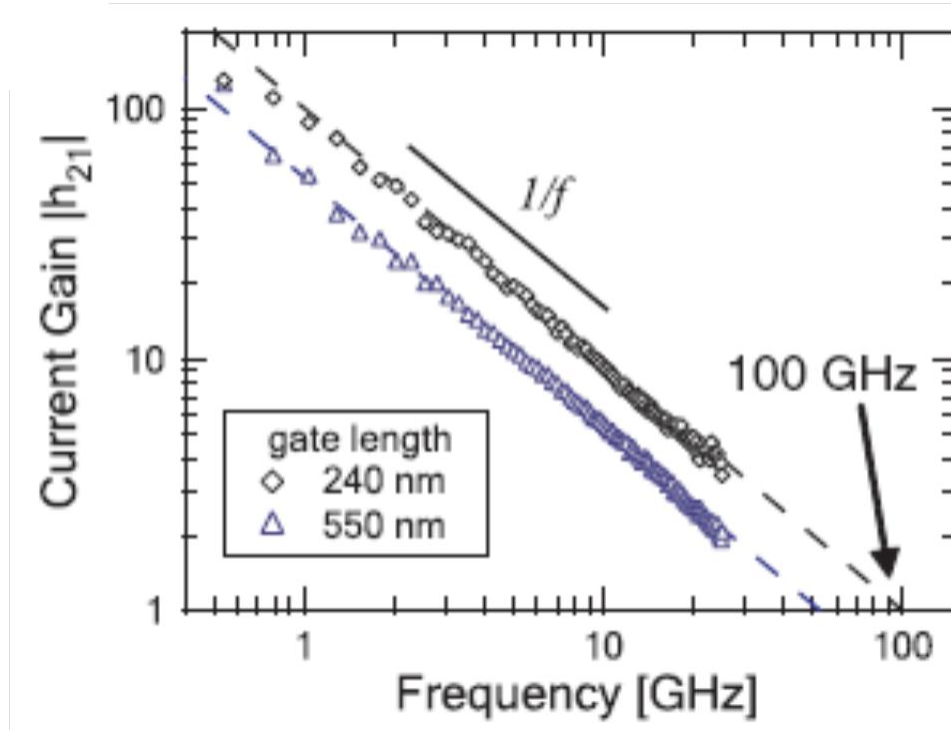


Figure 1-7 Measured small-signal current gain $|h_{21}|$ as a function of frequency f for a 240-nm-gate (\diamond) and a 550-nm-gate (\triangle) graphene FET at $V_D = 2.5$ V [28].

Since the cut-off frequency closely depends on carrier mobility and gate length, researchers are putting a lot of efforts to decrease gate length and the scattering between graphene channel and dielectric [29]. Nanowires have been used as etch masks for small feature devices fabrication for a long time. Recently, people started to use nanowires to pattern graphene FET devices to shrink gate length. A group from UCLA proposed using $\text{Co}_2\text{Si-Al}_2\text{O}_3$ core-shell nanowire for graphene FET fabrication [30]. The metallic Co_2Si was grown by CVD furnace then transferred on mechanical exfoliated graphene film. A 5nm layer of Al_2O_3 was deposited on the sample afterwards. After the source/drain patterning by electron-beam lithography, buffered oxide etchant was used to etch top layer Al_2O_3 and expose the Co_2Si . After then, a metal deposition process was introduced to form gate contact. The structure of the fabricated device is shown in Figure 1-8. Despite of unsatisfying current saturation behavior, the much better performance of graphene transistors compared to that of silicon MOSFETs is certainly impressive. Because the Al_2O_3 grew around the Co_2Si core rather than on the graphene surface, the interface scattering between graphene and Al_2O_3 is much lower than usual. Additionally, the gate length was decreased to 140 nm by the self-aligned nanowire gate. A cut-off frequency of 300 GHz was achieved with this gate length. With further decreasing graphene gate length and improving interface quality, graphene transistors with even higher cut-off frequency can be realized soon.

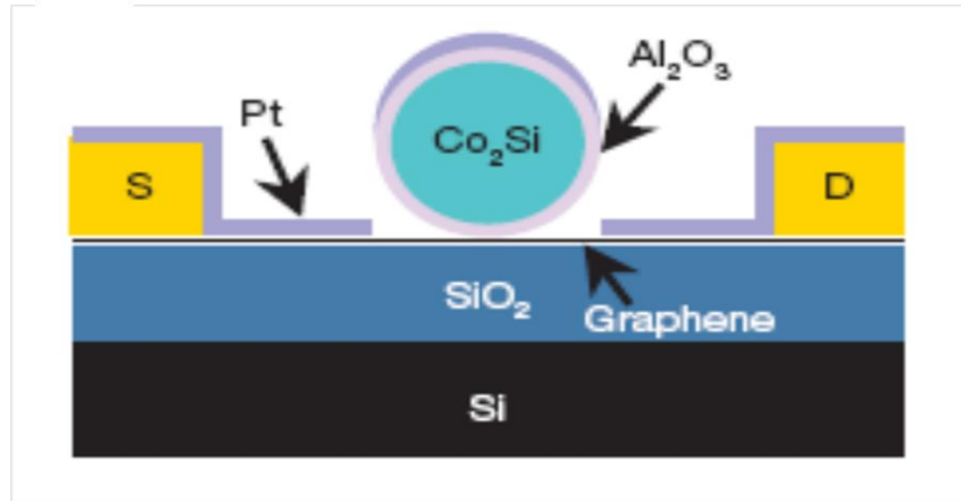


Figure 1-8 Schematic of the cross-sectional view of the graphene channeled Co_2Si – Al_2O_3 core–shell nanowire device.

1.1.4.3 Digital devices

Modern digital circuits require devices with a high on/off ratio for low power consumption and device integration. In silicon technology, an on/off ratio of more than a million is usually achievable in complementary metal oxide semiconductor (CMOS) structure. However, a graphene based device cannot be fully turned off due to the zero bandgap, which limits the on/off ratio to less than 10 [18]. Therefore, a bandgap opening is required for integrating graphene into digital circuits. Three major ways have been proposed to open a bandgap for graphene: constraining graphene into one dimension nanoribbons [31], strain engineering graphene [32] and electrically biasing bi-layer

graphene [33]. It was calculated and measured that a bandgap excess of 200 meV for graphene nanoribbons narrow than 20 nm. However, the edges of graphene nanoribbons can be armchair, zigzag and a mix of these two. The opened bandgap strongly depends on the edge type, while the precise control of the edge is almost impossible for current patterning technology. Additionally, a rough edge also severely decreases the carrier mobility and the performance of devices. Hence, various approaches for better controlling the edges of graphene nanoribbons are proposed.

Strain engineering graphene was also found to be able to open a bandgap. But it seems that opening a gap in this way requires a global uniaxial strain exceeding 20%, which is difficult to be achieved in practice. Bi-layer graphene is also gapless by nature. Its valence and conduction bands have a parabolic shape near the K point. But a bandgap can be opened if an electric perpendicular field is applied. As confirmed by experimental testing, a theoretical simulation has also found a big bandgap of 200-250 meV for high fields $((1-3) \times 10^7 \text{ V/cm})$. This bandgap opening has been consistently observed for graphene produced by various methods including exfoliation, SiC graphitization and chemical synthesis, which makes it more suitable for potential applications compared to other two opening methods.

1.2 Memory

1.2.1 Memory introduction

Hard disk drive, optical disc (CD, DVD and blue-ray) and memory are three major categories for modern data storage devices. Hard disk drive features rotating rigid platters on a motor-driven spindle within a protective enclosure. Data is magnetically read from and written to the platter by read/write heads that float on a film of air above the platters. Hard disk drive has decreased in cost and physical size over the years while dramatically increased in capacity since it was first invented in the year of 1956. The optical disc device use optical property of the storage materials such as polycarbonate to record digital “1” and “0”. To read the data, a laser beam is focused on the polycarbonate layer first. The change in height on the layer surface results in a difference in the way the light is reflected. By measuring the intensity change with a photodiode, the data can be read from the disc.

Unlike hard disk that uses only magnetic technology or optical disc that uses only optical technology, memory uses various kinds of technologies. Hence, memory technology can be further divided as semiconductor memory, magnetic memory and biological memory, according to what technology is used. Among them, the most dominant one is semiconductor memory. It uses semiconductor-based integrated circuits to store information. Typically, a memory chip may contain millions of tiny transistors or capacitors. A memory is called “volatile memory”, if data is lost after the power turned off. Otherwise, the memory belongs to “nonvolatile memory”.

1.2.1.1 Volatile memory

In the category of volatile memory, dynamic random-access memory (DRAM) and static random-access memory (SRAM) are two most massively manufactured devices. A DRAM cell consists of one transistor and one capacitor. The capacitor can be either charged or discharged, and these two states represent the two values of a bit, logical “0” and “1”. Because capacitor leaks charge, the stored charges eventually fade. A periodical refreshing of devices is needed to maintain data. Due to this refresh requirement, it is called as a dynamic memory as opposed to SRAM and other static memories. Since only one transistor and one capacitor are required for DRAM unit cell, this structural simplicity allows DRAM to achieve very high data storage density. Billions of unit cell can fit on a single memory chip.

SRAM consists of six transistors as shown in Figure 1-9 [34]. Each bit in an SRAM is stored in four transistors (M1-M4). Two inverters (M1-M2, M3-M4) are cross-coupled to form two stable states. Two additional access transistors (M5-M6) control the access to unit cell for read and write operations. Because of this bistable latching structure, SRAM doesn’t need to be periodically refreshed, but the stored data will be lost if the V_{DD} is not powered, so SRAM still counts as volatile memory. Since more transistors are needed for SRAM than for DRAM, the price for SRAM is much higher than that of DRAM. However, SRAM consumes much lower power since it requires no

periodical refreshing and provides fast I/O speed, making it very suitable for central processing unit (CPU) cache.

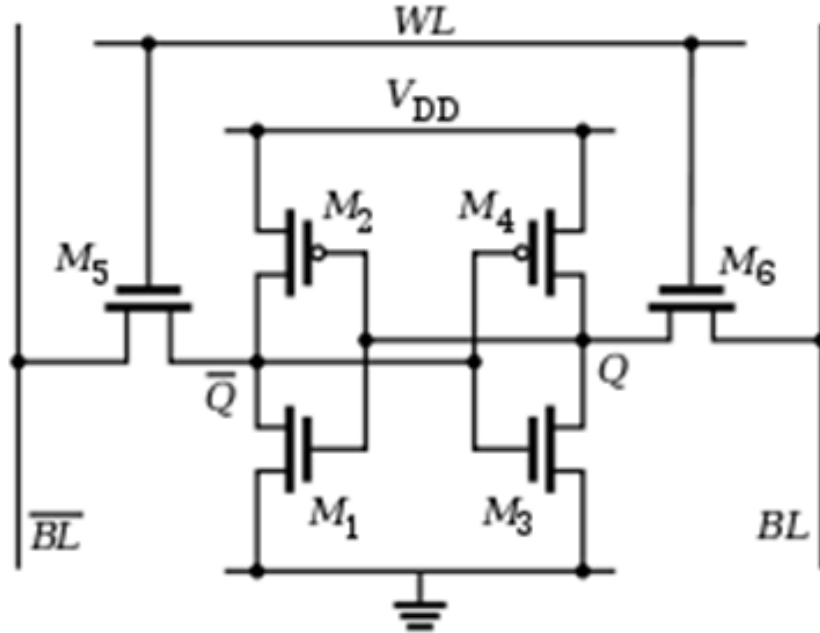


Figure 1-9 A structure of SRAM unit cell [34].

1.2.1.2 Nonvolatile memory

Nonvolatile memory (NVM) retains the stored information even when the device is not powered. NVM is typically used for the task of secondary storage, or long-term persistent storage, such as digital camera, storage card and cell phone. Examples of NVM include flash memory, magnetic random access memory (MRAM), ferroelectric random access memory (FeRAM) and phase change memory (PCM). The discussion about flash

memory is given in a separated section later in this thesis. Only other three types of NVM are discussed here.

Unlike in other types of NVM, the data in MRAM is stored by magnetic storage unit cells rather than by electric charges or current flows. Each unit cell consists of two ferromagnetic plates which are separated by a thin insulating layer. Between these two plates, one is a permanent magnet fixed to a particular polarity; the other's field can be changed according to external field for data storage. The operation mechanism of MRAM device is given as follows. First of all, a particular unit cell is addressed by powering the associated transistor. The electrical resistance of the unit cell changes with different combinations of the orientation of the magnetic fields in the two plates. If the two plates have the same polarity, the unit cell has a low resistance state which is defined as logic "1", while if the two plates have the opposite polarity, the high resistance state makes the unit cell defined as logic "0". Because of its simple structure, MRAM can easily achieve a high density as DRAM can. At the same time, periodic refreshing is not required for data storage due to the usage of the magnetic materials, leading to low power consumption for MRAM. Hence, MRAM has been considered as one of promising candidates to replace both DRAM and SRAM. However, to date, MRAM has not been widely adopted in the market. The reason is that the manufacture technology for MRAM is quite different with other types of NVM, and further development is needed for massive production.

FeRAM is a random access memory which has similar construction to DRAM but uses a ferroelectric layer instead of a dielectric layer to achieve memory effect. As mentioned before, the capacitor in DRAM is charged with electrons to store data. For a FeRAM unit cell, logic “0” and “1” are defined by the polarization of the electric dipoles in the crystal structure of the ferroelectric materials. When the electric dipoles are oriented to one direction, it represents “1”, and it represents “0” when the electric dipoles are oriented to the opposite direction. The ferroelectric characteristic has hysteresis loop with the change of applied electric field. When an external electric field is applied, the positions of atoms and distributions of electronic charge in the crystal structure will have a small shift, which align the dipoles with the field direction. After the applied field is removed, the dipoles remain the same polarization until the opposite electric field is applied. The reading operations between DRAM and FeRAM are different. In a FeRAM cell, if the cell is written with a “0” by a negative voltage, then if a negative voltage is used to read the data, nothing will happen to the output. But if the cell is written with a “1”, a negative reading voltage will induce a current pulse due to the change of the polarized dipoles. A further operation is required to rewrite “1” back to the cell. High density can also be achieved by FeRAM due to the similar simple structure as DRAM. Additionally, periodical refreshing is not necessary as it is in DRAM, leading to much low power consumption.

PCM has two terminals with chalcogenide glass filling in between. The chalogogenide glass can be either conductive or isolative depends on the state of the material. The crystalline state makes two terminals electrically shorted which represents

“1”, while the amorphous state isolates two terminals indicating “0”. Chalcogenide is also used in optical data storage technology, such as CD and DVD, while the optical property is manipulated instead of electric resistivity. In PCM cell, the resistivity of chalcogenide can be changed by passing through an electrical current. When the temperature increases above the crystallization point due to joule heat, the chalcogenide will transform into a crystalline state with a much lower resistance. Because of its simpler structure compared to DRAM and FeRAM, PCM can achieve even higher memory density. However, PCM also has drawbacks as follows. Firstly, the greatest challenge for phase-change memory has been the requirement of high programming current density ($>10^7$ A/cm²; compared to 10^5 - 10^6 A/cm² for a typical transistor or diode) in the active volume [35]. The heat dissipation is a severe issue for using PCM in circuits. Secondly, the junction between hot phase change region and the adjacent material is also a problem. The heat dissipated from active area tends to make the dielectric leaks. Finally, the long-term resistance of the amorphous state slowly increases, leading to a drift of threshold voltage, which jeopardizes the operation of the cell if the drift is larger than the designed value.

1.2.2 Flash memory

1.2.2.1 The basic structure and program/erase operations

Like the other memories discussed in the last section, flash memory is also nonvolatile memory device which can be electrically programmed and erased. The only difference between a flash memory cell and a regular digital cell is the embedded floating

gate inside gate dielectric (Figure 1-10). The floating gate works as a charge reservoir to store data. By applying a high enough positive voltage, electrons from channel will have energy to tunnel through the oxide layer and be captured by the floating gate. Since the floating gate controls at least part of the underlying transistor channel, the charge on this gate will directly influence the current in the channel. For a NMOS device, the typical neutral transfer curve is shown in Figure 1-11. By extrapolating the linear region between drain current I_{DS} and gate voltage V_{gate} , the threshold voltage V_{th} can be acquired as the interception with x axis. V_{th} is defined as the gate voltage at which the device is turned on. After electrons are programmed into the floating gate, the extra electric field generated by stored charges will shift the V_{th} and $I_{DS} \sim V_{gate}$ curve right. With the same reading voltage as previous V_{th} , the device shows “off” state instead of previous “on” state, corresponding to logical “1”. On the other hand, by applying a high enough negative voltage to the gate, electrons can be erased from the floating gate to the channel, leading to the opposite shift of V_{th} and the operation of writing a “0” to the device.

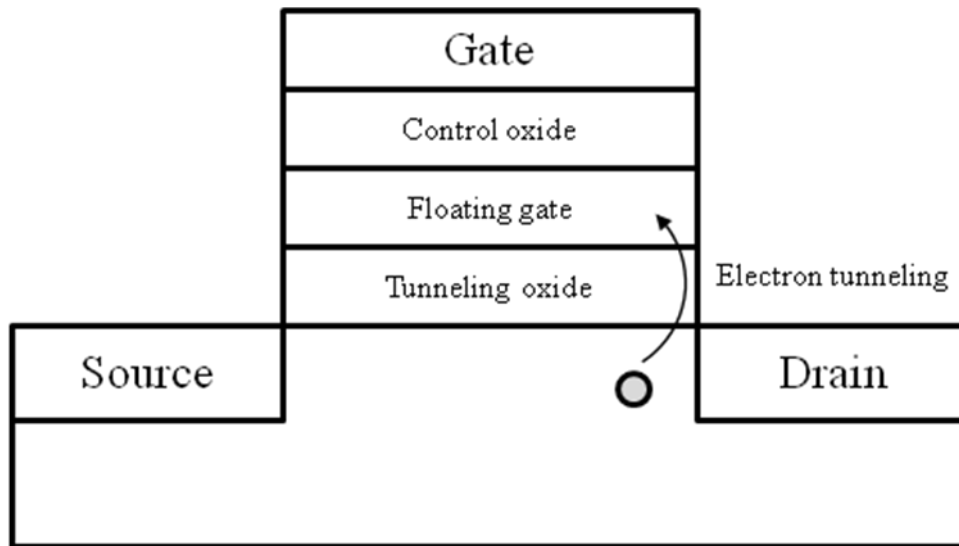


Figure 1-10 A structure of flash memory cell.

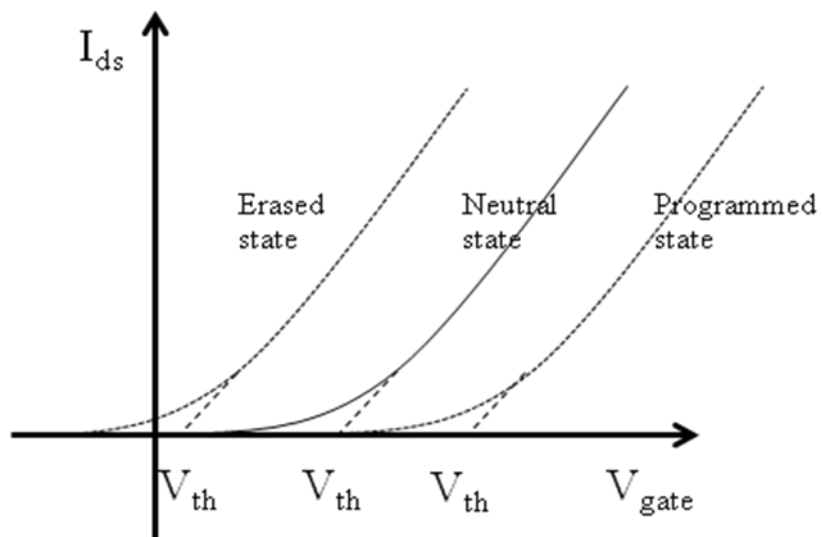


Figure 1-11 Drain current versus gate voltage for a memory device at neutral state, programmed state and erased state.

1.2.2.2 Endurance

Because strains and traps introduced by electrons tunnel through the oxide during program/erase operations, the oxide gradually degrades in its lifetime, and such degradation will jeopardize the performance of the memory device. To understand this effect, the endurance of the device is introduced and defined as the ability to perform according to the specifications when subjected to the repeated program/erase cycling.

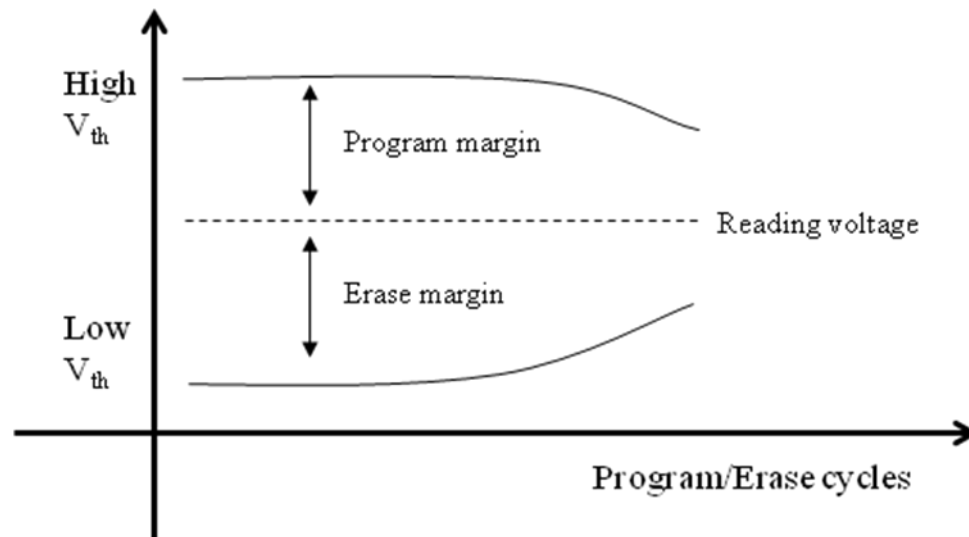


Figure 1-12 The endurance testing of a flash memory device.

When looking at a single flash memory, the intrinsic endurance is usually monitored by measuring the threshold voltage window as a function of the number of program/erase cycles (Figure 1-12). With the increase of the cycles, the high V_{th} of programmed state and low V_{th} of erased state start to merge due to the device degradation, which shrinks the threshold voltage window between two states. In theory, as long as the high V_{th} is bigger than the reading voltage, the program margin is positive, and the stored

“1” can be distinguished by circuits. In other words, the erase margin also needs to be bigger than zero to maintain the stored “0”. However, the high/low V_{th} has a distribution for different memory devices in one chip, which makes the minimum of program/erase margin a positive number instead of zero.

An important remark is that the above device-level endurance test always underestimates the real lifetime of the device because a large number of cycles are applied to the device in a very short period in order to reduce test time. In practice, there will be more time between cycles, and the degradation will be relaxed because of recovery effects such as, for example, charge detrapping from the oxide [36]. The actual *extrinsic* endurance is tested at circuit-level and can be much different with the device-level endurance testing. Two aspects can cause the circuit-level failure. One is the breakdown events of memory cells. If there is a distribution for the failure time for different memory cells, some cells can fail much sooner than other cells. The larger the memory chip is, the sooner the first cell in the chip fails. To prevent the disfunction of a whole chip due to only several failed cells, a certain amount of redundant cells are fabricated in the chip by design. The other one is the failure of peripheral circuitry. There is possibility that the sense amplifier determines the threshold voltage at which an erased cell will be detected as having been “written”. A change of endurance testing results between device-level and circuits-level can be observable only if the combination of the characteristic changes and the readout circuitry is unfavorable [36].

1.2.2.3 Retention

A nonvolatile memory device should have the ability of containing its stored data without powering the device. The retention performance of a flash memory device is defined as the ability to retain valid data over a prolonged period of time. Usually, the retention performance is conducted by measuring threshold voltage changes with time. With extrapolating the trend of the relation, an estimated value of time can be acquired. There are several mechanisms relating to the loss of the charges from floating gate, such as intrinsic charge loss, oxide defects, tunneling oxide breakdown, hole injection from top gate, ionic contamination and cycling induced charge loss [37, 38]. The effects of different mechanisms to the retention performance are different. To distinguish these effects, a temperature dependent retention testing is proposed [37, 38]. This is usually characterized by measuring retention performance at different high temperatures. With the acceleration created by high temperatures, the loss of charges becomes severer, leading to a shorter retention time. In practice, the retention time has an exponential relationship with the testing temperature as followed.

$$t_{\Delta V_{th}} \propto \exp\left(\frac{E_A}{kT}\right)$$

Where $t_{\Delta V_{th}}$ is retention time, E_A is activation energy, k is Boltzmann's constant and T is temperature. For different charge loss mechanisms, active energies are different. For the memory using standard poly-Si and SiO₂ as floating gate and tunneling oxide, the intrinsic charge loss has the highest activation energy of 1.4 eV. This mechanism refers to the fact that the stored electrons actually jump over the physical barrier between

polysilicon gate and tunneling oxide. The charge loss through the oxide defects usually only has a small activation energy of 0.6 eV, while tunnel oxide breakdown has an even smaller activation energy (0.3 eV). Ionic impurities such as mobile ions which are released from the dielectric layers or from the passivation layer also play a very important role for device retention. When attracted by the applied electric field, they tend to move into gate stack and compensate certain portion of stored charges which leads to an accelerated electron loss. This mechanism also has an activation energy of 1.2 eV. The actual numbers of activation energies for different mechanisms give us an accurate estimation of the dominate charge loss reason for a given device. Hence, it provides us a solution to improve the retention performance for flash memory cell [36].

1.2.3 Graphene and carbon nanotube flash memory

As two candidates for post-Si materials, carbon nanotube (CNT) and graphene have been used for flash memory fabrication since they were discovered. Since both of them can be semiconductor materials at certain circumstances, field effects can be acquired by using them as device channel.

In CNT case, CNT was grown by standard CVD method first, and then transferred onto SiO₂ covered Si substrate. As discussed before, a tunneling oxide and storage layer are needed for flash memory devices. But the defects and interface traps in oxide usually can also be used for storing charges. Hence, a layer of dielectric such as HfO₂ has the same function as that of floating gate. Some researchers even have both

sides of CNT deposited with dielectric layer to enhance the memory performance as shown in Figure 1-13 (a) [39]. After that, the source and drain areas are formed by depositing metal contacts on the two ends of CNT, and the highly doped Si substrate is directly used as back gate. A hysteresis can be observed by the $I_{DS} \sim V_G$ sweep (Figure 1-13 (b)), indicating memory effect is achieved by such structure. Because CNT typically doesn't have a good interface with dielectric, one major source of the memory effect is the charge trapping and de-trapping of interface defects. Another source is the charge storage of oxide traps which attribute to imperfection of as-grown dielectrics specially HfO_2 .

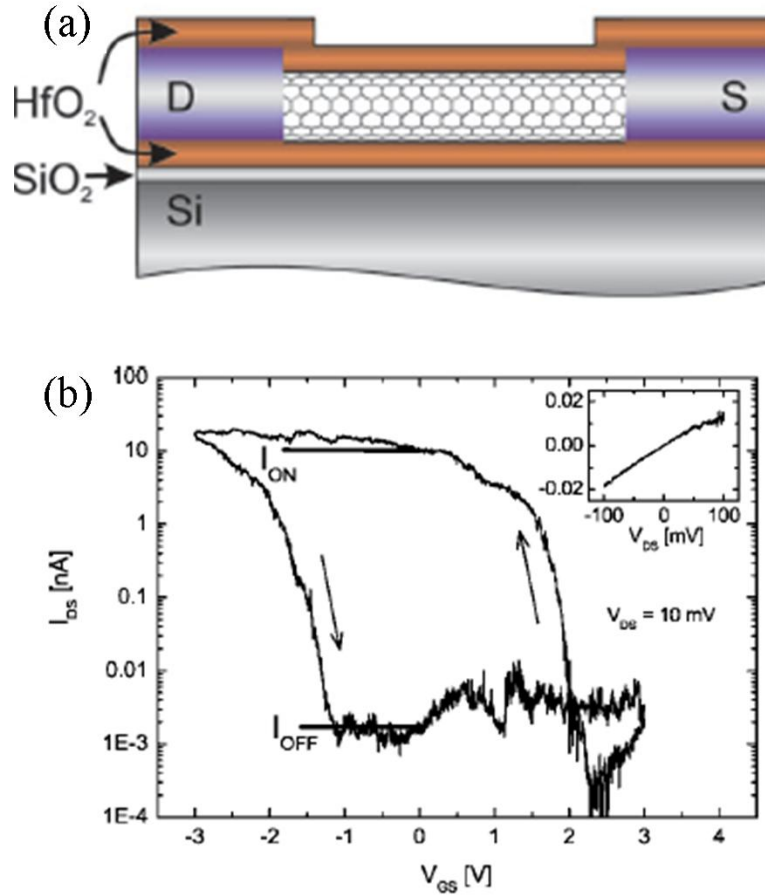


Figure 1-13 (a) A structure of CNT based flash memory device using HfO_2 as storage layer, (b) Hysteresis loop of a typical SWCNT-FET [39].

For graphene flash memory, both graphene flake [40] and graphene nanoribbon [41] can be chosen as channel materials. After graphene channel fabricated on SiO_2/Si substrate, Ti/Au are chosen as metal contacts to form source and drain. Without further deposition of dielectric, the Si substrate is used as back gate. A drain current hysteresis can be observed by sweeping the back gate. Since no dielectric is used in this structure, the hysteresis loop should originate from the charge trapping effect between the channel

and water molecules. High temperature annealing and vacuum condition can change the memory performance of devices as confirmed by reference [40, 41], which makes this structure not suitable for practical application. A better structure of using graphene in flash memory devices is given in chapter 4.

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Chapter 2: Layer-by-layer synthesis of large-area graphene films by thermal cracker enhanced gas source molecular beam epitaxy

2.1 Introduction

Graphene is a two dimensional carbon film with atoms densely packed together as hexagonal structure. Since it was discovered [1], graphene has attracted vast interests in condensed matter physics, chemistry, and nanotechnology communities due to its unique properties, such as extremely high mobility [2], anomalous quantum Hall effect [3-4], high mechanical strength, large thermal conductivity, good optical transparency, and high chemical stability [5]. Graphene may find many applications such as sensors, catalyst-support, composites, drug delivery, gas storage, energy storage and conversion, transparent conducting material, and post-silicon material for microelectronics industry.

Graphene has been synthesized by various methods. Solution/soft chemistry based synthesis methods such as solvothermal synthesis [6] and graphite oxide reduction [7] may lead to graphene materials with large volume and/or small pieces, but not large and uniform thin sheets. These graphene films may be suitable for applications other than electronics. To use graphene for applications in nanoelectronics, it is essential to have large-area graphene substrates manufactured to tightly controlled specifications.

Currently, three major approaches are used to make large-area graphene. The first method is using mechanical exfoliation of graphite [1]. This method usually makes graphene with highest quality in terms of high electron mobility and low defect density, but the yield is very low and the approach is not suitable for commercialization. Second,

graphitization of single crystal SiC was also used to produce ultrathin epitaxial graphite films by sublimation of Si from SiC substrate [4]. Graphene produced by this method is usually very fragile and contains many defects due to the large lattice mismatch between SiC substrate and graphene itself. Additionally, large-area production is also limited by the expensive SiC substrate. The third method is carbon precipitation from metal substrate. Hydrocarbon gas is decomposed and dissolves into certain metals in a chemical vapor deposition (CVD) system. The dissolved carbon atoms segregate onto metal surface and form thin graphitic layers as the substrate temperature cools [9]. Nickel [9-11] and copper [5, 12] have been used as catalyst substrates in CVD system at high temperature (1000 °C). Due to this precipitation mechanism, very fast substrate cooling is needed; therefore, the accurate control of substrate temperature cooling rate is difficult. Additionally, the atmosphere or low-pressure process in CVD system may lead to over-saturation of carbon in metal substrate and subsequently make it difficult to control the number of layers of the as-grown films. Obviously, although having achieved a great deal of success, these methods still have various limitations and other methods to obtain uniform large-area graphene films are still desirable.

Here, thermal cracker enhanced gas source molecular beam epitaxy (GSMBE) graphene synthesis is proposed as an alternative method. The thermal cracker provides atomic carbon onto a metal surface, and these carbon atoms migrate on the surface to form graphene film directly. The direct growth of graphene on a surface is expected to possess better growth controllability than carbon precipitation for high quality and controllability of the number of layers.

2.2 Experimental

2.2.1 Sample growth and transfer

Figure 2-1 shows the diagram of the GSMBE chamber. The substrate is heated by a DC power supply. The thermal cracker is a spring-shaped tungsten filament with gas line coming through. Another DC power supply provides power to heat the filament. Typically, the tip and shell of the thermal cracker can reach 1200 °C and 550 °C, respectively. The bonds of gas molecules (acetylene) coming through the cracker are broken by high temperature, and carbon atoms are impinged onto the substrate for epitaxial growth.

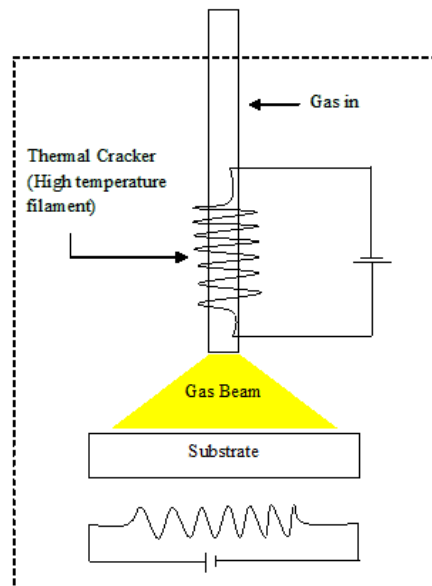


Figure 2-1 Diagram of thermal cracker enhanced GSMBE system.

The procedure for graphene growth in thermal cracker enhanced GSMBE system is given as follows (Figure 2-2). First of all, 300 nm SiO₂ covered n-type Si was used as substrate, and 300 nm nickel film was deposited by electron beam evaporation. After this deposition, the whole sample was transferred into a GSMBE system. The substrate started to heat up with a ramp rate of 10 °C/min when the vacuum in the chamber is good enough ($< 1 \times 10^{-7}$ Torr). After the target temperature was reached (usually 800 °C), a period of 10 min was needed for temperature stabilization. Acetylene was then introduced to the chamber. The flow speed was usually in the range of 5~10 sccm (standard cubic centimeters per minute). The sample was cooled at a rate of 10 °C/min after carbon growth for 6 minutes.

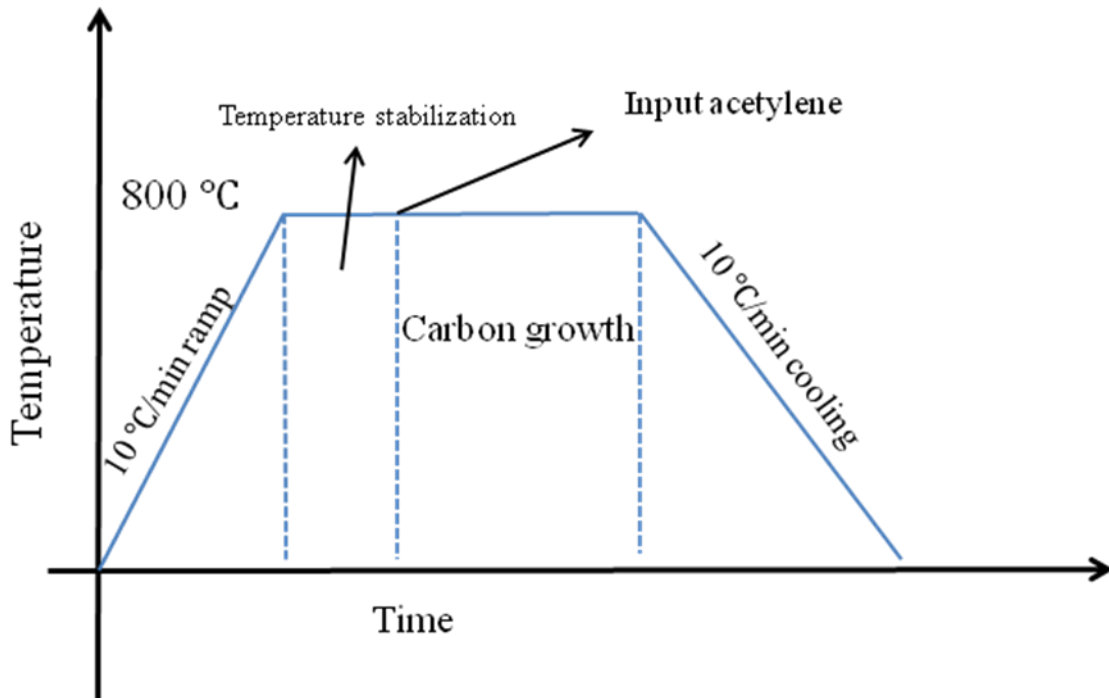


Figure 2-2 The procedure of graphene growth using nickel in GSMBE chamber.

Because graphene cannot be used as any field effect materials or transparent electrode with conductive nickel underneath, a transfer method is given in Figure 2-3. A mild HCl solution (5%) was used to etch the nickel film. The sample was dipped into HCl solution for several hours. After the nickel film was etched away, graphene floated inside the solution and was ready to be transferred. The same SiO₂/Si or glass substrate was put into the solution to lift the floating graphene slowly. To vaporize the water coming with the graphene, the sample was heated up to 100 °C for 10 minutes.

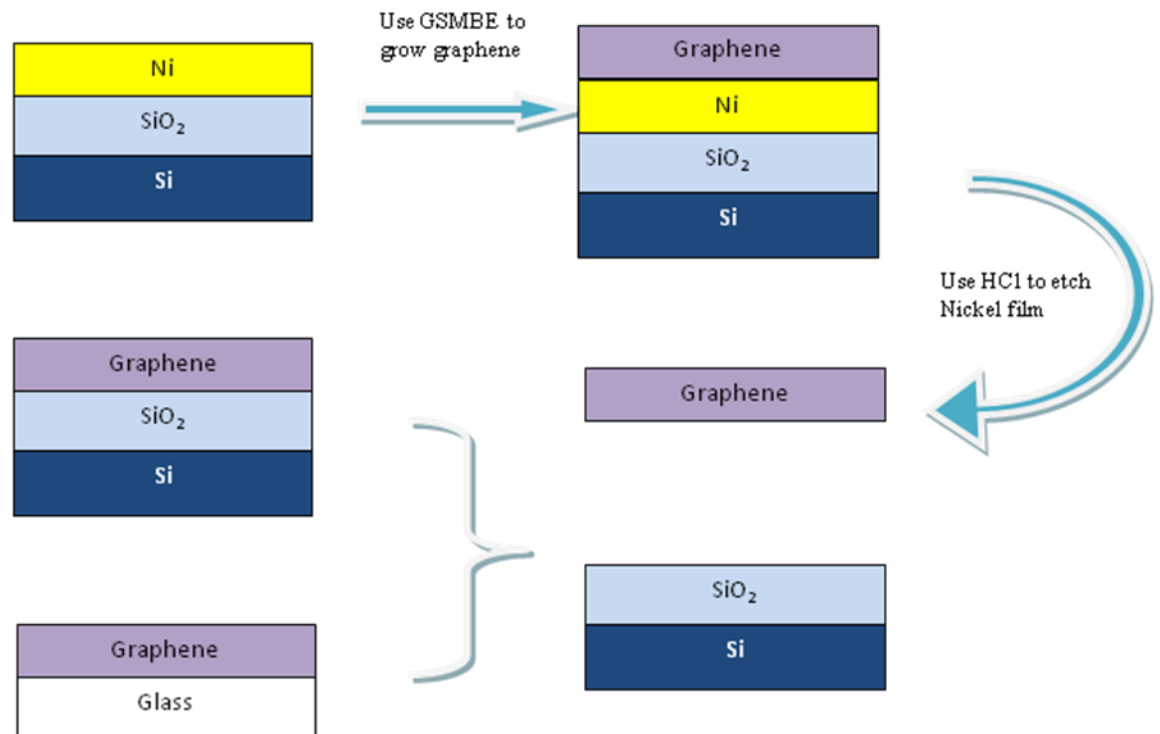


Figure 2-3 The procedure of transferring graphene onto SiO₂/Si or glass substrates.

2.2.2 Characterization tools

2.2.2.1 Transmission electron microscopy

Transmission electron microscopy (TEM) is capable of imaging at a significantly higher resolution than optical microscopes or scanning electron microscope (SEM), owing to the small de Broglie wavelength of high energy electrons. It enables the instrument's user to examine fine details at even atomic level. In this chapter, TEM was used to check the morphology of as-grown graphene. The number of graphene layers can also be counted by cross-sectional TEM images. Additionally, TEM diffraction pattern provides detailed information of the quality of as-grown films.

TEM takes advantage of the interaction between a specimen and a focused electron beam while is transmitting through an ultra thin sample. An image is formed from the interaction and focused onto an imaging device, such as a fluorescent screen, or detected by a CCD camera. Figure 2-4 shows a typical structure of TEM [13-14]. The first component from the top is an emission gun, which is a lanthanum hexaboride (LaB6) source for the TEM used in this experiment. By applying the emission gun with high voltage (typically ~100-300 kV), electrons will emit by field electron emission into the vacuum. Once extracted, the upper lenses of the TEM allow for the formation of the electron probe to the desired size and location for later interaction with the sample. There are two physical effects for the lenses of the TEM to manipulate electron beam. First, the interaction of electrons with a magnetic field will cause electrons to move according to the right hand rule, thus allow the electron beam to be manipulated by electromagnets.

Secondly, electrostatic fields are used to cause the electrons to be deflected through a constant angle. Coupling of two electrostatic deflections in opposing directions with a small intermediate gap can make the electron beam parallel shifted. These two physical effects, combined with the use of an electron imaging system, provide sufficient control of the beam needed for TEM operations [13-14]. High-resolution Philips CM300 TEM with electron gun voltage of 300 KV was used to characterize as-grown films in this experiment.

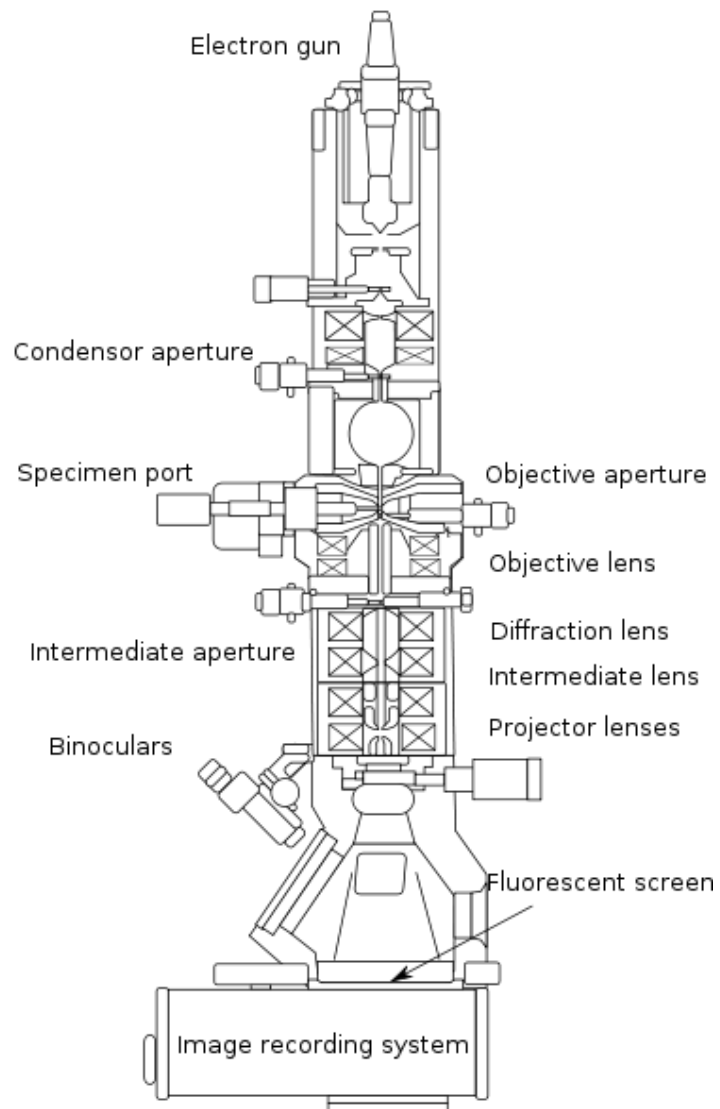


Figure 2-4 The typical structure of TEM.

2.2.2.2 Raman spectra

Raman spectroscopy is a spectroscopic technique used to study vibrational, rotational, and other low-frequency modes in a system. Raman scattering occurs because

of an interaction between incident laser and a material, which leads to the annihilation or creation of a phonon. The difference between the scattered photon and the incident photon is defined as Raman shift, which is given by the following formula.

$$\Delta\omega = \left(\frac{1}{\lambda_0} - \frac{1}{\lambda_1} \right)$$

, where $\Delta\omega$ is the Raman shift expressed in wavenumber, λ_0 is the excitation wavelength, and λ_1 is the Raman spectrum wavelength. By measuring detected laser intensity versus Raman shift, the information of as-grown graphene films can be acquired.

The Raman spectroscopy system used here consists of three major components. They are excitation source, light detector, and light collection and delivery system. The excitation sources for every Raman systems in the world are exclusively laser. Here, we use Ar ion lasers with the wavelength of 532 nm. Because Raman shift measures the wavelength difference between the incident laser and the scattered light. The monochromatic property of the incident should be good enough to the point where its linewidth is much lower than the width of the Raman lines in the Raman spectrum. Although increasing the laser power can increase the Raman scattering intensity and bring a better signal to noise ratio, this excessive heat could potentially be harmful to sample in some cases. The light detection system consists of slit, diffraction grating, mirror, and detector. The slit prevents too much light from entering the detection system which causes the diffraction of light, the light will act as a point source with a narrow slit. From the slit, the light travels to a lens and then onto a diffraction grating, which has a

number of closely packed slits to split up the light into its component wavelengths. Then, the selected wavelengths of light are guided towards a focusing lens. Considering the light here is relatively weak, a cooled CCD camera is used to detect light due to its inherent low noise feature.

2.2.2.3 Atomic force microscope

Atomic force microscope (AFM) is a very high-resolution type of scanning probe microscopy, with demonstrated resolution on the order of a few nanometers. The schematic of an AFM system is shown in Figure 2-5. The AFM consists of a cantilever with a sharp tip (probe) at its end that is used to scan the specimen surface. The tip radius of the cantilever is typically on the order of nanometers. While scanning, the force between the tip and the sample is measured by monitoring the deflection of the cantilever. A topographic image of the sample is obtained by plotting the deflection of the cantilever versus its position on the sample. If the tip is held at constant height above the sample, the risk of collision between the tip and rough surface exists. Instead, the height is controlled by a feedback loop to maintain a constant force between tip and sample in most cases. The tip is mounted on a vertical piezo scanner while the sample is being scanned in X and Y directions. The resulting map of the area $z = f(x,y)$ represents the morphology of the sample [15].

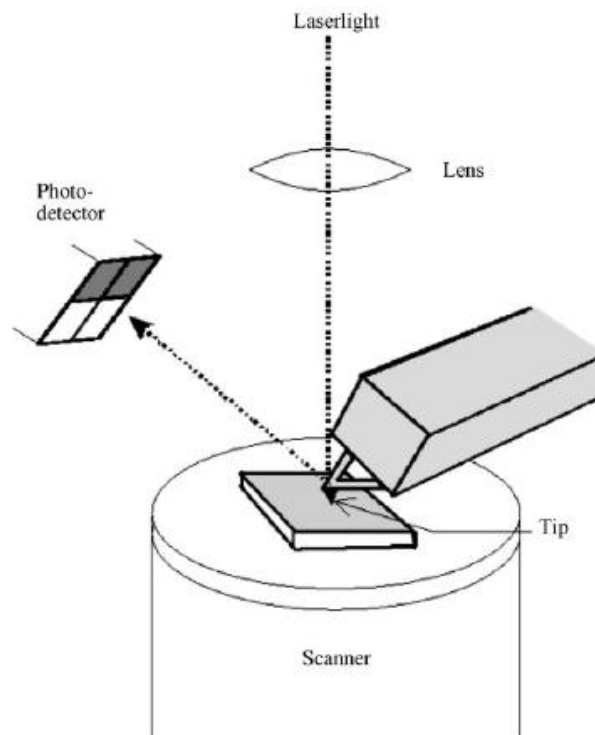


Figure 2-5 Schematic of AFM [15].

Tapping mode AFM was used for measuring the surface morphology of as-grown graphene samples. In tapping mode, the cantilever is driven to oscillate up and down at near its resonance frequency by a small piezoelectric element mounted in the AFM tip holder. When the tip comes close to the surface, the various interaction forces will act on the cantilever, such as Van der Waals force, dipole-dipole interaction and electrostatic forces. These interaction forces decrease the amplitude of this oscillation as the tip gets closer to the sample. An electronic feedback loop uses piezoelectric actuator to control the height of the cantilever above the sample. The feedback loop adjusts the height to maintain a set cantilever oscillation amplitude as the cantilever is scanned over the sample. A tapping AFM image is therefore produced by imaging the force of the

intermittent contacts of the tip with the sample surface [15]. In this thesis, the Veeco Dimension 5000 scanning probe microscope was used for AFM measurement.

2.3 Results and discussion

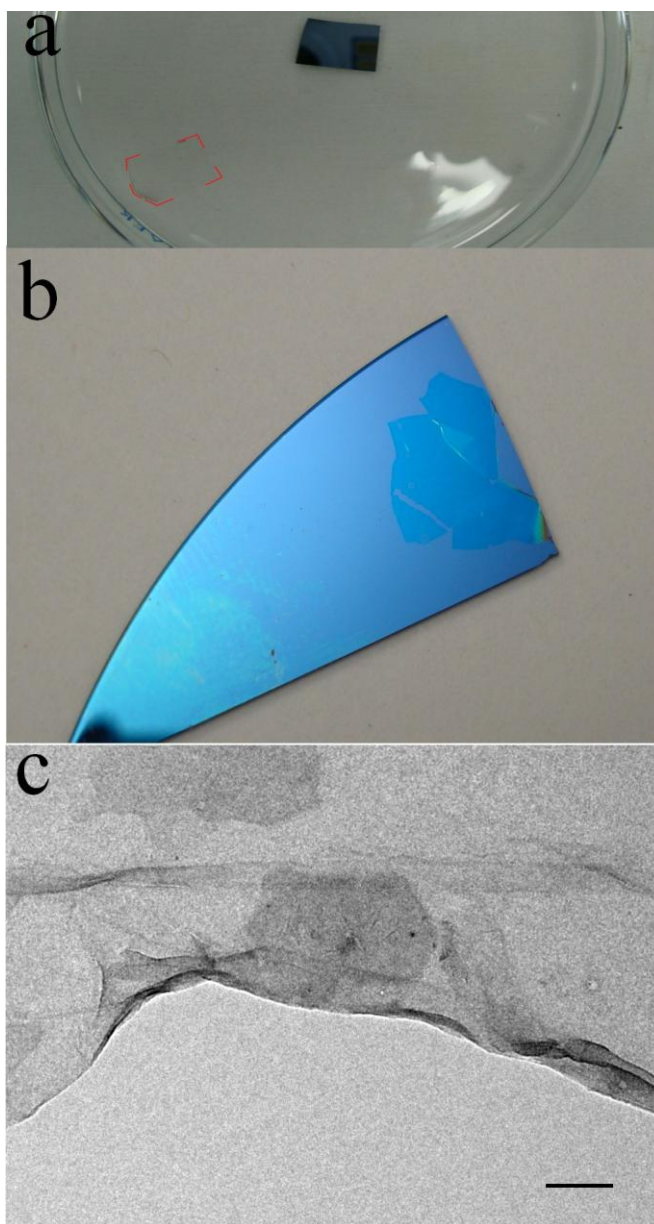


Figure 2-6 (a) A floating graphene (shown in red polygon) after underneath nickel film was etched in 5% HCl solution. (b) A transferred graphene film on SiO₂(300 nm)/Si substrate. (c) Top-view TEM image of the graphene film (Scale bar is 100 nm).

Figure 2-6(a) shows the graphene film grown at 800 °C floating in the 5% HCl solution after the nickel film was etched. Obviously, the graphene film can maintain its size and flatness after the metal film was etched. Figure 2-6(b) shows an image of the transferred graphene film on SiO₂/Si substrate. The Van der Waals interaction guaranteed the graphene to strongly attach to the substrate. To understand the surface morphology of graphene, a top-view TEM image was taken and shown in Figure 2-6(c). It shows clear contrast between areas with different thicknesses of graphene. This variation of number of layers is mainly due to the formation of nickel grains. A similar phenomenon was also found for CVD growth [9-11].

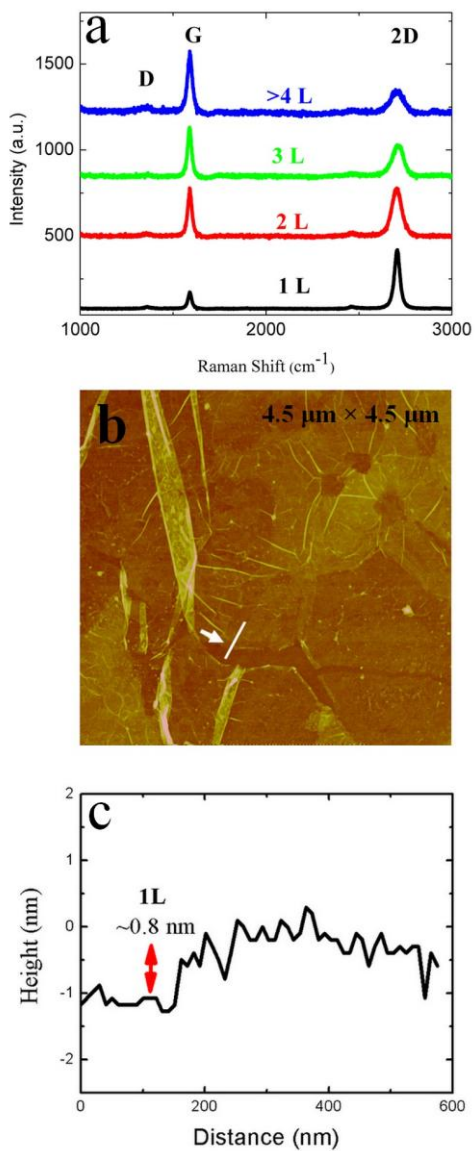


Figure 2-7 (a) Raman spectra of graphene films grown at 800 °C by thermal cracker enhanced GSMBE. Curves correspond to single layer, bilayer, triple layer and multi-layer graphene from the bottom to the top. (b) AFM image of the same sample. (c) Height measurement profile of the cross section indicated by the arrow in (b).

After transferring graphene to the SiO₂/Si substrate, micro-Raman analysis was used to characterize the graphene film with the laser wavelength of 532 nm. G band (~1580 cm⁻¹) and 2D band (2700 cm⁻¹), which are the most prominent phonon features of graphene film, were found (Figure 2-7(a)). The G band is associated with the doubly degenerate (iTO and LO) phonon mode at the Brillouin zone center, and 2D band originates from a second-order process involving two iTO phonons near the K point. Negligible D band (~1350 cm⁻¹) indicates the high quality of graphene films with very few defects. The thin sections of graphene, which correspond to the bright parts in Figure 2-6(c), have two major types of curves shown as the bottom two curves in Figure 2-7(a). The ratio between G band and 2D band (I_G/I_{2D}) can be used to distinguish the number of layers for as-grown graphene samples [11]. The small ratios of 0.28 and 1 for these two curves correspond to single layer and bilayer graphene films, respectively, which occupy almost 70% of the whole film. The Raman spectroscopy of dark parts of the film is also shown as the third curve from the bottom in Figure 2-7(a). The bigger I_G/I_{2D} ratio of 1.57 indicates three-layer graphene for these dark parts. For some parts of film especially on boundaries between nickel grains, a I_G/I_{2D} ratio of more than 1.8 was found (the top curve in Figure 2-7(a)). Because of the limitation of the Raman scattering method [11], a ratio bigger than 1.8 cannot be used to tell how many layers exactly the film has.

Figure 2-7(b) shows an AFM image of the transferred film. The variation of the contrast in the image indicates different thickness of layers. The height measurement profile (Figure 2-7(c)) of the cross section indicated by the arrow in Figure 2-7(b) shows that the thickness of the film is around 0.8 nm, suggesting single-layer graphene in this

selected area [11]. Different grains cause different number of layers during growth, and the boundaries between grains have thermal stress induced by the terraces-like steps [9]. Hence, the graphene films on boundaries tend to grow vertically and form as wrinkles, which can be seen as bright lines in the AFM image (Figure 2-7(b)).

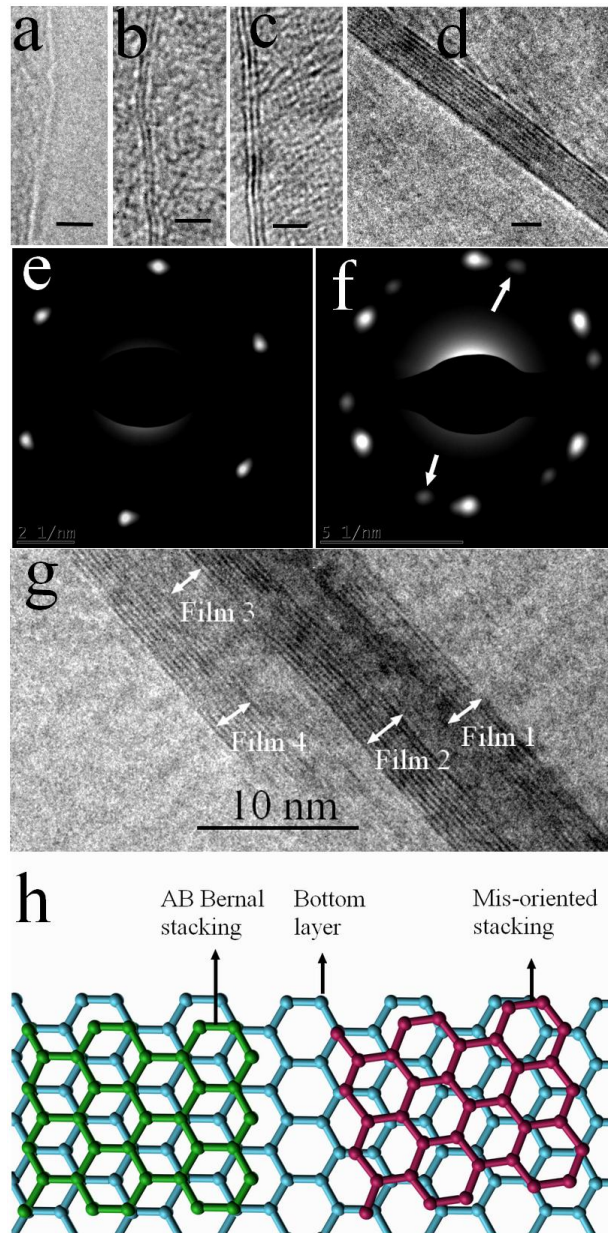


Figure 2-8 Cross-sectional TEM images of **(a)** single-layer, **(b)** bi-layer, **(c)** tri-layer and **(d)** multi-layer graphene. The scale bar is 2 nm. **(e)** Diffraction pattern of as-grown sample. **(f)** Diffraction pattern of certain part of the film has the second sets of spots as shown by arrows. **(g)** Several films stacking together. **(h)** Illustration of AB Bernal stacking graphene (green) and mis-oriented stacking graphene (red).

In conjunction with Raman scattering and AFM characterization, TEM measurement was carried out. The graphene was transferred to TEM copper grid by the same method as if it was transferred onto the SiO₂/Si substrate. A lacy copper grid without any carbon film was chosen and dipped into HCl solution. After the floating graphene was lifted up, remaining water on the grid was naturally vaporized. The graphene tends to fold back, which gives a convenient way to take a cross-section view. Single-layer, bilayer, trilayer and multilayer graphene were all found by TEM (Figures 2-8 (a)-(d)). The interlayer distance of about 3.4 Å was estimated by fast Fourier transform, which agrees with the interlayer distance of graphite. Furthermore, the diffraction pattern of most parts of films has a very clear hexagonal pattern, which confirms the three-fold symmetry of the arrangement of carbon atoms (Figure 2-8(e)). This also agrees with the high quality of the film derived by the Raman spectra. Besides this major hexagonal diffraction enhanced spots, some part of the film also has secondary hexagonal enhanced spots shown in Figure 2-8(f). Two reasons might contribute to this phenomenon. On one hand, because the graphene films tend to fold back randomly, there is great chance that some films stack

together as the one shown in Figure 2-8(g), which has four individual films folded together. On the other hand, the secondary sets of spots can originate from the mis-stacked order of individual films. Graphene films exfoliated from HOPG are stacked in AB Bernal stacking order (Figure 2-8(h)), where the vacant centers of the hexagons on one layer have carbon atoms on hexagonal corner sites on the two adjacent graphene layers along c-axis. Depending on growth conditions, different layers in as-grown graphene films may not be stacked together according to AB Bernal stacking order; they could be stacked in a mis-oriented stacking order (Figure 2-8(h)). This can be proved from Raman scattering results (Figure 2-8(a)). If the graphene films adopt AB Bernal stacking order, the profile of 2D band should evolve with different number of layers, and it was noticed that only 2D band of single layer graphene films has Lorentzian feature [16] as shown in Figure 2-9. But for the Raman spectra obtained here, even the films of more than one layer have Lorentzian distributed 2D band, while the full width at half maximum (FWHM) increases with the number of layers. FWHM varies as 34 cm^{-1} , 62 cm^{-1} , 69 cm^{-1} and 94 cm^{-1} for single-layer, bi-layer, tri-layer and multilayer graphene, respectively (Figure 2-8(a)). This is due to the weak interaction between adjacent mis-oriented layers [17]. Therefore, both the Raman spectra and diffraction patterns may be used to predict the stacking order of as-grown graphene films.

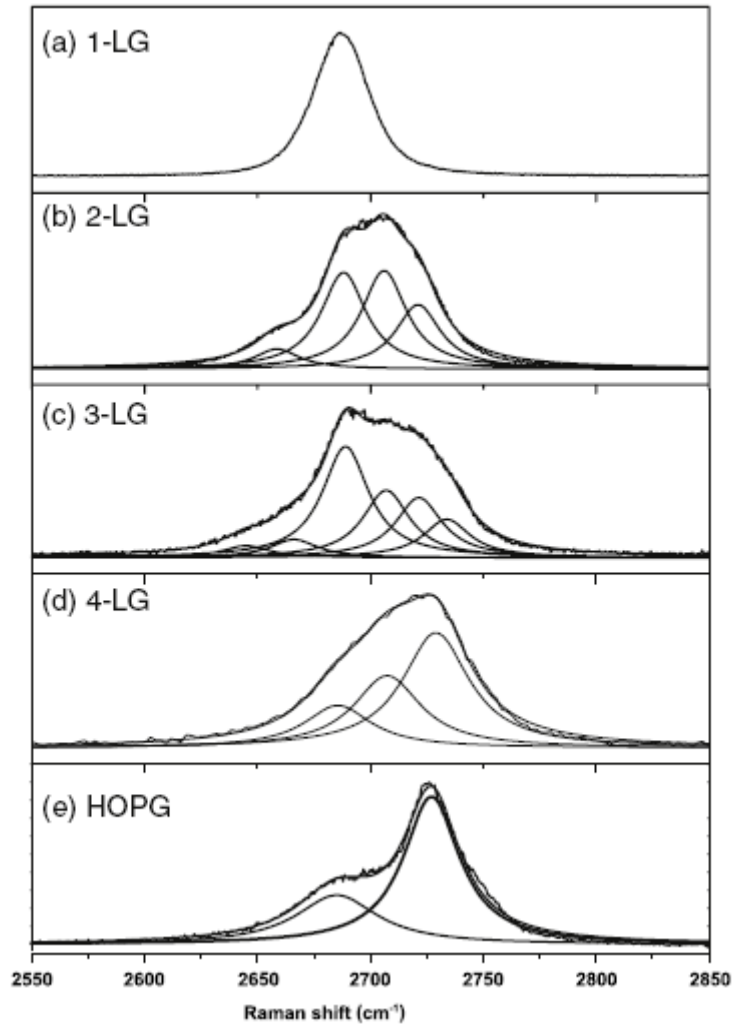


Figure 2-9 The measured 2D Raman band with 2.41 eV laser energy for (a) 1-LG, (b) 2-LG, (c) 3-LG, (d) 4-LG, (e) HOPG and (f) turbostratic graphite. The splitting of the 2D Raman band opens up in going from mono- to three-layer graphene and then closes up in going from 4-LG to HOPG [17].

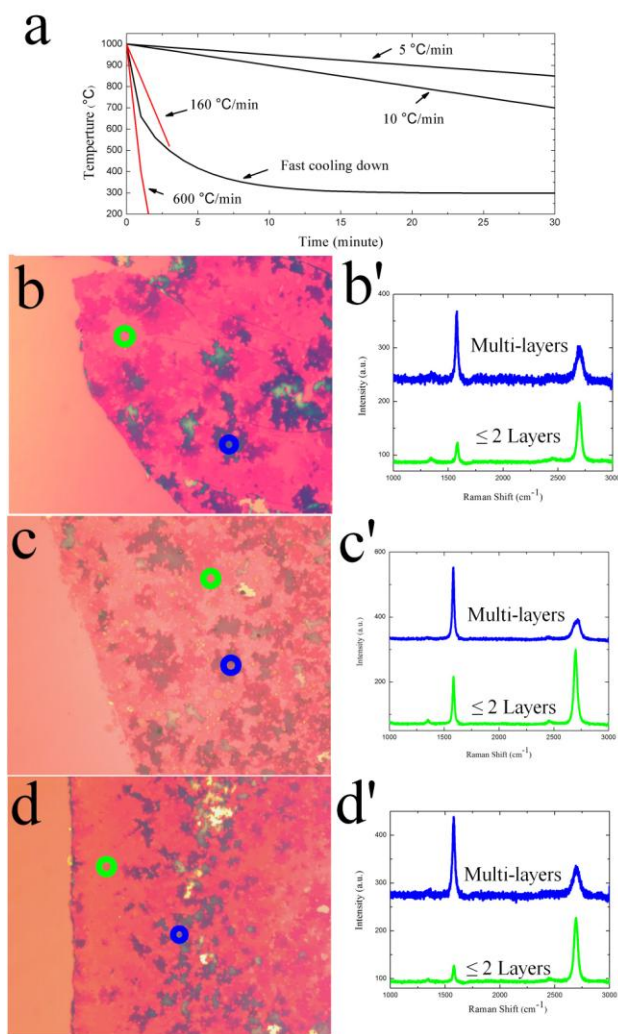


Figure 2-10 (a) Different cooling rates. 160 °C/min and 600 °C/min (shown in red lines) cooling were used by CVD method [9-10, 18-19]. Fast cooling, 10 °C/min and 5 °C/min cooling were tested in the thermal cracker enhanced GSMBE for comparison. Optical microscopy images (b, c and d) and corresponding Raman spectra (b', c' and d') of as-grown graphene films with different cooling rates on 300 nm SiO₂/Si substrates. (b) Fast cooling as shown in (a). (c) 10 °C/min cooling. (d) 5 °C/min cooling. Representative

positions where Raman spectra were taken are identified by circles in corresponding color in optical images.

Although still controversial, the over-saturated carbon atoms precipitate to metal surface to form graphene at lower temperature in CVD process. Rapid substrate cooling rate is found in many CVD processes to suppress the formation of multi-layers or even graphite and obtain few layers graphene. Typically, 160 °C/min [9] and 600 °C/min [10, 18-19] were tried and proved to be necessary for growth of a few layers. To verify the growth mechanism of our thermal cracker enhanced GSMBE system, different cooling rates were investigated. Figure 2-10(a) shows the comparison of cooling rates used in CVD method (shown in red lines) from the literature and our GSMBE system. Fast cooling in between 160 °C/min and 600 °C/min, 10 °C/min, and 5 °C/min were chosen as different cooling rates at a growth temperature of 1000 °C in our experiments. Figures 2-10 (b)-(d) shows the optical microscopy images of graphene films, which were grown with these different cooling rates and subsequently transferred onto 300 nm SiO₂/Si substrates. Because the optical contrast is interfered by the thickness of graphene film, different parts of a graphene sample with the same optical contrast should have the same number of layers. To identify the number of layers in the light red parts of these samples, micro-Raman spectra were carried out on certain positions enclosed by green circles in the optical images. The corresponding Raman curves are shown in green in the right side of each image, which all have a I_G/I_{2D} ratio less than one, indicating single-layer or bilayer graphene film. Other dark parts (enclosed by blue circles) of these samples have much bigger I_G/I_{2D} ratio (shown in blue color in the right side of each image), suggesting

the formation of multi-layer graphene. From the optical images of these samples, the percentage of single-layer and bilayer graphene are approximately 75%, 70% and 74% for fast cooling, 10 °C/min and 5 °C/min, respectively. Fast cooling and very slow cooling do not have obvious difference for graphene growth in the thermal cracker enhanced GSMBE system, therefore rapid cooling is not required for thermal cracker enhanced MBE growth.

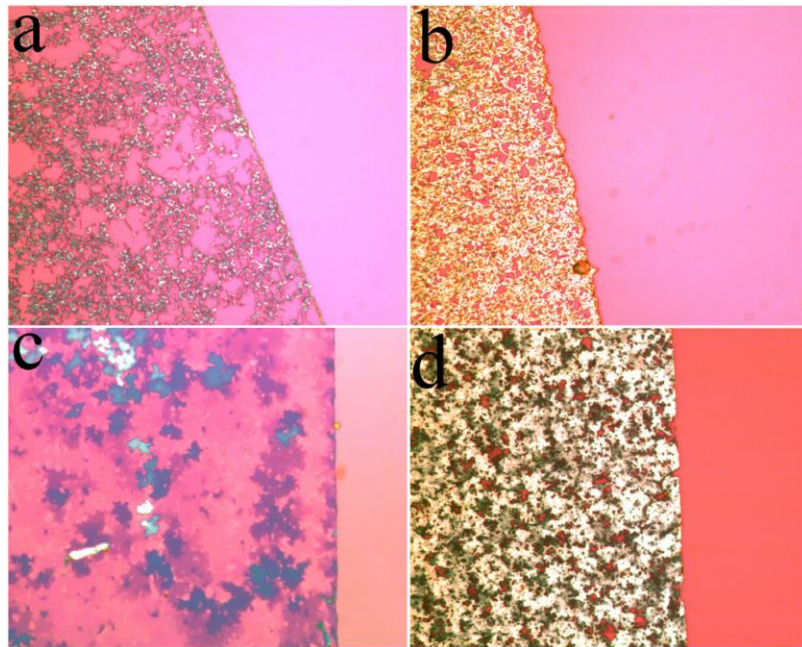


Figure 2-11 Optical microscopy images of as-grown graphene films with different growth time on 300 nm SiO₂/Si substrate. **(a)** 1 minute, **(b)** 4 minutes, **(c)** 6 minutes, **(d)** 10 minutes.

To further investigate the mechanism of thermal cracker enhanced GSMBE growth, different growth times were tested. Figure 2-11 shows optical microscopy images of transferred samples on SiO₂/Si substrate with the growth time of 1 minute, 4 minutes,

6 minutes and 10 minutes, respectively. All other growth conditions were kept the same, including the substrate temperature of 800 °C, cooling rate of 10 °C /min, etc. For the sample with only 1 minute growth, the as-grown carbon layer is not a film yet but a porous net (Figure 2-11(a)). With the increase of growth time, more and more carbon atoms grow into porous net and form a continuous film (Figures 2-11(b) and (c)). As the growth time reaches 10 minutes (Figure 2-11(d)), the film becomes a very dense carbon film with much higher contrast compared to SiO₂, which means most parts of film already had become multi-layers graphene or even graphite. Therefore, it is not the different cooling rates but the growth time that manipulate the number of layers of the grown films in the GSMBE system. This means we observe traditional growth of one layer on top of another carbon layer, rather than graphene growth of one layer at the bottom of another carbon layer in CVD method.

To verify the direct growth mechanism from a different angle, graphene films were also grown at different temperatures of less than 800 °C in our GSMBE system, which are normally too low to form any graphene in CVD method. Figures 2-12 (a)-(d) show the evolution of Raman spectra for graphene films grown at temperatures from 750 °C to 600 °C. As the temperature decreases from 800 °C to 750 °C, an obvious defect peak appears. The ratio between D peak and G peak is usually used to indicate the amount of defects. The value for 750 °C sample is 0.58 which demonstrates a large amount of defects in the films, and it increases to 0.8 for the sample grown at 700 °C. As the substrate temperature keeps decreasing, the D peak still exists and gradually merges into G peak. Additionally, the 2D peak, which is supposed to be around 2700 cm⁻¹, does

not appear anymore; instead, a big “wave packet” occurs from 2500 cm^{-1} to 3200 cm^{-1} for $650\text{ }^{\circ}\text{C}$ and $600\text{ }^{\circ}\text{C}$ samples. This is a typical indication of carbon amorphization [20]. Corresponding TEM diffraction patterns of these films are shown in Figure 2-12 (a’)-(d’). The diffraction pattern for $800\text{ }^{\circ}\text{C}$ sample. Figure 2-8(e) has a very clear hexagonal pattern agreeing with the high quality of the film derived by the Raman spectrum. The diffraction pattern starts to appear as ring-like shape besides hexagonal pattern for $750\text{ }^{\circ}\text{C}$ sample (Figure 2-12(a’)), it should be due to the fact that the film starts to become more polycrystalline and adjacent layers start to distribute more randomly, which brings more defects also indicated in Raman spectrum. From $650\text{ }^{\circ}\text{C}$ and $600\text{ }^{\circ}\text{C}$ samples, the hexagonal pattern disappears and the ring-like shape occurs (Figures 2-12 (c’)-(d’)). This proves that the films are already starting to be amorphous at these temperatures, which agrees with Raman spectra of these samples. Two major reasons may contribute to this evolution. On one hand, the decrease of temperature causes insufficient thermal energy provided by substrate and decrease the diffusion length of carbon atoms on the nickel surface. Instead of forming as “graphitic” carbon, the carbon atoms reconstruct as other forms, such as relaxed dislocation geometries for vacancy units [21] or “carbide” carbon [22-23], which have less formation energy. Further decrease of substrate temperature to $650\text{ }^{\circ}\text{C}$ and below results in the fact that these carbon atoms cannot have enough energy to form any crystals. On the other hand, the lower the temperature is, the rougher the nickel surface is. A surface morphology comparison was done between nickel films annealed at $800\text{ }^{\circ}\text{C}$ and $600\text{ }^{\circ}\text{C}$ as given in Figure 2-13, showing much rougher surface for the films annealed at lower temperature. Because nickel film provides the supporting

template for carbon to form graphene, rougher surface obviously prevents the carbon atoms from diffusing freely, leading to compromised quality.

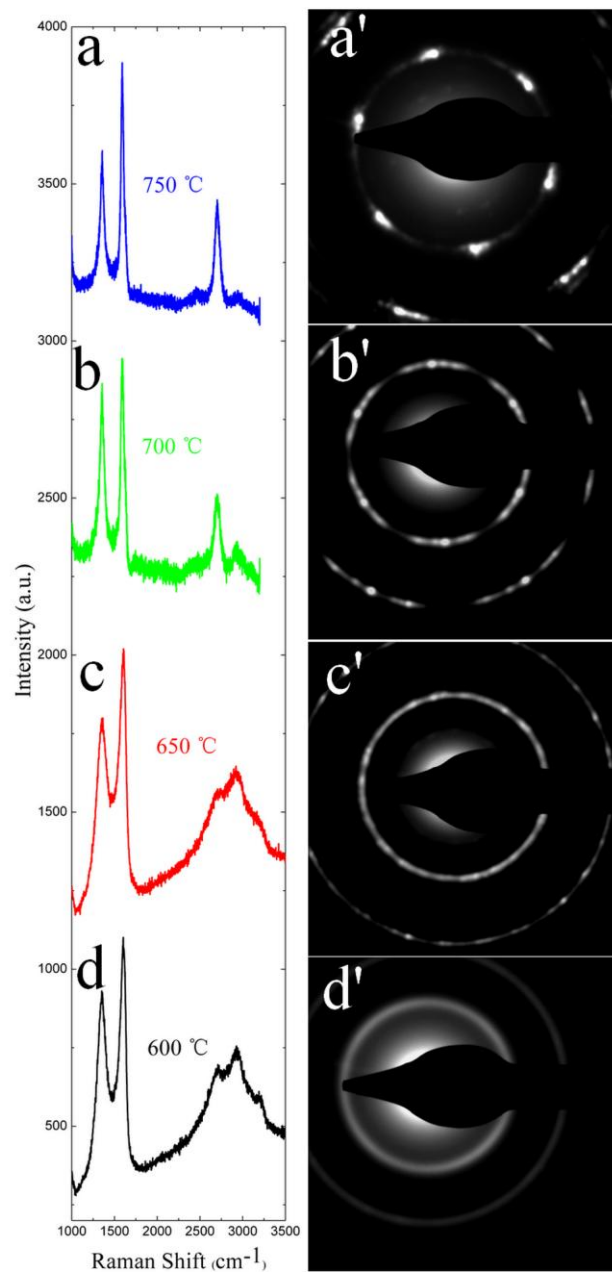


Figure 2-12 Evolution of Raman spectra (**a**, **b**, **c** and **d**) and corresponding diffraction patterns (**a'**, **b'**, **c'** and **d'**) for graphene films grown at different temperatures. (**a**) 750 °C, (**b**) 700 °C, (**c**) 650 °C and (**d**) 600 °C.

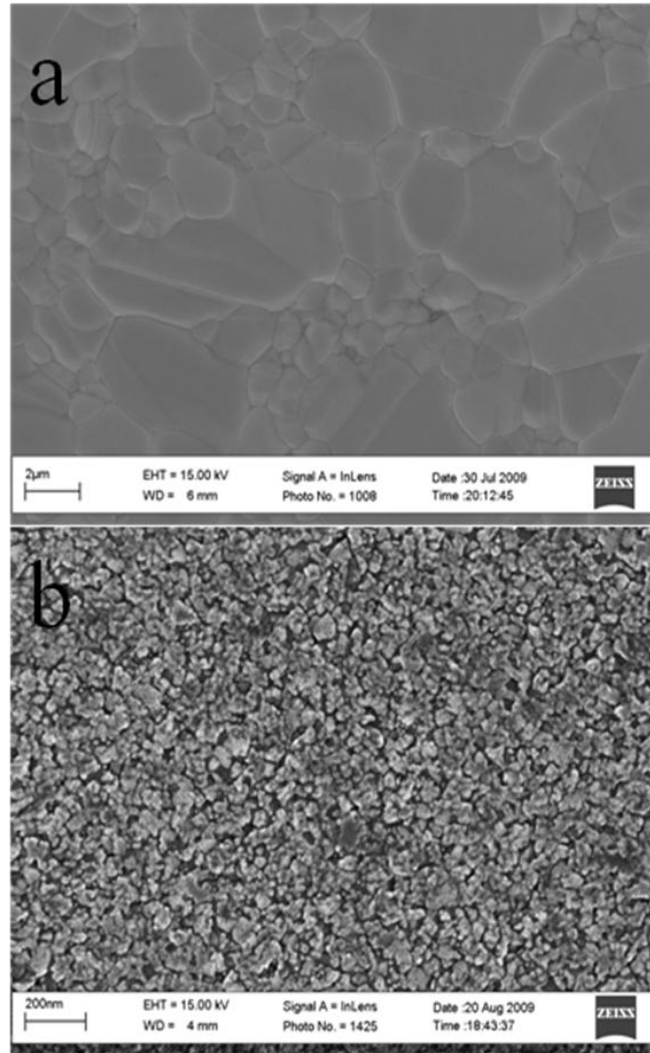


Figure 2-13 SEM images of nickel film annealed at (a) 800 °C and (b) 600 °C.

In the CVD method, the graphene is formed in the cooling period; by contrast, the results above indicate that the thermal cracker enhanced GSMBE system forms graphene during the hydrocarbon gas inputting period. The high-temperature thermal cracker breaks the gas molecules into atoms, the carbon atoms are impinged on the nickel surface. While portion of these atoms may be dissolved into the nickel film, many carbon atoms

are adsorbed on the nickel surface and diffuse around. A complete graphene layer can be formed by these adsorbed carbon atoms fitting the hollow sites of the substrate [22-23]. Once the nickel surface is covered by this graphitic carbon layer, the catalytic activity of nickel film is greatly reduced [22]. This as-grown graphene layer provides the template for further layer by layer growth. Therefore, nickel films mainly serve as adsorption sites for the graphene growth in this method rather than as catalyst in CVD method. This leads to a key difference between CVD method and thermal cracker enhanced GSMBE method in terms of when graphene films are formed. The thermal cracker enhanced GSMBE method has tremendous potential for controllable growth of graphene with different layers. Depending on the substrate temperature and the flatness of the substrate, the graphene film may be quickly formed. The as-grown graphene suppresses further dissolving carbon into nickel film, which would never become carbon saturation. Therefore, during the substrate cooling, no carbon atoms may segregate onto the nickel surface to form additional graphene layers. This suggests that different cooling rates have no effect on the formation of graphene, as shown earlier.

2.4 Conclusions

Large-area, few-layer graphene films were synthesized by thermal cracker enhanced GSMBE, and the growth mechanism was found to differ from that of CVD. The quality of as-grown graphene films was controlled by the growth time rather than the cooling rate. Large-area, few-layer graphene films were achieved at 800 °C, about 200 °C

lower than the temperature used in the typical CVD method. Clear diffraction patterns indicate a high-quality hexagonal structure. The profile of the 2D bands and diffraction patterns prove the mis-oriented stacking order of as-grown films. More defects in the graphene film occur at lower growth temperature; it becomes amorphous carbon when the temperature reaches 650 °C. These results suggest that graphene has been synthesized on the nickel substrate through layer-by-layer growth mode.

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Chapter 3: Cobalt-assisted large-area epitaxial graphene growth in thermal cracker enhanced gas source molecular beam epitaxy

3. 1 Introduction

Due to its unique properties, graphene has attracted tremendous attention in various fields since it was discovered [1]. High flexibility, low resistance and good optical transparency make it very promising for flexible electronics [2]. Graphene based 100-GHz transistors have already been achieved because of its extremely high mobility [3]. Anomalous quantum Hall effect [4-5] and spin transport [6] in graphene make it an ideal material for spintronics. To realize all these potential applications, it is critical to reliably synthesize high-quality, large-area graphene.

There are already a few methods to synthesize large-area graphene. The mechanical exfoliation method [1] provides graphene with highest quality in term of no defects and highest electron mobility. Nevertheless, produced films usually are very small, which limits its potential for practical application. Graphitization of single crystal SiC [5] substrate can produce wafer-size graphene film. The drawback is the fact that SiC substrates are very expensive. By far, the closest method to industrial production for synthesizing large-area graphene is using metal substrates in chemical vapor deposition (CVD). Various metals including Ni [7-9], Cu [10-11], Ru [12], Co [13-15] and Ir [16] have been used. Because of its very small lattice mismatch to graphene [17], Co has attracted particular interest. Carbon adsorption on Co substrate phenomenon has been observed [13]. Nevertheless, large-area, high-quality graphene is still a challenge for

CVD process. Earlier, as-grown graphene films were either very small (several nanometers, or tens micron by tens micron) or containing inhomogeneous islands [14, 15]. Ago et al. reported large-area graphene on Co/sapphire using CVD, which relied on rapid cooling of the sample by pulling out the substrate from the furnace immediately after the growth [18]. Carbon precipitation from Co is responsible for the CVD growth of graphene, however, rapid temperature cooling rate is not very controllable, leading to inability of controlling the number of graphene layers, which may be desired. Recently we reported large-area graphene growth on Ni substrate by using thermal cracker enhanced molecular beam epitaxy (MBE) [19]. Unlike growing graphene by carbon precipitation from oversaturated Ni [7-8, 20] substrate in CVD system, very fast cooling to suppress the formation of multilayer is not required in MBE growth. Here, we extend this method to synthesize graphene films on Co substrates. It is found that not only high-quality, large-area graphene can be synthesized, but also the morphology of the graphene is better than those grown on Ni substrate. High single-layer and bi-layer coverage of 93% is achieved by precisely controlling growth temperature and time. The mechanism of the graphene growth is tentatively discussed.

3.2 Experimental details

500 nm Co film was deposited on SiO₂ (300nm)/Si substrate by electron beam evaporation. The substrate was immediately transferred into GSMBE chamber for preventing surface contamination. Figure 3-2 (a) shows the diagram of epitaxial graphene

growth in GSMBE. The thermal cracker in this system is a spring-shaped filament, which is heated to 1200~1300 °C during graphene growth. The bonds of gas molecules (acetylene) coming through the cracker were broken by high temperature, and carbon atoms then impinged onto the substrate for epitaxial growth. After cobalt film was transferred into GSMBE chamber, the substrate started to heat up with a ramp rate of 10 °C/min. Hydrogen of 10 sccm was input into the chamber during temperature ramping up. After temperature stabilized at the target value for 10 min, acetylene was introduced into the chamber through the thermal cracker to provide atomic carbon beam. The gas flow rate was kept at 10 sccm. The sample was cooled to room temperature after carbon growth (Figure 3-1).

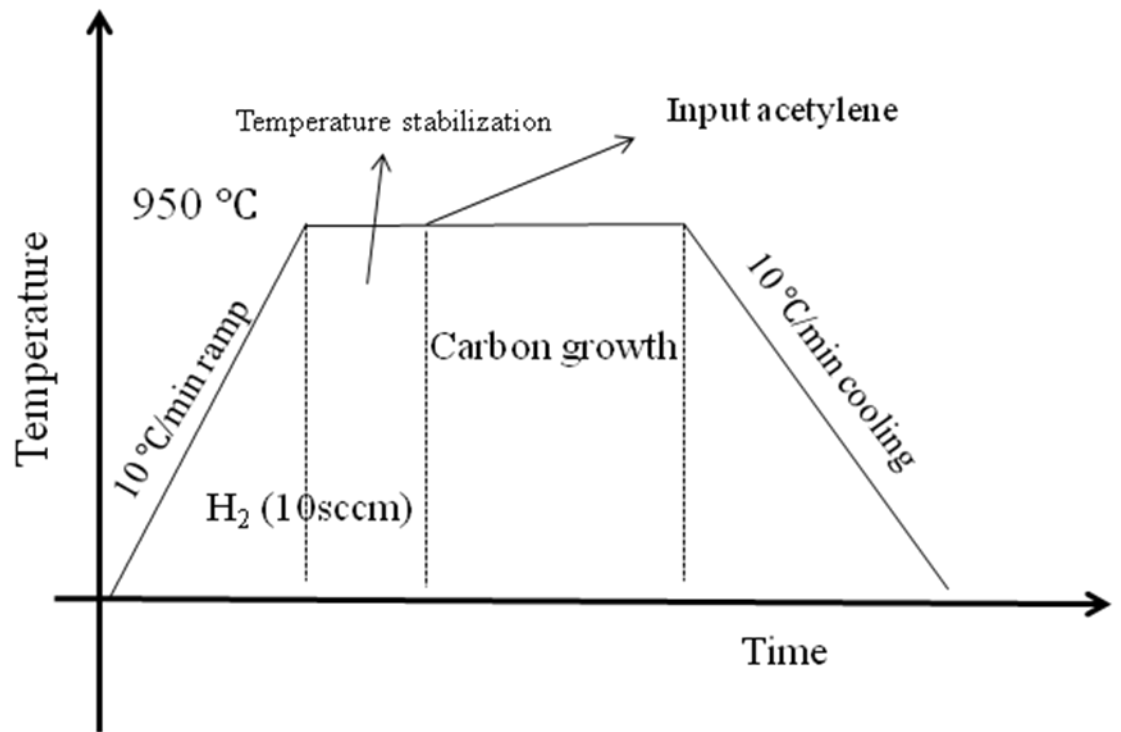


Figure 3-1 The procedure of graphene growth using cobalt in GSMBE chamber.

To transfer as-grown graphene films to desired substrates, polymethylmethacrylate (PMMA) was spin-coated on graphene/Co/SiO₂/Si substrate. After baked at 180 °C for 2 minutes, the whole sample was dipped into a mild HCl solution (5%) and the Co film was etched, which usually took 12 hours. After the Co film was etched away, PMMA/graphene film floating inside the solution was lifted by the same SiO₂/Si substrate slowly. Acetone was used to dissolve the PMMA layer after transferring PMMA/graphene to a desired substrate.

High-resolution Philips CM300 TEM with electron gun voltage of 300 KV was used to characterize as-grown films. Raman spectrum was measured at room temperature with laser wavelength of 532 nm and power of 0.3 mW.

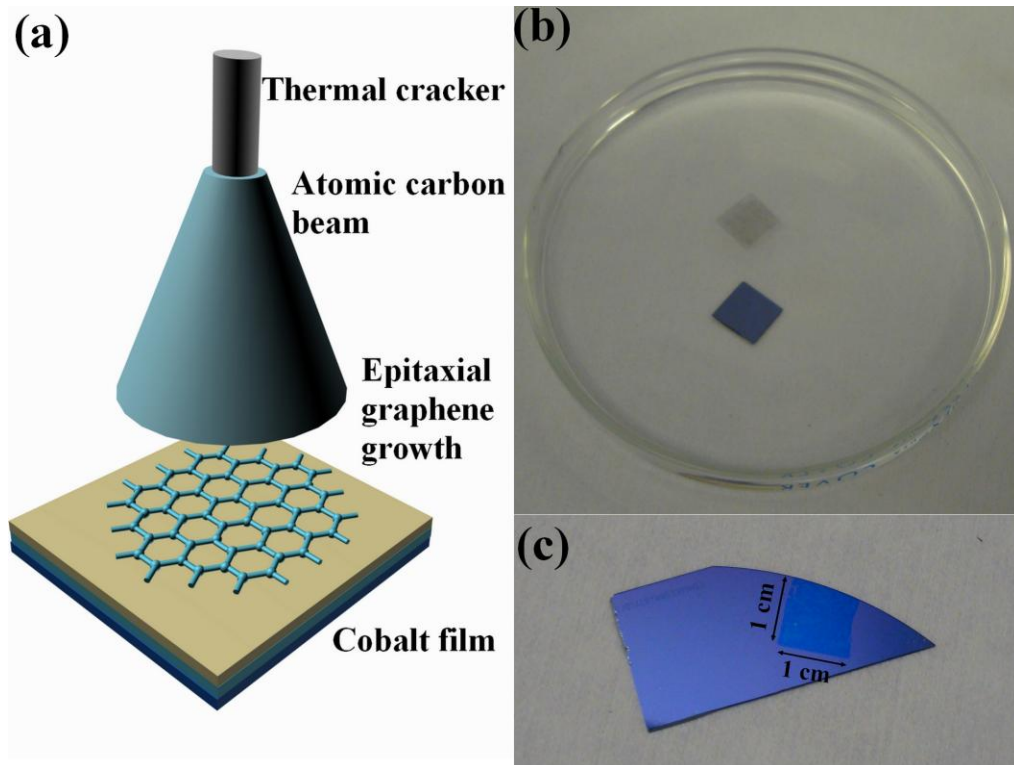


Figure 3-2 (a) A diagram of epitaxial graphene growth in thermal cracker enhanced GSMBE. (b) A floating PMMA/graphene after underneath Co film was etched in 5% HCl solution. (c) A transferred graphene film on SiO₂(300 nm)/Si substrate.

3.3 Results and discussion

Figure 3-2(b) shows the PMMA/graphene film floating inside solution after the metal substrate was etched. This sample was grown at the temperature of 950 °C. After 4-minute carbon growth with acetylene flow rate of 10 sccm, the sample was cooled at a rate of 10 °C/min. As seen from the figure, the PMMA layer effectively protects the intactness of the as-grown film. After the PMMA layer was dissolved, the graphene film still maintained continuous form and strongly attached to the SiO₂/Si substrate (Figure 3-2(c)). The size of the film is 1 cm × 1 cm, which is limited by the size of the substrate holder in the GSMBE system.

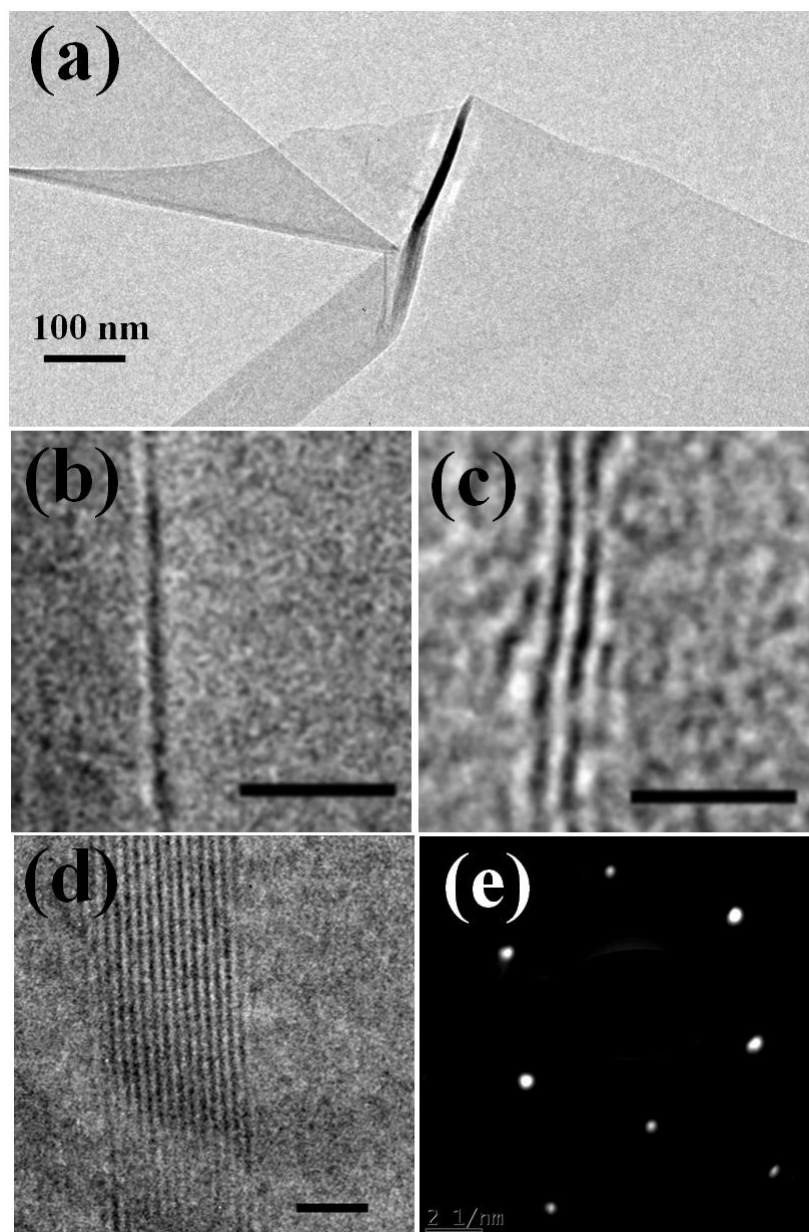


Figure 3-3 (a) Top-view TEM image of the graphene film. (b), (c) and (d) are TEM cross-sectional images of single-layer, bilayer and multi-layer graphene, respectively (The scale bar is 2 nm). (e) Diffraction pattern of as-grown sample.

Figure 3-3(a) shows a top-view transmission electron microscopy (TEM) image of the film. Except the areas where the graphene films fold up with each other, very even brightness of the film is evident, which indicates a good morphology of the as-grown film. Figures 3-3(b)-(d) show cross-sectional TEM images of single-layer, bi-layer and multilayer graphene, respectively, which exist in the same sample. The interlayer distance of 3.4 Å obtained by fast Fourier transform agrees with that of graphite. A clear hexagonal shape diffraction pattern from most part of the film confirms good crystalline of the as-grown film (Figure 3-3(e)).

Figure 3-4(a) shows an AFM image of the transferred film. The variation of the contrast in the image indicates different thickness of layers. The height measurement profile (Figure 3-4(b)) of the cross section indicated by the arrow in Figure 3-4(a) shows that the thickness of the film is around 0.8 nm, indicating single-layer graphene in this selected area. Different grains cause different number of layers during growth, and the boundaries between grains have thermal stress induced by the terraces-like steps. The edges between graphene and SiO₂ show as bright lines in Figure 3-4(a), the height of these edges is more than 2 nm according to the data from Figure 3-4(b), corresponding to graphene edges folding vertically.

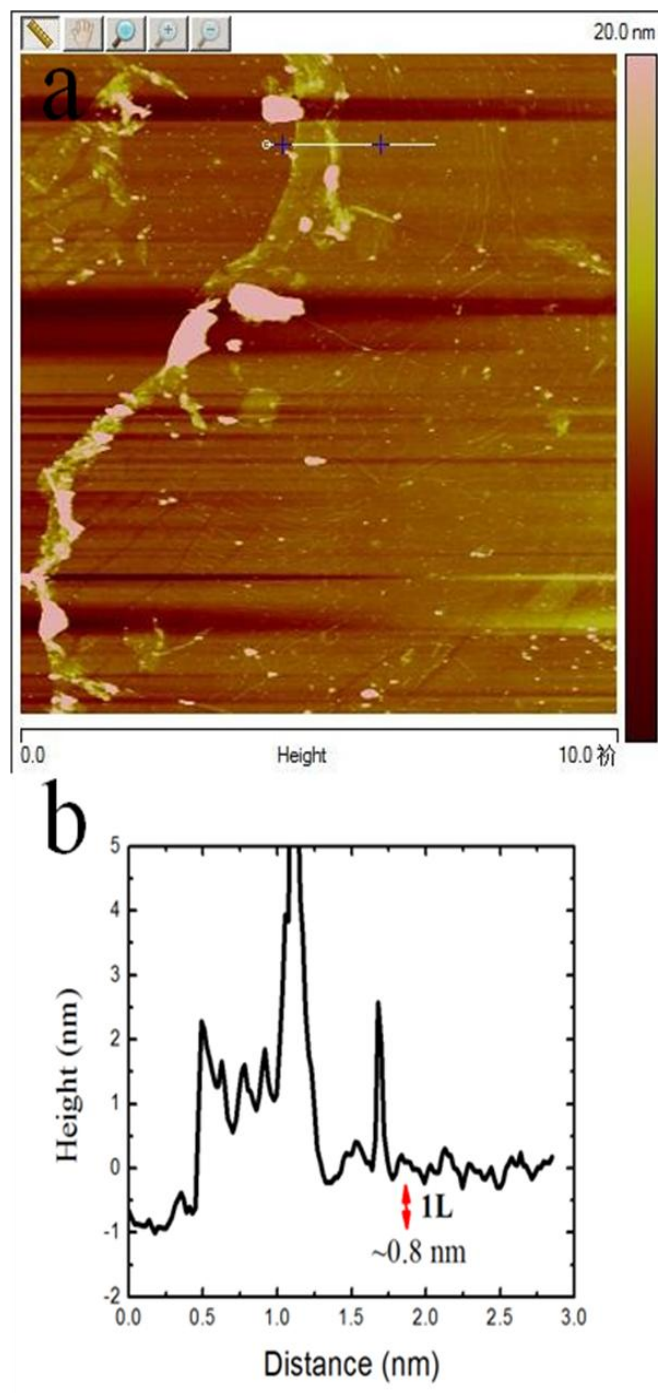


Figure 3-4 **(a)** AFM image of the graphene film. **(b)** Height measurement profile of the cross section indicated by the arrow in (a).

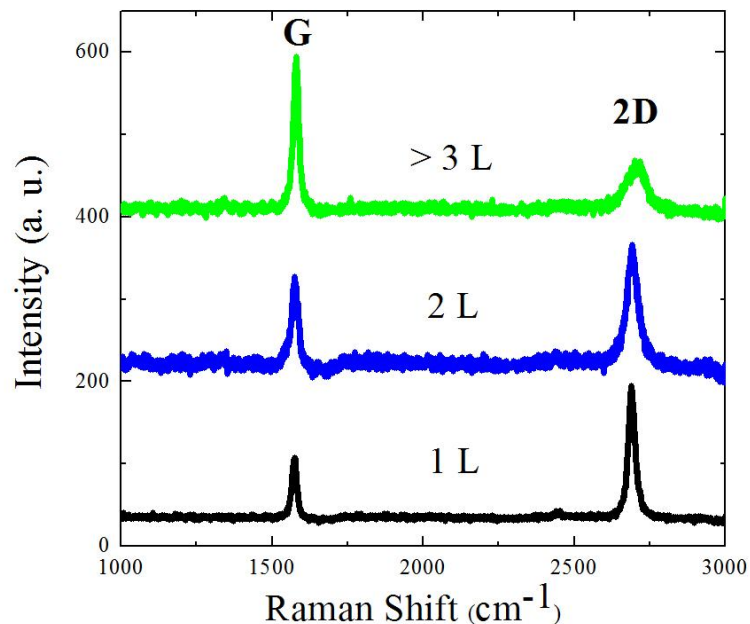


Figure 3-5 Raman spectra of graphene film grown at 950 °C.

Raman spectroscopy is a very powerful tool for characterizing carbon nanostructures because of its sensitivity to carbon sp^2 and sp^3 bonds. It has been noticed that the position of G peak ($\sim 1580 \text{ cm}^{-1}$), profile of 2D peak ($\sim 2700 \text{ cm}^{-1}$) and ratio of intensities between these two peaks (I_G/I_{2D}) change with the thickness of graphene films. Therefore, these features are widely used for counting the number of layers of graphene, especially exfoliated graphene films. However, due to the interface strain between as-grown graphene films and SiO_2 substrate during transferring process, G peak position is easily affected [21]. In addition, as-grown graphene usually does not have strict AB Bernal stacking between each layer, leading to insignificant dependence of evolution of

2D peak on the thickness of as-grown graphene films [22]. The only distinct feature left is the intensity ratio I_G/I_{2D} . Reina et al [9] found a quantitative relation between I_G/I_{2D} and number of layers; usually ratios of < 0.5 and $0.5\sim 1$ correspond to single- and bi-layer, respectively. For higher ratio (>1.8), the films are either multilayer graphene or graphite. To obtain the thickness distribution for graphene grown in thermal cracker enhanced GSMBE, this ratio gauge was also used. Figure 3-5 shows Raman spectra of the graphene grown at $950\text{ }^{\circ}\text{C}$, which was already transferred to SiO_2/Si substrate. Three curves were taken from three typical positions that exhibit different optical contrast under the optical microscope. The intensity ratios I_G/I_{2D} for the curves from bottom to top are 0.45, 0.73 and 3.17, corresponding to single-layer, bi-layer and multi-layer graphene, respectively. 93% single-layer and bi-layer coverage can be obtained by Raman mapping and color histogram in the optical microscopy image, which is much higher than that of graphene grown on Ni in CVD [7, 9]. No detectable D band ($\sim 1350\text{ cm}^{-1}$) was observed in single-layer and bi-layer areas, indicating good quality of the as-grown film. A very small D peak can be found in multilayer region, which may be due to the formation of dislocations at boundaries.

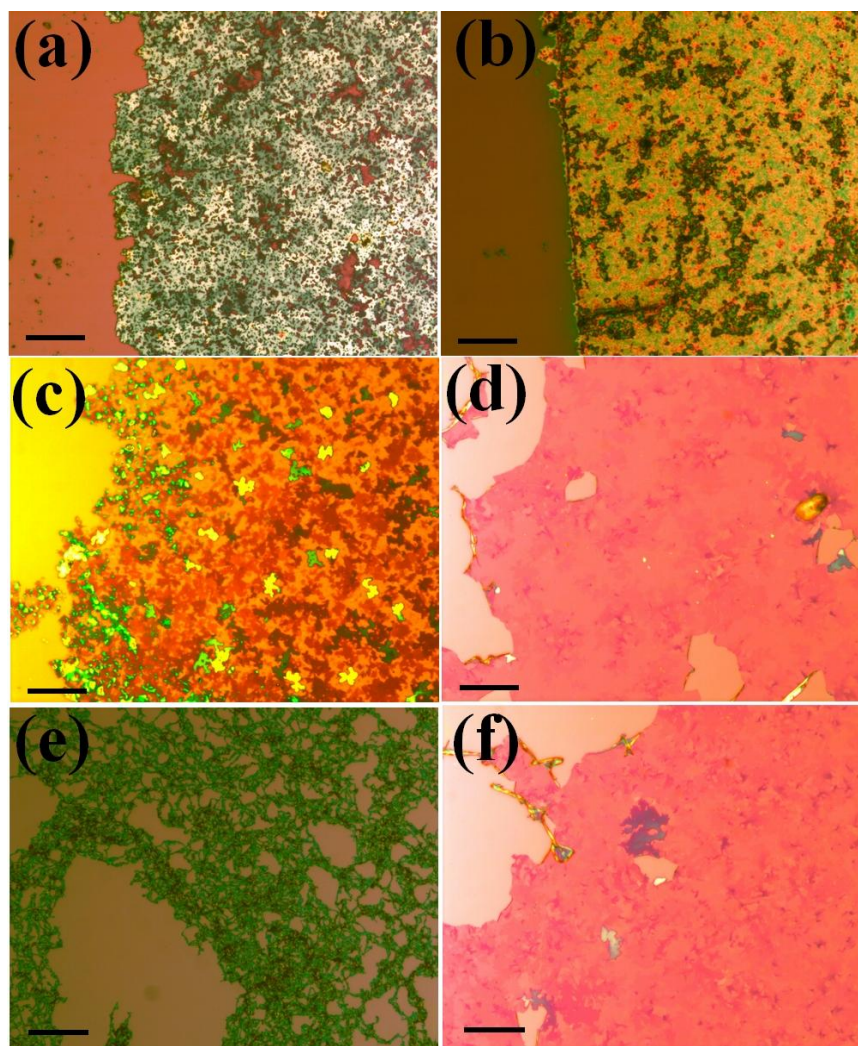


Figure 3-6 Optical microscopy images of grown graphene films on 300 nm SiO₂/Si substrate with different growth temperatures, (a) 800 °C, (b) 850 °C, (c) 900 °C, (d) 950 °C, (e) 1000 °C. The scale bar is 50 μm. Cooling rate of 10 °C/min was used for these five samples. (f) Graphene film synthesized at the same growth condition as (d) except using an average cooling rate of 200 °C/min.

Figures 3-6(a)-(e) show optical microscopy images of graphene films transferred on SiO₂/Si substrates. These films were grown at the temperatures from 800 °C to

1000 °C, respectively. All other growth conditions were kept the same including a cooling rate of 10 °C/min, a growth pressure of 3×10^{-3} Torr, a flow rate of 10 sccm, and a growth time of 4 minutes. As seen from Figures 3-6(a)-(b), very high color contrast between graphene films (right side of the images) and SiO₂ (left side of the images) can be observed, indicating the growth of graphite, which is also confirmed by Raman scattering measurements (not shown here). The as-grown films become thinner with the increase of the temperature, few-layer graphene with only small percentage (Figure 3-6(c)) emerges at 900 °C. As the temperature reaches 950 °C, uniform and continuous graphene films dominated by single-layer and bi-layer finally grow on the substrate (Figure 3-6(d)). Some holes in the image are mainly due to inadvertent physical damage during transferring process. Nevertheless, further increase of temperature to 1000 °C leads to graphene with porous net morphology (Figure 3-6(e)). Therefore, the growth temperature is critical to obtain good quality of graphene films in thermal cracker enhanced GSMBE. As-grown films could be either thick graphite or porous net if the temperature would be lower or higher than the optimal one, which is 950 °C in this case.

Graphene grown by carbon precipitation mechanism in CVD method typically requires a rapid cooling rate (160 °C/min or 600 °C/min [7-8, 20, 23]) to suppress the formation of multilayer graphene. In thermal cracker enhanced GSMBE, the situation is different. Figure 3-6(f) shows an optical microscopy image of the graphene sample, which was grown at a cooling rate of 200 °C/min from 950 °C. All other growth conditions for this sample are the same as that of the sample shown in Figure 3-6(d), in which a cooling rate of only 10 °C/min was used. No observable difference can be found

between Figure 3-6(d) and Figure 3-6(f), which means different cooling rates do not result in different number of layers in graphene growth. This result implies that the growth mechanism is direct epitaxial carbon growth in thermal cracker enhanced GSMBE rather than carbon precipitation as observed in CVD, which is further confirmed by growth time dependence as described in the following.

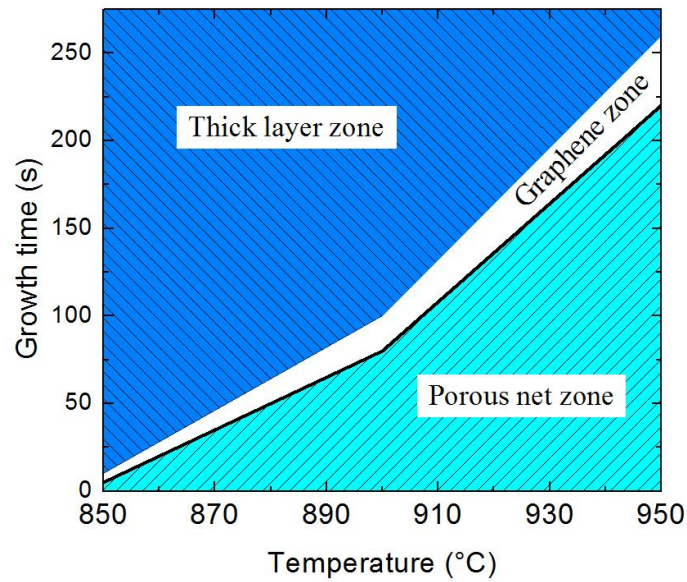


Figure 3-7 Diagram of the morphology of as-grown films versus growth time at different temperatures.

In addition to growth temperature dependence, similar phenomenon was observed when the films were grown at different growth times. Growth time dependence was carried out at the temperatures of 850 °C, 900 °C and 950 °C, respectively (Figure 3-7). At each temperature, graphene films started with porous net structures as the growth was short; became continuous films as the growth time was moderate; and evolved to thick

graphite as the growth was long. Since the cooling rate used in each growth is the same at 10 °C/min, this result is the direct evidence of direct carbon growth on Co. For quantitative analysis purpose, the thick film with single-layer and bi-layer coverage of less than 50% is defined as thick layer, and the film with holes occupying more than 50% of the whole area is defined as porous net. Figure 3-7(a) shows this quantitative dependence at different temperatures. The major part of the image is occupied by “thick layer zone” and “porous net zone”, graphene is formed only in a very small growth window. This growth window is only 5 seconds at 850 °C, and it becomes bigger with the increase of temperature, reaching 40 seconds as temperature is 950 °C.

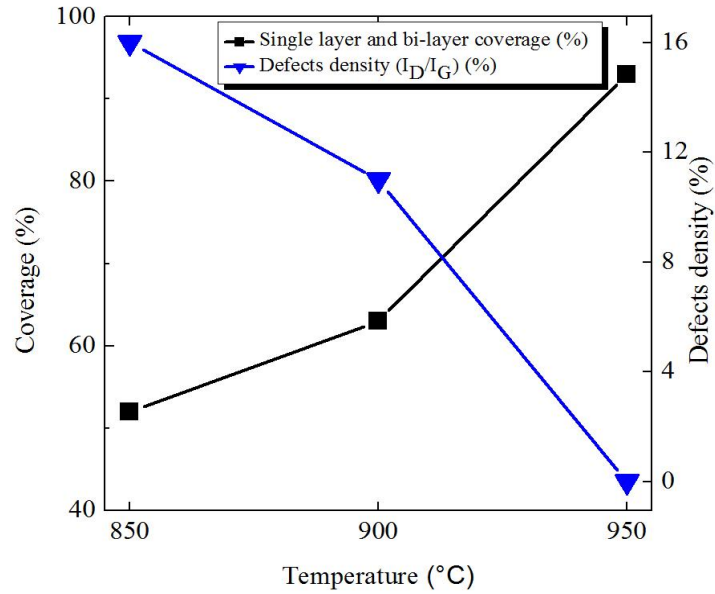


Figure 3-8 Single-layer and bi-layer coverage and defects density dependence on growth temperature.

Figure 3-8 shows single-layer and bi-layer coverage, and corresponding defects density (Raman peak intensity ratio I_D/I_G) as a function of growth temperature. The coverage of films grown at 850 °C is only 52%, and increases to 63% at 900 °C, and 93% at 950 °C; while the I_D/I_G ratio decreases from 16% at 850 °C, to 11% at 900 °C and further to negligible percentage at 950 °C. Low temperature causes insufficient thermal energy provided by substrate, which decreases the diffusion length of carbon atoms on the Co surface. The areas with more nucleation centers on grain boundaries easily keep absorbing carbon atoms and forming graphene. In the mean time, other areas have much less carbon to grow, which brings about unevenness and also lots of defects between different areas. With the increase of the substrate temperature, carbon atoms have larger diffusion length and more freely migrate around Co substrate. Fewer defects are observed because of more evenness across different areas. In addition, flatter Co surface may be generated at higher temperature, leading to more uniform first-layer graphene growth.

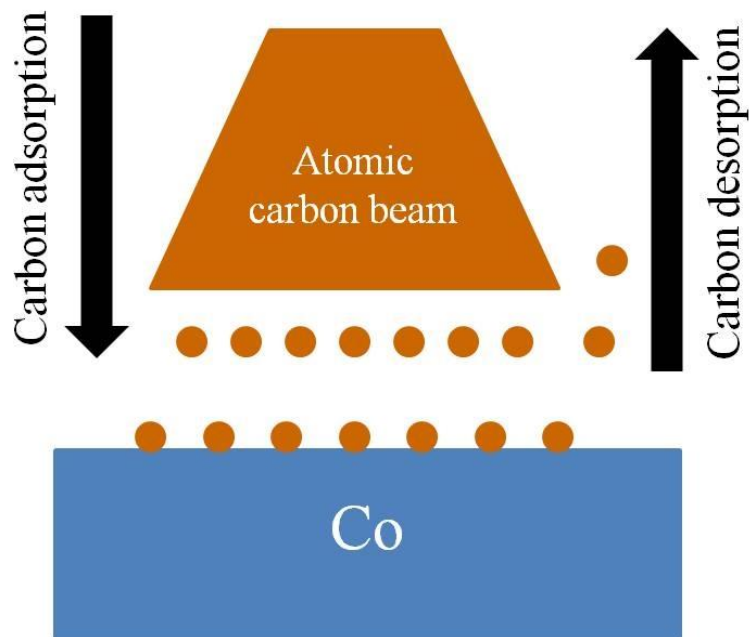


Figure 3-9 Diagram of graphene growth process in thermal cracker enhanced GSMBE system using Co as substrate.

Figure 3-9 indicates the growth dynamic process for graphene growth in thermal cracker enhanced GSMBE system. Once acetylene molecules are broken by thermal cracker, atomic carbon beam will be formed and impinge onto Co substrate. The substrate then adsorbs in-coming carbon atoms to form graphene. At initial stage when there are not enough incoming carbon atoms, boundaries and surface defects act as nucleation centers, having priority to absorb carbon atoms and form graphene film, which explains why short-time growth always brings about porous net. Once monolayer graphene covers Co surface, further carbon beam acts as source for epitaxial growth on existing layer, leading to thick layer growth. Besides the adsorption process, desorption process also plays an important role in graphene growth. As desorption coefficient

increases at higher temperature, carbon atoms get harder to be absorbed by Co to form graphene, leading to porous net morphology at 1000 °C (Figure 3-6(e)).

To measure the electrical properties and carrier mobility, graphene transistors were fabricated according to the procedure shown in Figure 3-10. After the film was transferred onto the SiO₂/Si substrate, the sample was annealed at 450 °C for 2 hours under H₂/Ar (100 sccm/ 100 sccm) flow to eliminate polymethyl-methacrylate (PMMA) residue occurred during the transfer. Photolithography was then carried out to create a 20 μm × 5 μm pattern followed by the deposition of 50 nm Cr mask using an electron beam evaporator. Oxygen plasma process was then conducted to etch the unprotected area in a reactive ion etching system to make the graphene channel. A second photolithographic step was used to open windows at the two ends of the graphene channel, followed by the deposition of Ti/Au (10 nm/80 nm) into these windows to form source and drain contacts. The highly doped n-type Si substrate with a resistivity of 0.025-0.05 Ω·cm was directly used as back gate.

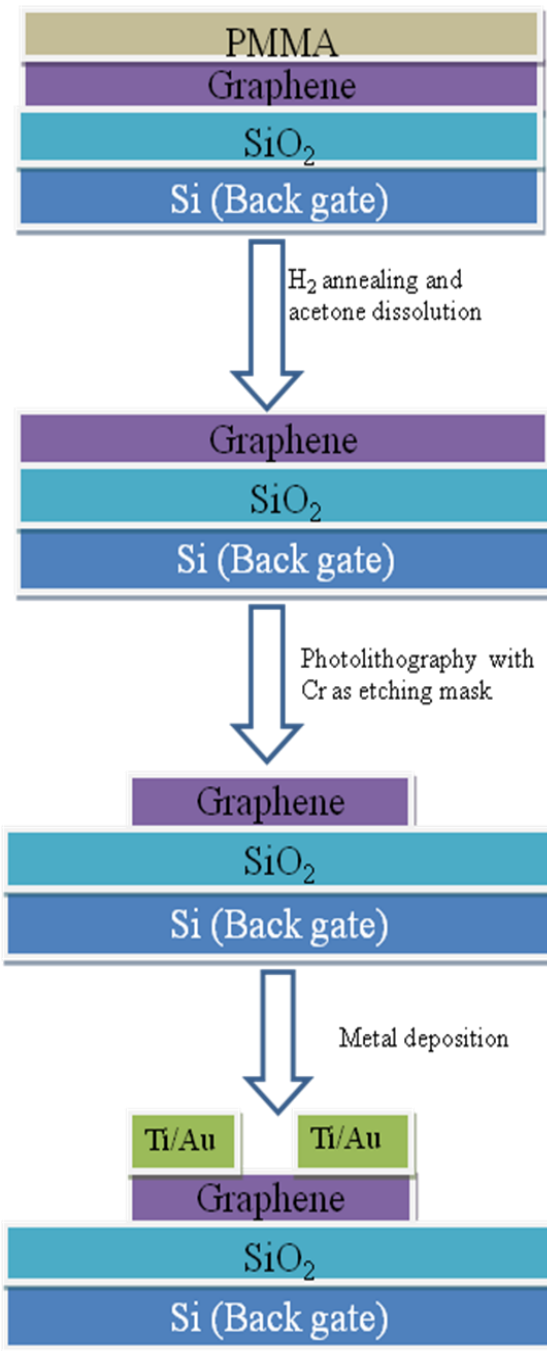


Figure 3-10 The fabrication flow of graphene transistors for field effect mobility testing.

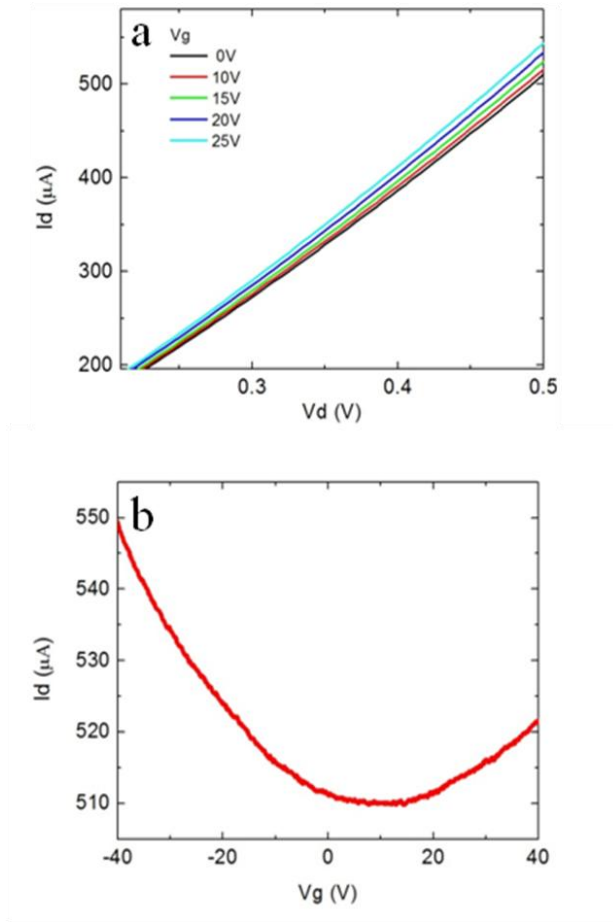


Figure 3-11 (a) Drain current I_d changes with drain voltage V_d under different gate voltages V_g . (b) Transfer curves at the drain voltage V_d of 0.5V.

Figure 3-11(a) shows the change in drain current I_d with drain voltage V_d at different gate voltages from 0 V to 25 V. No current saturation is observed, indicating the semi-metallic property of as-grown films. The transfer curves at the drain voltage of 0.5 V are shown in Figure 3-11(b). An ambi-polar characteristic shows the symmetric band structures for both electrons and holes near the Dirac point as predicted by theory. To calculate the field effect mobility of carriers, the following formula is used:

$$\mu = m_{lin} \frac{L}{W} \frac{1}{V_D} \frac{1}{C_i}$$

, where C_i is the gate insulator capacitance per unit area, m_{lin} is the slope of drain current versus gate voltage. Typically, motilities from $800 \text{ cm}^2/(\text{V s})$ to $1450 \text{ cm}^2/(\text{V s})$ can be acquired from as-grown films.

3.4 Conclusions

Large-area epitaxial grapheme films were achieved on Co substrates in thermal cracker enhanced GSMBE system. Clear TEM diffraction pattern and lacking D peak in Raman spectra indicate high quality of as-grown films. The single-layer and bi-layer coverage of 93% was achieved at an optimized temperature of 950°C . A narrow growth time window was found for different growth temperatures. Carbon absorption and desorption phenomena were responsible for temperature-dependent and growth time-dependent graphene morphology. Direct epitaxial growth mechanism was confirmed through temperature cooling rate and growth time dependent experiments. These studies suggest that thermal cracker GSMBE can be promising in growing large-area graphene on Co substrates.

3.5 References

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Chapter 4: Graphene based nickel nanocrystal flash memory

4.1 Introduction

As a potential candidate to replace silicon for future nanoelectronics, graphene has been used to fabricate various devices such as inverters [1], radio-frequency transistors [2], spin transport devices [3], resistive switches [4-5], ferroelectric memory [6] and flash memory [7-8]. Among these flash memories, water molecules or hydroxyl groups located on the interface between graphene and air were used as storage nodes [7-8]. The memory performance was strongly dependent on the surrounding air humidity and fabrication processes. For example, stored charges can easily leak out as a result of direct exposure of storage nodes to the ambient, leading to short retention performance of only several hours [7]. The retention performance was significantly reduced by placing the samples in vacuum. The traps discharge over approximately 1 day at a pressure of 10^{-2} mbar and > 3 days at 10^{-5} mbar (Figure 4-1). The appreciable volatility under ambient hints toward interaction between water molecules and functional groups on the SiO₂ (e.g., silanol groups) or hydroxyl groups located at the graphene edges [7]. To resolve these issues, we propose a structure of graphene flash memory using embedded nickel (Ni) nanocrystals as storage layer. Figure 4-2 shows the schematic of the device. High performance is demonstrated.

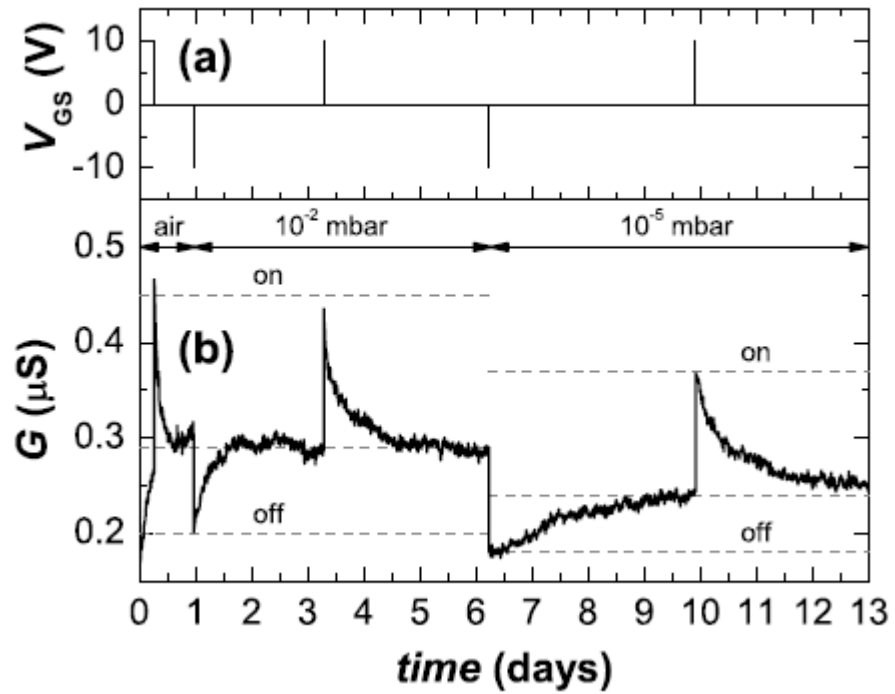


Figure 4-1 Data retention in the unpowered memory device. (a) Trigger signal. (b) Conductance acquired under ambient conditions and at room temperature at a pressure of 10^{-2} mbar and 10^{-5} mbar [7].

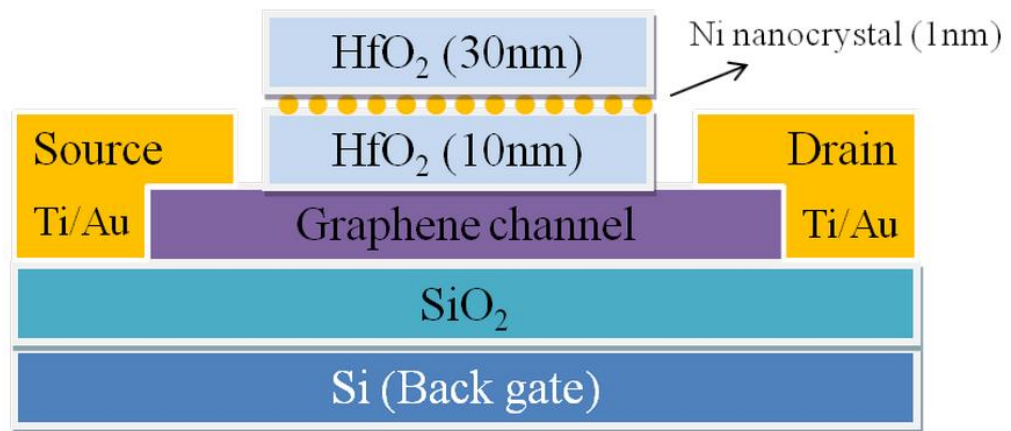


Figure 4-2 Schematic of graphene channelled Ni nanocrystal flash memory.

4.2 Device fabrication

To fabricate the device, graphene films were synthesized on Co thin films in a thermal cracker enhanced gas source molecule beam epitaxy, and were then transferred onto a $\text{SiO}_2(300\text{nm})/\text{Si}$ substrate. The growth details can be found elsewhere [9]. Figure 4-3(a) shows a planar view transmission electron microscopy (TEM) image of the graphene film. The even brightness of the film indicates a good morphology of the as-grown film. Most part of the film is comprised by single or bi-layer graphene as shown in the inset of Figure 4-3(a), which can also be proved by the low intensity ratio of G peak and 2D peak (less than 1) in Raman spectrum (Figure 4-3(b)) [10]. The absence of D peak in the Raman curve and clear hexagonal diffraction pattern (Figure 4-3(c)) indicates the high quality of as-grown film.

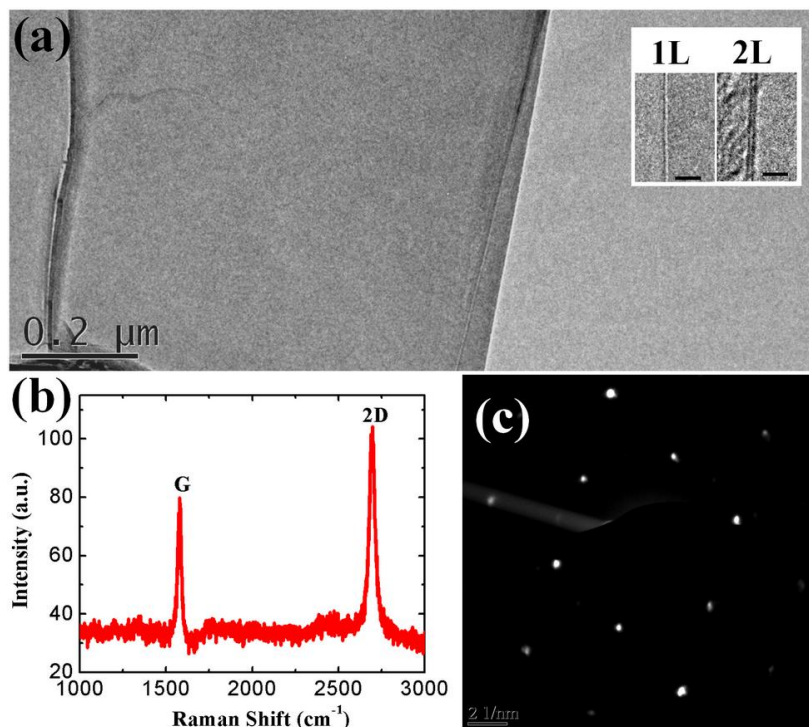


Figure 4-3 (a) Top-view TEM image of the graphene film. The inset shows the cross-sectional images of single and bi-layer graphene, respectively (The scale bar is 2nm). (b) Raman spectrum of synthesized graphene film. (c) Diffraction pattern of as-grown sample.

After the film was transferred onto the SiO₂/Si substrate, the sample was annealed at 450 °C for 2 hours under H₂/Ar (100 sccm/ 100 sccm) flow to eliminate the surface adsorbates (such as water molecule) and polymethyl-methacrylate (PMMA) residue occurred during the transfer. Photolithography was then carried out to create a 20 μm × 5 μm pattern followed by the deposition of 50 nm Cr mask using an electron beam evaporator. Oxygen plasma process was then conducted to etch the unprotected area in a reactive ion etching (RIE) system to make the graphene channel. A second

photolithographic step was used to open windows at the two ends of the graphene channel, followed by the deposition of Ti/Au (10 nm/80 nm) into these windows to form source and drain contacts. The highly doped n-type Si substrate with a resistivity of 0.025-0.05 $\Omega\cdot\text{cm}$ was directly used as back gate. After that, a 10 nm HfO_2 was grown at 110 $^\circ\text{C}$ on the top of the graphene channel by atomic layer deposition (ALD) to form the tunneling layer. A 1nm Ni layer deposited on the HfO_2 film an electron beam evaporator with a deposition rate of 0.1 $\text{\AA}/\text{s}$, followed by a rapid thermal annealing (RTA) at 600 $^\circ\text{C}$ for 15 seconds in N_2 . Figure 4-4 shows scanning electron microscope (SEM) images of Ni nanocrystals before and after thermal annealing. A high density of $\sim 1.1 \times 10^{12} \text{cm}^{-2}$ and an average size of 7nm were found for the as-annealed dots. Finally, another 30 nm HfO_2 blocking oxide was grown by ALD to passivate the nanocrystals. Since the source/drain metals were also covered by the deposited HfO_2 film, a third photolithography step was conducted to open windows at the source/drain areas, where the insulator film was etched by a HF solution until the metal contacts were exposed. The fabrication procedure is also shown in Figure 4-5.

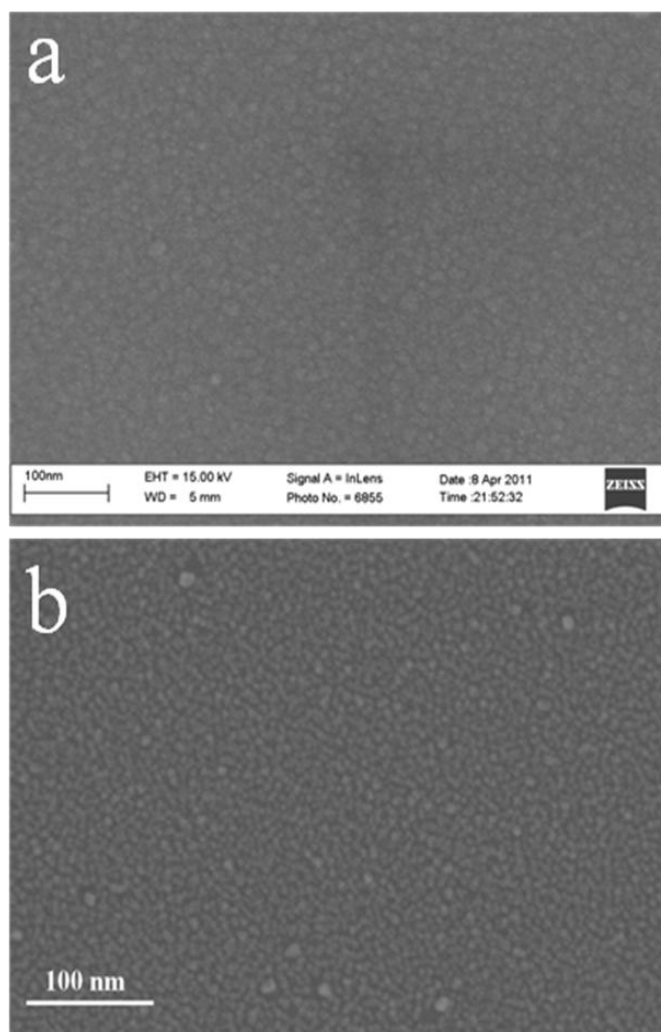


Figure 4-4 SEM images of Ni nanocrystals. (a) Before annealing (b) After annealing.

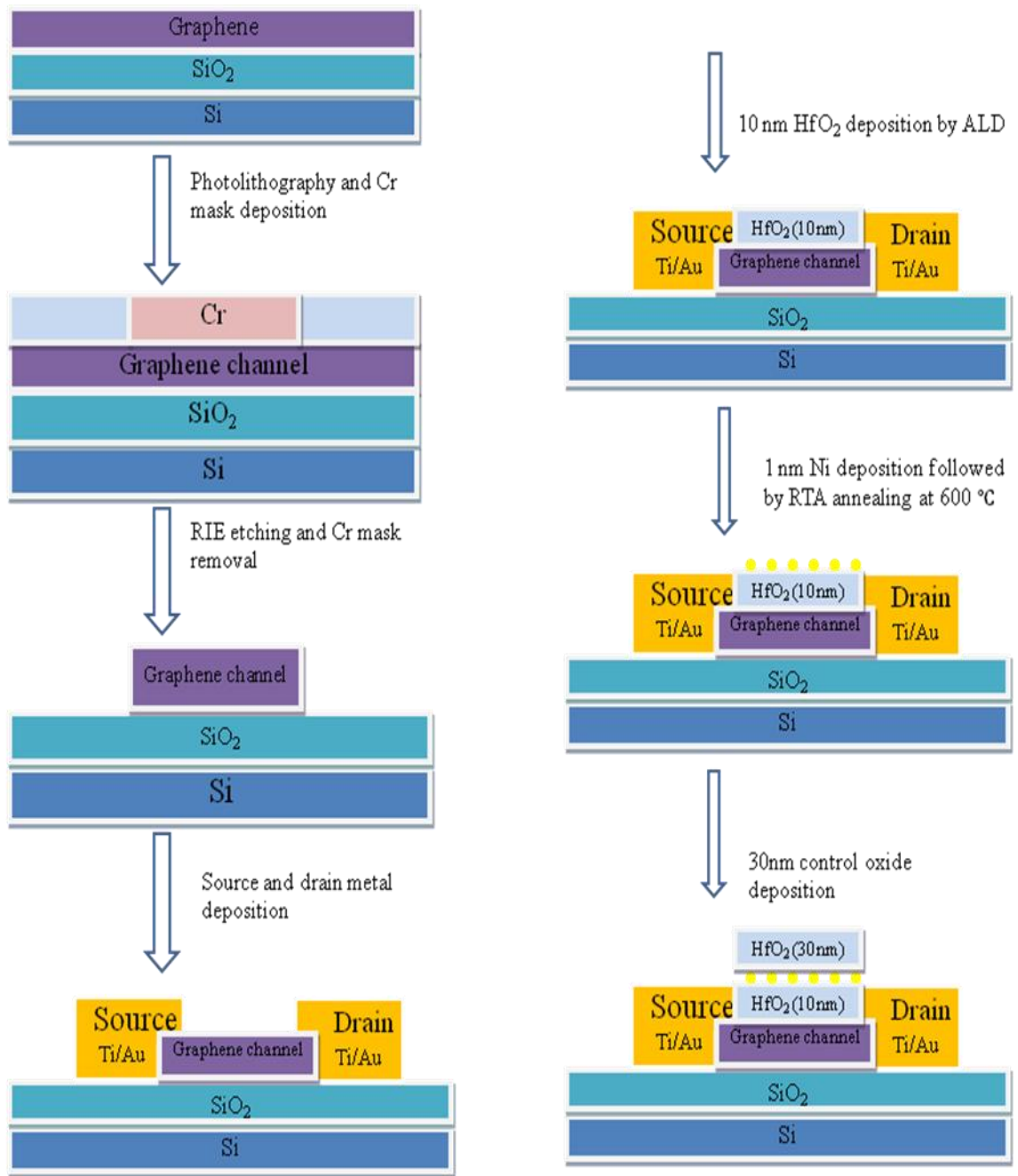


Figure 4-5 The fabrication procedure of graphene based nickel nanocrystal flash memory.

4.3 Device testing and discussions

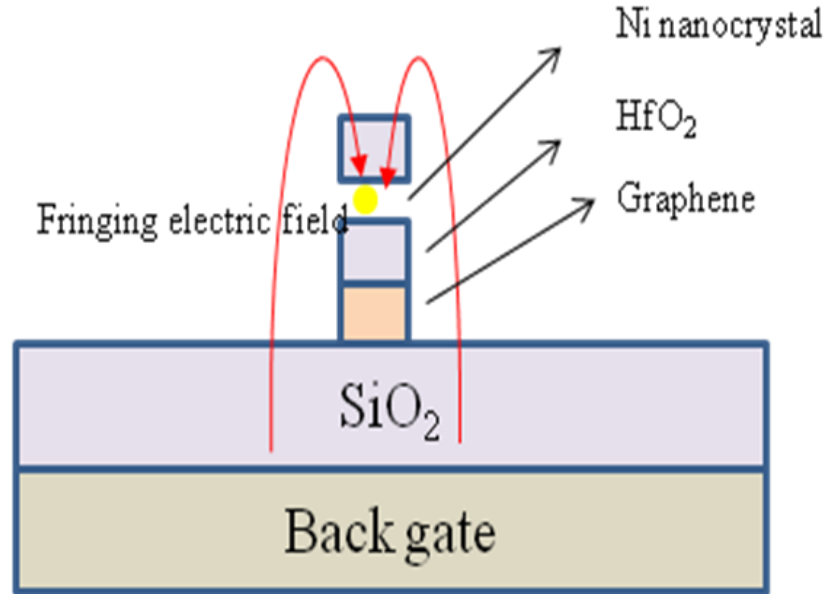


Figure 4-6 The diagram of charging and discharging processes of nickel nanocrystals by back gate voltage.

Figure 4-7(a) shows the change in drain current I_d with the back gate sweep within a ± 20 V range. The Dirac point shift, i.e., memory window of larger than 10V was demonstrated, which is much bigger than other reported graphene or carbon nanotube flash memory data [7,11]. The reason that the device can be programmed and erased with a back gate is that unlike a planar two-dimensional Si channel, the graphene strip here can be considered as one-dimensional channel because of its much smaller size compared to the two-dimensional back gate. In this case, the fringing electric fields originated from the gate have effect on both the channel and the nanocrystals. Therefore, the nanocrystals have a potential between that of the back gate and the channel, which is grounded during

the programming/erasing; and the potential difference between the nanocrystals and channel results in charging and discharging of the storage node during the operation (Figure 4-6) [12]. As seen in Figure 4-7(a), when the sweep starts with -20 V, electrons are repelled from the nanocrystals through the oxide to the graphene, which moves the Dirac point to the left. As the sweep starts from +20V, the Dirac point is shifted to the right due to the electron storage from the channel to the nanocrystals.

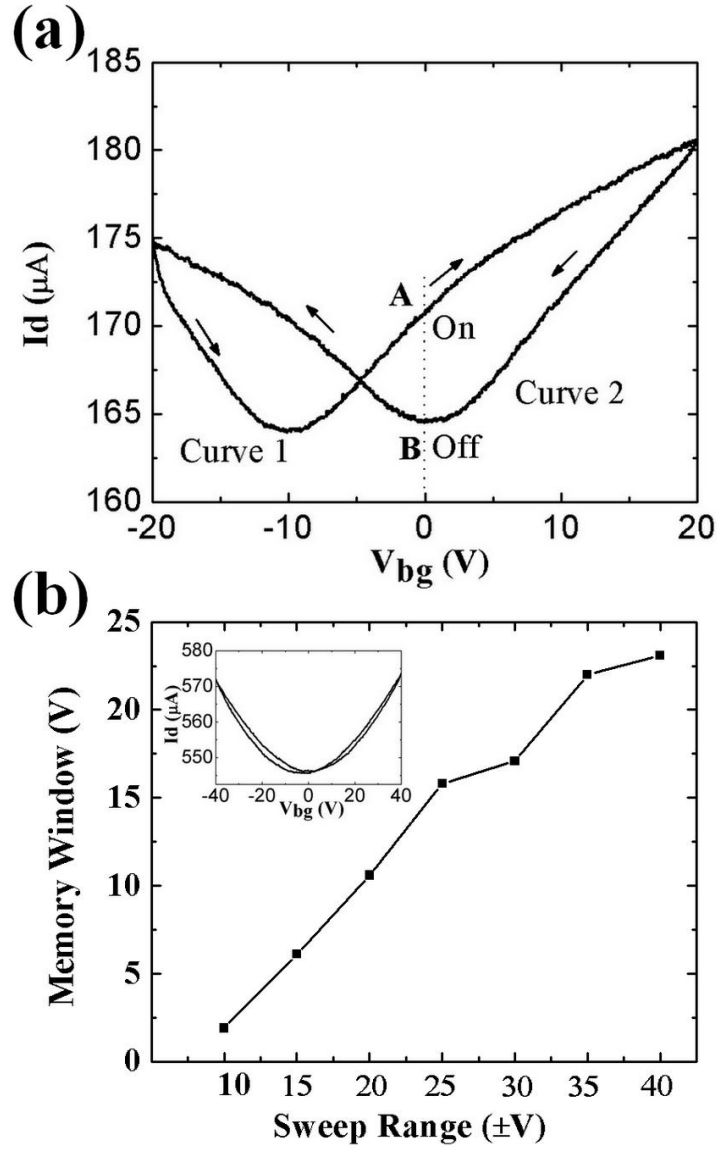


Figure 4-7 (a) Transfer curves of graphene based Ni nanocrystal memory at the drain voltage V_{ds} of 1V. The gate sweep direction is indicated by the arrows. (b) Memory window as a function of the sweep range for graphene based Ni nanocrystal memory. The inset shows the I_d - V_{bg} sweep for the reference device without Ni nanocrystals.

Figure 4-7(b) shows memory windows at different sweep ranges. The memory window is only 1.9 V when the range is from -10 V to +10 V, and increases almost linearly with the increase of the range from $\pm 10\text{V}$ to $\pm 35\text{V}$, beyond which it starts to show saturation. The window reaches 23.1 V when the range is $\pm 40\text{V}$. To clarify the source of this memory effect, a reference device was also fabricated. Only 40nm HfO_2 cap layer was deposited on graphene channel with the same recipe by ALD, and no Ni nanocrystal was embedded in HfO_2 thin film. The inset of Figure 4-7(b) shows the transfer curves for this reference device. Only a small memory window of about 3 V was found, compared to that of 23.1 V for the nanocrystal device under similar sweep range. As mentioned before, the only difference between the nanocrystal device and the reference sample is the embedded Ni nanocrystals, indicating that the large memory window primarily derives from the Ni nanocrystals but not the HfO_2 thin film. However the small memory window of the reference sample should be due to the existence of bulk traps in HfO_2 [13].

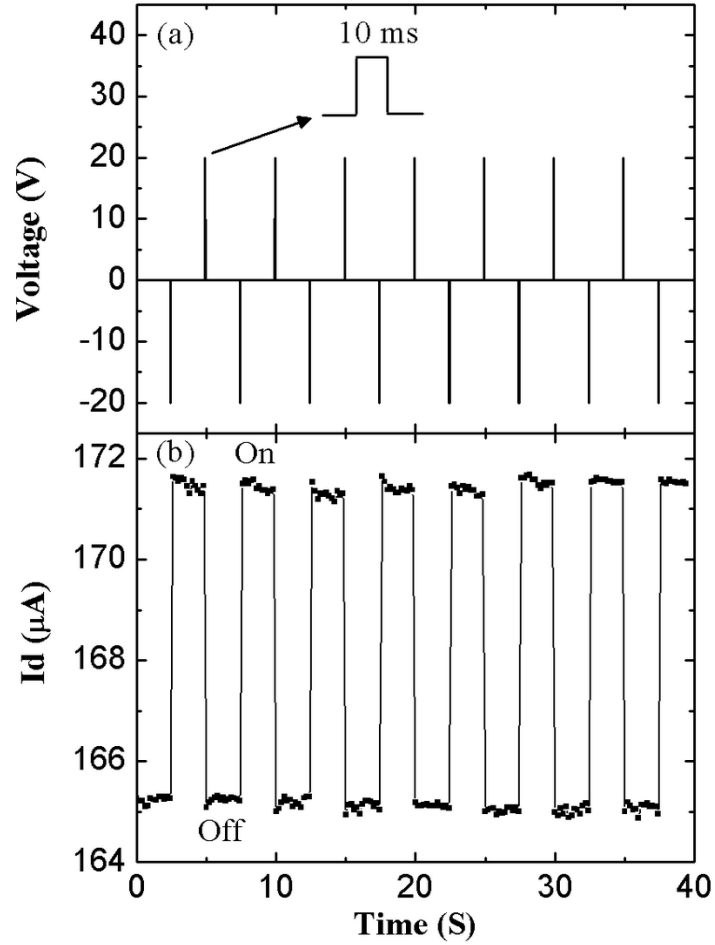


Figure 4-8 Memory effect of graphene based Ni nanocrystal memory. (a) A back gate trigger signal with amplitudes of ± 20 V, a pulse width of 10 ms, and a period of 5 s. (b) Drain current response to the trigger signal in (a).

To further study the memory effect of the device, bipolar pulse signals of ± 20 V were applied on the back gate as program/erase biases. The reading gate bias was set to 0 V to eliminate the static charge and its effect on retention performance during testing

(Figure 4-8(a)). The very short pulse with width of 10 ms periodically charges or discharges the nanocrystals and shifts the I_d - V_{bg} scan. After a positive gate pulse, the Dirac point shifts right as shown by curve 2 in Figure 4-8(a), while curve 1 is a result of a negative gate pulse. To understand the on/off operation of this device, the higher current (point A) at zero gate bias in curve 1 is defined as on state, and the lower point B in curve 2 is recognized as off state in Figure 4-8(a). During static pulse response measurement, as shown in Figure 4-8(b), the on and off states, which were monitored under the drain voltage of 1 V, appear immediately after a negative or positive 20 V pulse. The two states persist after the pulse is reset, which indicates the good memory performance of the device. Additionally, endurance testing was done with the same ± 20 V pulse on the back gate at a frequency of 5 Hz and a duty cycle of 0.2%. No obvious failure or performance degradation was found after programming/erasing cycles of 5×10^5 , which suggests very good endurance of the device. While the same bipolar pulse was applied on the reference sample, no distinguishable on and off states were found (not shown here), which indicates little memory effect for the reference sample.

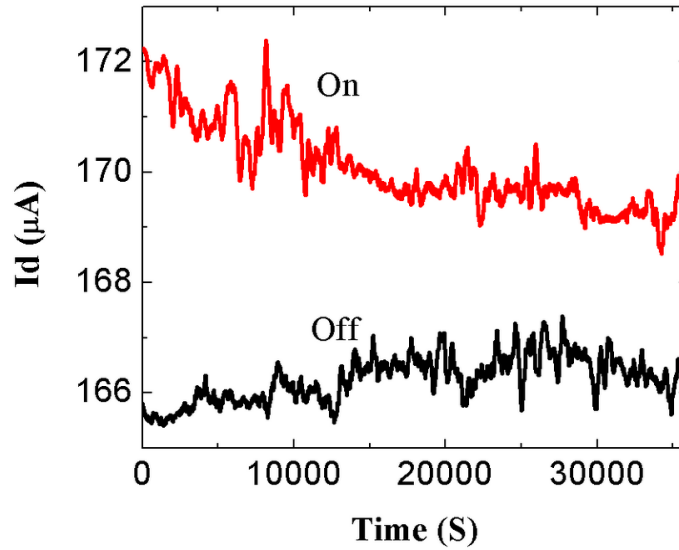


Figure 4-9 Retention performance for the on and off states of graphene based Ni nanocrystal memory.

Because of a relatively flatten curve near the Dirac point in the ambipolar transfer characteristic, drain current instead of threshold voltage change versus time has been chosen to perform retention test for the device. A +20V/-20V bias was applied on the back gate for 10s prior to the off state/on state retention test, respectively. Figure 4-9 shows the on and off states retention performance while the drain is constantly biased at 1V. Both on and off state currents decay slightly during the earlier retention stage within about 1.4×10^4 s, after which an evidently large memory window was still observed even if the measurement reaches 3.6×10^4 s, indicating significant improved charge retention performance over other graphene or carbon nanotube flash memory devices (Figure 4-10) [7, 11]. The improvement attributes to much better charge retention ability of embedded Ni nanocrystals compared to that of water molecules [7] and bulk oxide defects [11].

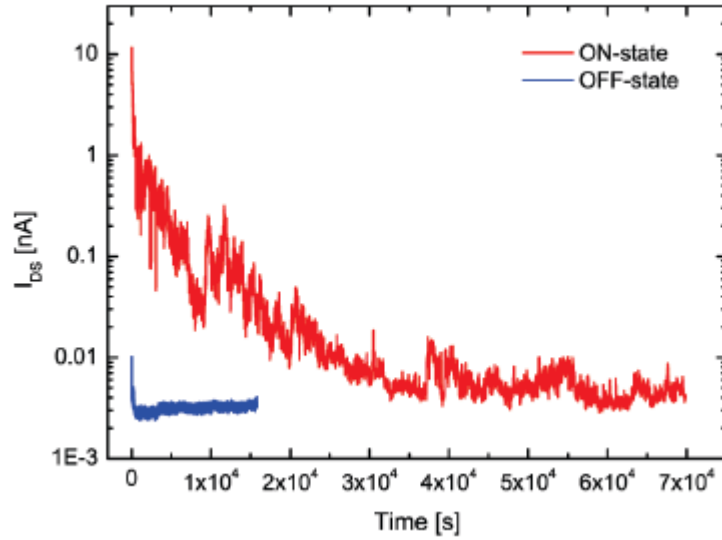


Figure 4-10 The retention performance of CNT flash memory [11].

The field effect mobility was acquired as $310 \text{ cm}^2/(\text{V s})$ by calculating transfer curves using the same formula as in last chapter. Typically, a value variation between $300 \text{ cm}^2/(\text{V s})$ to $520 \text{ cm}^2/(\text{V s})$ (Transfer curves are shown in Figure 4-11) can be found among different devices. The significant field effect mobility degradation ($\sim 60\%$) can be observed after HfO_2 deposition on top of graphene surface. The graphene mobility before dielectric deposition is majorly limited by the scattering between the synthesized graphene boundaries [14] and the lattice interaction from underneath SiO_2 substrate. After dielectric deposition, ALD deposited HfO_2 films are generally oxygen deficient, these oxygen vacancies and other imperfection of as-grown films form as points defects. Because of the energy band alignment between HfO_2 and graphene, these points defects can be easily charged as impurities when electrons move out. The significant mobility

degradation after HfO_2 deposition should be attributed to the effect from charged impurities. A similar discussion can also be found elsewhere [15].

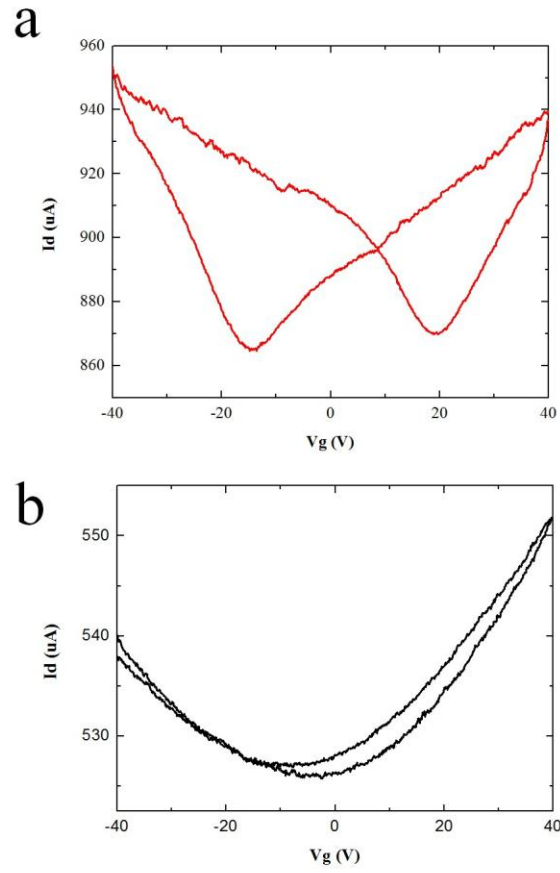


Figure 4-11 Transfer curves of (a) graphene based Ni nanocrystal memory and (b) a comparison device without embedded Ni nanocrystal.

4.4 Conclusions

In summary, Ni nanocrystals were used as storage node for graphene field effect transistor memory. Large memory window of 23.1V was demonstrated. Excellent endurance and long retention were also observed. The results suggest that nanocrystal based graphene memory is promising for future nonvolatile memory technologies.

4.5 Reference

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Chapter 5: Graphene nano dots memory capacitor

5.1 Introduction

Flash memory has been scaling down following Moore's Law since 1990S. However, this scaling becomes more and more difficult beyond 32 nm node. Because a very thin gate oxide of less than 10 nm is used, the conventional floating gate type structure has the following drawbacks. First of all, the stored charges can easily leak out through the weak points of thin tunneling oxide, leading to short retention performance. Secondly, the operation voltage (V_{DD}) decreases while devices scale down, but the conventional flash memory device needs higher voltage than V_{DD} to make sure electrons have enough energy to overcome the barrier between channel and floating gate. To solve the above issues, silicon-oxide-nitride-oxide-silicon (SONOS) memory and nanocrystal based flash memory were proposed.

For a SONOS memory, a small sliver of silicon nitride was embedded inside gate oxide. The sliver of nitride is non-conductive but contains a large number of charge trapping sites and is able to hold an electrostatic charge. The nitride layer is electrically isolated from the surrounding transistor, so charges stored on the nitride directly affect the conductivity of the underlying transistor channel without interfering others. The oxide/nitride/oxide sandwich typically consists of a 2 nm thick tunneling oxide, a 5 nm thick silicon nitride middle layer, and a 5-10 nm block oxide. The structure can be seen in Figure 5-1. Nanocrystal flash memory uses discrete nano dots as storage nodes instead of having continuous conductive floating gate as conventional structure. The shared

advantage of SONOS and nanocrystal memories over the conventional structure is the immunity of retention from the leaky paths in the oxide. The leaky paths could be either from fabrication process or stress induced defects generated in the high field programming/erasing.

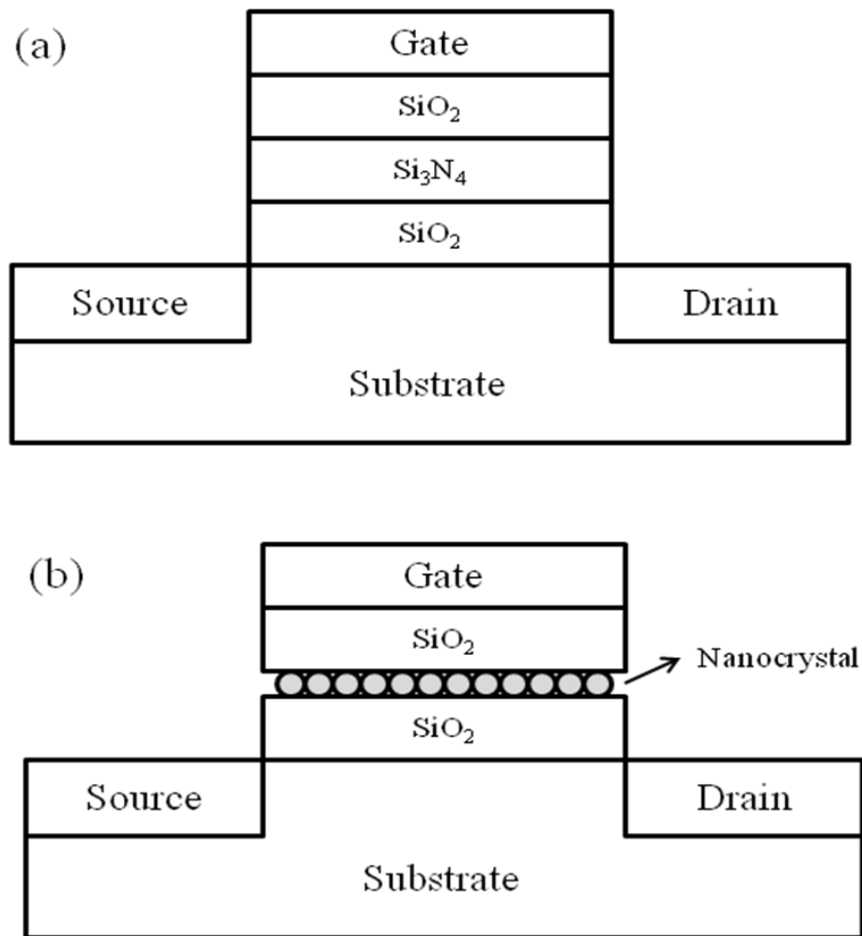


Figure 5-1 The structures of (a) SONOS memory and (b) nanocrystal flash memory.

SONOS type memory has a simpler process complexity compared to forming nanocrystals of correct size and density and preserving them during subsequent processing as in flash memory fabrication. However, nanocrystal flash memory also

exhibits the following advantages. First of all, nanocrystal flash memory can have a deeper electron storage traps (~ 3 eV) than that of SONOS memory (1-2 eV), leading to an improved retention performance. Secondly, nanocrystal memory has a better feasibility to control the ordering of trap sites. The charge trapping sites in a SONOS cell originate from the nitride dangling bond, which is difficult to control. But the morphology of nano dots can be optimized by self-assembly method [1-3]. Thirdly, nanocrystal memory also has the potential application in multiple bits storage. Due to the small size of the nanocrystals (< 10 nm), coulomb blockade effect is strong. The electron charge will raise the nanocrystal's potential and reduce the electric field across the tunneling oxide, leading to the reduction of programming current [4]. For a nanocrystal of 3 nm diameter, 2.5 nm thick tunneling oxide and 5 nm control oxide, the electrostatic charge energy will be ~ 95 mV if one electron exists in the nanocrystal. This energy will increase to 380 mV after the second electron is stored into the dot [5]. The charging energy separates clearly at different memory charge statues, and favors the application for multi-level storage for the nanocrystal memory cells.

Both semiconductors and metals have been used to fabricate nanocrystals. Si and Ge are two mostly used materials due to their compatibilities to current silicon technology. High-density semiconductor nanocrystal memory has been reported and long retention time was observed. However, it is believed that traps and defects inside or at the surface of nanocrystals can work as storage nodes; the data storage mechanism is similar to SONOS memory. Therefore, the control of trap level and density is thus critical for performance consistency in different devices. However, such control is difficult because

of the high sensitivity of trap formation during the further annealing process. Various metals, such as Ag, Au, Pt, W, Co, Ni, etc, have also been tried to synthesize nanocrystals. Compared with semiconductor nanocrystal memories, metal nanocrystal memories generally possess several advantages, such as strong coupling with the conduction channel, a wide range of available work functions and high density of states around the Fermi level. By selecting suitable metal nanocrystals to engineer the work function, both the storage capacity and the retention time can be improved.

As a semi-metal material, graphene also has properties which are suitable for flash memory application as metals do. First of all, it is revealed that the work function of graphene is in a similar range to that of graphite (~ 4.6 eV) [6]. Figure 5-2 shows the energy diagram of a memory capacitor using graphene as the storage layer. The Fermi level of graphene is almost in the middle Si band gap. A good retention performance is expected because the deep quantum well prevents stored charges from leaking out. Additionally, because of the dome structure of fabricated nanocrystals with a typical height of 5~10 nm, the subsequent oxide growth will follow the topography of nanocrystals, the risk of high defects density can be predicted by the non-uniform block oxide growth. Because of the good surface morphology of as-grown graphene films, we propose to use graphene nano dots as storage nodes to fabricate memory capacitors.

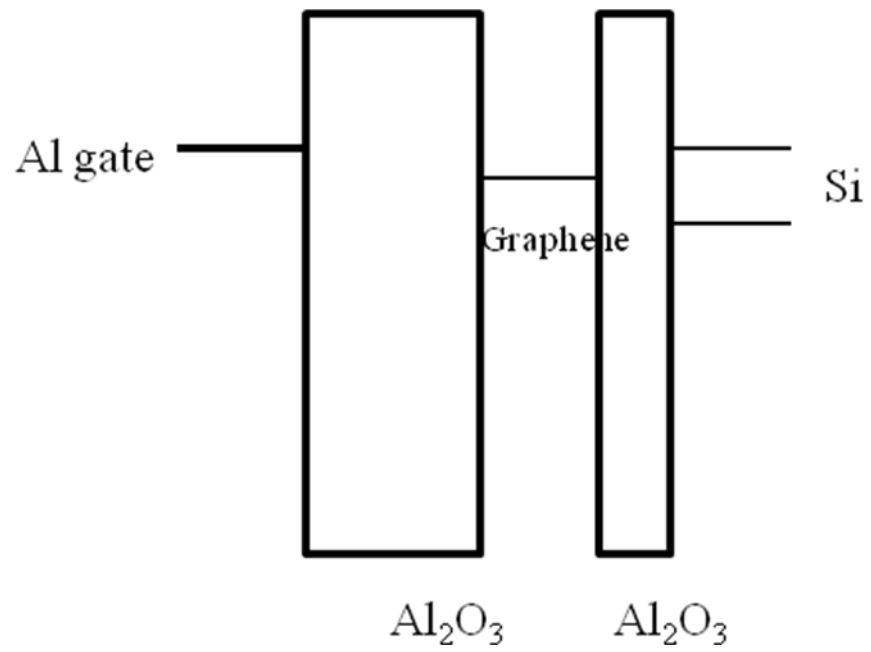


Figure 5-2 The energy diagram of a memory capacitor using graphene as the storage layer.

5.2 Device fabrication and experimental discussion

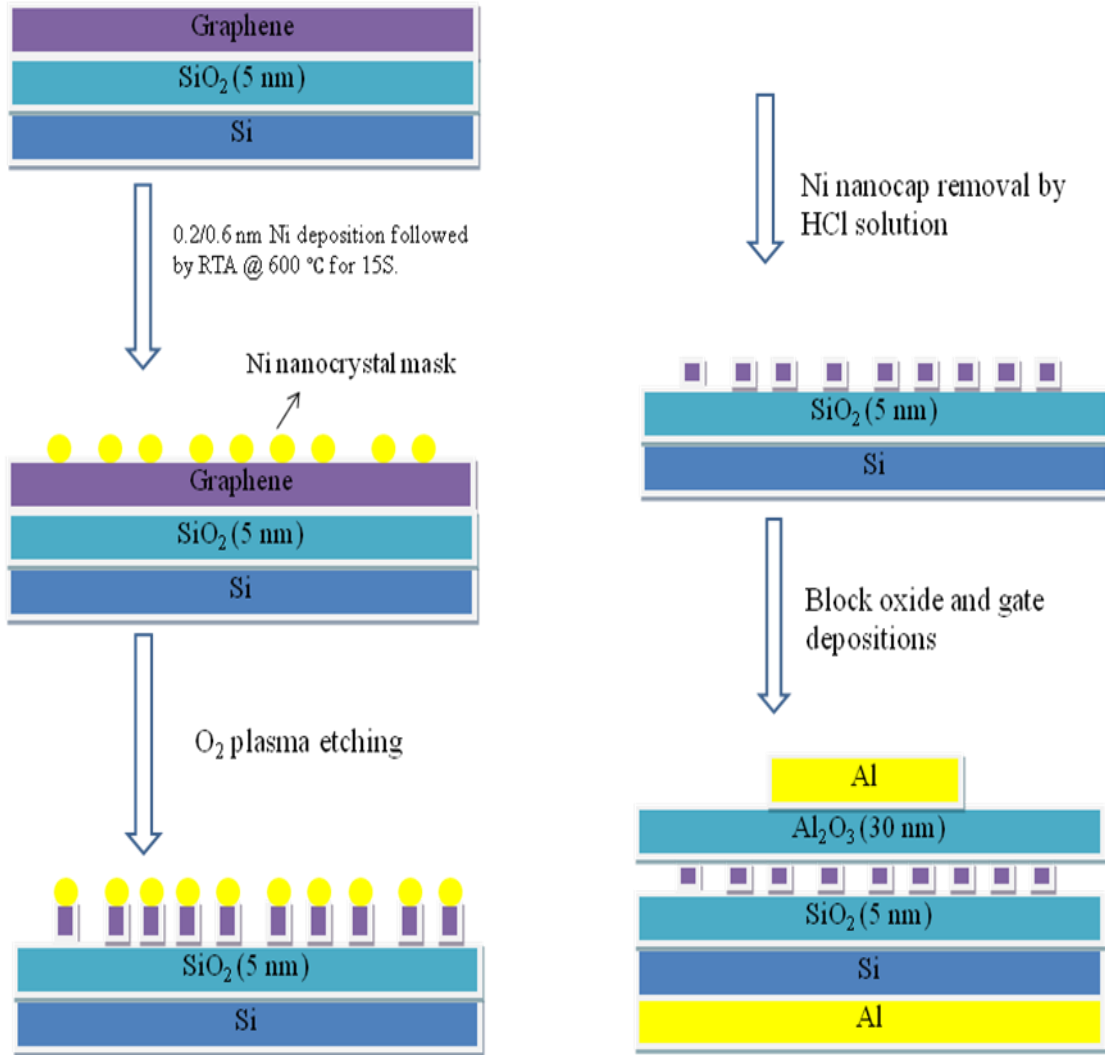


Figure 5-3 The fabrication procedure for graphene nano dots memory capacitor.

After graphene films were synthesized by using Co as substrate as mentioned in chapter 3, the film was transferred onto the SiO₂ (5 nm thermal oxide)/Si substrate and annealed at 450 °C for 2 hours under H₂/Ar (100 sccm/ 100 sccm) flow to eliminate the surface adsorbates (such as water molecule) and PMMA residue occurred during the

transfer. A thin Ni layer (0.2 nm ~ 0.6 nm) deposited on the graphene film by an electron beam evaporator with a deposition rate of 0.1 Å/s, followed by a RTA process at 600 °C for 15 seconds in N₂. Ni nanocrystal formed after annealing and worked as etch mask in subsequent processes. Oxygen plasma process was then conducted to etch the unprotected area in a reactive ion etching (RIE) system to make graphene nano dots. After that, a 30 nm Al₂O₃ was grown on the top of the graphene channel by ALD to form the block layer. Finally, 100 nm Al deposited on the both sides of the sample and formed as two contacts (Figure 5-3).

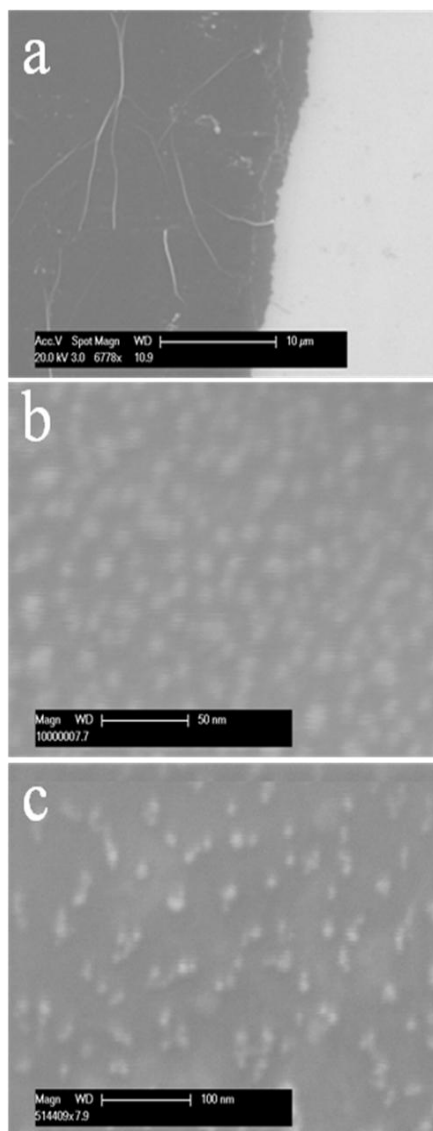


Figure 5-4 SEM images of (a) graphene film on SiO₂/Si substrate, (b) Ni nanocrystal on top of SiO₂/Si and (c) Ni nanocrystal on top of graphene.

Figure 5-4(a) shows a SEM image of graphene film on SiO₂/Si substrate. The left dark side is graphene. An even brightness of the graphene area indicates the uniform thickness of the as-grown film. After a thin Ni layer deposition followed by a RTA

process, a layer of Ni nanocrystals uniformly forms on top of SiO₂ surface as shown in Figure 5-4(b). However, the Ni nanocrystals on graphene are not well-ordered (Figure 5-4(b)). The reason might be due to the perfect surface of graphene films, which cannot provide nucleation sites for nanocrystal formation. Figure 5-5 shows the image of graphene nano dots after removing Ni nano caps. The discrete dark dots are graphene, and the left part of the image is SiO₂/Si substrate. Graphene dots with the range from 10 nm to 100 nm can be observed in the image.

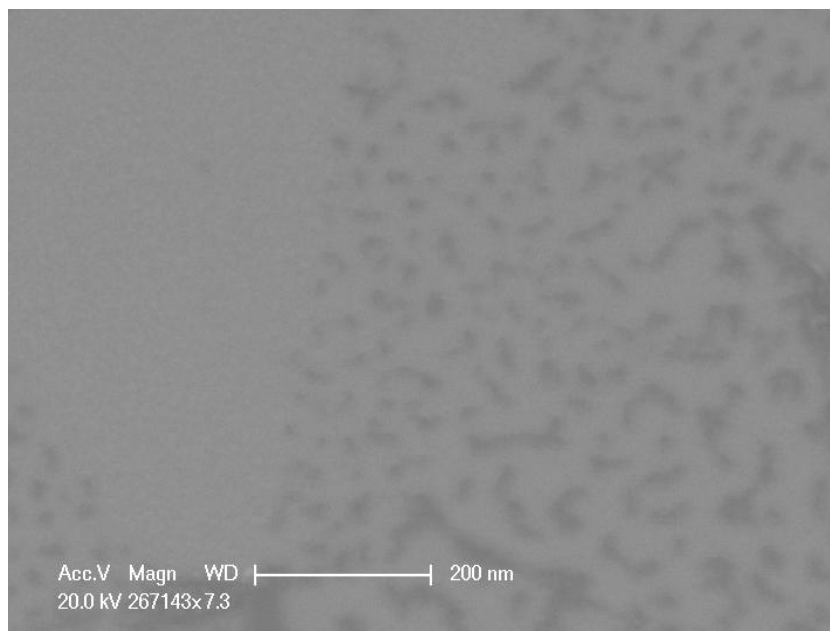


Figure 5-5 A SEM image of graphene nano dots.

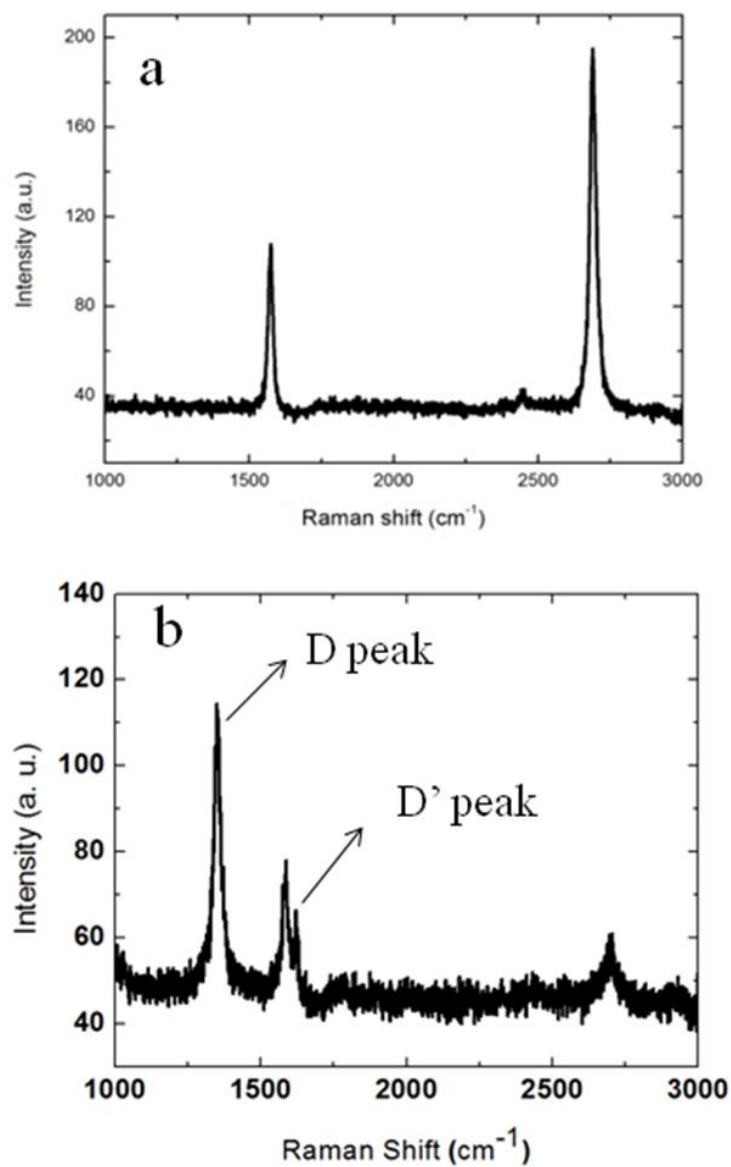


Figure 5-6 Raman spectra of (a) graphene films and (b) graphene nano dots.

To measure the quality of as-fabricated graphene nano dots, Raman spectra was carried out. Figure 5-6 shows the comparison between a graphene film and graphene nano dots. Both D peak and D' peak were observed for graphene nano dots. D peak

originates from a second-order Raman scattering process involving one iTO phonon and one defect, while D' peak also corresponds to another weak disorder-induced feature for a *intra-valley* process [7]. The reasons of the appearance of the two peaks are the defects and the edges effect induced by the etching process during nano dots fabrication [7-8].

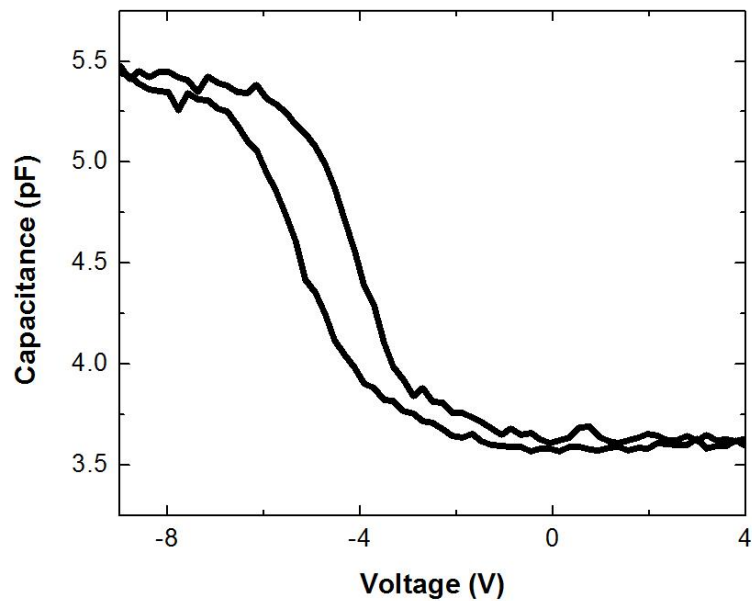


Figure 5-7 A C-V sweep of graphene nano dots memory capacitor.

The capacitance-voltage (C-V) measurement is a simple and effective way to examine the memory effect of MOS memory capacitors. This is done by a home-made Labview code using a GPIB card to communicate between a computer and an Agilent 4192 Precise LCR meter. Figure 5-7 shows a hysteresis of 1.5 V in the C-V sweep of graphene nano dots memory capacitor, indicating the memory capability of the capacitor.

During the gate voltage sweep, graphene dots are charged or discharged with electrons, which shift the flat band voltage.

5.3 Summary

Graphene nano dots were successfully fabricated by an etching process. Ni nanocrystals formed by RTA work as etch masks to protect the graphene dots area. By tuning the etching parameters, graphene dots with the size of 10 nm to 100 nm can be acquired. Raman spectrum confirms the defects and the edges effect of nano dots. A memory capacitor using a SiO₂/graphene dots/Al₂O₃ sandwich structure was fabricated. A hysteresis of 1.5 V from the C-V sweep proves the memory capability of the as-fabricated capacitor.

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Chapter 6: Conclusion

Large-area, few-layer graphene films were synthesized by thermal cracker enhanced GSMBE, and the growth mechanism was found to differ from that of CVD. The quality of as-grown graphene films was controlled by the growth time rather than the cooling rate. For nickel substrate, fast cooling in between 160 °C/min and 600 °C/min, 10 °C/min, and 5 °C/min were chosen as different cooling rates in our experiments, and no obvious difference in the coverage of single-layer and bi-layer graphene was found. With the increase of growth time, more and more carbon atoms grew on the metal surface. Therefore, it is not the different cooling rates but the growth time that manipulate the number of layers of the grown films in the GSMBE system. Large-area, few-layer graphene films were achieved at 800 °C, about 200 °C lower than the temperature used in the typical CVD method. Clear hexagonal diffraction patterns indicate the good quality of as-grown graphene film. The evolution of 2D peak and the secondary hexagonal enhanced spots indicate the mis-oriented stacking order of as-grown films. The quality of the films degrades at low growth temperatures, as proved by the occurrence of the D peak. These results suggest that graphene has been synthesized on the nickel substrate through layer-by-layer growth mode.

For cobalt substrate, the single-layer and bi-layer coverage of 93% was achieved at an optimized temperature of 950 °C. Clear TEM diffraction pattern and lacking D peak in Raman spectra indicate high quality of as-grown films. A narrow growth time window was found for different growth temperatures. Carbon atoms form as either thick graphene or porous net if the growth condition is out of this growth window. Carbon absorption

and desorption phenomena were responsible for temperature-dependent and growth time-dependent graphene morphology. Direct epitaxial growth mechanism was confirmed through temperature cooling rate and growth time dependent experiments. These studies suggest that thermal cracker GSMBE can be promising in growing large-area graphene on Co substrates.

Graphene channeled flash memory device was fabricated by standard semiconductor processes. High-density Ni nanocrystals ($\sim 1.1 \times 10^{12} \text{ cm}^{-2}$) with an average size of 7nm were formed by annealing 1 nm Ni film at high temperature. The nanocrystals work as charge reservoirs and provide the ability of data storage for the device. The measured transfer curves prove the field effect of the as-fabricated graphene channel. A big memory window of 23.1 V can be observed by the back gate voltage sweeping. By applying bipolar pulse signals of ± 20 V on the back gate as program/erase biases, the graphene memory transistor can be turned on/off. No obvious failure or performance degradation was found after programming/erasing cycles of 5×10^5 , which suggests very good endurance of the device. By measuring drain current versus time, a much better retention performance than other graphene/CNT memory devices was observed. The results suggest that nanocrystal based graphene memory is promising for future nonvolatile memory applications. A significant field effect mobility degradation ($\sim 60\%$) can be observed after the dielectric deposition on top of the graphene channel, which should be due to the scattering induced by HfO_2 films.

Graphene nano dots embeded flash memory capacitor was also demonstrated. By using Ni nanocrystals as etch masks, graphene nano dots were fabricated by O_2 plasma etch process. The occurence of D peak and D' peak in Raman measurent of graphene dots attribute to the defects and edges induced by the etch process. The memory capacitor was formed as a SiO_2 /graphene dots/ Al_2O_3 sandwich structure. By measuring the C-V sweep, a hysteresis was found, indicating that graphene dots are able to store electrons and be potentially used for memory applications.

Appendix

Publications:

[1] Layer-by-layer synthesis of large-area graphene films by thermal cracker enhanced gas source molecular beam epitaxy

Carbon, 49, 2046 (2011)

N. Zhan, M. Olmedo, G. Wang, and J. Liu

[2] Cobalt-assisted large-area epitaxial graphene growth in thermal cracker enhanced gas source molecular beam epitaxy

Applied Physics A, 105, 341 (2011)

N. Zhan, G. Wang, and J. Liu

[3] Graphene based Nickel Nanocrystal Flash Memory

Applied Physics Letters, 99, 113112 (2011)

N. Zhan, M. Olmedo, G. Wang, and J. Liu

[4] ZnO homojunction photodiodes based on Sb-doped p-type nanowire array and n-type film for ultraviolet detection

Applied Physics Letters, 98, 041107 (2011)

G. Wang, S. Chu, **N. Zhan**, Y. Lin, L. Chernyak, and J. Liu

[5] Synthesis and characterization of Ag-doped p-type ZnO nanowires

Applied Physics A, 103, 951(2011)

G. Wang, S. Chu, **N. Zhan**, H. Zhou, and J. Liu

[6] TiSi_2 nanocrystal metal oxide semiconductor field effect transistor memory

IEEE Transactions, Nanotechnology, 99 (2010)

H. Zhou, B. Li, Z. Yang, **N. Zhan**, D. Yan, R. K. Lake, and J. Liu

[7] Carbon Nanotube Memory by the Self-Assembly of Silicon Nanocrystals as Charge Storage Nodes

ACS Nano 5, 7972(2011)

M. Olmedo, C. Wang, K. Ryu, H. Zhou, J. Ren, **N Zhan**, C. Zhou, and J. Liu