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The Dependence of Electrical Properties on Miscut Orientation in Direct Bonded III-V Solar Cell Layers

A thesis submitted in partial satisfaction

of the requirements for the degree of Master of Science

in Materials Science and Engineering

By

Mark Seal

2015

# ABSTRACT OF THE THESIS

The Dependence of Electrical Properties on Miscut Orientation in Direct Bonded III-V Solar Cell Layers

By

Mark Seal

Master of Science in Materials Science and Engineering

University of California, Los Angeles 2015

Professor Mark S. Goorsky, Chair

Direct bonding is a materials integration process in which wafer substrates are directly bonded without any intermediate layers. This technique has been used to fabricate direct bonded n-GaAs//n-GaAs, n-GaAs//n-InP, and n-InP//n-InP structures comprised of combinations of on-axis substrates and substrates with (001) faces misoriented 4° toward <111> in order to study the effect of relative surface misorientation on the electrical properties of the bonded interface. Simulation and measurement of interface electrical conductivity were used to identify properties including height and shape of the potential barrier. Across all substrate combinations, as the relative surface misorientation was increased, the interface resistance and height of the interfacial potential barrier also increased. Current density – voltage measurements of GaAs//InP bonded structures revealed no band structure asymmetry at low ( ± 50 mV) bias. Transmission electron microscopy was used to observe the morphology of the interface between InP//InP and GaAs//InP structures. Consistent with previous reports, results of electrical measurements

indicate that the potential barrier height at interfaces containing at least one side InP are less sensitive to increased interface resistance with increasing misorientation.

Low temperature (≤ 600 °C) and kPa applied pressure to initiate bonding between $(NH_4S)_2$ pretreated GaAs and InP wafers was used to fabricate direct bonded structures. Wafers were bonded face-to-face on-axis, with relative misorientation of 4° or 8°, or a by bonding a combination of 4° miscut substrates bonded such that relative misorientation was zero. The samples were annealed at 400 °C for 2 hours to strengthen the bond, and then subjected to rapid thermal processing at 600 °C for 2 minutes to improve the electrical conductivity. When compared to on-axis structures, the interface resistance at room temperature for 4° misoriented bonded pairs increased from 0.011 $\Omega\cdot cm^2$ to 2.8 $\Omega\cdot cm^2$ for GaAs//GaAs structures, from 0.00824 $\Omega\cdot cm^2$ to 0.0161 $\Omega\cdot cm^2$ for GaAs//InP structures and only from 0.0063 $\Omega\cdot cm^2$ to 0.0089 $\Omega\cdot cm^2$ for InP//InP structures. The electronic behavior at the interface was modeled using the Seager-Pike theoretical model for electron tunneling between adjacent semiconductor bicrystals. In accordance with this model the zero-bias conductance was used to estimate the conduction barrier height at the bonded interface. The zero-bias conductance taken at temperatures from 90 to 340 K reveals an increase in potential barrier height across all wafer combinations as the degree of surface misorientation is increased, from 0.26 eV to 0.305 eV for InP//InP structures, from 0.32 eV to 0.39 eV for GaAs//InP structures, and from 0.54 eV to 1.0 eV for GaAs//GaAs structures.

For all material combinations studied, structures with zero relative misorientation displayed equivalent electrical performance to nominal on-axis substrates, demonstrating that relative surface misorientation rather than substrate miscut is responsible for changes in electrical resistivity. The large increase in potential barrier height for GaAs//GaAs structures indicates that

the degree of relative misorientation between GaAs//GaAs wafer bonded pairs has a significant impact on interface electrical properties, and is consistent with previous GaAs//GaAs studies. However for GaAs//InP wafer bonded pairs, the relative misorientation across the bonded interface plays a less significant role, and the impact of relative misorientation is least significant for InP/.InP bonded structures. This is illustrated by the increase in potential barrier of 0.04 eV for InP//InP structures, 0.06 eV for GaAs//InP structures, and 0.47 eV for GaAs//GaAs structures as relative misorientation is increased from 0° to 8°.

High resolution transmission electron microscopy and high-angle annular dark field are used to confirm the misorientation of GaAs//InP and InP//InP bonded samples and determine the interface morphology. No interfacial layer is present in InP//InP structures before or after rapid thermal processing. It is observed that regions adjacent to the interface undergo a process of atomic redistribution and recrystallize into the same lattice arrangement as the bulk semiconductor. GaAs//InP interfaces are observed to contain regions direct substrate contact with oxide inclusions in between after rapid thermal processing, consistent with previous work on GaAs//GaAs interfaces.

It is concluded that for III-V direct wafer bonded heterostructures, interface conductivity is a function of both the relative misorientation between the (001) surfaces and the material pair. The significance of this study is that the additional variable of lattice mismatch does not degrade electrical conductivity through GaAs//InP interfaces. This is significant for applications where heterostructure interface conduction must be controlled, such as the direct bonding of III-V wafers for photovoltaic applications.

The thesis of Mark Kristopher Seal is approved

Dwight C. Streit

Suneel Kodambaka

Mark S. Goorsky, Committee Chair

University of California, Los Angeles

2015

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# Chapter 1: Introduction

## 1.1 Introduction

Recent publications by Dimroth *et. al*[1] and Chiu *et. al*[2] that demonstrate multijunction solar devices with record efficiencies have highlighted the benefits of using cells with more than the standard three junctions. These benefits have been known for some time however cost and complications stemming from lattice mismatch during fabrication have limited the number of junctions within practical solar cells to three or fewer. These publications cite direct wafer bonding as the material integration technique used to fabricate their four and five junction cells which do not have the traditional symptoms caused by lattice mismatch in epitaxially grown cells with comparable junctions. Interestingly, neither publication give detailed surface preparation or bonding procedures, however Chiu *et. al*[2] notes that "further studies regarding bond resistance with respect to the identity and doping of the bonding layers, chemical pretreatment, and substrate miscut would be required to optimize the bond resistance."

Previous work by our group has been performed on the topic of III-V materials integration techniques including studies of surface chemical pretreatment, direct bonding parameters, and substrate miscut between GaAs and InP direct bonded structures[3-9]. Specifically, studies on the effect of substrate miscut on the electrical properties of GaAs//GaAs direct bonded interfaces were published beginning in 2012[3, 7, 8]. The work herein includes the background formed by these studies and extends to include understanding of the effect of substrate miscut on the electrical properties of InP//InP and GaAs//InP interfaces. GaAs and InP constitute the substrates for lattice matched epitaxial growth of 2 or 3 junction cells, which are subsequently directly bonded together as demonstrated in the fabrication of both 4 and 5 junction cells mentioned previously[1, 2]. Due to the complexity and large fabrication cost of multijunction

solar cells, GaAs and InP wafer substrates will be used as a simplified model for the multijunction device for this work.

This research will provide a fundamental study into the role of relative surface misorientation on band structure and electronic properties between directly bonded InP//InP and GaAs//InP structures using on-axis and 4° misoriented substrates. This will form the guide for future work in which layers lattice matched to GaAs and InP are epitaxially grown on miscut substrates and then directly bonded together in order to align research with practical fabrication of multijunction solar cells.

At the interface between the two bonded layers, a discontinuous interface is generated, and acts as a grain boundary containing interfacial charge states, leading to the formation of a double depletion region and a potential energy barrier to conduction[10]. For multijunction solar devices, overall efficiency is limited by the least conductive component, which is the direct bonded interface. It is therefore critical to decrease this potential barrier to conduction in order to increase overall device performance. Previous work has shown that the surfaces of these layers can be passivated with sulfur prior to hydrophilic direct bonding in order to reduce the density of interface charge states that form after bonding[11]. The presence of unfavorable native oxides that are mechanically difficult to remove and would result in a non-ohmic bond between wafers can be replaced by sulfur that is chemisorbed in the top 2-5 Å of the surface[4, 12, 13].

This method of direct wafer bonding for multijunction integration is under investigation in this thesis, which allows two lattice mismatched materials to be bonded directly via secondary van der Waals forces without any induced strain[14]. While previous work has shown the effect of off-axis substrates on linear transconductance in direct wafer bonded GaAs structures[3, 8], the effect of off-axis substrates in other III-V material combinations has not been investigated. The

purpose of this research is to investigate the effect of miscut substrates on the electrical conductivity across InP and GaAs direct bonded wafers with on-axis and miscut substrates to generate structures with a range of misorientations, and to examine the role of relative surface misorientation on conductivity.

## 1.2 Organization

The background and theory of wafer bonding including off-axis substrates commonly used in the solar industry, characterization techniques such as transmission electron microscopy, atomic force microscopy, and electrical measurements are discussed in Chapter 2. Chapter 3 outlines the experimental methods and equipment used. Chapter 4 provides analysis of electrical properties and interface morphology for wafer bonded GaAs//GaAs, InP//InP, and InP/GaAs structures. Chapter 5 includes a summary and conclusion of the research.

# Chapter 2: Background and Theory

## 2.1 Wafer Bonding

The dependence of friction on surface roughness has long been a topic of study, first mentioned by Desaguiliers in 1734[15] who noted a decrease in the friction between two solids as the roughness of their surfaces was decreased. Desaguiilier's observation holds true until a specific point for every solid material, at which the friction increases as the roughness is decreased due to bonding between the surfaces. This phenomenon has been applied to great effect in the semiconductor industry starting with silicon wafers in the 1960's[16] and more recently for III-V materials integration[17]. Today wafer bonding is used in the commercial manufacturing of devices for micro-electro-mechanical systems (MEMS) and silicon-on-insulator (SOI) devices.

The process of wafer bonding can be classified as either hydrophobic or hydrophilic, depending on the surface conditioning techniques prior to bonding. For SOI and MEMS applications, direct bonding has been well-studied and serves as the foundation for which most material pairs, including III-V systems, are understood. Hydrophobic bonding is achieved by creating a non-polar surface by etching the surface oxide with a strong acid. This creates a non-polar surface which does not form strong bonds with polar water molecules. For hydrophilic bonding, a surface terminated by polar oxide or hydroxide species is formed by either reaction with oxidizing species such as air or an additional reaction on the surface. This polar surface creates strong hydrogen bonds with water molecules. The characterization of a surface as hydrophobic or hydrophilic can be performed by measuring the equilibrium contact angle between the water molecules on the surface. Hydrophobic surfaces have a tendency to form more spherically shaped water droplets each with a large contact angle. Hydrophilic surfaces tend to

form a ‘wetted’ surface, containing drops with a hemispherical shape and subsequent low contact angles.

Creating a hydrophilic or hydrophobic surface is a key step in successful wafer bonding. For the application of multijunction III-V solar cells, overall conversion efficiency is limited by the least conductive element in the solar cell structure. Therefore large areas of well bonded interface with low resistance between the layers in the bonded structures are a necessity while maintaining low optical absorption. Consequently a surface containing of a layer of non-conductive oxide or an additional insulating layer containing hydroxide must be minimized, and a hydrophobic bonding treatment is the appropriate choice for surface treatment for the work herein.

However for both hydrophobic and hydrophilic wafer bonding techniques, achieving a low surface roughness prior to bonding is a requirement. The root-mean-square (RMS) deviation of the surface about the mean height is the standard method for measuring roughness for wafer bonding, and can be achieved by atomic force microscopy (AFM). A typical value for RMS roughness appropriate for wafer bonding is 1 nm[14]. A low RMS roughness ensures proper wafer to wafer contact on a local scale, however additional values typically used in the semiconductor industry to describe wafer shape such as total thickness variation and surface curvature must be minimized to promote the maximum of wafer to wafer contact area.

For hydrophobic bonding, initial adhesion between the two surfaces is achieved through secondary van der Waals forces between the surface molecules. For hydrophilic bonding, initial adhesion is achieved through hydrogen bonding between surface molecules. These forces are too weak for use in device fabrication and therefore thermal processing is used to strengthen this bond. Elevated temperatures and in some cases pressures are used to provide the energy

necessary to convert the van der Waals or hydrogen bonds into strong covalent bonds. In this work, hydrophobic surfaces are created by treatment with $(NH_4)_2S$.

Because wafer bonding is typically used to integrate different materials, differences in the coefficient of thermal expansion between materials places a limit on the amount of thermal processing available in the wafer bonding process. The large mechanical stress that will be created by the different rates of expansion between the materials involved in the bonded interface can create cracks or damage to the bonded interface which degrade electrical performance. An additional limitation is the thermal budget for dopant profiles in the wafers. Due to the complicated designs in many devices common in consumer electronics such as complementary metal-oxide semiconductor integrated circuits, elevating the device temperature for long periods of time to promote successful wafer bonding would cause over-diffusion of dopant species and degrade device performance.

To avoid issues created by long annealing times, wafer fusion is a technique wherein pressure is applied to the wafers during the heating process in order to disrupt the interfacial layer and promote direct contact between semiconductor layers. The pressures used in this technique are typically in the MPa range[18] and structures fabricated with this technique often exhibit bond failure or a large density of voids at the interface. Due the mechanically weaker properties of III-V materials when compared to Si and the thin structures necessary for the optoelectronic applications that the materials presented in this thesis are intended, only kPa pressure was applied to initiate bonding, and no compressive force was applied during subsequent processing. This low pressure and thermal budget bonding technique could be applied to wafer bonding processes where thicker (and therefore mechanically stronger) III-V materials are acceptable.

Despite efforts to create hydrophobic surfaces between III-V wafers prior to bonding, there is often a 5-10 nm layer of amorphous oxide at the bonded interface[19]. This oxide layer contributes to the interface resistance that must be minimized for optoelectronic applications. Annealing at temperatures around 600 °C for short (~30 min) has been shown to disrupt this continuous oxide layer into regions containing direct semiconductor to semiconductor contact, with improved interface resistance[19]. Additional surface activation to increase the overall surface energy has been shown to reduce the thickness of the amorphous oxide layer post thermal processing. Previous work has shown that for III-V wafer bonding, the cleaned surface can be reacted with a sulfur species which replaces the oxygen bonds at the surface oxide layer[5, 9]. After annealing at 400°C for 2 hours and 600 °C for 2 minutes, the continuous oxide layer present in both sulfidized and unsulfidized samples has rearranged to form regions of good contact between the wafers, however only sulfidized samples displayed a reduced interface resistance[5] to below 0.01 ohm·cm$^2$. This technique allows for thermal annealing at significantly lower times and therefore impact on the thermal budget.

## 2.2 Surface Misorientation

### Out-Of-Plane Relative Surface Misorientation

On-axis and miscut (001) n-GaAs and n-InP wafers are used for these wafer bonded structures. Figure 1 shows the different orientations between the wafer faces post bonding that were used to create structures with relative miscut of 0°, 4°, and 8°. On-axis samples were fabricated according to (a) in Figure 1.  A non-zero relative surface misorientation was created by positioning the faces face-to-face prior to bonding such that the (001) planes on either side of

the bonded interface are divergent, as shown in (b) and (c) of Figure 1. The total out-of-plane relative misorientation is the sum of each substrate's individual miscut angles. Off-axis substrates can be bonded such that there is zero relative misorientation between the planes as shown in (d) of Figure 1 by positioning the surfaces face-to-face such that the (001) planes on adjacent sides of the interface are parallel to each other. This is achieved by rotating either the top or bottom substrate in (c) of Figure1 by 180° around the axis perpendicular to the surface prior to bonding.

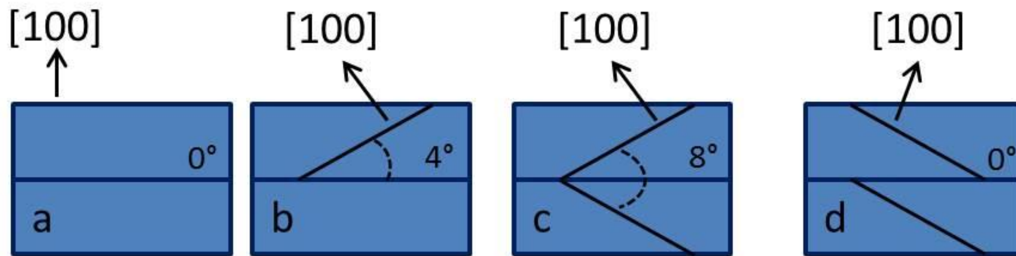


**Figure 1. Diagram of the various types of bonded samples: (a) zero relative surface misorientation with on-axis substrates, (b) 4° relative surface misorientation with one offcut substrate, (c) 8° relative surface misorientation with two offcut substrates, and (d) zero relative surface misorientation with offcut substrates.**

### In-Plane Rotational Misorientation

Imperfect wafer cleaving and bonding can lead to a non-zero in plane rotation misorientation parallel to the bonded interface shown in Figure 2[8]. The effect of in-plane misorientation on direct bonded III-V material systems similar to those in this work (GaAs//InP, GaP//InGaP, GaP//GaP) has been reported[20- 22] with results indicating that differences in direct bonding procedure and material system determine the impact of in-plane misorientation on

electrical properties. During the bonding procedure wafers were aligned in order to minimize the rotational misorientation; however in this study the in-plane misorientation was not considered as a variable and is discussed in more detail in section 5.

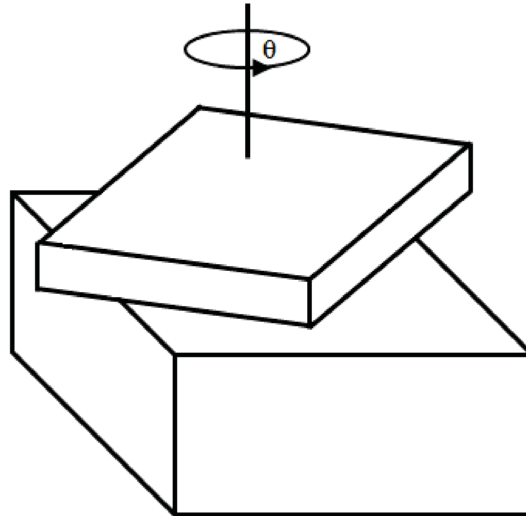


**Figure 2. Diagram of in-plane rotational misorientation, Θ reproduced from [8].**

### 2.3 Interface Electrical Properties

The discontinuous nature of an interface between the two semiconductor surfaces can be treated as a grain boundary. Semiconductor grain boundaries introduce broken bonds which affect the local energy band structure and can significantly impact the mechanical and electrical properties of devices in these regions. For this reason, in many of the optoelectronic applications for semiconducting materials it is desirable to use single crystal substrates. During integration of the single crystal substrates into wafer bonded structures, a discontinuous interface between the bonded substrates is created. This interface creates charge states, leading to the formation of a

carrier traps at mid-gap energy levels. These interfacial charge states create an accumulation of charge at the interface, which leave behind immobile ionized dopants and a depletion of majority charge carriers on either side of the interface. For direct bonded n-type semiconductors, a double Schottky-like junction is formed and described by a potential energy barrier $\phi_{BO}$ to ohmic conduction[10] as shown in Figure 3, where $E_{CBM}$ is the energy of the conduction band, ξ is the energy from the Fermi level to the conduction band edge, $E_g$ is the energy of the band gap, $E_{VBM}$ is the energy of the valance band, and Z is the distance from the interface[9].

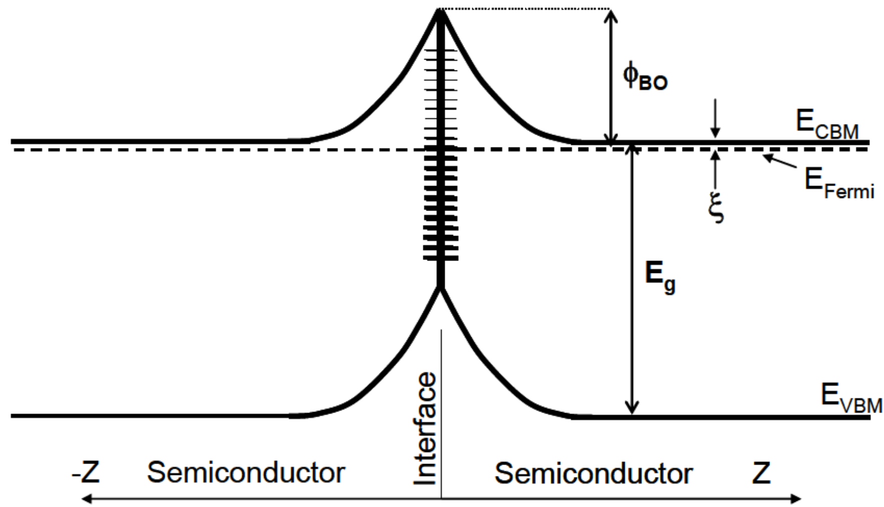


**Figure 3. Band structure for n-type homojunction containing interface states. Reproduced from [9].**

This barrier can be surmounted by a combination of mechanisms: (i) thermionic emission electrons over a potential barrier characterized by an Arrhenius relationship with respect to temperature. (ii) quantum mechanical electron tunneling through the potential barrier, (iii) diffusion of majority carriers in the depletion region formed by the interface. For cases when

electron transport over the barrier is dominated by the thermionic emission mechanism it will exhibit current-voltage behavior according to Equation 4[23]

$$J(V) = A_R T^2 \cdot exp\left[\frac{-(\phi_{BO} + \xi)}{kT}\right]\left[\exp\left(\frac{eV}{kT}\right) - 1\right] \tag{4}$$

Where $A_R$ is the Richardson constant of the semiconductor, $\phi_{BO}$ is the conduction band barrier height, and $\xi$ is the energy from the Fermi level to the conduction band edge. This mechanism is responsible for the majority of the current associated with transport in semiconductors doped in $10^{15}$-$10^{16}$cm$^{-3}$ range, where grain boundary barriers are too large for substantial tunneling current[10].

For n-type semiconductors doped at the $10^{17}$- $10^{18}$ cm$^{-3}$ level, grain boundary barriers are narrow enough to permit substantial electron tunneling. Seager and Pike proposed a theoretical model for the zero-bias conductance across semiconductor bicrystals doped in the $10^{17}$-$10^{18}$ cm$^{-3}$ range[5, 10, 24] which is used to quantify the potential barrier height formed at the bonded interface by measuring current-voltage performance across a range of temperatures and fit to the model in Equation 5.

$$\frac{G_0}{T} = \frac{qA_R}{k_b^2 T} \cdot \int_0^{\phi_{BO}} \frac{e^{-\frac{2}{E_0}\left[\sqrt{\left(\phi_{BO}\cdot(\phi_{BO}-E)\right)}-E\cdot ln\left\{\frac{\sqrt{\phi_{BO}}+\sqrt{(\phi_{BO}-E)}}{\sqrt{E}}\right\}\right]}}{1+e^{\left[\frac{(E+\xi)}{k_b T}\right]}}\, dE \tag{5}$$

$G_0$ is the zero-bias interface conductance ($\Omega^{-1}\cdot$cm$^{-2}$), $A_R$ is the Richardson constant for the appropriate semiconductor, $\phi_{BO}$ is the conduction barrier height, $\xi$ is the Fermi energy level relative to the conduction band edge, $T$ is the temperature, $q$ is the charge of an electron, $k_b$ is the Boltzmann constant, and $E_0$ is a reference energy defined by Equation 6 as:

$$E_0 = \sqrt{\frac{\hbar^2 q^2 N_D}{4 m_t \varepsilon_r \varepsilon_0}} \quad (6)$$

Where $N_D$ is the doping concentration, $m_t$ is the electron tunneling effective mass for the appropriate semiconductor, ħ is the reduced Plank constant, $\varepsilon_0$ is the permittivity of free space, and $\varepsilon_r$ is the dielectric constant. In order to achieve reasonable fitting between the experimental n-type GaAs and InP structures synthesized in these experiments $\phi_{BO}$, is adjusted and the $A_R$ and $E_0$ parameters are scaled by individual pre-factors.

This potential barrier has been shown to be lowered by reducing the density of interface states[3, 5, 9, 25] as demonstrated in Figure 4 through two mechanisms: (i) surface passivation of substrates prior to bonding and (ii) thermal processing post bonding.

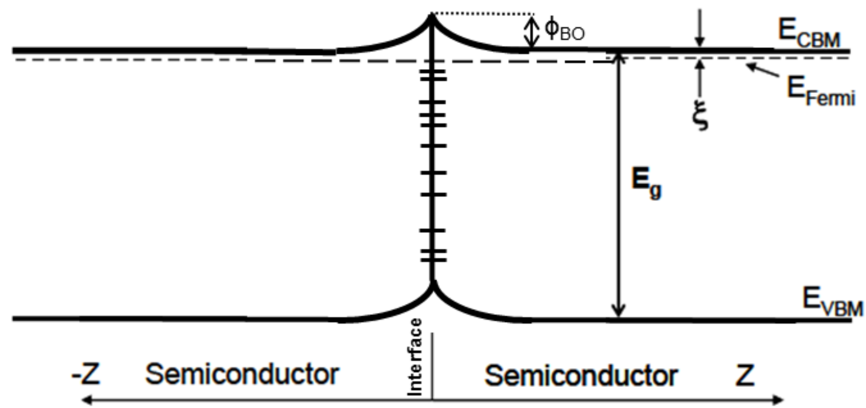


**Figure 4. Band structure for n-type homojunction containing interface states, showing a reduction of potential energy barrier due to surface passivation and thermal treatments.**

## 2.4 Interface Resistance

Interface resistance was calculated by the inverse slope of current density as a function of voltage for the various GaAs and InP combinations at a maximum range of ± 1V. Equipment limits of 1A current restricted the range of voltages available for testing for highly conductive InP//InP samples to ± 0.1V. These measurements were taken to inspect for any non-ohmic behavior that could be attributed to the interface. The interface resistance, $R_{INT}$ is separated out of the total measured resistance $R_{TOT}$, which includes the system resistance, $R_{SYS}$, the contact resistance $R_{CON}$, and the bulk semiconductor resistance $R_{SEMI}$ as appropriate for GaAs or InP as shown in Figure 5[8].

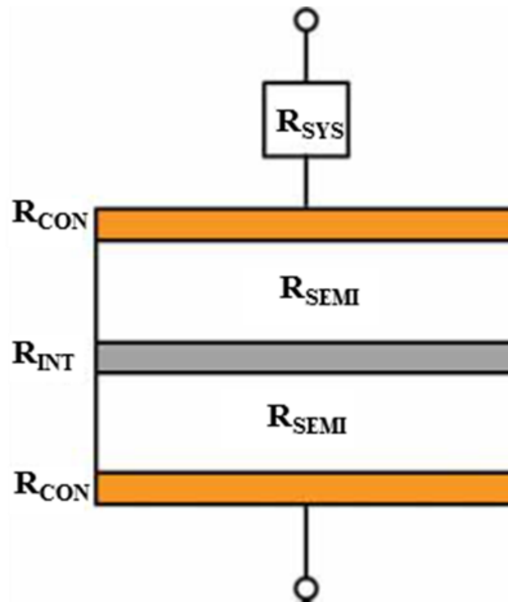


**Figure 5. Diagram of bonded semiconductor structure with all components to total resistance. Reproduced from [8].**

Because $R_{TOT}$ can be treated as a sum of the separate components in series, the interface resistance is separated according to Equation 7[8].

$$R_{INT} = R_{TOT} - (2 \cdot R_{SEMI} + 2 \cdot R_{CON} + R_{SYS}) \qquad (7)$$

Reference on-axis (001) GaAs and InP with equivalent doping concentrations and subjected to the same metal contact deposition and thermal processing treatments as the bonded samples were used to estimate the $(2 \cdot R_{SEMI} + 2 \cdot R_{CON} + R_{SYS})$ quantity. The zero-bias conductance is calculated from the inverse of the $R_{INT}$ taken from a $\pm$ 50 mV range about zero bias at temperatures down to 90 °K.

### 2.5 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is a characterization technique that is required to obtain the necessary resolution for observation of the bonded interface morphology. The microscope uses a field emission gun to produce electrons with small angular divergence and a narrow energy range. This electron beam is passed through a condenser system which is used to adjust the beam before it reaches the sample. This system consists of a series of magnetic lenses and apertures. The lenses control the diameter of the electron beam as it is focused on the sample, while the apertures are located between the lenses and are used to control the convergence angle of the beam. In this way, the condenser system can control both the beam diameter (spot size) and intensity. The beam is passed through the sample, which should be sufficiently thin for electron transparency (typically 100 nm or less). The sample stage controls the position of the sample and can be moved in X, Y, or Z directions as well as tilted to achieve the desired alignment. After passing though the sample the electron beam then passes through

the objective and intermediate lenses which can focus the beam to form a magnified image or a diffraction pattern. The image is then passed through the projector lens which projects the final image onto a phosphor viewing screen, photographic film, or charge coupled device screen for display.

Standard TEM images can be generally described showing regions and features with bright and dark features. This contrast can be used to discern the shape and morphology of the specimen, but also the structure. Primary electrons that are transmitted through the sample are affected by both elastic and inelastic scattering. This gives rise to the mass-thickness contrast, where regions that are thick or dense will more effectively scatter the transmitted electrons, causing dark features to appear in the image. Conversely, thin or less dense regions will not scatter electrons as effectively and will therefore appear brighter. However it is not enough to state that scattering occurs only by the mass-thickness contrast. Since the de Broglie wavelength of electrons is much smaller (~$10^{-2}$ Å at 300 kV)[26] than the distances between atoms (~ 1 Å) in this work, much of the scattering (and resulting contrast) results from diffraction of electrons by the periodic nature of a crystal. Particular angles based on the crystal orientation and electron energy will split the incident beam into (i) a transmitted beam that passes through the sample, and (ii) many diffracted beams, as depicted in Figure 6[9].

Beyond the basic TEM images, high resolution TEM (HRTEM) can resolve atomic planes. The sample is first aligned to a major zone axis in order to obtain several reciprocal lattice points of similar intensity, and then a composite image is formed by combining all of the diffracted beams together. Several strongly diffracting beams pass through the optical aperture and interfere with each other, and the outcome of this interaction is a phase contrast mechanism, in which each diffracting beam contributes a pattern of light and dark fringes to the composite

image. These fringes overlap and form a series of bright and dark spots that correspond to individual lines of atoms.

To probe larger regions of the sample, scanning TEM (STEM) is used to raster the electron beam across the sample. The magnetic lenses that focus the beam in the condenser system vary their voltages to move the beam across the sample, while the detector collects intensity information. An overall image is constructed by combining the detected intensity as a function of beam position. An additional feature on some STEM setups is high-angle annular dark field (HAADF), in which the camera length is reduced so that the detector accepts electrons scattered through a much wider angle. The resulting diffraction contrast is reduced in favor of atomic number contrast, allowing one to distinguish between features of different atomic number. This is particularly useful for interfaces where an oxide may be present.

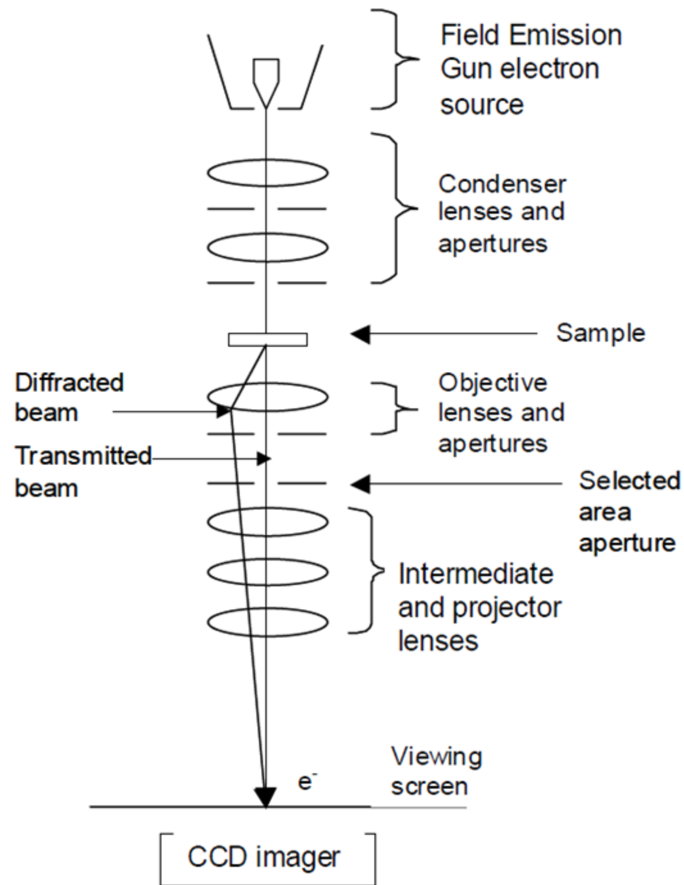


**Figure 6. Illustration of Transmission Electron Microscope showing main constituents. Reproduced from [9].**

## 2.6 Atomic Force Microscopy

AFM is a technique commonly used for measuring surface roughness that can achieve sub-nanometer resolution. A probe tip with a radius of curvature on the order of 1 nm at the end of a cantilever is brought close to a sample surface such that the van der Waals electrostatic forces between the sample surface and probe tip deflect the cantilever. A laser focused on the cantilever and reflected into a detector is used to monitor the vertical deflection of the cantilever as the laser reflection angle is changed. Prior to wafer bonding, 40x40 $\mu m^2$ scans are taken of the polished surface to measure surface roughness and check for contaminating particles. Sufficient

cleaning and polishing to reduce RMS roughness < 1 nm is necessary, as surface particulates create voids at the bonded interface; these voids lower mechanical strength and degrade electrical properties. A benefit of this technique to measure surface roughness is that it is not limited by the space resolution due to the diffraction limit typically encountered by optical microscopy. Additionally, samples do not need to be observed under vacuum as in electron microscopy. To reduce the risk of the tip colliding with the surface and causing damage, a feedback mechanism is employed to adjust the top-to-sample distance to maintain a constant force between the tip and the sample.

### 2.7 Electronic Materials Group

Materials integration techniques for III-V materials have been studied for some time by our group and others. Beginning in 2010, publications from our electronic materials group detailing surface and thermal treatments of GaAs//GaAs, InP//InP, and GaAs//InP direct bonded structures demonstrated that sulfur passivation is effective at minimizing oxide incorporation at the interface and modifies the way the interfaces with thermal treatments similar to those used in this work (400 °C for 2 hours, 550°C for 1 minute) of the interface during annealing[6, 9].

Further studies of a low temperature (≤ 600 °C) and low applied force (kPa) to initiate bonding between GaAs//GaAs and InP//InP direct bonded wafers including a dry sulfidization step were subsequently performed[4, 8]. This led to large bonding areas (~ 50 $cm^2$), with bulk fracture strength achieved after annealing GaAs//GaAs at 400 °C and InP//InP at 300 °C for times between 2 and 12 hours. Examination of the bonding surface revealed that sulfide is

present at the interface and that the oxide components show a reduced concentration when compared to samples that were treated with only an oxide etch solution.

Additional studies of surface treatments incorporating a wet sulfidization step via ammonium sulfide demonstrated equivalent results with the dry sulfidization step for GaAs//GaAs direct bonded structures, and both sulfur techniques displayed an improvement over samples treated with only an oxide etch solution[5]. Changes in the interface morphology were observed for all three treatments after thermal treatments (400 °C for 2 hours, 500-600 °C for 1-2 minutes), revealing a microstructure rearrangement from a continuous amorphous oxide layer into spherical shaped "blobs". J-V and zero-bias measurements were used to quantify the interface resistance and band structure, revealing a reduction in the interface potential energy barrier and resistance for sulfur treated specimens after thermal processing compared to those that were treated with only an oxide etch solution.

GaAs//GaAs structures with miscut substrates and treated with similar thermal (400 °C for 2 hours, 600 °C for 2 minutes) and surface treatments (ammonium sulfide) were subsequently studied and compared to on-axis specimens[3,7, 8]. This demonstrated that increases in relative misorientation between the (001) planes caused a corresponding increase in potential barrier height and interface resistance. Specifically, an increase of 8° caused an increase in interface resistance from 0.01 ohm·cm$^2$ to 3.4 ohm·cm$^2$.

# Chapter 3: Experimental Procedure

## 3.1 Wafer Bonding

Epitaxy-ready 50 mm Si-doped (001) n-type GaAs and S-doped (001) n-type InP substrates from AXT LLC were used for all experiments. Wafers with offcut angles of 4° towards <111>A, as well as nominal on-axis substrates, were selected. Specifically, on-axis GaAs wafers with doping level $2.5 \times 10^{18}$ cm$^{-3}$, 4° miscut GaAs wafers with doping level $2.9 \times 10^{18}$ cm$^{-3}$, on-axis InP wafers with doping level $4.1 \times 10^{18}$ cm$^{-3}$, and 4° miscut InP wafers with doping level $1.6 \times 10^{18}$ cm$^{-3}$ were used. Table 1 details the bonding combinations if the GaAs//GaAs, GaAs//InP, and InP//InP wafers and resulting relative surface misorientation.

**Table 1**

**GaAs//GaAs , GaAs//InP, and InP//InP bonding combinations**

| Wafer1//Wafer2 | Relative Misorientation (°) |
|---|---|
| GaAs//GaAs | 0 (On-Axis) |
| | 4 |
| | 8 |
| | 0 |
| GaAs//InP | 0 (On-Axis) |
| | 4 (GaAs On-Axis) |
| | 4 (InP On-Axis) |
| | 8 |
| | 0 |
| InP//InP | 0 (On-Axis) |
| | 4 |
| | 8 |
| | 0 |

The surface roughness of the samples was measured before bonding with a Quesant Q-Scope 250 AFM to verify that the RMS roughness was below the 1 nm required for wafer bonding. The wafers were first exposed to an $O_2$ plasma (350 W) for 2 minutes. The native oxide was removed by etching the samples immersed in a dilute 1:9 $NH_4OH:H_2O$ solution for 5 minutes, followed by a 1:9 $HCl:H_2O$ solution (HCl step only for GaAs) for 5 minutes. The surface was passivated by soaking in a 20% aqueous $(NH_4)_2S$ solution at room temperature for 5 minutes, then rinsed in deionized water and dried under $N_2$. Wetting angles were not measured quantitatively, however a noticeable increase in the number and "spherical-ness" of water droplets was observed by eye after surface treatment with ammonium sulfide $(NH_4)_2S$.

The samples were brought face-to-face and manual pressure (kPa pressure) was applied at the center to allow the bonding front to develop towards the periphery. The bonded wafers were annealed at 400 °C for 2 hr with a 3 °C/min ramp rate up and down in order to strengthen the bond. Transmission infrared images were taken after bonding and after annealing in order to monitor the bonded areas and determine the presence of any interfacial voids. Subsequent annealing did not cause the existing voids to significantly expand/contract or new voids to develop.

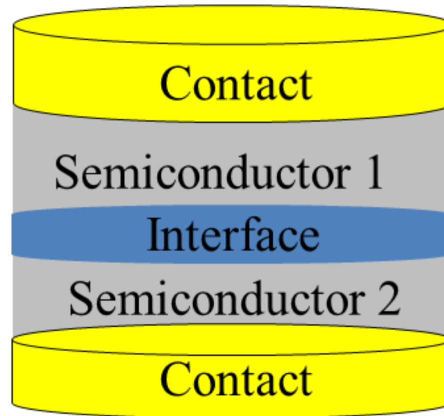


**Figure 7. Cross-section diagram of bonded semiconductor structure.**

The samples were prepared for electrical measurements by depositing metal contacts made of 2000 Å of AuGe, 400 Å of Ni, 1000 Å of Au on both sides of the bonded pairs by electron beam evaporation and alloyed at 400 °C for 2 min under $N_2$. A diagram of the bonded structure is shown in Figure 7. Samples were diced into 2x2 $mm^2$ die using a DISCO 321 saw dicing machine and then subjected to rapid thermal processing (RTP) at 600 °C for 2 min, in accordance with previous publications that reported on improved conductance across bonded layers due to a reduction in amorphous interfacial regions[27]. Reference samples were also fabricated by depositing the same front and back contacts on single on-axis (001) wafers of similar carrier concentration and exposed to the same annealing conditions. The reference was used to eliminate the resistance contributed by the metal contacts, instrumentation and semiconductor material not associated with the bonded interface from the conductance calculations.

### 3.2 Current-Voltage Measurements at Room Temperature

Current-voltage measurements were performed both before and after 600 °C rapid thermal processing with a Keithley 2400 digital source meter under computer control. The resistance from the bonded interface was calculated by subtracting out the resistance from the system, contacts, and 2x2 $mm^2$ reference GaAs or InP wafers as explained in section 2.4. The slope of the I-V curve was used to calculate the interface resistance

### 3.3 Zero-Bias Conductance

A Linkam THM S600 thermal microprobe stage with liquid $N_2$ source was used to control the chamber temperature, and I-V curves were acquired at 20 K intervals between 90 K and 340 K. The slope of the I-V curve at ± 50 mV was used to find the conductance, which was divided by temperature and plotted against inverse temperature in order to fit the data to the Seager-Pike theoretical model. Parameters including potential barrier height, doping levels, and appropriate constants were adjusted to achieve good agreement between the theoretical model and measured data.

### 3.4 Interface Morphology and Composition

TEM samples were prepared by milling with a focused ion beam (FIB) on FEI NOVA 600 FIB to extract cross-sections that included the interface from the bonded and diced 2x2 $mm^2$ structures. Once the samples had been thinned to electron transparency, a FEI TITAN S/TEM with an accelerating voltage of 300 kV was used to image the interface. The camera length was

shortened in HAADF/STEM mode for better Z-contrast and all samples were aligned to the [110] zone axis for HRTEM.

# Chapter 4: Data and Discussion

## 4.1 Infrared and Optical Measurements

An example of a transmission infrared (IR) image overlaid with the optical image of diced wafer is shown in Figure 8. It is observed that regions with voids found in IR imaging were mechanically weaker and more likely to debond during dicing or performed poorly electrically when compared to die without voids present. Comparison of electrical properties between bonded wafer orientations is in reference to 2x2 $mm^2$ die that were bonded away from the non-bonded regions along the interface due to voids or edge effects, and therefore displayed the lowest interface resistances. For all bonding combinations, the ratio of bonded area to unbonded area was always greater than 71% and typically 87%, as measured by IR camera.

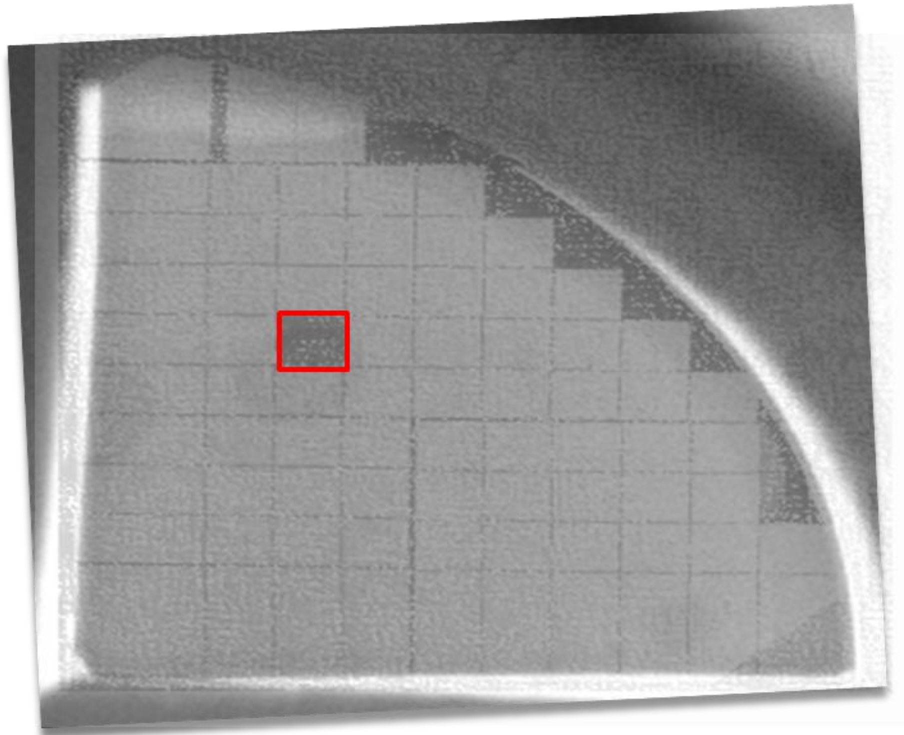

**Figure 8. Overlay of IR and optical image of bonded InP//InP quarter wafers diced into 2x2 $mm^2$ samples. Die highlighted in red debonded during dicing.**

### 4.2 Electrical Measurements at room temperature

Electrical measurements were taken at room temperature to examine the interface resistance, as outlined in section 2.4. On-axis samples exhibited superior conductivity compared to those with miscut substrates and non-zero relative surface misorientation. Table 2 gives the resistance values for the components of the bonded wafer structures after 600 °C RTP. Our observations indicate that InP//InP bonded structures exhibited categorically lower interface resistances than GaAs//InP, and GaAs//GaAs, with GaAs//GaAs structures exhibiting the largest values for interface resistances.

A large number of 2x2 $mm^2$ die were generated during the dicing process (35-75 per bonded combination) and electrical performance varied among dice taken from the same substrate combination. The range of interface resistance for the 10 most conductive dice for a given substrate combination were used to generate the values in Table 2 which are displayed graphically as range bars in Figures 9, 10, and 11. The range bars are overlaid with the data for the most conductive die for a given substrate combination. Noise observed in interface resistance measurements is expressed as uncertainty in Table 2, and is caused by changes in contact and equipment resistance. Uncertainty values were never more than 8% of the measured interface resistance, and more normally less than 3.5%. The most conductive die for each substrate combination was then used for the zero-bias measurement in Figures 14, 15, and 17.

**Table 2. Interface resistances for GaAs//GaAs , GaAs//InP, and InP//InP bonding combinations after 600 °C RTP for 2 min.**

| Wafer1//Wafer2 | Relative Misorientation (°) | Interface Resistance ($\Omega\cdot cm^2$) | Range of top 10 most conductive dice per sample ($\Omega\cdot cm^2$) |
|---|---|---|---|
| GaAs//GaAs | 0 (On-Axis) | 0.0110 ± 0.0003 | 0.0110-0.0120 (± 0.0003) |
| | 4 | 0.0210 ± 0.0007 | 0.0210-0.0224 (± 0.0007) |
| | 8 | 2.8 ± 0.22 | 2.8-3.1 (± 0.22) |
| | 0 | 0.0123 ± 0.0003 | 0.0123-0.0133 (± 0.0003) |
| InP//InP | 0 (On-Axis) | 0.0063 ± 0.0002 | 0.0063-0.0068 (± 0.0002) |
| | 4 | 0.0089 ± 0.0002 | 0.0089-0.0094 (± 0.0002) |
| | 8 | 0.0073 ± 0.0003 | 0.0073-0.0078 (± 0.0003) |
| | 0 | 0.0085 ± 0.0002 | 0.0085-0.0091 (± 0.0002) |
| GaAs//InP | 0 (On-Axis) | 0.0082 ± 0.0002 | 0.0082-0.0091 (± 0.0002) |
| | 4 (GaAs On-Axis) | 0.0153 ± 0.0006 | 0.0153-0.0165 (± 0.0006) |
| | 4 (InP On-Axis) | 0.0160 ± 0.0006 | 0.0160-0.0175 (± 0.0006) |
| | 8 | 0.0173 ± 0.0006 | 0.0173-0.0189 (± 0.0006) |
| | 0 | 0.0120 ± 0.0004 | 0.0120-0.0129 (± 0.0004) |

The J-V performance of the bonded structures reveals an increase in interface resistance as the degree of relative surface misorientation is increased for all wafer bonded combinations, as shown in Figures 9, 10, and 11. Comparing the GaAs//GaAs samples with 8° of misorientation to the on-axis structures, an increase in interface resistance by 2 orders of magnitude (from 0.011 $\Omega\cdot cm^2$ to 2.8 $\Omega\cdot cm^2$) is observed along with a display of non-linear behavior. This is consistent with previous work[3, 8, 21] that report an increase in interface resistances at comparable misorientations.

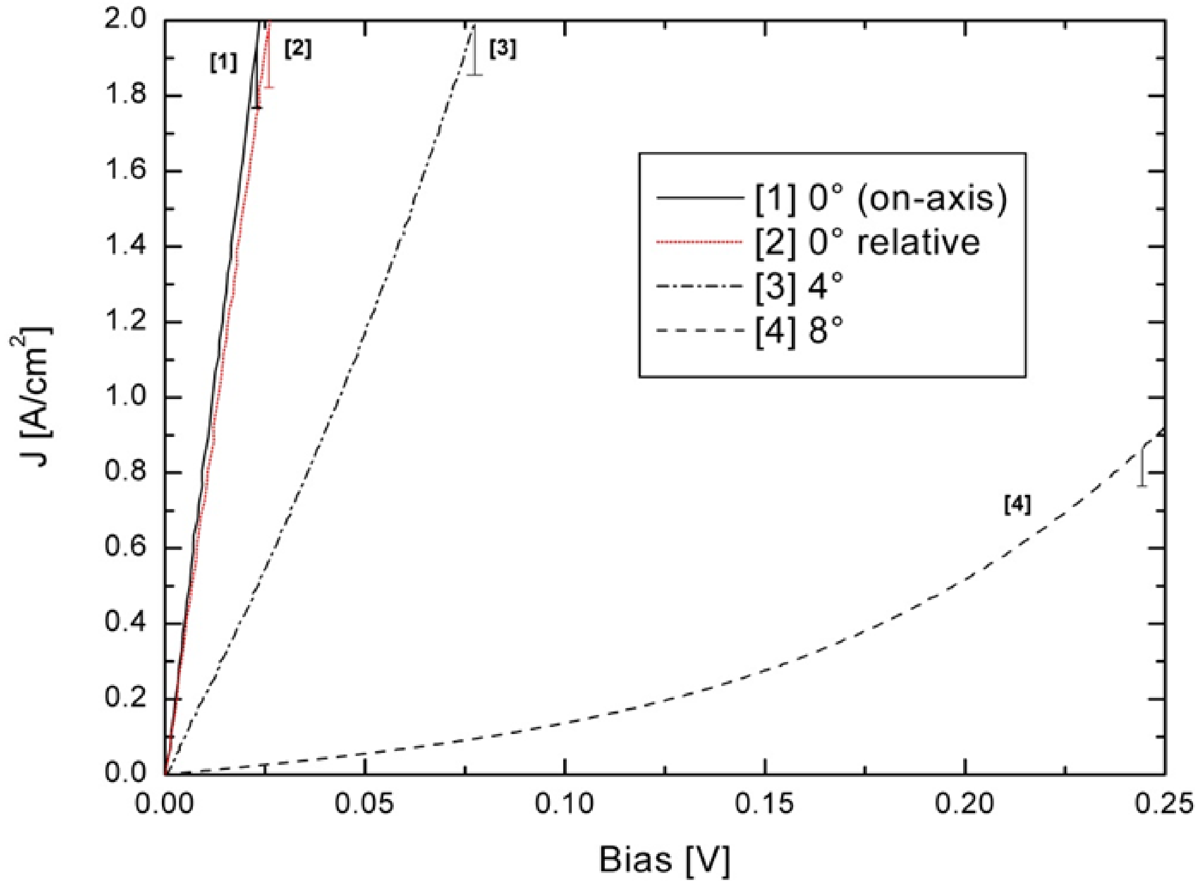


**Figure 9. Current-density vs voltage for 2x2 mm$^2$ GaAs//GaAs structures after 2-min RTP at 600 °C with AuGe/Ni/Au contacts on front and back for various relative surface misorientations.**

J-V performance of InP//InP structures is shown in Figure 10. InP//InP exhibited the lowest interface resistances, from 0.0063 Ω·cm$^2$ for on axis structures to 0.0089 Ω·cm$^2$ for structures misoriented 4°. Interestingly, the interface resistance for InP//InP samples with 4° of misorientation had the highest values for interface resistance. Additionally the interface resistance for the 0° relative misoriented InP//InP samples were 35% higher than the 0° on-axis sample (0.0063 vs 0.0085 Ω·cm$^2$). A possible explanation is that the in-plane twist component was greater for the InP//InP 4° and 0° relative misoriented samples and contributed to higher interface resistance. This is discussed in further detail in section 5.1.

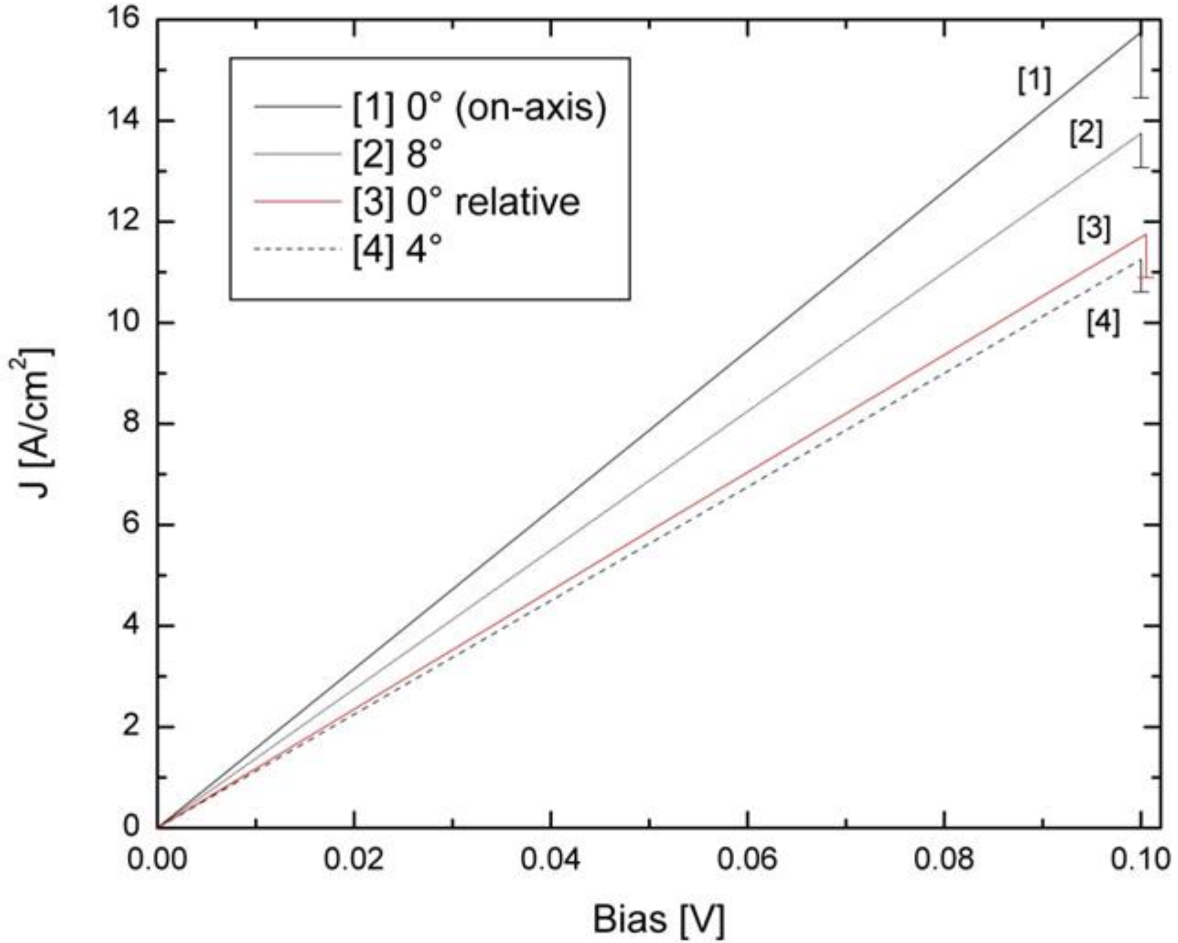


**Figure 10. Current-density vs voltage for 2x2 mm$^2$ InP//InP structures after 2-min RTP at 600 °C with AuGe/Ni/Au contacts on front and back for various relative surface misorientations.**

J-V performance for GaAs//InP structures is shown in Figure 11. Interface resistances were intermediate between GaAs//GaAs and InP//InP and increased from 0.0082 to 0.017 Ω·cm2 between on-axis and 8° misoriented samples. Unlike InP//InP structures, the interface resistance consistently increased as the relative out-of-plane misorientation increased. J-V curves remained linear across the range of misorientations studied, and the interface resistance essentially doubled as the relative misorientation was increased to 8°. This is much less than the two order of magnitude increase in interface resistance observed in GaAs//GaAs structures with comparable

misorientations. This is consistent with a higher tolerance for relative misorientation between interfaces with at least one side being InP.

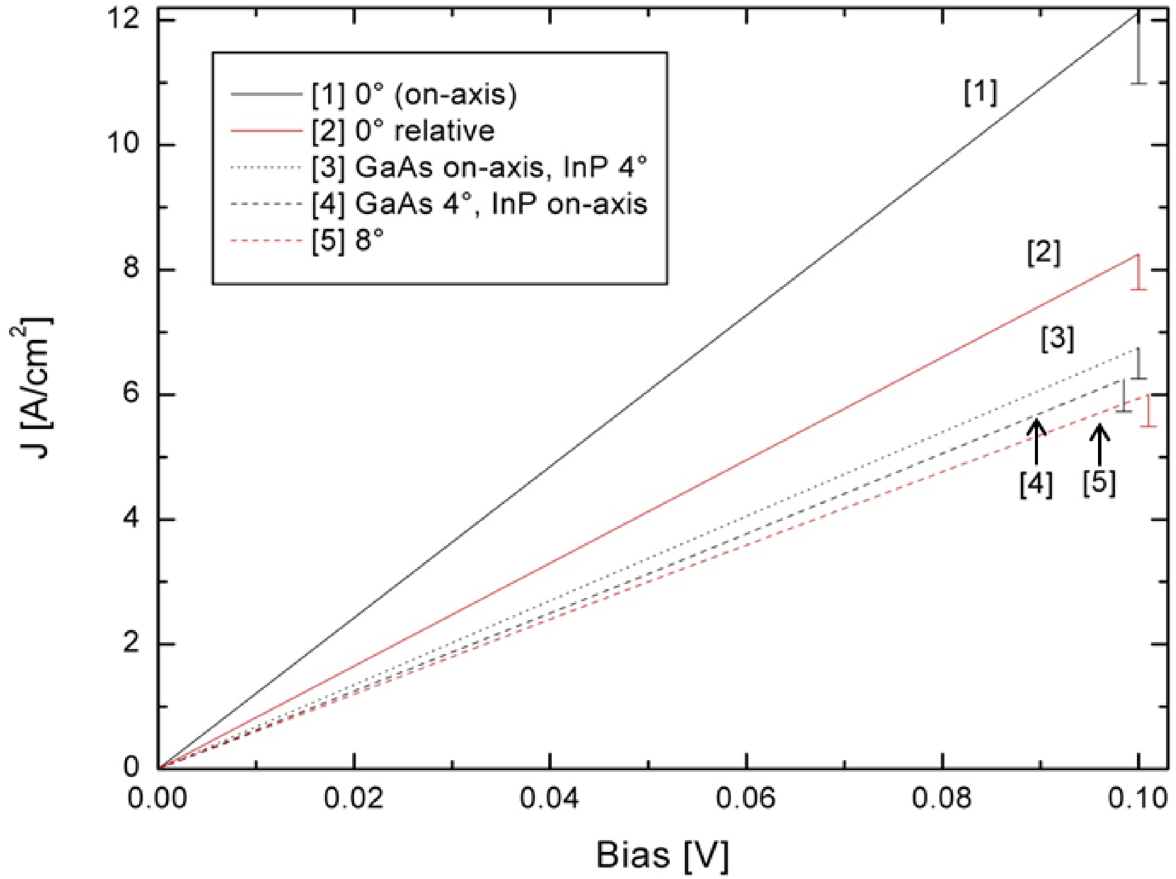


**Figure 11. Current-density vs voltage for 2x2 mm$^2$ GaAs//InP structures after 2-min RTP at 600 °C with AuGe/Ni/Au contacts on front and back for various relative surface misorientations.**

“Automat for simulation of heterostructurs” (AFORS-HET)[28, 29] was used as modeling software in order to simulate the band structure at the interface to visualize the band bending that occurs due to interface charge states. For homojunctions, curves were symmetric and similar to Figure 4. However for heterojunctions, asymmetry in the band structure is observed and shown in a) and b) of Figure 12.

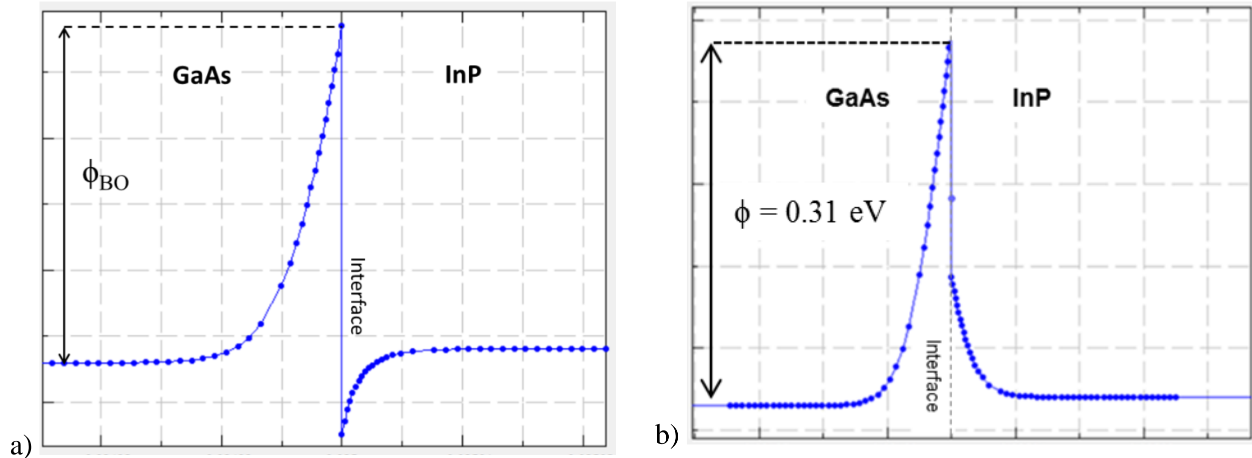


**Figure 12. Band structure of GaAs//InP interface a) without interface charge states and b) with interface charge states, $q_{int} = 8.5*10^{11}$.**

Comparing a) and b) of Figure 12, the addition of charge states to the interface in order to match the potential barrier height calculated by the Seager-Pike model (see Figure 18) changes the band structure to be more symmetric and similar to those of homojunctions as demonstrated in Figure 4. Despite this change there remains some asymmetry which has the potential to be observed in J-V measurements. In order to examine the possibility of non-symmetric behavior due to a difference in potential barrier heights in the heterostructure, J-V performance about the origin were simulated and measured and then compared. To compare forward and reverse bias, the current-voltage graphs were overlaid by taking the absolute values of the reverse bias sweep and plotting then with the forward bias as shown in Figure 13. J-V simulation of the heterostructure indicated that the heterostructure would begin to display slight asymmetry above around 0.08 V, as shown in a) of Figure 13. However this asymmetry was not observed in measured J-V performance of the GaAs//InP structure at the bias range used in this experiment as shown by b). Experimental interface resistances were higher than simulated interface resistances (0.0083 vs 0.00625 $\Omega \cdot cm^2$), this is attributed to calculation differences between the

Seager-Pike model and AFORS-HET software, as simulated interface resistances can be matched to measured interface resistances by adjusting the potential barrier height from 0.31 eV to 0.34 eV for GaAs//InP on-axis structures.

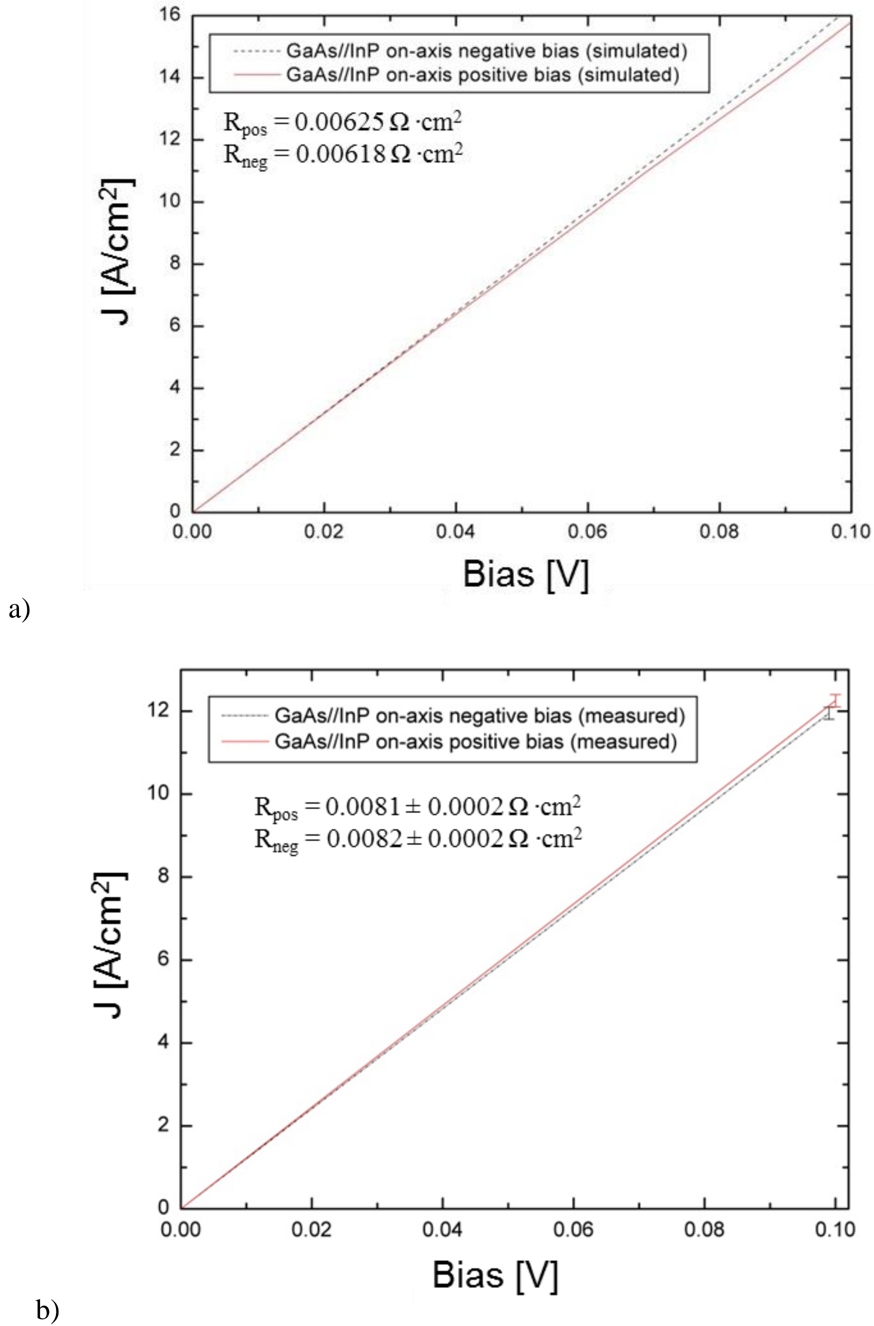


**Figure 13. J-V performance of GaAs//InP with on-axis substrates examining effect of asymmetric barrier $\phi_{BO}$ = 0.31 eV a) simulated with AFORS-HET and b) measured.**

All GaAs//InP combinations were compared over the bias range ± 0.1V and no asymmetry was measured, and therefore at these low biases the asymmetric heterostructure potential barrier height was not a factor in J-V performance. This is due to charge states at the interface which reduce the band asymmetry to below measurable levels at these low biases. Without charge states in the simulation, J-V performance was strongly asymmetric as demonstrated in Figure 14. Reduction of sample size to achieve a larger voltage range is a topic discussed further in section 5.

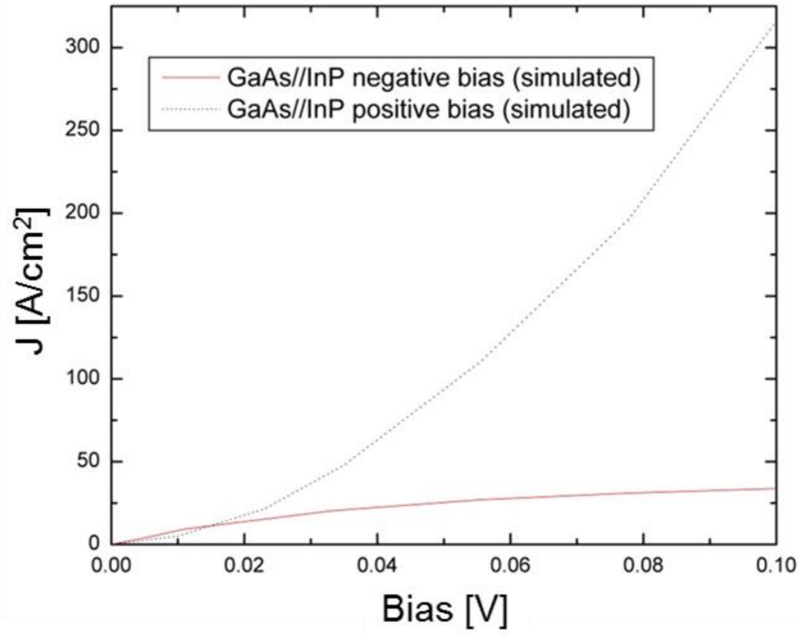


**Figure 14. J-V Simulation of GaAs//InP structure without charge states at the interface.**

### 4.3 Zero-bias conductance vs 1/T

To estimate the conduction barrier height of the double depletion region at the interface, the zero-bias interface conductance with respect to temperature was fitted to the Seager-Pike electron tunneling model. At temperatures above 170 K the conductance is characterized as an exponential relationship with temperature, from which the slope can be used to extract the

activation energy of the conduction barrier, and is consistent with thermionic emission over the barrier being the primary electron transport mechanism across the bonded interface. At lower temperatures, thermionic emission is suppressed and the conduction becomes independent of temperature, as shown by the saturation of conductance curves at around 140 K in Figures 16, 17, and 18. In the low temperature regime, conduction occurs by electron tunneling through the potential barrier, and results are found to agree well with the model proposed by Seager and Pike for the tunneling contribution across a grain boundary in GaAs doped in the $10^{18}$ range[24].

The n-type Schottky diode under forward bias is used to approximate the diffusion transport mechanism across the double depletion region[8, 30]. The diffusion current can potentially contribute a significant portion to the overall conduction, and the expression for diffusion current is given in Equation 8 below:

$$J_n = J_D \cdot \left[e^{\frac{qV}{kT}} - 1\right] \tag{8}$$

Where $J_n$ is the diffusion current density, $J_D$ is the saturation current density, $V$ is the voltage bias. $J_D$ is less dependent on temperature when compared to the square power law current-temperature relationship in thermionic emission. As a result the applied bias $V$ is the governing parameter in diffusion current[30].The Seager-Pike model derives the zero-bias conductance from the slope of J-V curves within a narrow ±50 mV range about zero bias. Simulation of forward bias diffusion current density shown in Figure 15 with material properties for n-GaAs ($N_d = 10^{18}$, $J_D$ = $10^{-12}$) that matched well with [32]. Due to the relatively small voltages under evaluation, diffusion transport is not considered to be a significant factor (< 0.1 mA/cm$^2$) for GaAs doped in the $10^{18}$ range in the overall electron conduction across the bonded interface for these experiments[8, 27, 31].

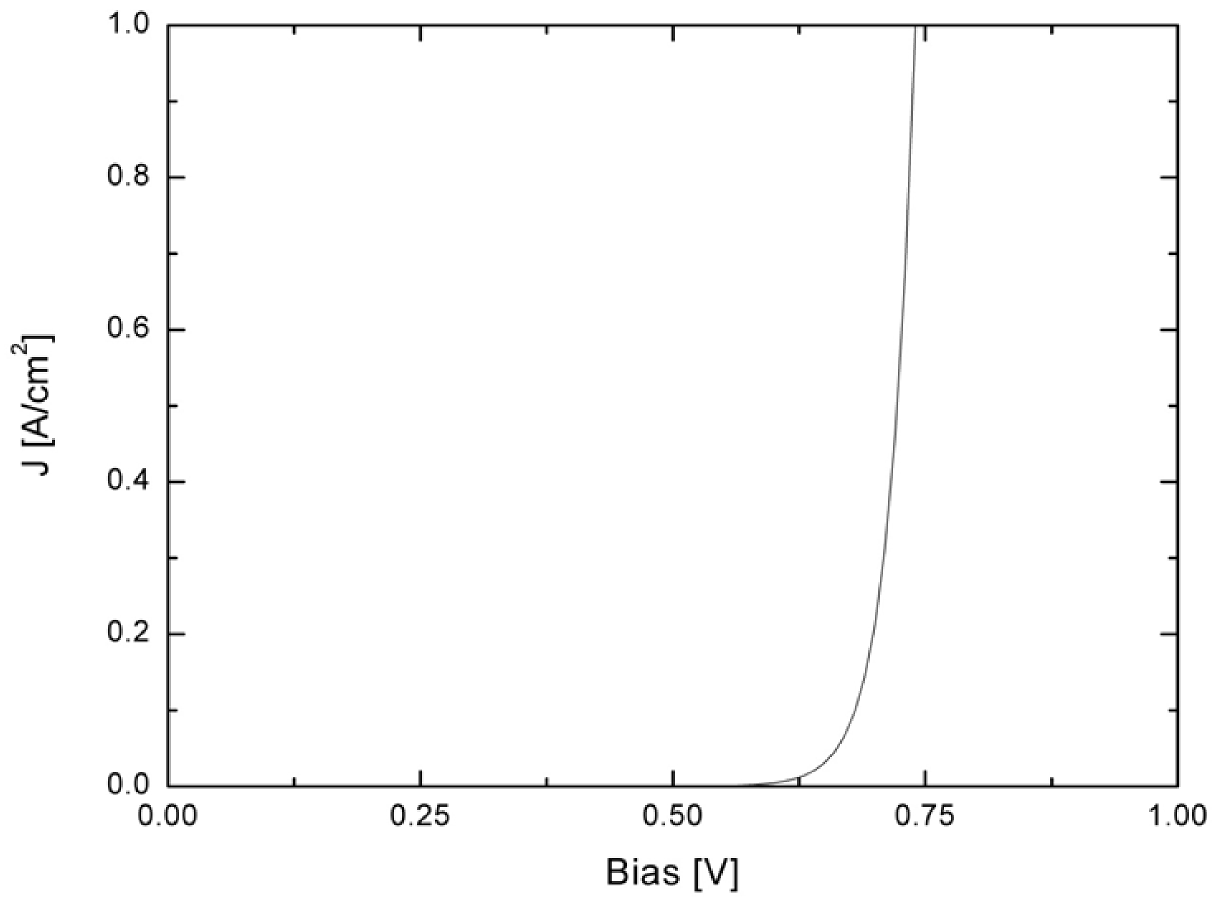


**Figure 15. Simulated forward bias diffusion current density vs voltage[32] for GaAs ($N_d = 10^{18}$) Schottky diode, $J_D = 10^{-12}$.**

**Table 3. Interface potential barrier height for GaAs//GaAs , GaAs//InP, and InP//InP bonding combinations**

| Wafer1//Wafer2 | Relative Misorientation (°) | Interface Potential Barrier Height (eV) |
|---|---|---|
| GaAs//GaAs | 0 (On-Axis) | 0.56 |
| | 4 | 0.61 |
| | 8 | 1.0 |
| InP//InP | 0 (On-Axis) | 0.26 |
| | 4 | 0.31 |
| | 8 | 0.29 |
| | 0 | 0.27 |
| GaAs//InP | 0 (On-Axis) | 0.31 |
| | 4 (GaAs On-Axis) | 0.37 |
| | 4 (InP On-Axis) | 0.35 |
| | 8 | 0.39 |
| | 0 | 0.32 |

The barrier height for each material combination is shown in Table 3. Results for GaAs//GaAs samples are shown in Figure 16, taken from previous publications on GaAs//GaAs bonded structures with comparable relative surface misorientations[3, 8]. A potential barrier height of 0.54 eV was calculated for on-axis structures, and a height of 1.0 eV was calculated for structures with 8° of misorientation. This is consistent with previous findings by our group showing an increase in barrier heights with increased relative misorientation[3, 5] .

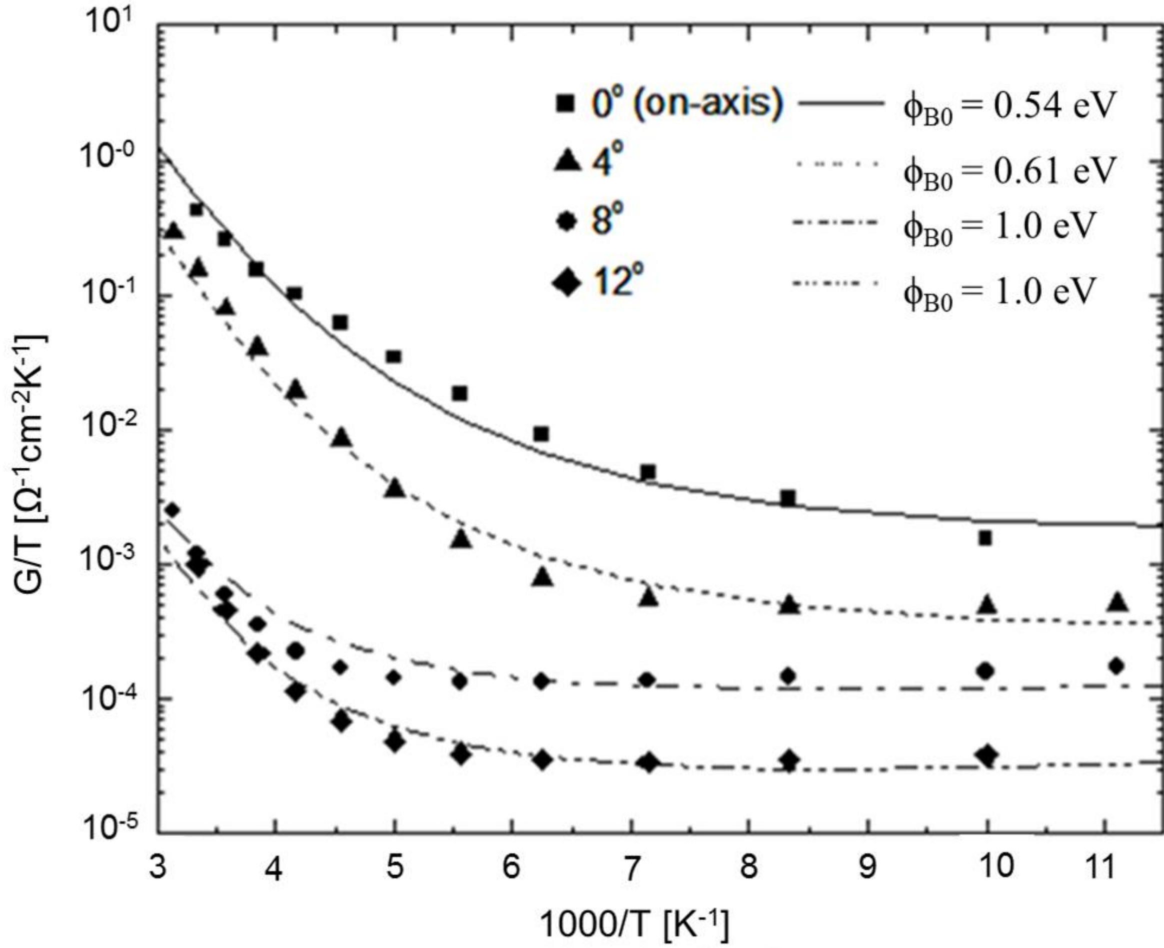


**Figure 16. Fit of zero-bias conductance vs 1000/T to Seager-Pike model for GaAs//GaAs, reproduced from [3].**

Work published by Okuno *et. al*[20] with comparable barrier height of 0.35 eV for similarly doped GaAs//InP structures bonded at higher temperatures and times (600-700 °C, 30 min) at kPa pressure during bonding without sulfur passivation demonstrated that the electrical properties of the interface are not affected by in-plane rotation of 90°. Earlier published work from Kish *et. al*[21] reported GaP//$In0_{.5}Ga_{0.5}P$ and GaP//GaP structures bonded at higher temperatures (1000 °C, ~1 hour) at MPa pressures without sulfur passivation and demonstrated that an in-plane rotational misorientation of 5° caused an ~80% decrease in J-V performance of

both the homo and hetero structures. However the decrease in conductivity became negligible when in-plane misorientation was 180° when compared to conductivity in samples with 0° in-plane misorientation. The relationship between electrical properties caused by in-plane misorientations is therefore complex, with in-plane misorientation causing a decrease in conductivity until a certain point at which conductivity increases to be equivalent to nominal structures. In-plane misorientation for samples in this study is much less than 90° and likely closer to 5°, and this could explain the results for InP//InP samples. However without measuring in-plane twist it is difficult to quantify its impact on this specific material system and bonding procedure. This topic is further addressed in section 5.

Results for InP//InP structures are shown in Figure 17. A potential barrier height of 0.26 eV was obtained for on-axis bonded pairs and as the relative misorientation was increased, the potential barrier height increased. The 4° misoriented samples exhibited a height of 0.31 eV, and the 8° misoriented samples a height of 0.29 eV. The larger increase in potential barrier height for the 4° misoriented structure is perhaps explained by a larger component of in-plane twist for the 4° misoriented sample.

The barrier for on axis structures was comparable with the 0.27 eV barrier observed for 0° relative misoriented samples, indicating that relative surface misorientation rather than substrate miscut is responsible for the band structure at the interface. Compared to the GaAs//GaAs and GaAs//InP structures, the conductivity of InP//InP structures was greater at room temperature and did not decrease below 0.1 $(ohm*cm^2*K)^{-1}$ across the range of temperatures studied for equivalent relative misorientations.

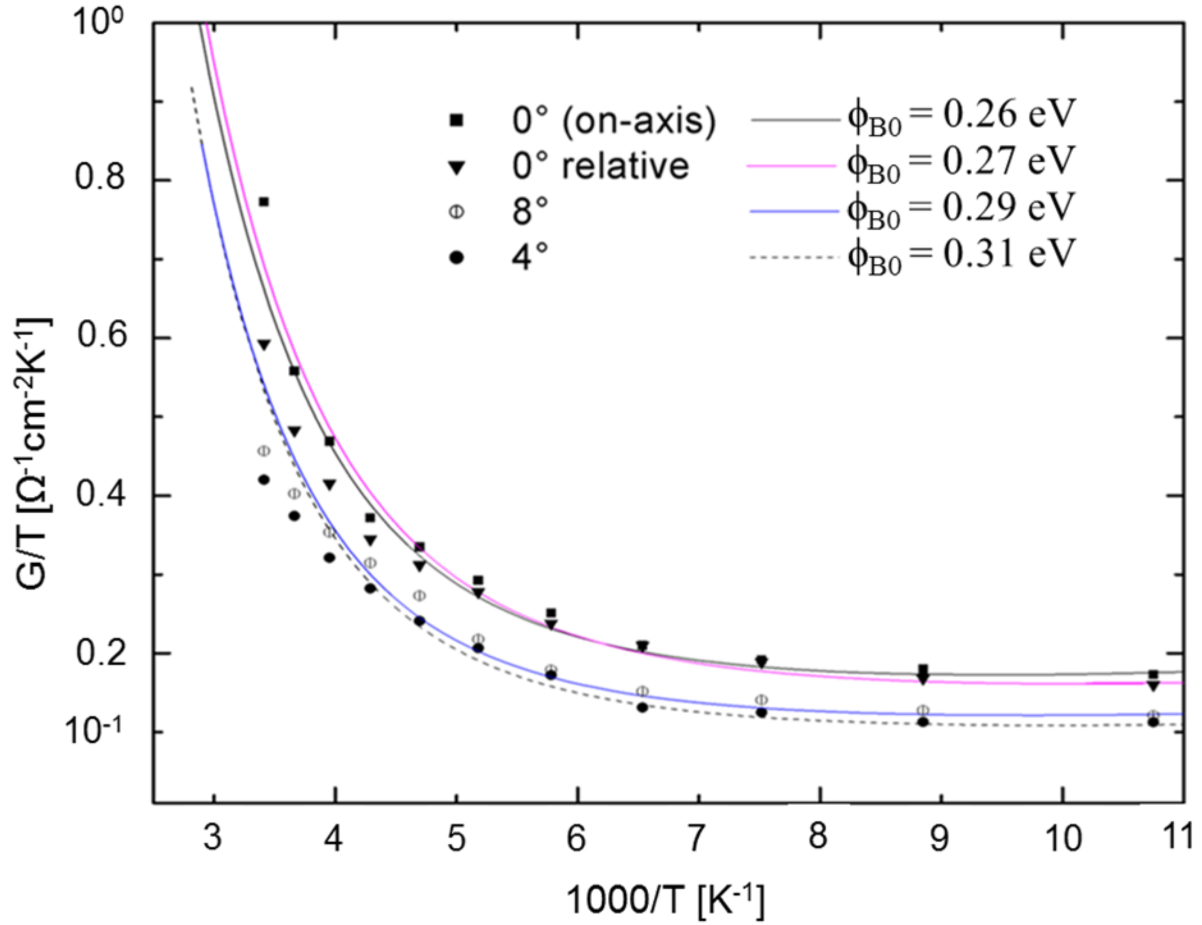


**Figure 17. Fit of zero-bias conductance vs 1000/T to Seager-Pike model for InP//InP.**

GaAs//GaAs and InP//InP structures demonstrate comparable increases in barrier height between on-axis structures and those with 4° of relative misorientation (0.07 eV increase for GaAs//GaAs and 0.05 eV increase for InP//InP). GaAs//GaAs structures with 8° of misorientation displayed a larger increase in barrier height (0.46 eV increase for GaAs//GaAs vs 0.03 eV increase for InP//InP) when compared to the on-axis structures.

For GaAs//InP samples, we investigate the effect of lattice mismatch (~4% difference in lattice parameter between GaAs and InP) on potential barrier height, and zero-bias measurement results are found in Figure 18. A barrier height of 0.31 eV was calculated for on-axis structures

and agrees fairly well with the 0.35 eV barrier height reported for similar structures reported by Okuno *et. al*[20]. As relative misorientation was introduced, the barrier height increased accordingly. Structures with on-axis InP substrates bonded to 4° misoriented GaAs (resulting in a relative misorientation of 4°) demonstrated a barrier height of 0.35 eV. Structures with on-axis GaAs substrates bonded to 4° misoriented InP substrates (resulting in a relative misorientation of 4°) demonstrated a barrier height of 0.37 eV. This difference in barrier height for heterostructures with equivalent 4 ° relative misorientation is due to the difference in doping levels of the respective substrate wafers. GaAs//InP structures with 8° of relative misorientation resulted in a barrier height of 0.39 eV.

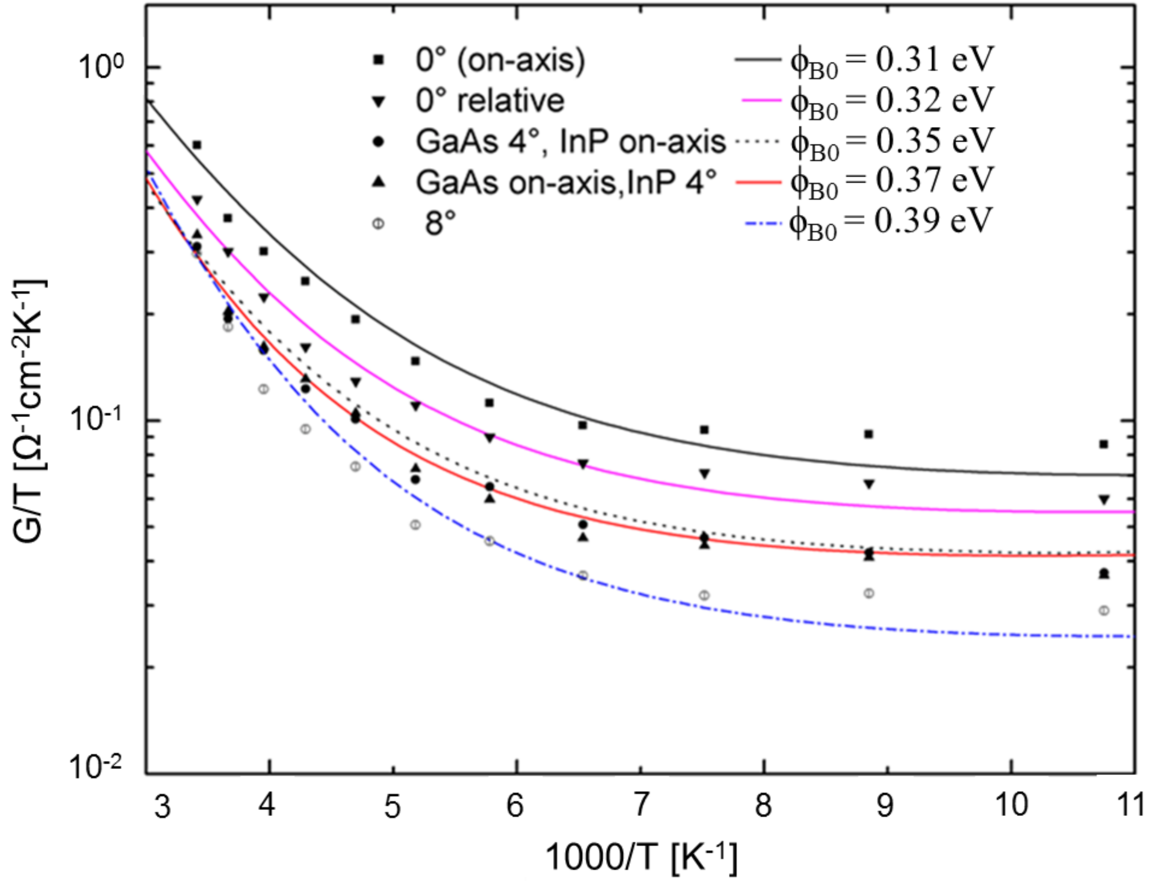


**Figure 18. Fit of zero-bias conductance vs 1000/T to Seager-Pike model for GaAs//InP.**

The change in barrier height between on-axis and 8° misoriented GaAs//InP structures (0.08 eV increase) is comparable to the increase for InP//InP structures with similar misorientation (0.05 eV increase) and much lower than the increase in barrier height for GaAs//GaAs structures with similar misorientation (0.46 eV increase). Samples with 0° relative misorientation resulted in a height of 0.32 eV, which compares with that of on-axis structures. These results are consistent with our previous observations on GaAs//GaAs and InP//InP bonded structures that show an increase in potential barrier height with increased relative misorientation between the substrates. Figure 19 demonstrates that structures containing at least one side InP are

more stable to misorientation changes, and that the electrical conductivity across GaAs//InP bonded structures is not impacted by the additional variable of lattice mismatch.

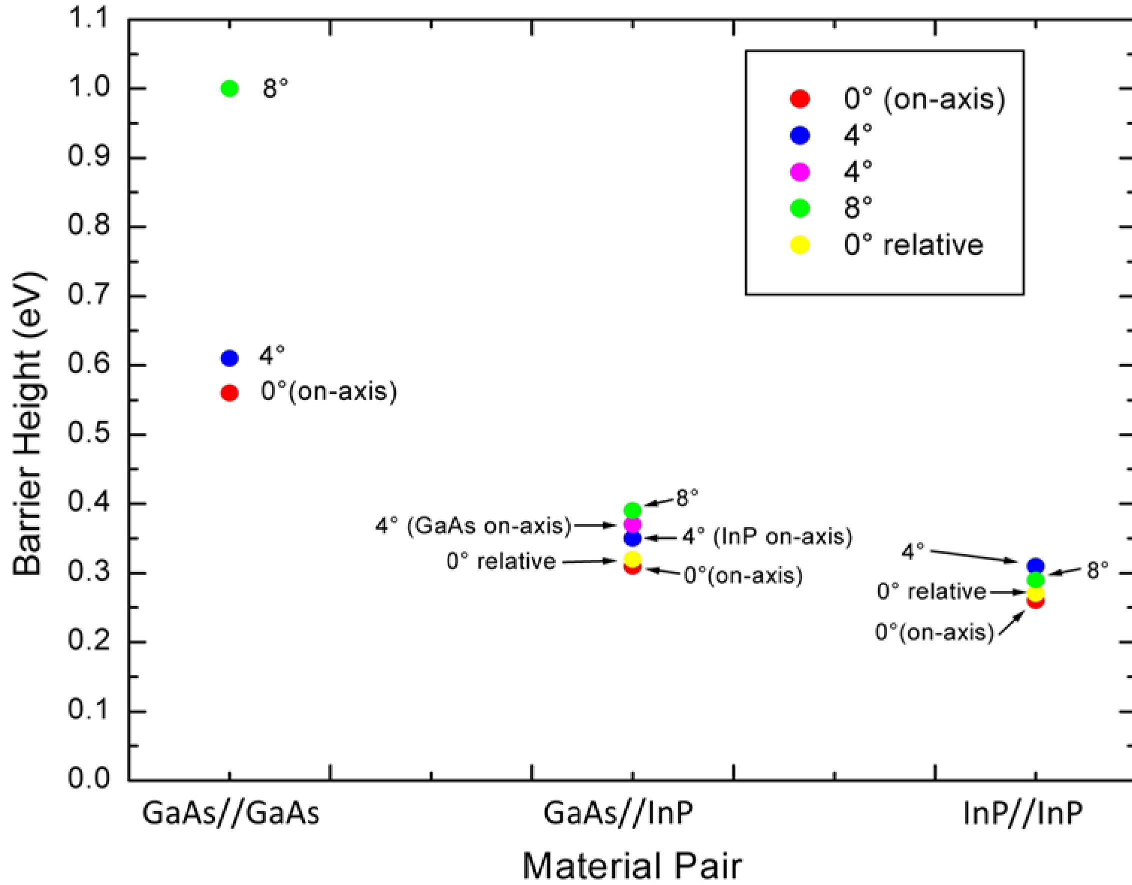


**Figure 19. Barrier height as a function of material pair.**

The treatment of GaAs and InP surfaces with sulfur or sulfide-containing solutions has been shown to improve the surface electronic properties primarily due to replacement of surface oxide with a thin sulfide layer[6, 9, 11, 33, 34] which reduces the Schottky barrier height for both GaAs and InP. For equivalently treated InP and GaAs surfaces, it has been shown that InP surfaces have lower barrier heights (0.25-0.55 eV) than GaAs surfaces (0.4-1 eV)[33]. Additionally, previous work on polycrystalline InP and GaAs has shown that the degradation of

electrical conduction through n-GaAs grain boundaries is more severe due to Fermi level pinning below mid-gap compared to grain boundaries in n-InP, in which Fermi levels are pinned above mid-gap[35] . These findings are consistent with the lower barrier height for n-InP//n-InP interfaces (0.26 eV-0.31 eV) compared to n-GaAs//n-GaAs (0.54-1.0 eV) interfaces in this study.

### 4.4 HRTEM/STEM

HRTEM images of selected bonded combinations were taken to observe microstructural changes and compare the interface morphologies across the homo and hetero structures. Figure 20 shows the high resolution cross section TEM images taken with direct semiconductor to semiconductor contact. The change of interface microstructure with this higher temperature annealing has been previously reported in GaAs//GaAs interfaces annealed for longer times (5-30 minutes) and is attributed to the reduction of interface surface tension of the amorphous oxide by forming spherical shaped aggregates, coupled with the diffusion of oxygen into interfacial inclusions or into the semiconductor bulk[19, 36, 37]. The lack of oxide layer present in InP//InP samples before and after annealing for 2 minutes at 600°C is consistent with lower oxide concentrations on InP surfaces prior to bonding[11, 33].

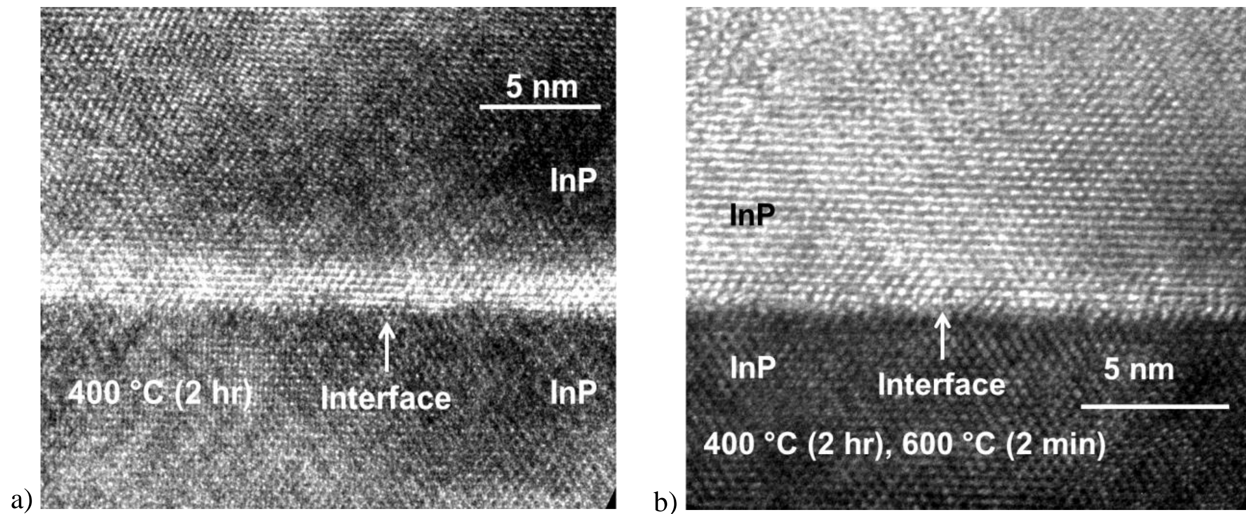


**Figure 20. HRTEM of InP//InP interface a) annealed for 400 °C for 2 hours b) plus a 2 minute 600 °C RTP step.**

HAADF/STEM images were taken of the GaAs//InP on-axis interface after 2 minutes at 600 °C RTP to observe morphology across a larger region than HRTEM, as presented in Figure 21. Consistent with previous work on similarly treated GaAs//GaAs interfaces, regions of oxide inclusions represented by the dark regions have formed at the interface[3, 19] with areas of direct of substrate contact in between. The area of investigation in HRTEM images (~20 nm$^2$) is several hundred times smaller than the HAADF/STEM images (500 nm$^2$). By focusing in on regions without oxide inclusions, a HRTEM image can be taken that displays direct contact between substrates. The bright spots in the InP substrate are likely surface damage due to the softness of the substrate compared to GaAs, and were created during the TEM sample preparation process.

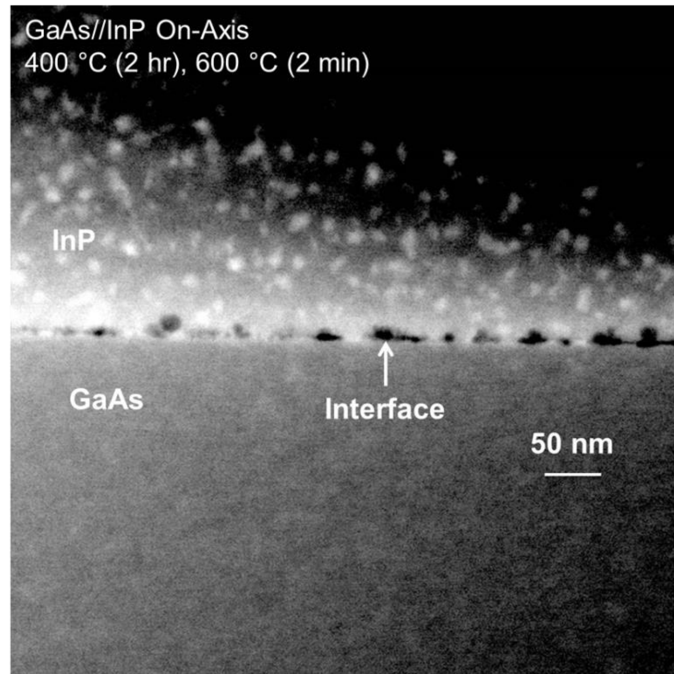


**Figure 21. STEM/HAADF of GaAs//InP on-axis interface post 600 °C RTP for 2 min.**

# Chapter 5: Conclusion and Future Work

Direct wafer bonding has been used to fabricate n-GaAs//n-GaAs, n-GaAs//n-InP, and n-InP//n-InP structures using substrates with zero and four degrees of miscut to achieve a range of relative surface misorientations of 0°, 4°, and 8°. Structures with non-zero relative misorientation have been compared with on-axis structures in order to investigate the effect of the misorientation on the electrical conductance through the interface. Structures with zero relative misorientation were also compared to on-axis structures to examine the effect of relative surface misorientation. As the relative surface misorientation was increased, all samples exhibited an increase in interface resistance. For GaAs//GaAs samples, interface resistance increased by two orders of magnitude from 0.011 to 2.8 $\Omega \cdot cm^2$ for 8° relative misoriented samples when compared to on-axis specimens. For InP//InP samples, interface resistance increased from 0.0063 to 0.0073 $\Omega \cdot cm^2$ for 8° relative misoriented samples when compared to on-axis specimen. For GaAs//InP samples, interface resistance increased from 0.0082 to 0.018 $\Omega \cdot cm^2$ for 8° relative misoriented samples when compared to on-axis specimen. The band structure of the homo and hetero structures was simulated and J-V measurements of GaAs//InP bonded structures revealed no asymmetry at the low biases used to determine interface resistance. A significantly lower interface resistance was measured for samples containing at least on side InP, implying that the interface conductance of these structures is more stable to changes in relative surface misorientation without suffering significant electrical conductivity degradation.

The zero-bias conductance with respect to inverse temperature was fit to the Seager and Pike electron model to extract the potential barrier heights. For GaAs//GaAs structures, misorientation of 8° resulted in a 0.46 eV increase in barrier height. For InP//InP samples, misorientation of 8° resulted in a 0.03 eV increase in barrier height. For GaAs//InP samples,

misorientation of 8° resulted in a 0.08 eV increase in barrier height. HRTEM characterization of the InP//InP bonded interface after RTP display no interfacial layer with correspondingly low interface resistances (<0.01 ohm·$cm^2$). TEM characterization of 8° misoriented GaAs//InP interface after RTP show regions of both interfacial oxide and direct substrate to substrate contact. These findings establish that material choice and relative misorientation (rather than substrate miscut) in the direct bonded interface are crucial parameters to maintain high conductivity between direct-bonded structures in multijunction solar cells.

Future work on this topic is needed to gain a more complete understanding of the effect of relative surface misorientation on the interface resistance. This study has shown that while lattice mismatch does not significantly increase resistance through GaAs//InP structures, both material choice and relative misorientation between substrate have a significant impact on interface conductivity. Specifically, future work includes additional HAADF TEM images of GaAs//InP 8° interface to examine interface morphology and confirm presence of amorphous inclusions.

The effect of in-plane rotational misalignment between bonded miscut wafers should be examined. For the work herein, in-plane twist was not considered as a variable; however due the manual bonding procedure some in-plane twist was inevitably introduced. Improved cleaving and bonding procedures could reduce the magnitude of in-plane twist, but a study of the effect of in-plane twist on electrical properties between miscut substrates should be carried out.

The effect of band asymmetry on electrical performance at large bias is another area that should be studied. For the small bias ranges used in this work no asymmetry in J-V behavior was found, however simulation of the heterostructures predicted asymmetry above 0.1V. This could be tested by reducing the area of the die, and larger current densities can be achieved. Previous

publications have reported techniques for reducing the area of the wire-saw die for homostructures, and should be adapted for this work.

Due to the practical application of these results into solar cell structures, the natural progression of this project is to directly bond layers that participate in the bonded interface of multijunction solar devices. For example, with one recent publications detailing epitaxially grown solar structures that are lattice matched to GaAs and InP substrates and then directly bonded together serving as the guide[1], Ga(In)As (1.4 eV) should be epitaxially grown atop on-axis and miscut GaAs substrates, and then bonded to GaInPAs (1.05 eV) epitaxially grown atop on-axis and miscut InP substrates. This would unite the research directly with the multijunction devices achieving world record power conversion efficiencies.

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