UNIVERSITY OF CALIFORNIA, SAN DIEGO

Fast Hopping High-Frequency Carrier Generation in Digital CMOS Technology

A dissertation submitted in partial satisfaction of the
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in

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by

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2009

The dissertation of Mohammad Farazian is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2009

DEDICATION

To my parents,
my sister Maryam and my brother Maysam.

EPIGRAPH

”A clever person solves a problem. A wise person avoids it.”

—Albert Einstein

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ABSTRACT OF THE DISSERTATION

Fast Hopping High-Frequency Carrier Generation in Digital CMOS Technology

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)
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Lawrence E. Larson, Chair

One of the challenges in implementing a frequency synthesizer for Multi-band OFDM Ultra Wideband (MB-OFDM UWB) is overcoming the agility limitations of conventional synthesizers. The MB-OFDM proposal for UWB divides the spectrum from 3.1 GHz to 10.6 GHz into 14 different bands, and frequency hops at the rate of 3.2 MHz between them with a specified frequency settling time of only 9.5 nS. Design techniques that eliminate the use of on-chip inductors, and which are compatible with low voltage operation, are critical for increasing the level of integration for future implementations.

An inductor-less design methodology may have several advantages over traditional design techniques: (1) While the area required to implement an on-chip inductor does not scale down in the finer technology nodes, inductor-less designs benefit from technology scaling. (2) On the other hand, the quality factor of the on-chip inductors may worsen in finer technology nodes, which can lead to an increase in the required current consumption to generate a given voltage swing. (3) It is more straightforward to port an inductor-less design into a new technology node. The penalty for an inductor-less design methodology is a slightly increase in the current consumption to achieve the necessary gain and voltage swing in the absence of inductors.

In this work, a frequency plan is proposed that can generate all the required frequencies from a single fixed frequency and can implement any center frequency with a maximum of two levels of SSB mixing. In order to generate all the required frequen-

cies for the operation of this frequency synthesizer out of a single frequency, fractional frequency dividers are needed. Therefore, a study is performed on the architectures that can obtain a fractional division ratio. This study involves an analysis of the operation, stability, and phase noise of injection-locked regenerative frequency dividers. In addition, the operation, stability, locking range, and phase noise of two-stage ring-oscillators, which are compact ways to generate quadrature output phases and can be used in injection-locked regenerative frequency dividers, are analyzed.

This work presents the first CMOS inductor-less single PLL 14-band frequency synthesizer for MB-OFDM UWB which is capable to perform any arbitrary band switching specified in less than 2 nS. Implemented in a 0.13μm CMOS process, it uses a single 1.2 V supply voltage, and dissipates 135 mW. The mixing sideband level is better than -31 dBc and the phase noise is better than -110 dBc/Hz at 1 MHz offset.

Chapter 1

Introduction

1.1 Wireless Personal Area Networks

The prevalence of universal serial bus (USB) technology in consumer households and beyond is unquestionable. USB has become a de facto standard for interfacing a personal computer (PC) to different peripherals such as webcams, printers, keyboards, and digital cameras. In addition, the fast speed of USB 2.0 (480 Mbps) makes it an appropriate medium for applications such as high-speed data transfer between a PC and external data storages or streaming high definition video contents. Indeed, at its arrival, the ubiquitous USB logo was a sign of comfort and relief. With the universal interface, consumers were liberated from the chains of interface limitations and USB related products soared. From computer pointing devices (mouse, keyboard, etc.) to digital imaging products, USB is everywhere.

However, the increase in USB related products encourages an environment filled with USB cables. Consumer households, for example, are typically cluttered with multiple digital cameras, portable MP3 players, and communication devices that interface with personal computers on a daily basis. As a result, dorm rooms, family rooms, and other personal areas are cluttered with USB cables, and users are trapped in an unnecessary web of tangles.

Indeed, a wireless solution will simplify a great deal of chaos, and the demand in developing a high-speed wireless personal area network (WPAN) to replace the existing

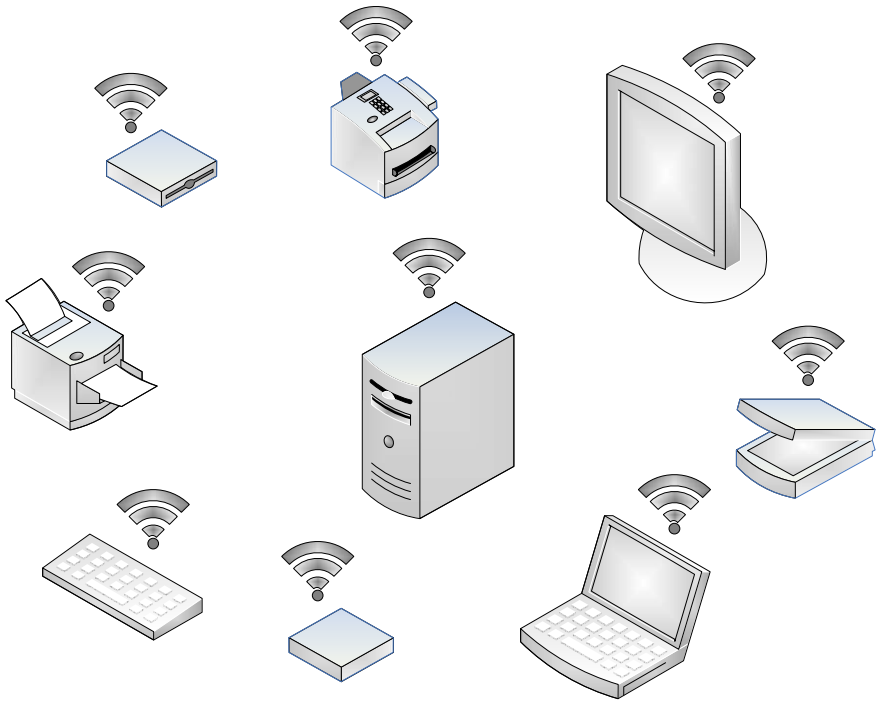


Figure 1.1: Application of a WPAN to provide WUSB in home and office.

USB cables with a wireless USB (WUSB) link is inevitable. Wireless USB, or WUSB, is an implementation of the USB standard using an appropriate WPAN standard that can match the data rate of USB in short range. WUSB devices must be capable of sending 480 Mbps at distances up to 2 meters and 110 Mbps at up to 10 meters. As WUSB is a relatively novel standard, it has yet to be fully adopted by the industry. However, support continues to grow as more devices are being ported to use the technology. Figure 1.1 shows application of a WPAN, in the form of WUSB, in home or office to connect PC to peripherals. Figure 1.2 shows the application of WPAN in consumer's houses to connect set top boxes, DVD players, Hi-Fi audio systems, digital cameras, and camcorders to high definition TV (HDTV) wirelessly.

1.2 An Overview of Wireless Personal Area Networks

There are few existing standards for short range wireless data networks that could be used to provide a WPAN, including Bluetooth and ZigBee. Bluetooth oper-

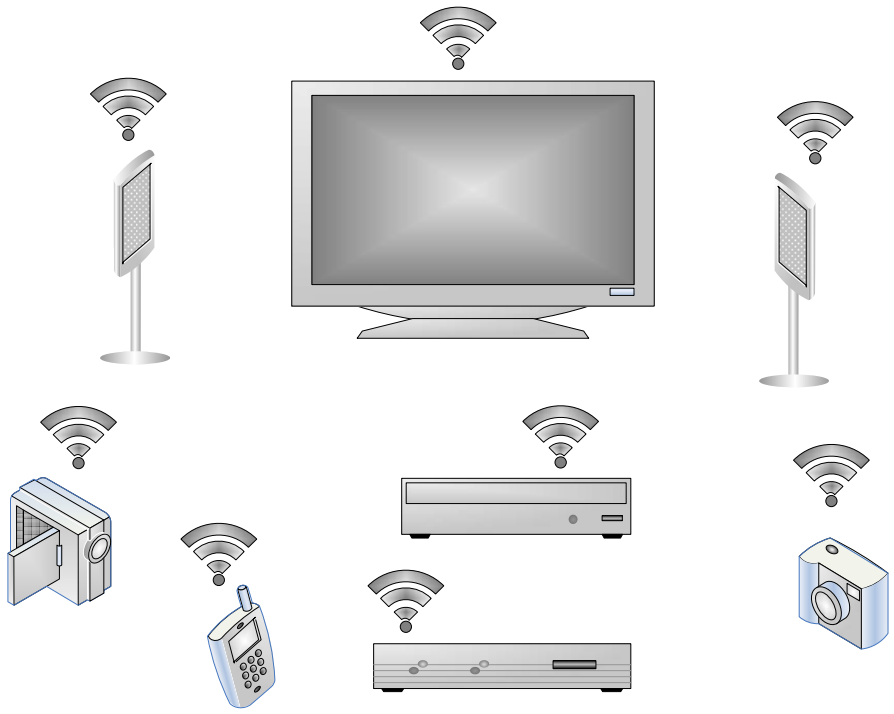


Figure 1.2: Consumer electronics application of WPAN in homes.

ates at 2.4 GHz, uses GFSK modulation, and provides a data rate of 1 Mbps for short distances. An enhancement to Bluetoothe (EDR) can increase this data rate to 3 Mbps.

ZigBee can operate at multiple carriers, including 2.4 GHz, and exploits Direct-Sequence Spread Spectrum (DSSS). The achievable data rate of ZigBee is limited to 250 kbps per channel and it can cover distances of 10 to 75 meters.

In addition, there are other wireless data networks that are mainly designed to be used in a WLAN and they can provide moderately high data rates, including different variations of Wi-Fi 802.11 standard. For instance, 802.11a and 802.11g operate at 5 and 2.4 GHz bands respectively, and occupy 20 MHz bandwidth, use 64 QAM constellation and OFDM modulation, and provide a maximum data rate of 54 Mbps, for a range of 100 meters. Additionally, 802.11n can operate at both of the mentioned carrier frequencies and uses the same modulation, with bandwidth of 40 MHz, and provides up to 130 Mbps per beam, or a maximum of 600 Mbps when four beams are used, and covers a range of 300 meters.

Lastly, Ultra-Wideband (UWB) can provide data rates as high as 480 Mbps for

distances less than 2 meters. This data rate drops to 110 Mbps for distances up to 10 meters. More details about UWB will be discussed later in this chapter.

A comparison of the mentioned wireless data networks is depicted in Fig. 1.3.

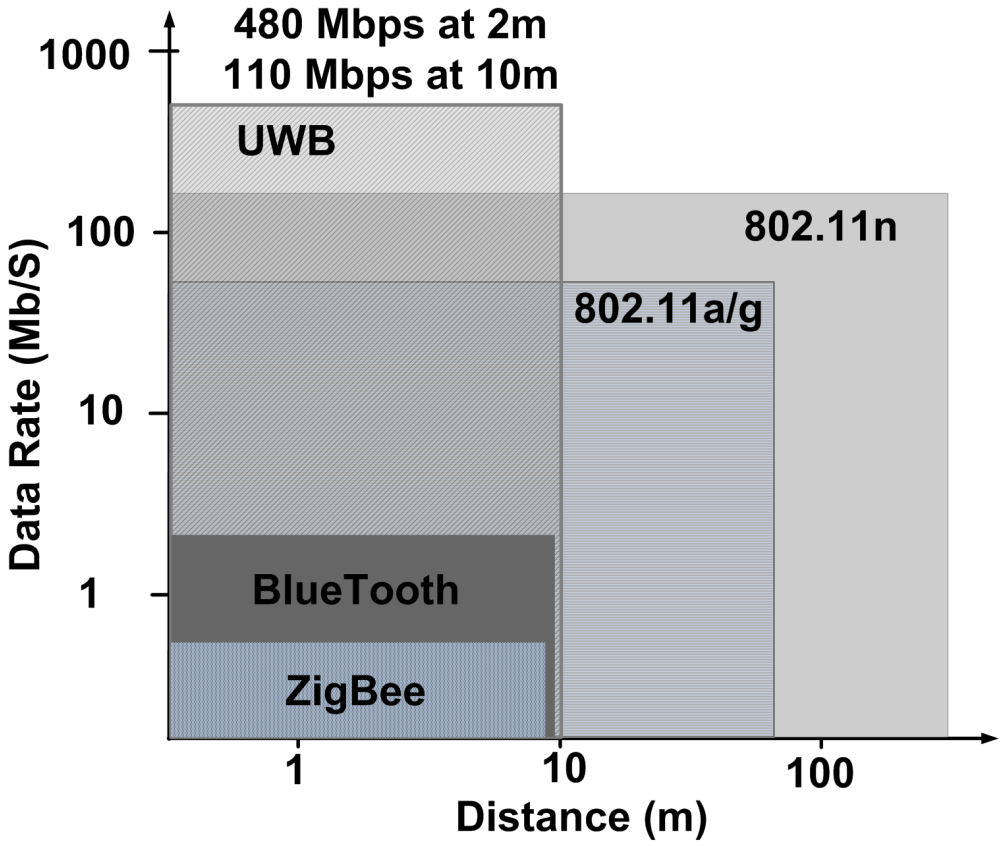


Figure 1.3: A typical UWB transceiver.

Among these networks, only UWB and 802.11n can achieve the desired data rate required for applications such as wireless USB. However, it needs to be mentioned that UWB achieves this data rate with less power consumption and less hardware (single antenna vs. three or four beams), and with a lower cost. In addition, the coverage of UWB is more appropriate for a WPAN.

1.3 Multi-band OFDM Ultra-Wideband

An ultra-wideband system is defined as a system that has a fractional bandwidth greater than 0.2, or a system that occupies an instantaneous bandwidth of greater than 500 MHz [1], and fractional bandwidth for any communication system is defined by

$$Fractional\ Bandwidth = (f_U - f_L)/f_C \tag{1.1}$$

where $f_C = (f_U + f_L)/2$ is the band center frequency, f_L is the band lower frequency, and f_U is the upper frequency. According to this definition, most communication standards are considered as narrow band systems. For instance, the fractional bandwidth of Wi-Fi 802.11n that operates at 5.4 GHz and has a bandwidth of 40 MHz is only 0.0074.

MultiBand Orthogonal Frequency Division Modulation (MB-OFDM) scheme for Ultra-Wideband divides the spectrum of 3.1 GHz to 10.6 GHz into fourteen 528 MHz bands. Each of the center frequencies for MB-OFDM can be expressed as

$$f_c = (5.5 + n) \times 528\ MHz \tag{1.2}$$

where n is the band number from 1 to 14. These fourteen bands are grouped into six band groups as shown in Table 1.1 [2]. All band groups consist of 3 bands except band group 5 which only includes bands 13 and 14.

The principles of operation of ultra-wideband can be described by the well-known Shannon-Hartley theorem for capacity of a communication channel with additive white Gaussian noise, as follows

$$C = B \log_2(1 + S/N) \tag{1.3}$$

where B is the bandwidth of the communication channel, and S and N are the average signal and noise power at the output of the channel, respectively [3].

According to (1.3) exploiting large bandwidth enables UWB to achieve high data rates with low transmitted signal power and using simple constellations. This is in contrast to 802.11 a/g/n that uses 64 QAM. In other words, UWB benefits from linear increase in the channel capacity by increasing the channel bandwidth in contrast to the logarithmic increase of channel capacity due to the increase in the signal power.

Table 1.1: MB-OFDM band group allocation.

Band Group	Band ID n_b	Lower Frequency (GHz)	Center Frequency (GHz)	Upper Frequency (GHz)
1	1	3.168	3.432	3.696
	2	3.696	3.960	4.224
	3	4.224	4.488	4.752
2	4	4.752	5.016	5.280
	5	5.280	5.544	5.808
	6	5.808	6.072	6.336
3	7	6.336	6.600	6.864
	8	6.864	7.128	7.392
	9	7.392	7.656	7.920
4	10	7.920	8.184	8.448
	11	8.448	8.712	8.976
	12	8.976	9.240	9.504
5	13	9.504	9.768	10.032
	14	10.032	10.296	10.560
6	9	7.392	7.656	7.920
	10	7.920	8.184	8.448
	11	8.448	8.712	8.976

Clearly UWB works in the noise floor of other communication systems. This can be well seen from the indoor in-band emission limits of UWB which is 74 nW/MHz compared to the ones for Bluetooth and WLAN that range from 1.2 to 30 μW/MHz (for different classes of Bluetooth)and 5-50 mW/MHz, respectively [4].

1.3.1 UWB Physical Layer (PHY) Description

Each of the bands in Table 1.1 consists of 128 sub-carriers with a spacing of 4.125 MHz. A total of 122 sub-carriers, including 100 data sub-carriers, 10 guard sub-carriers, and 12 pilot sub-carriers to enable coherent detection, are used to transmit information in MB-OFDM UWB.

A combination of frequency-domain spreading, time-domain spreading, and forward error correction (FEC) coding are used to optimize the performance of MB-OFDM for a variety of channel conditions. A convolutional code with coding rates of 1/3, 1/2, 5/8 and 3/4 is used in forward error correction [2].

Next, a time-frequency code (TFC) is used to distribute the coded information over different bands within a group. There are three different types of time frequency codes defined in [2]. The first one is time-frequency interleaving (TFI) where the coded data is spread over three bands of a band group. The second one is two-band time-frequency interleaving (TFI2) where the coded data is spread over two bands within a band group, and the third is referred to as fixed frequency interleaving (FFI) where the coded data is transmitted over a single band of a band group.

An example of time frequency interleaving, also known as band switching or frequency hopping, for bands in band group 6 is shown in Fig. 1.4.

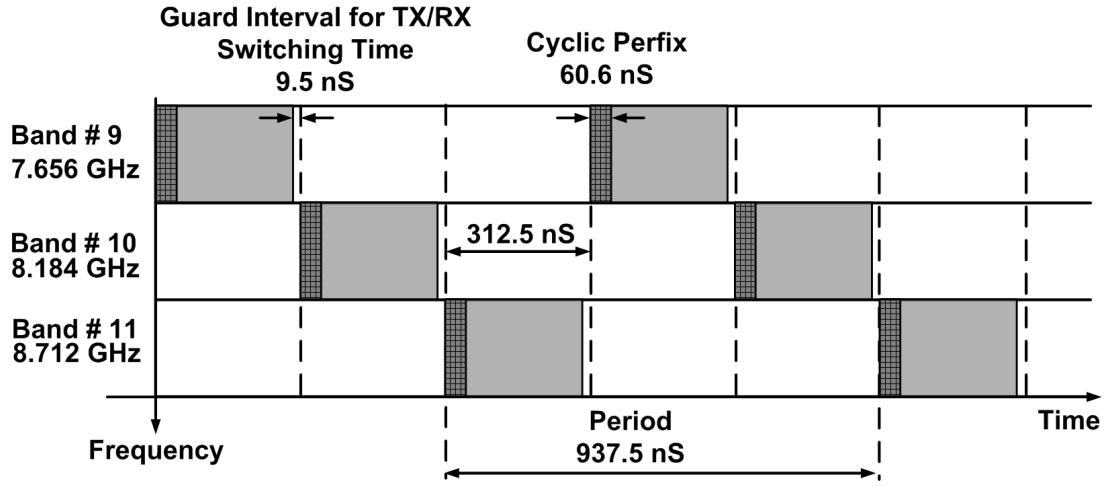


Figure 1.4: An example of time frequency interleaving for band group 6.

Time frequency codes (TFC) required for different band groups are specified in [2]. TFC codes of band group one are shown in Table 1.2. This table shows a total of ten TFC codes, hence it can support up to ten different channels. Time frequency codes for other band groups are similar to ones for band group one, with the exception of the fifth and the sixth band groups. The band group 5 only consists of two bands (bands 13 and 14). Hence, it only has one two-band time-frequency interleaving (TFI2) channels and one fixed frequency interleaving (FFI) channel. Band group six shares one band with band group three and two bands with band group four. As a result, all of its FFI codes and one of its TFI2 codes overlap with channels of band groups three and four.

Table 1.2: Time-Frequency Code Patterns for Band Group 1.

TFC number	Base sequence/ Preamble	Band ID (n_b) for TFC					
1	1	1	2	3	1	2	3
2	2	1	3	2	1	3	2
3	3	1	1	2	2	3	3
4	4	1	1	3	3	2	2
5	5	1	1	1	1	1	1
6	6	2	2	2	2	2	2
7	7	3	3	3	3	3	3
8	8	1	2	1	2	1	2
9	9	1	3	1	3	1	3
10	10	2	3	2	3	2	3

1.3.2 Signal Generation

The transmitted RF signal for MB-OFDM UWB can be described as

$$S_{RF}(t) = \mathrm{Re}\left\{ \sum_{n=0}^{N_{packet}-1} S_n(t - nT_{SYM}) e^{j2\pi f_c(q(n))t} \right\} \tag{1.4}$$

where $S_n(t)$ is the complex baseband OFDM signal for the n^{th} symbol ($s_n(t) = 0$ for $t \notin [0, T_{SYM})$, T_{SYM} is the symbol length, N_{packet} is the number of symbols in each packet, $f_c(\cdot)$ is one of the MB-OFDM carrier frequencies, and $q(\cdot)$ is the mapping function that maps the n^{th} symbol to an appropriate carrier frequency.

$S_n(t)$ is an OFDM signal generated from the complex coefficients of the n^{th} symbol ($d_n(k)$) as shown below.

$$S_n(t) = \sum_{k=0}^{N_{FFT}-1} d_n(k) e^{j2\pi k \Delta f t} \tag{1.5}$$

where $d_n(k)$ coefficients could either be data symbols, pilots, or other training sequences. The timing parameters of MB-OFDM are shown in Table 1.3.

MB-OFDM uses quadrature phase-shift keying (QPSK) modulation for the data rates 200 Mbps and lower and it uses dual carrier modulation (DCM) for the data rates of 320, 400, and 480 Mbps. Table 1.4 shows the data rate dependent modulation parameters of MB-OFDM UWB.

Table 1.3: Timing parameters of MB-OFDM UWB.

Parameter	Value
Sampling frequency (f_s)	528 MHz
Number of sub-carriers or FFT size (N_{FFT})	128
Number of data sub-carriers (N_D)	100
Number of pilot sub-carriers (N_P)	12
Number of guard sub-carriers (N_G)	10
Number of sub-carriers used ($N_T = N_D + N_P + NG$)	12
Sub-carriers frequency spacing ($\Delta f = f_s/N_{FFT}$)	4.125 MHz
FFT and IFFT period ($T_{FFT} = 1/\Delta f$)	242.42 nS
Symbol interval (T_{SYM})	312.5 nS
Symbol rate ($F_{SYM} = 1/T_{SYM}$)	3.2 MHz
PHY band switching time	9.47 nS

Table 1.4: Data rate-dependent modulation parameters of MB-OFDM UWB.

Data Rate (Mbps)	Modulation	Coding Rate (R)	FDS	TDS	Coded Bits/ 6 OFDM Sym.	Info Bits/ 6 OFDM Sym.
53.3	QPSK	1/3	Yes	Yes	300	100
80	QPSK	1/2	Yes	Yes	300	150
106.7	QPSK	1/3	No	Yes	600	200
160	QPSK	1/2	No	Yes	600	300
200	QPSK	5/8	No	Yes	600	375
320	DCM	1/2	No	No	1200	600
400	DCM	5/8	No	No	1200	750
480	DCM	3/4	No	No	1200	900

It is customary to present the baseband binary interleaved coded serial data, defined in [2], by $b[k]$, where $k \in \mathbb{N}_0$, and $\mathbb{N}_0$ is the set of non-negative integer numbers. In this case, by using $\tilde{b}[k] = 2b[k] - 1$ we obtain a ± 1 bit stream. This ± 1 bit stream ($\tilde{b}[k]$) is used to generate QPSK, or DCM symbols. QPSK symbols are generated by transforming each two adjacent bits into a normalized complex number using a gray-coded mapping, as shown below.

$$d[k] = K_{MOD_Q}\left(\tilde{b}[2k] + j\tilde{b}[2k+1]\right) \tag{1.6}$$

where $K_{MOD_Q} = 1/\sqrt{2}$. The resultant QPSK constellation is shown in Fig. 1.5.

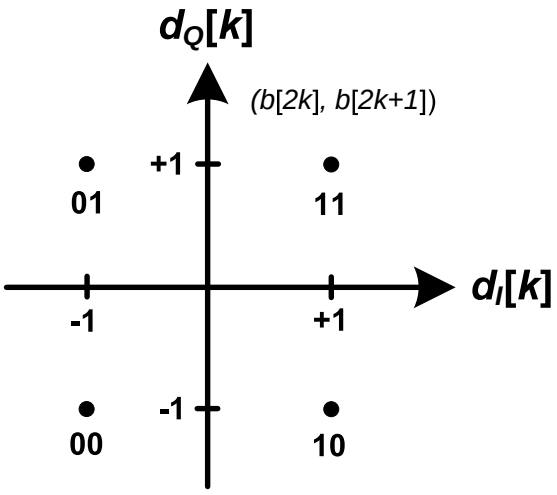


Figure 1.5: Mapping for QPSK.

As discussed earlier, dual carrier modulation (DCM) must be used for data rates higher than 320 Mbps. To perform dual carrier modulation (DCM), the ± 1 bit stream of coded and interleaved binary serial baseband data ($\tilde{b}[k]$, $k \in \mathbb{N}_0$) are first grouped into groups of 200 bits. Later on, these 200 bits are grouped into 50 four-bit groups in the form of ($\tilde{b}[g(k)]$, $\tilde{b}[g(k)+1]$, $\tilde{b}[g(k)+50]$, $\tilde{b}[g(k)+51]$) where $k \in [0, 49]$ and $g[k]$ is defined as follows

$$g[k] = \begin{cases} 2k & k \in [0, 24] \\ 2k + 50 & k \in [25, 49] \end{cases}. \tag{1.7}$$

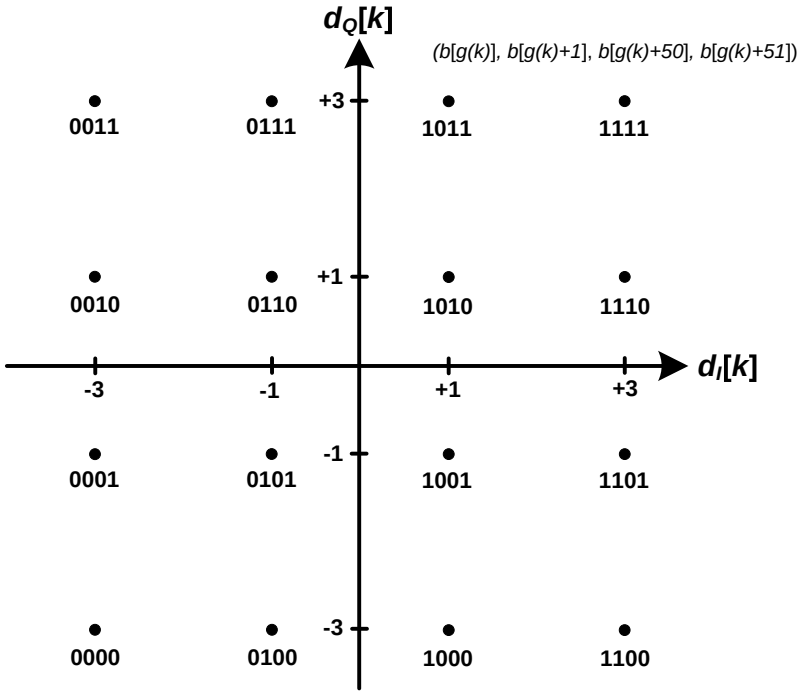
Each four-bit group is converted into two normalized complex numbers, $d[k]$ and

$d[k+50]$, using the following transform [2, 4]:

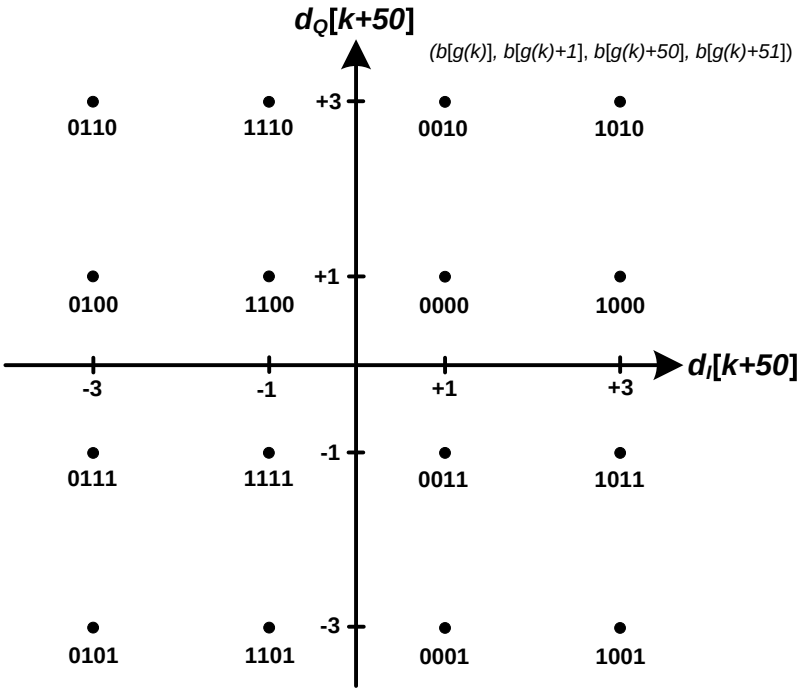
$$d[k] = K_{MOD_D}\Big[(2\tilde{b}[g(k)] + \tilde{b}[g(k)+1]) + j(2\tilde{b}[g(k)+50] + \tilde{b}[g(k)+51])\Big] \tag{1.8a}$$

$$d[k+50] = K_{MOD_D}\Big[(\tilde{b}[g(k)] - 2\tilde{b}[g(k)+1]) + j(\tilde{b}[g(k)+50] - 2\tilde{b}[g(k)+51])\Big] \tag{1.8b}$$

where $K_{MOD_D} = 1/\sqrt{10}$. $d[k]$ and $d[k+50]$ would be placed on two different subcarriers. The DCM mapping of $d[k]$ and $d[k+50]$are shown in Fig. 1.6(a) and Fig. 1.6(b), respectively.



(a)



(b)

Figure 1.6: DCM mapping (a) mapping for $d[k]$, (b) mapping for $d[k + 50]$.

1.3.3 Coexistence, Emission Limits, and Worldwide Regulations of MB-OFDM UWB

Figure 1.7 shows the narrowband wireless systems that exist in the vicinity of the UWB span or are overlapping with that [4, 5, 6]. As can be seen from this figure, certain wireless systems, such as WiMax and different variations of Wi-Fi, overlap with the spectrum of 3.1 - 10.6 GHz. Operation of a UWB device must not cause any performance degradation for other devices that use the UWB spectrum. In addition, UWB must not generate out of band spurs that can affect operation of systems outside the UWB spectrum.

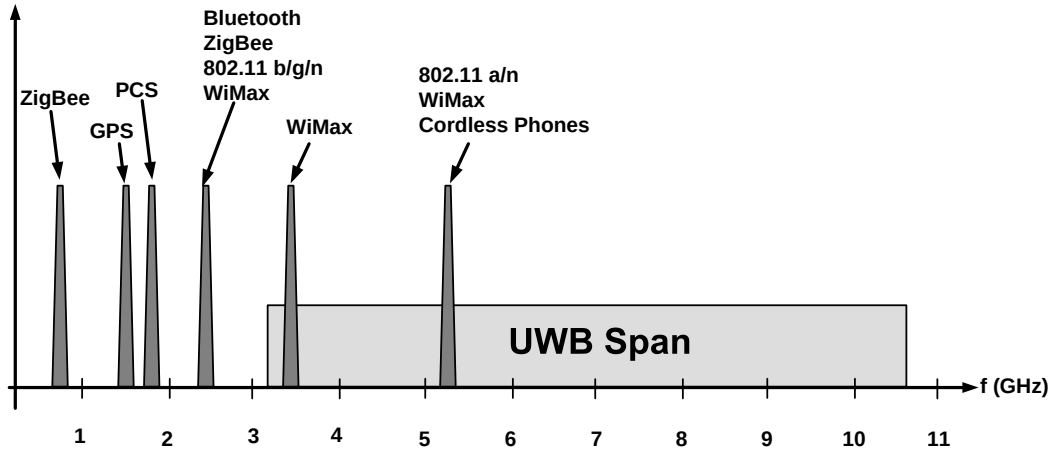


Figure 1.7: Frequency usage of the spectrum of 1 GHz to 11 GHz by wireless communication standards.

According to part 15 of Federal Communications Commission (FCC) regulations, the allowable transmitted signal power of any UWB device needs to be less than -41.3 dBm in 1 MHz bandwidth while using a bandwidth greater than 500 MHz [1]. In addition, the maximum equivalent isotropically radiated power (EIRP) for the operation of indoor and hand held (outdoor) UWB devices are specified by FCC and is depicted in Fig. 1.8.

The worldwide regulation of the spectrum of 3.1 GHz to 10.6 GHz is shown in Fig. 1.9 [2, 7]. As can be seen from Fig. 1.9, this 7.5 GHz of bandwidth is unlicensed in the United States, but not available worldwide. Only band group six is available

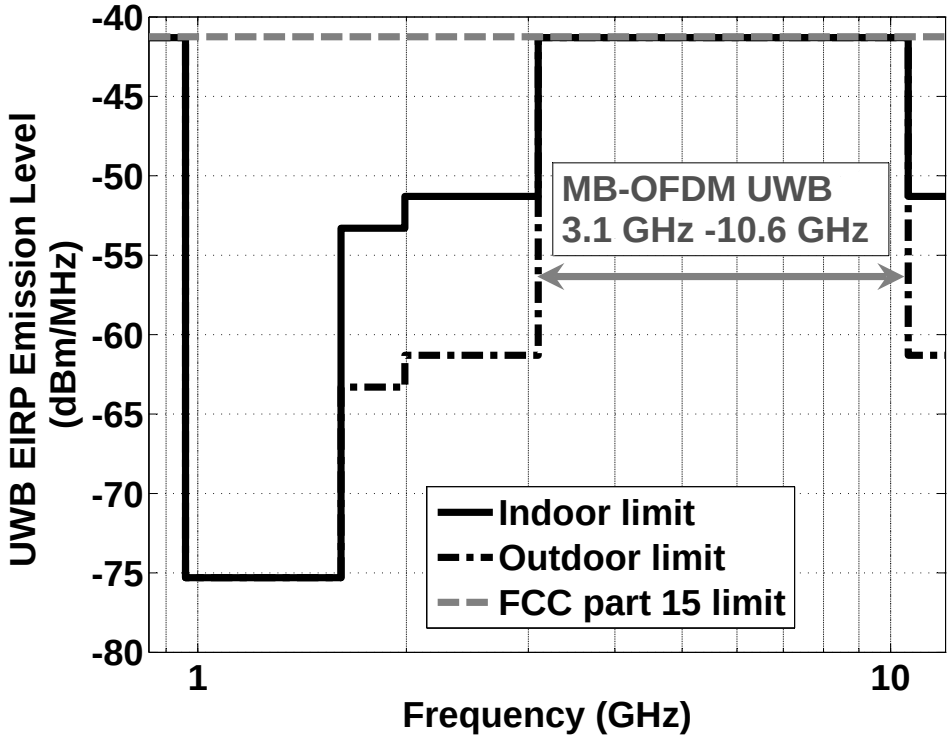


Figure 1.8: Emission for MB-OFDM UWB.

worldwide. As a result, all the UWB devices need to support band group six. However, band eleven requires detection and avoid (DAA) for operation in Europe.

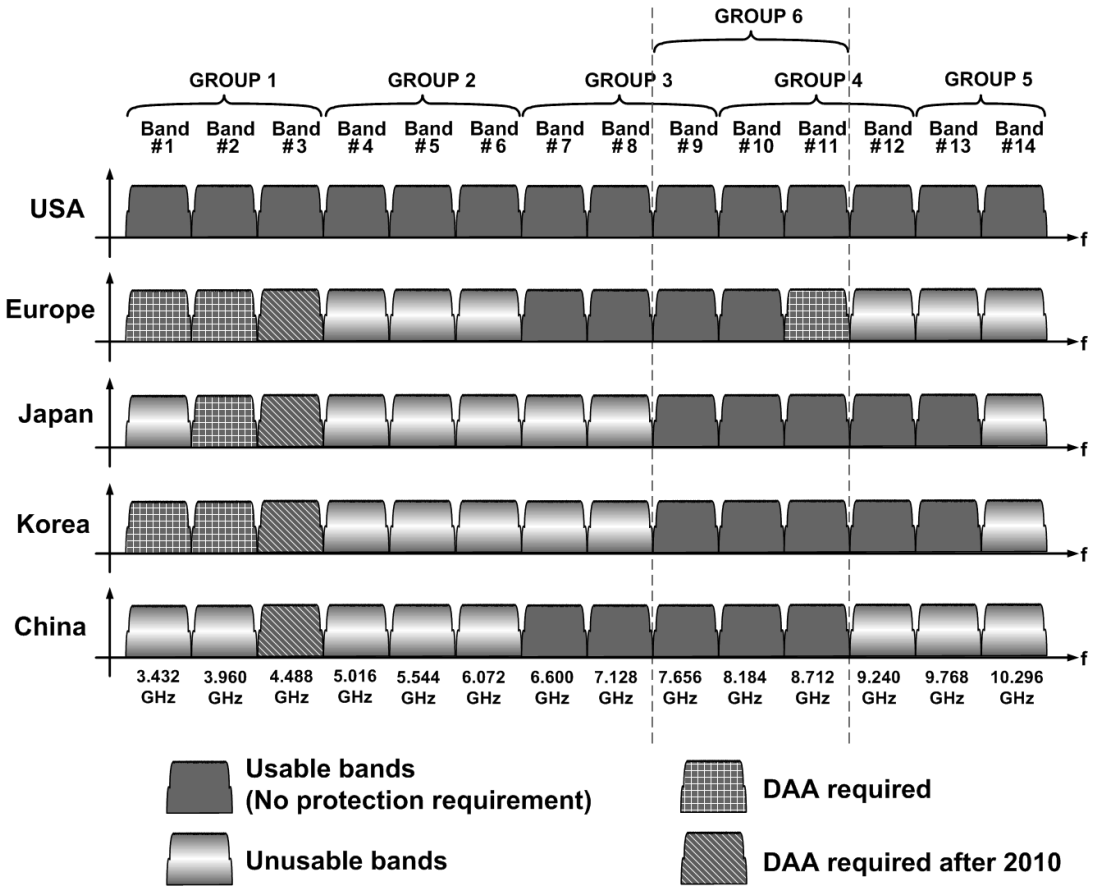


Figure 1.9: Worldwide regulatory for MB-OFDM UWB.

1.3.4 Detection and Avoid

In general, the operation of an ultra-wideband device must not causes any degradation in the quality of service of another wireless data networks, such as WiMax or Wi-Fi. As shown in Fig. 1.9, certain bands require Detection and Avoid (DAA) which means detecting activity of another communication service, a WiMax mobile terminal for instance, and avoiding any performance degradation caused by the operation of an UWB device. An example of destructive interference between UWB and WiMax in

home applications is depicted in Fig. 1.10.

A detection technique based on Fast Fourier Transform (FFT) to measure the LO leakage of a WiMax mobile terminal is presented in [8]. After detecting the activity of a WiMax mobile terminal, some actions need to be taken to avoid performance degradation of the WiMax terminal due to the activity of a UWB device. There are several options to avoid performance degradation of the detected mobile terminal including controlling the transmit power of UWB device, frequency notching, and active interference control [9]. Any UWB device needs to provide support for transmit power control (TPC) to minimize the transmit power spectral density and yet providing a robust link to transfer data.

On the other hand, some mechanism are provided in the PHY layer to allow nulling individual OFDM sub-carriers [2]. These mechanisms along with the choice of the appropriate channels in each band group provide controlling the spectrum and allow coexistence of UWB with other radios in that spectrum. An example of sub-carrier nulling in MB-OFDM UWB is shown in [10].

1.4 Frequency Synthesizer for MB-OFDM UWB

A block diagram of a typical UWB transceiver is shown in Fig. 1.11. One of the main challenges in the design of a transceiver for UWB is to achieve a wide bandwidth with low power consumption and small die area.

One of the main challenges in the design of any UWB radio is to provide a hardware-efficient fast hopping frequency synthesizer that can implement the center frequencies expressed by (1.2). As specified in Section 1.3, a UWB synthesizer frequency hops every 312.5 nS (hopping rate of 3.2 MHz) and the allotted time for a UWB synthesizer to perform the band switching is only 9.5 nS. This fast settling time poses several design challenges on the synthesizer for MB-OFDM UWB.

Moreover, to prevent the bit error rate (BER) degradation, system simulations show that the in-band spurs must be as low as -30 dBc. Additionally, for coexistence with Wi-Fi, the spurious tones at 2.4 GHz and 5 GHz need to be smaller than -45 dBc and -50 dBc, respectively.

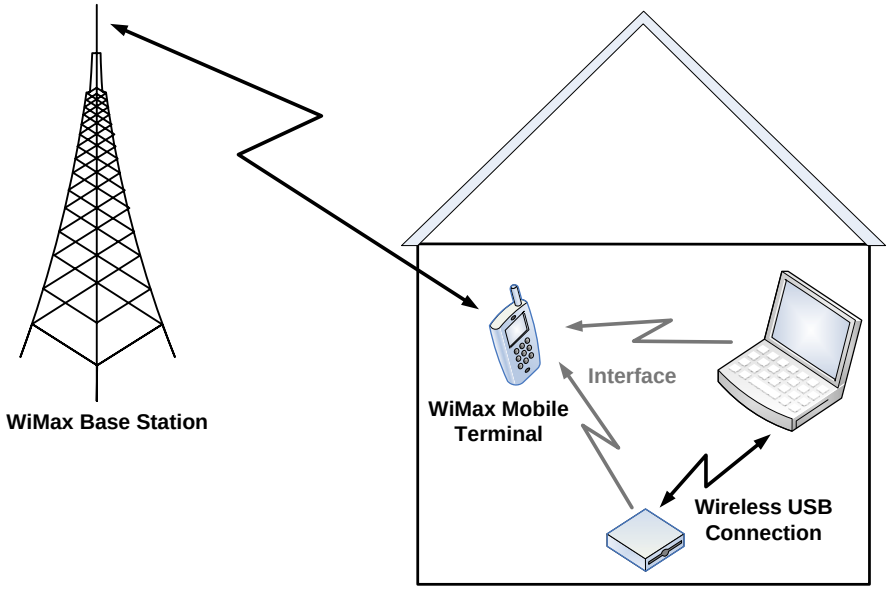


Figure 1.10: An example of destructive interference in coexistence of WiMax and UWB.

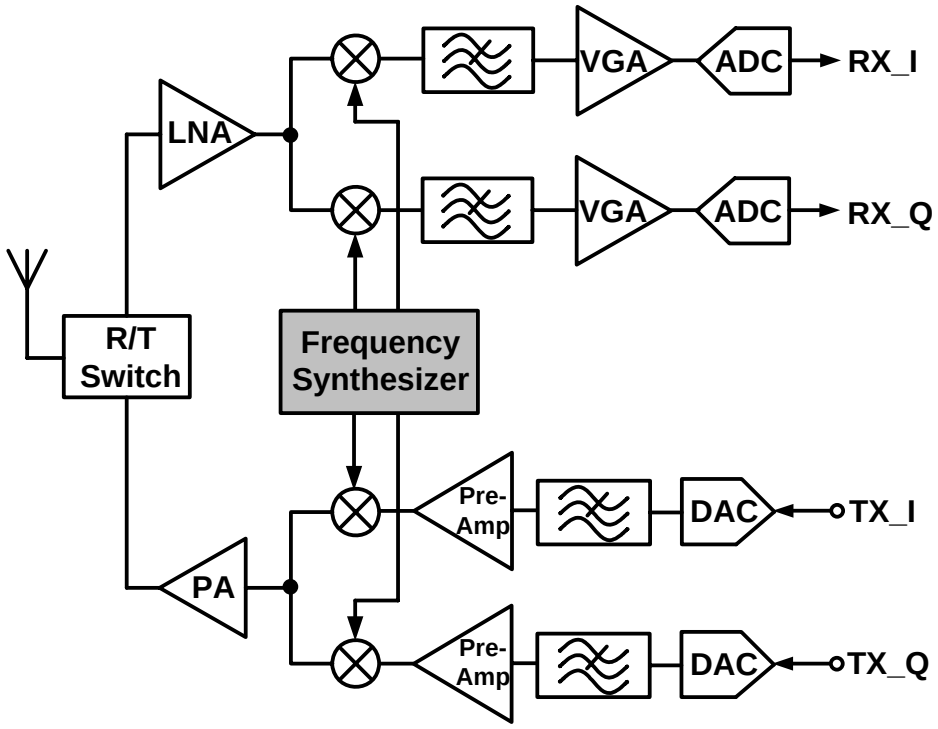


Figure 1.11: A typical UWB transceiver.

It is also revealed from system simulations that a phase noise of better than -100 dBc/Hz at 1 MHz offset is required. In addition, the transmitted center frequency needs to be accurate within $\pm$20 ppm [2]. Furthermore, quadrature 50% duty cycle outputs are needed for proper operation of SSB mixers of Fig. 1.11.

Figure. 1.9 suggests that the MB-OFDM UWB frequency synthesizer needs to cover all fourteen-bands specified by (1.2) in order to have a universal UWB solution.

Meeting all these specification for the UWB frequency synthesizer in a digital CMOS technology using low power consumption and small chip area requires appropriate frequency planning and novel circuit design techniques. Accordingly, implementing this block would be the main focus of this dissertation.

1.5 Frequency Synthesis Techniques

In this section, traditional frequency synthesis techniques, such as using a direct digital frequency synthesizer (DDFS) or a phase-locked loop (PLL) are previewed, and compared, and an architecture suitable to implement a fast settle fourteen-band synthesizer that meets the specification stated in Section 1.4 is chosen.

1.5.1 Direct Digital Frequency Synthesizer

A block diagram of a Direct Digital (DDFS)-based frequency synthesizer for MB-OFDM UWB is shown in Fig. 1.12. It consists of a DDFS and an SSB mixer for frequency translation. A DDFS is composed of an accumulator, a ROM-based lookup table, and a digital to analog converter (DAC). If an R-bit accumulator is used, the output of the accumulator is a discrete-time ramp with mean frequency of $f_{out} = W(t)/Nf_{clk}$ where $N = 2^R$ [11]. As a result, based on the input frequency word ($W(t)$), the output of the accumulator is at a frequency which is a fraction of a master clock. Using this way one can generate channel spacing, or multiples of channel spacing, from a higher frequency clock.

As can be seen in Fig. 1.12, the accumulator is followed by a sine lookup table that converts the ramp output of the accumulator into a discrete-time sine wave. Fi-

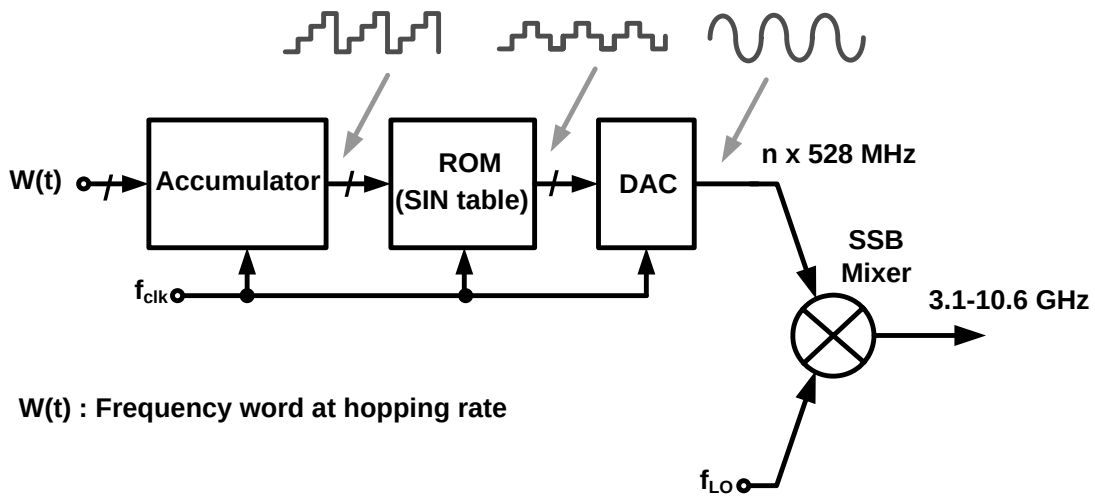


Figure 1.12: Block diagram of a direct digital frequency synthesizer (DDFS) for UWB.

nally, the DAC generates a continuous time waveform suitable for frequency translation applications.

A DDFS can achieve a very fast switching time. However, implementing a DDFS for UWB requires high-speed digital circuits, which would have very high power consumption, and very difficult to be implemented in today's CMOS technology. On the other hand, another challenge is to mitigate the spurious tones at the output of a DDFS [11]. Moreover, the architecture of Fig. 1.12 requires a linear SSB mixer, to suppress the mixing spurious response at the output. Implementing a linear SSB mixer in a low-voltage CMOS process poses several challenging design constraints, and generally increases the power consumption. In addition, an SSB mixer requires quadrature phases of both mixing signals with sufficiently good amplitude and phase accuracy to achieve adequate side-band cancellation. However, using an SSB mixer seems to be inevitable in a fast hopping frequency synthesizer, as would be discussed later.

High-speed logic requirement makes the architecture of Fig. 1.12 attractive only to cover one band group, and makes it very difficult for this architecture to cover a wider span.

1.5.2 Phase-Locked Loop Based Approaches

A phase-locked loop (PLL) can directly generate all required frequencies without any additional frequency translation, such as SSB mixers. Nonetheless, stringent settling requirement forces the reference frequency of the PLL to be extremely high. Consequently, the phase detection need to be done at frequencies beyond the capability of current device technologies. For instance, the reference frequency to a PLL needs to be higher than 10 GHz to achieve a settling time of 9.5 nS [12]. In addition, a fractional-N PLL would be required to obtain the channel spacing of 528 MHz out of that reference frequency. These limitations make any single PLL approach unfeasible.

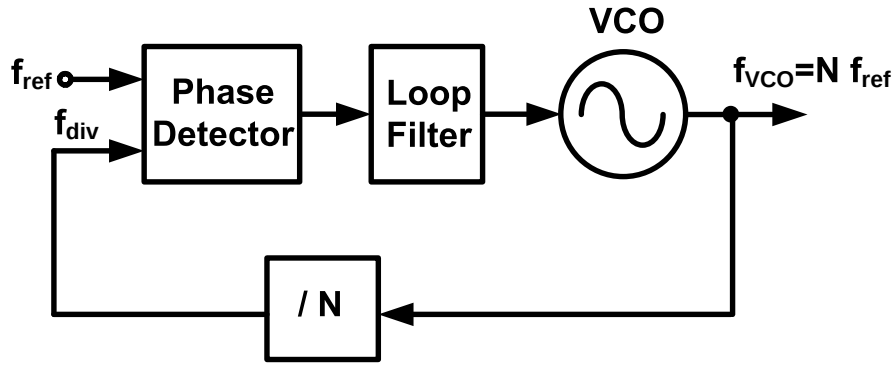


Figure 1.13: Block diagram of a PLL-based frequency synthesizer for UWB.

A couple of approaches have been suggested to overcome the stringent settling requirement of a PLL for UWB frequency synthesizer.

One technique is based on using a dedicated fixed-frequency PLL for each band. Consequently, there would be no settling problem. In addition, this technique does not require any SSB mixer, hence there is no mixer related linearity and spurious problem. An example of this method to generate center frequencies of band group 1 is presented in [12]. Another example is the synthesizer of [13] that requires three separate PLL's to synthesize center frequencies of band groups one and three. However, using a dedicated PLL for each band becomes impracticable to cover large number of bands due to practical problems of having several voltage controlled oscillators (VCO's) on one chip, such as VCO pulling.

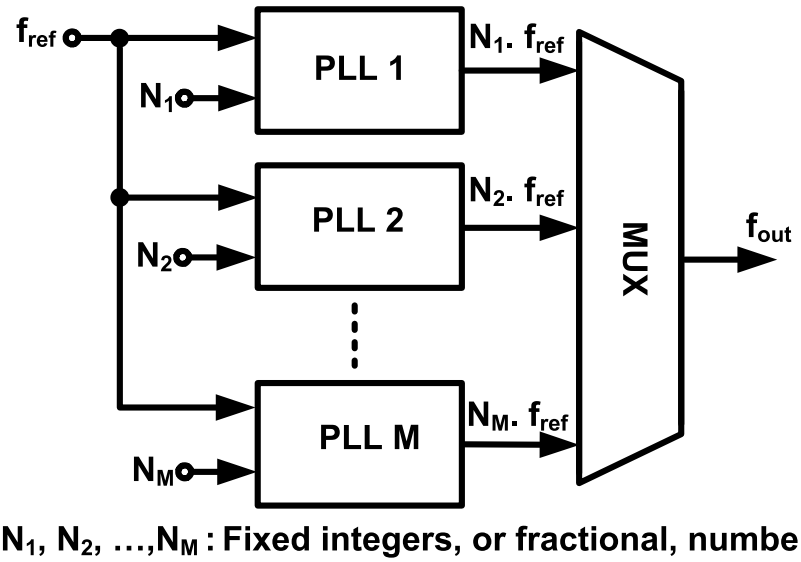


Figure 1.14: Block diagram of a UWB frequency synthesizer based on multiple fixed-frequency PLL's.

Another architecture presented in [14] is based on using two fast settle PLL's. In this technique, each PLL has 312.5 nS to settle (one symbol period) instead of 9.5 nS. As a result, it is feasible to implement a phase detector and a charge pump that operate at that speed, as shown in [14].

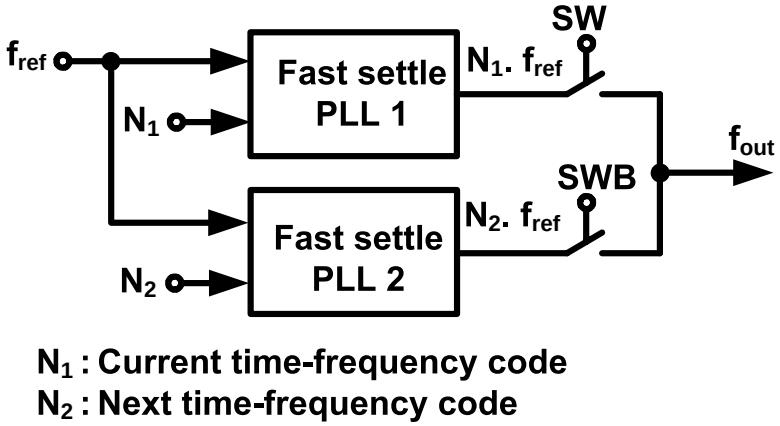


Figure 1.15: Block diagram of a frequency synthesizer for UWB based on two fast settle PLL's.

A simplified block diagram of this technique is shown in Fig. 1.15. As can be seen from this figure, this synthesizer does not require any SSB mixer, hence there is no

mixer related linearity problem. However, it is very difficult to expand this architecture to cover the entire UWB span since the VCO's cannot cover such wide frequency range. On top of that, extending the frequency range of a VCO usually leads to degradation of its phase noise. As a result, the architecture of Fig. 1.15 cannot be used to implement a 14-band UWB frequency synthesizer.

1.5.3 Sub-harmonic Injection-Locking Technique

One alternative way to overcome the PLL's settling time limitations is based on using a stand alone oscillator, and injection-locking it to an appropriate frequency. In this technique, the oscillator can be injection-locked to a low phase noise reference signal that is a sub-harmonic of the desired frequency. In general the reference frequency needs to be a common divisor of all the output frequencies. A simplified block diagram of this technique is shown in Fig. 1.16 [15].

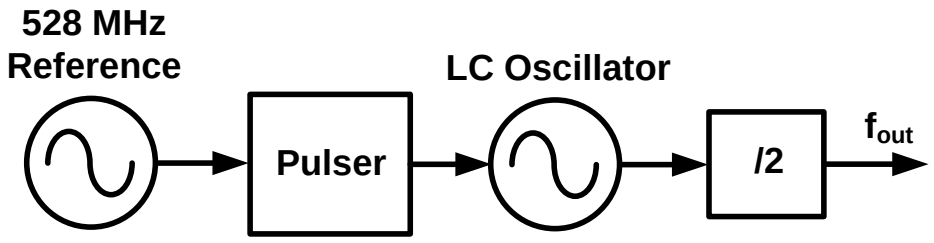


Figure 1.16: Block diagram of a frequency synthesizers for UWB based on frequency division and mixing.

The synthesizer of [15] is implemented using an LC oscillator followed by a divide-by-2 for quadrature generation. The oscillator is sub-harmonic injection-locked to an external 528 MHz reference signal external. It generates the center frequencies band group six, and achieves a settling time of 4 nS. However, this technique requires aggressive filtering to suppress the unwanted spurious tones. In addition, it is not easy to extend this to cover the entire UWB span.

1.5.4 Techniques Based on Polyphase Filtering

Another technique to solve the agility problem of the frequency synthesizer is by doing the band selection in baseband or a low intermediate frequency (IF) [16]. This scheme uses a fixed frequency quadrature carrier (the center frequency of the middle band of a given band group) to downconvert the entire band group with the middle band centered at DC. A fast-hopping polyphase filter is used to select the negative frequency band or the positive frequency band. Band selection is performed by feeding the appropriate quadrature sequence (clockwise or counter-clockwise) to the polyphase filter. The polyphase filter can also be bypassed to pass the middle band of the group. A high-speed ADC followed by digital processing can recover the band of interest.

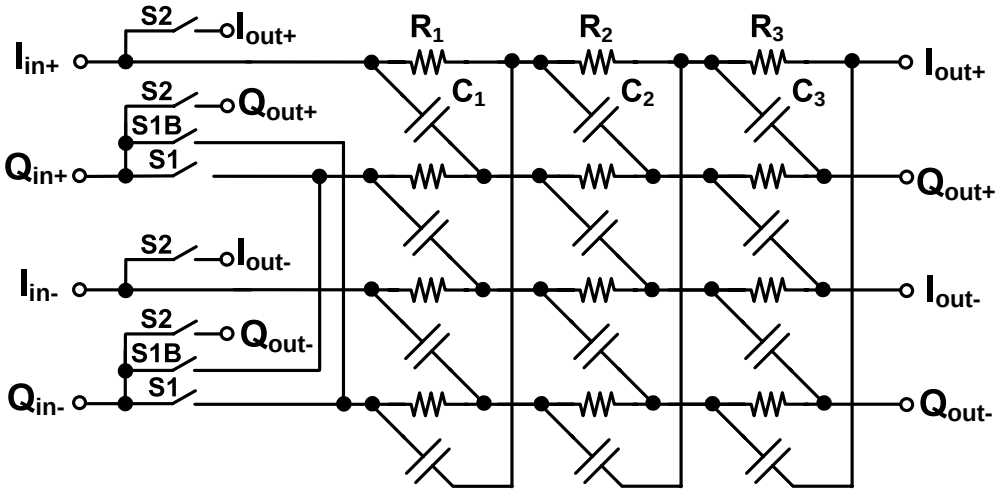
The synthesizer used in the transceiver of [16] covers band group three, and uses a fixed frequency PLL to generate the center frequency of band eight (7.128 GHz). It uses the fast-hopping polyphase filter of Fig. 1.17(a) to select a band of interest. The principles of operation is shown in Fig. 1.17(b). The polyphase filter is followed by a 1 GS Analog-to-digital converter (ADC). The ADC undersamples the downconverted signal. Final downconversion to DC for bands seven and nine will be done after analog-to digital conversion in digital domain.

The synthesizer presented in [16] eliminates the use of SSB mixers in the synthesizer path and does not suffer from mixing spurious tones. However, due to limitations in the speed and dynamic range of ADC's, it is very difficult for this architecture to cover more than one band group using a single fixed frequency PLL.

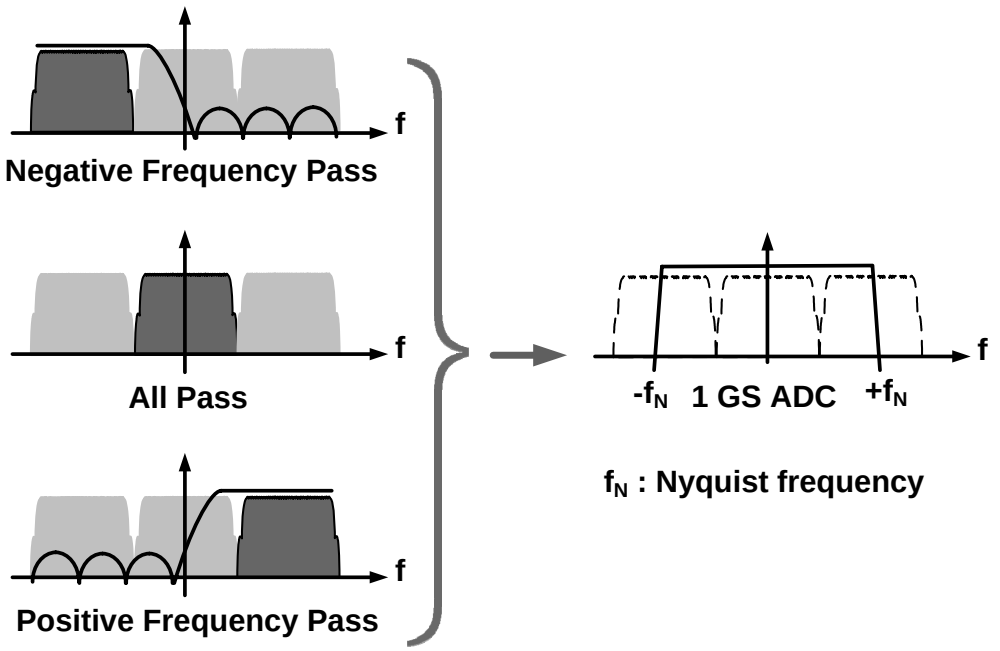
1.5.5 Frequency Division and Mixing

Another architecture that can be used to implement a frequency synthesizer, is a hybrid architecture shown in Fig. 1.18 where a combination of fixed frequency PLL's, frequency dividers, and SSB mixers are required. In this architecture, all the MB-OFDM UWB carriers are generated by combination of frequency division and SSB mixing. Accordingly, this technique alleviates the challenging settling requirement of the PLL.

The architecture of Fig. 1.18 can achieve a very fast switching time, as low as 1



(a)



(b)

Figure 1.17: (a) Schematic of a fast-hopping polyphase filter, and (b) principles of operation. By feeding the appropriate quadrature sequence, the polyphase filter can pass the positive, or negative, frequency band.

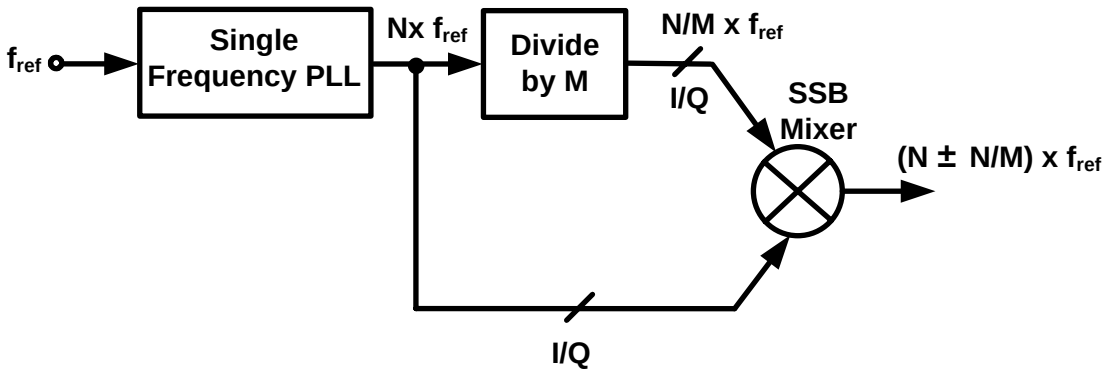


Figure 1.18: Block diagram of a frequency synthesizers for UWB based based on frequency division and mixing.

nS. In addition, it can cover the entire UWB span. However, the main drawback of this architecture is in using SSB mixers. As was discussed in Section 1.5.1, using SSB mixers implies availability of quadrature phases of both the mixing signals with sufficiently good amplitude and phase accuracy to achieve adequate side-band cancellation. On the other hand, every mixing stage introduces multiple spurious tones. Mixer linearization, and appropriate frequency planning can lead to spurious response. However mixer linearization reduces the conversion gain, and it will require additional power consumption to achieve same voltage swing at the mixer output.

A generalization to the architecture of Fig. 1.18 using two SSB mixers is shown in Fig. 1.19. The main challenge in implementing the architecture of Fig. 1.19 is to achieve a hardware efficient design compatible with digital CMOS technology.

For instance, the synthesizer of [17] requires two PLL's and one level of SSB mixing to generate the center frequencies of band group one. Another example is the frequency synthesizer of [18] which uses two separate PLL's and one SSB mixer to generate seven band center frequencies of MB-OFDM UWB (the old band allocation [19]).

The architecture of Fig. 1.19 is used in the majority of UWB frequency synthesizers that cover more than one band group, such as [20], and in most of the 14-band UWB frequency synthesizers [21, 22], due to flexibilities in covering a wide frequency range and overcoming the settling issues.

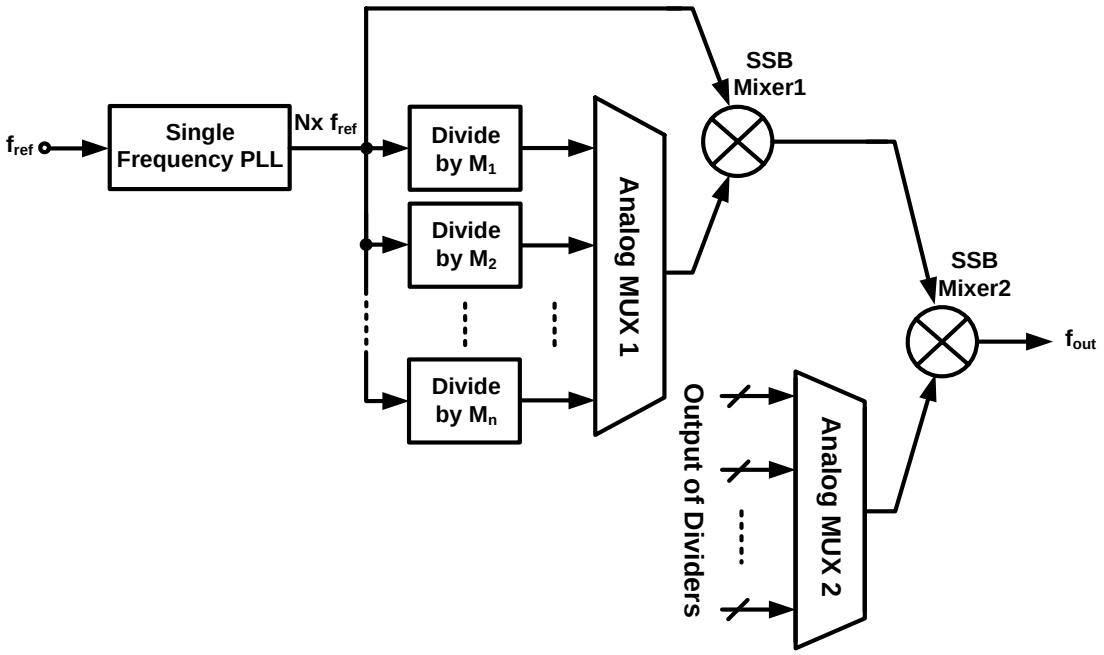


Figure 1.19: Block diagram of a frequency synthesizers for UWB based on frequency division and mixing.

1.6 Dissertation Organization

In this dissertation, different architectures for implementing a frequency synthesizer for MB-OFDM UWB are studied, and an architecture suitable to implement a 14-band synthesizer for MB-OFDM UWB in digital CMOS technology is introduced. A hardware efficient implementation of a 14-band frequency synthesizer based on the architecture of Fig. 1.19 may require use of fractional frequency dividers as well as injection-locked frequency dividers (ILFD's). Therefore, this dissertation contains some analysis of injection-locked frequency dividers and semi-dynamic regenerative frequency dividers which can be used to generate fractional frequency dividers. Moreover, quadrature signals are required for proper operation of the SSB mixers in this architectures.

Chapter 2 includes an overview of quadrature generation at microwave frequencies using ring-oscillators. Furthermore, it consists of locking range comparison of multi-modulus injection-locked frequency dividers that can combine the frequency division and quadrature generation. An injection-locked multi-modulus four-stage ring-oscillator-based frequency divider is presented as an example. This frequency divider is

implemented in 0.13 μm CMOS, and the measured data for locking range agrees with predictions.

A comparison of the techniques to implement frequency dividers with fractional division ratios is presented in Chapter 3. Moreover, this chapter presents a detailed study of the operation and stability of semi-dynamic regenerative frequency dividers for the first time, which provides a better understanding of the steady-state operation, locking range, and phase noise of this group of frequency dividers. For our analysis, driving the locking range and output phase noise of this frequency divider, required the locking range and free-running phase noise of the two-stage ring-oscillators. Therefore, some part of this chapter is devoted to study the free-running and injection-locked behavior of the two-stage ring-oscillators-based on negative-resistance delay cells. These analysis are presented for the first time. Moreover, a design example along with design considerations to obtain a 50% quadrature output fractional division ratio is presented. All the calculation are compared with circuit simulations and show great agreement.

Chapter 4 presents the design of the first inductor-less, fourteen band, fully quadrature frequency synthesizer for MB-OFDM UWB in a 0.13 μm CMOS technology. An inductor-less design methodology is introduced and techniques for spurious tones mitigation, such as SSB mixing, polyphase filtering, and low-voltage linearization techniques, in the absence of tuned inductive circuits are discussed. This chapter also contains of some analysis of the frequency response of multi-stage RC polyphase filters.

Finally, Chapter 5 concludes the this dissertation, and presents some suggestion for further improvement of the performance metrics.

Chapter 2

Frequency Division and Quadrature Generation at Microwave Frequencies

2.1 Introduction

High-speed frequency dividers are key building blocks in the implementation of high-frequency Phase Locked Loops (PLL's). There have been many efforts to implement low power, area efficient, frequency dividers for V-band [23, 24]. Implementing dividers with division ratios of larger than two can ease frequency synthesis at high frequencies and reduce power consumption and die area. Static frequency dividers work well up to a fraction of the transition frequency (f_T), and above that limit, their power consumption becomes extremely high. Moreover, they require a large signal swing, which is not easy to achieve at frequencies close to f_T. In addition, static frequency dividers usually achieve a division ratio of two, and to achieve larger division ratios, a cascade is required.

Injection-locked frequency dividers can work at higher frequencies compared to static frequency dividers. However, they usually suffer from a narrow input frequency locking range. Several groups have reported regenerative, or injection-locked, dividers working at frequencies up to 70 GHz [23] - [25]. However most designs cannot supply quadrature phases at the output. Furthermore, these architectures are inductor-based, which may require a large die area.

The goal of this work is to implement multi-phase frequency dividers capable of operating at frequencies close to f_T with division ratios of larger than two. For compatibility with digital CMOS technology, the frequency divider must be able to operate at supply voltages as low as 1.2 V, and an inductor-less design methodology is adopted which leads to a smaller die area. But the power consumption of such an approach may be higher in the absence of tunable circuits and inductors.

2.2 Injection-Locked Frequency Divider Design

As was mentioned earlier, the goal of this work is to achieve both frequency division and multiple phases of output at microwave frequencies. Because of its practical importance, our focus is mainly on achieving quadrature outputs at the output of frequency dividers.

There are certain techniques to generate quadrature output phases, including filter-based techniques, e.g. using a high-order polyphase filters to generate quadrature outputs, and ring-oscillator-based techniques.

In filter-based techniques, the frequency divider is followed by a multi-phase filter. As a result, the frequency division and quadrature generation are not performed at the same time. Another limitation of this method is the insertion loss of on-chip filters that can leads to significant loss of signal. Consequently, post-filtering amplification is required which adds to the power consumption and area.

On the other hand, techniques that are based on using a ring-oscillator-based frequency divider can obtain multiple phases of the output and frequency division at the same time. Proper choice of the number of stages can provide the desired output phases. An N-stage ring-oscillator provides introduce a phase shift of π/N per stage at its self resonance oscillation frequency. As a result, a two-stage or a four-stage ring-oscillator is required to obtain quadrature output phases.

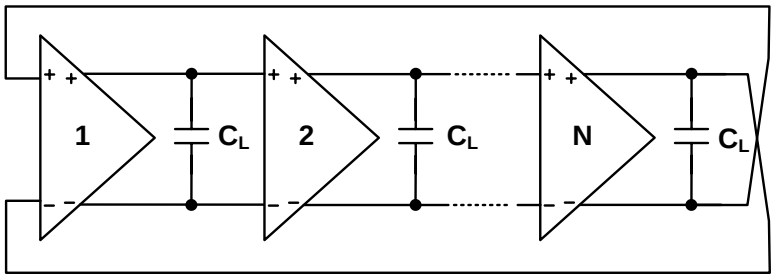
Barkhausen criteria for the loop gain of oscillators puts a minimum required gain per stage in any ring-oscillator, and this requirement is more relaxed for a four-stage oscillator than a two-stage ring-oscillator. This becomes more important when moving to higher frequencies, and it would justify using four-stage ring-oscillators. Therefore,

in this section, we concentrate on ring-oscillators with more than two stages to combine the frequency division and quadrature output generation. Two-stage ring-oscillators are studied in details in Section3.5.

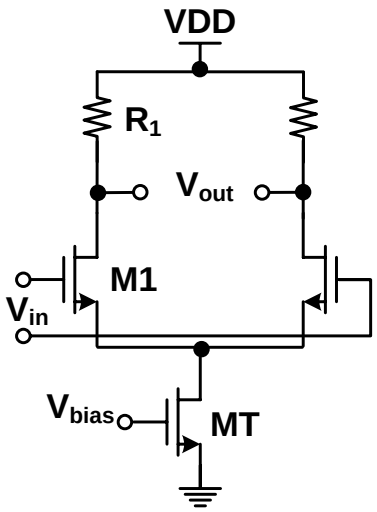
Consider an N-stage ring-oscillator (Fig. 2.1(a)). As shown in [26], the oscillation frequency of the ring-oscillator is given by

$$f_{osc} \approx \frac{1}{2NR_LC_L \ln 2} \tag{2.1}$$

where R_L and C_L are respectively the equivalent resistance and capacitance at the output of each delay cell.



(a)



(b)

Figure 2.1: (a) N-stage ring-oscillator, (b) resistive load differential pair delay cell.

At the oscillation frequency, each stage must introduce a phase shift of π/N to

satisfy the criteria for oscillation. This ring-oscillator can be implemented using the differential pair delay stage with resistive load shown in Fig. 2.1(b). However, more than two delay stages are required to meet the phase shift requirement.

Here, we generate quadrature phases at the output, so a ring oscillator is required with at least four delay stages, when the delay stage in Fig. 2.1(b) is used. Increasing the number of stages beyond four increases the area and power dissipation, and reduces the achievable Self-Resonance Frequency (SRF).

To analyze injection-locking in ring-oscillators, we use the nonlinear ILFD model introduced in [27], which is shown in Fig. 2.2. The input signal is injected to the tail current source of the first delay stage of the ring-oscillator, which is modeled as a single-balanced mixer. The function $f(.)$ models the nonlinearity caused by the differential pair in commutating the tail current. The nonlinearity of $f(.)$ introduces harmonics of ω_o prior to mixing. In this case, the current at the mixer output (drain current of M1 in Fig. 2.1(b))can be written as

$$I_D = g_m A_{inj} \sin(\omega_{inj} t + \phi_{inj}) f(V_O) \tag{2.2}$$

where g_m is the transconductance of the tail current source (MT) in Fig. 2.1(b). For simplicity, the LO-to-output leakage of the single balanced mixer is not considered in (2.2). It can be shown that this term does not contribute to the locking range or division ratio of the ILFD.

Since V_O is a periodic signal, $f(V_O)$ can be expressed using a Fourier series expansion of the harmonics

$$f(V_O) = \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_o t} \tag{2.3}$$

where a_k coefficients are the Fourier coefficients of the output. If V_O is large enough, has a 50% duty cycle and the nonlinearity of the $f(.)$ has odd symmetry, and we can estimate $f(.)$ by a ± 1 square wave. In this case, the differential output current of the mixer can be expressed as

$$I_D = \sum_{k=1}^{\infty} (\pm) \frac{2 g_m A_{inj}}{(2k-1)\pi} \cos[\omega_{inj} t + \phi_{inj} \mp (2k-1)\omega_o t] \tag{2.4}$$

The LPF removes the high-frequency mixing components, and only those that satisfy the following condition survive.

$$|\omega_{inj} - (2k-1)\omega_o| = \omega_o \tag{2.5}$$

Assuming $\omega_{inj} > (2k-1)\omega_0$ (low side injection in the mixer), it can be concluded that

$$\frac{\omega_o}{\omega_{inj}} = \frac{1}{2k} \tag{2.6}$$

The ILFD must be locked to the $2k^{th}$ harmonic of its SRF. In this case, ω_{inj} and the $(2k-1)^{th}$ harmonic of the SRF (ω_0) satisfy (2.5). On the other hand, the $(2k+1)^{th}$ harmonic of the SRF, which corresponds to high-side injection in the mixer, also satisfies (2.5). Therefore, after low-pass filtering, (2.4) can be simplified as follows.

$$I_D \cong \frac{4g_m A_{inj}}{\pi(4k^2-1)}\left(2k\cos\phi_{inj}\cos\omega_o t - \sin\phi_{inj}\sin\omega_o t\right) \tag{2.7}$$

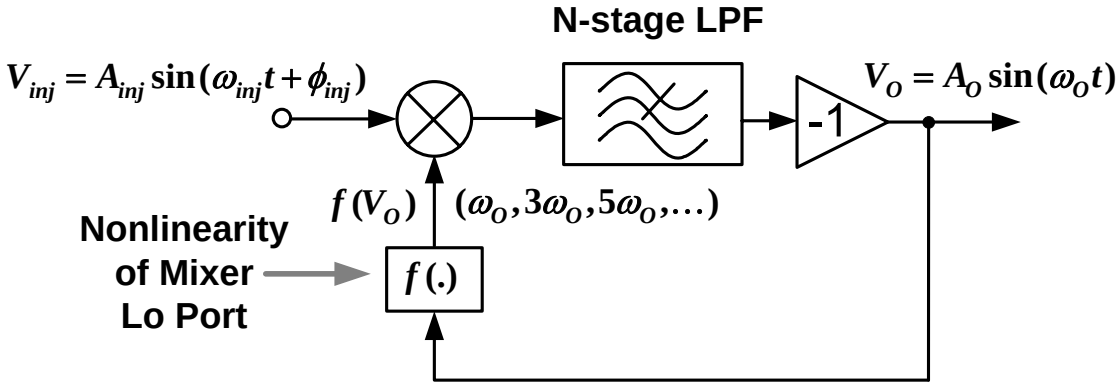


Figure 2.2: Nonlinear model for ring-oscillator-based ILFD.

The upper limit of the mixer output current derived in (2.7) is therefore

$$|I_{D_{max}}|_{\omega=\omega_o} < 4g_m A_{inj}\frac{2k}{\pi(4k^2-1)} \tag{2.8}$$

As can be seen in (2.7) and (2.8), the mixer output current drops inversely with the division ratio. This leads to a reduction of the input sensitivity of the ILFD when

injection-locked to higher-order harmonics of ω_o. This leads to the well-known narrower input frequency range for larger division ratios. In this work, we use a tuning mechanism to compensate for this problem.

2.3 Circuit Implementation

The quadrature output ring-oscillator-based ILFD is shown in Fig. 2.3. It consists of four delay stages. This divider generates eight different phases of the output signal.

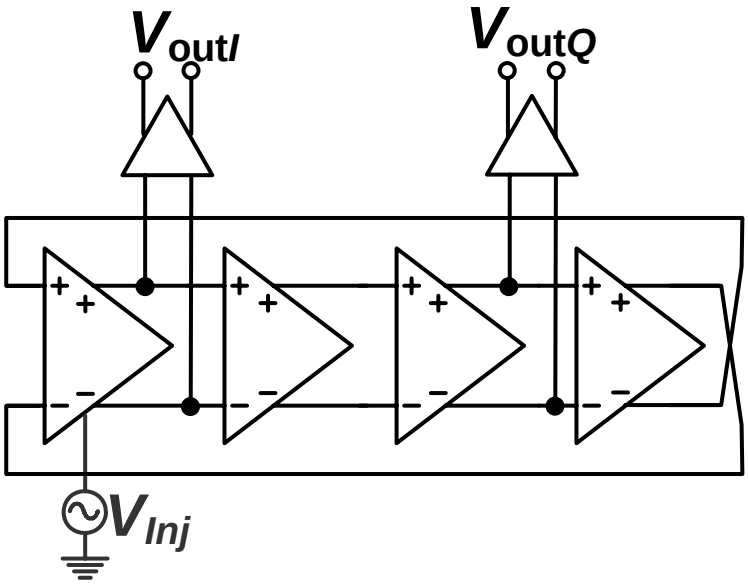


Figure 2.3: Four stage ring-oscillator-based ILFD.

Compared to two or three-stage ring-oscillators, a four-stage ring-oscillator relaxes the gain requirement of each stage to meet the loop gain criteria. As a result, a smaller load resistor is used in the delay cell, which will allow the ring-oscillator to achieve a higher self-resonance frequency, but this will increase the required power consumption to achieve the desired voltage swing. As was discussed in Section 2.2, the ILFD needs some tuning mechanism to overcome the narrow locking range problem. An additional tuning element will add some parasitics, and limit the maximum achievable SRF, so the SRF is tuned by changing the bias current of each delay cell. Changing

the bias current directly affects the output impedance of each cell, which changes the SRF of the ring-oscillator, as expressed by (2.1).

2.4 Measurement Results

This frequency divider is implemented in an IBM 0.13μm CMOS technology. Input sensitivity curves at different division ratios are plotted in Fig. 2.4. This ILFD achieves a locking range of roughly 5.5 GHz when operated as a divide-by-two, a locking range of 1.4 GHz when operated as a divide-by-four, and 1 GHz for divide-by-six mode.

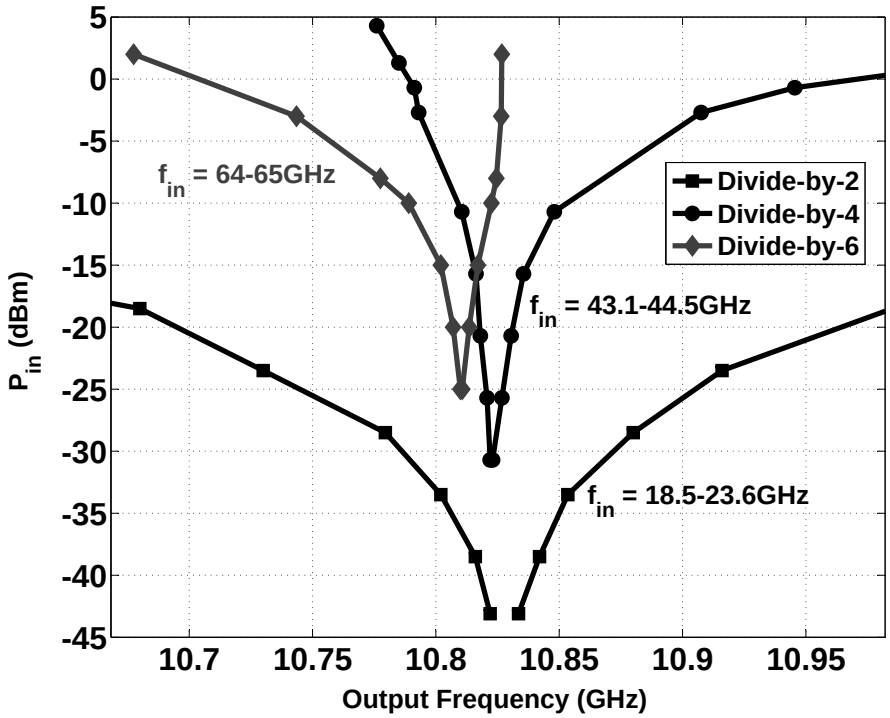


Figure 2.4: Measured input sensitivity curves for different modes of operation.

The measured time domain waveforms of the input and output of the frequency divider for different division ratios are shown in Fig. 2.5 . In all these measurements, a single ended input is applied to the ILFD. In Fig. 2.5(a), the input is at 17.5 GHz and the ILFD achieves division ratio of two. Similarly in Fig. 2.5(b) and Fig. 2.5(c)

division ratios of four and six are achieved for input signals at 38.8 GHz and 64.6 GHz, respectively.

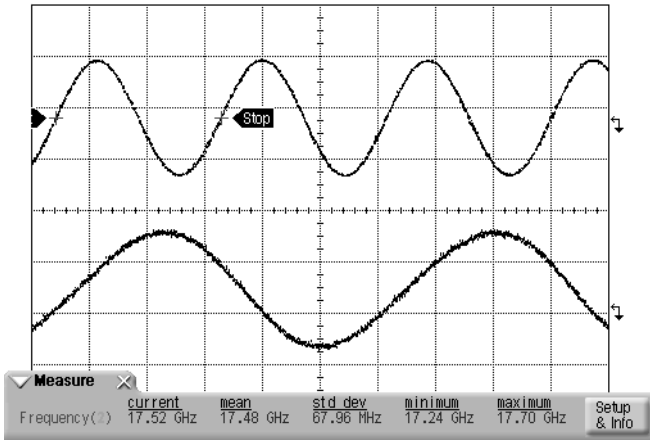
The differential quadrature phases of the output when the ILFD is operating as a divide-by-6 are shown in Fig. 2.6. The I/Q phase and amplitude mismatch are roughly 4 degrees and 0.5dB for a 55 GHz input.

Tuning curves of this ILFD for operation in the divide-by-six mode are shown in Fig. 2.7. Although these curves are plotted for 50mV steps in VDD, this tuning can be done continuously. These curves show the possibility of extending the effective input range of the ILFD to 51-65 GHz. Moreover, this tuning capability provides sufficient margin to compensate for process variations.

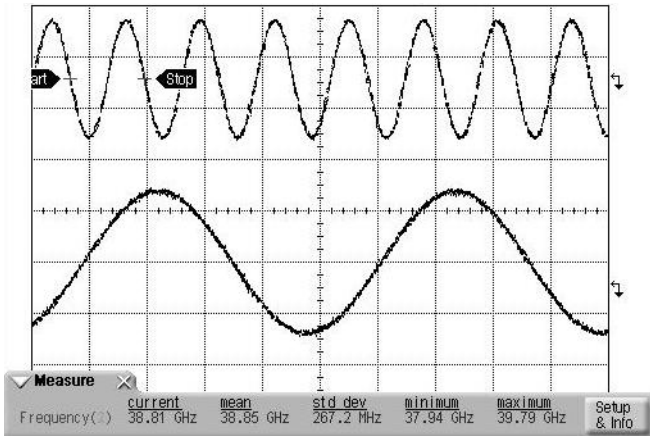
The phase noise of the free-running ILFD and the phase noise of the ILFD under locked conditions for a 17.5 GHz input are plotted in Fig. 2.8. Despite the poor phase noise of ring-oscillators, they track the phase noise of the input source when they are injection-locked [28]. This ILFD achieves phase noise of -104 dBc/Hz and -116dBc/Hz at 10 kHz and 1 MHz offset respectively.

Figure 2.9 shows the measured SRF and the measured phase noise of the ILFD, when operated as a divide-by-six, for different values of external tuning. As is shown in this figure, the phase noise is better than -110 dBc/Hz at 1MHz offset for all the values of external tuning.

The performance of this ILFD is compared with other published CMOS V-band frequency dividers, and is summarized in Table 2.1. Figure 2.10 shows the chip microphotograph.



(a)



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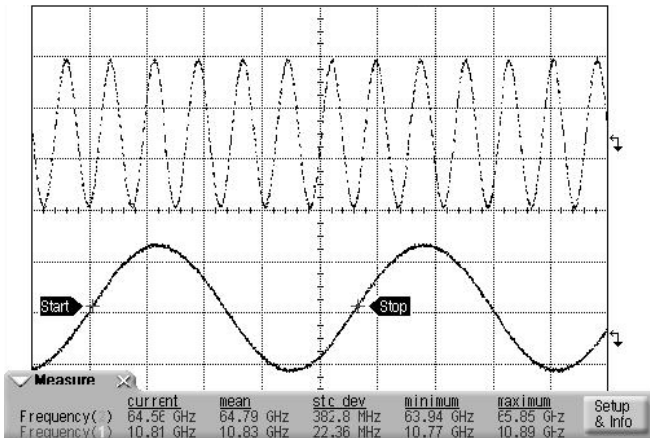


(c)

Figure 2.5: Measured time domain waveforms when the ILFD is operating as (a) a divide-by-2 at 17 GHz, (b) divide-by-4 at 39 GHz, and (c) divide-by-6 at 65 GHz.

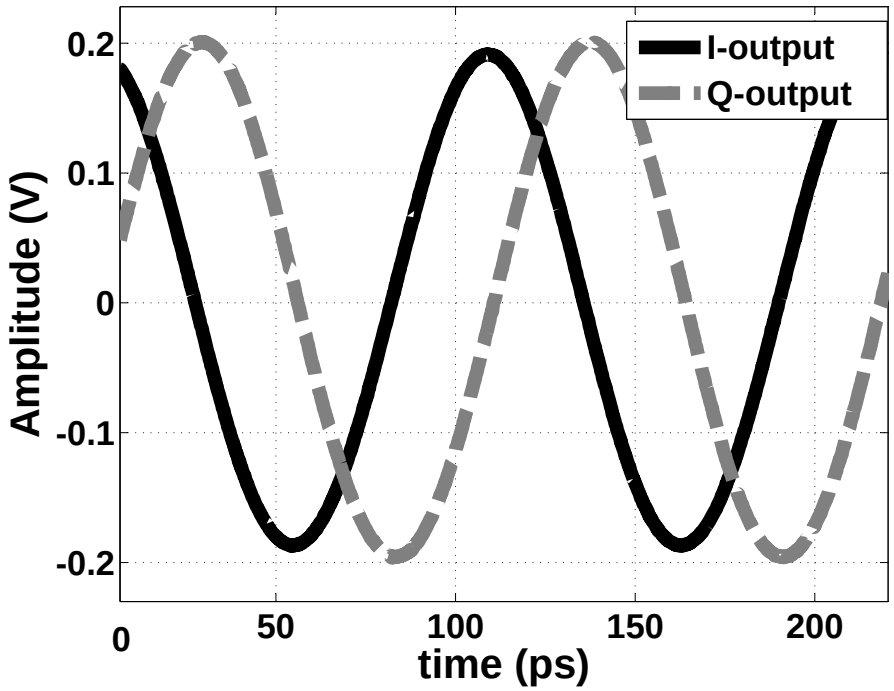


Figure 2.6: Measured in-phase and quadrature phases at the output of ILFD operated in the divide-by-6 mode, f_{in}=55 GHz.

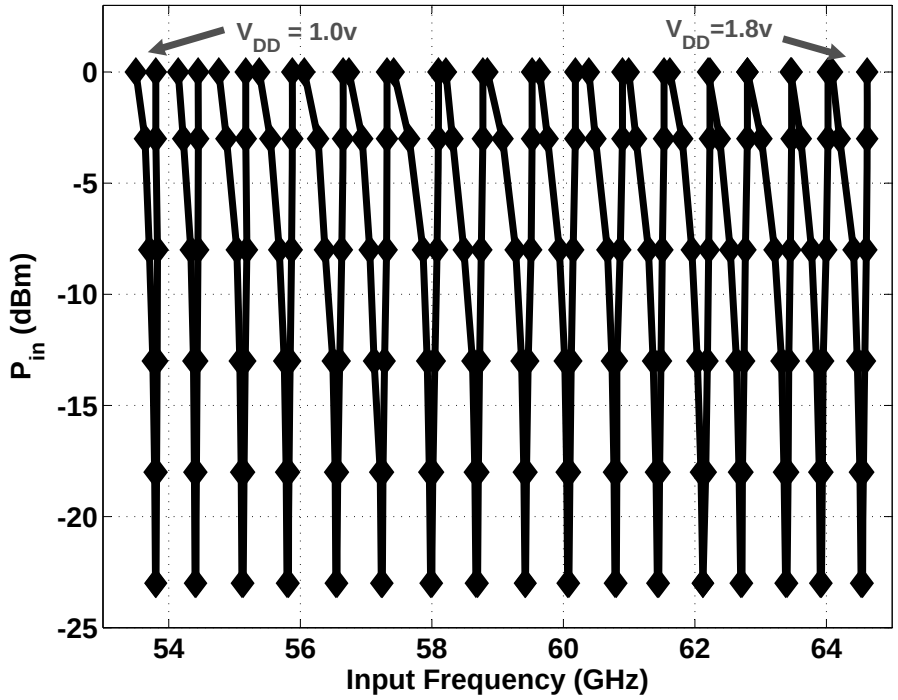


Figure 2.7: Measured input frequency range for divide-by-six mode when external tuning is applied.

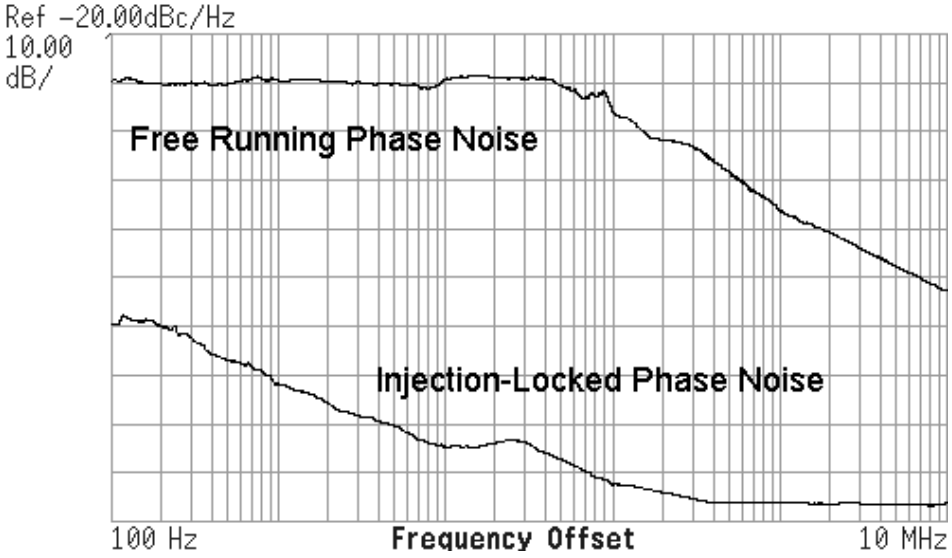


Figure 2.8: Measured phase noise the ILFD for free-running and injection-locked conditions.

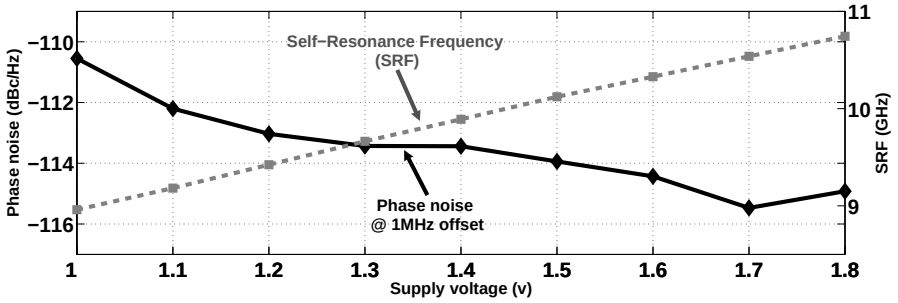


Figure 2.9: Measured phase noise, and SRF for divide-by-six mode vs. external tuning.

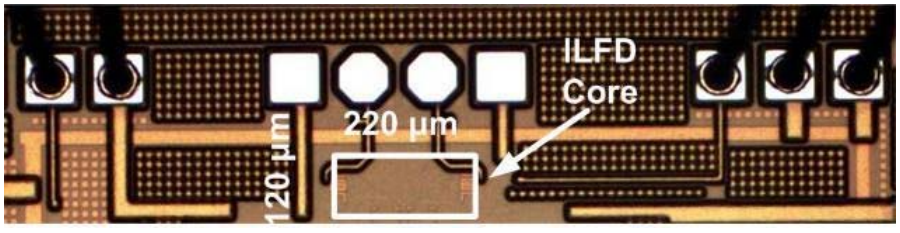


Figure 2.10: Chip microphotograph.

Table 2.1: Performance comparison with recent V-band dividers.

Reference	[23]	[24]	This Work
Input Frequency	70 GHz	70 GHz	65 GHz
Output phases	1	2	4 (Capable of 8)
Division Ratio	4	2	6
Lock Range	1.3%	9.4%	1.5%
Tuning Range	63-72 GHz	No tuning	51-65 GHz
Input Level	0 dBm	-2 dBm	0 dBm
Phase Noise (@ 1MHz offset)	-	-114 dBc/Hz	-110 - -115 dBc/Hz
Technology	90nm	130nm	130nm
Supply current	5.5mA	5mA	12-24mA
Die Size	0.014 mm^2	0.120 mm^2	0.026 mm^2

2.5 Conclusion

A CMOS V-Band multi-phase divide-by-six ring-oscillator-based ILFD is presented. The divider also achieves division ratios of four and two when 44 GHz or 22 GHz signals are applied respectively. It does not contain any on-chip inductor nor on-chip transformer, and the core area is 0.026 mm^2. This work demonstrates the possibility of designing compact, low-noise, multi-phase frequency dividers at frequencies close to (f_T) with CMOS technology.

This chapter has been published in part in the following publication:

- M. Farazian, P. S. Gudem, and L. E. Larson, "A CMOS Multi-Phase Injection-Locked Frequency Divider for V-Band Operation", *IEEE Microwave and Wireless Components Letters*, pp 239 - 241, April 2009.

Chapter 3

Analysis of Injection-Locked Regenerative Frequency Dividers

3.1 Introduction

Frequency dividers are one of the most important components of any frequency synthesizer. In some applications, fractional division ratios are required [29]. In addition, 50% duty cycle quadrature output phases will allow the use of SSB frequency conversion. It is challenging to implement a high-frequency fractional 50% duty cycle and quadrature output frequency divider in a digital CMOS technology with small die area and low power consumption.

We begin this chapter with a general overview of fractional frequency dividers in Section 3.2. Injection-locked regenerative frequency dividers are introduced in Section 3.3. Their stability is analyzed in Section 3.4. Two-stage ring-oscillators are good candidates to be used in quadrature output injection-locked regenerative frequency dividers. The steady-state operation, stability, and injection-locked behavior of two-stage ring-oscillators (based on negative resistance delay cells) are studied in Section 3.5. Phase noise analysis of the injection-locked regenerative frequency dividers is performed in Section 3.6. Section 3.7 contains a design example of injection-locked regenerative dividers to implement a divider with fractional division ratio and quadrature output phases, followed by circuit simulation result . Section 3.8 summarizes and concludes

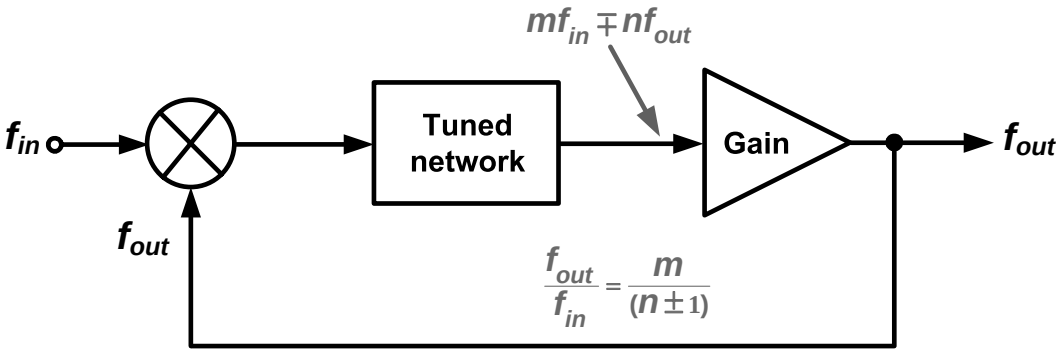
this chapter.

3.2 Fractional Frequency Dividers

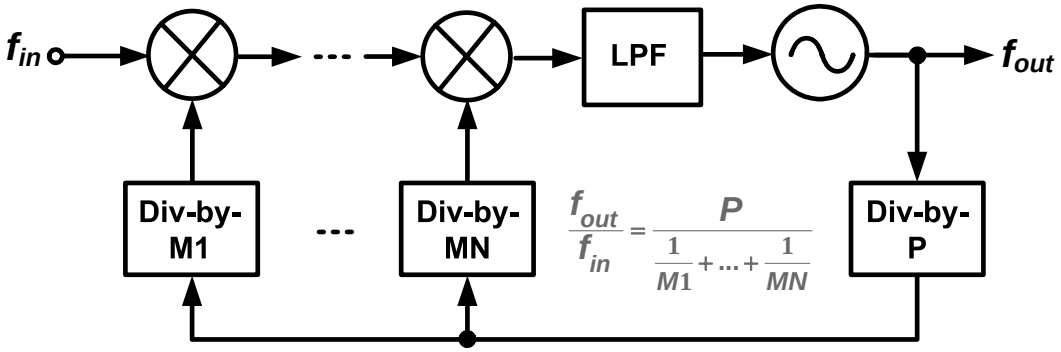
Traditionally, regenerative frequency dividers [30] are used to achieve fractional division ratios. Figure 3.1(a) shows a block diagram of a regenerative frequency divider. A mixer, or a nonlinear network in general, is used to create the mixing products of the input and output frequencies. The tuned network in the forward path passes the desired mixing product to the output. As shown in [29], this divider can achieve the desired fractional division ratio. However, regenerative frequency dividers have several limitations: (1) They are usually not able to provide quadrature output phases, (2) The sensitivity and output amplitude are degraded when higher-order mixing products are needed to achieve larger than two, or fractional, division ratios [31], (3) They often require inductively tuned loads, which require a large die area, and (4) The locking range is limited by the Q of the tuned load.

The block diagram of a frequency divider based on the heterodyne phase locking technique [24] is shown in Fig. 3.1(b). This technique can also be used to obtain a fractional division ratio. However, it requires tuned loads for filtering the sum component at the output of the mixer. In addition, the divider of Fig. 3.1(b) requires more than one mixer to implement a fractional division ratio. Increasing the number of mixers will increase the power consumption and die area. At the same time, this frequency divider cannot provide quadrature phases of the output, unless a quadrature VCO, or a combination of a VCO at twice the desired frequency and a divide-by-two, is used in the forward path. These approaches require more area and power consumption. In addition, a quadrature VCO poses its own limitations on the I/Q amplitude and phase accuracy, as well as the achievable phase noise.

Another approach to implement a fractional division ratio is to use multiple phases of the input clock and interpolating between them using a sequential logic circuit [32]. However, the speed of this technique is limited to lower frequencies, since it relies on digital sequential circuits. Moreover, it can neither provide quadrature output phases nor achieve a 50% duty cycle.



(a)



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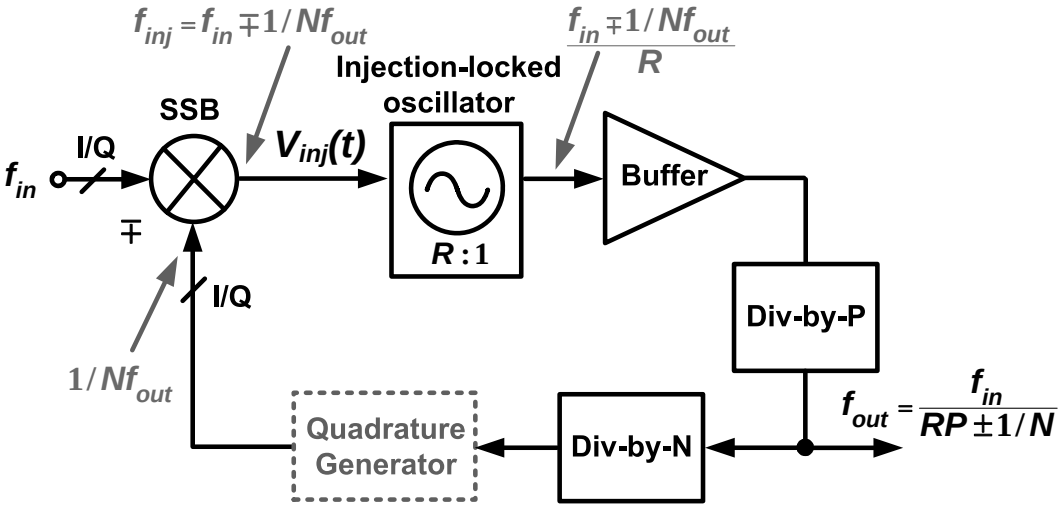


(c)

Figure 3.1: (a) Block digram of a traditional regenerative frequency divider, (b) general block diagram of a frequency divider based on heterodyne phase locking technique, (c) generalized injection-locked regenerative frequency divider.

In this chapter, a different category of frequency dividers is analyzed, which can achieve both fractional division ratio and 50% duty cycle quadrature output phases. This class of frequency dividers is discussed in Section 3.3, and its operation and stability conditions are analyzed in Section 3.4.

3.3 Injection-Locked Regenerative Frequency Dividers

A general block diagram of the injection-locked regenerative frequency divider is shown in Fig. 3.1(c). This divider consists of an injection-locked oscillator in the forward path, which is followed by a frequency divider with division ratio P, and a frequency divider with division ratio N in the feedback path. The mixer in this divider functions as a frequency converter, and the signal at the output of the mixer has a component at $f_{in} \mp 1/N f_{out}$. The mixer output, V_{inj}, can injection-lock the oscillator if its amplitude is sufficiently large and its frequency, f_{inj}, is within the locking range of the oscillator.

An SSB mixer can be used in this architecture to set the mixer output to $f_{in} - f_{out}/N$ or $f_{in} + f_{out}/N$ if quadrature phases of both signals are available. This helps eliminate the inductor tuned load of the mixer, which eases the implementation of the frequency divider in a digital CMOS technology and expands the frequency divider input range.

If the oscillator is injection-locked to the R^{th} harmonic of its output frequency, i.e. $f_{inj} = R f_{out}$, the output frequency of the injection-locked regenerative frequency divider can be expressed by

$$f_{out} = \frac{f_{in}}{RP \pm \frac{1}{N}}. \tag{3.1}$$

The $\pm$ in (3.1) depends on whether the difference or sum of two frequencies is chosen at the SSB mixer output. Equation (3.1) shows the possibility of obtaining fractional division ratios using the injection-locked regenerative frequency divider of Fig. 3.1(c). Similarly, if the oscillator is injection-locked to its R^{th} subharmonic, i.e. $f_{inj} = f_{out}/R$, then

$$f_{out} = \frac{f_{in}}{\frac{P}{R} \pm \frac{1}{N}}. \tag{3.2}$$

As can be seen from (3.1) and (3.2), injection-locked regenerative frequency dividers can generate almost any arbitrary division ratio. Moreover, as can be observed from Fig. 3.1(c), it can simultaneously provide multiple division ratios. Additionally, the proper choice of the divide-by-P block, e.g. a divide-by-two, enables a 50% duty cycle quadrature outputs. Appropriate distribution of the integer part of the division ratio in (3.1), i.e. RP (or the R/P ratio in (3.2)) may provide more options that can also lead to 50% duty cycle quadrature outputs. A design example that achieves fractional division ratios, a 50% duty cycle, and quadrature outputs is presented in Section 3.7.

Both (3.1) and (3.2) show the possibility of obtaining fractional division ratios. However, for the rest of this chapter our focus is on the case of super-harmonic injection-locking the oscillator to its R^{th} harmonic, i.e. $f_{inj} = Rf_{out}$, since this scenario has more applications in the frequency divider arena; hence we use (3.1) as the input-output frequency relationship of the frequency divider of Fig. 3.1.

Because of the similarities between the regenerative frequency divider, shown in Fig. 3.1(a), and the injection-locked regenerative frequency divider, the divider of Fig. 3.1(c) is sometimes referred to as a *Modified Regenerative Divider* [29]. However, the divider of Fig. 3.1(c) is a separate category of frequency divider, since it relies on an injection-locked oscillator for its operation. To clarify this point, when there is no input signal to a traditional regenerative frequency divider, it does not generate any output. In fact, as discussed in [30], this is one of the stability criteria of regenerative frequency dividers. However, in the injection-locked regenerative frequency divider of Fig. 3.1(c), the oscillator free-runs in the absence of an input.

3.4 Stability Analysis of Injection-Locked Regenerative Frequency Dividers

To analyze the stability of the frequency divider of Fig. 3.1(c), we assume that the oscillator in the forward path is injection-locked to a frequency that is close to the R^{th} harmonic of its self-resonance frequency, and an SSB mixer is used to generate the difference (or sum) of f_{in} and $1/Nf_{out}$. In this case, the relation between f_{out} and f_{in} is expressed by (3.1). In addition, we assume that the input signal is applied to

the LO port of the SSB mixer. If we represent the input and output of the injection-locked regenerative frequency divider by $V_{in}(t) = A_i \cos(\omega_{in} t + \theta_i)$ and $V_{out}(t) = A_o \cos(\omega_{out} t)$, the differential mixer output, $V_{inj}(t)$, can be expressed as

$$V_{inj}(t) = G_M Z_M A_o \cos(\omega_{out} t/N) f[A_i \cos(\omega_{in} t + \theta_i)] \tag{3.3}$$

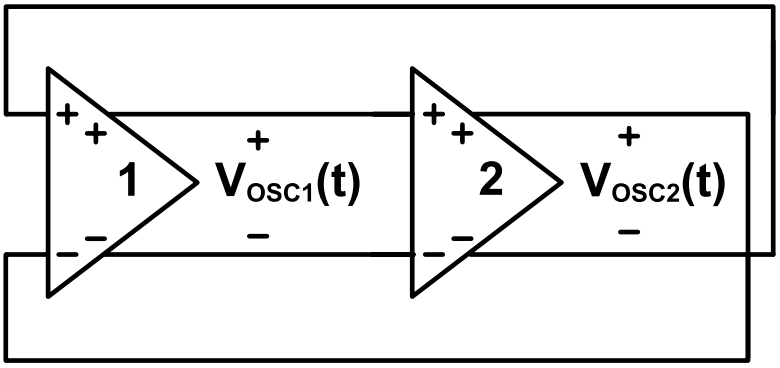
where G_M is the transconductance of the Gm-stage of the SSB mixer, and Z_M is the load impedance of the SSB mixer. In an inductor-less design approach, Z_M is a parallel combination of the load resistor and the parasitic capacitances. Therefore, for simplicity, both Z_M and G_M can be considered constant within the locking range of the oscillator. Moreover, for simplicity, we assume that Z_M and G_M do not contribute any phase shift.

The function $f(\cdot)$ in (3.3) models the nonlinearity of the LO port of the mixer. If the input amplitude, A_i, is sufficiently large, $f(\cdot)$ can be approximated with a ± 1 square wave. Under this assumption, if we substitute the Fourier series expansion of $f[A_i \cos(\omega_{in} t + \theta_i)]$ into (3.3), the component of $V_{inj}(t)$ which is at a frequency close to the self-resonance frequency of the oscillator is

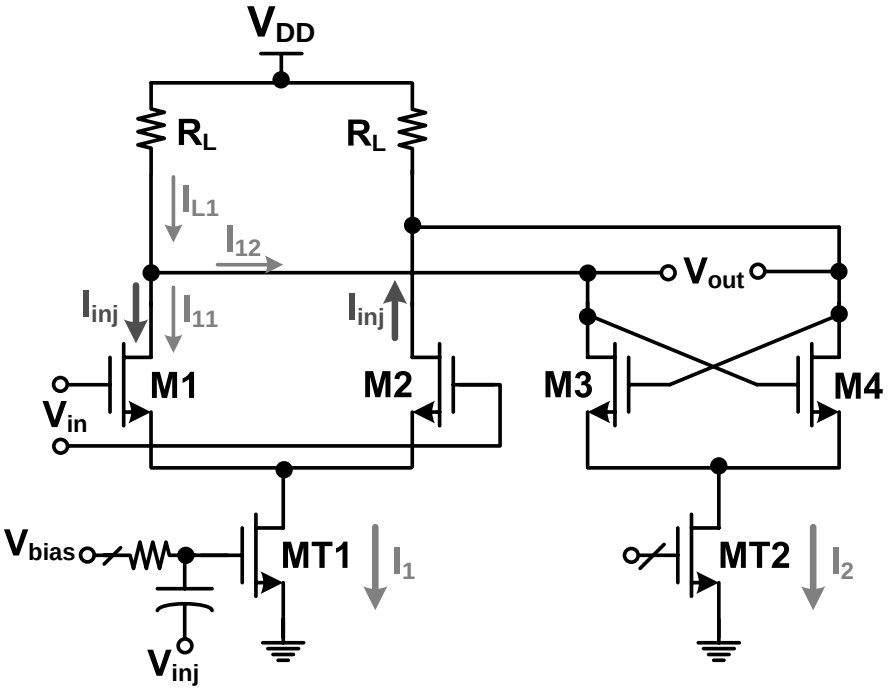
$$V_{inj}(t) = \frac{2}{\pi} G_M Z_M A_o \cos\left(\frac{RP}{RP \pm \frac{1}{N}} \omega_{in} t + \theta_i\right). \tag{3.4}$$

Other mixing products at the output of the SSB mixer, which are caused by the nonlinearity of the LO port are sufficiently far from the self-resonance frequency of the oscillator, hence cannot injection-lock the oscillator. Linearizing the Gm-stage of the mixer will suppress the mixing products caused by the nonlinearity of its transconductance (G_M). As a result, only the term shown in (3.4) plays a role in injection-locking the oscillator and other terms are ignored.

Clearly, the minimum input sensitivity of the frequency divider occurs when the output frequency is f_{SRF}/P, which corresponds to $f_{in} = [(RP \pm 1/N)/P] f_{SRF}$, where f_{SRF} is the self-resonance frequency (SRF) of the oscillator. If the amplitude of the signal at the mixer output (V_{inj}) is adequate to injection-lock the oscillator to $[P/(RP \pm 1/N)] f_{in}$, the oscillator and the frequency divider will operate in the stable region. If the amplitude is not adequate, the oscillator is pulled and will generate sidebands [33]. As a result, the stable region of operation of the injection-locked regenerative frequency divider is determined by the locking range of the oscillator.



(a)



(b)

Figure 3.2: Two-stage CMOS ring-oscillator (a) block diagram (b) negative resistance delay cell.

In order to super-harmonic injection-lock an oscillator to one of the oscillator's even harmonics, the injection signal must be applied to a common-mode node [34]. For instance, in the two-stage ring-oscillator of Fig. 3.2(a), which can be implemented using the negative resistance delay cell of Fig. 3.2(b), the injection current signal must be applied to the source terminals of transistors $M1$ and $M2$. In order to do that, a common choice is to apply $V_{inj}(t)$ to the gate of the tail current source of one of the delay cells in the ring oscillator. If $V_{inj}(t)$ is applied to the gate of transistor $MT1$ of Fig. 3.2(b), the component of injection current ($I_{inj}(t)$) at frequency $[P/(RP\pm 1/N)]f_{in}$ that reaches the oscillator output can be found using an approach similar to [34], i.e.

$$I_{inj}(t) = \frac{8}{\pi^2(R^2-1)} g_{mT} G_M Z_M A_o \frac{\sin\theta_i}{\cos\chi} \cos\left(\frac{P}{RP \pm \frac{1}{N}}\omega_{in}t - \chi\right) \tag{3.5}$$

where

$$\chi = \tan^{-1}\left(R\cot\theta_i\right) \tag{3.6}$$

and g_{mT} is the transconductance of $MT1$ of Fig. 3.2(b). The $I_{inj}(t)$ expressed in (3.5) injection-locks the oscillator to frequency $[P/(RP \pm 1/N)]f_{in}$. The magnitude of this injection current in terms of θ_i can be expressed as

$$|I_{inj}(t)| = \frac{8}{\pi^2(R^2-1)} g_{mT} G_M Z_M A_o \sqrt{1+(R^2-1)\cos^2\theta_i}. \tag{3.7}$$

These expressions are valid for differential oscillators where the injection signal is applied to the gate of the tail current source.

It is clear that the stable region of operation of an injection-locked regenerative frequency divider depends on the relationship between the locking range of the oscillator and the amplitude of the injection signal. This relationship is derived for LC oscillators in [35, 33], and for ring-oscillators, with more than three stages, in [26, 36, 37]. The locking range of a two-stage ring-oscillator is of interest, since it requires the fewest number of delay cells to generate quadrature output phases. Consequently, it can achieve smaller die area and lower power consumption.

The free-running and injection-locked behavior of this oscillator will be studied in Section 3.5, and its locking range for different injection-locking scenarios will be derived.

3.5 Injection-Locked Two-Stage Ring-Oscillator

In the previous section we showed how injection at the gate of $MT1$ generates differential injection current at the output of oscillator, as shown in Fig. 3.3. Writing KCL at the drain of $M1$ of the first delay cell results in

$$\frac{V_{OSC1_-}(t) - V_{DD}}{R} + C\frac{d}{dt}V_{OSC1_-}(t) + I_{D1}(t) + I_{D3}(t) - I_{inj_-}(t) = 0. \tag{3.8}$$

Similarly, writing KCL at the drain of transistor $M2$ of the first delay cell results in

$$\frac{V_{OSC1_+}(t) - V_{DD}}{R} + C\frac{d}{dt}V_{OSC1_+}(t) + I_{D2}(t) + I_{D4}(t) - I_{inj_+}(t) = 0. \tag{3.9}$$

From (3.8) and (3.9) we obtain the following differential equation.

$$\begin{aligned}\frac{V_{OSC1}(t)}{R} + C\frac{d}{dt}V_{OSC1}(t) &= [I_{D1}(t) - I_{D2}(t)] + [I_{D3}(t) - I_{D4}(t)] \\ &\quad + I_{inj}(t).\end{aligned} \tag{3.10}$$

In (3.10), $I_{inj}(t)$ is the differential injection current and is defined by $I_{inj_+}(t) - I_{inj_-}(t)$, and R and C are the equivalent output resistance and capacitance at the output of the delay cell. A similar differential equation is obtained for the second delay cell, without the injection current, as shown below.

$$\frac{V_{OSC2}(t)}{R} + C\frac{d}{dt}V_{OSC2}(t) = [I_{D1}^{'}(t) - I_{D2}^{'}(t)] + [I_{D3}^{'}(t) - I_{D4}^{'}(t)] \tag{3.11}$$

where $I_{D1}^{'}(t)$, $I_{D2}^{'}(t)$, $I_{D3}^{'}(t)$, and $I_{D4}^{'}(t)$ are the drain currents of the second delay cell.

In the steady-state, $V_{OSC1}(t)$ and $V_{OSC2}(t)$ can be expressed using Fourier series representation, i.e.

$$V_{OSC1}(t) = \sum_{k=-\infty}^{+\infty} V1_{(2k-1)}e^{j\theta_{1,(2k-1)}(t)} \tag{3.12a}$$

$$V_{OSC2}(t) = \sum_{k=-\infty}^{+\infty} V2_{(2k-1)}e^{j\theta_{2,(2k-1)}(t)} \tag{3.12b}$$

where

$$\theta_{1,(2k-1)}(t) = (2k-1)\omega_o t + \phi_{1,(2k-1)} \tag{3.13a}$$

$$\theta_{2,(2k-1)}(t) = (2k-1)\omega_o t + \phi_{2,(2k-1)}. \tag{3.13b}$$

In order to have a real solution for oscillator voltages, $Vi_{(-2k-1)}$ and $Vi_{-(2k-1)}$ must be complex conjugates (i=1,2).

If the values of $V_{OSC1}(t)$ and $V_{OSC2}(t)$ are sufficiently large, the transistors of each delay cell are fully switched and the current waveforms of $I_{D1}(t) - I_{D2}(t)$ and $I_{D3}(t) - I_{D4}(t)$ are similar to a ± 1 square wave. These waveforms are in-phase with the fundamental component of their controlling voltages [26], i.e. $I_{D1}(t) - I_{D2}(t)$ in the first delay cell is in phase with the fundamental harmonic of $-V_{OSC2}(t)$ and $I_{D3}(t) - I_{D4}(t)$ is in phase with the fundamental harmonic of $V_{OSC1}(t)$, thus they could be represented using Fourier series as follows.

$$[I_{D1}(t) - I_{D2}(t)] = \sum_{k=-\infty}^{+\infty} I1_{(2k-1)} e^{j[(2k-1)\theta_{2,1}(t) - \pi]} \tag{3.14a}$$

$$[I_{D3}(t) - I_{D4}(t)] = \sum_{k=-\infty}^{+\infty} I2_{(2k-1)} e^{j(2k-1)\theta_{1,1}(t)} \tag{3.14b}$$

The factor $-\pi$ in the argument of the instantaneous phase of $I_{D1}(t) - I_{D2}(t)$ in (3.14a) comes from its controlling voltage, i.e. the fundamental harmonic of $-V_{OSC2}(t)$.

To represent a real current, $Ij_{(2k-1)}$ and $Ij_{-(2k-1)}$ must be complex conjugate (j=1,2). As shown in [38], under the stated assumptions, $I1_1$ and $I2_1$ are respectively $2I_1/\pi$ and $2I_2/\pi$. We also assume that the differential injection current can be represented by $I_{inj}\cos(\theta_{inj}(t))$ where $\theta_{inj} = \omega_{inj} t + \phi_{inj}$. By substituting (3.12a), (3.12b), (3.14a), and (3.14b) into (3.10), and considering stabilized amplitude of oscillation under steady-state, (3.15) is obtained.

$$\sum_{k=-\infty}^{+\infty} \frac{V1_{(2k-1)}}{R} e^{j\theta_{1,(2k-1)}(t)} + jC\left(\sum_{k=-\infty}^{+\infty} V1_{(2k-1)} \frac{d}{dt}[\theta_{1,(2k-1)}(t)] e^{j\theta_{1,(2k-1)}(t)}\right) =$$
$$-\sum_{k=-\infty}^{+\infty} I1_{(2k-1)} e^{j(2k-1)\theta_{2,1}(t)} + \sum_{k=-\infty}^{+\infty} I2_{(2k-1)} e^{j(2k-1)\theta_{1,1}(t)} + I_{inj}\cos\theta_{inj} \tag{3.15}$$

When the oscillator is injection-locked, $\omega_o = \omega_{inj}$. Equating the coefficients of similar exponents in (3.15) results in (3.16) where $\delta_{(2k-1),\pm1}$ is the Kronecker delta and equals one for the fundamental harmonic of output voltages ($k = 0, 1$) and is zero for other harmonics.

$$\frac{V1_{(2k-1)}}{R}e^{j\theta_{1,(2k-1)}(t)} + jCV1_{(2k-1)}\frac{d}{dt}[\theta_{1,(2k-1)}(t)]e^{j\theta_{1,(2k-1)}(t)} = -I1_{(2k-1)}e^{j(2k-1)\theta_{2,1}(t)} + I2_{(2k-1)}e^{j(2k-1)\theta_{1,1}(t)} + \frac{1}{2}I_{inj}e^{j\theta_{inj}(t)}\delta_{(2k-1),\pm1} \tag{3.16}$$

where $k \in \mathbb{Z}$.

The harmonics of the currents of (3.14a) and (3.14a) have a roll-off of approximately $1/\left|2k-1\right|$. Moreover these harmonics go through the low-pass filter of the output load of each delay cell. As a result, the fundamental harmonic is dominant.

Substituting $k = 1$ into (3.16) results in a differential equation for the fundamental harmonic of $V_{OSC1}(t)$,

$$\frac{V1_1}{R}e^{j\theta_{1,1}(t)} + jCV1_1\frac{d\theta_{1,1}(t)}{dt}e^{j\theta_{1,1}(t)} = -I1_1e^{j\theta_{2,1}(t)} + I2_1e^{j\theta_{1,1}(t)} + \frac{1}{2}I_{inj}e^{j\theta_{inj}(t)} \tag{3.17}$$

After substituting the values of $I1_1$ and $I2_1$ into (3.17), it can be re-written as

$$\frac{V1_1}{R} + jCV1_1\frac{d\theta_{1,1}(t)}{dt} = -\frac{2I_1}{\pi}e^{j[\theta_{2,1}(t)-\theta_{1,1}(t)]} + \frac{2I_2}{\pi} + \frac{1}{2}I_{inj}e^{j[\theta_{inj}(t)-\theta_{1,1}(t)]} \tag{3.18}$$

A similar equation can be obtained for the second delay cell.

$$\frac{V2_1}{R} + jCV2_1\frac{d\theta_{2,1}(t)}{dt} = \frac{2I_1}{\pi}e^{j[\theta_{1,1}(t)-\theta_{2,1}(t)]} + \frac{2I_2}{\pi} \tag{3.19}$$

To further simplify our analysis, we define $\Delta\theta$ and ψ as follows

$$\Delta\theta \triangleq \theta_{1,1}(t) - \theta_{2,1}(t) \tag{3.20a}$$

$$\psi \triangleq \theta_{inj}(t) - \theta_{1,1}(t). \tag{3.20b}$$

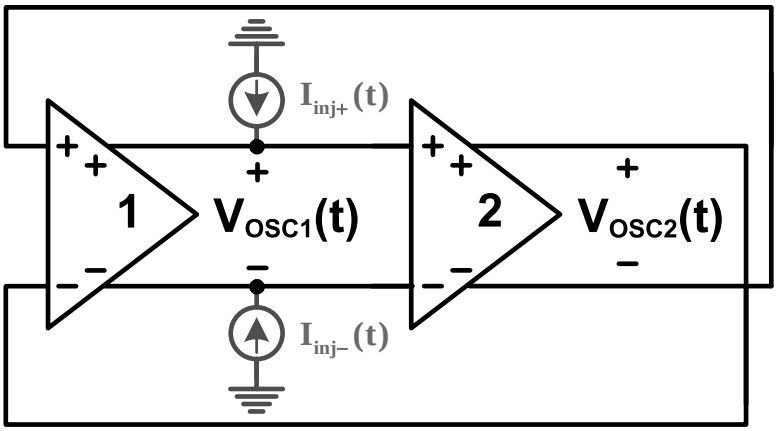


Figure 3.3: Schematic of the two-stage CMOS ring-oscillator when an external signal is injected at the output of the first delay cell.

By separating the real and imaginary parts of (3.18) and (3.19) we obtain

$$\frac{d\theta_{1,1}(t)}{dt} = \frac{1}{RC}\frac{I_1 \sin\Delta\theta + \frac{\pi}{4} I_{inj}\sin\psi}{-I_1\cos\Delta\theta + I_2 + \frac{\pi}{4} I_{inj}\cos\psi} \tag{3.21a}$$

$$\frac{d\theta_{2,1}(t)}{dt} = \frac{1}{RC}\frac{I_1 \sin\Delta\theta}{I_1\cos\Delta\theta + I_2}. \tag{3.21b}$$

These nonlinear differential equations are very similar to those from [26] for ring-oscillators with more than three stages. Equations (3.18) and (3.19) are used to calculate $V1_1$ and $V2_1$. If we represent the amplitudes of the fundamental harmonics of the first and second stage by V_{a1} and V_{a2}, $V_{a1} = 2Re[V1_1]$ and $V_{a2} = 2Re[V2_1]$, thus

$$V_{a1} = R\left(-\frac{4I_1}{\pi}\cos\Delta\theta + \frac{4I_2}{\pi} + I_{inj}\cos\psi\right) \tag{3.22a}$$

$$V_{a2} = R\left(\frac{4I_1}{\pi}\cos\Delta\theta + \frac{4I_2}{\pi}\right). \tag{3.22b}$$

We use (3.21a) and (3.21b) to analyze the free-running and injection-locking behavior of the two-stage ring-oscillator of Fig. 3.3.

3.5.1 Free-Running Oscillation

In steady-state and in the absence of an external signal, i.e. $I_{inj} = 0$, the ring-oscillator oscillates at its self-resonance frequency (SRF). In this case,

$$\frac{d\theta_{1,1}(t)}{dt} = \frac{d\theta_{2,1}(t)}{dt} = \omega_{_{SRF}}. \tag{3.23}$$

After substituting $I_{inj} = 0$ into (3.21a) and combining it with (3.21b) and (3.23), and from Appendix A, it is concluded that in steady-state

$$\Delta\theta = +\frac{\pi}{2}. \tag{3.24}$$

The self-resonance frequency is obtained by substituting $\Delta\theta = +\pi/2$ into (3.21a) or (3.21b), and then

$$\omega_{_{SRF}} = \frac{1}{RC}.\frac{I_1}{I_2} \tag{3.25}$$

and hence the steady-state solution for $\theta_{1,1}(t)$ and $\theta_{2,1}(t)$ can be written as shown below.

$$\theta_{1,1}(t) = \omega_{_{SRF}}t \tag{3.26a}$$

$$\theta_{2,1}(t) = \omega_{_{SRF}}t - \frac{\pi}{2} \tag{3.26b}$$

From (3.22a), (3.22b), and (3.24) the steady-state amplitudes of the fundamental harmonics of the output voltages are

$$V_{a1} = V_{a2} = \frac{4I_2R}{\pi}. \tag{3.27}$$

3.5.2 Two-stage Ring-Oscillator Under Single Node Injection

Assuming that an external signal is injected at the output of the first delay cell of the two-stage ring-oscillator, as shown in Fig 3.3, and has injection-locked the oscillator to its frequency (ω_{inj}). In this case,

$$\frac{d\theta_{1,1}(t)}{dt} = \frac{d\theta_{2,1}(t)}{dt} = \omega_{inj}. \tag{3.28}$$

We can use (3.28), (3.21a), and (3.21b) to find the steady-state solution for $\theta_{1,1}$ and $\theta_{2,1}$. Also, from (3.21a), (3.21b), and (3.28) the oscillation frequency under injection-locking can be expressed as

$$\omega_o|_{inj} = \omega_{inj} = \frac{1}{RC}\frac{I_1 \sin\Delta\theta}{I_1 \cos\Delta\theta + I_2}. \tag{3.29}$$

It is important to note that the oscillation frequency for this scenario is a function of $\Delta\theta$. Substituting the $\omega_{_{SRF}}$ from (3.25) into (3.29) results in

$$\omega_{inj} = \omega_{_{SRF}}\frac{\sin\Delta\theta}{1 + RC\omega_{_{SRF}}\cos\Delta\theta}. \tag{3.30}$$

The corresponding phase shift ($\Delta\theta$) for any given injection frequency (ω_{inj}) can be found from (3.30). Equation (3.30) can be re-written as

$$1 + \alpha\cos\Delta\theta - \beta\sin\Delta\theta = 0 \tag{3.31}$$

where α and β are

$$\alpha = RC\omega_{_{SRF}} \tag{3.32a}$$

$$\beta = \frac{\omega_{_{SRF}}}{\omega_{inj}}. \tag{3.32b}$$

The solution for (3.31) can be expressed as

$$\Delta\theta = \sin^{-1}\left(\frac{1}{\sqrt{\alpha^2 + \beta^2}}\right) - \tan^{-1}\left(\frac{\alpha}{\beta}\right). \tag{3.33}$$

Equation (3.33) determines the phase difference between the fundamental component of the output voltages (V_{OSC1} and V_{OSC2}). As can be seen from (3.33), injection-locking a two-stage ring-oscillator to any frequency other than its self-resonance frequency (using this scheme of injection-locking) results in non-quadrature fundamental harmonics of the outputs. As an example, a two-stage ring-oscillator, based on the delay cell of Fig. 3.2(b) is designed in a $0.13\mu m$ CMOS technology using a 1.2 V supply, and is used to verify this conclusion through simulation. In this oscillator, $R_L = 500\ \Omega$, $I_1 = 1.25\ mA$, $I_2 = 650\ \mu A$, and the self-resonance frequency is approximately 4 GHz.

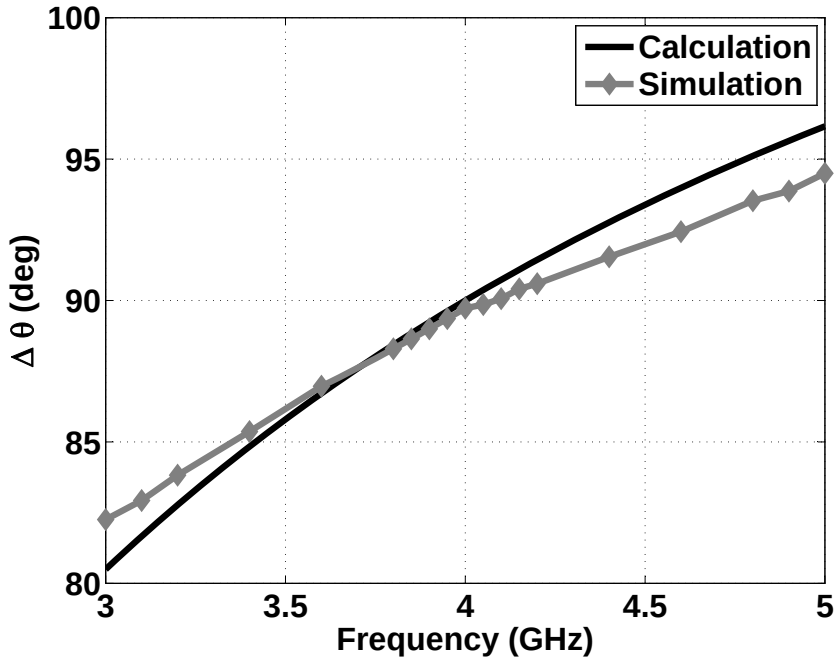


Figure 3.4: Simulated and calculated phase difference, using (3.33), at the output of a two-stage ring-oscillator, when an external signal is injected to the output of the first delay cell, f_{SRF}= 4 GHz.

The calculated output phase difference for a prototype two-stage ring-oscillator is plotted in Fig. 3.4 and is compared to circuit simulation, and the agreement is excellent.

We now calculate the required minimum amplitude and phase of the external signal to injection-lock the oscillator to ω_{inj}. From (3.21a), (3.21b), and (3.28) it can be concluded that

$$\frac{I_1 \sin\Delta\theta + \frac{\pi}{4} I_{inj} \sin\psi}{-I_1 \cos\Delta\theta + I_2 + \frac{\pi}{4} I_{inj} \cos\psi} = \frac{I_1 \sin\Delta\theta}{I_1 \cos\Delta\theta + I_2}. \tag{3.34}$$

Equation (3.34) can be simplified to

$$I_1^2 \sin 2\Delta\theta + \frac{\pi}{4} I_{inj} \left[I_1 \sin\left(\psi - \Delta\theta\right) + I_2 \sin\psi \right] = 0. \tag{3.35}$$

Using (3.35) one can find ψ, as a function of $\Delta\theta$ and injection current, as follows.

$$\psi = \xi - \sin\left(\frac{4}{\pi} \frac{I_1^2 \sin 2\Delta\theta}{I_{inj}\sqrt{I_1^2 + I_2^2 + 2I_1 I_2 \cos\Delta\theta}} \right) \tag{3.36}$$

where

$$\xi = \tan^{-1}\left(\frac{I_1 \sin\Delta\theta}{I_1 \cos\Delta\theta + I_2}\right). \tag{3.37}$$

The smallest required amplitude of injection current to injection-lock the oscillator at ω_{inj} is obtained from (3.36).

$$I_{inj} \geq \frac{4}{\pi}\frac{I_1^2\,|\sin 2\Delta\theta|}{\sqrt{I_1^2 + I_2^2 + 2I_1 I_2 \cos\Delta\theta}} \tag{3.38}$$

Therefore, by substituting $\Delta\theta$ from (3.33) into (3.38), one can find a lower bound for I_{inj} to injection-lock the oscillator to ω_{inj}. Lastly, the solution for ψ is found by substituting the lower bound for I_{inj} into (3.36).

Repeating this procedure for different values of ω_{inj} results in the input sensitivity curve (I_{inj} vs. ω_{inj}) of the two-stage ring-oscillator.

Using this procedure, the calculated locking-range of the two-stage ring-oscillator is obtained and plotted in Fig. 3.5 and is compared with circuit simulations, and the agreement is excellent.

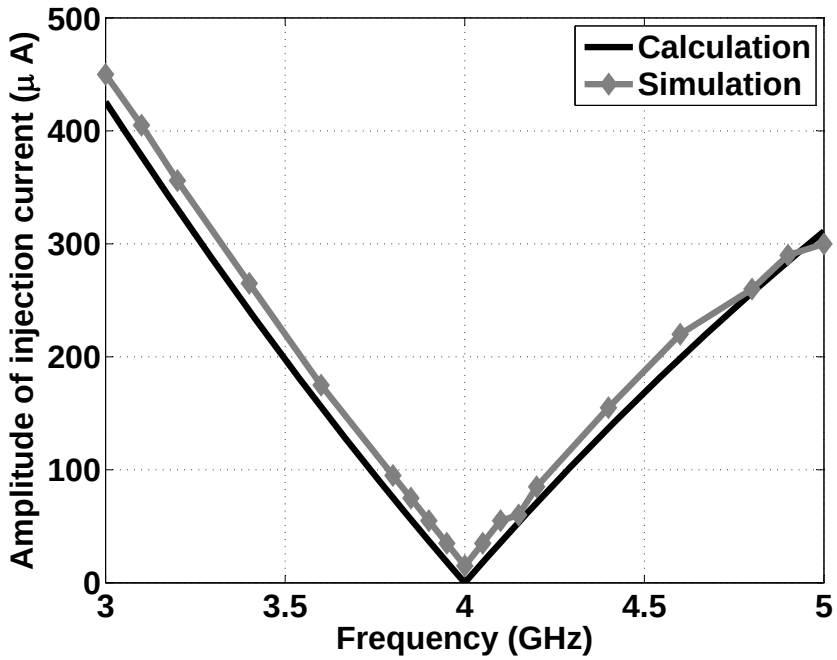


Figure 3.5: Calculated, using (3.38), and simulated locking range of a two-stage ring-oscillator when an external signal is injected to the output of the first delay cell.

It can be concluded from (3.22a) and (3.22b) that in the presence of any external signal, even if it is at the same frequency as SRF, the amplitudes of the oscillation voltages are not equal. Figure 3.6 shows the calculated and simulated amplitudes of the output voltages as a function of injection frequency, assuming the minimum required injection current, from (3.38), is injected at the output of the first delay cell. As can be observed in Fig. 3.6, the output voltages have equal amplitude at the SRF. The calculated and simulated amplitude difference vs. injection frequency is shown in Fig. 3.7, and the agreement between the two is excellent.

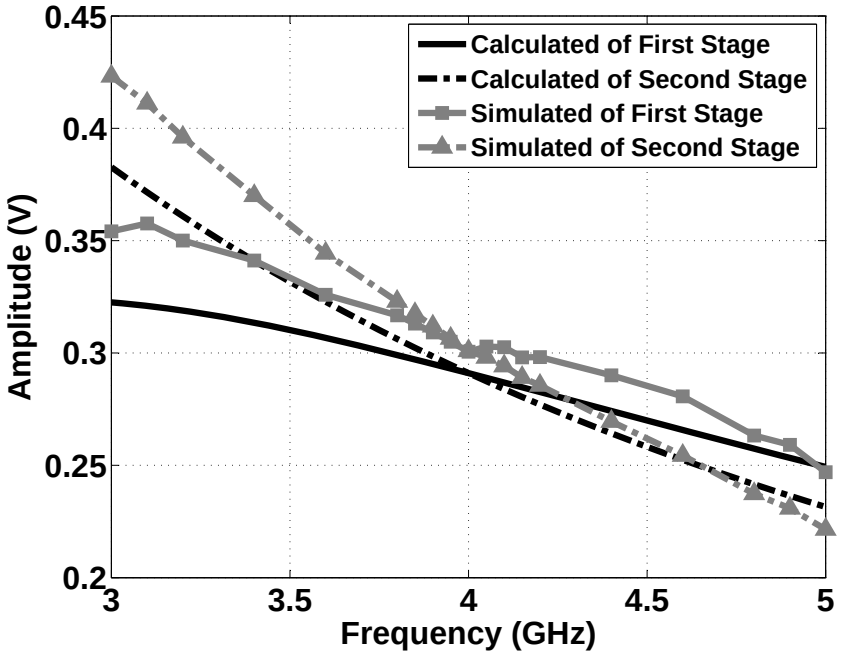


Figure 3.6: Calculated, using (3.22a) and (3.22b), and simulated amplitudes of output voltages vs. injection frequency when external signal is injected at the output of the first delay cell and the minimum required injection current is applied, f_{SRF}= 4 GHz.

Figure 3.8(a) shows a graphical representation of the steady-state solution for the oscillation phases of the oscillator of Fig. 3.3 when it free-runs. In this representation, I_{11} and I_{12} are the corresponding phasors for the I_1 and I_2 current sources of the first delay cell, shown in Fig. 3.2(b), and I_{21} and I_{22} are the corresponding current phasors of the second delay cell. The resultant currents of the delay cells are denoted by I_{L1} and I_{L2}. As can be seen in Fig. 3.8(a), when the two-stage ring-oscillator free-runs, or locks

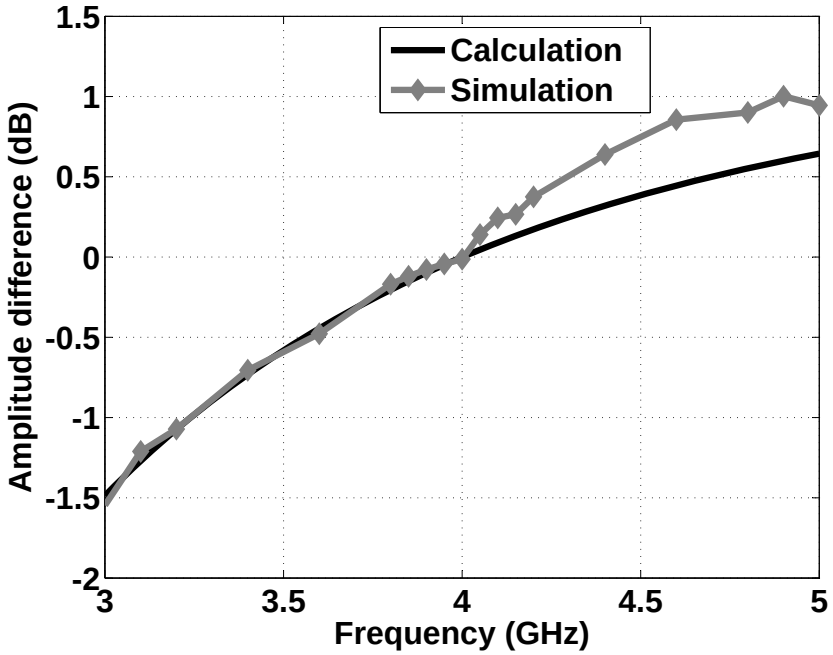


Figure 3.7: Calculated, using (3.22a) and (3.22b), and simulated amplitude difference vs. injection frequency when external signal is injected at the output of the first delay cell and the minimum required injection current is applied, f_{SRF}= 4 GHz.

to its self-resonance frequency, the two oscillation phases are orthogonal. In this case, the angle between the phasors of the resultant current and the corresponding voltage of each stage is $\phi_0 = tan^{-1}(I_1/I_2)$.

Figure 3.8(b) shows the same currents and voltages when the oscillator of Fig. 3.3 is injection-locked to a frequency lower than its SRF. In this case, the phase difference between oscillation phases, $\Delta\theta$, is less than $\pi/2$. It can be shown that– in this case– the angle between the phasors of the resultant current and the voltage of each delay cell ($\phi_1^{'}$ in the first delay cell and $\phi_2^{'}$ in the second one) is less than ϕ_0. Similarly, Fig. 3.8(c) depicts the voltage and current phasors when the oscillator is injection-locked to a frequency greater than its self-resonance frequency. In this case, $\Delta\theta$ is greater than $\pi/2$. Similarly, it can be shown that in this case $\phi_1^{'}$ and $\phi_2^{'}$ are greater than ϕ_0.

The non-quadrature output phases obtained for this scheme of injection-locking when the oscillator is injection-locked to frequencies other than its self-resonance frequencies, makes this scheme of injection-locking less attractive for the applications with

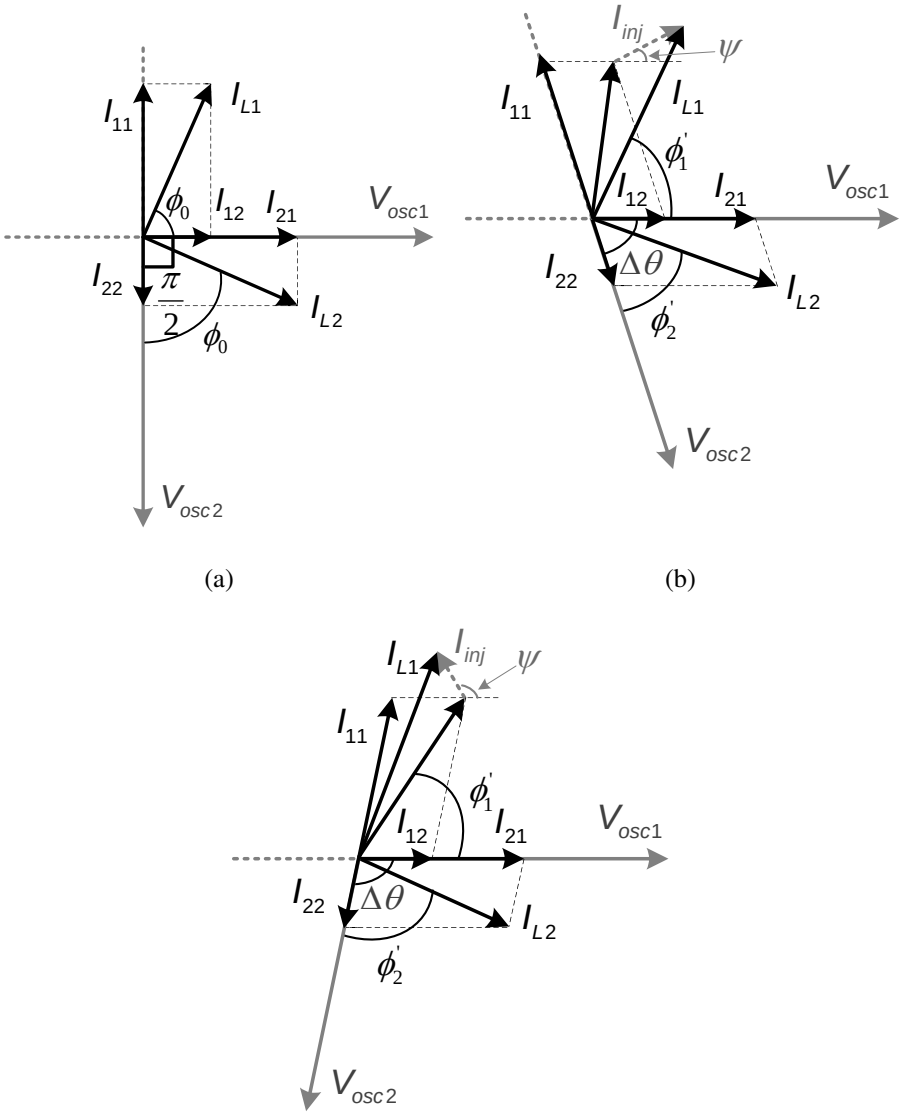


Figure 3.8: Graphical representation of steady-state solution for the voltage and current phasors of the two-stage ring-oscillator (a) free-running, (b) injection-locked to a frequency lower than its self-resonance frequency (SRF), and (c) injection-locked to a frequency greater than its SRF. External signal is injected at the output of the first delay cell.

demanding quadrature accuracy. In Section 3.5.3, this oscillator is analyzed when the external signal is injected at the output of both the delay cells.

3.5.3 Two-stage Ring-Oscillator Multi-Node Injection

In this section, we investigate the two-stage ring-oscillator when the external signal is injected to both of its delay cells, as shown in Fig. 3.9. There are several reasons to inject the external signal at multiple nodes instead of a single node:

1. It provides balanced loading for the previous stage in differential circuits.
2. It may increase the locking range of the oscillator under injection, as shown in [26, 36].
3. In this problem, it may help to maintain quadrature phases ($\Delta\theta = \pi/2$) and equal amplitudes for the fundamental harmonics of output voltages in the entire locking range.

In this section we propose a technique to maintain $\Delta\theta = \pi/2$ for the entire locking range of the oscillator.

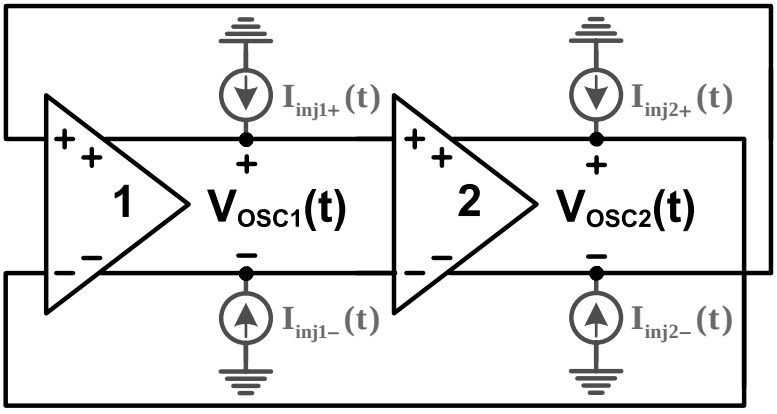


Figure 3.9: Two-stage ring-oscillator when external signal is injected at the output of both delay cells.

Using similar assumptions and procedures that were used to derive (3.18) and (3.19), the following set of differential equations are derived for the amplitudes and

phases of the oscillator when external signals are injected to the outputs of both delay cells (Fig. 3.9).

$$\frac{V1_1}{R} + jCV1_1\frac{d\theta_{1,1}(t)}{dt} = -\frac{2I_1}{\pi}e^{j[\theta_{2,1}(t)-\theta_{1,1}(t)]} + \frac{2I_2}{\pi} + \frac{1}{2}I_{inj1}e^{j[\theta_{inj1}(t)-\theta_{1,1}(t)]} \tag{3.39a}$$

$$\frac{V2_1}{R} + jCV2_1\frac{d\theta_{2,1}(t)}{dt} = \frac{2I_1}{\pi}e^{j[\theta_{1,1}(t)-\theta_{2,1}(t)]} + \frac{2I_2}{\pi} + \frac{1}{2}I_{inj2}e^{j[\theta_{inj2}(t)-\theta_{2,1}(t)]} \tag{3.39b}$$

Separating the real and imaginary parts of (3.39a) and (3.39b) will result in a differential equations that relate the amplitudes and phases of the fundamental harmonic of the output voltages to the amplitudes and phases of the injection signals. One can use (3.20a) and the following definitions to simplify the results;

$$\psi_1 \triangleq \theta_{inj1}(t) - \theta_{1,1}(t) \tag{3.40a}$$

$$\psi_2 \triangleq \theta_{inj2}(t) - \theta_{2,1}(t) \tag{3.40b}$$

results in

$$\frac{d\theta_{1,1}(t)}{dt} = \frac{1}{RC}\frac{I_1\sin\Delta\theta + \frac{\pi}{4}I_{inj1}\sin\psi_1}{-I_1\cos\Delta\theta + I_2 + \frac{\pi}{4}I_{inj1}\cos\psi_1} \tag{3.41a}$$

$$\frac{d\theta_{2,1}(t)}{dt} = \frac{1}{RC}\frac{I_1\sin\Delta\theta + \frac{\pi}{4}I_{inj2}\sin\psi_2}{I_1\cos\Delta\theta + I_2 + \frac{\pi}{4}I_{inj2}\cos\psi_2}. \tag{3.41b}$$

In addition, the steady-state amplitudes of the fundamental harmonics of the output voltages are obtained from (3.39a) and (3.39b).

$$V_{a1} = R\left(-\frac{4I_1}{\pi}\cos\Delta\theta + \frac{4I_2}{\pi} + I_{inj1}\cos\psi_1\right) \tag{3.42a}$$

$$V_{a2} = R\left(\frac{4I_1}{\pi}\cos\Delta\theta + \frac{4I_2}{\pi} + I_{inj2}\cos\psi_2\right) \tag{3.42b}$$

To complete the analysis, we also assume that the external signals that are used to injection-lock the oscillator have equal amplitudes, i.e. $I_{inj1} = I_{inj2} = I_{inj}$. From

(3.28), (3.41a), and (3.41b), it is concluded that in steady-state the following relation between ψ_1, ψ_2, $\Delta\theta$, and I_{inj} holds.

$$\frac{I_1 \sin\Delta\theta + \frac{\pi}{4} I_{inj} \sin\psi_1}{-I_1 \cos\Delta\theta + I_2 + \frac{\pi}{4} I_{inj} \cos\psi_1} = \frac{I_1 \sin\Delta\theta + \frac{\pi}{4} I_{inj} \sin\psi_2}{I_1 \cos\Delta\theta + I_2 + \frac{\pi}{4} I_{inj} \cos\psi_2} \tag{3.43}$$

We need to find a solution for (3.43) that satisfies $\Delta\theta = \pi/2$ for every value of I_{inj}, ψ_1, and ψ_2. By substituting $\Delta\theta = \pi/2$ into (3.43) we obtain the following equation.

$$\begin{aligned} &\sin(\frac{\psi_1 - \psi_2}{2})[2I_1 \sin(\frac{\psi_1 + \psi_2}{2}) + 2I_2 \cos(\frac{\psi_1 + \psi_2}{2}) \\ &+ \frac{\pi}{2} I_{inj} \cos(\frac{\psi_1 - \psi_2}{2})] = 0 \end{aligned} \tag{3.44}$$

By inspection we can see that $\psi_1 = \psi_2$ satisfies (3.44) for all the values of I_{inj}. If we define $\Delta\theta_{inj}$ as $\theta_{inj1} - \theta_{inj2}$, it can be shown that to have quadrature output phases in the oscillator of Fig. 3.9, the following condition needs to be true.

$$\Delta\theta_{inj} = \pi/2 \tag{3.45}$$

To provide quadrature inputs for this scheme of injection-locking, one can use a polyphase filter, or supply these phases using another ring-oscillator. However, when the ring-oscillator of Fig. 3.9 is used as a divide-by-two frequency divider, the external signal is applied to the gate of tail current source $MT1$ of the delay cell shown in Fig. 3.2(b). Since this signal is at a frequency twice the ω_{SRF}, the external signals applied to the gate terminals of the tail current sources in delay cells need to be 180 degrees out of phase to satisfy (3.45). This simplifies the problem of providing the oscillator under locking with the appropriate phases of external signal. Moreover, in this case, the oscillator/ frequency divider can provide balanced loading for its preceding differential stage. It is particularly of practical interest in injection-locked regenerative frequency dividers where the oscillator is driven by a differential SSB mixer.

By substituting the solution to (3.44), i.e. $\psi_1 = \psi_2 = \psi$, into (3.43) one can find an expression for the oscillation frequency under injection-locking in terms of the circuit parameters and the amplitudes and phases of the external signals.

$$\omega_{inj} = \omega_{_{SRF}} \left(\frac{1 + \gamma \sin \psi}{1 + \delta \cos \psi} \right) \tag{3.46}$$

where

$$\gamma = \frac{\pi}{4} \frac{I_{inj}}{I_1} \tag{3.47a}$$

$$\delta = \frac{\pi}{4} \frac{I_{inj}}{I_2}. \tag{3.47b}$$

A comparison with the case where the external signal is only injected to the first delay cell reveals that the oscillation frequency of the multi-node injection case is modulated by the angle between the injection current and the oscillation voltage (ψ), as shown in (3.46), while $\Delta\theta$ modulates the oscillation frequency in the single-injection case, as shown in (3.30).

If ω_{inj} is in the locking range of the oscillator, ψ can be determined by

$$\psi = \sin^{-1} \left(\frac{\omega_{inj}/\omega_{_{SRF}} - 1}{\gamma \sqrt{1 + (RC\omega_{inj})^2}} \right) - \tan^{-1}(RC\omega_{inj}). \tag{3.48}$$

The minimum required injection current to injection-lock the two-stage ring-oscillator to ω_{inj} is obtained from (3.48) and (3.25).

$$I_{inj} \geq \frac{4}{\pi} \frac{I_1}{\sqrt{1 + \left(\frac{I_1}{I_2} \frac{\omega_{inj}}{\omega_{_{SRF}}} \right)^2}} \left| \frac{\omega_{inj}}{\omega_{_{SRF}}} - 1 \right| \tag{3.49}$$

Using (3.49) one can obtain the locking-range of the two-stage ring-oscillator when injection current is injected to both the delay cells. The calculated and simulated locking-range of the two-stage ring-oscillator are plotted in Fig. 3.10 and the agreement is excellent.

This simulated locking range is compared with the simulated locking range from Section 3.5.2 where the external signal was only applied to the first delay cell. The result is plotted in Fig. 3.11. It is observed from this plot that applying the external signal to both the delay cells, with appropriate phase sequence and equal amplitudes,

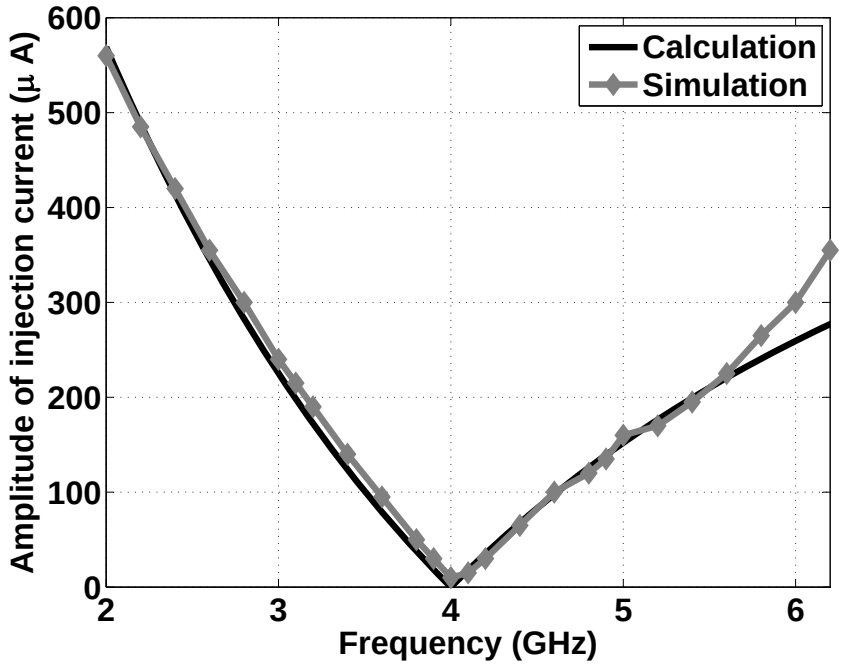


Figure 3.10: Calculated, using (3.49), and simulated locking range of a two-stage ring-oscillator when external signals are injected at the output of both delay cells.

leads to a wider locking range, and hence improves the sensitivity of the injection-locked oscillator. This result is in agreement with what was obtained in [26, 36] for ring-oscillators with more than three stages.

An output phase difference ($\Delta\theta$) of $\pi/2$ between fundamental harmonics of the output voltages is expected for this scheme of injection-locking. The calculated output phase difference for the designed two-stage ring-oscillator is plotted in Fig. 3.12 and is compared with circuit simulation. As can be seen from Fig. 3.12, circuit simulations show excellent agreement with calculations.

Note that under these assumptions, the amplitudes of the output voltages remain equal for all the values of injection frequency within the locking range of the oscillator and are expressed by

$$V_{a1} = V_{a2} = R\left(\frac{4I_2}{\pi} + I_{inj}\cos\psi\right). \tag{3.50}$$

The calculated and simulated amplitudes of the fundamental component of the output voltages are plotted in Fig. 3.13. It is expected from (3.50) that for this scheme of

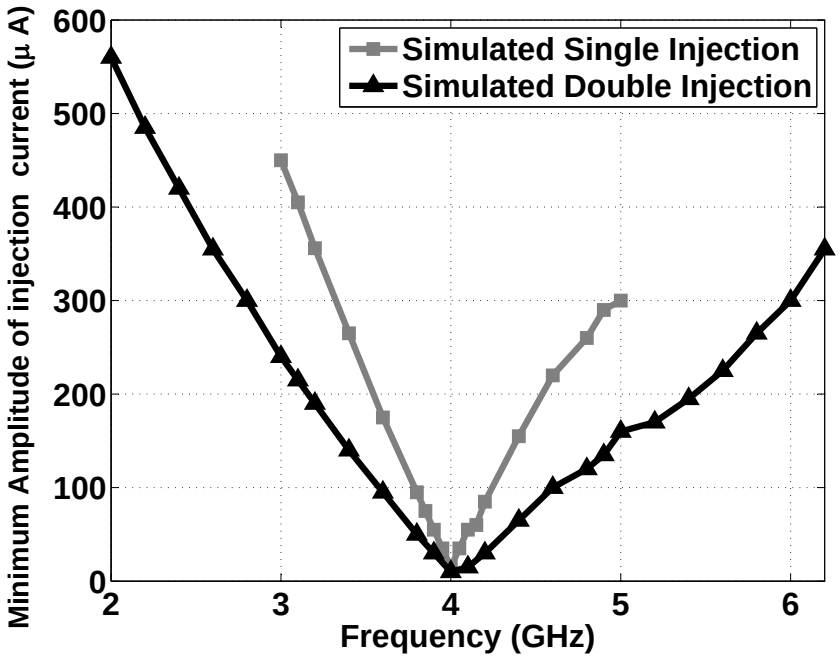


Figure 3.11: Simulated locking range of a two-stage ring-oscillator, $f_{_{SRF}} = 4GHz$.

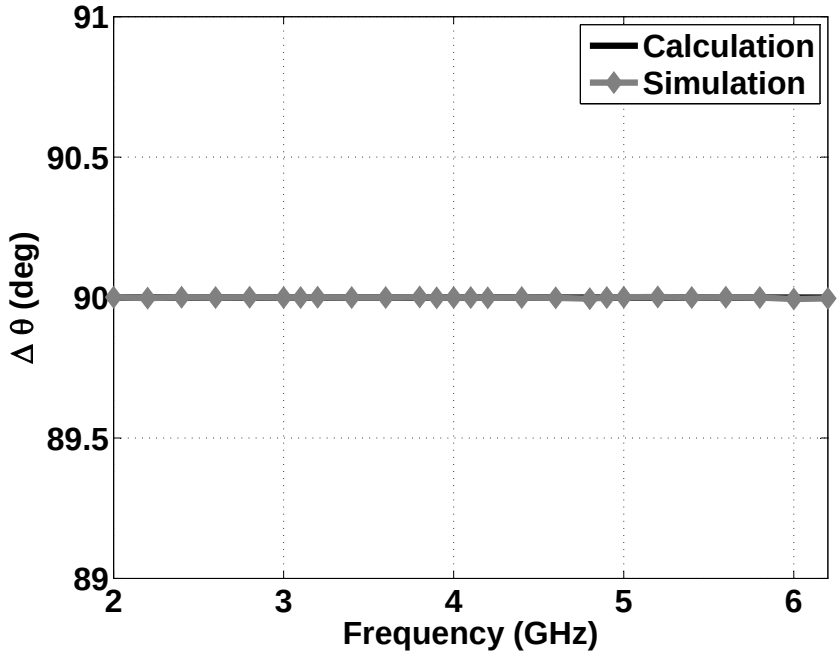


Figure 3.12: Calculated and simulated phase difference at the output of a two-stage ring-oscillator when quadrature external signals are injected to both delay cells with equal amplitudes, $f_{_{SRF}} = 4GHz$.

injection-locking, the amplitudes of the output voltages remain equal within the locking range of the two-stage ring-oscillator, and as shown in Fig. 3.14, the circuit simulations showed excellent agreement with calculations.

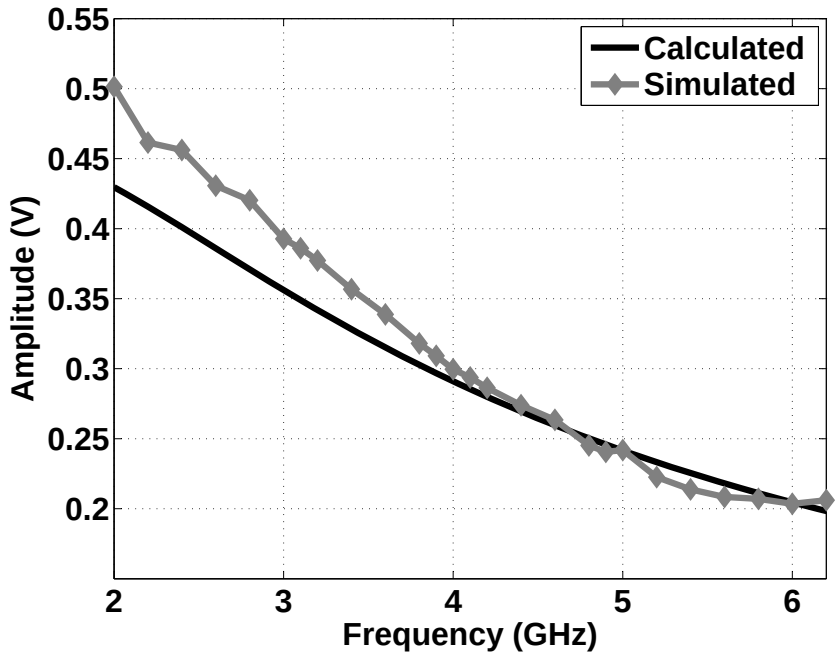


Figure 3.13: Calculated, using (3.50), and simulated amplitudes of output voltages vs. injection frequency.

Figure 3.15 shows a graphical representation of the steady-state solution for the phasors of voltages and currents of the oscillator of Fig. 3.9 when external signals are injected to both delay cells. It can be seen that under the constraints derived for external signals ($I_{inj1} = I_{inj2}$ and $\Delta\theta_{inj} = \pi/2$) the oscillation voltages remain in quadrature with equal amplitudes. Similar to Fig. 3.8(a), I_{11} and I_{12} are the corresponding phasors for I_1 and I_2 current sources (Fig. 3.2(a)) of the first delay cell, and I_{21} and I_{22} are the corresponding current phasors to the second delay cell, and I_{L1} and I_{L2} are the resultant currents of the first and second delay cells respectively.

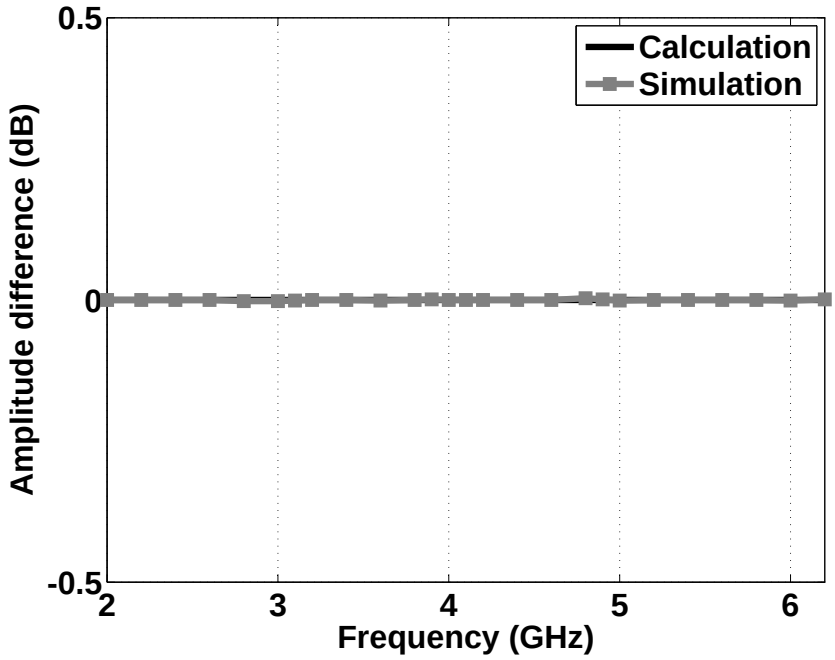


Figure 3.14: Calculated, using (3.50), and simulated amplitude difference when external signals are applied to both delay cells, and the minimum required injection current is used, $f_{_{SRF}} = 4GHz$.

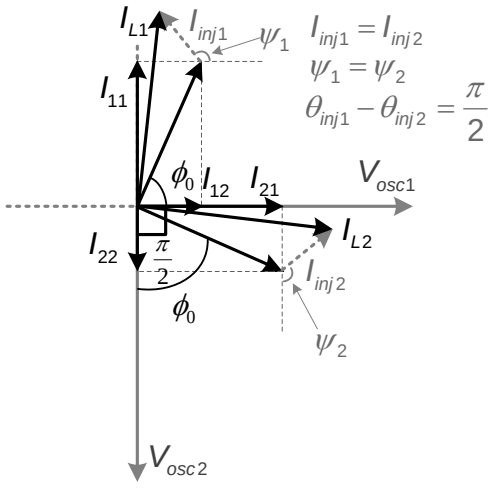


Figure 3.15: Graphical representation of steady-state solution for the voltage and current phasors of the two-stage ring-oscillator when external signals are injected to both delay cells with the equal amplitudes, and quadrature phases.

3.6 Phase Noise Analysis of Injection-Locked Regenerative Divider

To analyze the output phase noise of the injection-locked regenerative frequency divider, we use the simplified block diagram of this divider with main phase noise sources shown in Fig.3.16. It is assumed that the oscillator's internal phase noise and the phase noise of the input frequency to the divider are the main contributors to the output phase noise.

To start the analysis, we assume that steady-state is reached and the oscillator is super-harmonic injection-locked to the R^{th} harmonic of its output frequency.

It is shown in [28] that a super-harmonic injection-locked oscillator, to the R^{th} harmonic of its output frequency, behaves like a first-order PLL with an input phase to output phase transfer function of $G(S) = \frac{1}{1+S/\omega_P}$ where $S = j\Delta\omega$ and as shown in Appendix B, ω_P for the injection-locked oscillator of Fig. 3.9 is approximately

$$\omega_P = \frac{\omega_{inj}}{2}\frac{I_2 + \frac{\pi}{4}I_{inj}\cos\psi}{I_1}. \tag{3.51}$$

Therefore, the phase nosie at the output of the oscillator $(\Phi_{n_{OL}}(j\Delta\omega))$ can be in terms of oscillator's intrinsic noise $(\Phi_{n_{OF}}(j\Delta\omega))$ and the phase noise of the injection signal $(\Phi_{n_{inj}}(j\Delta\omega))$.

$$\Phi_{n_{OL}}(j\Delta\omega) = \frac{1}{R}G(j\Delta\omega)\Phi_{n_{inj}}(j\Delta\omega) + [1 - G(j\Delta\omega)]\Phi_{n_{OF}}(j\Delta\omega) \tag{3.52}$$

From (3.52), the rms value of the phase noise at the output of the injection-locked oscillator $(\overline{\phi^2_{n_{OL}}}(\Delta\omega))$ can be expressed as

$$\overline{\phi^2_{n_{OL}}}(\Delta\omega) = \frac{1}{R^2}\frac{1}{1+(\Delta\omega/\omega_P)^2}\overline{\phi^2_{n_{inj}}}(\Delta\omega) + \frac{(\Delta\omega/\omega_P)^2}{1+(\Delta\omega/\omega_P)^2}\overline{\phi^2_{n_{OF}}}(\Delta\omega). \tag{3.53}$$

As can be seen from (3.53), the phase noise at the output of the oscillator consists of two components: the oscillator's intrinsic phase noise, which goes through a first-order high-pass transfer function, and the phase noise of the injection signal which encounters a first-order low-pass transfer function. Consequently, the close-in phase

noise of the injection-locked oscillator is dominated by the phase noise of the injection signal, while the high-frequency phase noise follows the internal phase noise of the free-running oscillator. Therefore, $\overline{\phi^2_{n_{OL}}}(\Delta\omega)$ can be approximated for close-in phase ($\Delta\omega \ll \omega_P$) and high-frequency phase noise ($\Delta\omega \gg \omega_P$) by

$$\overline{\phi^2_{n_{OL}}}(\Delta\omega) \approx \begin{cases} \frac{1}{R^2}\overline{\phi^2_{n_{inj}}}(\Delta\omega) & \Delta\omega \ll \omega_P \\ \overline{\phi^2_{n_{OF}}}(\Delta\omega) & \Delta\omega \gg \omega_P \end{cases}. \tag{3.54}$$

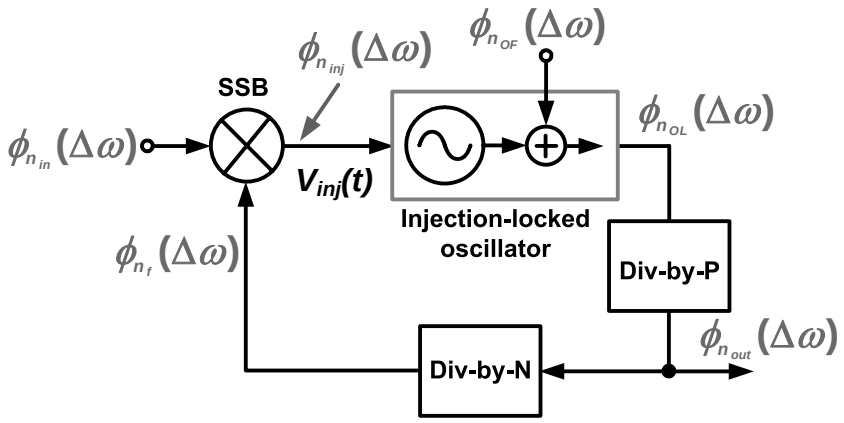


Figure 3.16: Phase noise mechanism in an injection-locked regenerative frequency divider.

As discussed in [39], if the SSB phase noise of the inputs to the mixer of Fig. 3.1(c) are $\overline{\phi^2_{n_{in}}}$ and $\overline{\phi^2_{n_f}}$, and if the amplitude of the signal at the mixer output is sufficiently large, the output phase noise of the mixer is mainly dominated by the phase noise of the inputs and can be written as

$$\overline{\phi^2_{n_{inj}}}(\Delta\omega) = \overline{\phi^2_{n_{in}}}(\Delta\omega) + \overline{\phi^2_{n_f}}(\Delta\omega). \tag{3.55}$$

Since the divide-by-P is locked to the oscillator output, we can assume that its output phase noise is dominated by the phase noise of the injection-locked oscillator, i.e. $\overline{\phi^2_{n_{out}}}(\Delta\omega) = \overline{\phi^2_{n_{OL}}}(\Delta\omega)/P^2$. As a result, the phase noise of the feedback signal (the output of the divide-by-N) is

$$\overline{\phi^2_{n_f}}(\Delta\omega) = \overline{\phi^2_{n_{OL}}}(\Delta\omega)/(NP)^2. \tag{3.56}$$

Substituting (3.55) and (3.56) into (3.54), the output phase noise of the injection-locked regenerative divider, $\pounds_{out}\{\Delta\omega\} = 10\log[\overline{\phi^2_{n_{out}}}(\Delta\omega)]$, can be expressed as

$$\pounds_{out}\{\Delta\omega\} \approx \begin{cases} 10\log\left[\frac{\overline{\phi^2_{n_{in}}}(\Delta\omega)}{(RP)^2-1/N^2}\right] & \Delta\omega \ll \omega_P \\ \\ 10\log\left[\frac{\overline{\phi^2_{n_{OF}}}(\Delta\omega)}{P^2}\right] & \Delta\omega \gg \omega_P \end{cases}. \tag{3.57}$$

It can be concluded from (3.53) that if the injection signal is noise-less, the phase noise at the output of the frequency divider would be equal to the attenuated extrinsic phase noise of the oscillator [26, 28], in other words

$$\pounds_{out}\{\Delta\omega\} = 10\log\left[\frac{(\Delta\omega/\omega_P)^2}{1+(\Delta\omega/\omega_P)^2}\frac{\overline{\phi^2_{n_{OF}}}(\Delta\omega)}{P^2}\right]. \tag{3.58}$$

To complete this section, we investigate the phase noise of the two-stage ring-oscillator of Fig. 3.2(a). The free-running phase noise of a two-stage ring-oscillator-based VCO that uses negative resistance delay cells with active loads is calculated in [40] using the impulse sensitivity function (ISF) technique of [41, 42]. Here we use the result obtained in [40] to find the phase noise of the two-stage ring-oscillator of Fig. 3.2. In this case, the free-running phase noise at the offset $\Delta\omega$ from the carrier (in dBc/Hz) can be expressed as

$$\pounds_{FR}\{\Delta\omega\} = 10\log\left[\frac{\pi^2}{24}\frac{(\overline{i^2_n}/\Delta f)}{(CV_{sw})^2(\Delta\omega)^2}\right] \tag{3.59}$$

where $\overline{i^2_n}/\Delta f$ is the output referred mean square current noise density which contains both thermal and flicker noises, and can be expressed by $\overline{i^2_n}(M1,\ M2,\ M3,\ M4)/\Delta f + 2 \times 4kT/R_L$. In this expression, R_L is the load resistor used in the delay cell of Fig. 3.2(b) since it is the only noisy component of the output resistance at the output of each delay cell. Using the oscillation frequency given by (3.25), the phase noise (3.59) can be re-written as

$$\pounds_{FR}\{\Delta\omega\} = 10\log\left[\frac{\pi^2}{24}\left(\frac{RI_2}{V_{sw}I_1}\right)^2\frac{(\overline{i^2_n}/\Delta f)}{(\Delta\omega/\omega_{_{SRF}})^2}\right]. \tag{3.60}$$

The simulated and calculated free-running phase noise of the prototype two-stage ring-oscillator from Section 3.5.2 is plotted in Fig. 3.17(a). To precisely calculate

the phase noise, $\overline{i_n^2}/\Delta f$ is measured using circuit simulation, and then substituted into (3.60). The simulated injection-locked phase noise of this two-stage ring-oscillator for different amplitudes of the injection signal is shown in Fig. 3.17(b). To obtain these plots, this two-stage ring-oscillator is used as a divide-by-two and noise-less differential injection signals are applied to the gates of transistors labeled by $MT1$ (Fig. 3.2(b)) in each delay cell. As was discussed before, the output phase noise of the oscillator is its attenuated internal noise, and this noise is more attenuated for a larger amplitudes of injection signal.

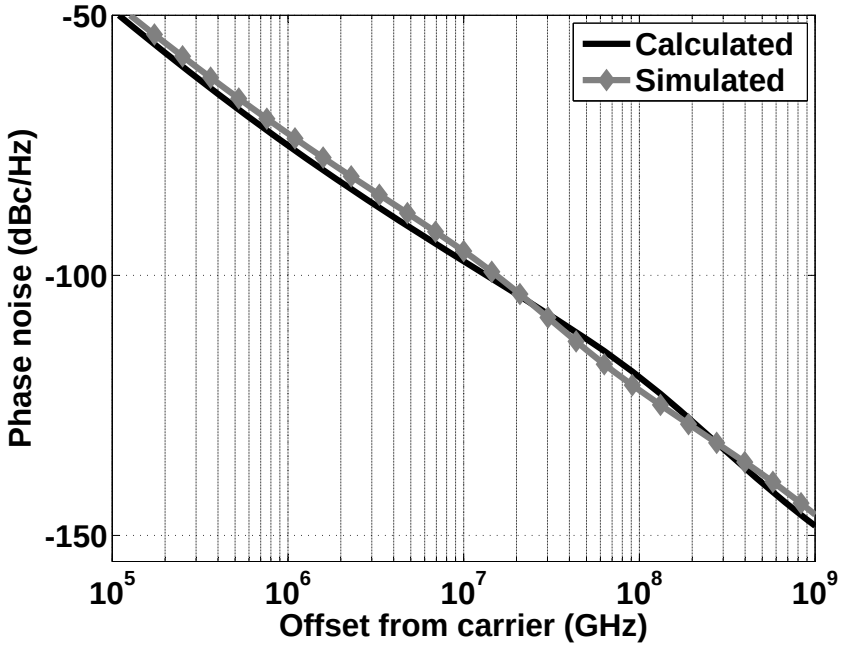
Using (3.57), (3.60), and the phase noise of the injection signal, one can calculate the output phase noise of the injection-locked regenerative frequency divider.

3.7 Design Example of A Divide-by-2.25/4.5

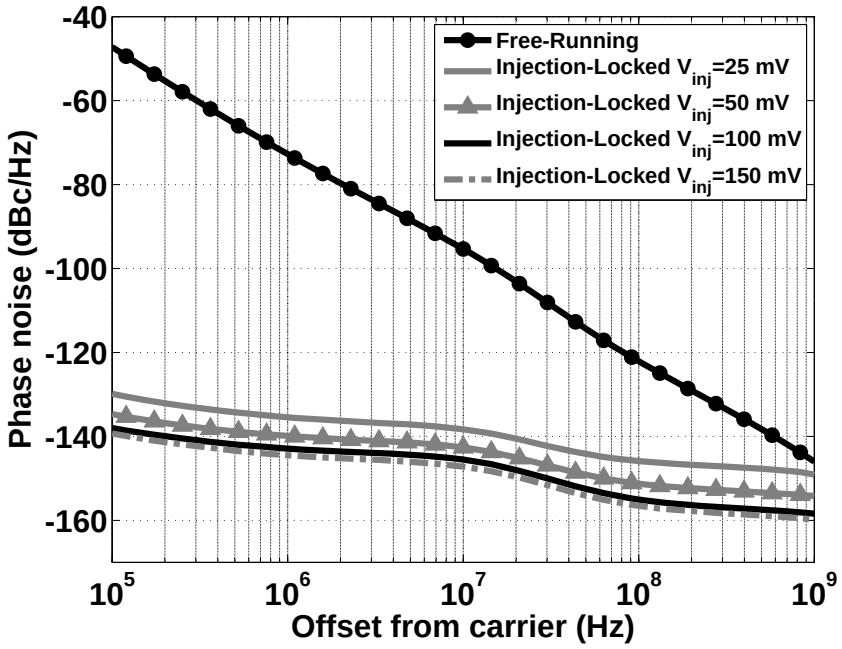
As mentioned earlier, one of the benefits of the injection-locked regenerative frequency divider is its ability to obtain fractional division ratios while providing 50% duty cycle quadrature output phases. In this section we present a design example of an injection-locked regenerative frequency divider that generates a fractional division ratio.

One of the design goals is to achieve a design suitable for implementation in a digital CMOS submicron technology using no on-chip inductor. This goal implies using ring-oscillators with resistive loads and also exploiting SSB mixers in the injection-locked regenerative frequency divider. The latter requires availability of quadrature phases of both the input to the frequency divider, and its output, or more precisely, the output of the feedback path.

There are several ways to provide quadrature phases of input, such as using polyphase filters, or preceding the divide-by-2.25 by another frequency divider or a ring-oscillator that can generate quadrature output phases. As previously stated, a block with quadrature outputs in the forward path is required to generate quadrature output phases. A divide-by-two flip-flop is usually a good candidate for this purpose, since most divide-by-two circuits can provide quadrature output phases. On the other hand, any oscillator that is injection-locked to its second harmonic can be used as a divide-by-two. Two-stage, or four-stage, ring-oscillators are good examples that serve as divide-



(a)



(b)

Figure 3.17: Phase noise of the prototype two-stage ring-oscillator (a) calculated phase noise from (3.60) vs. simulated free-running phase noise, and (b) simulated phase noise when injection-locked to a noise-less injection signal for different values of injection signal (external signal is injected to both of the delay cells).

by-two circuits and provide quadrature outputs.

Figure 3.18 shows a fractional frequency divider based on the general architecture of Fig. 3.1(c). This frequency divider is primarily designed to obtain a division ratio of 2.25 to be used for frequency synthesis for Multiband OFDM UWB that will be discussed in Chapter 4. As shown in Fig. 3.18, an injection-locked frequency divider (ILFD) implemented using a two-stage ring-oscillator with negative resistance delay cells is used in the forward path. An ILFD can operate with smaller input drive, and it also has the speed advantage when compared to static frequency dividers.

The feedback path consists of a cascade of two flip-flop-based CML divide-by-two circuits. Using divide-by-two blocks in the feedback path provides quadrature phases for the operation of SSB mixer.

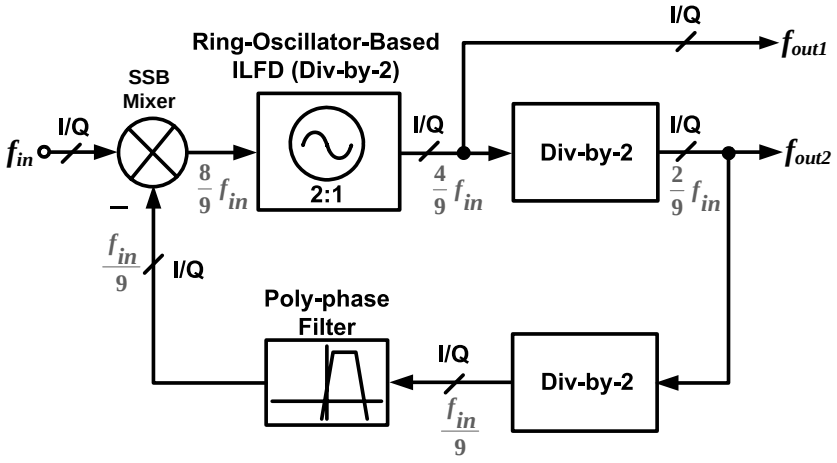


Figure 3.18: Block diagrams of a divide-by-2.25/4.5 with quadrature outputs and 50% duty cycle using an injection-locked regenerative frequency divider architecture.

From (3.1) it can be concluded that in the steady-state, $f_{out1} = f_{in}/2.25$ and $f_{out2} = f_{in}/2.25$. Therefore, the frequency divider of Fig. 3.18 achieves division ratios of both 2.25 and 4.5. In contrast to the previous approaches [29], no on-chip inductor is required to implement this function.

The input signal to the frequency divider can be applied to either the RF port (Gm-stage) or the LO port of the SSB mixer. When it is connected to the RF port, as shown in Fig. 3.19(a), the divider achieves a better input sensitivity; thus, it can function with smaller input power. On the other hand, the output of the feedback path

frequency divider is fed to the LO port. The large swing of the CML divider output is suitable for saturation operation of the LO port of the mixer. However, in this case, all the odd harmonics of the feedback signal contribute to in-band mixing products at the mixer output since the feedback signal is at a lower frequency than the input signal. Consequently the signal at the output of the mixer can achieve a non-50% duty cycle which leads to the I/Q phase inaccuracy at the final output of the main frequency divider. Moreover, as shown in [20], any frequency spur at the input of a divide-by-two translates to a spur at the output of the divider at the same offset frequency.

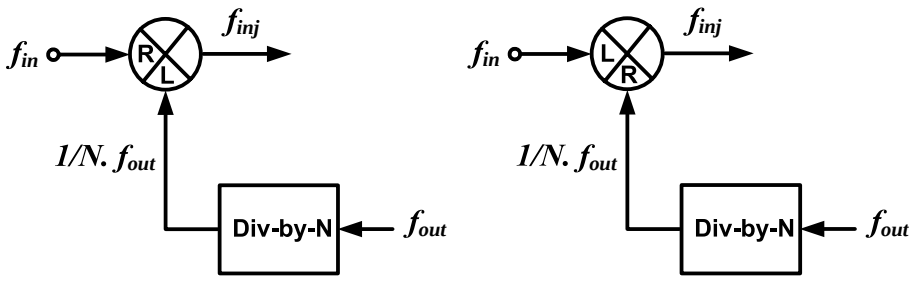


Figure 3.19: Block diagrams of the injection-locked regenerative frequency dividers with quadrature outputs and 50% duty cycle, (a) a with fractional division ration (2.25 and 4.5), (b) with integer division ratio (divide-by-three).

To solve these issues, one can use the scheme shown in Fig. 3.19(b) in which the input signal, which is at a greater frequency than the feedback signal, is applied to the LO port of the SSB mixer. In this scheme the feedback signal is applied to the RF port (Gm-stage) of the mixer. The contribution of the feedback signal to higher-order in-band mixing products can be minimized by linearizing the Gm-stage of the mixer. In addition, the feedback signal, which is rich in harmonics, can go through harmonic suppression filtering. In the presence of the quadrature phases of the feedback signal, a polyphase filter can be used since: (1) It provides balanced loading for all the outputs of the feedback frequency divider. (2) It can achieve better harmonic suppression by generating imaginary zeros. (3) It does not require any on-chip inductor or balun. The drawback of the scheme shown in Fig. 3.19(b) is the degraded input sensitivity of the resultant frequency divider.

In this scheme, if the input signal is smaller than required for the saturation operation of the mixer LO port, the amplitude of the mixer output signal depends on the input amplitude, and hence could be small. As previously stated, using an ILFD in the forward path of the divide-by-2.25 has the advantage that it can operate with smaller input drive. As a result, it can guarantee robust operation of the injection-locked regenerative divider of Fig. 3.18.

As was discussed in Section 3.4, the choice of this ILFD, or generally the forward path oscillator, is directly tied to the stability of the injection-locked regenerative divider. Nonetheless, using an ILFD mandates careful analysis and simulations to make sure that the it has a wide enough locking range to compensate for process variations. A ring-oscillator based ILFD has wider locking range compared to LC oscillator. In addition, it can provide multiple phases of output, occupies smaller area on silicon, and is more compatible with the digital CMOS technology.

As was shown in Section 3.4, the locking range of the injection-locked regeneration divider follows the locking range of its oscillator. The input to the RF port of the mixer (Fig. 3.18) is set by the output of its preceding frequency divider. So, in order to control the amplitude of $V_{inj}(t)$, the amplitude of the input to the LO port of the mixer is varied. The simulated locking range of this divider is shown in Fig. 3.20 and is compared with the locking range of the two-stage negative resistance-based ring-oscillator. As can be seen, the simulation result is in a very good agreement with the expected locking range.

Figure 3.21 shows the simulated free-running and locked phase noise of the frequency divider for an output frequency of 4 GHz when a noise-less input signal is input to the divider. The amplitude of the injection signal is changed by changing the amplitude of the input to the LO port of the mixer.

From (3.58) we expect to obtain similar output phase noise to those in Fig. 3.17, and comparing Fig. 3.21 and Fig. 3.17 shows a very good agreement.

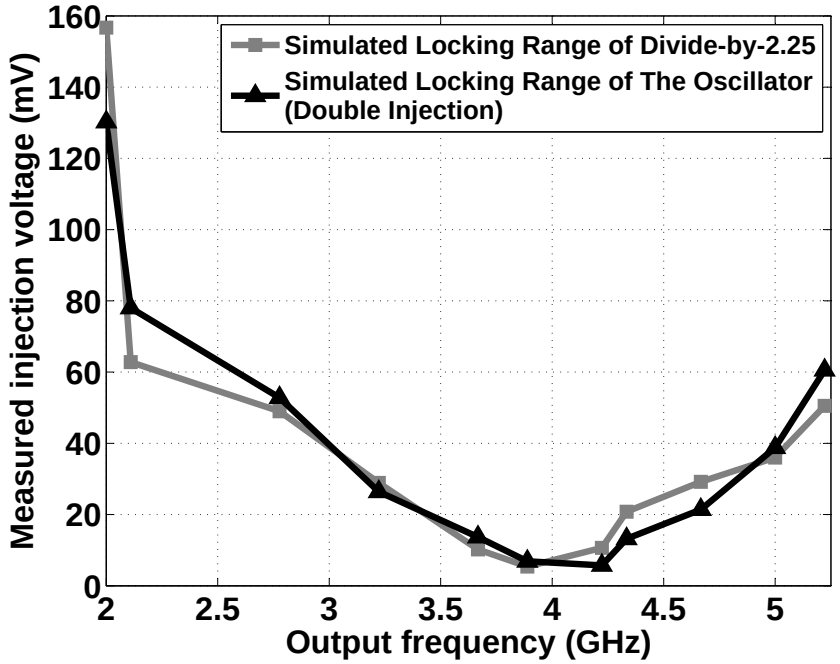


Figure 3.20: Simulated locking range of the prototype divide by 2.25/4.5, and comparison with the locking range of the oscillator used in it.

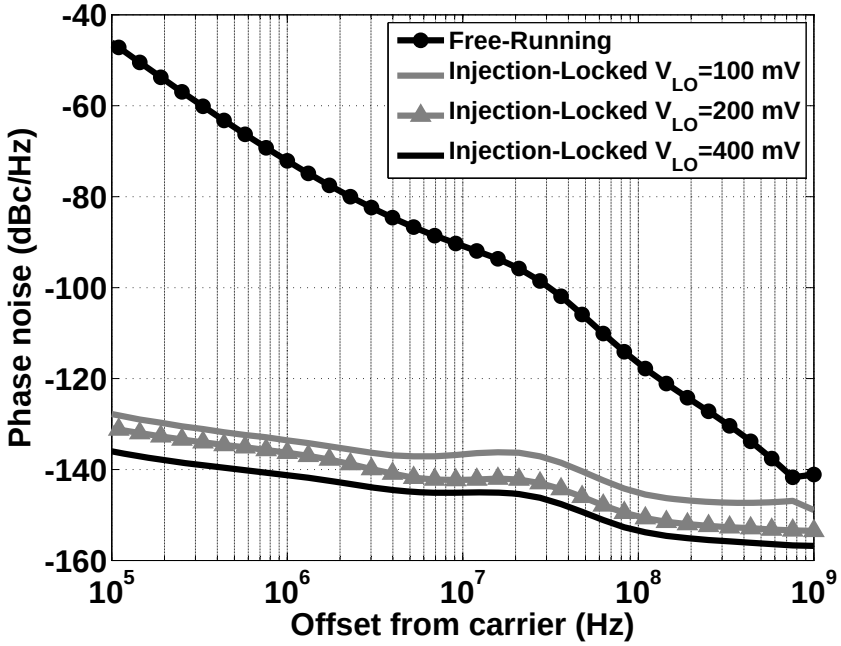


Figure 3.21: Simulated free-running and injection-locked phase noise of the prototype divide by 2.25/4.5 for different LO amplitudes.

3.8 Conclusion

This chapter presented an analysis of the operation, stability, locking range, and phase noise of injection-locked regenerative frequency dividers. In addition, the injection-locked behavior of two-stage ring-oscillators (based on negative resistance delay cells) is studied and their locking range is derived for the first time. Finally, a design technique was presented for implementing a regenerative frequency divider in a digital CMOS technology (using no on-chip inductor or balun) for achieving fractional division ratios with a 50% duty cycle quadrature output phases. The circuit simulation results of the designed oscillator and the fractional injection-locked regenerative frequency divider are in excellent agreement with the calculations.

This chapter has been submitted in part to the following publication:

- M. Farazian, P. S. Gudem, and L. E. Larson, "Stability and Operation of Injection-Locked Regenerative Frequency Dividers", *IEEE Transactions on Circuits and Systems-I: Regular Papers*, (in review).

Chapter 4

An inductor-less CMOS 14-band Frequency Synthesizer for UWB

4.1 Introduction

One of the challenges in implementing a frequency synthesizer for the emerging Multi-band OFDM (MB-OFDM) UWB standard is overcoming the agility limitations of conventional synthesizers. The MB-OFDM proposal for UWB divides the spectrum from 3.1 GHz to 10.6 GHz into 14 different bands, and frequency hops at the rate of 3.2 MHz between them [43] with a specified frequency settling time of only 9.5 nS. The EVM requirements also pose challenging constraints on the spurious performance. Design techniques that eliminate the use of on-chip inductors, and which are compatible with low voltage operation, are critical for increasing the level of integration for future implementations.

An inductor-less design methodology may have several advantages over traditional design techniques: (1) While the area required to implement an on-chip inductor does not scale down in the finer technology nodes, inductor-less designs benefit from technology scaling. (2) On the other hand, the quality factor of the on-chip inductors may worsen in finer technology nodes, which can lead to an increase in the required current consumption to generate a given voltage swing. (3) It is more straightforward to port an inductor-less design into a new technology node. The penalty for an inductor-

less design methodology is a slightly increase in the current consumption to achieve the necessary gain and voltage swing in the absence of inductors.

Most 14-band MB-OFDM UWB synthesizers are based on the method of frequency division and mixing [21, 44, 22]. This approach helps to overcome the agility problems of conventional frequency synthesizers, and it can be expanded to cover a large number of frequency bands. However, it is challenging to realize a hardware and power efficient implementation using this approach that meets the UWB specifications at all frequencies. In previous synthesizer implementations, a significant percentage of the die area is taken by on-chip inductors. In addition, UWB synthesizers often use multiple PLL's and several mixing stages, which together occupy a large die area.

In this work, appropriate frequency planning, harmonic suppression polyphase filters, and low-voltage linearization techniques in the SSB mixers allowed us to remove the on-chip inductors in the synthesizer, while achieving sidebands as low as -38 dBc. This approach reduces die area and improves integrability with digital circuits, but may increase the power consumption. So low-power design techniques are essential.

4.2 Synthesizer Architecture

The latest band groups and band allocation for MB-OFDM UWB is shown in Fig. 4.1. It consists of 6 band groups, and 14 individual bands, as described in [7]. Figure 4.1 also shows the frequency plan for the synthesizer. Each of the center frequencies for MB-OFDM can be expressed as

$$f_c = (5.5 + n) \times 528\ MHz \tag{4.1}$$

where n is the band number from 1 to 14. This implies that fractional frequency division is required to synthesize the channel spacing (528 MHz) from any of the band center frequencies.

Moreover, the frequency plan of Fig. 4.1 requires quadrature phases of 1.584 GHz and 3.168 GHz (three and six times the channel spacing respectively). For this purpose, the center frequency of Band 8 is very useful, since all the required translation

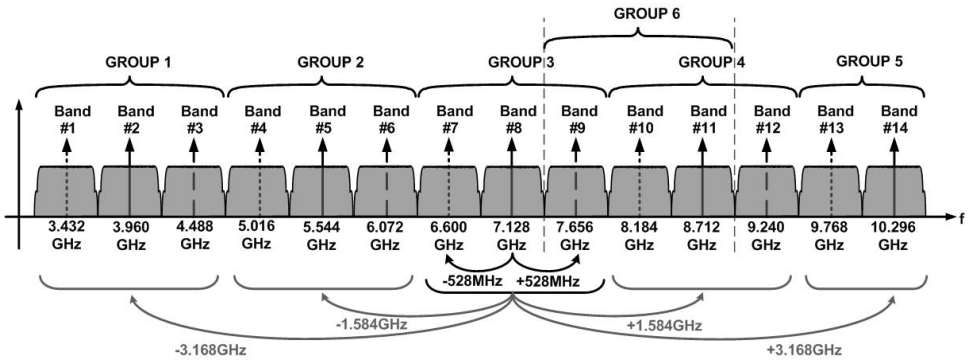


Figure 4.1: Proposed UWB synthesizer frequency plan.

frequencies (528 MHz, 1.584 GHz and 3.168 GHz) can be derived from it when the fractional frequency dividers of Fig. 4.2 are used, in a similar manner to the 3-band synthesizer of [29]. Figure 4.2 shows our proposed architecture to implement the frequency plan shown in Fig. 4.1.

The proposed frequency synthesizer uses a single external 14.256 GHz input. Quadrature signals for the operation of the first mixing stage are generated from a ring-oscillator-based Injection Locked Frequency Divider (ILFD) whose output is the center frequency of Band 8. The channel spacing of 528 MHz is obtained from the output of two additional regenerative dividers, with total division ratio of 13.5. A cascade of quadrature output divide-by-2.25, divide-by-2, and divide-by-3 circuits provides the required frequencies. As shown in Fig. 4.2, two similar frequency dividers are used to generate quadrature phases at 7.128GHz. This scheme avoids any I/Q amplitude or phase mismatch induced due to routing, compared to the case when only one frequency divider is used.

4.3 Circuit Design

In order to achieve a compact design, and also for further compatibility with digital CMOS technology, an inductor-less design methodology is adopted. On-chip inductors can significantly reduce the spurious tones, and improve the voltage gain and swing at RF frequencies. In this work, a combination of SSB mixers, polyphase filters,

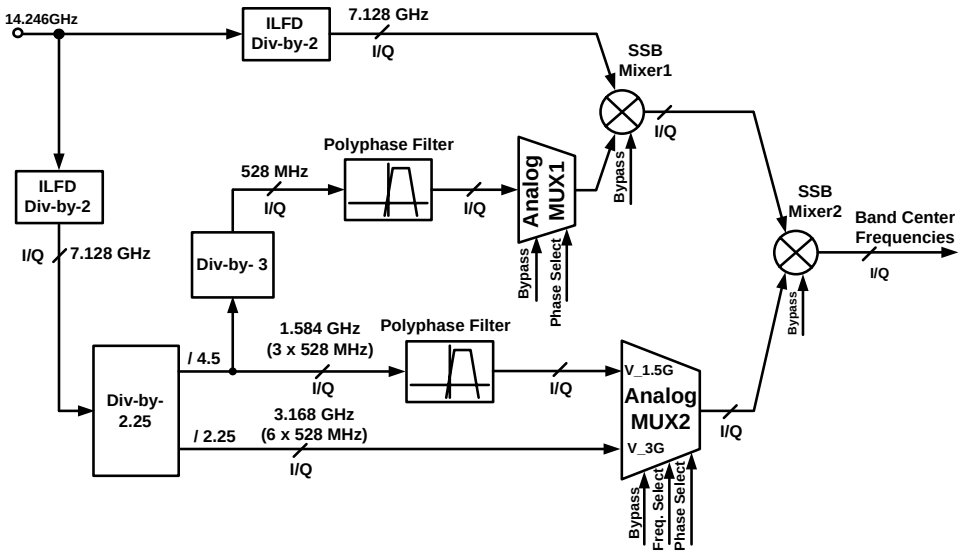


Figure 4.2: Architecture for the universal 14-band UWB frequency synthesizer.

and appropriate linearization techniques help to meet the spurious requirements in the absence of on-chip inductors. A combination of different amplifier topologies is used to achieve the required voltage gain for interfacing between different blocks. Low-voltage design techniques are employed to make this implementation feasible at 1.2 V supply. In this section, circuit implementation details of the key blocks are presented.

4.3.1 Frequency Dividers

As was discussed in Section 4.2, implementation of the frequency synthesizer of Fig. 4.1 requires 528 MHz, 1.584 GHz, 3.168 GHz, and 7.128 GHz. The cascade of frequency dividers shown in Fig. 4.2 suggests a hardware efficient way to obtain all these required frequencies from a 14.256 GHz source. But these frequency dividers must also provide quadrature output phases. In addition, proper operation of the SSB mixers, with adequate LO leakage suppression requires input mixing signals with 50% duty cycle. It is straightforward to implement a divide-by-2 with quadrature outputs and a 50% duty cycle at the output. However, divide-by-3 circuits often have a non-50% duty cycle at the output, and achieving quadrature output phases is difficult [21, 45]. Lastly, frequency dividers with fractional division ratios (2.25 and 4.5) with 50% duty cycle and quadrature outputs are required.

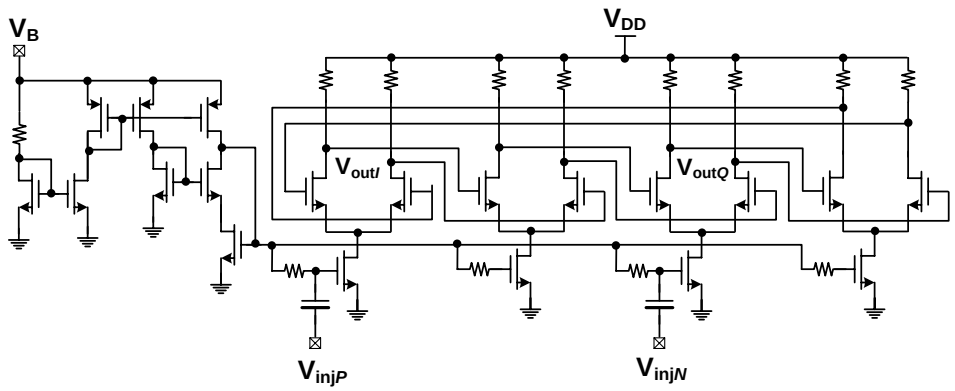


Figure 4.3: Schematic of the four-stage ring-oscillator-based ILFD implemented using resistive load differential pair delay cell.

The front-end divide-by-2 circuit in Fig. 4.2 is implemented using a four-stage ring-oscillator-based ILFD shown in Fig. 2.3. There are at least two advantages in using ILFD's instead of static frequency dividers: (1) The ILFD's operate at higher frequencies compared to static frequency dividers. (2) ILFD's require significantly smaller input drive for proper operation. The speed criteria changes for different CMOS technologies, since static frequency dividers can achieve faster speeds in finer technology nodes. However, the required input drive of ILFD's is lower than that of static frequency dividers. This becomes more important at higher frequencies, where achieving large voltage signal swing is difficult. An inductor-less design methodology makes it even harder to achieve adequate input drive for operation of the static frequency dividers. This is the primary motivation for choosing an ILFD for the front-end frequency divider.

As shown in chapter 2, the four-stage ring-oscillator-based frequency divider of Fig. 4.3 can achieve a division ratio of two with an input at approximately twice the self-resonance frequency (SRF), where the proper amplitude is applied. In this work, a single phase 14.256 GHz input is applied to the tail current source of the first delay stage. This frequency divider provides quadrature phases at 7.128 GHz, which will be used by the SSB mixer, and other frequency dividers. It was shown in 2 that when the frequency divider of Fig. 4.3 operates as a divide-by-2, it can achieve a locking range of greater than 25% around its SRF, which is greater than the simulated variation of its SRF at different process corners. Therefore, a wide locking range guarantees the proper

operation of the ILFD after fabrication.

Regenerative frequency dividers [30] are a technique to obtain fractional division ratios. However, as was discussed in Chapter 3, regenerative frequency dividers usually require some tuned circuit in the forward path. Moreover, they usually do not provide quadrature output phases [30]. In this work, in order to achieve both fractional division ratio and quadrature output phases, an injection-locked regenerative frequency divider is used.

Figure 3.18 shows our proposed divide-by-2.25 circuit. It is designed using t the procedure described in Section 3.7, operates at an input frequency of 7.128 GHz, achieves division ratios of both 2.25 and 4.5, and provides quadrature outputs with a 50% duty cycle. In contrast to the previous approaches [29], this frequency divider is implemented using no on-chip inductor.

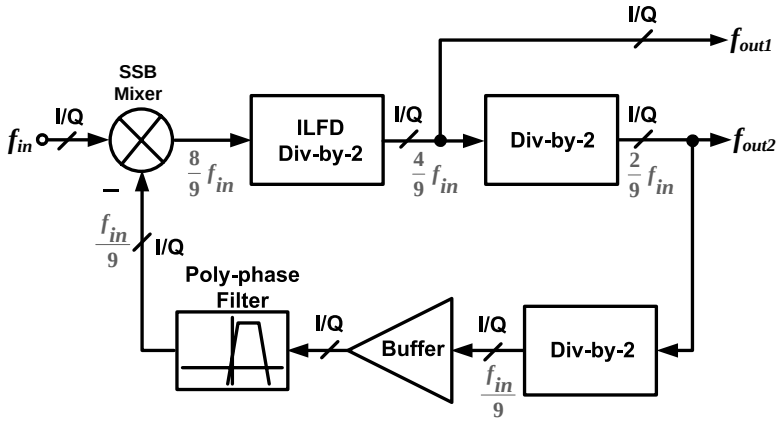


Figure 4.4: Block diagram of the injection-locked regenerative divide-by-2.25

An ILFD divide-by-two, implemented using a two-stage ring-oscillator (with negative resistance stages), is used in the forward path, and a cascade of two CML divide-by-2 circuits is used in the feedback path. As was discussed earlier, an ILFD is chosen in the feed-forward path of the divide-by-2.25 because it can operate with smaller input drive, and also for its speed advantage over a static frequency divider. Careful analysis and simulations are done to make sure that the ILFD has a wide enough locking range for robust operation of the divide-by-2.25 in the presence of process variations. The stability and locking range of this frequency divider was discussed in 3.

In order to make the divider chain hardware efficient, the divide-by-2.25 and its subsequent divide-by-2 are combined together. So, in Fig. 3.18, we propose a modified frequency divider architecture that achieves division ratios of both 2.25 and 4.5.

In a similar fashion, an injection-locked regenerative divide-by-3, composed of a CML divide-by-2 in the forward path, and a low-pass filter in the feedback path is shown in Fig. 4.5. Despite the use of conventional divide-by-3 circuits, this divider can provide a 50% duty cycle quadrature outputs.

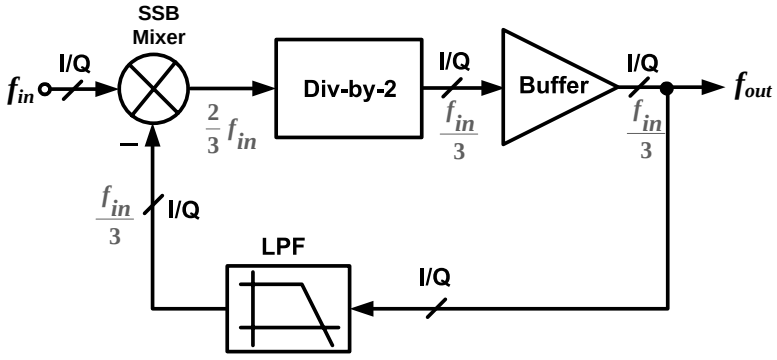


Figure 4.5: Block diagram of the injection-locked regenerative divide-by-3 with a 50% duty cycle quadrature outputs.

The second output of the divide-by-2.25, f_{out2}, is fed to the divide-by-3, to generate the channel spacing for operation of $SSB\ Mixer1$.

4.3.2 Linearity Considerations

An architecture based on the method of frequency division and mixing may suffer from spurious tones arising from the mixing. One method for spurious tone mitigation is a combination of SSB mixers with tuned loads [21]. However, in the absence of on-chip inductors, or generally any frequency selective load at the output of the mixers, the best approach is the use of SSB mixers along with linearization techniques. In this case, not only must the mixer be linearized, but the harmonic content of the inputs to the mixer must also be reduced [12]. Careful layout techniques play a very critical role in this case.

As was discussed earlier, the outputs of the frequency dividers are used for fre-

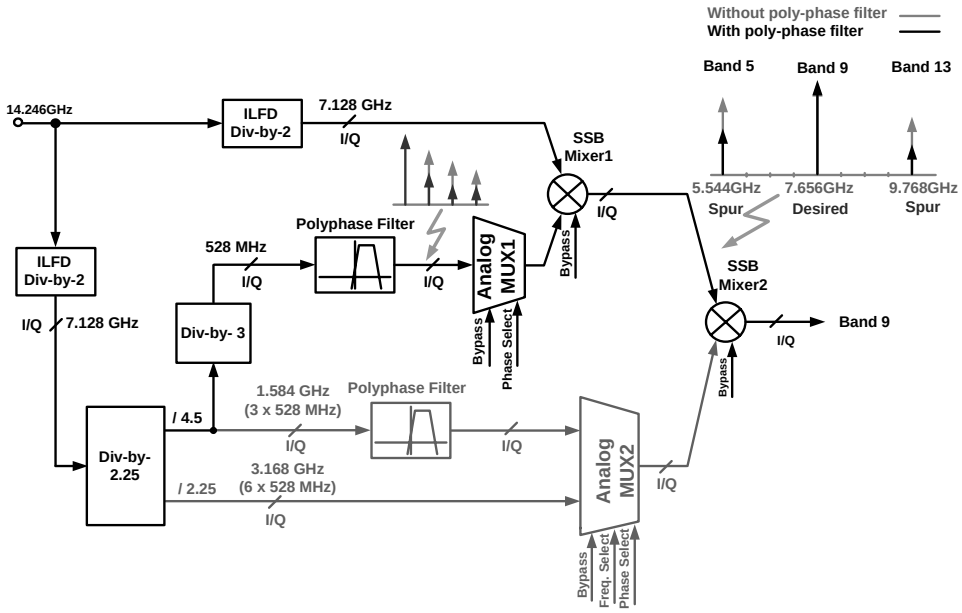


Figure 4.6: The effect of polyphase filter on side-band reduction.

quency mixing. These signals are rich in harmonics. The worst case is the output of the divide-by-3 in Fig. 4.2 which is at 528 MHz. When the harmonics of 528 MHz contribute to mixing, they generate the center frequency of other bands. Depending on the process corner and the temperature, the output of this divider has a frequency roll-off proportional to $1/k^2$ when it is a triangular waveform, or proportional to $1/k$ when it is a square waveform. System simulations based on these waveforms reveal that at least 20 dB of attenuation of the third harmonic of the divide-by-3 output is required in order to meet the spurious level requirement of MB-OFDM UWB. In this frequency synthesizer, the output of the divide-by-3 and the output of the divide-by-4.5 are filtered prior to mixing. As will be discussed in Section 4.3.3, a combination of RC polyphase filters meets these requirements. Figure 4.6 shows a simulation of the spurious tones at the mixer output with and without polyphase filter spur reduction.

Mixer linearization is also a key in meeting the spurious specifications, and will be discussed in Section 4.3.4.

4.3.3 Polyphase Filter

As was discussed in Section 4.3.2, the filter preceded by the divide-by-3 needs to provide over 20 dB suppression of the third harmonic of 528 MHz. To meet the emission requirements of MB-OFDM UWB, other harmonics of 528 MHz need to be lower than -40 dBc with respect to the fundamental. One way to do this is by generating a filter with imaginary zeros to cancel the harmonics. When on-chip inductors are not available, an alternative method is to use RC polyphase filters [46],[47]. This method is available, since quadrature phases at all the intermediate and output nodes are available.

Figure 4.7(a) shows an RC polyphase filter. The relationship between the inputs and outputs of this filter is

$$\begin{bmatrix} V_{O_{I+}}(s) \\ V_{O_{Q+}}(s) \\ V_{O_{I-}}(s) \\ V_{O_{Q-}}(s) \end{bmatrix} = \begin{bmatrix} a(s) & b(s) & 0 & 0 \\ 0 & a(s) & b(s) & 0 \\ 0 & 0 & a(s) & b(s) \\ b(s) & 0 & 0 & a(s) \end{bmatrix} \begin{bmatrix} V_{I_{I+}}(s) \\ V_{I_{Q+}}(s) \\ V_{I_{I-}}(s) \\ V_{I_{Q-}}(s) \end{bmatrix} \tag{4.2}$$

where $a(s)$ and $b(s)$ are defined as

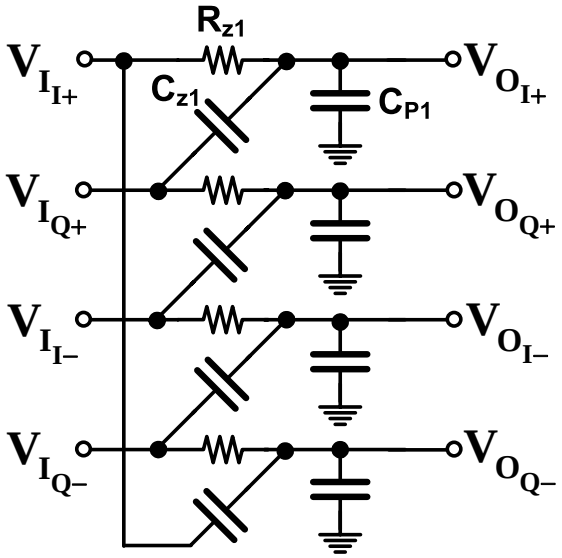
$$a(s) = \frac{1}{1 + sR_{z1}(C_{z1} + C_{p1})} \tag{4.3a}$$

$$b(s) = \frac{sR_{z1}C_{z1}}{1 + sR_{z1}(C_{z1} + C_{p1})} \tag{4.3b}$$

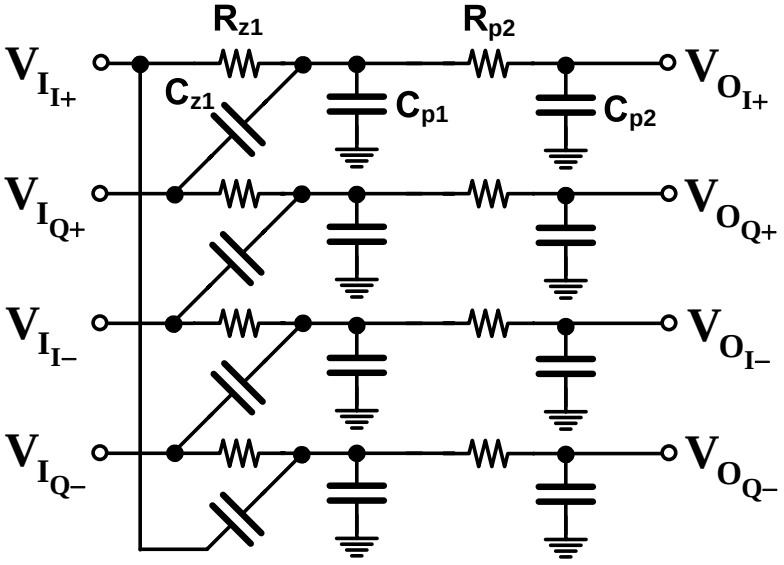
When the filter shown in Fig. 4.7(a) is driven by quadrature inputs, its transfer function can be simplified as

$$\frac{V_O}{V_I}(s) = \frac{1 \pm jsR_{z1}C_{z1}}{1 + sR_{z1}(C_{z1} + C_{p1})} \tag{4.4}$$

The $\pm$ in (4.4) depends on the quadrature input sequence. The plus corresponds to a counter-clockwise sequence of the inputs, while the minus sign corresponds to a clockwise sequence. The transfer function in (4.4) has an imaginary zero at $\pm j/R_{z1}C_{z1}$ and a real Left Half Plane (LHP) pole at $-1/R_{z1}(C_{z1} + C_{p1})$. At high frequencies, the gain of this transfer function is $C_{z1}/(C_{z1} + C_{p1})$. To further reduce the gain at high



(a)



(b)

Figure 4.7: (a) Implementation of an imaginary zero (b) Adding a real pole to maintain the roll-off

frequencies, another pole is added to the polyphase filter. This new filter is shown in Fig. 4.7(b). The transfer function can be described by (4.2), where $a(s)$ and $b(s)$ are

$$a(s) = \frac{1}{a_2 s^2 + a_1 s + 1} \tag{4.5a}$$

$$b(s) = \frac{s R_{z1} C_{z1}}{a_2 s^2 + a_1 s + 1} \tag{4.5b}$$

The a_1 and a_2 coefficients in (4.5a) and (4.5b) are

$$a_1 = R_{z1}(C_{z1} + C_{p1} + C_{p2}) + R_{p2} C_{p2} \tag{4.6a}$$

$$a_2 = R_{z1} R_{p2} (C_{z1} + C_{p1}) C_{p2} \tag{4.6b}$$

When quadrature inputs are applied to the input of Fig. 4.7(b), its transfer function can be simplified to

$$\frac{V_O}{V_I}(s) = \frac{1 \pm j s R_{z1} C_{z1}}{a_2 s^2 + a_1 s + 1} \tag{4.7}$$

When compared to Fig. 4.7(a), the location of the imaginary zero is unchanged, and the filter achieves two LHP real poles. Moreover the gain of Fig. 4.7(b) goes to zero at high frequencies, which is desirable to suppress higher-order harmonics. This filter is suitable for the output of the divide-by-4.5 because the output of this frequency divider (1.584 GHz) is triangular shaped. Therefore, its harmonics have a frequency roll-off proportional to $1/k^2$ and the third harmonic is roughly 20 dB smaller than the fundamental, and the fifth harmonic is roughly 28 dB lower than the main harmonic. As a result, and from simulations, a single zero and two real poles provide sufficient attenuation of higher-order harmonics.

In addition, the gain of the multiplexers and the Gm stage of the mixer is lower for the harmonics of 1.584 GHz. This relaxes the design requirements of the filter after the divide-by-4.5 circuit. On the other hand, these two conditions are not true for the output of the divide-by-3 (528 MHz). Therefore a higher-order filtering is required for that divider.

Frequency dividers usually generate the quadrature output phase by delaying the output by a quarter period. Delaying a periodic signal by a quarter period leads to a

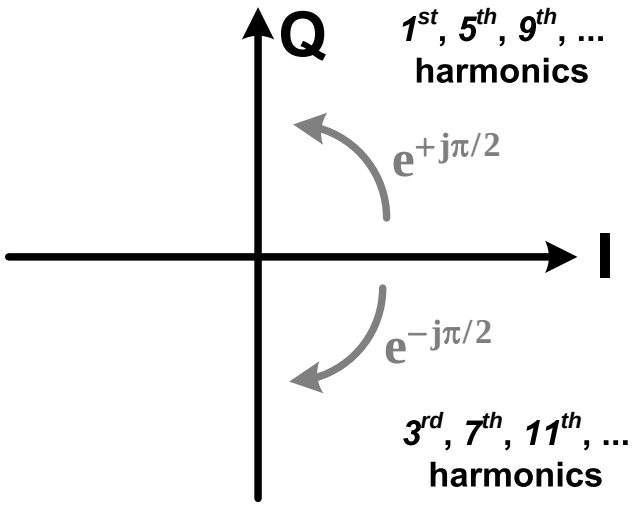


Figure 4.8: I/Q phase sequence for different harmonics at the output of the frequency divider.

phase shift of $-jn\pi/2$ of its n^{th} harmonic. In the case of a waveform with odd symmetry, which only contains odd harmonics, the $(4k+1)^{st}$ harmonics of the frequency divider output have a counter-clockwise quadrature sequence $\big(exp(+j\pi/2)\big)$, while the $(4k+3)^{rd}$ harmonics have a clockwise quadrature sequence $\big(exp(-j\pi/2)\big)$, where k takes any positive integer number, including zero. This is illustrated in Fig. 4.8.Therefore, when the harmonics are significant, we need at least two imaginary zeros, for the harmonics with different quadrature sequences.

A higher-order polyphase filter can be obtained by cascading the filters shown in Fig. 4.7(a) and Fig. 4.7(b). If one inserts a buffer between these stages, the location of the poles and zeros of the overall transfer function will be the same as in the individual stages. However, this becomes challenging in a CMOS implementation since CMOS source-followers are quite lossy at these frequencies [48].

It can be shown that when cascading the polyphase filters of Fig. 4.7(a) and Fig. 4.7(b) - even without inserting a buffer between the stages - the location of the imaginary zeros is preserved. This eases the design and control of the zeros of the overall transfer function. However, the poles of the combined polyphase filter will change as a result of the interconnection.

On the other hand, cascading these passive RC stages increases the insertion loss

of the overall filter. Here, two polyphase stages, similar to the one shown in Fig. 4.7(a) but with different quadrature sequences, are used to achieve adequate attenuation of all the close-in harmonics. In order to increase the roll-off of the mixer at high frequencies, an extra pole is added to the network, as in Fig. 4.7(b).

The resultant polyphase filter is shown in Fig. 4.9(a).

If we assume that the input of Fig. 4.9(a) is driven by quadrature inputs, its transfer function can be written as

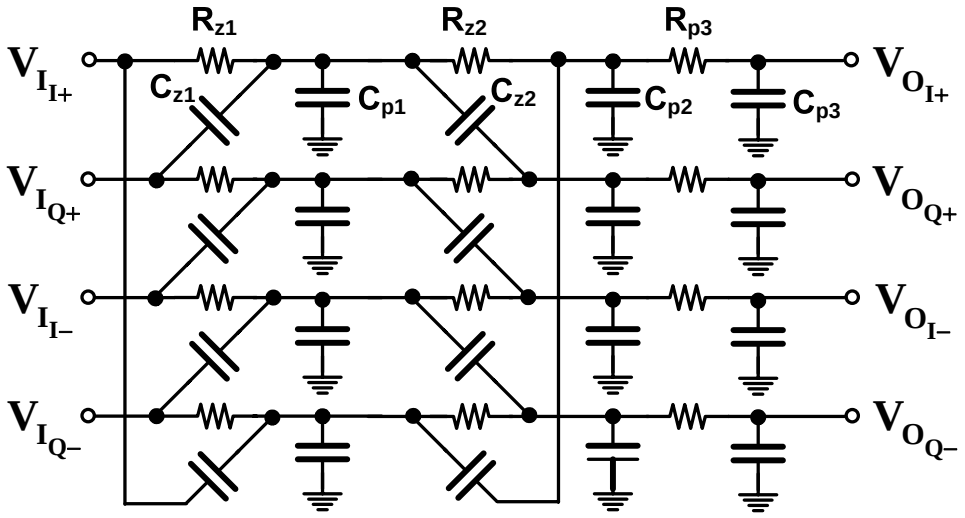
$$\frac{V_O}{V_I}(s) = \frac{(1 \pm jsR_{z1}C_{z1})(1 \mp jsR_{z2}C_{z2})}{a_3s^3 + a_2s^2 + a_1s + 1} \tag{4.8}$$

where the coefficients of the denominator of (4.8) are

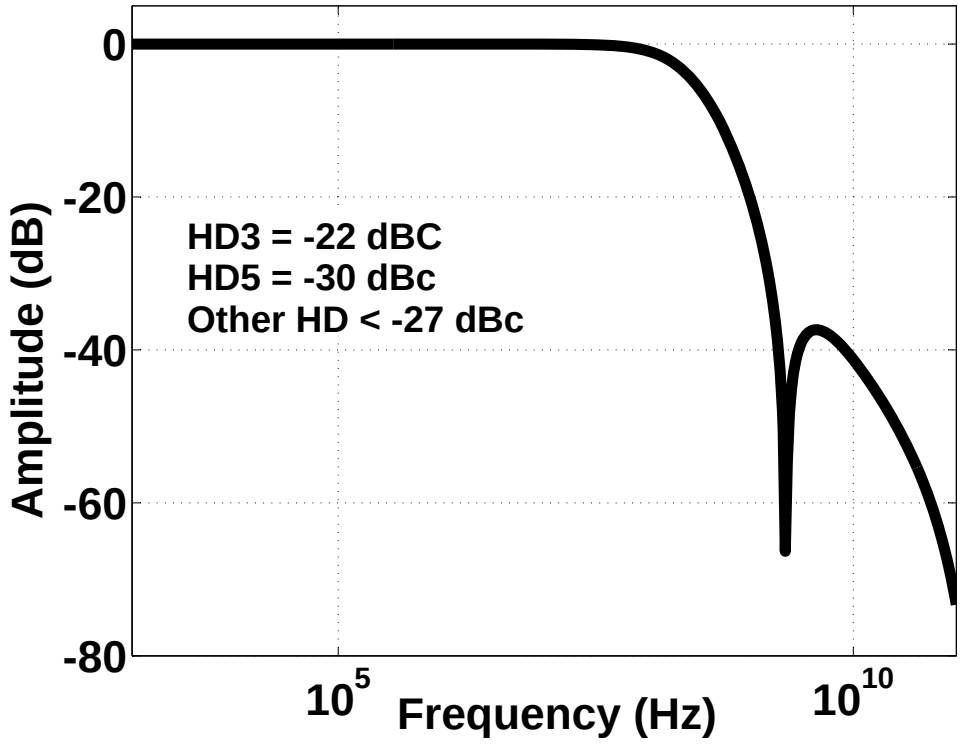
$$\begin{aligned} a_1 &= R_{p3}C_{p3} + R_{z1}(C_{z1} + 2C_{z2} + C_{p1} + C_{p2} + C_{p3}) \\ &\quad + R_{z2}(C_{p2} + C_{z2} + C_{p3}) && \text{(4.9a)} \\ a_2 &= R_{z1}R_{z2}\Big((C_{p1} + C_{z1})(C_{p2} + C_{p3} + C_{z2}) + C_{z2} \\ &\quad (c_{p2} + C_{p3})\Big) + R_{z1}R_{p3}C_{p3}(C_{z1} + 2C_{z2} + C_{p1} + C_{p2}) \\ &\quad + R_{z2}R_{p3}C_{p3}(C_{p2} + C_{z2}) && \text{(4.9b)} \\ a_3 &= R_{z1}R_{z2}R_{p3}C_{p3}\Big((C_{p1} + C_{z1})(C_{p2} + C_{z2}) + C_{p2}C_{z2}\Big) && \text{(4.9c)} \end{aligned}$$

The transfer function in (4.8) has imaginary zeros at $\pm j/R_{z1}C_{z1}$ and $\mp j/R_{z2}C_{z2}$. When $R_{z1} = R_{z1} = R_z$ and $C_{z1} = C_{z2} = C_z$, this filter has a pair of complex conjugate imaginary zeros at $\pm j/R_zC_z$. This guarantees a symmetric response for the clockwise and counter-clockwise harmonics while leveraging the properties of the polyphase filters in implementing imaginary zeros. The frequency response of the polyphase filter of Fig. 4.9(a) is shown in Fig. 4.9(b). This shows more than 22 dB attenuation for the third harmonic of 528 MHz, and roughly 30 dB attenuation of its fifth harmonic. All other harmonics are attenuated by more than 27 dB.

To make the polyphase filters less sensitive to the parasitics, all the capacitors are chosen to be larger than 200 fF. Monte Carlo simulations are performed to examine the effects of process variation and mismatch on the performance of the polyphase filters.



(a)



(b)

Figure 4.9: Two-stage polyphase filter used to suppress the harmonics at the output of the divide-by-3 (a) schematic (b) simulated frequency response.

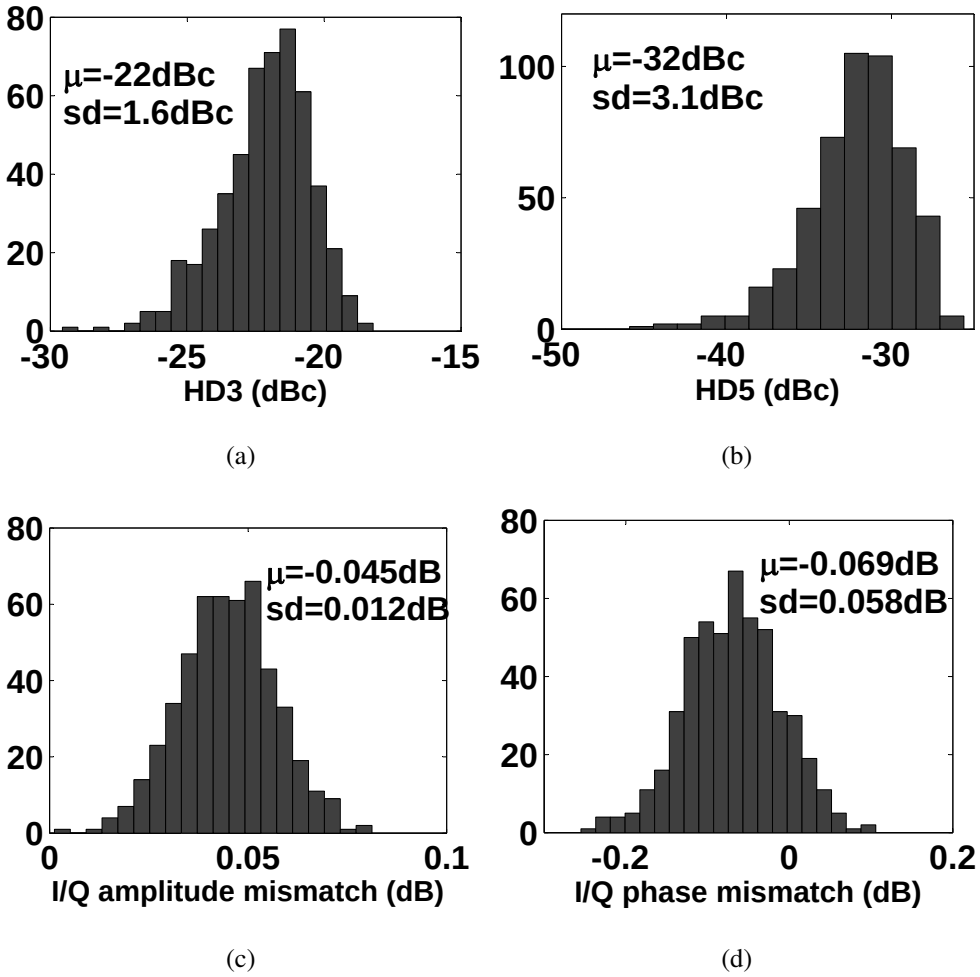


Figure 4.10: Monte Carlo simulation results of the 528MHz polyphase filter, (a) simulated HD3, (b) simulated HD5, (c) simulated differential I/Q amplitude mismatch, (d) simulated differential I/Q phase mismatch.

Figure 4.10 shows the simulated results of 500 runs of Monte Carlo simulation of the polyphase filter of Fig.4.9(a). As can be seen, the mean value of the HD3 is -22 dBc with a standard variation of 1.6 dBc. It is also observed that the I/Q amplitude and phase mismatches at the output of the polyphase filter respectively remain less than 0.1 dB and 0.2 degrees. Similar Monte Carlo simulations are performed for the polyphase filter of Fig. 4.7(b). In this case the mean value of HD3 is -22 dBc with a standard variation of 3.1 dBc, while the mean value of HD5 is -16 dBc with standard variation of 0.9 dBc. The I/Q amplitude and phase mismatches at the output of this polyphase filter are respectively less than 0.03 dB and 0.5 degrees. So, the process variation will not significantly degrade the performance of the polyphase filters.

4.3.4 SSB Mixer

The synthesizer uses differential quadrature signals throughout, so that SSB mixers can be employed. The function of the SSB mixers in this frequency synthesizer is to implement in-phase and quadrature phases of the sum or difference of two frequencies. $SSB\ Mixer1$ generates the center frequencies for the bands in Group 3. Depending on the target band and group, $SSB\ Mixer2$ will down-convert, up-convert or leave unchanged the output of $SSB\ Mixer1$.

Most of the frequency synthesizers that are implemented based on this method use inductive loads in the SSB mixers [21, 44, 22]. This is desirable for an efficient use of the headroom, achieving a large signal swing, and suppression of the spurious responses. However, when a resistive load is used at the output of the mixers, especially at 1.2 V or lower, the headroom problems becomes more challenging. To overcome headroom problems, the Gm stage of $SSB\ Mixer1$ is folded (Fig. 4.11), mirrored, and fed to the NMOS switching quad. In this case, the signal swing at the output of the mixer will not cause the Gm stage to enter the triode region. Moreover, the output stage has greater headroom, and achieving a larger signal swing at the output is feasible. But it increases the power consumption.

Both SSB mixers can be bypassed if necessary (for example, for synthesis of Band 8), by reconfiguring them as a differential pair that passes the LO frequency. Tran-

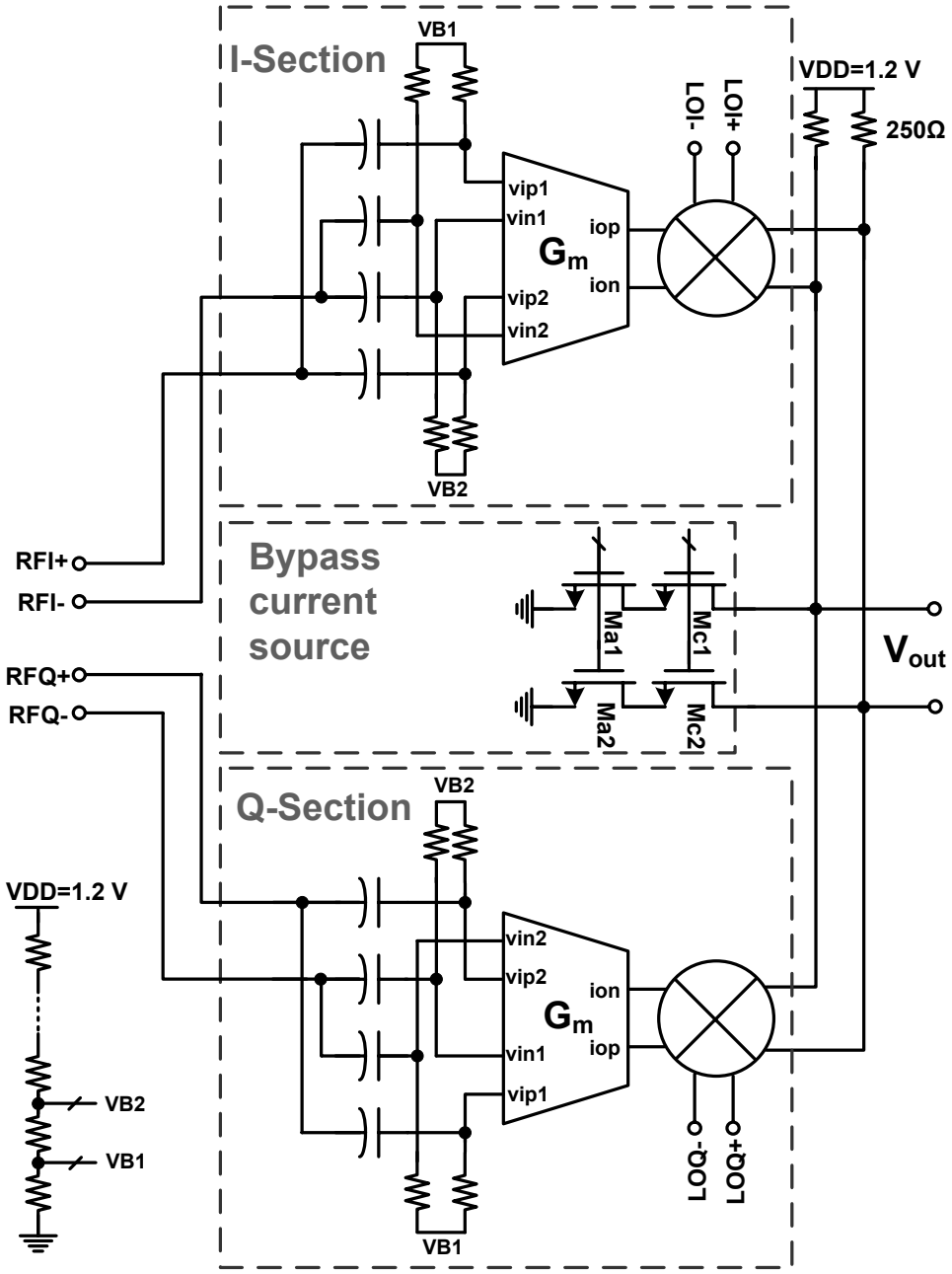


Figure 4.11: SSB mixing stage.

sistors $Ma1$ and $Ma2$ in Fig. 4.11 sink dc current to maintain a constant common-mode DC level in the two modes. This technique, along with a fast settle dc bias circuit that turns on $Ma1$ and $Ma2$ very quickly, results in a switching time of less than 2 nS for most of the switching scenarios. To adjust for I/Q mismatch, quadrature correction is embedded inside the LO buffer prior to $SSB\ Mixer1$ and $SSB\ Mixer2$. One remaining spurious output is the (fixed) LO to output leakage, which occurs through layout asymmetry, systematic offset in the mixers, and inductive coupling in the power supply lines, and which is roughly -20 dBc at 7.128 GHz. This can be further reduced through improved high-frequency packaging.

Because of its stringent linearity requirements $Analog\ Mux1$ is implemented using resistively degenerated differential pairs. $Analog\ Mux2$ selects the correct phase as well as the appropriate frequency. As shown in Fig. 4, it is composed of four Gm stages. In order to achieve sufficient swing with the low power supply, and also because of its moderate linearity requirements, inverter-based Gm stages are used for $Analog\ Mux2$. When $SSB\ Mixer2$ is in bypass mode, the Gm stages in $Analog\ Mux2$ are switched off and the output of $Analog\ Mux2$ is shorted to ground to provide better isolation.

The input frequencies to the $SSB\ Mixer1$ are 7.128 GHz and 528 MHz. Reduction of the spurious tones, due to 528 MHz signal, at the output of this mixer implies that: (1) the 528 MHz signal must have low harmonic content, (2) a linear Gm stage is needed in the mixer to avoid generating harmonics, and (3) a small amount of I/Q amplitude and phase mismatch is caused. The first requirement is met by means of polyphase filtering of the harmonics, as was discussed in Section 4.3.3. The I/Q amplitude and phase matching of (3) is achieved by careful symmetric layout.

The second requirement is achieved by linearizing the Gm stage of the mixer. Among all different methods of Gm linearization, we require a method that is suitable for low supply voltage and high frequencies, and yet does not reduce the conversion gain. Source-degeneration [49] leads to a reduction of the conversion gain of the mixer. In this work, the Gm stage of the mixer of Fig. 4.11 is linearized by using a multi-tanh Gm stage [50]. This technique provides a linear input range and does not degrade the gain of the Gm stage. The Gm stage is shown in Fig. 4.12(a), and the overall linearized

transconductance is plotted in Fig. 4.12(b). Voltages $VB1$ and $VB2$ in Fig. 4.11 are chosen to maximize the gain flatness for the desired input voltage range.

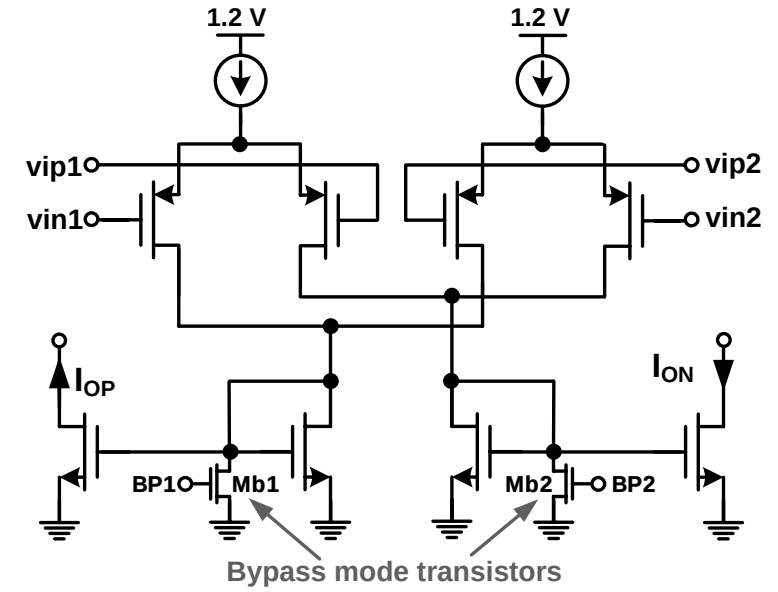
A fast bias circuit shown in Fig. 4.13(b) is used to reduce the time it takes the mixers to go to the bypass mode. Compared to the conventional bias circuit of Fig. 4.13(a), transistors $M4$, $M5$, and $M6$, are added. Transistor $M5$ in the fast-settle bias circuit never enters the triode region, which speeds its switching. When the bypass goes low, $M5$ charges up the gate of $M1$, node A, by injecting extra current. When the voltage at node A reaches the desired value, $M5$ turns off.

Figure 4.13(c) shows the simulation result of these two bias circuits. The fast settle bias circuit of Fig. 4.13(b) enables this frequency synthesizer to achieve a switching time of less than 2 nS in all the band switching scenarios.

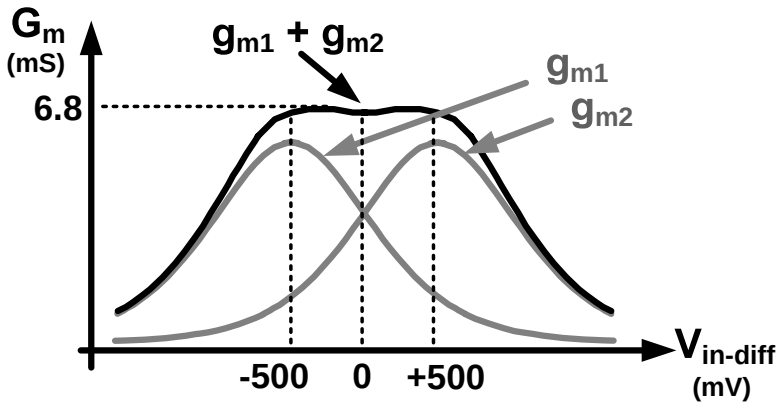
4.3.5 LO Amplifier

As was discussed in Section 4.3.4, this synthesizer uses up to two levels of SSB mixing. The output of the first SSB mixer goes to the LO port of the second mixer. This is shown in Fig. 4.14. This method of interfacing has two main advantages: (1) it allows linearization of the Gm stage of $SSB\ mixer2$, which is vital to meet the out-of-band emission requirements. (2) Since all the odd harmonics of the LO signal contribute to the mixing products, the higher frequency signal is applied to the LO port of $SSB\ mixer2$. In the proposed frequency plan, this signal can be at 6.6 GHz, 7.128 GHz, or 7.656 GHz, depending on the synthesized band. As a result, higher-order mixing products, due to higher-order harmonics of LO signal, lie outside the UWB span, and at the same time, experience low gain at those frequencies.

This scheme also eases the design and linearization of multiplexers used for band switching. One interfacing problem is the large gain-bandwidth product requirement of the LO amplifier shown in Fig 4.14. The large gain is required so it does not degrade the conversion gain, as well as the noise performance. A tuned amplifier is usually the way to achieve high gain for these applications. Another solution is Cherry-Hooper amplifier [51, 52]. But it is not a very efficient architecture for low voltage CMOS design. Architectures based on active inductors [53] also are not well suited for low



(a)



(b)

Figure 4.12: Mixer linearization using multi-tanh Gm stage (a) multi-tanh Gm stage with improved headroom (b) linearized Gm.

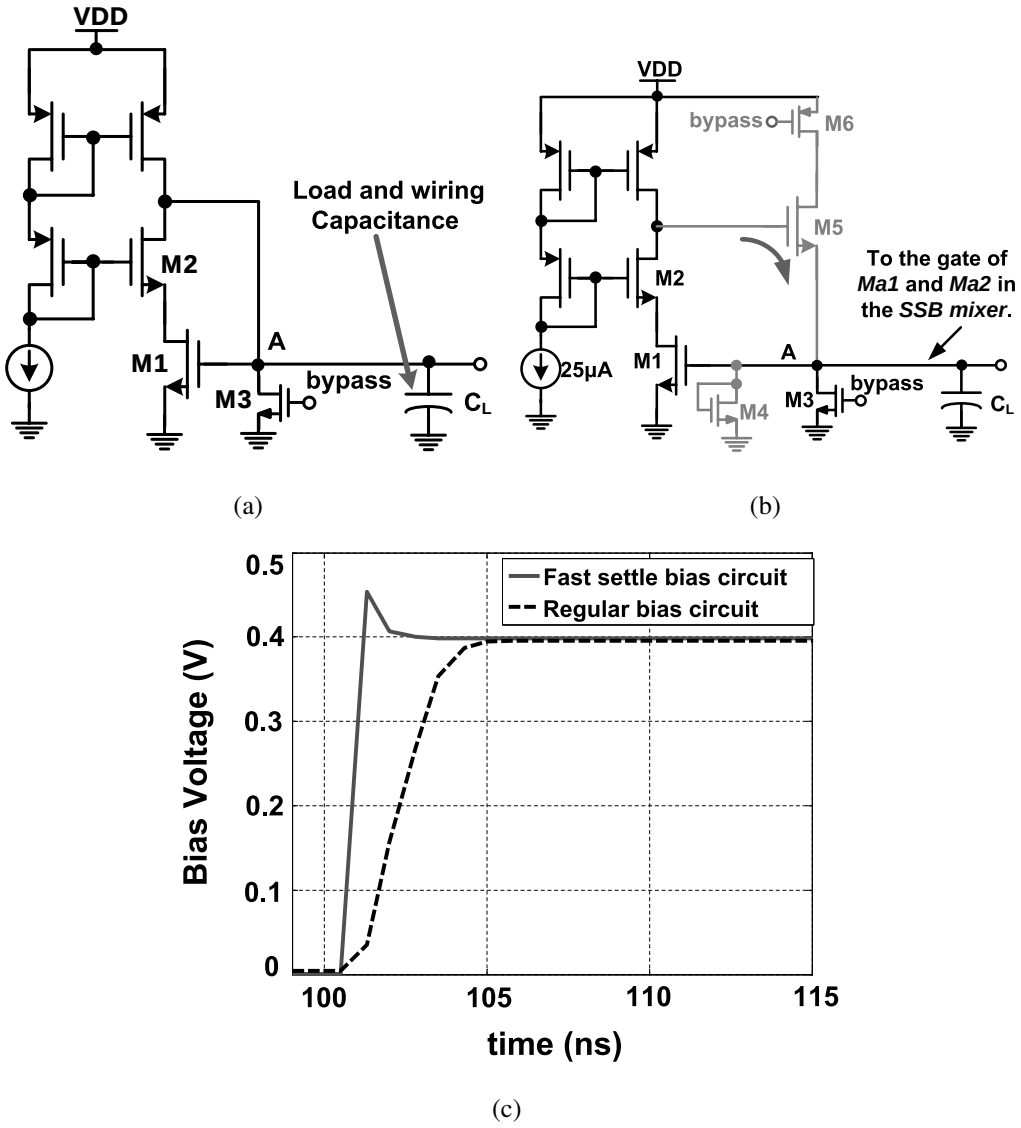


Figure 4.13: (a) Regular bias circuit (b) fast-settle bias circuit (c) Comparison of start-up time of regular bias circuit and fast bias circuit.

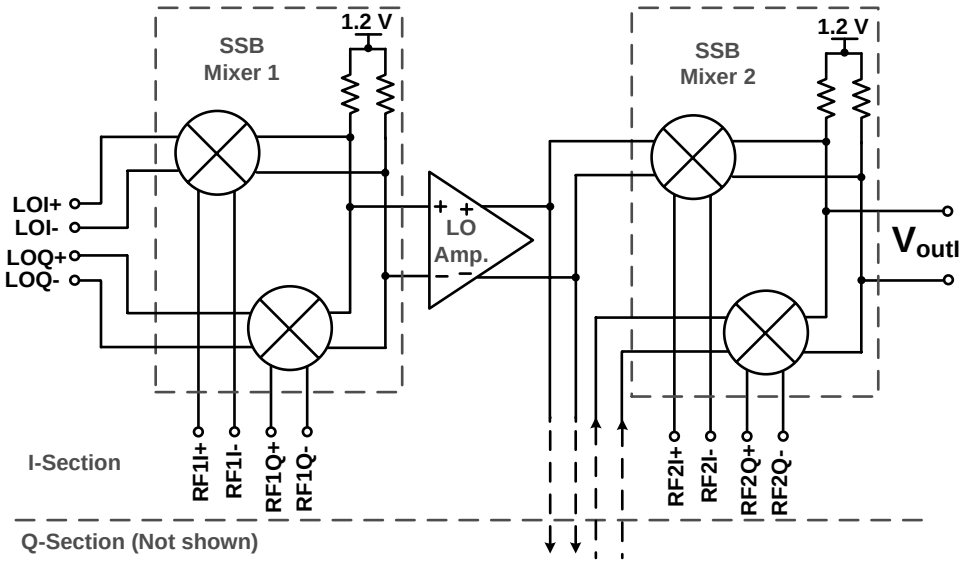


Figure 4.14: Mixing stages and LO amplifier interface.

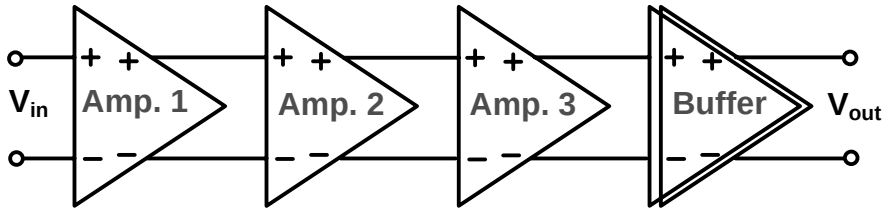
supply voltages.

In this work, a three-stage amplifier followed by a driver stage is used. The LO amplifier is shown in Fig. 4.15(a). In Fig. 4.15(a), each amplifier is implemented using a differential pair with resistive load and a negative impedance generator [54] for bandwidth enhancement. This cell is shown in Fig. 4.15(b). The admittance of the cross-coupled transistors and capacitor C_N is

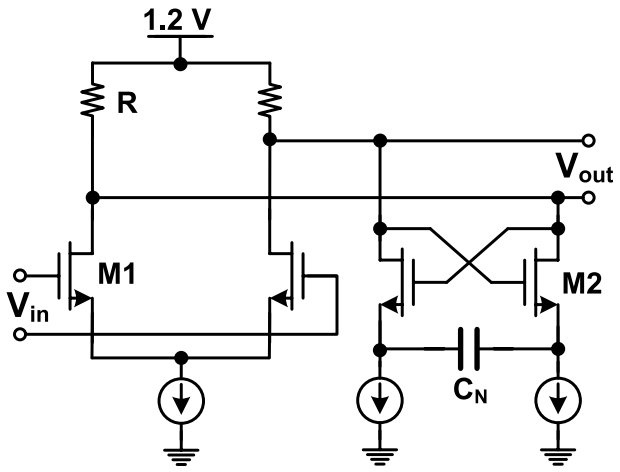
$$Y_N(s) = 2sC_{gd2} - sC_N \frac{g_{m2} - sC_{gs2}}{g_{m2} + s(C_{gs2} + 2C_N)} \tag{4.10}$$

This cell was described as a negative capacitance generator [54], and it is shown in Appendix C that it can provide a negative capacitance in parallel with a negative conductance, depending on the frequency and the value of C_N. This can lead to an enhancement of the gain-bandwidth product of the amplifier of Fig. 4.15(b). Since the negative impedance generator of Fig. 4.15(b) is used in the LO path, its large signal behavior is also discussed in Appendix C.

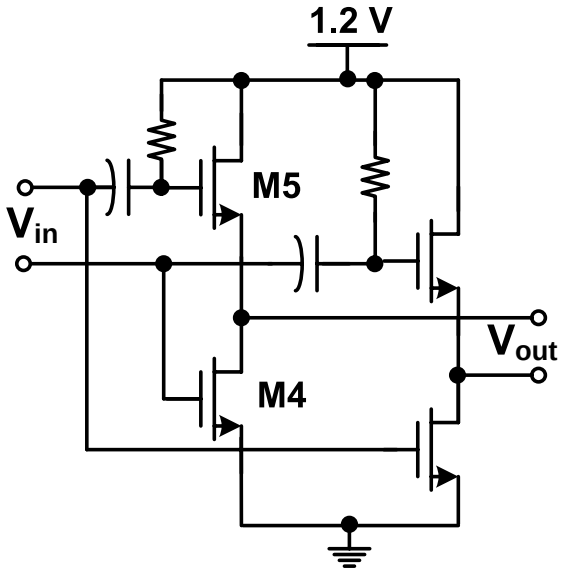
The cascade combination of the amplifier shown in Fig. 4.15(b) provides enough amplification for the output of $SSB\ Mixer1$ to be used as the LO for $SSB\ Mixer2$. In



(a)



(b)



(c)

Figure 4.15: (a) LO amplifier (b) differential pair with negative impedance generator (c) output buffer.

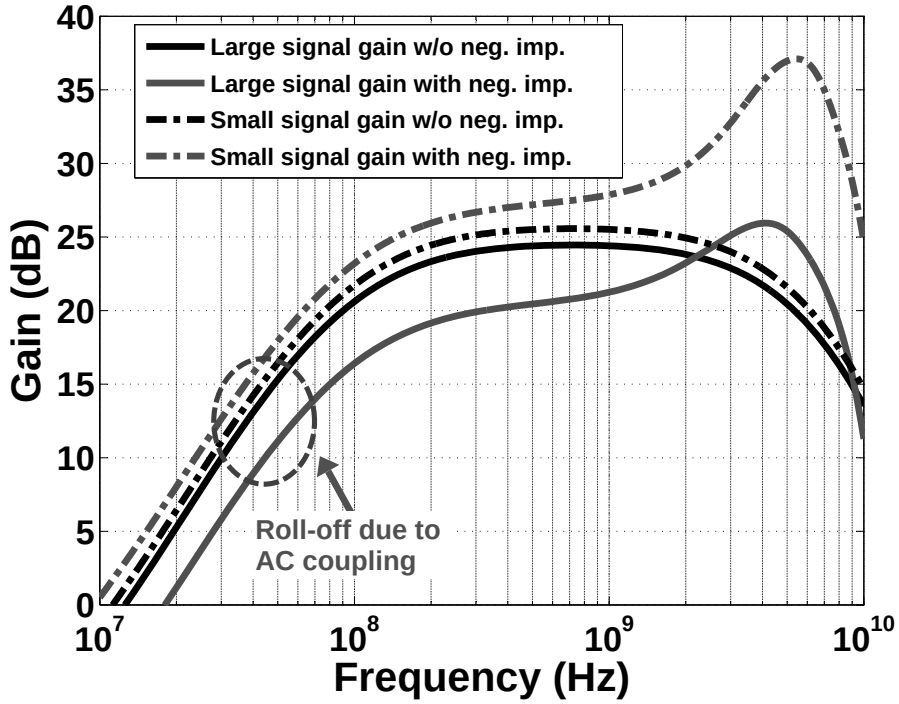


Figure 4.16: Simulated large-signal and small-signal gain of the LO amplifier of the Fig. 4.15.

order to drive the capacitive load of $SSB\ Mixer2$, a differential driver stage consisting of common source and source-follower amplifiers [55, 25], shown in Fig. 4.15(c), is used.

Both large-signal and small-signal gains of the LO amplifier of Fig. 4.15 are shown in Fig. 4.16. As can be seen from Fig. 4.16, the differential pair with a negative impedance generator leads to gain peaking at the frequency band of interest. In the implementation of the LO amplifier of Fig. 4.15, all the stages are AC coupled. Therefore a fast roll-off at low frequencies can be seen in the gain plots of Fig. 4.16.

As was discussed in Section 4.3.4, it may be necessary to compensate for the residual I/Q amplitude and phase mismatch. One can compensate for the I/Q amplitude and phase mismatches by mismatching the gain of the LO amplifiers from their nominal value by varying the dc current.

4.3.6 Multiplexers

A fully quadrature implementation of the frequency synthesizer requires two of the SSB mixers shown in Fig. 4.11 in each mixing stage. If we refer to these mixers as $SSB\ Mixer_I$ and $SSB\ Mixer_Q$, and also assume that the signals applied to the LO port and Gm stage of the SSB mixers are respectively at the frequency of ω_{LO} and ω_{RF}, then the following sequence shown in Table 4.1 needs to be applied to the mixer in order to achieve the $\cos((\omega_{LO} \pm \omega_{RF})t)$ at the output of $SSB\ Mixer_I$ and $\sin((\omega_{LO} \pm \omega_{RF})t)$ at the output of $SSB\ Mixer_Q$. In Table 4.1, LOI and LOQ are the differential signals applied to the LO port of the SSB mixer shown in Fig. 4.11, while RFI and RFQ are the differential signals applied to its Gm stage.

Table 4.1: Operation of multiplexers.

	SSB Mixer$_I$	**SSB Mixer**$_Q$
LOI	$\cos(\omega_{LO}t)$	$\sin(\omega_{LO}t)$
LOQ	$\sin(\omega_{LO}t)$	$\cos(\omega_{LO}t)$
RFI	$\cos(\omega_{RF}t)$	$\cos(\omega_{RF}t)$
RFQ	$\mp\sin(\omega_{RF}t)$	$\pm\cos(\omega_{RF}t)$

As can be seen in Table 4.1, in order to perform the band switching, only the signal to the Gm stage of the mixer undergoes a change in its polarity, and the LO signal is always fixed. This method is used in both multiplexers for both stages of mixing. This method eases the implementation of the multiplexers, since the signal applied to the Gm stage of each mixer is always at a lower frequency than the LO signal. On the other hand, in the second stage of mixing, $Analog\ Mux2$ must be able to apply different frequencies to the Gm stage. Therefore, this method combines the phase and frequency selection in one block. $Analog\ Mux1$ accomplishes this function for the first level of mixing. A quadrature differential 528 MHz is applied to the $Analog\ Mux1$, and it applies the appropriate phases of 528 MHz to the Gm stage of the SSB mixers in the first level of mixing. Due to its high linearity requirement, $Analog\ Mux1$ is linearized using a source-degenerated structure [49]. The simplified schematic of $Analog\ Mux1$

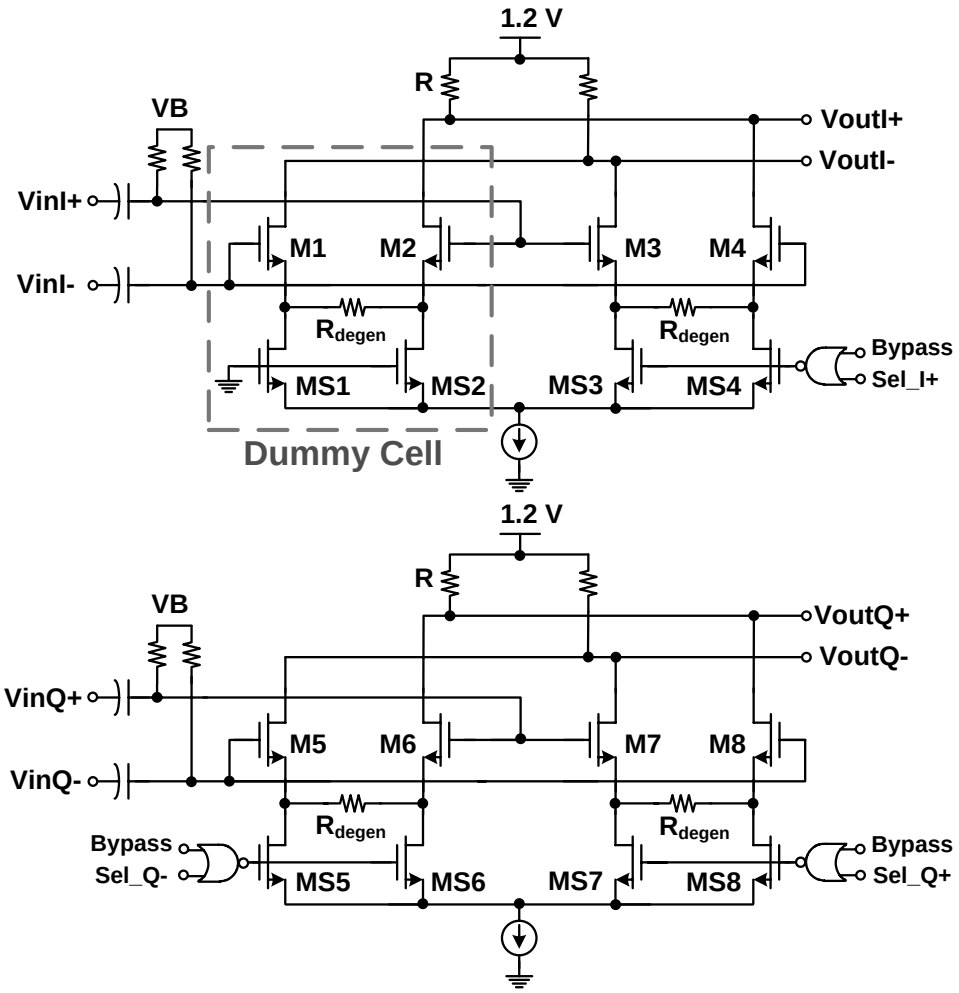


Figure 4.17: Schematic of multiplexer 1 used in the first level of SSB mixing to choose the appropriate phase of the 528 MHz signal.

is shown in Fig. 4.17.

$Analog\ Mux2$ has to provide the appropriate phase sequences of the signal, but it also has to provide the right frequency for the operation of $SSB\ Mixer2$. In order to achieve a compact implementation, and also to achieve large gain, inverter-based Gm stages [56] are used.

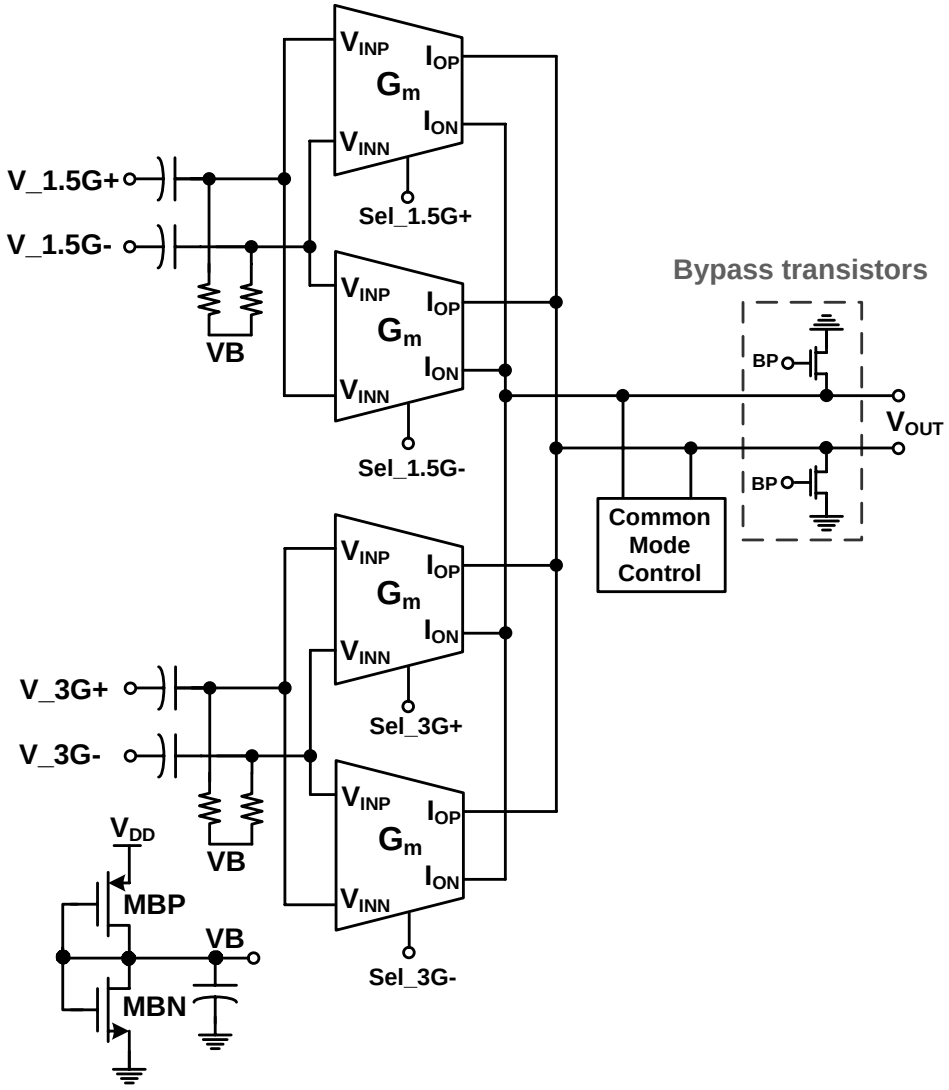


Figure 4.18: Top level block diagram of the inverter-based Analog Mux2.

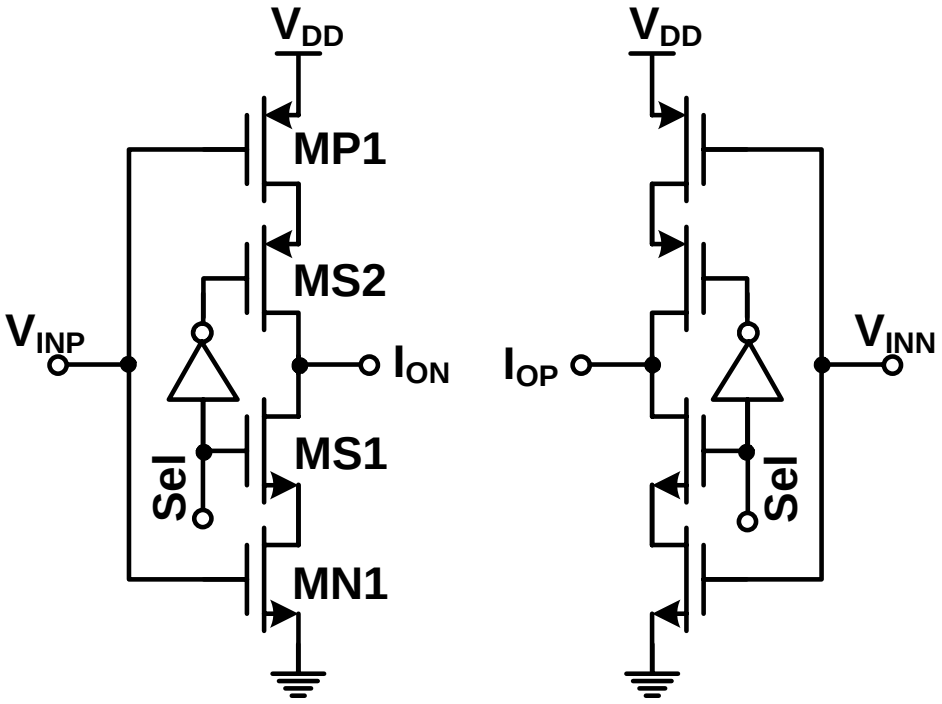
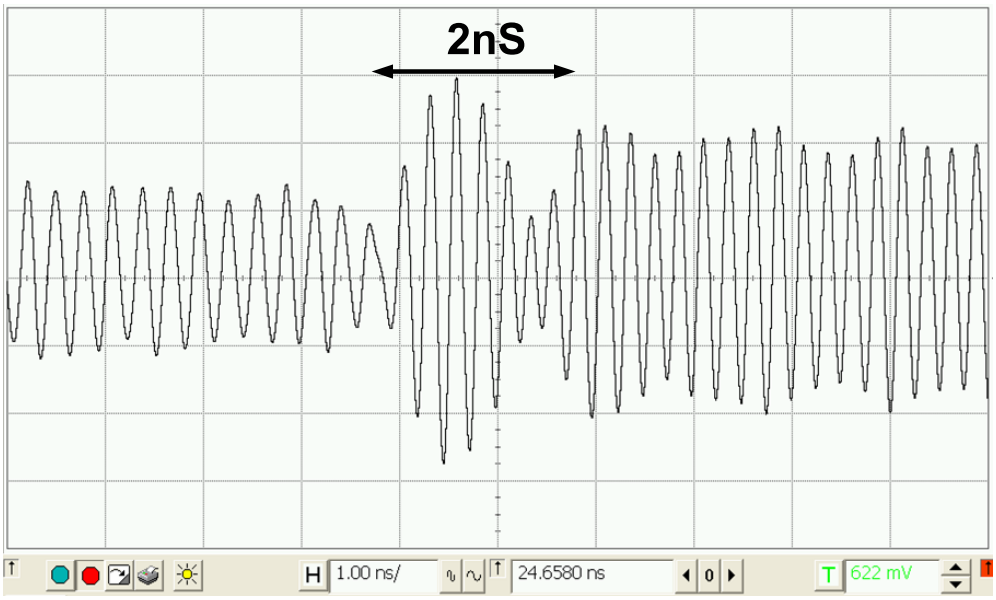


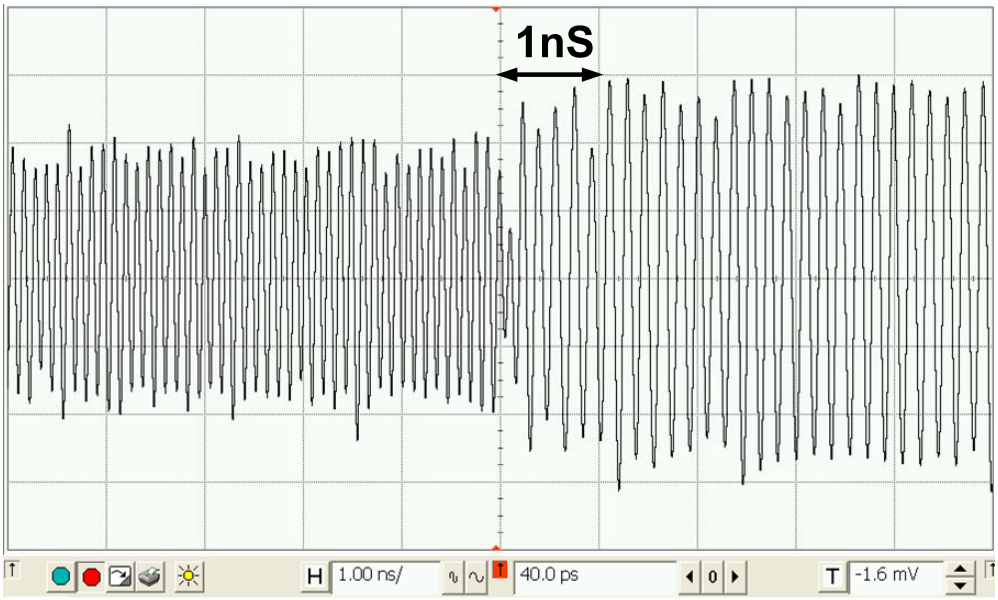
Figure 4.19: Pseudo-differential inverter-based Gm stage used in Analog Mux2.

4.4 Measured Results

Figure 4.20 shows the measured band switching of the frequency synthesizer. In contrast to many of the reported UWB frequency synthesizers, this design is capable of hopping from any arbitrary band to any other. It also supports operation in each of the individual band groups (1-6) specified in [7]. Two different band switching scenarios are shown in Fig. 4.20: switching within bands of a group, and switching between bands of different groups. The synthesizer settles in approximately 2 nS when hopping from Band 1 to Band 2, and settles in approximately 1 nS when hopping from Band 11 to Band 5. Further measurement results show that this design achieved settling times of less than 2 nS when hopping between any of the other UWB bands.



(a)



(b)

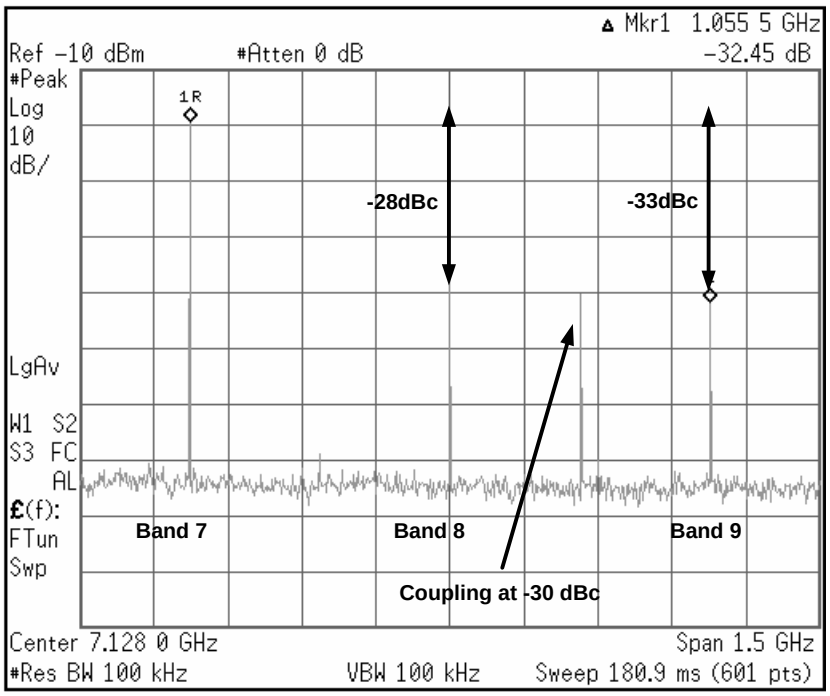
Figure 4.20: Measured band switching time. (a) band switching within a group (band #1 to band #2) (b) band switching between groups (band #11 to band #5).

Figure 4.21(a) and Fig. 4.21(b) show the measured output spectrum of frequency band #7 within band group three and in the entire UWB span, respectively. Note that the increase in the noise floor in the 3.1 to 6.0 GHz band is due to the measurement setup. The measurement results of other bands have similar spectra.

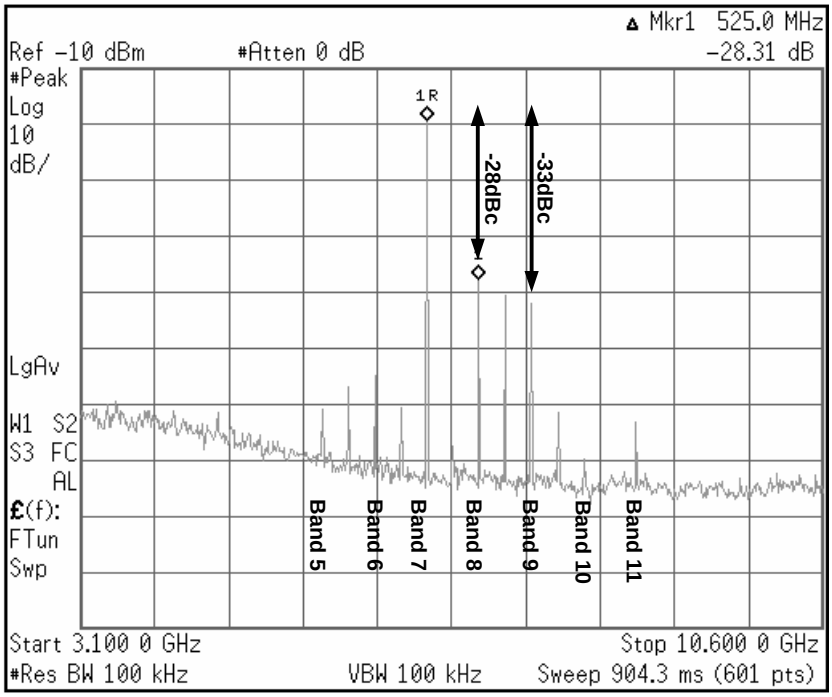
The in-band spurious tones for all fourteen bands are shown in Table 4.2. As can be seen from this table, the mixing sidebands are better than -30 dBc. In addition, as mentioned earlier, here is a fixed LO to output leakage at 7.128 GHz which is smaller than -20 dBc, depending on the band group. This spurious tone occurs through inductive coupling in the power supply lines, layout asymmetry in SSB Mixer1, and systematic offset in the mixers.

To clarify the coupling in the power supply and bias lines, the photograph of the packaged chip, using a 7 mm $\times$ 7 mm 48-lead MLF-QFN package, is shown in Fig. 4.22. As can be seen from this Fig. 4.22, the package body size is significantly larger than the chip dimensions. As a result, the bonding wires are very long and major cross talk occurs among the supply lines that leads to an unwanted spurious tone at 7.128 GHz. This can be further reduced through improved high-frequency packaging or using chip on board assembly to shrink the length of the bonding wires.

Another spurious tone that can be seen in Table 4.2 is the LO to output leakage in the second SSB mixer which is roughly -28 dBc or better, depending on the band and band group of operation. This spurious tone also occurs due inductive coupling in the power supply lines, layout asymmetry in SSB Mixer2, and systematic offset in the mixers, and it could be reduced by improving the layout and using a high-frequency packaging technique.



(a)



(b)

Figure 4.21: Measured output spectrum of band #7(a) spurious tones in group 3, and (b) spurious tones in the whole UWB span.

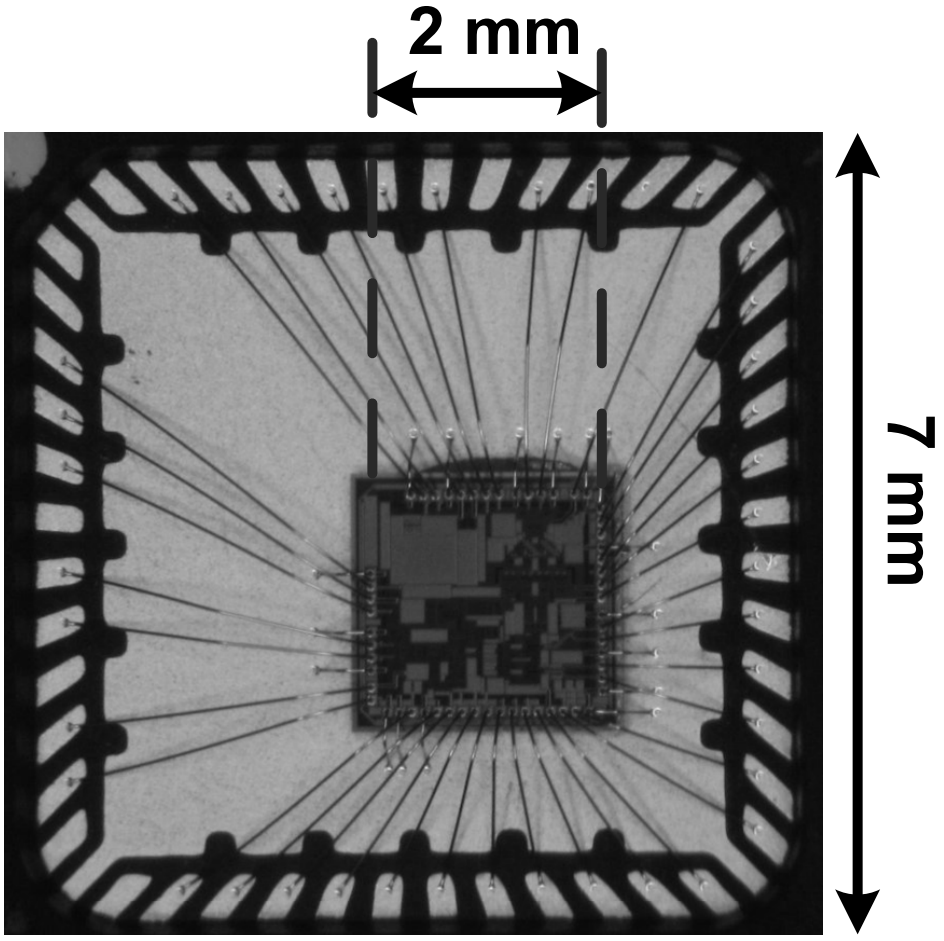


Figure 4.22: The packaged chip using a 7 mm $\times$ 7 mm 48-lead MLF-QFN package.

Table 4.2: Spurious tones.

Target band group/ band		Spurious tones		
		Band 1	Band 2	Band 3
Band group 1	Band 1	-	-34 dBc	-34 dBc
	Band 2	<-60 dBc	-	<-60 dBc
	Band 3	-34 dBc	-28 dBc	-
		Band 4	Band 5	Band 6
Band group 2	Band 4	-	-32 dBc	-39 dBc
	Band 5	<-55 dBc	-	<-55 dBc
	Band 6	-37 dBc	-28 dBc	-
		Band 7	Band 8	Band 9
Band group 3	Band 7	-	-28 dBc	-33 dBc
	Band 8	No spurious tone	-	No spurious tone
	Band 9	-37 dBc	-23 dBc	-
		Band 10	Band 11	Band 12
Band group 4	Band 10	-	-29 dBc	-31 dBc
	Band 11	<-55 dBc	-	<-55 dBc
	Band 12	-30 dBc	-30 dBc	-
		Band 13	Band 14	-
Band group 5	Band 13	-	-37 dBc	-
	Band 14	<-55 dBc	-	-

Figure 4.23 shows the measured phase noise for different bands. The phase noise is always better than -114 dBc/Hz. The phase noise of Band 8 is the best of all, since generating this band requires no mixing. The phase noise worsens as the number of mixing and division stages in the signal path increases. As a result, the phase noise of the center band in each group (bands 2, 5, 8, 11, and 14) is better than the phase noise of the other bands in that group.

Table 4.3 summarizes the measured results of the UWB synthesizer, and compares it with other published 14-band synthesizers. Compared to similar designs, the proposed synthesizer is implemented using minimal hardware, no on-chip inductors, and uses the lowest supply voltage. The inductor-less design methodology will lead to further area reduction when the design is migrated to other technology nodes.

Figure 4.24 shows the chip microphotograph. The core area is 1.3 mm^2. The chip is packaged using a 48 pin MLF-QFN package.

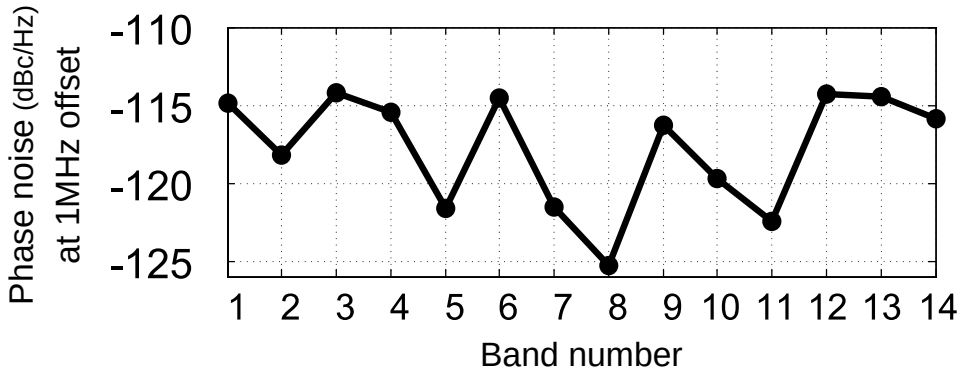


Figure 4.23: Phase noise for different bands at 1 MHz offset.

Table 4.3: Table of comparison with other 14-band frequency synthesizers.

Reference	Liang ISSCC 2006	Werther ISSCC 2008	Lu ISSCC 2008	**This Work**
Technology	0.18μm CMOS	0.13μm SiGe	0.18μm CMOS	**0.13μm CMOS**
Required PLL's	2	1	1	**1**
on-chip inductors [a]	8	Not reported	8	**0**
SSB Mixing levels	3	2	3	**2**
Switching time	$<$ 3 nS	$<$ 3 nS	$<$ 3 nS	$<$ **2 nS**
Supply voltage	1.8 V	2.4/1.2 V	1.8 V	**1.2 V**
Power Consumption	160 mW	Not reported	117 mW	**135 mW**
Die area	1.5 mm^2 [b]	Not reported	5.5 mm^2	**1.3 mm**^{2} [c]

[a] Minimum required number of on-chip inductors in the synthesizer part. The inductors in the VCO, and VCO buffer(s) are not taken into account.

[b] Core area reported.

[c] Core area reported.

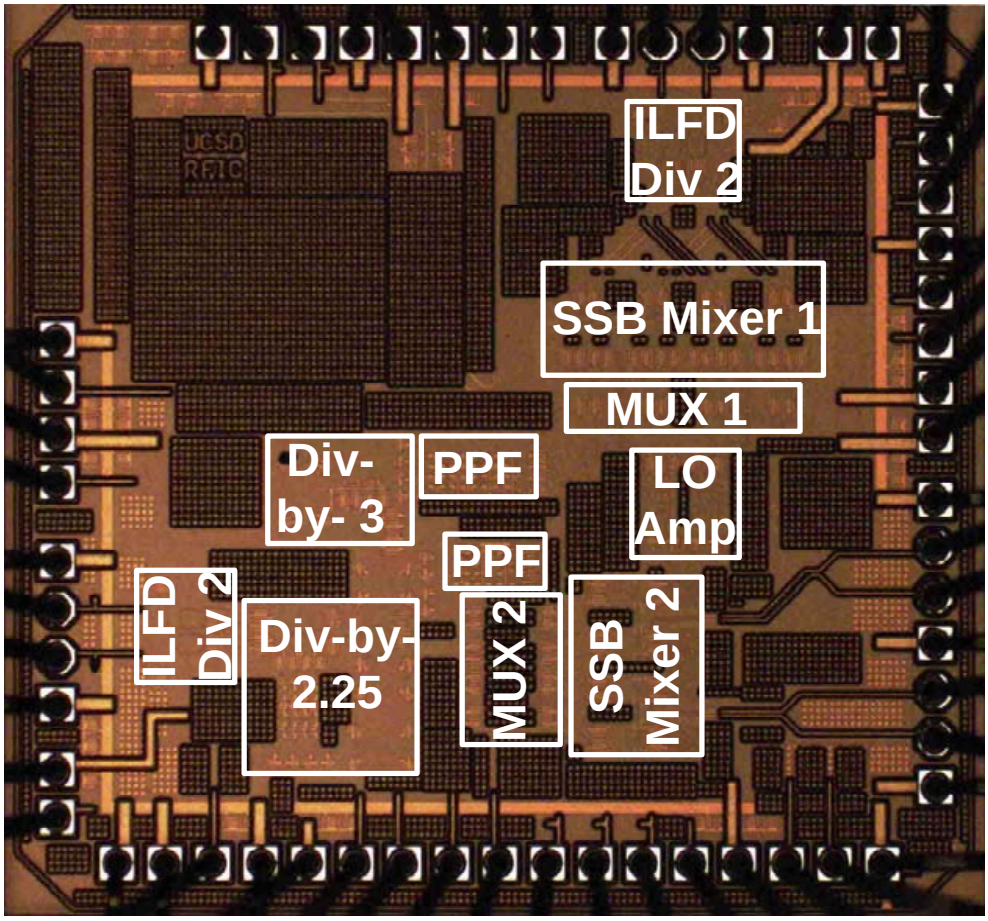


Figure 4.24: Chip microphotograph.

4.5 Conclusion

This work presented the first CMOS inductor-less single PLL 14-band frequency synthesizer for MB-OFDM UWB which is capable to perform any arbitrary band switching, or operate in any individual band groups specified in [7]. This synthesizer exploits up to two levels of SSB mixing and uses an external 14.256 GHz signal to generate all the required frequencies. It is implemented in a 0.13μm CMOS process, uses a single 1.2 V supply voltage, and dissipates 135 mW. The mixing sideband level is better than -31 dBc. The synthesizer can perform frequency switching among all different bands and groups, and the switching time is roughly 2 nS for all different hopping scenarios. The phase noise is better than -110 dBc/Hz at 1 MHz offset.

This chapter has been submitted in part to the following publication:

- M. Farazian, P. S. Gudem, and L. E. Larson, "An Inductor-less CMOS 14-Band Frequency Synthesizer for Universal Multi-band OFDM UWB", *IEEE Transactions of Microwave Theory and Techniques*, (in review).

Chapter 5

Conclusion

The wide bandwidth and stringent agility requirements of MB-OFDM UWB poses several design challenges on implementation of a monolithic UWB transceiver. On the other hand, since the spectrum of 3.1 GHz to 10.6 GHz is not universally available, any UWB solution needs to be able to operate in different band groups to be marketable globally. One major challenge in the implementation of any UWB transceiver that covers several band groups is to generate all the band center frequencies and meeting the agility requirements of WiMedia UWB as well as the spurious tone limitations imposed by FCC. On the other hand, UWB is targeting applications such as wireless USB that imply a very low cost UWB solution. This can only be achieved when a hardware efficient architecture for a UWB radio is implemented in a standard CMOS technology and only using the standard features of a digital CMOS process. As a result, the focus of this dissertation is on

- Presenting an architecture for monolithic frequency synthesizer for MB-OFDM UWB that can operate in all six band groups of WiMedia UWB.
- Implementing the proposed architecture in a digital submicron CMOS technology without using any on-chip inductor or balun.

To overcome the settling time limitations of conventional frequency synthesizers and covering the entire band groups of UWB (a bandwidth of 7.5 GHz with 528 MHz channel spacing), an architecture based on the method of frequency division and mixing

is used. The main challenge in using this architecture is to reduce the number of required PLL's and SSB mixers.

Since operation of SSB mixers requires quadrature signals, the techniques for quadrature generation at microwave frequencies are investigated, and four-stage ring-oscillator-based injection-locked frequency dividers are studied as a technique to implement a frequency divider and achieve quadrature phases of output. Toward this goal, a multi-phase multi-modulus ring-oscillator-based ILFD is designed in a 0.13μm CMOS technology that works as a divide-by-6 at V-band, and can also achieves division ratios of four and two.

In this work, a frequency plan is proposed that can generate all the required frequencies from a single fixed frequency and can implement any center frequency with a maximum of two levels of SSB mixing. In order to generate all the required frequencies for the operation of this frequency synthesizer out of a single frequency, fractional frequency dividers are needed. Therefore, another study is performed on the architectures that can obtain a fractional division ratio. This study involves an analysis of operation and stability of injection-locked regenerative frequency dividers. This is followed by a phase noise analysis of this class of frequency dividers.

In addition, the operation, stability, locking range, and phase noise of two-stage ring-oscillators, which are compact ways to generate quadrature output phases and can be used in injection-locked regenerative frequency dividers, are analyzed.

In order to meet the linearity requirement in an inductor-less design, low-voltage linearization techniques along with polyphase filtering are employed. To use polyphase filters for spurious tones mitigation, the behavior of polyphase filters in the presence of process variations is carefully examined.

Finally, this dissertation presented the first CMOS inductor-less single PLL 14-band frequency synthesizer for MB-OFDM UWB which is capable to perform any arbitrary band switching, or operate in any individual band groups specified in [7]. This synthesizer exploits up to two levels of SSB mixing and uses an external 14.256 GHz signal to generate all the required frequencies. It is implemented in a 0.13μm CMOS process, uses a single 1.2 V supply voltage, and dissipates 150mW. The mixing sideband level is better than -31 dBc. The synthesizer can perform frequency switching among

all different bands and groups, and the switching time is roughly 2 nS for all different hopping scenarios. The phase noise is better than -110 dBc/Hz at 1 MHz offset.

This work presented the possibility of fast hopping high-speed signal generation in a digital CMOS technology. This methodology fully benefits from the technology scaling, and our proposed inductor-less design methodology leads to a smaller die area and lower power consumption when this design is ported to a finer technology node.

Appendix A

Stability Analysis of The Oscillation Phases of the Two-Stage Ring-Oscillator

Equation (3.24) states that when the two-stage ring-oscillator of Fig. 3.3 is free-running ($I_{inj} = 0$), the outputs have a phase difference of $\Delta\theta = \pm\pi/2$. In this section we use perturbation analysis, a similar approach to [26], to investigate the stability of these solutions for $\Delta\theta$. We first start with $\Delta\theta = +\pi/2$. For this case $\theta_{1,1}$ and $\theta_{2,1}$ can be expressed as

$$\theta_{1,1}(t) = \omega_{_{SRF}} t + \delta\theta_1 \tag{A.1a}$$

$$\theta_{2,1}(t) = \omega_{_{SRF}} t - \frac{\pi}{2} + \delta\theta_2 \tag{A.1b}$$

where $\delta\theta_1$ and $\delta\theta_2$ are perturbations added to $\theta_{1,1}$ and $\theta_{2,1}$ respectively. Substituting (A.1a) and (A.1b) into (3.21a) and (3.21a) results in

$$\omega_{_{SRF}} + \frac{d}{dt}\delta\theta_1(t) = \frac{1}{RC}\frac{I_1\cos\left(\delta\theta_1(t) - \delta\theta_2(t)\right)}{I_2 + I_1\sin\left(\delta\theta_1(t) - \delta\theta_2(t)\right)} \tag{A.2a}$$

$$\omega_{_{SRF}} + \frac{d}{dt}\delta\theta_2(t) = \frac{1}{RC}\frac{I_1\cos\left(\delta\theta_1(t) - \delta\theta_2(t)\right)}{I_2 - I_1\sin\left(\delta\theta_1(t) - \delta\theta_2(t)\right)} \tag{A.2b}$$

If we define $\Delta(\delta\theta)$ as $\delta\theta_1 - \delta\theta_2$, and also considering that $\delta\theta_1$ and $\delta\theta_2$ are very small compared to $\theta_{1,1}$ and $\theta_{2,1}$, we can derive a differential equation for $\Delta(\delta\theta)$ using (A.2a) and (A.2b), as shown below.

$$\frac{d}{dt}\Delta(\delta\theta(t)) \approx -\frac{1}{\tau}\Delta(\delta\theta(t)) \tag{A.3}$$

where

$$\tau = \frac{1}{2\omega_{_{SRF}}}\frac{I_2}{I_1}. \tag{A.4}$$

The solution to (A.3) is

$$\Delta\left(\delta\theta(t)\right) = \Delta\left(\delta\theta(0)\right)\exp(-t/\tau). \tag{A.5}$$

As can be seen from (A.5), any perturbation on the phase difference will eventually diminish. A similar analysis can be done for $\delta\theta_1(t)$ and $\delta\theta_2(t)$. From (A.2a), (A.2b), and (A.5) the solution for $\delta\theta_1(t)$ and $\delta\theta_2(t)$ can be expressed as follows

$$\delta\theta_1(t) = \frac{I_2}{I_1}\frac{1}{2\tau}\left[\tau\ln\left(e^{t/\tau} + \frac{I_1}{I_2}\Delta(\delta\theta(0))\right) - t\right] \tag{A.6a}$$

$$\delta\theta_2(t) = \frac{I_2}{I_1}\frac{1}{2\tau}\left[\tau\ln\left(e^{t/\tau} - \frac{I_1}{I_2}\Delta(\delta\theta(0))\right) - t\right] \tag{A.6b}$$

Using (A.6a) and (A.6b) it can be shown that $\lim_{t\to\infty}\delta\theta_1(t) = 0$ and $\lim_{t\to\infty}\delta\theta_2(t) = 0$.

A similar analysis for $\Delta\theta = -\pi/2$ results in

$$\Delta\left(\delta\theta(t)\right) = \Delta\left(\delta\theta(0)\right)\exp(+t/\tau) \tag{A.7}$$

which shows that, in this case, any perturbation sustains and grows with time. A similar analysis can be performed to check the stability of the solutions for oscillation phases in the presence of an external signal (I_{inj}).

Appendix B

Step Response of Injection-Locked Two-Stage Ring-Oscillator

Assuming that the ring-oscillator of Fig. 3.9 is injection locked to a signal at frequency ω_{inj} and steady-state is reached. We also assume that the conditions stated in Section 3.5.3 for quadrature equal amplitude output voltages ($V_{a1} = V_{a2}$ and $\Delta\theta = \pi/2$) are satisfied, i.e. $I_{inj1} = I_{inj2} = I_{inj}$, $\psi_1 = \psi_2 = \psi$. Hence, (3.21a) results in

$$\omega_{inj} = \frac{1}{RC}\frac{I_1 + \frac{\pi}{4}I_{inj}\sin\psi}{I_2 + \frac{\pi}{4}I_{inj}\cos\psi}. \tag{B.1}$$

If a phase step with magnitude of $\Delta\theta_{inj}$ is applied to both inputs to the oscillator at time $t = 0^+$, i.e. both θ_{inj1} and θ_{inj2} jump for $\Delta\theta_{inj}$ from their initial values, $\theta_{1,1}(t)$ and $\theta_{2,1}(t)$ for $t > 0^+$ would change accordingly as

$$\theta_{1,1}(t) = \omega_{inj}t + \Delta\theta_{1,1}(t) \tag{B.2a}$$

$$\theta_{2,1}(t) = \omega_{inj}t - \pi/2 + \Delta\theta_{2,1}(t). \tag{B.2b}$$

Consequently, $\psi_1(t)$ and $\psi_2(t)$ for $t > 0^+$ are

$$\psi_1(t) = \psi + \Delta\theta_{inj} - \Delta\theta_{1,1}(t) \tag{B.3a}$$

$$\psi_2(t) = \psi + \Delta\theta_{inj} - \Delta\theta_{2,1}(t). \tag{B.3b}$$

In addition, $\Delta\theta(t)$ undergoes the following change.

$$\Delta\theta(t) = \pi/2 + \Delta\theta_{1,1}(t) - \Delta\theta_{2,1}(t) \tag{B.4}$$

Assuming $\Delta\theta_{1,1}(t) - \Delta\theta_{2,1}(t)$ is negligible compared to $\pi/2$, and substituting (B.2a) and (B.3a) into (3.21a) results in

$$\omega_{inj} + \frac{d}{dt}\Delta\theta_{1,1}(t) = \frac{1}{RC}\frac{I_1 + \frac{\pi}{4}I_{inj}\sin\psi_1(t)}{I_2 + \frac{\pi}{4}I_{inj}\cos\psi_1(t)}. \tag{B.5}$$

By substituting (B.3a) into (B.5) and assuming that $\Delta\theta_{inj} - \Delta\theta_{1,1}(t)$ is small compared to psi we obtain

$$\begin{aligned}\omega_{inj} + \frac{d}{dt}\Delta\theta_{1,1}(t) = &\frac{1}{RC}\frac{I_1 + \frac{\pi}{4}I_{inj}\sin\psi}{I_2 + \frac{\pi}{4}I_{inj}\left[\cos\psi - (\Delta\theta_{inj} - \Delta\theta_{1,1}(t))\sin\psi\right]} \\ &+ \frac{1}{RC}\frac{\frac{\pi}{4}I_{inj}\left(\Delta\theta_{inj} - \Delta\theta_{1,1}(t)\right)\cos\psi}{I_2 + \frac{\pi}{4}I_{inj}\left[\cos\psi - (\Delta\theta_{inj} - \Delta\theta_{1,1}(t))\sin\psi\right]}.\end{aligned} \tag{B.6}$$

Since $\frac{\pi}{4}I_{inj}\left(\Delta\theta_{inj} - \Delta\theta_{1,1}(t)\right)$ is smaller than I_2, we can simplify the denominator in (B.5). Using (B.1), equation (B.6) results in

$$\frac{d}{dt}\Delta\theta_{1,1}(t) = -\frac{1}{\tau}\left(\Delta\theta_{1,1}(t) - \Delta\theta_{inj}\right) \tag{B.7}$$

where

$$\tau = \frac{I_2 + \frac{\pi}{4}I_{inj}\cos\psi}{\frac{\pi}{4}I_{inj}\cos\psi}RC. \tag{B.8}$$

Using (B.1), equation (B.8) can be re-written as

$$\tau = \frac{I_1 + \frac{\pi}{4}I_{inj}\sin\psi}{\frac{\pi}{4}I_{inj}\omega_{inj}\cos\psi}. \tag{B.9}$$

Equation (B.7) shows that an injection-locked two-stage ring-oscillator tracks the step on the phase of the injection with a time constant τ. Consequently, $\Delta\theta_{1,1}(t)$ approaches $\Delta\theta_{inj}$. A similar conclusion is obtained for $\Delta\theta_{2,1}(t)$ following same steps, i.e.

$$\frac{d}{dt}\Delta\theta_{2,1}(t) = -\frac{1}{\tau}\left(\Delta\theta_{2,1}(t) - \Delta\theta_{inj}\right). \tag{B.10}$$

As a result, the final values of $\theta_{1,1}(t)$ and $\theta_{2,1}(t)$ can be expressed as

$$\theta_{1,1}(t) \rightarrow \omega_{inj}t + \Delta\theta_{inj} \tag{B.11a}$$

$$\theta_{2,1}(t) \rightarrow \omega_{inj}t + \Delta\theta_{inj} - \frac{\pi}{2}. \tag{B.11b}$$

Equations (B.7) and (B.10) represent first-order systems with a transfer function

$$G(S) = \frac{1}{1 + S/\omega_P} \tag{B.12}$$

where

$$\omega_P = \frac{1}{\tau} = \frac{\frac{\pi}{4} I_{inj} \cos\psi}{I_1 + \frac{\pi}{4} I_{inj} \sin\psi} \omega_{inj}. \tag{B.13}$$

Appendix C

Analysis of The Negative Impedance Generator

The negative impedance generator used in the amplifier of Fig. 4.15(b) is redrawn in Fig. C.1(a). We start with the small-signal analysis of this circuit. The input admittance of the circuit shown in Fig. C.1(a) is given by (4.10). $Y_N(s)$ consists of a parallel capacitor, and a residual part, $Y_0(s)$, which is given by (C.1).

$$Y_0(s) = -sC_N \frac{g_{m2} - sC_{gs2}}{g_{m2} + s(C_{gs2} + 2C_N)} \tag{C.1}$$

Equation (C.1) shows that Y_0 has a net capacitive part, which can be found as

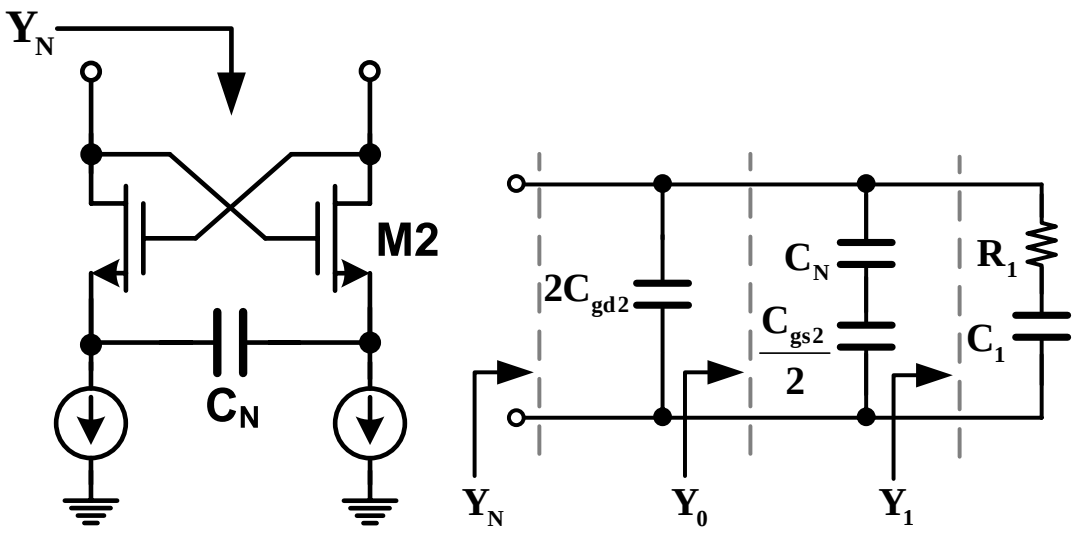
$$\lim_{s\to\infty} \frac{Y_0}{s} = \frac{C_{gs2}C_N}{C_{gs2} + 2C_N} \tag{C.2}$$

The term given by (C.2) is a series combination of two capacitors with the values of $C_{gs2}/2$ and C_N. Therefore Y_0 can be written as

$$Y_0(s) = \frac{C_{gs2}C_N}{C_{gs2} + 2C_N} s + Y_1(s) \tag{C.3}$$

It can be shown that Y_1 is a series combination of a resistor and a capacitor. So, Z_1 can be written as

$$Z_1(s) = \frac{1}{Y_1(s)} = R_1 + \frac{1}{sC_1} \tag{C.4}$$



(a) (b)

Figure C.1: (a) Negative impedance generator, (b) equivalent circuit for negative impedance generator.

where R_1 and C_1 are given by

$$R_1 = -\frac{(2C_N + C_{gs2})^2}{2C_N(2C_N + C_{gs2})g_{m2}} \tag{C.5a}$$

$$C_1 = -\frac{(2C_N + C_{gs2})^2}{2C_N(2C_N + C_{gs2})} \tag{C.5b}$$

Figure C.1(b) shows an equivalent circuit for the negative impedance generator of Fig. C.1(a) in which R_1 and C_1 are independent of frequency. However, a parallel combination of R_1 and C_1, as shown in Fig. C.2, is more desirable for analysis of the net capacitance and conductance of this circuit.

To do so, we define $Y_1(s)$ as

$$Y_1(s) = G_P + sC_P \tag{C.6}$$

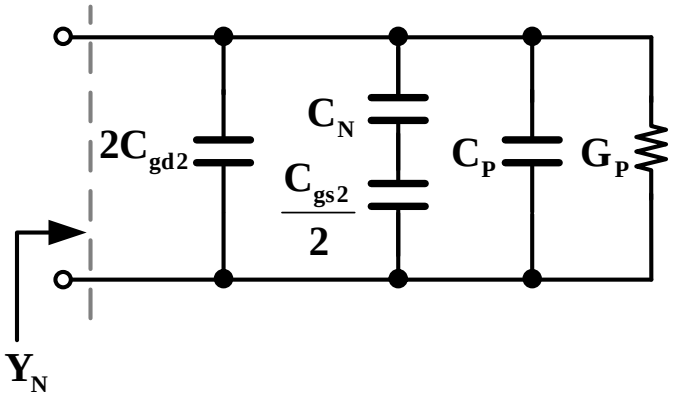


Figure C.2: Equivalent circuit for negative impedance generator.

where G_P and C_P are given by

$$G_P = -\frac{2C_N(C_N + C_{gs2})\omega^2 g_{m2}}{g_{m2}^2 + (2C_N + C_{gs2})^2\omega^2} \tag{C.7a}$$

$$C_P = -\frac{2C_N(C_N + C_{gs2})}{2C_N + C_{gs2}} \cdot \frac{g_{m2}^2}{g_{m2}^2 + (2C_N + C_{gs2})^2\omega^2} \tag{C.7b}$$

Equation (C.7a) and (C.7b) show that the circuit of Fig. C.1(a) can exhibit negative capacitance and negative conductance, which lead to gain and bandwidth expansion at high frequencies.

The negative capacitance obtained from the circuit of Fig. C.1(a) becomes negligible in the large-signal regime. However, the negative conductance has a small variation over a wide range of signal swings. In this case, if we assume that the total output conductance and capacitance of the differential pair of Fig. 4.15(b), without the negative impedance generator, are G_L and C_L respectively, and the total output conductance and capacitance of the negative impedance generator of Fig. C.1(a) are respectively $G_{NIG}(S)$ and $C_{NIG}(S)$, then the transfer function of the amplifier of Fig. 4.15(b) can be written as:

$$A(S) = \frac{G_m}{G_{eq}(S)} \cdot \frac{1}{1 + SC_{eq}(S)/G_{eq}(S)} \tag{C.8}$$

where G_m is the large signal transconductance of transistor $M1$ in Fig. 4.15(b) and

$$G_{eq}(S) = G_L + G_{NIG}(S) \tag{C.9a}$$

$$C_{eq}(S) = C_L + C_{NIG}(S). \tag{C.9b}$$

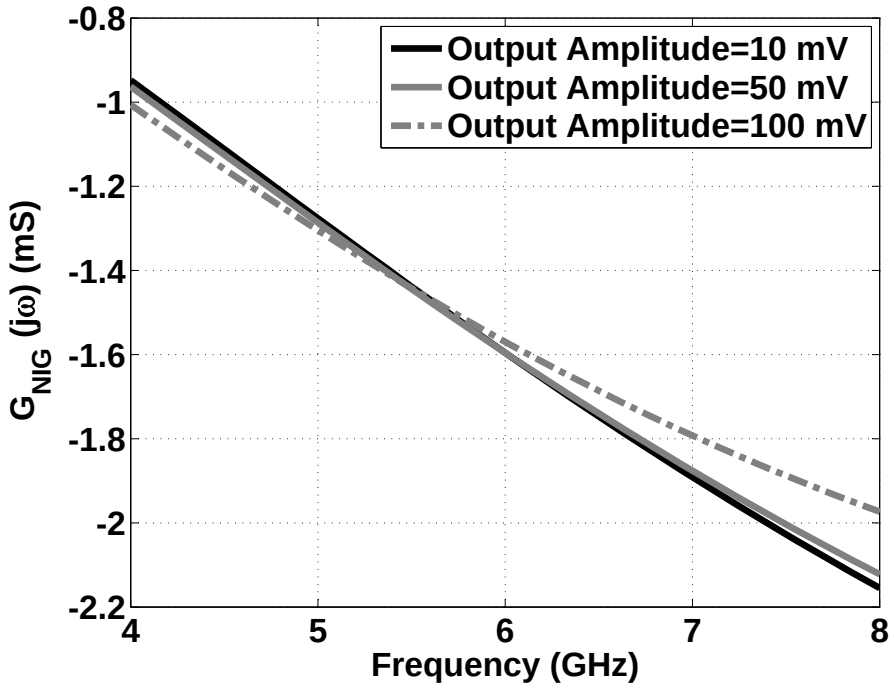


Figure C.3: Simulated G_{NIG} vs. frequency for different values of output amplitude.

Figure C.3 shows the simulated G_{NIG} vs. frequency for various output swings. As can be seen from Fig. C.3, G_{NIG} within the frequencies of interest (6 GHz to 8 GHz) can be approximated by

$$G_{NIG}(j\omega) = -g_0 - g_1\omega \tag{C.10}$$

where g_0 and g_1 are positive numbers. From (C.8) and (C.10) we obtain

$$|A(j\omega)| = \frac{G_m}{\left[\left(C_{eq}^2(j\omega) + g_1^2\right)\omega^2 - 2(G_L - g_0)g_1\omega + (G_L - g_0)^2\right]^{\frac{1}{2}}} \tag{C.11}$$

The maximum value of the transfer function described in (C.11) occurs at $\omega = \widetilde{\omega}$ where $\widetilde{\omega}$ is given by

$$\widetilde{\omega} = (G_L - g_0)g_1/(\overline{C}_{eq}^2 + g_1^2) \tag{C.12}$$

and $\overline{C}_{eq}$ is the average value of $C_{eq}(j\omega)$ at the vicinity of $\widetilde{\omega}$. By evaluating (C.11) at $\omega = \widetilde{\omega}$ we obtain

$$|A(j\widetilde{\omega})| = \frac{G_m}{|G_L - g_0|}\left[1 + \left(g_1/\overline{C}_{eq}\right)^2\right]^{\frac{1}{2}}. \tag{C.13}$$

The gain given by (C.13) can be significantly larger than the DC gain of the differential pair without the negative impedance generator (G_m/G_L).

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