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**Stress-Tolerant and Temperature-Stable RF MEMS Capacitive  
Switches and Tunable Filters**

A dissertation submitted in partial satisfaction of the  
requirements for the degree  
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Isak C. Reines

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Professor Gabriel M. Rebeiz, Chair  
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Professor Larry Larson

2010



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The dissertation of Isak C. Reines is approved, and it is acceptable in quality and form for publication on micro-film and electronically:

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Chair

University of California, San Diego

2010

## DEDICATION

To my grandfather Frederick Reines (Nobel Laureate 1995).

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## ABSTRACT OF THE DISSERTATION

### **Stress-Tolerant and Temperature-Stable RF MEMS Capacitive Switches and Tunable Filters**

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2010

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This dissertation presents RF MEMS capacitive switches which are based on a thin-film aluminum circular beam geometry that exhibit reduced sensitivity to both initial residual stress and stress-changes versus ambient temperature. The device symmetry also facilitates low-series-inductance compact device arrays for high-value capacitances. These switches are built in the Raytheon RF MEMS process and show an 8-10x improvement in temperature stability over the standard fixed-fixed beam designs. Also, cascadable RF MEMS switched capacitors are demonstrated that are suitable for VHF and UHF tunable filters and reconfigurable matching networks. These devices are fabricated in the UCSD and Raytheon RF MEMS processes and result in a near ideal capacitor impedance over a 30:1 frequency range. The circular geometry is then used to demonstrate an RF MEMS switched capacitor with  $> 10$  W power handling at 10 GHz

under hot-switching conditions that maintains a relatively-low ( $< 30$  V) pull-in voltage. The device consists of separate RF and DC electrodes, which are defined underneath a temperature-stable circular beam, to result in both increased restoring force above the RF electrode and higher RF self-actuation voltage.

This thesis also presents a compact low-loss tunable X-Band bandstop filter that is implemented on a quartz substrate using both miniature RF-MEMS capacitive switches and GaAs varactors. The 2-pole filter is based on capacitively loaded folded- $\lambda/2$  resonators that are coupled to a microstrip line, and the filter analysis includes the effects of non-adjacent inter-resonator coupling. The RF MEMS loaded filter results in a measured 25 dB improvement in power handling and linearity compared to the GaAs varactor design.

Finally, a 1.6-2.4 GHz suspended 3-pole RF MEMS tunable filter is presented. The filter results in an insertion loss of 1.34-3.03 dB over the tuning range and a 3-dB bandwidth of 201-279 MHz. This design results in a tunable  $Q_u$  of 50-150 over the frequency range, and to our knowledge, is the first suspended RF MEMS filter with the best  $Q_u$ . The Appendix presents in full detail the UCSD RF MEMS capacitive switch process on a high-resistivity silicon substrate.

# Chapter 1

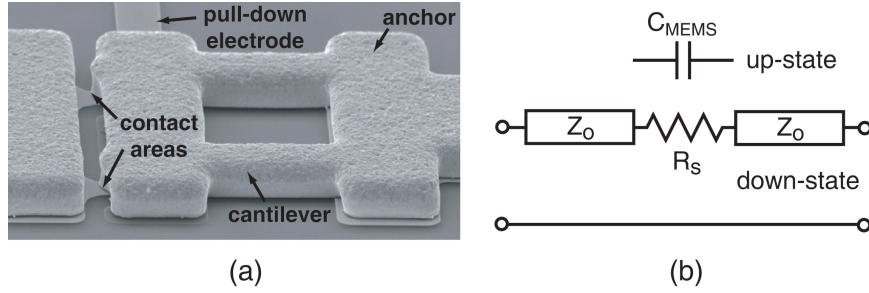
## Introduction

### 1.1 RF-MEMS Technology

Micro-Electro-Mechanical-Systems (MEMS) is the integration of mechanical elements, sensors, actuators, and electronics on a common substrate using micro-fabrication processes. MEMS devices vary in size from less than a micron to as large as several millimeters and are formed with standard “micro-machining” techniques, while the electronics are fabricated using integrated circuit (IC) processes (e.g. CMOS or Bipolar). The area of MEMS is extremely broad, and the devices which are designed to operate at the RF (Radio Frequency) to mm-wave frequencies (0.1 to 100 GHz) are called RF MEMS.

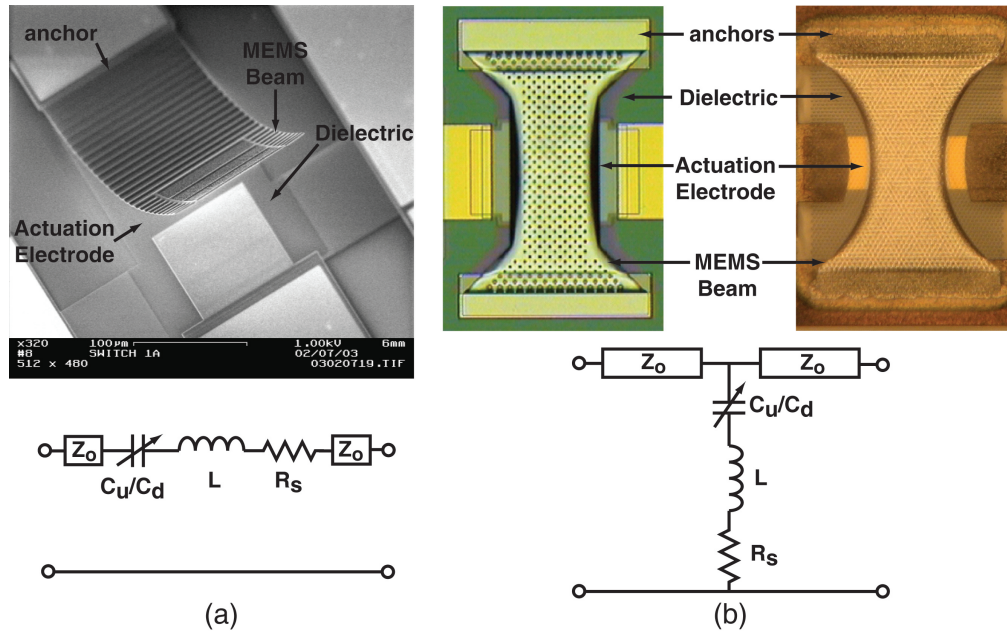
RF MEMS switches are miniature devices that use mechanical movement to create either a short or an open circuit in the transmission line. The forces required to achieve this mechanical displacement can be obtained using electrostatic, magnetostatic, piezoelectric, or thermal designs. Electrostatic actuation is the most commonly used due to its simplicity, compact size, and low power consumption. RF MEMS devices can be categorized by two configurations: metal-contact and capacitive-contact. Fig. 1.1a shows the Northwestern/Radant MEMS/Analog Device series metal-contact switch [3]. Series metal-contact switches present an open circuit in the up-state position due to the small capacitance ( $C_{up} < 10\text{-}20\text{ fF}$ ), while in the down-state position they act as a near short circuit ( $R_s < 1\text{-}2\ \Omega$ ) through the metal-to-metal contact (Fig. 1.1b). Metal-contact switches are typically used from DC-100 GHz with excellent performance.

Capacitive-contact devices use a metal-to-dielectric contact and can further be



**Figure 1.1:** Series metal-contact switch developed by Northwestern/ Radant MEMS/ Analog Device (a), and equivalent circuit model (b).

separated into three sub-categories: capacitive switches, switched capacitors, and analog varactors. Capacitive switches have a capacitance ratio of 20-150 and are mostly used as On/Off switches in applications such as phase shifters and switching networks. Fig. 1.2a shows the series capacitive switch developed by Lincoln Laboratory, while Fig. 1.2b shows the Raytheon (left), and MEMtronics (right) shunt capacitive switches.



**Figure 1.2:** Series capacitive switch developed by Lincoln Laboratory and equivalent circuit model (a), and shunt capacitive switches developed by Raytheon (left) and MEMtronics (right) along with the equivalent circuit model (b).

Switched capacitors have a capacitance ratio of 3-10 and are ideal devices for tunable filters, loaded-line phase shifters, and reconfigurable matching networks from

500 MHz to 100 GHz [4]- [6]. Analog varactors have a continuous tuning range of 1.5-8:1 and are well suited for applications that require precision tuning such as high-Q tunable filters where exact resonator loading is required [7]- [8].

RF MEMS switches have certain key advantages over PIN diodes and FET switches, which are the widely used for RF switching applications, that include:

1. *Very Low Insertion Loss*: Since RF MEMS switches are comprised of suspended metal structures instead of semiconductors, they inherently have very low conductor losses ( $< 0.05$ - $0.2$  from 1-100 GHz).
2. *Very High Isolation*: In the up-state position, MEMS metal-contact switches have air as a dielectric, and therefore have a very small off-state capacitance ( $C_u = 2$ - $16$  fF) resulting in very high isolation up to 40 GHz.
3. *Very High Linearity*: MEMS switches do not respond to varying electronic signals that are higher than the mechanical resonance frequency of the device, which is typically in the range of 10's of kHz to several MHz. Therefore, MEMS switches are very linear and produce low intermodulation products (20-50 dB better than GaAs or CMOS devices).
4. *Very Low Power Consumption*: Despite the high actuation voltage (20-100 V) requirement, there is virtually no DC current flowing into the device, and therefore MEMS switches have very low DC power consumption. It should be noted however, that the charge pump required to generate the MEMS bias voltage will consume 0.05-1 mW of power.
5. *Very High Cutoff Frequency*: The figure of merit for a series switch is the cutoff frequency,  $f_c = 1/(2\pi R_s C_u)$ , where  $R_s$  is the resistance in the on-state and  $C_u$  is the capacitance in the off-state. The cut-off frequency is 20-80 THz for MEMS switches compared to 1-4 THz for PIN diodes and 0.25-1 THz for FET switches.

Table 1.1 summarizes the performance of electro-static RF MEMS switches, FET switches, and PIN diodes. Despite all of these advantages, RF MEMS switches have their own share of issues which are currently hindering their commercial viability. Some of these concerns include:

1. *Reliability*: While the Radant-MEMS metal-contact switch has shown 200B cycles at 20 dBm ( $> 100$  devices), more research needs to be done on metal-contacts, creep, and a much larger number of devices need to be tested before widespread insertion into conservative application areas can occur. Capacitive switches such as the Lincoln Laboratories and Raytheon devices have demonstrated  $> 300$ B cycles, but these switches

**Table 1.1:** Performance comparison of FET switches, PIN diodes, and RF-MEMS electro-static switches [1]

Parameter	p-i-n Diode	FET	RF-MEMS
Voltage (V)	+/- 3-5	3-5	20-100
Current (mA)	3-20	0	0
Power Consumption (mW)	5 – 100 <sup>a</sup>	0.05 – 1 <sup>a</sup>	0.05 – 1 <sup>a</sup>
Switching Time	1-100 ns	1-100 ns	1-300 $\mu$ s
$C_u$ (Series) (fF)	40-80	70-140	2-16
$R_s$ (Series) ( $\Omega$ )	2-4	4-6	0.2-1
Capacitance Ratio	10	N/A	20 – 300 <sup>b</sup>
Cutoff Freq. (THz)	1-4	2-4	30-80
Isolation (1-10 GHz)	High	Medium	V.High
Isolation (10-40 GHz)	Medium	Low	V.High
Isolation (60-100 GHz)	Medium	None	High
Loss (1-100 GHz) (dB)	0.3-1.2	0.4-2.5	0.05-0.2
Power Handling (W)	< 10	< 10	5 – 10 <sup>c</sup>
$IIP_3$ (dBm)	27-50	27-50	66-80+

<sup>a</sup> Includes voltage up-converter or drive circuitry.

<sup>b</sup> Capacitive switch only. A ratio of 300 can be achieved with high- $\epsilon_r$  dielectrics.

<sup>c</sup> Power handling under hot-switching conditions.

still suffer from dielectric charging, and more work needs to be done to address this issue. Table 1.2 presents a current reliability summary for some of the more mature metal and capacitive-contact MEMS switches.

2. *Packaging*: MEMS switches need to be packaged in inert atmospheres (Nitrogen, Argon, etc..) and in very low humidity, which necessitates hermetic or near-hermetic seals. Hermetic packaging tends to increase the overall cost and can adversely effect the reliability and performance of the device.

3. *Switching Speed*: The switching speed of MEMS devices is in the range of 1-300  $\mu$ s, which is acceptable for many applications except certain communication and radar systems.

4. *Temperature Sensitivity*: MEMS switches based on fixed-fixed beam actuators such as the Raytheon and MEMtronics capacitive switches show a marked sensitivity to residual stress and temperature with pull-in voltage slopes vs. temperature between -0.2

to  $-0.3 \text{ V}/^{\circ}\text{C}$ .

5. *Power Handling*: The power-handling of both metal and capacitive-contact switches has steadily been improving and currently the Radant-MEMS switch has demonstrated  $> 10\text{B}$  cycles at  $10 \text{ W}$  under cold switching conditions, while the Raytheon capacitive switch has shown  $4\text{-}5 \text{ W}$  power-handling at  $10 \text{ GHz}$  under cold-switching operation. Still, some front-end transmit applications require  $25\text{-}50 \text{ W}$  power-handling under continuous RF power.

**Table 1.2:** Reliability summary of RF MEMS metal-contact and capacitive switches [2]

Parameter	RADANT	MIT-LL	Raytheon
Contact Type	Metal	Capacitive	Capacitive
Actuator Type	Cantilever	Cantilever	Bridge
Actuator Material	Au	$\text{SiO}_2/\text{Al}/\text{SiO}_2$	Al
Actuation Voltage (V)	90	55-65	30-40
Unipolar/Bipolar Actuation	40-80	70-140	2-16
Switching Speed ( $\mu\text{s}$ )	10	20	5
Capacitance Ratio	N/A	150:1	40:1
Metal Contact $R_{on}/C_{off}$ ( $\Omega/\text{fF}$ )	4/25 (2 contact)	N/A	N/A
Package Type	Hermetic Wafer Cap	Hermetic Wafer Cap	Hermetic Wafer Cap
<i>Reliability</i> <sup>a,b</sup> (# dev. tested)	200B at 20 dBm ( $>100$ )	600B at 0 dBm (6)	200B at 20 dBm (2)
	10B at 30 dBm ( $>50$ )		150B at 20 dBm (4)
	10B at 40 dBm ( $>10$ )		100B at 10 dBm (5)
Cycle Frequency (kHz)	20 <sup>c</sup>	5	5

<sup>a</sup> All tests stopped before switch failure.

<sup>b</sup> All reliability test done at  $10\text{-}35 \text{ GHz}$  when dBm is quoted.

<sup>c</sup> All switching waveforms have a 50% duty cycle.

Most of the current research in RF MEMS is focused on robust actuator design, power-handling, reliability, and packaging. The first part of this thesis is devoted to the realization of stress-tolerant and temperature-stable switched capacitors that exhibit reduced sensitivity to both initial in-plane stress and stress changes versus temperature, with measured pull-in voltage slopes versus temperature of only  $-22 \text{ mV}/^{\circ}\text{C}$ , which significantly extends the operating temperature of the device. The second part of this thesis focuses on improving the power-handling of RF MEMS switched capacitors. A new device is presented, which leverages a temperature-stable circular actuator, and consists of separate RF and DC electrodes that are routed under the beam to result in a larger spring constant under the RF electrode, resulting in both increased restoring force and RF self-actuation voltage. This switch demonstrates  $10\text{-}11 \text{ W}$  power handling under continuous RF power at  $10 \text{ GHz}$  with a relatively low actuation voltage ( $< 30 \text{ V}$ ).

## 1.2 Tunable Filter Overview

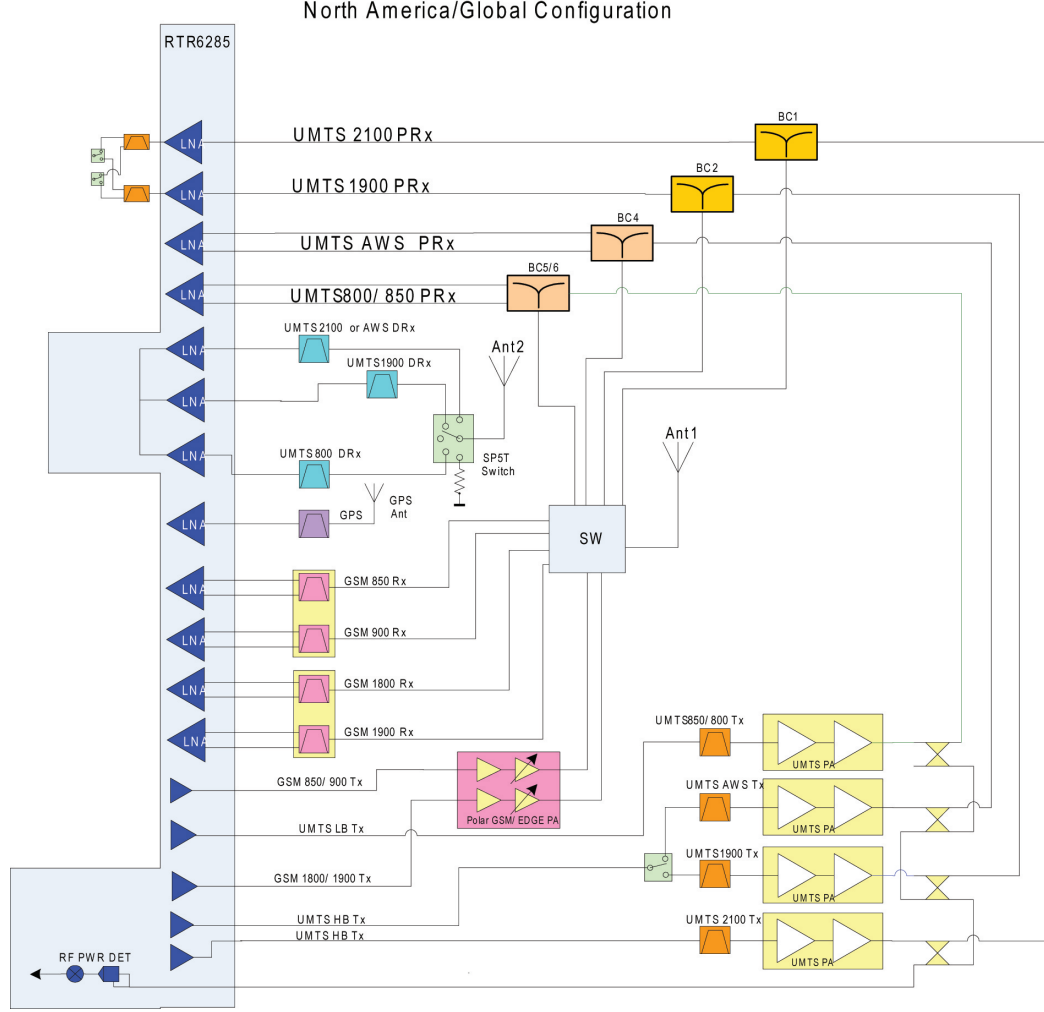
The trend in modern wireless communications systems is towards multi-band and multi-mode devices with increased adaptability and functionality. This trend is placing more stringent demands on the RF/microwave filters towards higher performance, smaller-size, lighter weight, and lower cost. Fig. 1.3 shows the architecture of a modern cell phone front-end with global system for mobile communication (GSM), code division multiple access (CDMA), and data channels covering 800 MHz to 2.4 GHz. This single silicon transceiver chip requires 14 fixed filters or diplexers which are implemented with either surface acoustic wave (SAW), or bulk acoustic wave (BAW) filters, and are selected using RF switching networks. The passive components on a multi-mode cell phone occupy 65-80% of the total RF board area. In order to reduce system size, weight, and complexity, it is of interest to replace the fixed filters with tunable filters (Fig. 1.4).

Tuning of the filter center frequency can be achieved by varying either the length or the inductive or capacitive loading of the resonators. Tunable filter technologies for wireless communications systems can be categorized into four tuner areas: YIG (Yttrium-Iron-Garnet) [9]- [12], BST (Barium Strontium Titanate) [13], varactor diode [14], and RF MEMS. YIG based tunable filters contain single-crystal Yttrium-Iron-Garnet spheres in the resonator and are controlled by applying DC magnetic field to change the ferromagnetic resonance frequency. These filters have multi-octave tuning, spurious free response, low insertion loss, and high quality factors. However, their power consumption, tuning speed, and weight are not suitable for low-cost portable wireless systems.

BST is a ferro-electric material that can be used as the dielectric in thin-film capacitors. Under paraelectric phase operation, the relative dielectric constant remains large ( $\epsilon_r \approx 300$ ) and can be tuned with an applied electric field supplied by DC voltages as low as 2-5 V [15]. BST capacitors have an  $IIP_3$  between 10-35 dBm, and due to their planar nature, can easily be fabricated with integrated circuits.

Varactor diodes have a capacitance that varies with reverse bias voltage across the diode. The advantage of varactor diodes is their fast switching speed, which is on the order of ns (limited by the bias network), and their small size. However, under large input signals the reversed bias diode turns on, which results in clipping, and creates harmonics and sub-harmonics which limit the dynamic range when used in a filter. Also, the low device Q at microwave frequencies results in a considerable loss when used in a



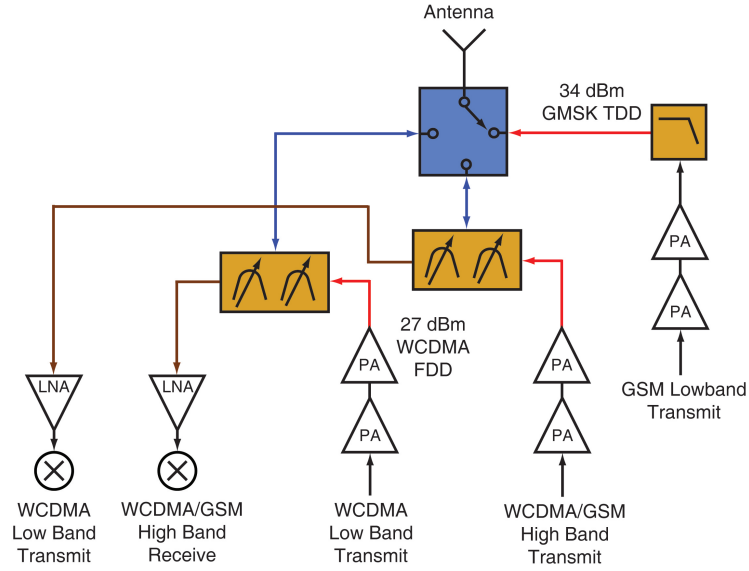


**Figure 1.3:** A modern cell phone front-end with four GSM bands, four UMTS bands, three diversity UMTS bands, GPS band for North American market.

tunable filter [16]- [17].

As discussed in section 1.1, an RF MEMS capacitive switch is an electro-mechanical device which is able to change its capacitance value in either an analog or digital fashion with an applied DC voltage. These switches have low loss and high  $Q$  (150-300) at RF and millimeter wave frequencies, and are very linear compared to varactor and BST tuning technologies [18]. Table 1.3 shows a performance comparison of different tunable filter technologies. It is clear from this comparison that none of these filter technologies can simultaneously satisfy all of the requirements for the “ideal” tunable filter.

The second subject area presented in this dissertation is the development of



**Figure 1.4:** The same cell phone front-end of Fig. 1.3 (without diversity) built using tunable filters and antennas.

high-performance tunable MEMS filters. An X-Band bandstop filter is demonstrated that provides a high level of rejection ( $> 24$  dB) over a limited bandwidth, which can be used to suppress spurious tones, block jamming signals, and to increase the isolation between the transmit and receive paths in high-power systems. The insertion loss of the bandstop filter is minimized so as not to impact receiver sensitivity. The compact low-loss bandstop filter is based on coupled folded  $\lambda/2$  resonators with capacitive loading and results in a  $Q$  of 135-60 from 11.34-8.82 GHz. The tunable filter is fabricated with miniature RF MEMS switches and GaAs varactors, and the performance is compared. In this work, for the first time, an analytic solution is presented for the effect of nonadjacent inter-resonator coupling in the notch filter. The final topic described in this thesis is the first demonstration of a suspended 3-pole RF MEMS bandpass filter with a  $Q$  of 50-150 from 1.6-2.4 GHz.

**Table 1.3:** Comparison of different tuning technologies [2]

Parameter	YIG	BST	Schottky Diode	p-i-n Diode	RF MEMS
Q	500-2000	30-150	30-150	$R_s=1\ \Omega$	$50 - 400^a$
Tuning Range	2-18 GHz	$C_r=2-3$	$C_r=3-5$	High	$C_r = 2 - 100^c$
Tuning Speed	ms	ns	ns	ns	$\mu s^d$
Linearity, $IIP_3(dBm)^e$	$\approx 20$	$10 - 35^b$	$10 - 35^b$	$>33$	$>60$
Power Handling ( $mW$ ) <sup>e</sup>	50-200	20-200	10-100	High	100-10000
Power Consumption	0.5-5 W	0	0	20-30 mA	0
Temperature Sensitivity	High	High	Low	Low	Low
Biasing	Magnet	High R	High-R	LC Choke	High-R
Planar	No	Yes	Yes	Yes	Yes
Cost	High	Low	Low	Low	$Low^f$

- PIN diode used as a switch capacitor tuner ( $R_s = 1\ \Omega$ ), 20-30 mA/diode.
- Q values given for 0.1-10 GHz applications for all devices except RF MEMS.
- Linearity and power handling for band-pass filter: 2-pole, 3-5% bandwidth.

<sup>a</sup> Q applicable for 0.1-100 GHz.

<sup>b</sup> Large values can be obtained as 1x3 arrays or anti-series diode pairs.

<sup>c</sup> MEMS used as an analog varactor or switched capacitor.

<sup>d</sup> Miniature MEMS can be switched at 200-800 ns.

<sup>e</sup> Power Handling and linearity are in tunable networks (filters) and are not in 50 $\Omega$  environments.

<sup>f</sup> Potential for low cost in high volume applications.

## Chapter 2

# Thin-Film RF MEMS Switched Capacitors with Stress-Tolerance and Temperature-Stability

### 2.1 Introduction

RF MEMS switched capacitors have been used extensively in a wide range of RF switching and reconfigurable networks with excellent performance due to their low-loss, high linearity, and low power consumption [1]- [24]. However, widespread insertion of RF MEMS switches into conservative application areas has yet to occur due to ongoing challenges in terms of reliability, power handling, packaging, and general robustness. Stable operation over temperature is a necessary criterion for any electronics technology.

Fixed-fixed beam RF MEMS capacitive switches typically have a marked sensitivity to temperature due to the fact the spring constant is highly dependent on the in-plane residual stress, which can change over temperature, if a difference in the thermal expansion coefficient (TCE) exists between the MEMS beam and substrate. The mechanical membrane in RF MEMS switches is often comprised of a metal layer which is anchored to an insulating substrate and results in a  $\sim 10\text{-}20$  ppm/ $^{\circ}\text{C}$  mismatch. Thermally induced stress changes lead to actuation voltages that can vary by as much as  $-0.1$  to  $-0.5$  V/ $^{\circ}\text{C}$ , depending on the particular choice of materials and device geometry [25]- [27].

One approach used to mitigate this issue is to match the TCE of the suspended

beam and the substrate materials [28]. This work has  $< 35 \text{ mV}/^\circ\text{C}$  actuation voltage slope over a  $150^\circ\text{C}$  temperature range, but is achieved at the expense of increased thermal and electrical bridge resistance, thus limiting the power handling capabilities. While the use of TCE matched materials minimizes the change in beam stress versus temperature, the spring constant of this device is still highly dependent on the initial in-plane stress, which can be difficult to control repeatedly, and can lead to varying device performance [28].

Another approach used to achieve temperature stability is to modify the switch geometry to reduce the effect of the fixed anchors on the suspended beam. H. Nieminen et al. demonstrated a pull-in voltage that varies less than 5% over a  $100^\circ\text{C}$  temperature range ( $< -6.5 \text{ mV}/^\circ\text{C}$ ) [29]. However, this design is very sensitive to vertical stress gradients, making it difficult to realize in thin metal fabrication processes. M. Ulm et al. presented a U-shape mechanical decoupling structure to reduce the temperature dependence of the switch [30]. This design functions mechanically like a fixed-free cantilever connected to a long and soft U-shaped spring, making it very sensitive to vertical stress gradients, while also introducing un-wanted bridge inductance and resistance.

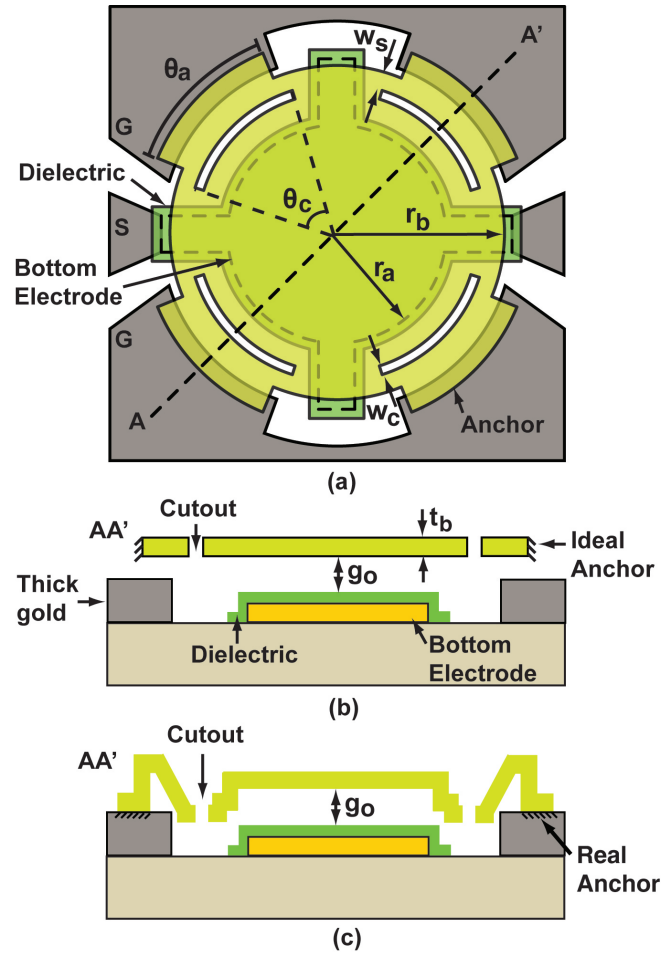
In this paper a symmetric circular switch geometry is investigated that can be designed within a thin metal process ( $t_b \leq 0.5 \text{ }\mu\text{m}$ ), while still tolerating moderate vertical stress gradients of  $\Delta\sigma \leq 20 \text{ MPa}/\mu\text{m}$ . The thin-film circular switch results in a pull-in voltage slope of  $-55 \text{ mV}/^\circ\text{C}$  measured from  $-5$ - $125^\circ\text{C}$ , which is achieved with low bridge inductance and resistance ( $L_s = 2 \text{ pH}$ ,  $R_s = 0.5 \text{ }\Omega$ ). This work is an extension to results published in [31]- [33], and includes detailed design information, stress analysis, and the effects of device topography.

## 2.2 Switch Design in the Raytheon RF MEMS Process

The spring constant of a fixed-fixed beam is given by  $K=K_1+K_2$ , where  $K_1$  is determined by the geometry, material properties, and the moment of inertia, and  $K_2$  is linearly dependent on the residual bi-axial beam stress. When the device is at a uniform temperature  $T$ , the fixed anchors exert a force on the suspended beam that changes the in-plane bi-axial beam stress as:

$$\sigma(T) = \sigma_{res} - [(\alpha_{beam} - \alpha_{sub})E(T_o - T)] \quad (2.1)$$

where  $\sigma_{res}$  is the initial residual stress at temperature  $T_o$ ,  $E$  is Young's modulus, and  $\alpha$  is the TCE of the beam and substrate, respectively. For  $T > T_o$  and  $\alpha_{beam} > \alpha_{sub}$ , the initial tensile beam stress is reduced leading to a drop in the spring constant and actuation voltage. At higher temperatures, the resulting beam stress becomes compressive leading to buckling of the beam and device failure. Therefore, in order to provide robust operation over temperature a perfectly symmetric circular geometry is investigated with the goal of minimizing the contribution of  $K_2$  relative to  $K_1$ . It should be noted, that in general achieving stress-tolerant and temperature-stable switches is easier with thick metal beams since  $K_1 \propto t_b^3$  and  $K_2 \propto t_b$ .



**Figure 2.1:** Top view of the RF MEMS switched capacitor (a), and device cross-section without topography (b), and with (c).

The switched capacitor was designed within the Raytheon RF MEMS fabrication process to result in an up and down-state capacitance of  $C_{up} = 50$  fF and  $C_d = 1$

**Table 2.1:** Circular RF MEMS Switched Capacitor Dimensions

Parameter	Value
$r_b$ ( $\mu\text{m}$ )	92
$r_a$ ( $\mu\text{m}$ )	60
$\theta_a$ (deg)	45
$\theta_c$ (deg)	55
$w_s$ ( $\mu\text{m}$ )	10
$w_c$ ( $\mu\text{m}$ )	5
$t_b$ ( $\mu\text{m}$ )	0.5
$g_0$ ( $\mu\text{m}$ )	3.5
$C_u, C_d$ (pF)	0.05/1
$K(K_1, K_2)^1$ (N/m)	10.31 (7.55, 2.76)
$V_p$ (V)	28

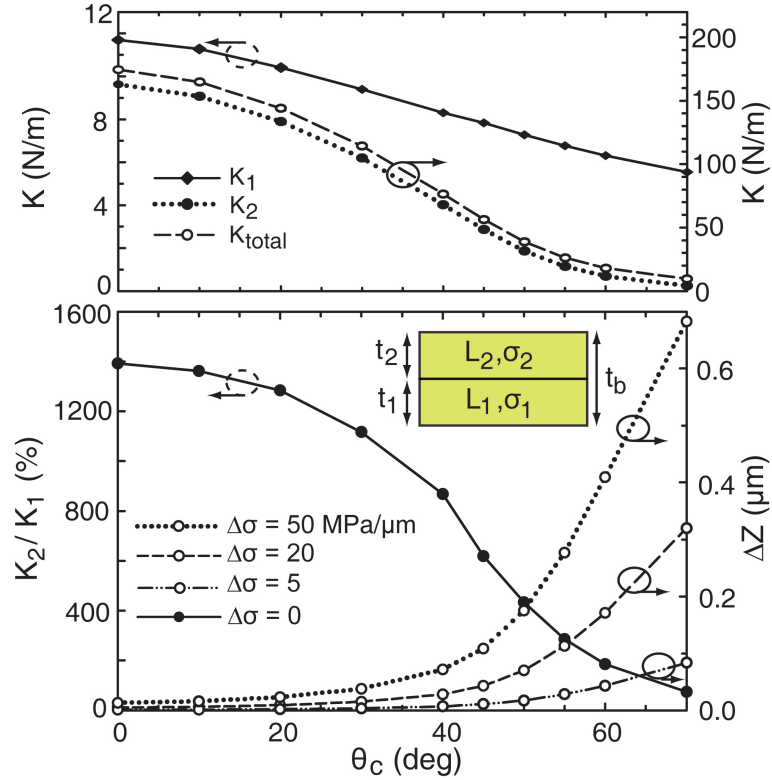
<sup>1</sup> Simulated with  $\sigma_{res} = 60$  MPa,  $\Delta\sigma = 10$  MPa/ $\mu\text{m}$

pF, respectively, which gives a capacitance ratio  $C_r = C_d/C_{up} = 20$ . The top-view of the switched capacitor and associated dimensions are shown in Fig. 2.1 and Table 2.1, along with cross-sections without beam topography (Fig. 2.1b) and with (Fig. 2.1c). The device is comprised of  $0.5 \mu\text{m}$ -thick circular aluminum beam with  $r_b = 92 \mu\text{m}$  that is anchored symmetrically in four locations each with an anchor angle  $\theta_a$ , and suspended with a gap height  $g_o = 3.5 \mu\text{m}$  above the bottom electrode. Arc-shaped cutouts with a width  $w_c = 5 \mu\text{m}$  and angle  $\theta_c$  are placed  $25 \mu\text{m}$  in front of each anchor to reduce the device sensitivity to residual bi-axial stress and temperature. The bottom electrode is shaped as a cross-hair (with  $r_a = 60 \mu\text{m}$ ) to provide symmetric actuation and to facilitate arraying of the devices (see Section 1.3). The switched capacitor is implemented in a shunt configuration on CPW transmission line and the device is actuated by supplying a DC voltage between the ground and signal electrodes.

### 2.2.1 Trade-off Between In-plane Bi-Axial Stress and Vertical Stress Gradient Effects

Due to the complex 3-D device geometry, finite element model (FEM) simulations of the circular switch were performed in Coventorware [34]. The spring constant is defined as the displacement ( $z$ ) in the center of the beam due to a uniform pressure

( $p$ ) distributed above the actuation electrode of area ( $a$ ), such that  $K = (p * a)/z$ . The simulation model assumes a Young's modulus of  $E = 77$  GPa and Poisson's ratio of  $\nu = 0.3$  for the aluminum beam, which is meshed with  $3 \mu\text{m}$  parabolic tetrahedral elements. Fig. 2.2 presents the spring constant as function of the cutout angle  $\theta_c$ , assuming anchors with a fixed angle of  $45^\circ$ ,  $\sigma_x = \sigma_y = \sigma_{res} = 60$  MPa,  $\sigma_z = 0$ , no underlying switch topography, and no vertical stress gradient (i.e.  $\Delta\sigma = 0$  MPa/ $\mu\text{m}$ ). Since the simulation model excludes topography, the ideal switch anchors are fixed in all directions on the side as shown in Fig. 2.1b.



**Figure 2.2:**  $K_1$ ,  $K_2$ , and  $K_{total}$  versus cutout angle ( $\theta_c$ ) with ( $\sigma_{res} = 60$  MPa,  $\Delta\sigma = 0$  MPa/ $\mu\text{m}$ ,  $\theta_a = 45^\circ$ ,  $t_b = 0.5 \mu\text{m}$ ) (top), and  $K_2/K_1$  versus  $\theta_c$  and initial vertical displacement with ( $\sigma_{avg} = 60$  MPa,  $\Delta\sigma = 5, 20$ , and  $50$  MPa/ $\mu\text{m}$ ) (bottom).

The total beam stiffness varies from 174.5-9.6 N/m for  $\theta_c$  between 0-70°, demonstrating the wide range of available spring constants given the fixed size and thickness of the beam. However, without cutouts (i.e.  $\theta_c = 0^\circ$ )  $K_2$  is dominant with a value of 162.8 N/m, demonstrating a marked sensitivity to residual stress and temperature. As  $\theta_c$  increases,  $K_2$  drops to 4.1 N/m ( $\theta_c = 70^\circ$ ). The arc-shaped cutouts are essential for robust device operation over temperature as they function to mechanically decouple the



center portion of the circular plate from the effects of the fixed anchor. In general, to achieve stable operation over temperature,  $\theta_c$  should be  $> \theta_a$ .

In order to model the effects of a vertical stepped stress gradient ( $\Delta\sigma$ ) on the circular switch, the aluminum beam is divided into two equal-thickness layers ( $t_1=t_2=t_b/2$ ) (Fig. 2.2) which are assigned different in-plane stress values  $\sigma_1$ , and  $\sigma_2$  such that the average in-plane stress ( $\sigma_{avg}$ ) remains constant with:

$$\sigma_{avg} = \frac{\sigma_1 t_1 + \sigma_2 t_2}{t_b} = 60 \text{ MPa} \quad (2.2)$$

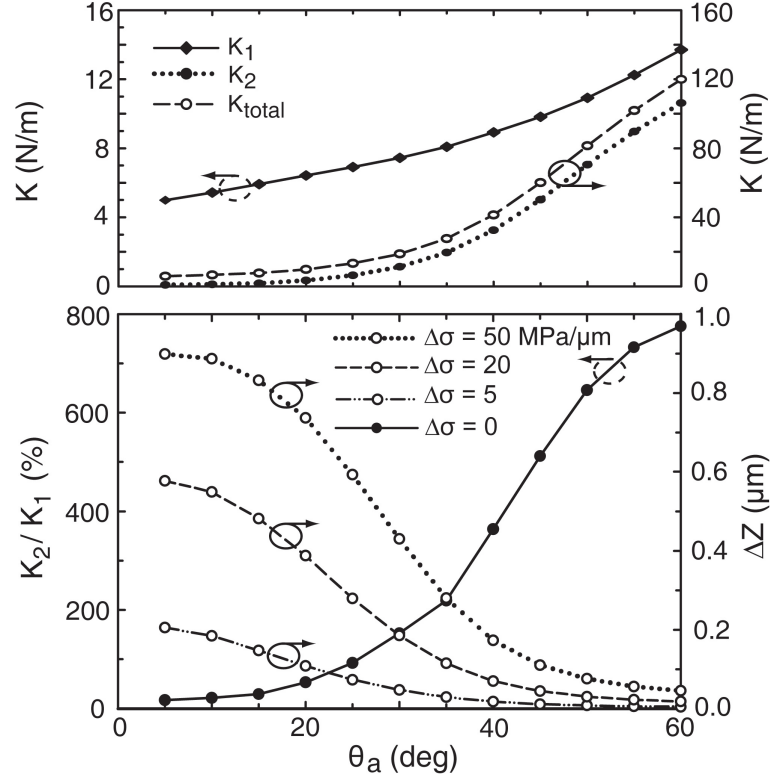
$$\Delta\sigma = \frac{\sigma_1 - \sigma_2}{t_b} \text{ MPa}/\mu\text{m} \quad (2.3)$$

Sputtered and evaporated thin metal films typically have a built in negative stress gradient (i.e.  $\sigma_1 > \sigma_2$ ), which is modeled by assigning the bottom layer of the beam  $L_1$  a higher tensile stress than the top layer  $L_2$ . It should be noted, that the “two-layer” stepped stress gradient ( $\Delta\sigma$ ), which is referred to in this thesis, can be converted into an equivalent “linearized” stress gradient ( $\Delta\sigma_{lin}$ ) with [1]:

$$\Delta\sigma_{lin} = \frac{3}{2}\Delta\sigma \quad (2.4)$$

Fig. 2.2 also presents the simulated ratio of  $K_2/K_1$  versus  $\theta_c$ , along with the initial change in the vertical displacement ( $\Delta Z$ ) in the center of the beam for stress gradients of  $\Delta\sigma = 5, 20$ , and  $50 \text{ MPa}/\mu\text{m}$ . A trade-off exists between the device sensitivity to in-plane bi-axial stress and vertical displacements arising from stress gradients. As  $\theta_c$  is increased, the device sensitivity to in-plane stress is reduced and  $K_2/K_1$  drops from 1393% ( $\theta_c = 0^\circ$ ) to 73% ( $\theta_c = 70^\circ$ ). However,  $\Delta Z$  increases with  $\theta_c$  and is  $0.32 \mu\text{m}$  for  $\Delta\sigma = 20 \text{ MPa}/\mu\text{m}$  and  $\theta_c = 70^\circ$ .

Another degree of freedom in the switch design is the anchor angle  $\theta_a$ . Fig. 2.3 shows the simulated spring constant plotted versus  $\theta_a$  given a fixed arc-cutout angle of  $\theta_c = 45^\circ$ . The total spring constant varies from 5.8-120 N/m for  $\theta_a = 5-60^\circ$ , while the ratio of  $K_2/K_1$  is 17-775% across this range indicating more in-plane stress dependence for larger anchor angles. Fig. 2.3 also presents  $\Delta Z$  versus  $\Delta\sigma$ , which again illustrates the trade-off between in-plane bi-axial stress dependence and vertical beam displacements arising from stress gradients. Proper selection of  $\theta_a$  and  $\theta_c$  therefore requires some prior knowledge of the vertical stress gradients in the mechanical beam layer. If the fabrication process results in a high-stress gradient beam layer, then  $\theta_c$  must be reduced for a given  $\theta_a$  in order to minimize  $\Delta Z$ . However, if a low-stress gradient process can be achieved



**Figure 2.3:**  $K_1$ ,  $K_2$ , and  $K_{total}$  versus anchor angle  $\theta_a$  with ( $\sigma_{res} = 60$  MPa,  $\Delta\sigma = 0$  MPa/ $\mu\text{m}$ ,  $\theta_c = 45^\circ\text{C}$ ,  $t_b = 0.5$   $\mu\text{m}$ ) (top), and  $K_2/K_1$  versus  $\theta_a$  and initial vertical displacement with ( $\sigma_{avg} = 60$  MPa,  $\Delta\sigma = 5, 20$ , and  $50$  MPa/ $\mu\text{m}$ ) (bottom).

in fabrication, then  $\theta_c$  can be increased to reduce the device sensitivity to in-plane bi-axial stress and temperature. Ideally, to provide robust operation over temperature the vertical stress gradient in the mechanical beam layer should be minimized allowing  $\theta_c$  to be maximized for a given  $\theta_a$ .

The thin  $0.5$   $\mu\text{m}$  aluminum beam as deposited by Raytheon has a typical average in-plane stress of  $60$  MPa and a vertical stress gradient of  $\Delta\sigma \leq 20$  MPa/ $\mu\text{m}$ . The required spring constant can be calculated using [1]:

$$K = \frac{27V_p^2 C_{up}}{8g_0^2} \quad (2.5)$$

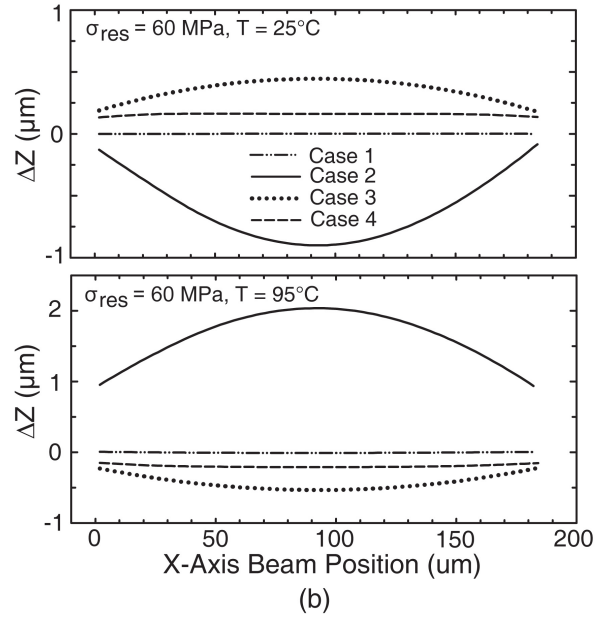
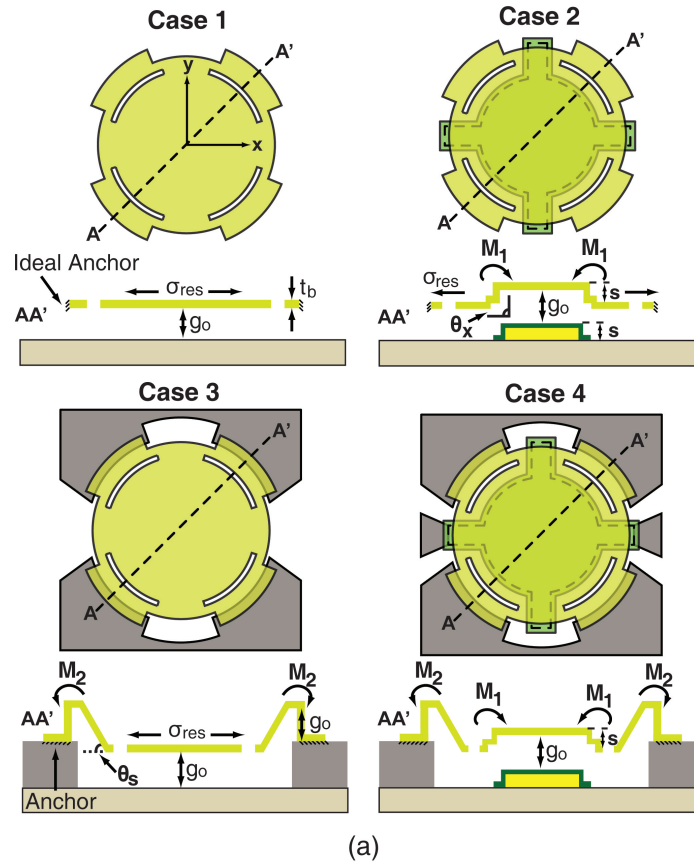
once the nominal switch gap ( $g_0$ ), up-state capacitance ( $C_{up}$ ), and switch pull-in voltage ( $V_p$ ) are specified. Given the required spring constant and expected stress gradient, base-line values for  $\theta_a$  and  $\theta_c$  can now be selected as shown in Table 2.1.

### 2.2.2 Effects of Topography

Without planarization processes during device fabrication, the underlying topography from the bottom electrode, dielectric, and thick gold post layers are transferred into the MEMS beam, since the sacrificial layer deposition is a semi-conformal process. The resulting topography of the sacrificial layer creates “*vertical steps*” in the membrane that follow the location and height of the underlying layers and are therefore locally non-symmetric and non-periodic. Periodic and symmetric vertical steps in the MEMS beam, are often referred to as vertical “*corrugations*,” and have been used extensively in the design of MEMS sensors, actuators, and RF MEMS switches to reduce stress and process dependence, lower actuation voltage and spring constant, and improve temperature stability [35]- [40]. While the non-symmetric vertical steps described here also function to reduce the stress dependence of the beam, unlike corrugations, their asymmetry can result in significant vertical beam displacement versus in-plane stress and temperature. The bending moments created by the vertical steps in the beam must be balanced to assure a stable up-state capacitance and actuation voltage.

Fig. 2.4a presents the top-view and cross-sections of four different cases of beam topography for the circular switch. Case 1 represents a perfectly flat circular membrane without any underlying topography, while case 2 depicts the topography in the beam from both the 0.5  $\mu\text{m}$ -thick bottom metal and 0.28  $\mu\text{m}$  dielectric layers assuming a sidewall angle  $\theta_x = 90^\circ$ , and total vertical step height of  $s = 0.78 \mu\text{m}$ . Ideal anchors are used in both cases 1 and 2. Case 3 represents only the topography in the anchor area that is created when the sacrificial layer is spun and patterned on top of the 3  $\mu\text{m}$ -thick post metal. In case 3, the side-wall angle  $\theta_s = 30^\circ$  (based on measured profiles of actual devices), while the step height is set by the sacrificial layer thickness  $g_o$ . Case 4 is the addition of case 2 and 3 and represents the real topography that exists in the circular switch. The simulation models in all cases assume a surface conformality factor (SCF) of 1 for the beam. While the height of the different vertical steps are fixed by the design and fabrication process, in general the larger the vertical step the larger the bending moment and amount of stress reduction.

The change in vertical displacement of the 0.5  $\mu\text{m}$ -thick beam is simulated with  $\sigma_{res} = 60 \text{ MPa}$  at  $T = 25^\circ\text{C}$  and  $95^\circ\text{C}$ , given  $T_o = 25^\circ\text{C}$ ,  $\Delta\sigma = 0 \text{ MPa}/\mu\text{m}$ , and  $g_o = 3.5 \mu\text{m}$  (Fig. 2.4b). For case 1 (without topography)  $\Delta Z = 0 \mu\text{m}$  at both  $25^\circ\text{C}$  and  $95^\circ\text{C}$ , while in case 2 the vertical steps in the beam profile create bending moments  $M_1$



**Figure 2.4:** Top view and cross-sections of 4 cases of switch topography (a), and the change in vertical displacement ( $\Delta Z$ ) of the beam versus x-axis position at both  $25^\circ\text{C}$  and  $95^\circ\text{C}$ , with ( $\sigma_{res} = 60 \text{ MPa}$ ,  $\Delta\sigma = 0 \text{ MPa}/\mu\text{m}$ , and  $T_o = 25^\circ\text{C}$ ) (b).

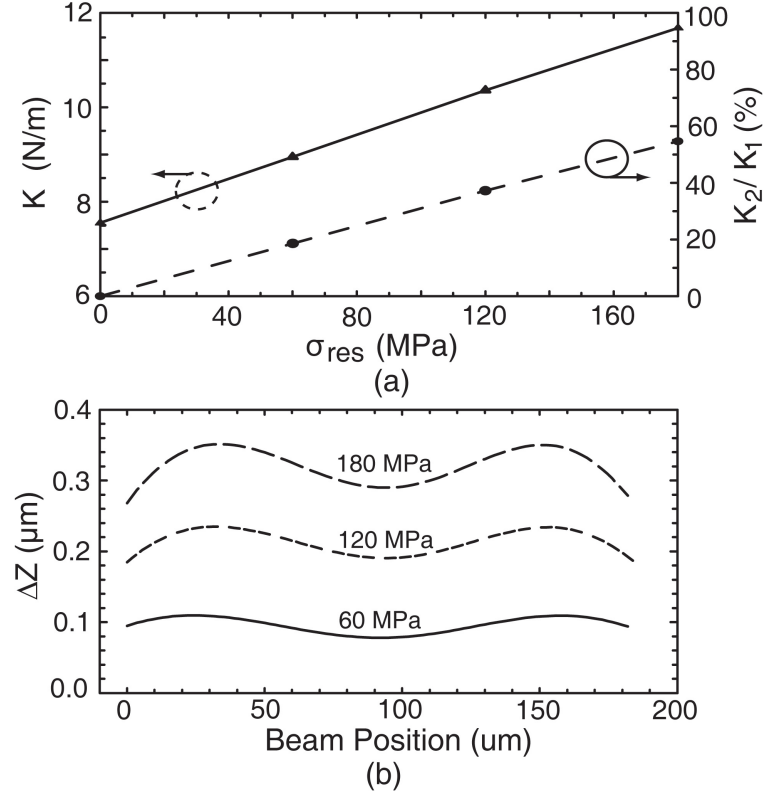
which yield an initial  $\Delta Z = -0.9 \mu\text{m}$  in the beam center. For case 2, with  $T = 95^\circ\text{C}$ ,  $M_1$  reverses direction resulting in a maximum  $\Delta Z = 2 \mu\text{m}$ . In case 3, the bending moments  $M_2$  result in  $\Delta Z = 0.45$  and  $-0.54 \mu\text{m}$  at  $25^\circ\text{C}$  and  $95^\circ\text{C}$ , respectively. In case 4,  $M_1$  and  $M_2$  are in opposition leading to a reduced deflection of  $0.16 \mu\text{m}$ , and  $-0.21 \mu\text{m}$ , at  $25^\circ\text{C}$  and  $95^\circ\text{C}$ , respectively, resulting in a balanced design. These simulation results show that the beam topography must be considered in the switch design as it results in vertical beam displacements versus both initial in-plane bi-axial stress and temperature, which if not minimized can lead to excessively varying up-state capacitance and pull-in voltage.

### 2.2.3 In-Plane Bi-Axial Stress and Temperature Including Device Topography

For case 4 with  $\sigma_{res} = 0\text{-}180 \text{ MPa}$ , the simulated spring constant is  $7.55\text{-}11.68 \text{ N/m}$  (Fig. 2.5a). With  $\sigma_{res} = 60 \text{ MPa}$ ,  $K = 8.95 \text{ N/m}$  with  $K_1 = 7.55 \text{ N/m}$  and  $K_2 = 1.4 \text{ N/m}$ , resulting in  $K_2/K_1 = 18.5\%$ . For comparison, an ideal rectangular aluminum fixed-fixed beam with  $w = 80 \mu\text{m}$ ,  $l = 121.6 \mu\text{m}$ , and  $t_b = 0.5 \mu\text{m}$ , results in the same  $K_1$  as the circular design assuming a distributed force above the center third of the beam [1]. However, with  $\sigma_{res} = 60 \text{ MPa}$ ,  $K$  increases to  $71 \text{ N/m}$  resulting in a  $K_2/K_1$  ratio of  $840\%$  demonstrating a high sensitivity to in-plane bi-axial stress and temperature. Under a tensile beam stress the bending moments  $M_2$  from the anchor topography dominate causing an initial upward deflection in the center of the beam of  $0.09\text{-}0.29 \mu\text{m}$  for  $\sigma_{res} = 60\text{-}180 \text{ MPa}$  (Fig. 2.5b).

The spring constant and beam profile were simulated for  $T = -30^\circ\text{C}$  to  $120^\circ\text{C}$ , assuming  $\sigma_{res} = 60$  and  $120 \text{ MPa}$  at  $T_o = 25^\circ\text{C}$  (Fig. 2.6). In order to reduce memory in the FEM simulations, the substrate is not included in the model, each beam anchor is fixed in position, and the TCE of the aluminum beam ( $\alpha_{beam}$ ) is reduced from  $23.1$  to  $16.3 \text{ ppm}/^\circ\text{C}$  to account for the expansion of the alumina substrate ( $\alpha_{sub} = 6.8 \text{ ppm}/^\circ\text{C}$ ). The change in beam stress versus temperature results in a linearly decreasing spring constant from  $11.4$  to  $5.2 \text{ N/m}$  for  $\sigma_{res} = 60 \text{ MPa}$ , yielding a slope of  $-51.7 \text{ mN}/^\circ\text{C}$ .

Fig. 2.6b presents  $\Delta Z$  as a function of beam position and temperature for  $\sigma_{res} = 60$  and  $120 \text{ MPa}$  at  $T_o = 25^\circ\text{C}$ . The dominant bending moments  $M_2$  result in a negative displacement for  $T > T_o$  and positive displacement for  $T < T_o$ . From  $-30^\circ\text{C}$  to  $120^\circ\text{C}$ , the center of the beam displaces downward by  $\sim 0.4 \mu\text{m}$  for both  $\sigma_{res} = 60$  and



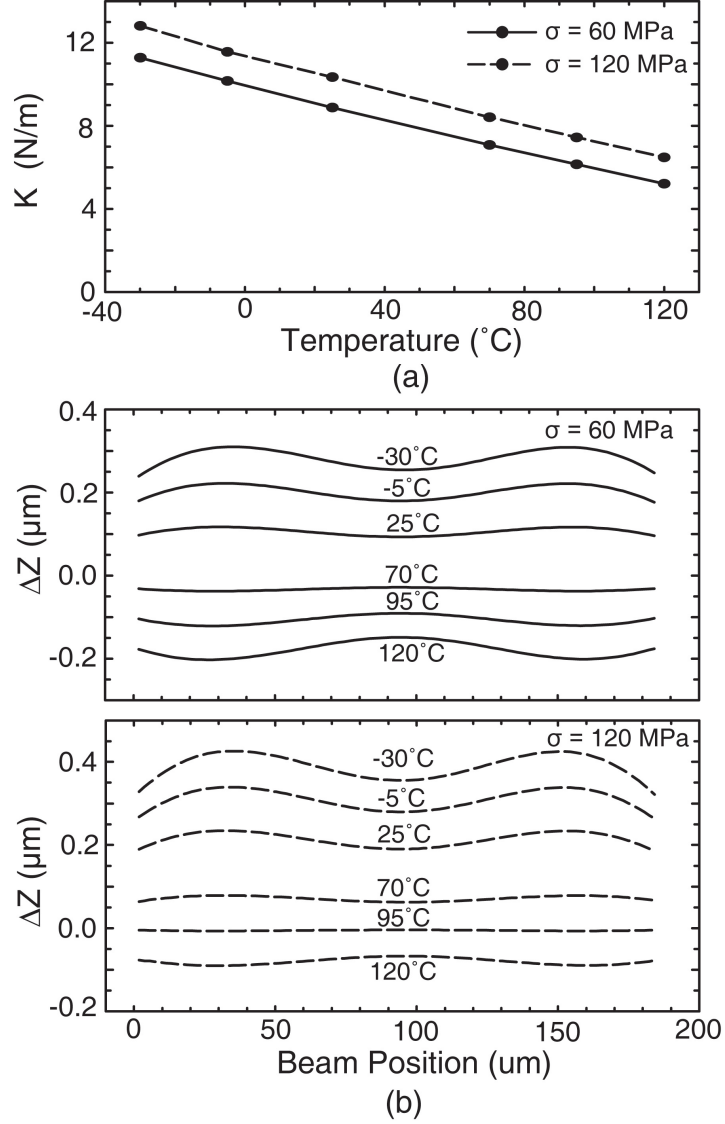
**Figure 2.5:** Simulated spring constant and  $K_2/K_1$  versus in-plane bi-axial stress (a), and  $\Delta Z$  versus beam position with ( $g_0 = 3.5 \mu\text{m}$ ,  $\sigma_{res} = 60, 120$ , and  $180 \text{ MPa}$  at  $T_o = 25^\circ\text{C}$ ) (b).

120 MPa.

#### 2.2.4 Vertical Stress Gradients and Temperature Including Device Topography

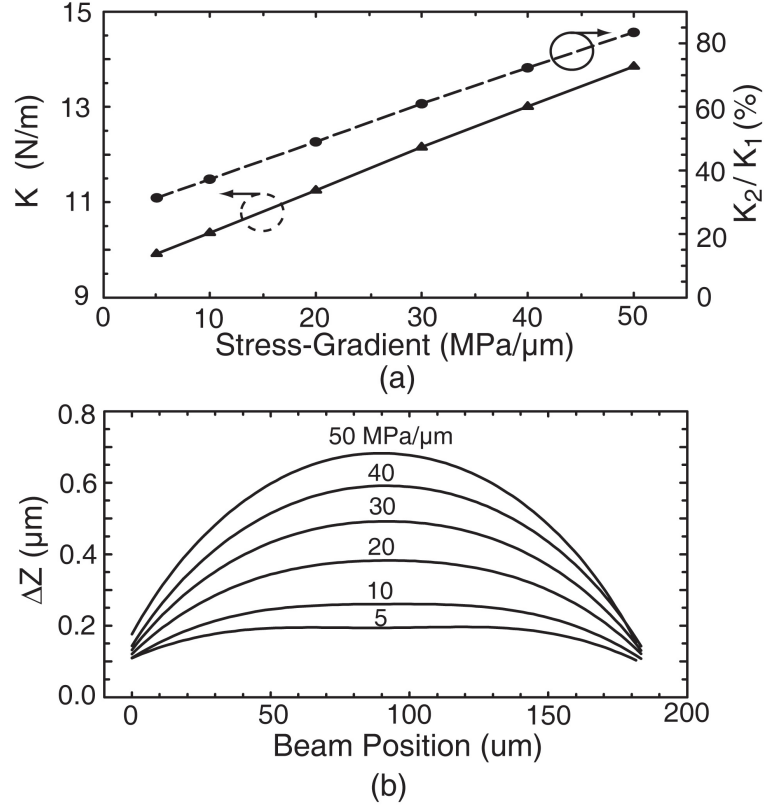
The presence of a vertical stress gradient in the circular switch leads to an upward curling of the beam which results in a stiffening of the spring constant. For case 4 and with  $\Delta\sigma = 5\text{-}50 \text{ MPa}/\mu\text{m}$ ,  $K$  increases from 9.92 to 13.85 N/m while  $K_2/K_1$  rises from 31.4-83.4% (Fig. 2.7a). Also, the center of the circular beam displaces upward by 0.19 to 0.68  $\mu\text{m}$  for  $\Delta\sigma = 5\text{-}50 \text{ MPa}/\mu\text{m}$  (Fig. 2.7b). For  $\Delta\sigma > 20 \text{ MPa}/\mu\text{m}$ ,  $\Delta Z > 10\%$   $g_0$ , which is non-ideal for this switch design.

Simulations of  $K$  versus temperature from  $-30\text{-}120^\circ\text{C}$  were also performed for  $\Delta\sigma = 5, 10$ , and  $50 \text{ MPa}/\mu\text{m}$ , and show a decrease in  $K$  of 6.3 N/m due to thermal stress changes independent of  $\Delta\sigma$  (Fig. 2.8a). The dominant bending moments  $M_2$  from the



**Figure 2.6:** Simulated spring constant versus ambient temperature with ( $T_o = 25^{\circ}\text{C}$ ,  $\sigma_{res} = 60$  and 120 MPa) (a), and the change in z-displacement versus beam position and ambient temperature with ( $\sigma_{res} = 60$  MPa and 120 MPa) (b).

anchor topography again cause a downward beam deflection for  $T > T_o$  and an upward for  $T < T_o$  (Fig. 2.8b). With  $\Delta\sigma = 5 \text{ MPa}/\mu\text{m}$ , the average beam displacement above the underlying actuation electrode deflects downward by  $-0.36 \mu\text{m}$  from  $-5$ - $95^{\circ}\text{C}$ , representing an 10.2 % change in the nominal switch gap. When the switch is under a relatively high stress gradient of  $50 \text{ MPa}/\mu\text{m}$ , the average  $\Delta Z$  above the actuation electrode is reduced to  $-0.16 \mu\text{m}$  from  $-5$ - $95^{\circ}\text{C}$ , as a result of the stiffer spring constant (Fig. 2.8b). These simulations indicate that the vertical stress gradient should be minimized in order to



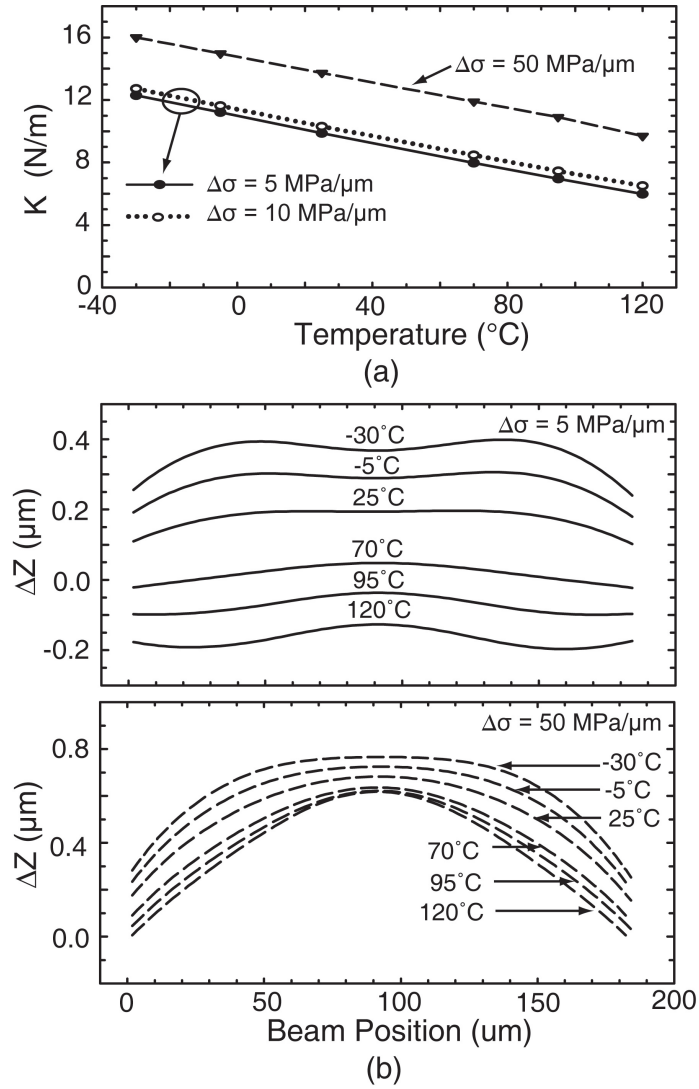
**Figure 2.7:** Simulated spring constant and  $K_2/K_1$  versus vertical stress gradients with  $\sigma_{avg} = 60$  MPa (a), and change in z-displacement versus beam position for  $\Delta\sigma$  from 5 to 50 MPa/μm (b).

provide stable operation over temperature since  $V_p \propto \sqrt{K}$ , and  $g_0^{1.5}$ , while  $C_{up} \propto 1/g_0$ .

### 2.3 Compact Switch Arrays

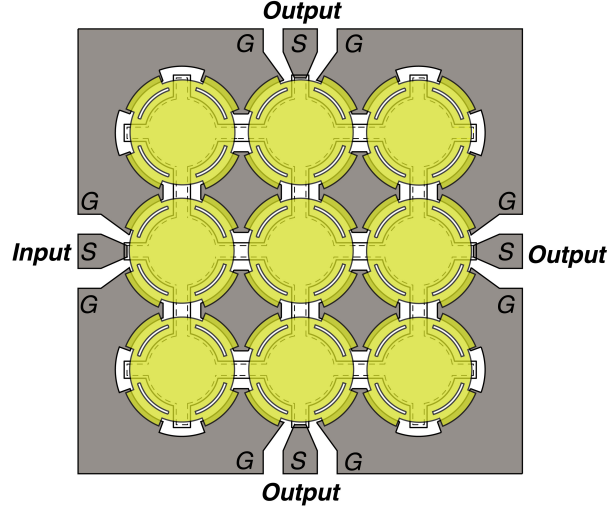
VHF-UHF tunable filters and reconfigurable matching networks require high-value switched capacitors. Achieving large capacitances with a single MEMS switch necessitates either scaling the device size up to increase the capacitive area or reducing the thickness of the dielectric, both of which are non-optimal choices. Another approach is to array the single circular switch by connecting the actuation electrodes in the x-y directions while keeping each beam mechanically separated (Fig. 2.9) [32], [6]. This is possible due to the symmetry of the circular switch which facilitates low-series-inductance interconnects between the separate devices resulting in a near ideal capacitor impedance. This topology can also be extended to 4x4 or even 8x8 arrays, while the output can be





**Figure 2.8:** Simulated spring constant versus ambient temperature with ( $T_o = 25^{\circ}\text{C}$ ,  $\Delta\sigma = 5, 10$ , and  $50$  MPa/ $\mu\text{m}$ ) (a), and  $\Delta Z$  versus beam position and ambient temperature with ( $\sigma_{avg} = 60$  MPa,  $\Delta\sigma = 5$  MPa/ $\mu\text{m}$ , and  $50$  MPa/ $\mu\text{m}$ ) (b).

taken from the “north” or “south” sides of the chip depending on it’s location in the reconfigurable network. These device arrays can also be arranged together to provide multi-bit capacitive tuners. Despite being mechanically separated, the individual circular beams have been shown to act in perfect mechanical phase [32].



**Figure 2.9:** Compact 3x3 switched capacitor array layout.

Compact 2x2 and 3x2 switched capacitor arrays have been implemented in a 2-port CPW transmission line to achieve down-state capacitance values of 4 and 6 pF, respectively. The 2x2 and 3x2 arrays have areas of 0.343 and 0.462  $mm^2$ , respectively. The short section of transmission line between each switch has an impedance of  $Z_0 = 66 \Omega$  and series inductance of 50 pH, and the equivalent circuit model is presented in Section 2.7.4 (Fig. 2.22b).

## 2.4 RF Power Dissipation in the Circular MEMS Beam

The power dissipated in the MEMS bridge ( $P_d$ ) can be calculated using

$$Loss = 1 - |S_{11}|^2 - |S_{21}|^2 \quad (2.6)$$

where this loss includes both the loss from the transmission line and the MEMS bridge. This is particularly useful since the symmetric circular MEMS switch (in a CPW transmission line), results in multiple impedance transitions from the nominal 50  $\Omega$  input and output impedance.

In order to extract only the power dissipated in the MEMS bridge, the switch is simulated in a full-wave EM simulator Sonnet [41] with the aluminum bridge having a finite conductivity ( $\sigma_{AL} = 3.77 \times 10^7$  S/m), while the CPW transmission lines, switch dielectric, substrate, and box walls are assumed lossless. The switch is simulated in the up-state position at 10 GHz with gap heights of  $g_0 = 4.1 \mu\text{m}$  and  $2.73 \mu\text{m}$  ( $2/3g_0$ ,  $V_{applied} = V_p$ ) (Table 2.2). The  $0.5 \mu\text{m}$  aluminum bridge dissipates 0.43-0.52% of the incident power in the up-state position with  $C_{up} = 51\text{-}70$  fF, which for  $P_{in} = 5$  W, results in 21.9-26.1 mW of power dissipated in the MEMS bridge. In the down-state position with  $C_d = 1$  pF, 1.03% of the incident power is dissipated in the bridge, which for  $P_{in} = 5$  W, yields  $P_d = 51.3$  mW.

**Table 2.2:** Simulated Power Dissipated in the MEMS Bridge at 10 GHz with  $P_{in} = 5$  W.

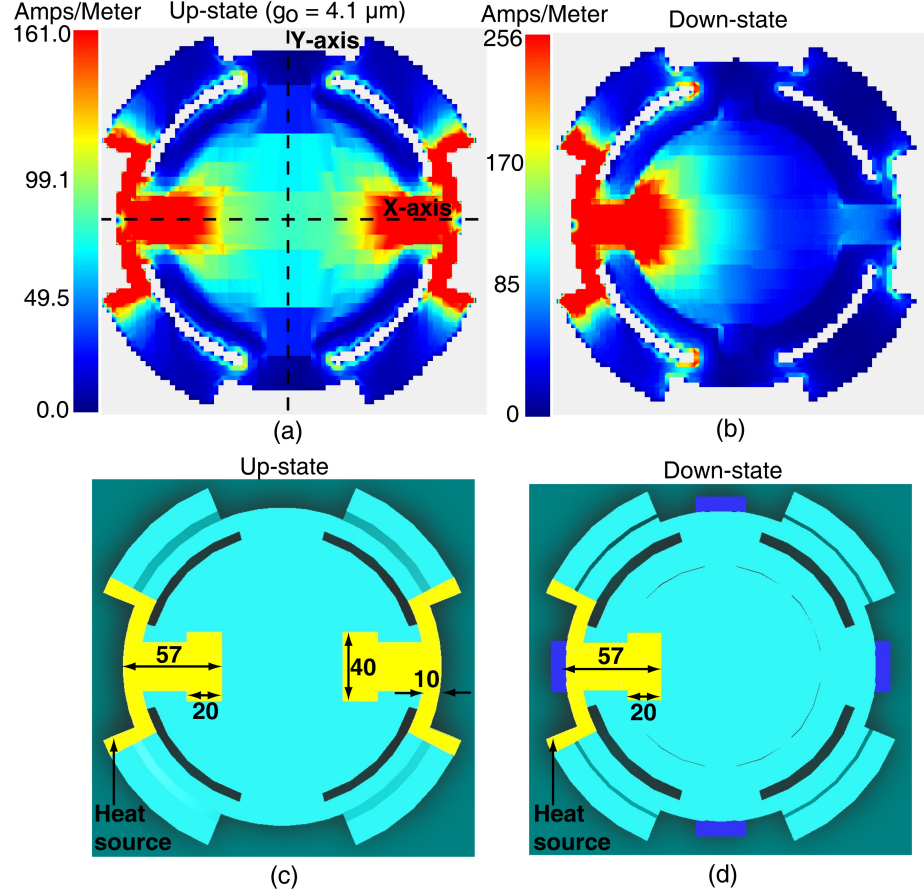
Gap ( $\mu\text{m}$ )	$C$ (pF)	$S_{11}$ (%)	$S_{21}$ (%)	$P_d$ (%)	$P_d$ (mW)
4.1	0.051	0.641	98.930	0.434	21.9
2.73	0.070	1.147	98.330	0.523	26.1
0 (down-state)	1.000	73.238	25.736	1.026	51.3

The RF current distribution on the circular MEMS bridge is also simulated at 10 GHz in both the up and down-state positions with  $P_{in} = 20$  mW. In the up-state position, the RF current is mainly concentrated in the thin  $10 \mu\text{m}$  switch springs and the section of the beam directly above both the input and output transmission lines (Fig. 2.10a). The current distribution in the down-state position is concentrated on the input side of the circular beam above the underlying transmission line and in the switch springs, since these areas presents a short circuit for the incoming power (Fig. 2.10b). These respective current distributions are used to determine the position of the heat sources in the steady-state thermo-mechanical simulations presented Section 2.5.

## 2.5 Steady-State Thermo-Mechanical Simulations

In this section, we show that the circular temperature-stable RF MEMS shunt capacitive switch fabricated in the Raytheon process exhibits an increasing spring constant and decreasing up-state capacitance under high-RF power levels. This results in a device which does not suffer from self-actuation and can handle high-RF power levels under cold switching applications.

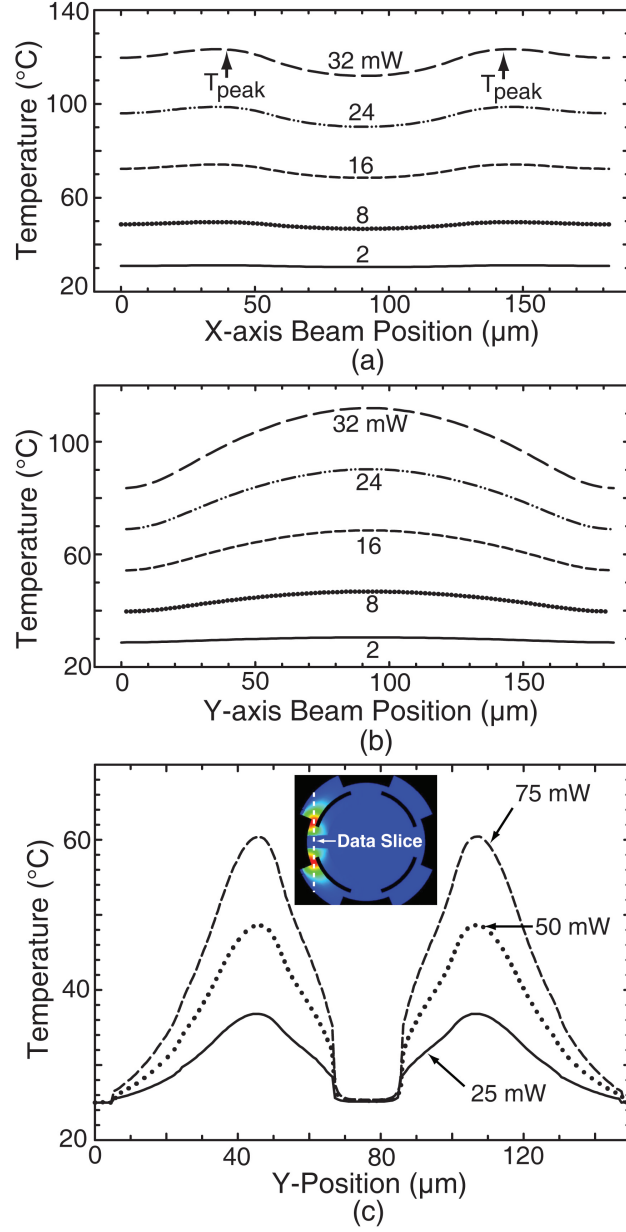
Thermo-mechanical simulations of the switch in both the up and down-state



**Figure 2.10:** Simulated RF current distribution on the circular RF MEMS switch at  $f_0 = 10$  GHz with  $P_{in} = 20$  mW in the up-state position with  $g_0 = 4.1 \mu\text{m}$  (a), down-state position (b), and placement of the heat sources in the up and down-state Coventorware thermo-mechanical simulations (c,d).

positions are performed in Coventorware with the location and dimensions of the heat sources shown in Fig. 2.10(c,d). In these simulations, a uniform power is applied on all shown areas such that the total power dissipated in the bridge is between 2-32 mW (up-state), and 25-75 mW (down-state). Since the skin depth is  $0.79 \mu\text{m}$  at  $f_0 = 10$  GHz, volumetric heat sources are used for the  $0.5 \mu\text{m}$ -thick MEMS beam. Heat transfer through conduction is considered while radiation and convection losses are ignored [1], [42]. The temperature of the bridge anchors, underside of the bottom electrode, and surrounding ambient are all set to  $T = 25^\circ\text{C}$ .

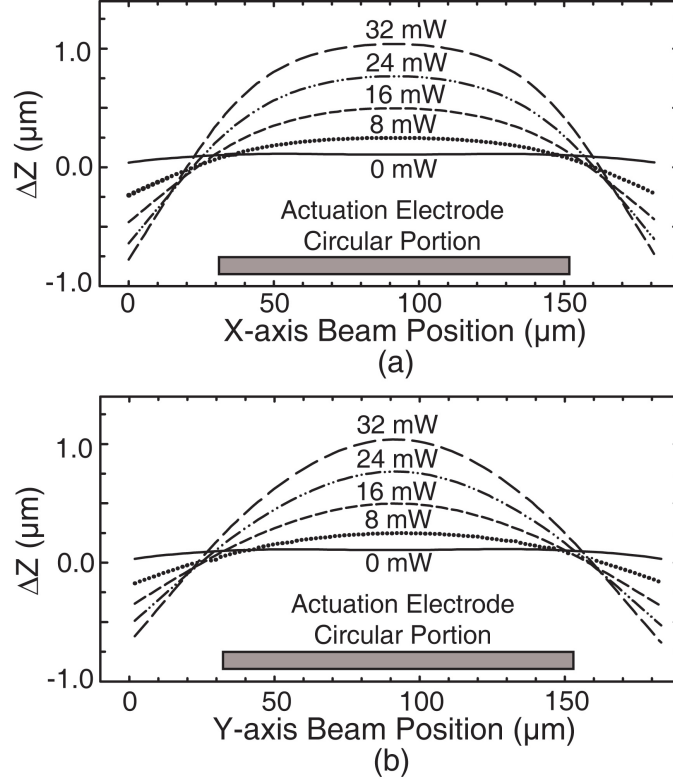
In the up-state position the peak temperature of the MEMS bridge occurs along the x-axis and is  $31.4\text{-}123.3^\circ\text{C}$  for 2-32 mW, respectively (Fig. 2.11a). The thermal conduction resistance of the suspended bridge is  $R_{cond} = \Delta T/Q = 3070^\circ\text{C/W}$ , where



**Figure 2.11:** Simulated temperature distribution of the circular beam versus dissipated power in the up-state position along the x-axis (a), y-axis (b) and in the down-state position (c), all with  $T_{ambient} = 25^\circ\text{C}$ , and  $T_{anchors}$  fixed at  $25^\circ\text{C}$ .

$\Delta T$  is the temperature difference between the peak location and the initial ambient temperature ( $^\circ\text{C}$ ), and  $Q$  is the rate of heat transfer (W). The thermal time constant of the beam is  $\tau = V\rho CR_{cond} = 106.2 \mu\text{s}$ , where  $V$ ,  $\rho$ , and  $C$  are the volume, density, and specific heat of the suspended aluminum beam. When the switch is in the down-state position, the areas of the beam which are in contact with the  $0.28 \mu\text{m}$  silicon nitride and

0.5  $\mu\text{m}$  gold bottom electrode remain at  $\sim T = 25^\circ\text{C}$ , while the peak temperature occurs in the elevated switch springs on the input side of the beam, which is  $T = 48.6^\circ\text{C}$ , for  $P_d = 50 \text{ mW}$  ( $P_{in} = 4.37 \text{ W}$ ). The shorter length of the conduction path in the down-state position results in  $R_{cond} = 472^\circ\text{C/W}$ .

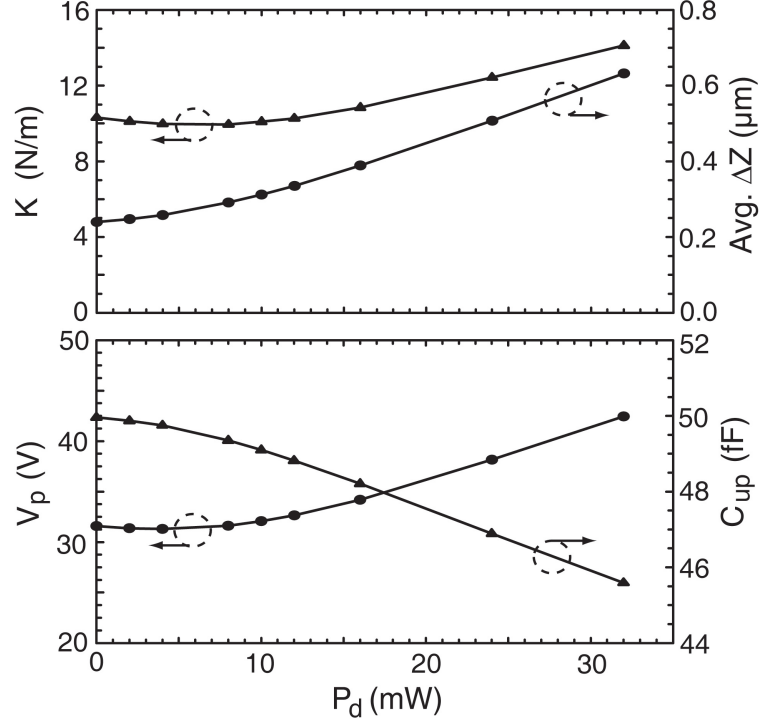


**Figure 2.12:** Simulated change in z-displacement versus power dissipated in the bridge: (a) the x-axis, (b) y-axis, with  $\sigma_{res} = 60 \text{ MPa}$ ,  $\Delta\sigma = 10 \text{ MPa}/\mu\text{m}$ .

In the up-state position, the non-uniform temperature distribution of the beam, which occurs under RF power, causes an increase in beam curvature and nominal switch gap (Fig. 2.12). The simulated average  $\Delta Z$  of the beam above the underlying electrode is 0.25-0.63  $\mu\text{m}$  for  $P_d = 2$  to 32 mW, given  $\sigma_{res} = 60 \text{ MPa}$ , and  $\Delta\sigma = 10 \text{ MPa}/\mu\text{m}$ .

Fig. 2.13 presents the simulated  $K$  and average  $\Delta Z$  above the circular portion of the actuation electrode versus dissipated power in the bridge. For  $P_d = 0$ -8 mW  $K$  decreases from 10.3 to 9.95 N/m primarily from thermally induced stress changes in the beam while above 8 mW the rising beam curvature leads to a linearly increasing spring constant from 9.95 to 14.1 N/m for  $P_d = 8$ -32 mW. Given  $K$  and the average  $\Delta Z$ ,  $V_p$  and  $C_{up}$  are calculated assuming  $g_0 = 3.9 \mu\text{m}$  (pre-release) (Fig. 2.13). The up-state

capacitance varies from 50-45.5 fF while the pull-in voltage increases from 31.6-42.5 V for  $P_d = 0-32$  mW.



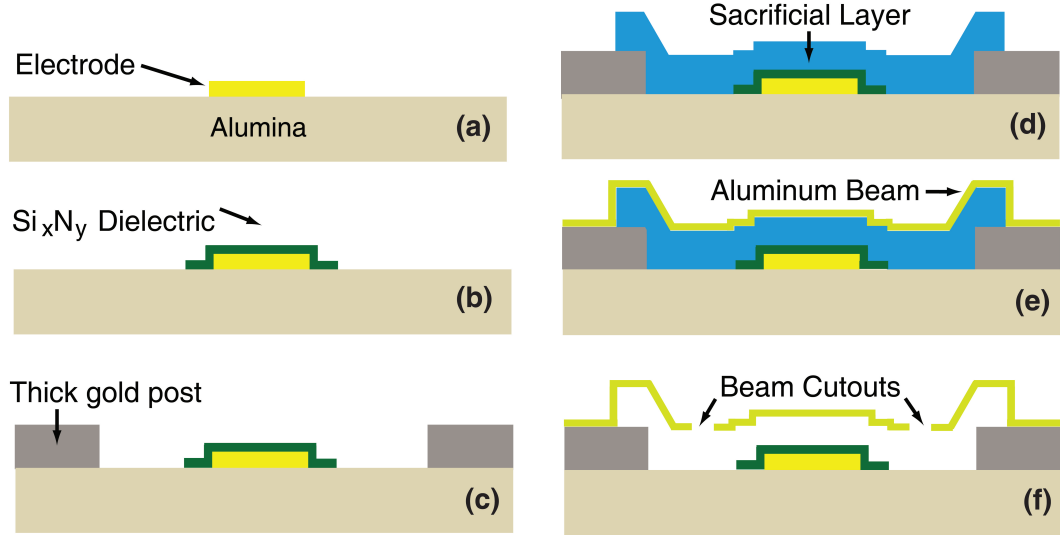
**Figure 2.13:** Simulated spring constant and average change in z-displacement above the actuation electrode as a function of dissipated power in the bridge with  $\sigma_{res} = 60$  MPa, and  $\Delta\sigma = 10$  MPa/ $\mu\text{m}$ , and calculated up-state capacitance and pull-in voltage.

When the circular switch is in the up-state position and passing continuous RF power, the beam is heated non-uniformly which leads to an increase in curvature that results in a stiffer beam and larger nominal gap. This combination produces an increasing  $V_p$  versus dissipated power in the bridge. This implies that the circular switch should not self-actuate under RF power which is in contrast to standard rectangular RF MEMS capacitive switches which show marked sensitivity of  $V_p$  versus RF power [28], [43], [44].

## 2.6 Fabrication

The circular switched capacitor is fabricated on a 4", 254  $\mu\text{m}$ -thick alumina substrate ( $\epsilon_r = 9.8$ ,  $\tan\delta = 0.0001$ ) using an RF MEMS capacitive switch process developed at Raytheon Co. A 0.5  $\mu\text{m}$ -thick gold layer is first deposited and patterned to

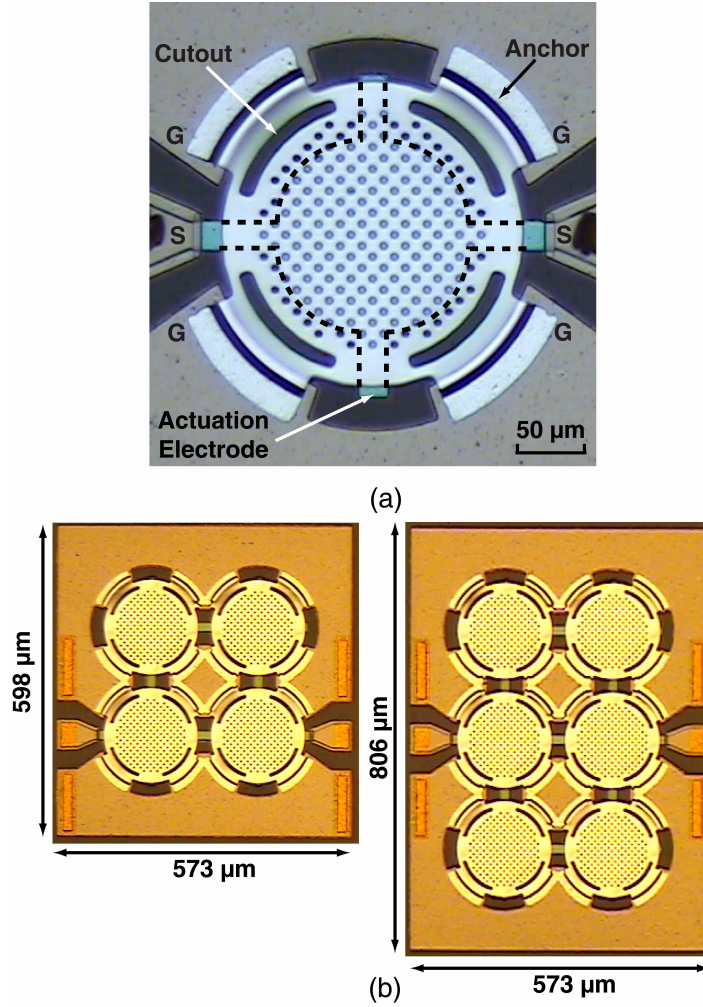
define the bottom electrode of the capacitor (Fig. 2.14a). Next a  $Si_xN_y$  dielectric is deposited and etched on top of the bottom electrode with a nominal thickness of  $\sim 0.28 \mu\text{m}$  (Fig. 2.14b). A  $3 \mu\text{m}$ -thick gold layer is next patterned to create the support posts for the suspended membrane and to reduce conductor losses in the transmission lines (Fig. 2.14c). Next the  $0.5 \mu\text{m}$ -thick aluminum beam layer is deposited on top of a thick sacrificial layer which is later removed with surface micromachining to release the suspended membrane (Fig. 2.14(d-f)). A micrograph of both the single circular switch, 2x2 and 3x2 device arrays are shown in Fig. 2.15.



**Figure 2.14:** Fabrication process for the circular RF MEMS switched capacitor.

The beam profile was measured post-release with a white light interferometer which shows a planarity of  $< 0.3 \mu\text{m}$  across the  $184 \mu\text{m}$  diameter switch (Fig. 2.16). This device has a measured post-release gap height of  $3.9 \mu\text{m}$  in the center of the bridge and corresponding actuation voltage of 33 V, which yields an extracted spring constant of 10.75 N/m with a measured  $C_{up} = 44.5 \text{ fF}$ . The actuation voltage of 4 circular switches located at each respective edge of the 4" alumina wafer ranged from 31-35 V at room temperature. Test structures were included on the mask to independently measure the resulting in-plane bi-axial stress and vertical stress gradient but did not yield useful data due to an incomplete release process. However, based on the measured switch profile and extracted spring constant, the estimated stress gradient for this fabrication run is  $\sim 10\text{-}20 \text{ MPa}/\mu\text{m}$ .



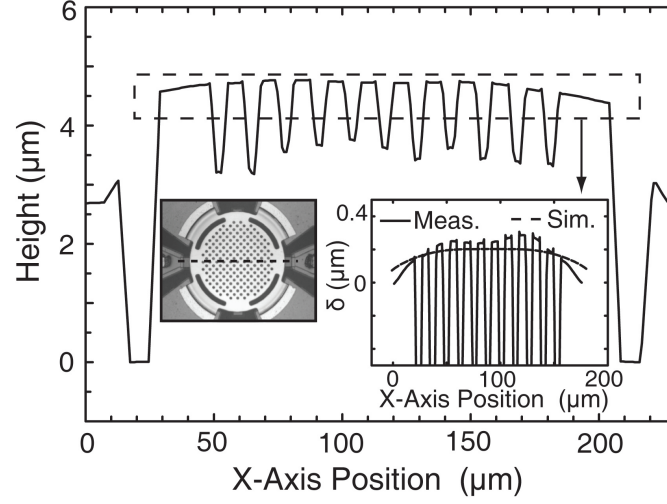


**Figure 2.15:** Micrograph of the circular RF MEMS switched capacitor (a), and the 2x2 and 3x2 arrays (b).

## 2.7 Measurements

### 2.7.1 RF Measurements

All S-parameter measurements were performed on a Cascade probe station equipped with a thermal chuck and microchamber with flowing nitrogen. The devices were initially baked at 120°C for 10 minutes to remove any surface moisture. A unipolar DC voltage is applied between the ground and signal electrodes to actuate the switches. At room temperature, the shunt switch has  $< 0.3$  dB insertion loss with  $> 14$  dB return loss up to 30 GHz (Fig. 2.17(top)). Most of the insertion loss at 30 GHz is from the reflection coefficient  $(1 - |\Gamma|^2)$  and is due to  $C_{up} = 45\text{-}50$  fF. In real applications, the



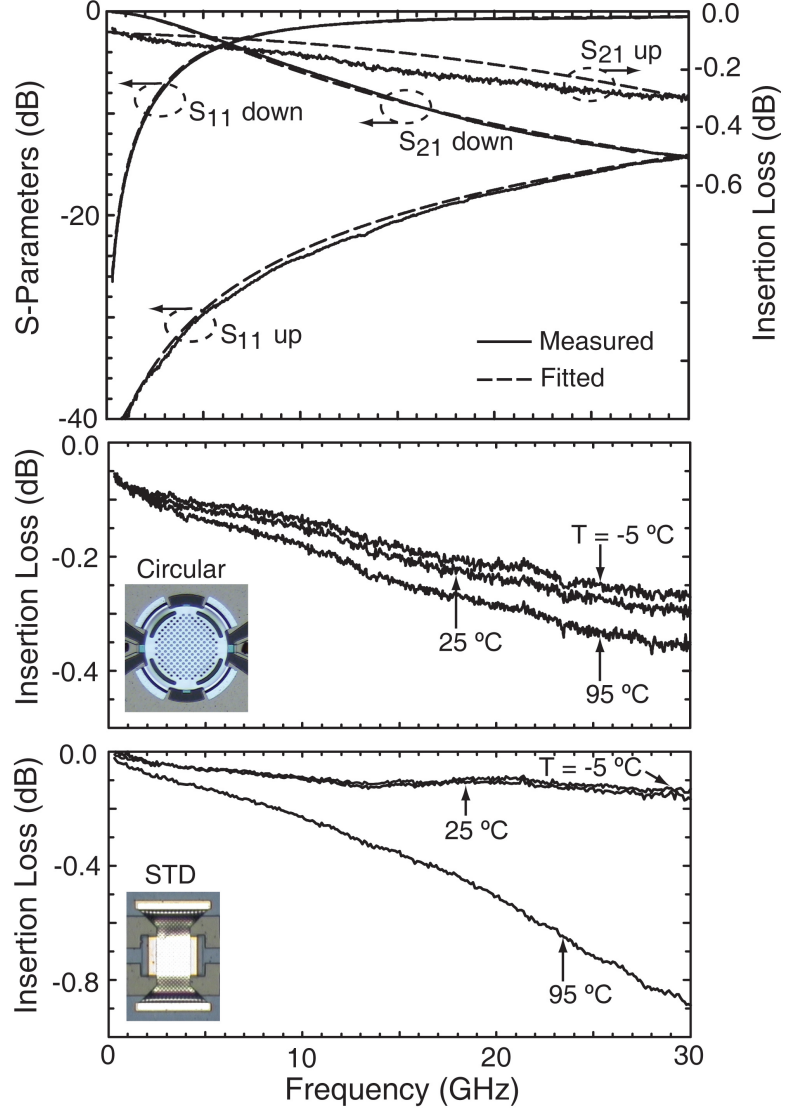
**Figure 2.16:** Measured switched capacitor profile taken post-release with a white light interferometer. Inset shows measured and simulated beam profiles with ( $\sigma_{avg} = 60$  MPa,  $\Delta\sigma = 10$  MPa/ $\mu\text{m}$ ).

insertion loss can be reduced with an input and output inductive matching section.

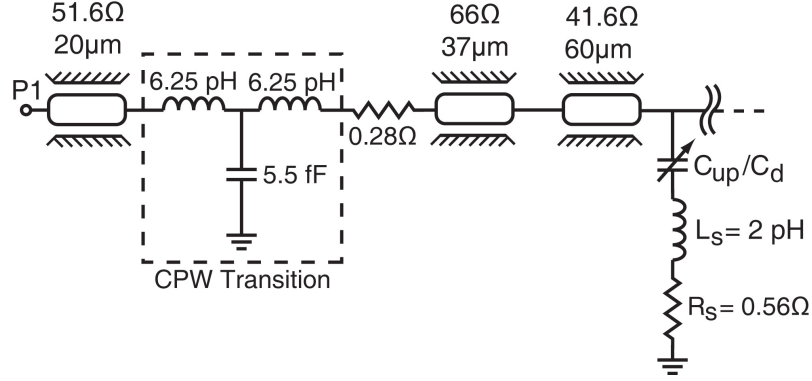
The up-and-down state capacitance, inductance and resistance of the switch were extracted from fitting the equivalent circuit model (Fig. 2.18) to the measured S-parameters (Fig. 2.17(top)). At room temperature  $C_u = 45$  fF and  $C_d = 1.05$  pF, respectively ( $C_r = 23.3$ ). The bridge inductance and resistance are extracted in the down-state and are  $L_s = 2$  pH, and  $R_s = 0.56$   $\Omega$ , respectively. The inductance is much lower than a rectangular bridge with  $L_s = 8$ -10 pH [1].

The measured insertion loss of the circular switch at 30 GHz increases from 0.27-0.38 dB for ambient temperatures from -5-95°C, respectively (Fig. 2.17(middle)). This variation is due to an increase in the up-state bridge capacitance  $C_{up}$  from 43-51 fF from -5-95°C (Note:  $C_{up} = 45$  fF at 25°C). Therefore, the nominal up-state capacitance decreases for  $T < T_o$  and increases for  $T > T_o$ . This measurement agrees well with the temperature simulations presented in Section 2.2.4, which predict that the topography and bending moments in the beam will result in upward beam displacement for  $T < T_o$ , and downward for  $T > T_o$ . The measured down-state capacitance did not change across the 100°C temperature range. Also, after several temperature cycles, the switches showed no change in either actuation voltage or up-state capacitance from the initial measurements.

The insertion loss of standard Raytheon capacitive shunt switches [45] that



**Figure 2.17:** Measured and fitted S-parameters for both circular switch states at 25°C (top), and insertion loss of the circular switch (middle), and standard Raytheon capacitive switch (bottom) at  $T = -5^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$ , and  $95^{\circ}\text{C}$ . (Fitted S-parameters use circuit model in Fig. 2.18 with  $C_{up} = 45 \text{ fF}$ ,  $C_d = 1.05 \text{ pF}$ ,  $R_s = 0.56 \Omega$ , and  $L_s = 2 \text{ pH}$ )



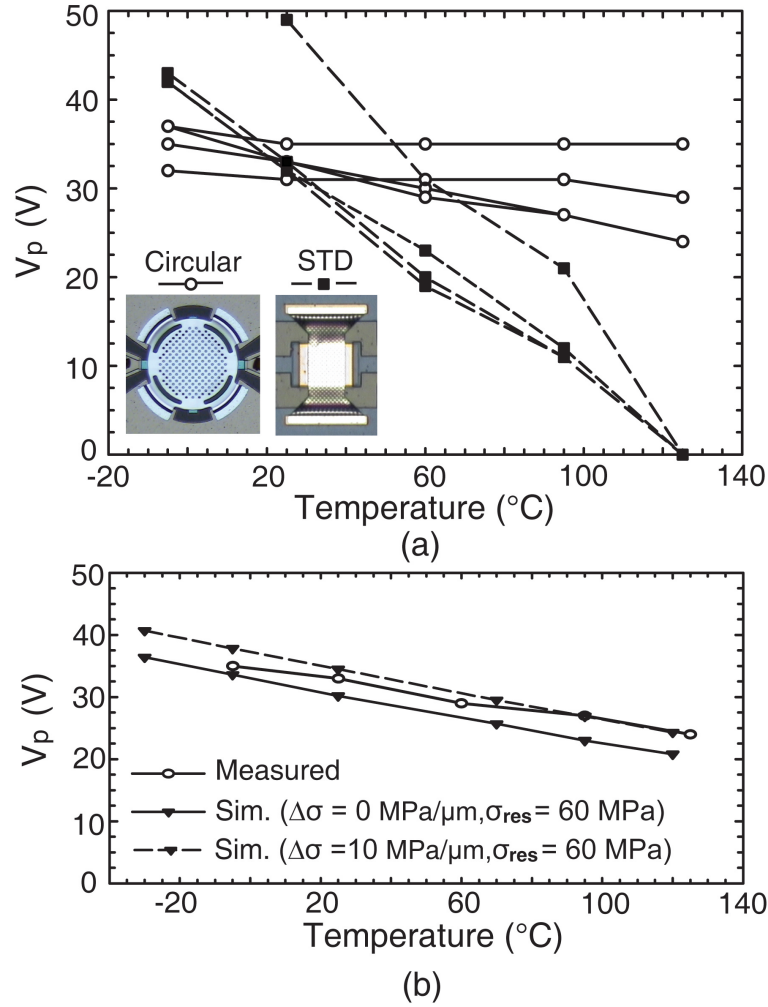
**Figure 2.18:** Half of the equivalent circuit model of the symmetric 2-port switched capacitor.

were fabricated on the same wafer were also measured from  $-5$  to  $95$   $^{\circ}\text{C}$  for comparison (Fig. 2.17(bottom)). The standard switches are about  $120$   $\mu\text{m}$  in width and  $320$   $\mu\text{m}$  in length, and are patterned on top of an  $\sim 45$   $\Omega$  CPW line with the top-view shown in Fig. 2.17(bottom). It should be noted, that the beam of the standard switch is also non-planar since the fabrication process is identical for both circular and standard designs. The measured insertion loss of the standard device at  $30$  GHz increases from  $0.131$  to  $0.889$  dB from  $-5$  to  $95$   $^{\circ}\text{C}$ , and is due to an increase in the bridge capacitance that is the result of the topography in the MEMS beam. It should be noted that at  $95$   $^{\circ}\text{C}$  the standard device shown in Fig. 2.18(bottom) is still operation with  $V_p = 12$  V despite the high insertion loss.

### 2.7.2 Pull-in Voltage vs. Temperature

To demonstrate the temperature robustness of the circular switch, the pull-in voltage was measured from  $-5$  to  $125$   $^{\circ}\text{C}$  for four devices located at each respective edge of the  $4''$  wafer (Fig. 2.19a). Standard Raytheon capacitive switches located near each circular switch were also measured for comparison. The average pull-in voltage slope versus temperature for the circular switch is  $-55$  mV/ $^{\circ}\text{C}$  with a range of  $-15$  to  $-100$  mV/ $^{\circ}\text{C}$  for the four measured devices. The variation in device pull-in voltage over temperature is influenced by the resulting beam topography (see Section 2.2.2) which is affected by fabrication tolerances. Some of the variation may also be due to differing vertical stress gradients across the wafer, but more devices need to be tested in order to confirm this. The standard Raytheon switches had an average pull-in voltage slope of  $-310$  mV/ $^{\circ}\text{C}$ , with  $V_p = 33$  V at  $25^{\circ}\text{C}$ . All of the standard switches buckled and

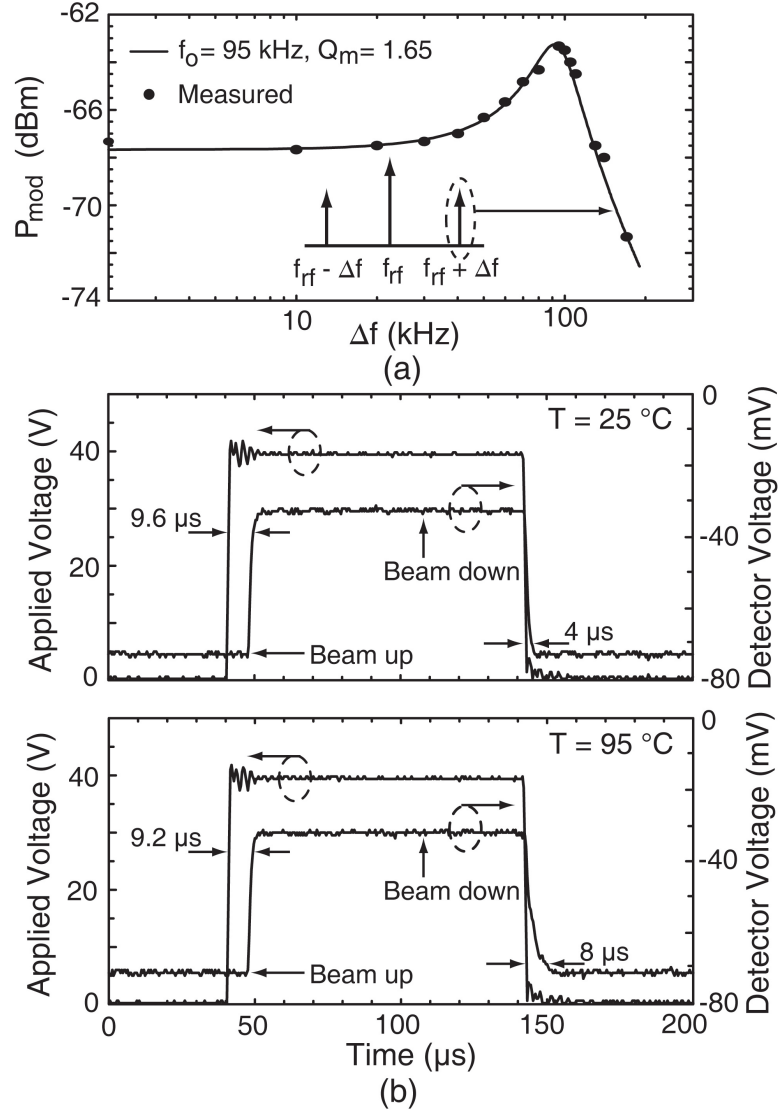
were non-operational at 125°C, while the circular switches maintained a pull-in voltage between 24-35 V.



**Figure 2.19:** Measured pull-in voltage for both standard and circular devices versus temperature for 4 die located across a 4" wafer (a), and measured vs. simulated pull-in voltage versus temperature.

Fig. 2.19b presents the simulated pull-in voltage versus temperature with  $\sigma_{\text{avg}} = 60$  MPa,  $\Delta\sigma = 0$  and 10 MPa/ $\mu\text{m}$ , and  $g_0 = 3.9 \mu\text{m}$  at 25°C. This nominal gap height is selected to match the measured device shown in Fig. 2.16 and 2.17. Simulations predict a voltage slope of -110 mV/°C for the two separate cases (i.e.  $\Delta\sigma = 0$  and 10 MPa/ $\mu\text{m}$ ) which fits well with the measured value of -100 mV/°C for this particular device.





**Figure 2.21:** Measured switching speed at  $25^\circ\text{C}$  and  $95^\circ\text{C}$  (a), and the measured and fitted mechanical resonance frequency of the circular switched capacitor (b).

assuming a nitrogen gas with a mean free path of  $\lambda = 0.061 \mu\text{m}$ ,  $T = 300^\circ\text{K}$ , and  $p = 101$  kPa. For a gap height of  $g_0 = 3.9 \mu\text{m}$ , the simulated damping coefficient is  $1.152 \times 10^{-5}$  N/(m/s) which shows good agreement with the extracted value.

The measured switching time at  $25^\circ\text{C}$  from up-to-down state is  $9.6 \mu\text{s}$  with a release time of  $4 \mu\text{s}$  for a device with  $V_p = 33$  V,  $g_0 = 3.9 \mu\text{m}$ , and  $V_{\text{applied}} = 40$  V (Fig. 2.21b). At  $95^\circ\text{C}$ , the switching time from up-to-down and down-to-up are  $9.2$  and  $8 \mu\text{s}$ , respectively (Fig. 2.21b). At  $95^\circ\text{C}$ , the switching time from up-to-down is reduced due to a lower spring constant and nominal switch gap, while the release time increases as a

**Table 2.3:** Switched Capacitor Measurements.

	$C_{up}$ (fF)	$C_d$ (pF)	$R_{se}$ ( $\Omega$ )	$Q_d$ ( $Z_d = -j50\Omega$ )	Freq. (MHz)
1x1	51	1.00	0.56	84.8	3127
2x2	305*	3.95	1	50	806
3x2	450*	5.89	0.85	58.8	541

\* Includes all parasitics between input and output ports

result of the lower release force given by  $F_r = Kg_0$ .

#### 2.7.4 Switch Array Measurements

Two-port 2x2 and 3x2 CPW implemented shunt switched-capacitor arrays, such as the ones shown in Fig. 2.16b, were measured from 300 MHz to 10 GHz. The measured up-state insertion loss at 10 GHz is -0.91 and -1.64 dB, while the down-state isolation with  $V_p = 34$  V is -16.0 and -19.3 dB for the 2x2 and 3x2 arrays, respectively (Fig. 2.22a). Fig. 2.22b presents the equivalent circuit model for the switched capacitor arrays which is fitted to the measured S-parameters (Fig. 2.22a). The measured capacitance of the 2x2 and 3x2 arrays are  $C_{up} = 305$  fF, 450 fF and  $C_d = 3.95$  pF, 5.89 pF, respectively.

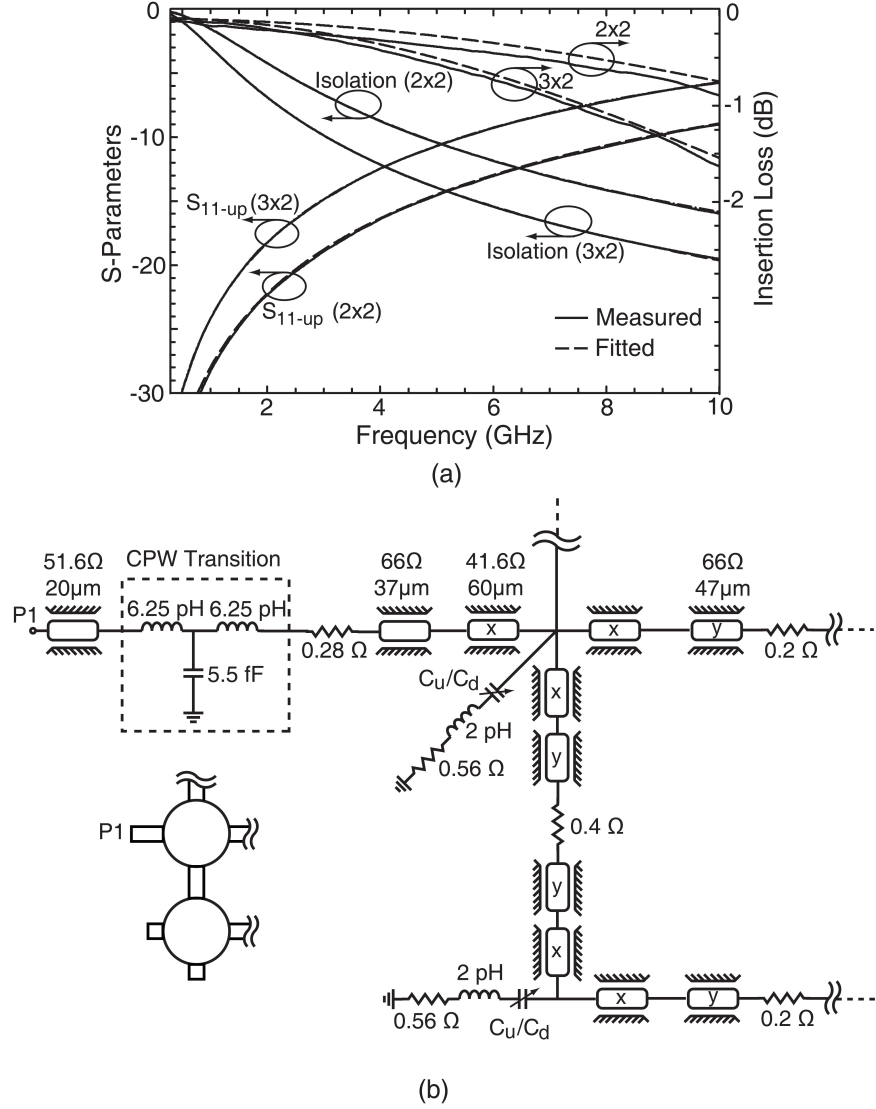
The measured down-state switch impedance of the single device, 2x2, and 3x2 arrays were extracted from the measured S-parameters and plotted with the ideal down-state impedance ( $Z_{ideal} = 1/j\omega C_d$ ) (Fig. 2.23a). The 2x2 and 3x2 arrays ( $C_d = 3.95$ , 5.89 pF) result in an impedance of 135-4  $\Omega$  and 91-3  $\Omega$  at 0.3-10 GHz, respectively. These devices act as near-ideal capacitors over a 33:1 frequency range due to the low-series-inductance.

The quality factor of the 2-port switched capacitor is

$$Q = \frac{|imag(Z_{12})|}{real(Z_{12})} \quad (2.9)$$

where  $Z_{12}$  is calculated from the measured S-parameters. Fig. 2.23b presents the measured down-state quality factor ( $Q_d$ ) which appears “noisy” at the lower frequencies due to the high device impedance. In order to extract an accurate quality factor at the lower frequencies, the equivalent resistance and capacitance are extracted directly from the measured S-parameters and used in  $Q_d = 1/(\omega R_{se} C_d)$  (dashed line in Fig. 2.23b). The down-state quality factor is specified at the frequency where  $Z_d = -j50 \Omega$  and is summarized in Table 6.2 along with the extracted  $R_{se}$  and  $C_d$  values. The down-state quality factor of the 3x2 array is 58.8 compared to 50 for the 2x2 array due to the additional



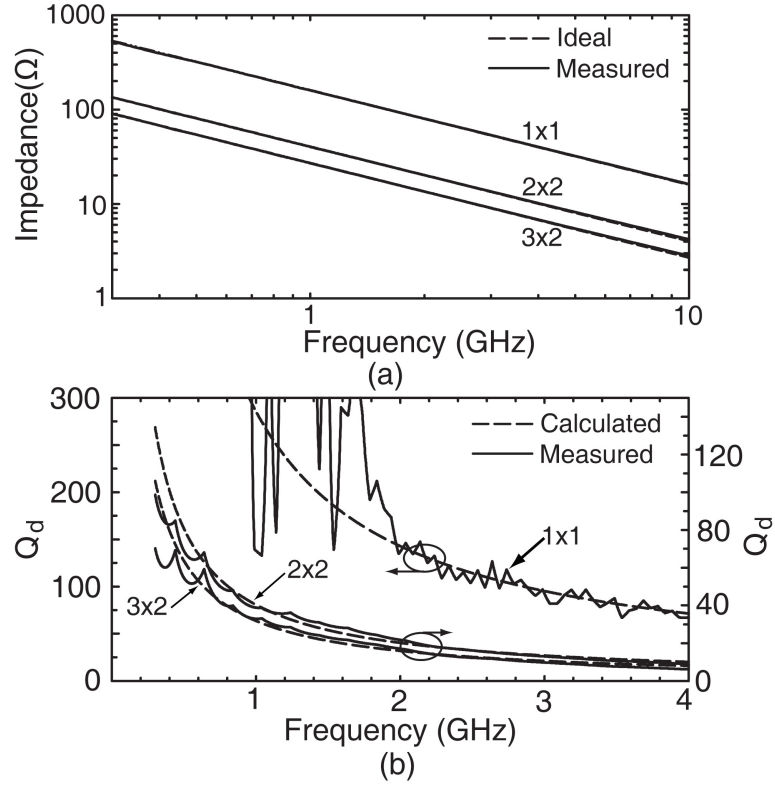


**Figure 2.22:** Measured and fitted S-parameters for both the 2x2 and 3x2 arrays (a), and equivalent circuit model for an NxM array.

parallel connection and lower  $R_{se}$ . The calculated quality factor of the switch arrays in the up-state is  $> 1000$  at 806 MHz and 541 MHz for the 2x2 and 3x2 arrays, and cannot be measured accurately via S-parameters.

### 2.7.5 Power Handling Measurements

The power handling of the RF MEMS shunt switched capacitor was measured at room temperature under continuous RF power at  $f_0 = 10$  GHz using the measurement setup shown in Fig. 2.24. The RF power supplied to the DUT was gradually increased,

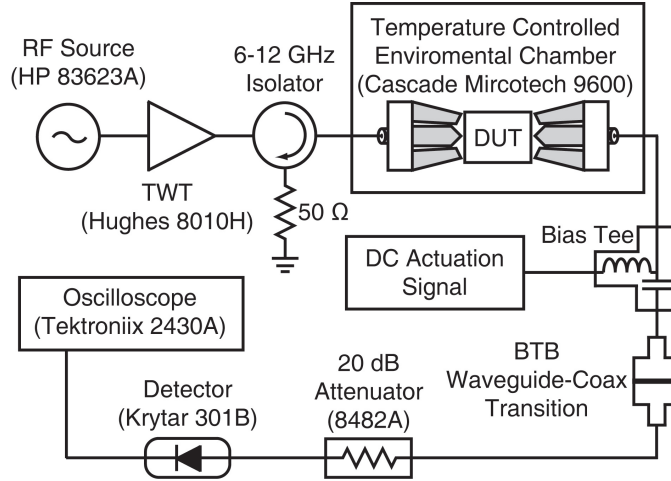


**Figure 2.23:** Measured and ideal down-state switch impedance(a), and measured and calculated down-state quality factor (b)

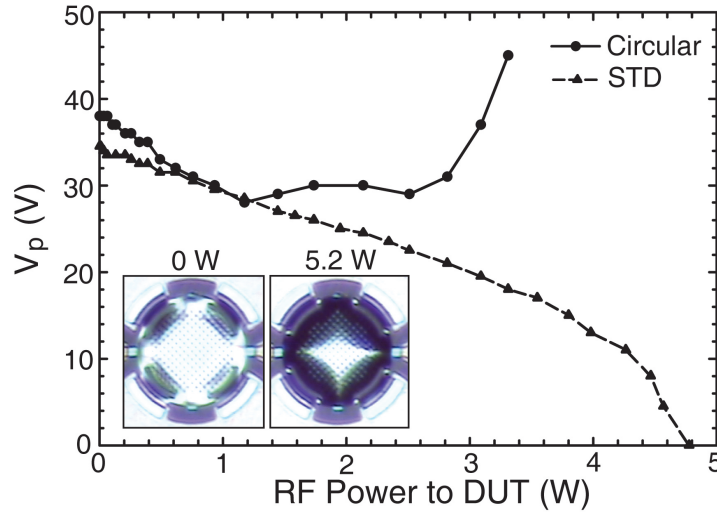
and at each power level the switch pull-in voltage was recorded. If the switch failed to release once the DC bias was removed the RF power was gradually lowered until the switch returned to its initial position. With this test setup a maximum power of 5.2 W was available at the device while the DC supply voltage was limited to 50 V.

The measured pull-in voltage as a function of RF power level is shown in Fig. 2.25 for both the standard Raytheon and circular RF MEMS switched capacitors. A total of 10 circular switches and 2 Raytheon devices were tested under RF power and the data shown in Fig. 2.25 is representative of the devices tested. The actuation voltage of the circular switch decreases linearly from 38-28 V for power levels from up to 1.2 W, before remaining relatively constant up to 2.5 W. Above 2.5 W the switch pull-in voltage increases rapidly and is  $> 50$  V for power levels  $> 3.5$  W.

Self-actuation of the circular MEMS switches did not occur for power levels up to the maximum available of 5.2 W. However, under hot switching conditions a power level  $\geq 1.38$  W was sufficient to cause “latching” of the switch from the effective  $V_{rms}$ .



**Figure 2.24:** Power handling measurement setup.



**Figure 2.25:** Measured pull-in voltage versus continuous RF power ( $f_0 = 10$  GHz) for both the standard Raytheon and circular RF MEMS shunt capacitive switches. Micrographs of the circular switch taken at 0 and 5.2 W.

For the standard Raytheon device, the pull-in voltage decreased linearly from 35 V until self-actuation occurred at 4.77 W. Fig. 2.25 also presents micrographs of the circular MEMS switch under incident RF power levels of 0 and 5.2 W, which clearly shows the curvature of the beam at 5.2 W. The experimental data is in good agreement with the simulations presented in Fig. 2.13.

## 2.8 Summary

This chapter presents a new design of a thin-film RF MEMS capacitive switch with improved tolerance to bi-axial stress and temperature variations. The design procedure shows that there is a trade-off between sensitivity to bi-axial stress and displacements arising from vertical stress gradients. This work also shows that the device topography has a strong effect on both the initial beam position and displacement versus temperature and cannot be neglected. The circular MEMS switch also results in low-series-inductance NxM arrays which lead to very large switched capacitors for 300 MHz to 10 GHz applications. The switch is tested under continuous RF power at 10 GHz and both simulations and measurements show that the non-uniform temperature distribution of the bridge under RF power causes a decreasing up-state bridge capacitance and an increasing spring constant. This combination results in a switch that does not suffer from self-actuation up to RF power levels of 5.2 W.

Chapter 2 is mostly a reprint of the material as it appears in IEEE Journal Microelectromechanical Systems, 2010. Isak Reines, Brandon Pillans, and Gabriel M. Rebeiz. The dissertation author was the primary author of this material. This chapter also includes material published in IEEE MTT-S Int. Microwave Symposium, 2010. Isak Reines, Brandon Pillans; and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

# Chapter 3

## Second Generation of Temperature-Stable Stress-Tolerant Capacitive Switches in the Raytheon RF MEMS Process

### 3.1 Introduction

In this chapter, we present the measurements of the second generation of stress-tolerant and temperature-stable RF MEMS switched capacitors that are designed and fabricated within the Raytheon RF MEMS process. The primary goal of these designs is to improve the impedance match and to reduce the insertion loss of the CPW-implemented shunt switch capacitor presented in Chapter 2. A smaller design is also included to investigate the scalability of the circular switch for higher frequency applications. Four switch designs are presented, two of which are slight variants of the baseline design from Chapter 2, and the other 2 with reduced dimensions and lower capacitances. All of the switches are placed in the standard Raytheon 2-port CPW test structure with additional matching inductors located on either side of the device to improve the impedance match.

## 3.2 Device Design Variations

Table 3.1 presents the particular layout dimensions which differ from the baseline design presented in Chapter 2. Unlike the baseline switch, these designs have 17 additional  $2 \times 2 \mu\text{m}$  size release holes which are placed in the anchors areas to assure a repeatable and complete removal of the photo-resist sacrificial layer during the dry release process. It should be noted that all other switch dimensions are identical to those presented in Chapter 2 (Table 2.1).

**Table 3.1:** Second Generation Temperature-Stable RF MEMS Capacitive Switch Dimensions.

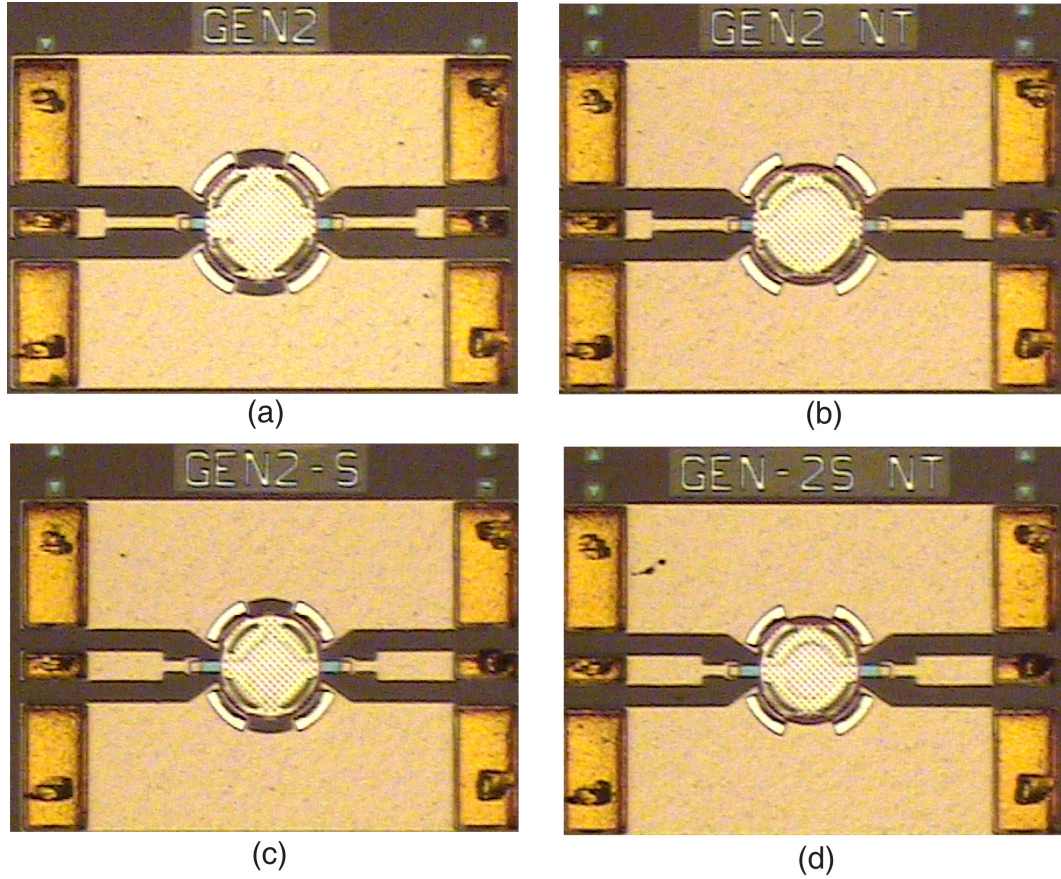
<i>Design</i>	$r_b$ ( $\mu\text{m}$ )	$r_a$ ( $\mu\text{m}$ )	<i>Actuation Tabs</i>
Gen2	92	60	Y
Gen2-NT	92	60	N
Gen2-S	82	45	Y
Gen2-S-NT	82	45	N

As mentioned in Chapter 2, the bottom electrode of the switched capacitor is shaped like a cross-hair in order to provide symmetric actuation and to facilitate arraying of the devices. Inclusion of the symmetric “actuation tabs” on the “north” and “south” side of the bottom electrode requires that a section of the CPW ground plane is removed to keep a minimum spacing. This increases the device loss since the RF current path along the ground plane becomes longer. As shown in Table 3.1, designs splits have been included for both switch sizes to study the effects of removing the “actuation tabs” on the device performance. Figure 3.1 presents the micrographs of the four design variations.

## 3.3 Measurements

### 3.3.1 Pull-in Voltage vs. Temperature

The pull-in voltage of four switches of each design type was measured versus ambient temperature from  $-5$  to  $95^\circ\text{C}$  in a microchamber with flowing nitrogen (Fig. 3.2). Standard Raytheon switches located near each circular switch were also measured for comparison and a summary of the average pull-in voltage slopes is presented in Table 3.2. All of the circular design variants demonstrated a high robustness to ambient temperature with pull-in voltage slopes ranging from only  $-22$  to  $-36 \text{ mV}/^\circ\text{C}$ , compared to  $-225.1 \text{ mV}/^\circ\text{C}$  for the standard Raytheon switch. In both design splits, the pull-in volt-

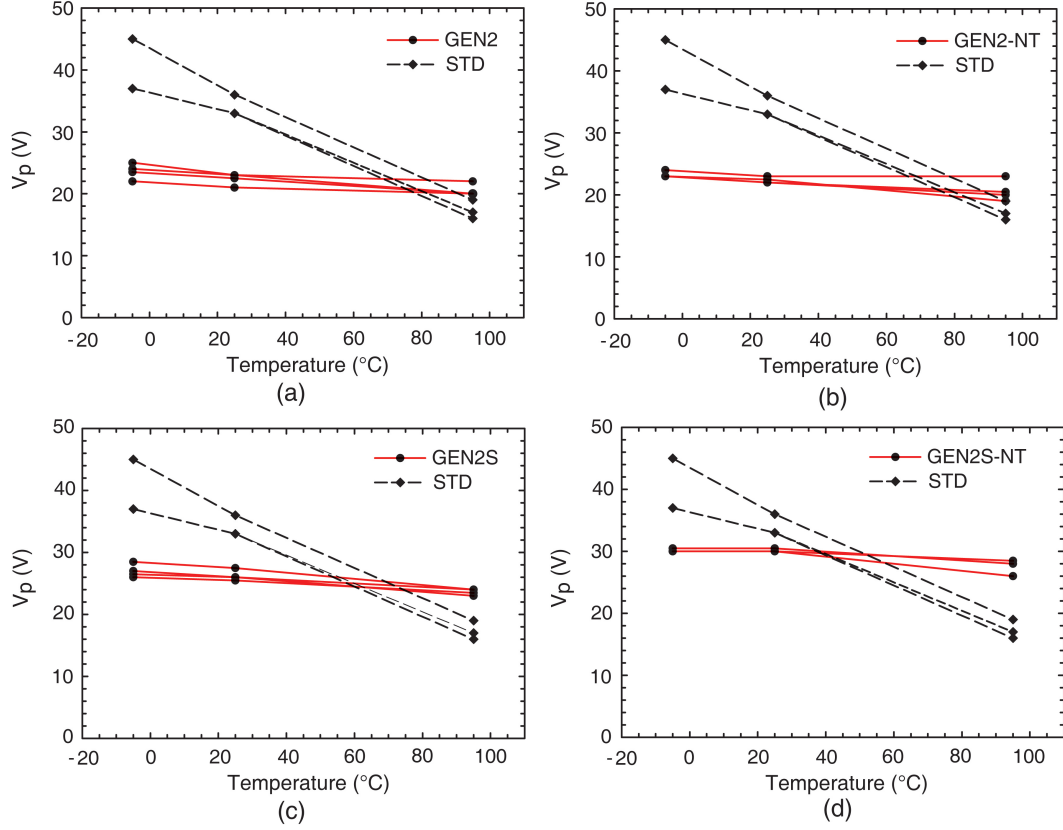


**Figure 3.1:** Micrograph of the Gen2 (a), Gen2-NT (b), Gen2-S, and Gen2-S-NT (d) RF MEMS switched capacitor design variations.

age slope is lower for the designs without the symmetric “actuation tabs” (i.e. designs Gen2-NT, Gen2S-NT), which can be explained by the fact that the change in the gap height versus temperature is larger in the area above the “actuation tabs” compared to in the center of the beam as shown in Chapter 2 (Fig. 2.8 with  $\sigma_{avg} = 60$  MPa, and  $\Delta\sigma = 5$  MPa/ $\mu\text{m}$ ). Therefore, by removing the tabs, a more stable pull-in voltage versus temperature can be achieved.

### 3.3.2 RF Measurements

S-parameters were measured from 0.1-40 GHz in both the up-and-down state positions and versus ambient temperature with each curve in Fig. 3.3 representing the average of four measured switches. At room temperature the circular Gen2 design has  $< 0.5$  dB of insertion loss and  $> 14$  dB of return loss up to 40 GHz with  $C_{up} = 44$  fF (Fig.



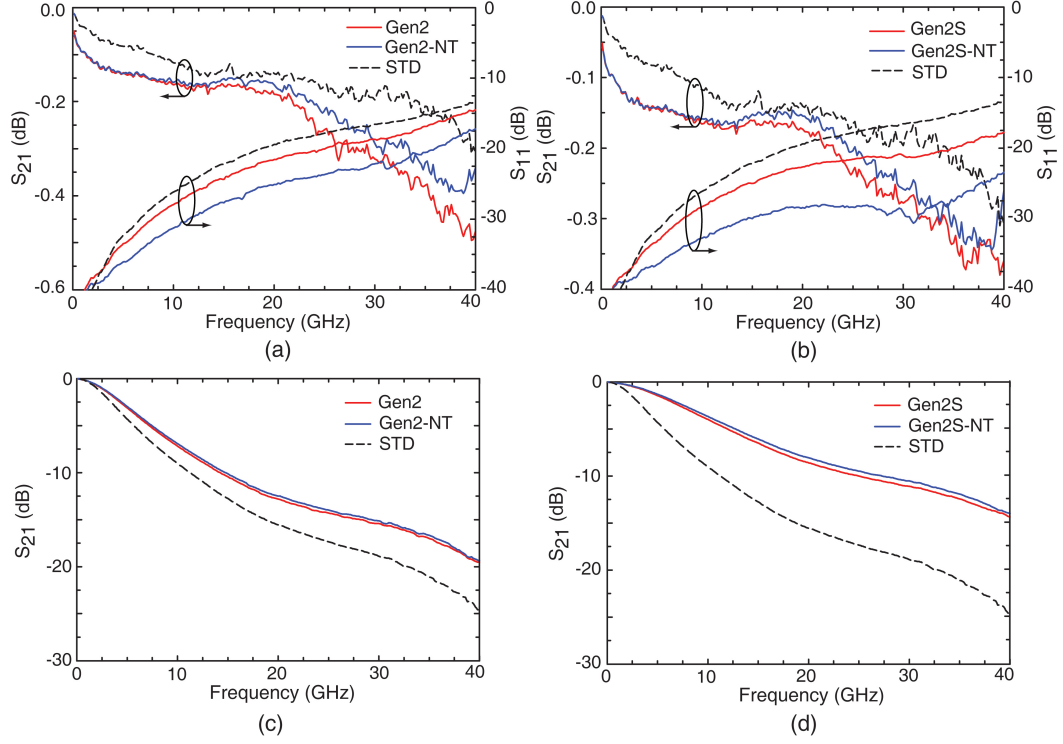
**Figure 3.2:** Measured pull-in voltage vs. temperature of the (a) Gen2, (b) Gen2-NT, (c) Gen2-S, and (d) Gen2-S-NT RF MEMS switched capacitors.

**Table 3.2:** Average pull-in voltage slope vs. temperature.

<i>Design</i>	$V_p$ Slope ( $mV/^{\circ}C$ )
Gen2	-29.6
Gen2-NT	-22
Gen2-S	-35.8
Gen2-S-NT	-28.7
Standard	-225.1

3.3a). The Gen2-NT switch has 10 fF less fixed parasitic capacitance with  $C_{up} = 39$  fF, resulting in  $< 0.33$  dB of insertion loss and  $> 16.6$  dB of return loss up to 40 GHz. The standard Raytheon switch with  $C_{up} = 39$  fF has  $< 0.31$  dB of insertion loss and  $> 13.6$  dB of return loss up to 40 GHz. In the down-state position with  $V_{bias} = 40$  V, the Gen2 and Gen2-NT designs have  $\sim 19$  dB of isolation at 40 GHz, while the standard switch has  $\sim 25$  dB (Fig. 3.3c).





**Figure 3.3:** Measured up-state S-parameters of the (a) Gen2 and Gen2-NT designs, (b) Gen2S and Gen2S-NT, and down-state isolation for the (c) Gen2 and Gen2-NT designs, and (d) Gen2S and Gen2S-NT.

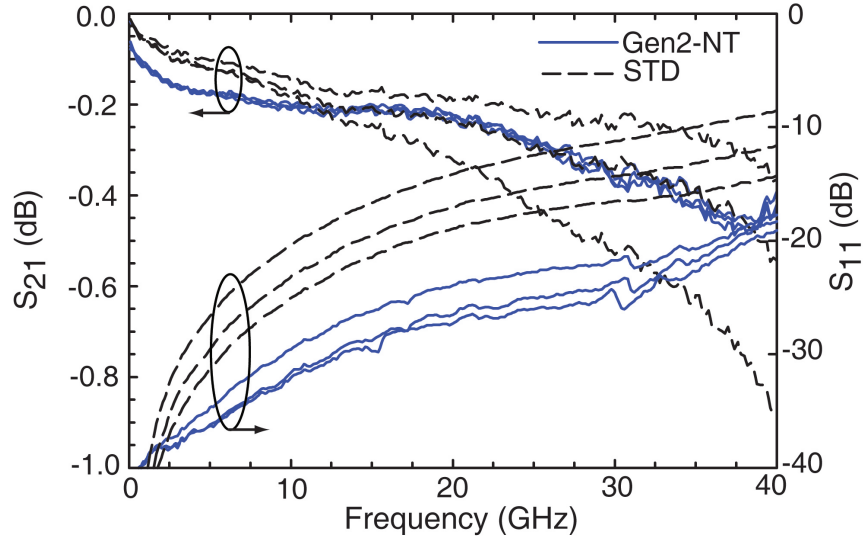
The smaller Gen2-S design with  $C_{up} = 33$  fF, has  $< 0.375$  dB of insertion loss and  $> 17$  dB of return loss up to 40 GHz (Fig. 3.3b). Without the “actuation tabs,” the smaller design has  $C_{up} = 27$  fF,  $< 0.35$  dB of insertion loss, and  $> 23$  dB of return loss up to 40 GHz. In the down-state position with  $V_{bias} = 40$  V, the smaller designs have  $\sim 14$  dB of isolation at 40 GHz (Fig. 3.3d). The extracted up-and-down state capacitances and capacitance ratios for all design variants are summarized in Table 3.3.

**Table 3.3:** Generation2 Raytheon RF MEMS Switch Capacitance Values.

<i>Design</i>	$C_{up}$ (fF)	$C_d$ (pF)	$C_r$
Gen2	44	1.23	28
Gen2-NT	39	1.20	30
Gen2-S	33	0.73	22
Gen2-S-NT	27	0.70	26
Standard	39	1.6	41

In the up-state position and at room temperature, the standard Raytheon ca-

capacitive switch has  $\sim 0.05$ - $0.1$  dB lower insertion loss compared to the Gen2-NT design depending on the particular frequency due to a series resistance in the transmission line of only  $0.2 \Omega$ . While the inductive matching section used in the circular designs improves the return loss, it also increases the resistance of the transmission line with  $R_{line} = 0.58 \Omega$  for the Gen2 and Gen2-NT designs. Fig. 3.4 presents the up-state S-parameters at  $95^\circ\text{C}$  for both the Gen2-NT and standard switch designs. At  $95^\circ\text{C}$ , all 3 standard switches are operational with pull-in voltages between 16-19 V, however the insertion loss of 2 of 3 of the standard switches has increased from 0.31 dB at  $25^\circ\text{C}$ , to 0.54 dB and 0.89 dB, respectively. The loss increase at  $95^\circ\text{C}$  is due to a larger up-state capacitance that results from the topography and bending moments in the standard design.



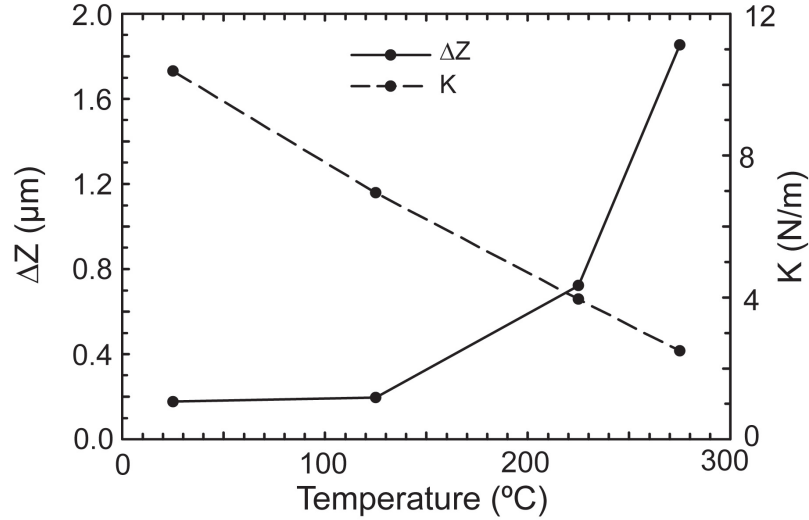
**Figure 3.4:** Measured up-state S-parameters at  $95^\circ\text{C}$  of the Gen2-NT and standard switch designs.

### 3.4 Packaging Considerations

RF MEMS capacitive switches are very sensitive to humidity and contaminants, and therefore they must be packaged in a dry nitrogen environment to facilitate reliable operation. Both thin-film encapsulation techniques [46]- [47] and wafer-to-wafer bonding [48] require packaging temperatures between  $250$ - $300^\circ\text{C}$ , which may not be compatible with the RF MEMS device. For example, plastic deformation of the MEMS beam may occur at these high temperatures which would permanently alter the device performance.

In the case of a thin-film package, where the top of the package may only be several microns from the beam, these high temperatures could cause the bridge to touch the lid of the package. In order to study the impacts of packaging, the Gen2-S design is simulated versus ambient temperatures from 25-275 °C, assuming  $\sigma_{avg} = 60$  MPa, and  $\Delta\sigma = 10$  MPa/ $\mu\text{m}$ .

Fig. 3.5 shows the change in displacement ( $\Delta Z$ ) in the center of the Gen2-S 164  $\mu\text{m}$  diameter beam, and the spring constant versus ambient temperature. From 25-275°C, the center of the beam deflects upward from 0.18-1.85  $\mu\text{m}$ , due to the topography and bending moments in the beam. Across this temperature range, the spring constant decreases from 10.4-2.5 N/m due to thermally induced stress changes in the beam. These results indicate that if thin-film encapsulation packaging techniques are to be used, that the upper lid should be placed  $>2$   $\mu\text{m}$  from the circular membrane. It is important to note, that no plastic deformation of the 0.5  $\mu\text{m}$  aluminum beam has been observed up to 300°C. These results indicate that the device can be hermetically packaged using either thin-film encapsulation or wafer-to-wafer bonding techniques.



**Figure 3.5:** Simulated change in beam displacement  $\Delta Z$  and spring constant vs. ambient temperature of the Gen2-S design from 25-275°C, assuming  $\sigma_{avg} = 60$  MPa, and  $\Delta\sigma = 10$  MPa/ $\mu\text{m}$ .

### 3.5 Summary

In this chapter we presented four temperature-stable and stress-tolerant RF MEMS switched capacitors that are fabricated in the Raytheon RF MEMS process. It has been demonstrated that the insertion loss, return loss, capacitance ratio, and temperature robustness of the circular capacitive switch can be improved without the symmetric “actuation tabs,” which should only be used when cascading the devices in  $N \times M$  arrays. The Gen2-NT device with  $C_{up} = 39$  fF and  $C_d = 1.2$  pF, has a measured pull-in voltage slope of only  $-22$  mV/ $^{\circ}\text{C}$  from  $-5^{\circ}\text{C}$ - $95^{\circ}\text{C}$  compared to  $-225.1$  mV/ $^{\circ}\text{C}$  for the standard Raytheon switch.

At  $25^{\circ}\text{C}$ , the Gen2-NT design has  $\sim 0.05$ - $0.1$  dB of additional insertion loss compared to the standard Raytheon design from  $0.1$ - $40$  GHz. However, at  $95^{\circ}\text{C}$  the Gen2-NT design has a more repeatable and lower insertion loss at  $40$  GHz compared to the standard design since the up-state capacitance is more stable versus temperature. A smaller circular design has been demonstrated with  $C_{up} = 27$  fF,  $C_d = 0.7$  pF, and a measured pull-in voltage slope versus temperature of only  $-28.7$  mV/ $^{\circ}\text{C}$  from  $-5$ - $95^{\circ}\text{C}$ . The temperature robustness of the smaller Gen2S-NT design shows the scalability of the circular design for higher frequency applications.

# Chapter 4

## Cascadable RF MEMS Switched Capacitors for 0.1-2 GHz Applications

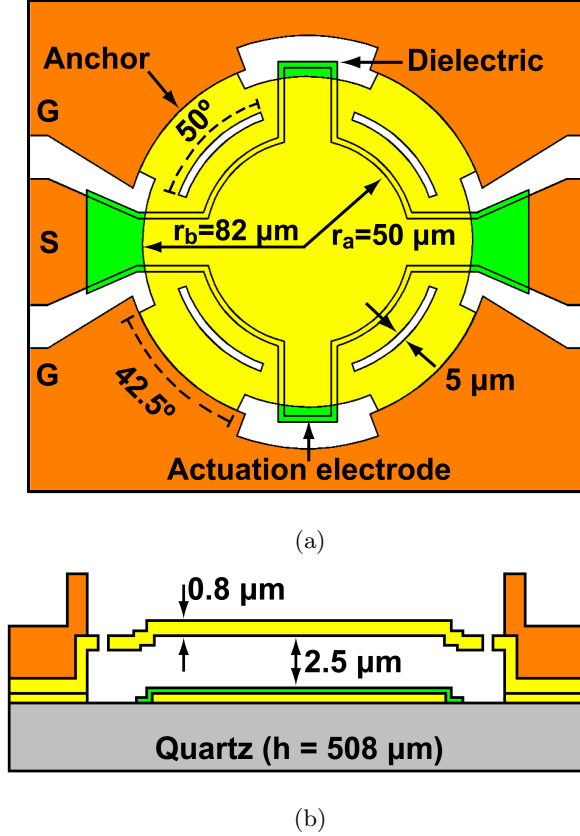
### 4.1 Introduction

RF MEMS tunable capacitors are attractive devices for reconfigurable systems due to their very linear and low-loss performance [1]. They have been used in many different RF/microwave filters and matching networks with excellent performance [49]-[22]. Commonly used rectangular fixed-fixed beam RF MEMS switches are sensitive to residual bi-axial beam stress which leads to a varying actuation voltage and up-state capacitance versus temperature, while also reducing device uniformity across the wafer and from wafer-to-wafer lots [25]. Previously, a novel RF MEMS switched capacitor based on a circular beam geometry demonstrated a pull-in voltage slope of only -50 mV/°C from -5°C to 95°C [31]. The stress-tolerant and temperature-stable circular beam design also results in low-series-inductance arrays for high value capacitive networks making them ideally suited for VHF and UHF reconfigurable applications.

### 4.2 UCSD Switch Design

The top view and cross section of a single shunt switched-capacitor are shown in Fig. 4.2. The device is based on a circular beam geometry which is anchored sym-

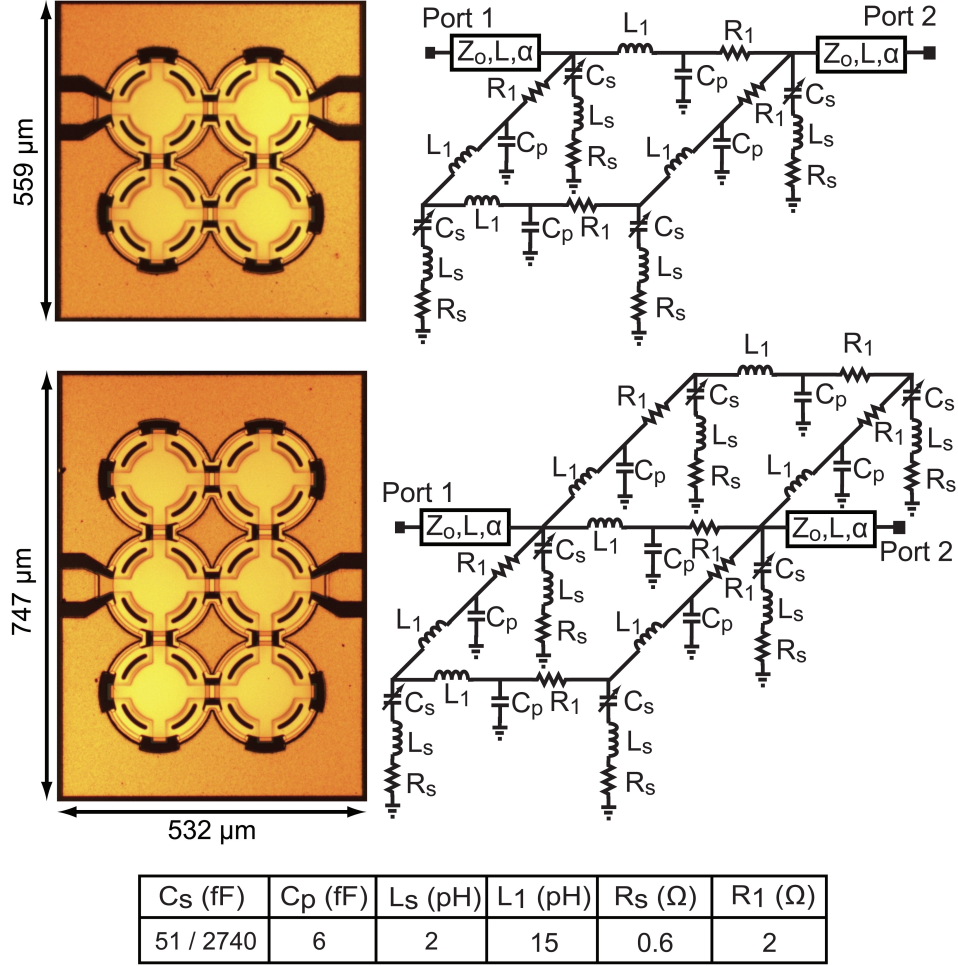
metrically in four locations. Arc-shaped cutouts are placed in the beam next to each anchor to reduce the sensitivity to residual biaxial stress and temperature. The bottom electrode of the switched capacitor is shaped as a cross-hair in order to provide symmetric actuation and to facilitate arraying of the devices. To reduce the effects of dielectric charging, the switched capacitor is actuated by supplying a 10 kHz bipolar voltage between the ground and signal electrodes.



**Figure 4.1:** Single device layout in a CPW configuration: (a) top view, (b) cross section.

Due to the complex geometry of this device, electro-mechanical simulations were performed in Coventorware [34]. The simulated spring constant, defined as the displacement in the center of the beam due to a distributed force in the area above the actuation electrode, is 42.5 N/m for a residual tensile beam stress of 100 MPa. The simulated pull-in voltage is  $V_p = 47 \text{ V}$  for a nominal gap of  $2.5 \mu\text{m}$ . The calculated up-state capacitance is 50 fF including a 30% fringing coefficient. The down-state capacitance is 2.1 pF assuming an effective permittivity of  $\epsilon_e = 3.7$  ( $0.5\epsilon_r = 7.4$  for  $\text{Si}_3\text{N}_4$ ). Modal analysis was also performed on the structure resulting in a first resonance mode at 85

kHz. The single switch cell can be arrayed to obtain larger value capacitances as shown in Fig. 4.2. This is achieved by connecting the pull-down electrodes together in both the x and y directions, while keeping the different circular beam switches mechanically separated.



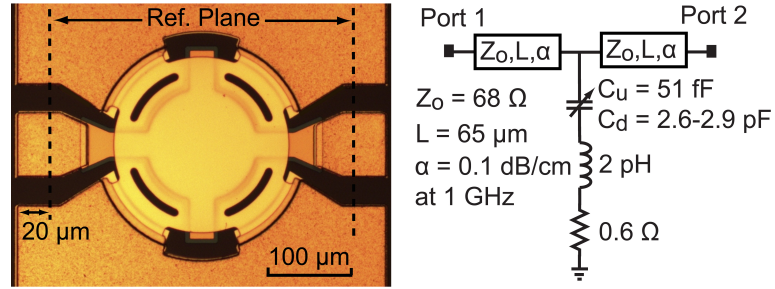
**Figure 4.2:** Two-port switched capacitor arrays and equivalent lumped-element circuit models.

### 4.3 Fabrication

The switched capacitors are fabricated on a  $508 \mu\text{m}$ -thick quartz substrate ( $\epsilon_r = 3.78$ ,  $\tan\delta = 0.0001$ ) using a standard RF MEMS capacitive switch process developed at the University of California San Diego. The bottom electrode is a sputtered layer of Ti/Au ( $200/3500 \text{ \AA}$ ). A  $1700 \text{ \AA}$  thick layer of PECVD-deposited  $\text{Si}_3\text{N}_4$  is patterned to

form the dielectric layer of the switch. PMMA with a thickness of  $2.5\ \mu\text{m}$  is deposited and patterned to define the sacrificial layer. The MEMS bridge is made from a sputtered layer of Ti/Au ( $200/8000\ \text{\AA}$ ) in which the bottom Ti layer is removed later during the release process. The transmission lines and bridge anchors are electroplated with  $1.5\ \mu\text{m}$  thick gold. Next, the bridge metal is selectively etched to define the cutouts in the beam. To release the switch, the sacrificial layer is removed in hot solvent before being dried in a  $\text{CO}_2$  super-critical point drier.

An optical picture of a fabricated device is shown in Fig. 4.3. The post release height of the MEMS bridge is  $2.5\ \mu\text{m}$  measured with a white light interferometer. The measured actuation voltage of the switch is  $V_p = 44\ \text{V}$  which yields an extracted spring constant of  $k = 45\ \text{N/m}$ .



**Figure 4.3:** Two-port shunt switched capacitor and its equivalent lumped-element circuit model.

## 4.4 Measurements

Two-port 1x1, 2x2, and 3x2 shunt switched-capacitors such as the ones shown in Figs. 4.2 & 4.3 were measured from 50 MHz to 6 GHz. All measurements were performed in lab ambient with no flowing nitrogen. The up-and-down-state capacitances were extracted by fitting the measured S-parameters to the equivalent lumped-element circuit models (Fig. 4.2). The extracted capacitances for the single 1x1 device are  $C_u = 51\ \text{fF}$ , and  $C_d = 2.6\ \text{pF}$  ( $C_r = 51$ ) for an actuation voltage of 46 V (Fig. 4.3). The  $C_d$  values varied from 2.6-2.9 pF for the individual switches due to variations in the  $\text{Si}_3\text{N}_4$  dielectric thickness across the wafer.

Metal-insulator-metal capacitors were measured on the same device wafer and show a  $\text{Si}_3\text{N}_4$  dielectric permittivity of  $\epsilon_r = 7.4$ . The effective permittivity of the RF



**Table 4.1:** 1-port Switched Capacitor Measurements.

	$C_u$ (fF)	$C_d$ (pF)	$R_{se}$ ( $\Omega$ )	$Q_d$ ( $Z_d=-j50\Omega$ )	Freq. (MHz)
1x1	51	2.74	0.60	83	1149
2x2	247	11.22	0.97	52	284
3x2	373	17.49	0.80	63	182

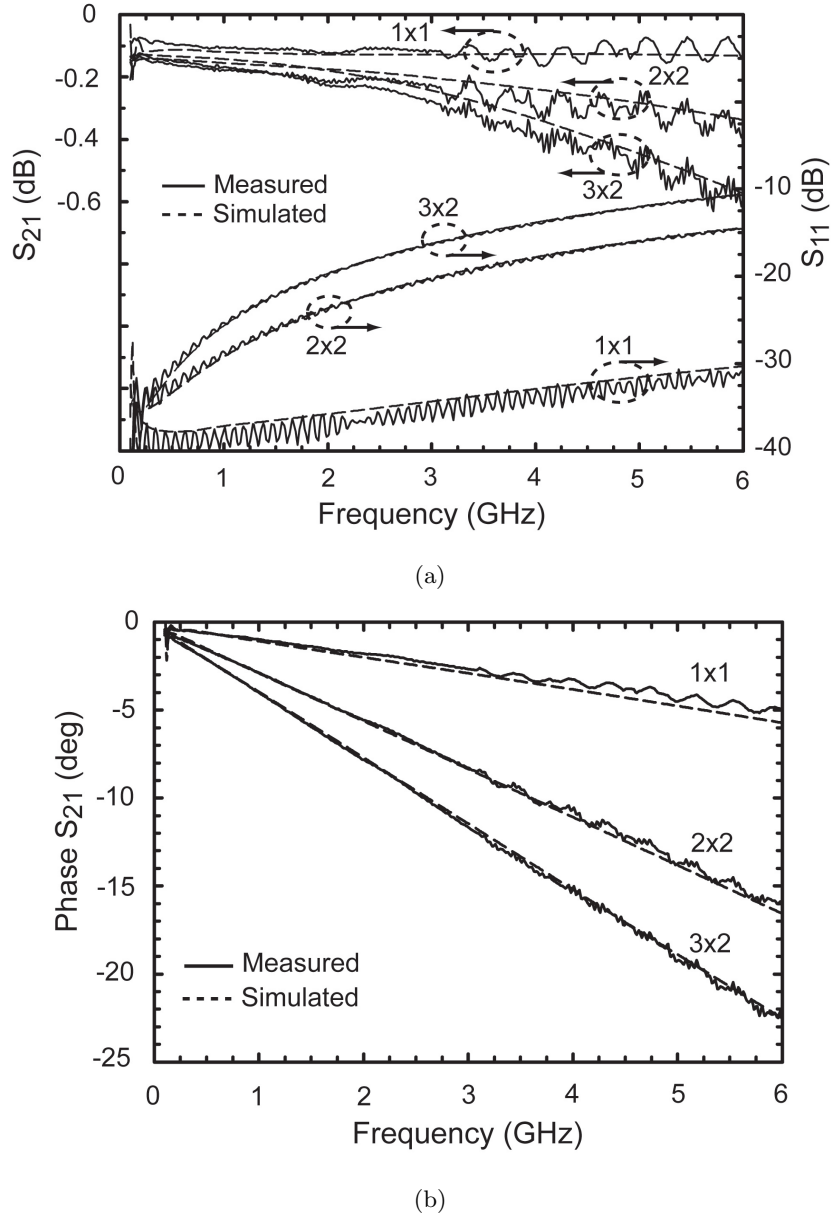
MEMS device dielectric is  $\epsilon_e = 4.4$  ( $0.6\epsilon_r$ ) due to a relatively smooth dielectric process (a 40-50 % roughness factor is typical in our technology). The single switched capacitor has only 2 pH of inductance with a resistance of 0.6  $\Omega$  that is dominated by the thin 3500 Å bottom metal (Fig. 4.3). The bottom metal should be increased in future designs to improve the device quality factor.

The equivalent circuit models for the 2x2 and 3x2 arrays and associated parameter values are shown in Fig. 4.2. The arrays include a short section of high impedance transmission line between devices, which is modeled as a series inductance of 15 pH and a shunt capacitance of 6 fF. The extracted capacitance for the 2x2 and 3x2 arrays are  $C_u = 241$  fF, 367 fF and  $C_d = 11$  pF, 16.6 pF, respectively. Both the single device and switch arrays were simulated the up-and-down state positions in a full-wave EM simulator Sonnet [41]. The measured and simulated S-parameters for both switch states are shown in Figs. 4.4 & 4.5, and show good agreement.

S-parameters were measured from 0.1-3 GHz from one-port 1x1, 2x2, and 3x2 switched capacitors in order to extract the down-state quality factor. The up-state quality factor is very-high and cannot be measured accurately using S-parameters. The measured down-state factor (Fig. 4.6) is “noisy” at the lower frequencies due to the high device impedance. In order to extract an accurate quality factor, the series switch resistance and down-state capacitance were extracted directly from the measured S-parameters and used in  $Q = 1/(\omega C_d R_{se})$  (dotted line in Fig. 4.6). The quality factor is specified at the frequency where the down-state capacitor impedance is  $Z_d = -j50 \Omega$  (Table 4.1). The 3x2 array has a lower series equivalent resistance ( $R_{se}$ ) compared to the 2x2 array due to the additional parallel connection.

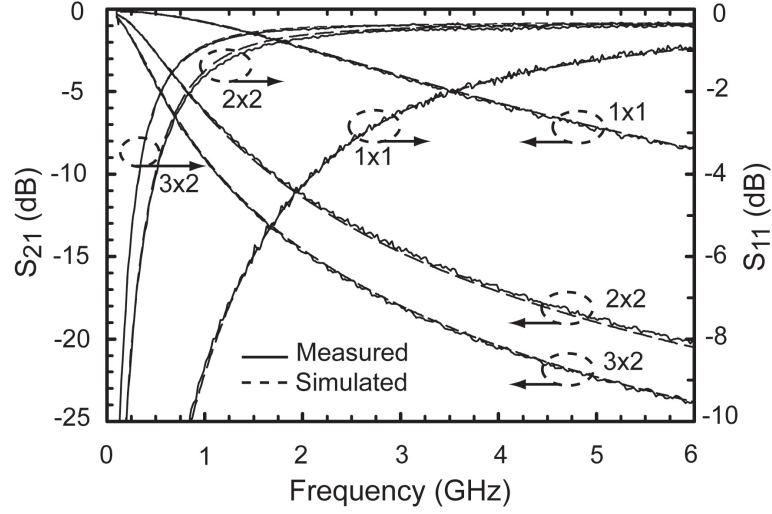
The measured and ideal down-state impedance are shown in Fig. 4.7. The 2x2 and 3x2 arrays ( $C_d = 11.22, 17.49$  pF) result in an impedance of 144-7  $\Omega$  and 91-4  $\Omega$  from 100-2000 MHz, respectively. These devices act as near-ideal capacitors over a 20:1 frequency range with very low-series inductance.

The RF power handling of the switched capacitors was also tested under a



**Figure 4.4:** Measured and simulated S-parameters in the up-state position (a) insertion and return loss (b) insertion phase.

continuous power at 1 GHz, and the release voltage was monitored versus the incident power level. The 2x2, and 3x2 arrays handled 400 mW under hot-switching conditions before “latching” occurred [43]. For a release voltage of 10 V, and a shunt impedance of 10-20  $\Omega$  for the 2x2 and 3x2 arrays, one would expect a hold-down power of 3.1-12.5 W, respectively (assuming no heating effects) [44]. Therefore the measured power handling is being limited by dielectric charging [50]. The arrays are well suited for UHF and VHF



**Figure 4.5:** Measured and simulated S-parameters in the down-state position.

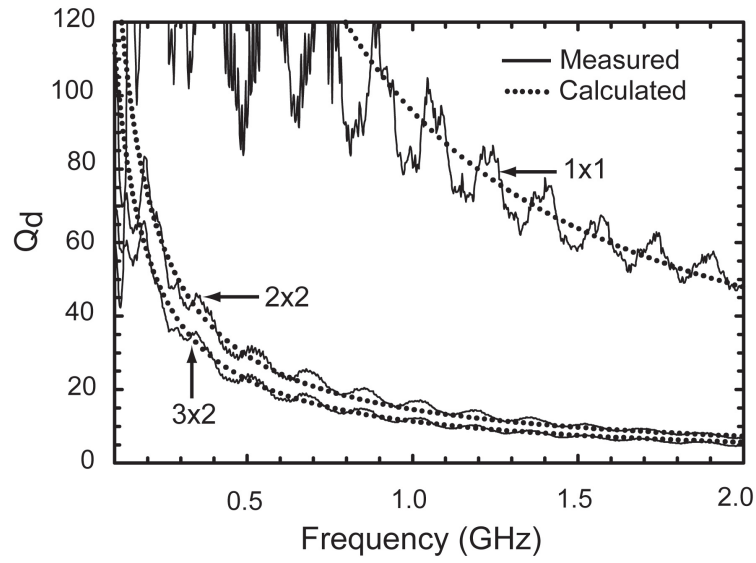
tunable filters and matching networks.

The measured frequency response of the 1x1, 2x2, and 3x2 switched capacitors are shown in Fig. 4.4a. The simulated mechanical resonance frequency is 85 kHz. The measured response of the 1x1 device shows good agreement with theory ( $f_o = 85 \text{ kHz}$ ,  $Q_m = 0.28$ ). The switch is over-damped, and future designs should include small holes in the membrane to reduce squeeze film damping. The 2x2 and 3x2 arrays show nearly the same mechanical resonance frequency and  $Q_m$ .

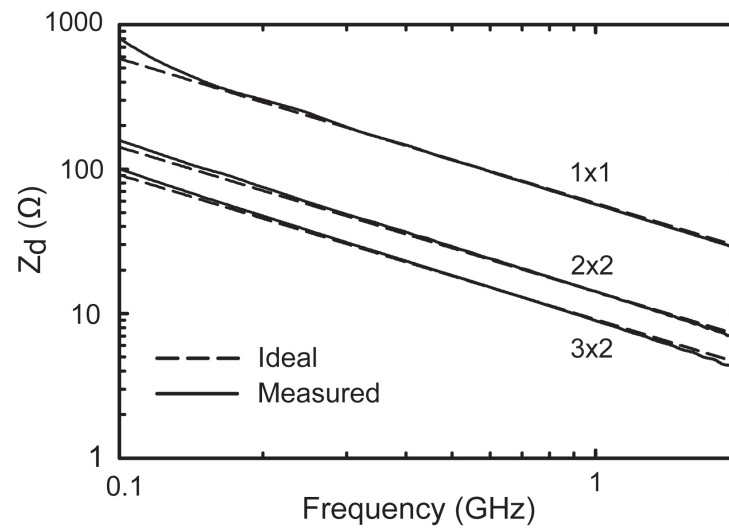
For the switching speed measurement, a 60 V unipolar voltage at 10 Hz is applied through the bias tee and the device is injected with 10 dBm of power at 10 GHz. A switching speed of  $18.8 \mu\text{s}$  was measured for the up-to-down switch transition for a 1x1 device. The measured switching time for the 2x2 and 3x2 arrays were within  $\pm 0.5 \mu\text{s}$  of the 1x1 device. The down-to-up switching speed could not be measured accurately due to significant dielectric charging induced by the 60 V unipolar voltage.

## 4.5 Summary

A cascable RF MEMS switched capacitor technology has been demonstrated for 0.1-2 GHz applications. Future improvements should concentrate on a thicker  $1 \mu\text{m}$  bottom metal for a higher electrical Q, additional release holes in the beam to reduce the switching speed, and a rougher and thicker dielectric for charging mitigation (at



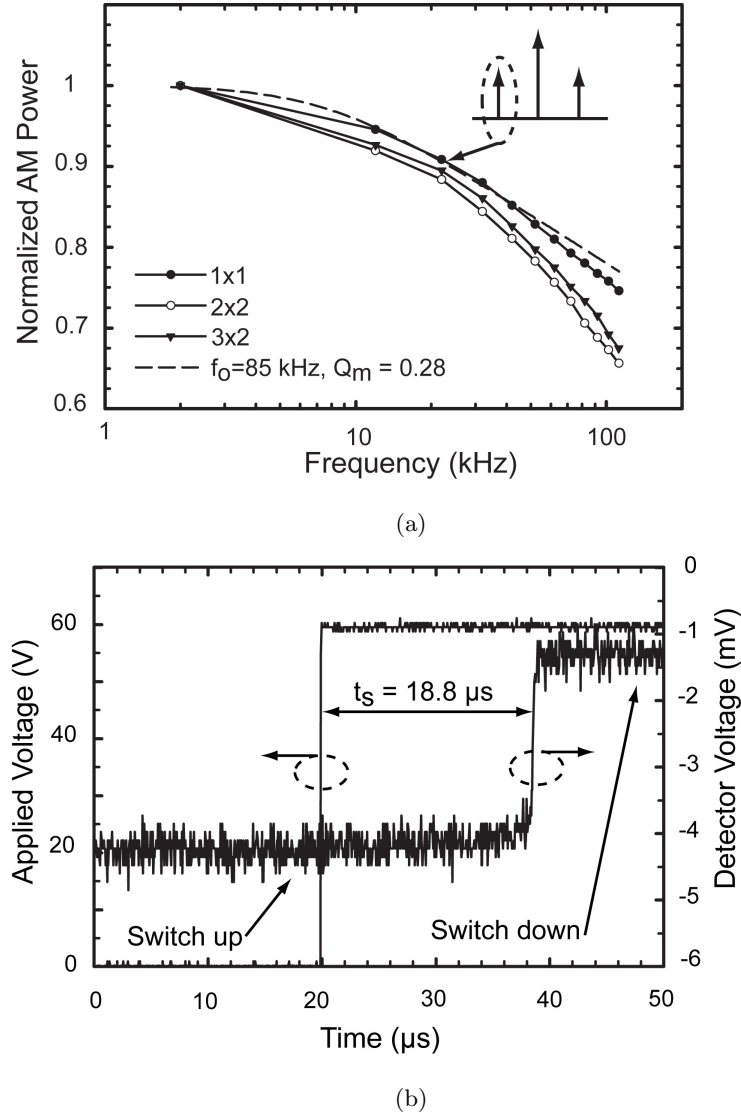
**Figure 4.6:** Measured down-state switched capacitor quality factor.



**Figure 4.7:** Measured and ideal down-state switched capacitor impedance.

the expense of a lower down-state capacitance). The topology can be extended to 4x4 or even 8x8 arrays with low-inductance. The output port can also be taken from the “north” or “south” sides of the chip, depending on its placement in the tunable network. These device arrays can also be arranged together to provide multi-bit capacitive tuners.

Chapter 4 is mostly a reprint of the material as it appears in IEEE Int. Microwave Symposium, 2009. Isak Reines and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.



**Figure 4.8:** (a) AM level vs. applied modulation frequency at the bias-tee (b) switching speed measurement from the up-to-down transition for a 1x1 device.

# Chapter 5

## A Robust High Power-Handling ( $>10$ W) RF MEMS Switched Capacitor

### 5.1 Introduction

Many reconfigurable front-end transmit applications require hot-switching operation under high power conditions. The power handling of RF MEMS capacitive shunt switches is limited by both the effective RMS voltage of the microwave signal and the non-uniform heating of the MEMS beam due to the dissipated power [44]- [42]. Under continuous RF power the limiting failure mechanism is “latching” of the MEMS beam which occurs when the RMS voltage from the incident power is greater than the device release voltage [43].

Recently, H. Yamazaki et al. reported a tunable RF MEMS capacitor with 5 W of continuous power handling at 2 GHz and 85°C with an actuation voltage of 21 V. However, this design requires 2 metal-insulator-metal (MIM) capacitors to reduce the RF voltage across the MEMS device which increases the overall die size and limits the obtainable capacitance ratio with a demonstrated  $C_r$  of 2.9 [51]. C. Palego et al. previously reported an RF MEMS switched varactor based on a double-step beam, that resulted in 10 W of hot-switched power handling at 3 GHz with a  $C_r = 7-8$ , but this varactor has a pull-in voltage of 115 V which is impractical for many applications and also leads to enhanced dielectric charging [52].

In this chapter, we present a  $> 10$  W hot-switched MEMS switched capacitor with a pull-in voltage  $< 30$  V and a  $C_r = 5.7$ . The switch utilizes a stress-tolerant circular beam geometry to minimize thermally induced changes in the spring constant and gap height due to RF power dissipation in the switch [53].

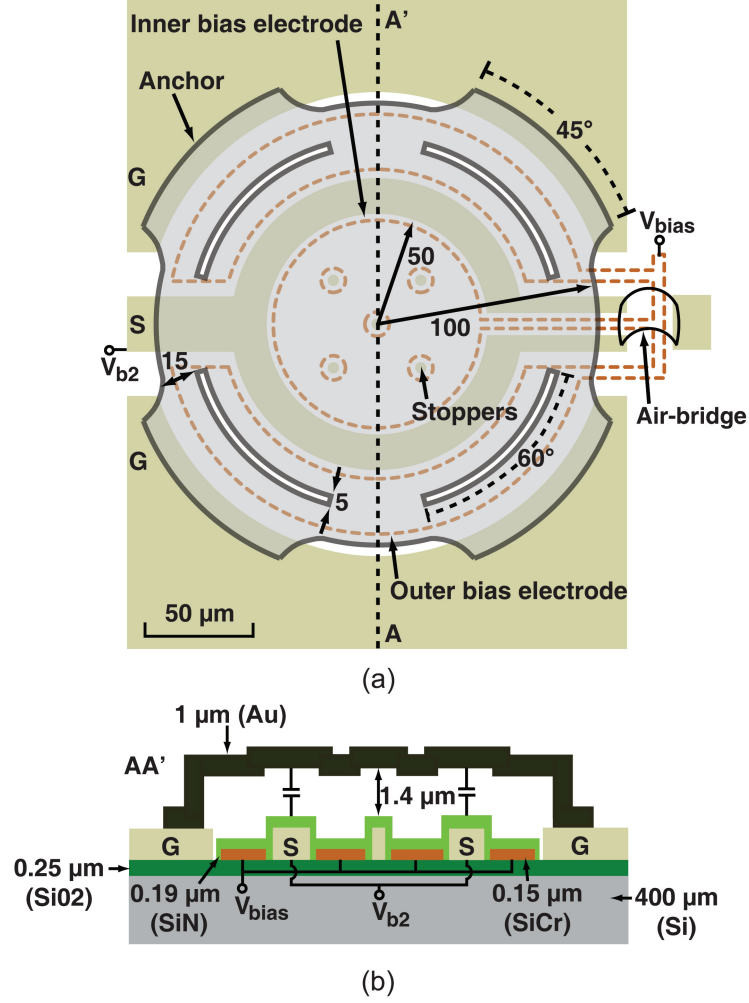
## 5.2 Switch Design

Fig.5.1 shows the top view and cross-section of the high-power RF MEMS shunt switched capacitor. The device consists of ring-shaped RF transmission line that is routed underneath the higher spring constant portion of the circular beam to increase both the restoring force above the RF line and the RF self-actuation voltage. Separate DC bias electrodes are placed on the either side of the RF line to maintain a relatively low pull-in voltage and to assure an intimate contact with the RF line once the switch is actuated. Isolated stopper bumps are placed within the center portion of the DC bias pad to reduce the amount of charge injected into the dielectric when switch is in the down-state position. An electroplated gold air-bridge is used to connect the signal line on the output side of the switch and to accommodate routing of the DC bias lines to the device (Fig.5.1).

The switch has a beam radius of  $100\ \mu\text{m}$  and overall footprint of  $120 \times 120\ \mu\text{m}^2$  including the anchor areas. The beam is comprised of a  $1\ \mu\text{m}$ -thick gold layer to reduce the thermal resistance of the bridge and arc-shaped cutouts are placed  $15\ \mu\text{m}$  from the edge of the circular beam. The wider springs function to lower the thermal resistance of the beam but also increase the device sensitivity to in-plane stress. In general, the closer the cutouts are placed to the anchor and the thinner the springs, the lower the ratio of  $K_2/K_1$  (i.e. sensitivity to in-plane biaxial stress). The switch design presented in Chapter 2 has a  $90^\circ$  corner located between the edge of the circular beam and anchor. Full-wave simulations of the switch, performed in both Sonnet and HFSS [54], have shown that these corner areas have the highest current density on the beam and produce current crowding and localized hot spots. To reduce the current density in these areas the  $90^\circ$  corners are replaced by smooth curved transitions.

Electro-mechanical simulations of the switch were performed in CoventorWare [34], with the results shown in Table 5.1. The spring constant is here defined as the displacement ( $\Delta Z$ ) in the center of the beam due to a uniform pressure ( $p$ ) distributed above the 3 DC bias electrodes of area ( $A$ ), such that  $K = (p \cdot A) / \Delta Z$ . The switch has a





**Figure 5.1:** Top-view (a), and cross-section (b) of the high-power RF MEMS switched capacitor.

spring constant of  $K = 85.3 \text{ N/m}$  assuming an in-plane beam stress of  $\sigma_{res} = 50 \text{ MPa}$  and linear vertical stress gradient of  $\Delta\sigma_{linear} = 15 \text{ MPa}/\mu\text{m}$ . The simulated up-state capacitance of the beam is 58 fF excluding any fixed parasitic capacitance, while the down-state capacitance is 649 fF for  $V_{bias} = 35 \text{ V}$  and  $\epsilon_{r-eff} = 3.0$ . The simulated pull-in voltage for the DC bias electrode is  $V_{p-bias} = 25.8 \text{ V}$ , while the pull-in voltage on the RF line is  $V_{p-RF} = 38.3 \text{ V}$ . The RMS voltage that will be generated between the capacitor electrodes for an incident power is given by

$$P_{in} = \frac{V_{p-RF}^2}{Z_o} \quad \text{for } \omega C_{up} Z_o \ll 1 \quad (5.1)$$

Since the signal line is split into two lines under the MEMS beam, the impedance is  $> 50$

**Table 5.1:** Simulated Electro-Mechanical Parameters of the High-Power RF MEMS Switch

Parameter	Value
$K_1, K_2, K_{total}$ (N/m)	42.6, 42.7, 85.3
$C_{up}$ (fF)	58
$C_d$ with ( $V_{bias} = 35$ V) (fF)	649
$V_{p-bias}$ (V)	25.8
$V_{r-bias}$ (V)	10 +/- 2.5
$V_{p-RF}$ (V)	38.3
$V_{r-RF}$ (V)	25 +/- 2.5

- Simulated with  $\sigma_{res} = 50$  MPa,  $\Delta\sigma_{linear} = 15$  MPa/ $\mu\text{m}$ , and  $\epsilon_{r-eff} = 3.0$

$\Omega$  and is approximated in ADS as two coupled lines between a ground plane and yields an even mode impedance of  $Z_e = 95 \Omega$ . With this impedance, and using the simulated pull-in voltage on the RF line ( $V_{p-RF} = 38.3$  V), the device is predicted to self-actuate at  $P_{in} = 15.6$  W (excluding the effects of RF power dissipation in the beam). The simulated release voltage of the switch for a voltage on the bias electrode is  $V_{r-bias} = 10$  V with an accuracy of +/- 2.5 V, while the release voltage on the RF line is  $V_{r-RF} = 25$  +/- 2.5 V. The release voltage simulations have an accuracy of +/- 2.5 V due to the voltage trajectory step sizes. In the down-state position, the RMS voltage across the switch is given by

$$V_{rms} = \frac{2\sqrt{P_{in}Z_o}}{\omega C_d Z_o} \quad \text{for } \omega C_d Z_o \gg 1 \quad (5.2)$$

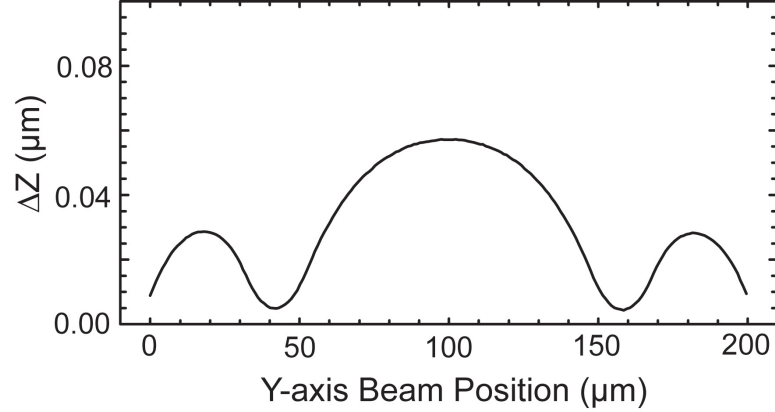
Table 5.2 summarizes the calculated RMS voltages across the switch in the down-state position with  $P_{in} = 5$  and 10 W for several capacitance values.

**Table 5.2:** Calculated RMS Voltage across Switch in the Down-state Position

$C_d$ (fF)	$V_{RMS}$ (V) with $P_{in} = 5$ W	$V_{RMS}$ (V) with $P_{in} = 10$ W
312	23.5	33.3
500	14.7	20.8
646	11.4	16.0

Fig. 5.2 presents the simulated change in Z-displacement ( $\Delta Z$ ) of the MEMS beam along the y-axis with  $\sigma_{res} = 50$  MPa, and  $\Delta\sigma_{linear} = 15$  MPa/ $\mu\text{m}$ . The change in vertical displacement is  $< 0.06 \mu\text{m}$  across the 200  $\mu\text{m}$  diameter switch, resulting in very

little change in the as-deposited gap height of the bridge.



**Figure 5.2:** Simulated change in Z-displacement of the beam ( $\Delta Z$ ) along the y-axis (with  $\sigma_{res} = 50$  MPa, and  $\Delta\sigma_{linear} = 15$  MPa/ $\mu\text{m}$ ).

### 5.2.1 RF Power Dissipation in the MEMS Switch

The RF power dissipation in the MEMS switch is simulated using a full-wave EM simulator [41], and the dissipated power is calculated using (2.6). The switch is simulated at 10 GHz in both the up-and-down state positions with a nominal gap height of  $g_o = 1.4 \mu\text{m}$  and  $0.93 \mu\text{m}$  ( $2/3g_o$ ,  $V_{applied} = V_{p-bias}$ ) for the up-state simulations, and a conservative conductivity of  $\sigma_{Au} = 3.1 \times 10^7$  S/m is used for the  $1 \mu\text{m}$ -thick gold beam. At 10 GHz, the MEMS beam dissipates 0.397-0.434% of the incident power which results in 39.7-43.4 mW of dissipated power for an incident power of 10 W (Table 5.4). In the down-state position, the MEMS beam dissipates 0.619-0.724% of the incident power for  $C_d = 312$ -649 fF, which results in 61.88-72.42 mW of dissipated power for  $P_{in} = 10$  W.

Conductor losses in the CPW transmission line contribute to the majority of power dissipation in the MEMS switch with 207.5 mW of dissipated power for  $P_{in} = 10$  W. The transmission line has a gold thickness of  $2.5 \mu\text{m}$ , except for the areas under the switch where it is  $0.5 \mu\text{m}$ , and the simulations assume a conductivity of  $\sigma_{Au} = 3.1 \times 10^7$  S/m. The substrate is  $400 \mu\text{m}$ -thick high-resistivity silicon ( $\tan\delta = 0.004$ ,  $\sigma = 0.0667$  S/m), which is coated on both sides with a  $0.25 \mu\text{m}$  layer of  $\text{SiO}_2$  ( $\tan\delta = 0.002$ ).

The RF current distribution on the MEMS beam is also simulated at 10 GHz in the up-and-down state positions with an incident power of 20 mW (Fig.5.3a-b). In the up-state position the peak RF current density occurs along the edge of the circular beam between the signal line and grounded switch anchors with an average value of  $\sim 600$

**Table 5.3:** Simulated Power Dissipated in the MEMS Switch at 10 GHz with  $P_{in} = 10$  W.

<i>Substrate</i>	<i>Beam</i>	<i>T – Line</i>	<i>Gap</i> ( $\mu\text{m}$ )	$P_{ref.}$ (%)	$P_{trans.}$ (%)	$P_{diss.}$ (%)	$P_{diss.}$ (mW)
Lossless	Lossy	Lossless	1.40	0.582	99.021	0.397	39.7
Lossless	Lossy	Lossless	0.93	1.499	98.067	0.434	43.4
Lossless	Lossless	Lossy	1.40	0.499	97.426	2.075	207.5
Lossy	Lossless	Lossless	1.40	0.610	99.018	0.373	37.3
Lossy	Lossy	Lossy	1.40	0.47	96.686	2.845	284.5
Lossless	Lossy	Lossless	0	25.326 <sup>a</sup>	74.055 <sup>a</sup>	0.619 <sup>a</sup>	61.88 <sup>a</sup>
Lossless	Lossy	Lossless	0	42.240 <sup>b</sup>	57.030 <sup>b</sup>	0.724 <sup>b</sup>	72.42 <sup>b</sup>

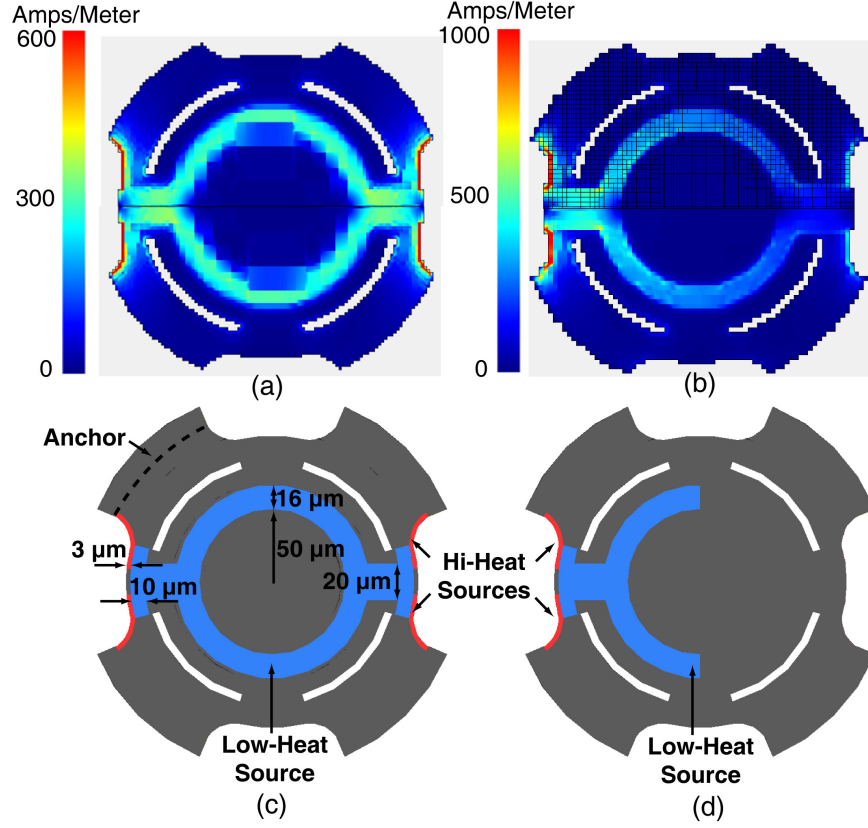
<sup>a</sup> Simulated with  $C_d = 312$  fF<sup>b</sup> Simulated with  $C_d = 649$  fF

A/m, while the remaining RF currents are distributed above the center portion of the ring shaped signal line with a value of  $\sim 250$  A/m. These RF current densities indicate that in the up-state position  $\sim 85\%$  of the incident power is dissipated along the edges of the switch with the remaining 15% occurring above the signal line. In the down-state position, the peak current density is located on input side of the switch along the edge of the beam between the ground and signal electrodes with an average value of 1000 A/m, while the remaining currents are located above the ring-shaped signal line on the input side of the beam with a value of  $\sim 400$  A/m. These results indicate that in the down-state position  $\sim 85\%$  of the power is dissipated along the edge of the beam with the remaining  $\sim 15\%$  above the input side of the beam above the signal line (Fig. 5.3b).

### 5.2.2 Thermo-Mechanical Simulations

Fig.5.3c-d shows the position and dimensions of the discrete volumetric heat sources used in the Coventorware thermo-mechanical simulations. Only heat transfer through conduction is considered while radiation and convection losses are ignored [42]. In the up-state simulations, the total dissipated power in the beam is varied from 0-50 mW and the base of the substrate is fixed at  $25^\circ\text{C}$  with an initial system temperature of  $25^\circ\text{C}$ . Fig. 5.4a presents the simulated spring constant and change in the vertical displacement in the center of the beam ( $\Delta Z$ ), versus dissipated power in the MEMS beam ( $P_d$ ) with  $\sigma_{res} = 50$  MPa, and  $\Delta \sigma_{linear} = 15$  MPa/ $\mu\text{m}$ .

Thermally induced stress changes in the beam lead to a linearly decreasing spring constant from 85.3-46.8 N/m for  $P_d = 0$ -50 mW ( $T_{peak} = 25$ -68.4 $^\circ\text{C}$ ), while  $\Delta Z$  increases from 0.06-0.23  $\mu\text{m}$  due to the effects of topography and non-uniform heating



**Figure 5.3:** Simulated RF current distribution on the circular RF MEMS switch in the up-state position (a), and down-state position (b), with  $f_o = 10$  GHz, and  $g_o = 1.4$   $\mu\text{m}$ , and placement of the discrete volumetric heat sources used in the Coventorware thermo-mechanical simulations in the up-state (c), and down-state (d) positions.

[53]. The combination of a decreasing spring constant and increasing gap height results in a stable pull-in voltage for up to 10 W of incident power since  $V_p \propto K^{0.5}$  and  $g_o^{1.5}$ . Fig. 5.4b shows the peak temperature of the MEMS beam in the up-state position versus dissipated power with the hottest region located in the switch springs between the signal and ground electrodes. The thermal conduction resistance of the beam is  $R_{cond-up} = 859^\circ\text{C}/\text{W}$ , which yields a peak temperature of  $62.3^\circ\text{C}$  for an incident power of 10 W ( $P_d = 43.4$  mW). The thermal time constant in the up-state position is  $\tau_{up} = 90.5$   $\mu\text{s}$ . In the down-state position, the peak temperature on the MEMS beam is located in the elevated springs between the signal line and grounded anchors, and is  $48.0$ - $51.9^\circ\text{C}$  for  $P_d = 61.88$ - $72.42$  mW. Since the majority of the beam is in contact with the underlying capacitor dielectric when the switch is actuated, the thermal conduction resistance is lower with  $R_{cond-down} = 372^\circ\text{C}/\text{W}$ . The thermal time constant in the down-state position is 39.2

$\mu\text{s}$ .

### 5.3 Fabrication

The CPW implemented switched capacitor is fabricated on a  $400\ \mu\text{m}$  high-resistivity silicon substrate ( $\epsilon_r = 11.9$ , and  $k = 149\ \text{W/mK}$ ) to dissipate the heat generated in the MEMS beam. First, a  $0.15\ \mu\text{m}$  layer of sputtered SiCr ( $R_s = 3\ \text{k}\Omega/\text{sq}$ ) is patterned for the bias lines and DC bias electrodes. A  $0.5\ \mu\text{m}$  layer of sputtered gold is then deposited to define both the bottom capacitive electrode and isolated stopper bumps. Next,  $0.19\ \mu\text{m}$  of PECVD deposited SiN is patterned using RIE to form the switch dielectric. The sacrificial layer of the switch is a  $1.4\ \mu\text{m}$ -thick layer of PMMA which is patterned using RIE. Next,  $1\ \mu\text{m}$  of sputtered gold is deposited to form the MEMS beam. The transmission lines are next electroplated with an additional  $1\ \mu\text{m}$  of gold to reduce conductor losses. Lastly, the gold MEMS beam is patterned with KII gold etchant and the sacrificial layer is removed in a solvent at  $80^\circ\text{C}$  before the devices are released in a  $\text{CO}_2$  critical point dryer.

A micrograph and 3-D white light interferometer image of the fabricated device are shown in Fig. 5.5a-b. The profile of the switch is measured pre-and-post release and shows a vertical beam deflection of  $< 0.1\ \mu\text{m}$  (Fig. 5.5c), which agrees well with the simulation presented in Fig. 5.2. A detailed description of the high-power RF MEMS switched capacitor fabrication process is presented in Appendix B.

### 5.4 Measurements

#### 5.4.1 Capacitance vs. Voltage

The capacitance versus voltage curve of the shunt switched capacitor referenced from the planes BB' (Fig. 5.5a) is extracted directly from the measured S-parameters at each particular bias voltage (Fig. 5.6a). All measurements are performed in an enclosed environmental chamber with flowing nitrogen. The switch has an up-state capacitance of  $C_{up} = 55\ \text{fF}$  and a down-state capacitance is  $C_d = 267\ \text{fF}$  for  $V_{bias} = 35\ \text{V}$ , which can be increased to  $C_d = 312\ \text{fF}$  by applying an additional voltage between the ground and signal electrodes with  $V_{b2} = 40\ \text{V}$ . The down-state capacitance is lower than predicted for this fabrication run due a rough PMMA sacrificial layer process that transferred additional roughness into the sputtered gold beam which reduces the down-state contact

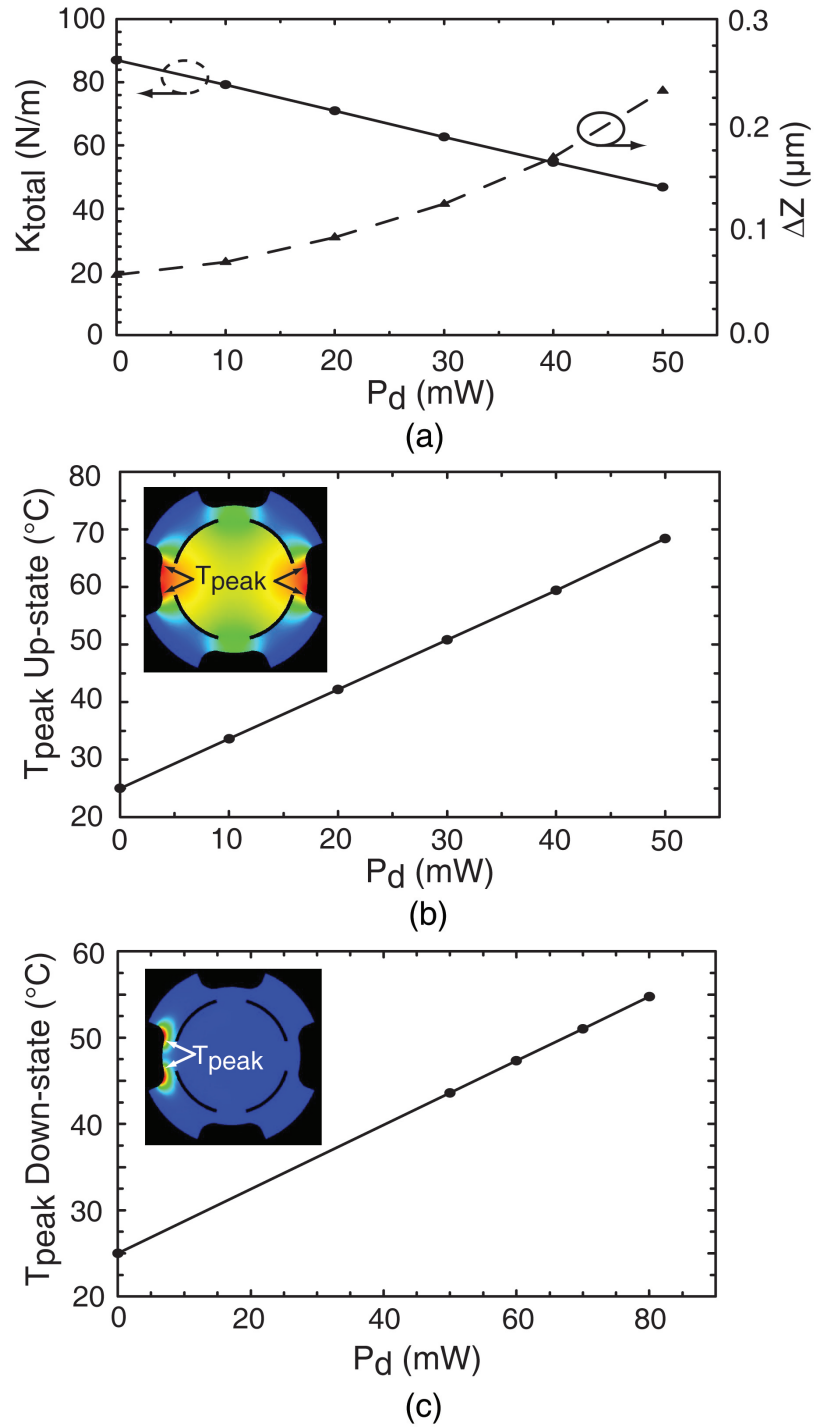
area of the beam. Devices from this wafer yielded a capacitance ratio of  $C_r = 5.7$  (with  $V_{bias} = 35$  V and  $V_{b2} = 40$  V), while simulations predict that a  $C_r$  of 10-11 is possible with improved fabrication processes and without the use of voltage  $V_{b2}$ . The equivalent circuit model of the switch from planes BB' is presented in Fig. 5.6b, which is based on a combination of Sonnet EM simulations and fitting to the measured S-parameters. The switched capacitor has an extracted bridge inductance and resistance of 3 pH, and 0.3  $\Omega$ , respectively. The standard rectangular switch, which is used for comparison, has an up-and-down state capacitance of  $C_u = 59$  fF, and  $C_d = 0.8$  pF, respectively. It has a length of 230  $\mu\text{m}$ , a width of 80  $\mu\text{m}$ , and is patterned over a 80  $\mu\text{m}$  wide signal line.

#### 5.4.2 Pull-in Voltage vs. Temperature

The pull-in voltages of both the circular and standard switched capacitors from the same wafer were measured from 25-105°C (Fig. 5.7). The standard rectangular fixed-fixed beam switch has a width of 80  $\mu\text{m}$  and length of 230  $\mu\text{m}$ , and is patterned on top of an 80  $\mu\text{m}$  wide signal line with the top-view shown in Fig. 5.7. The standard switch has an up-and-down-state of capacitance of 59 fF and 800 fF, respectively. The circular switch has a pull-in voltage slope vs. temperature of -112.5mV/°C, compared to -300 mV/°C for the standard design. The standard switch failed at 85°C ( $V_p = 0$  V), while circular switch was still operational with  $V_p = 20$  V. Some plastic deformation of the 1  $\mu\text{m}$  sputtered gold beam was observed after temperature cycling the switches to 105°C, which caused both an increase in the nominal gap height and pull-in voltage when the device was returned to room temperature. This issue is purely a materials problem which can be solved by using a different beam metal such as aluminum.

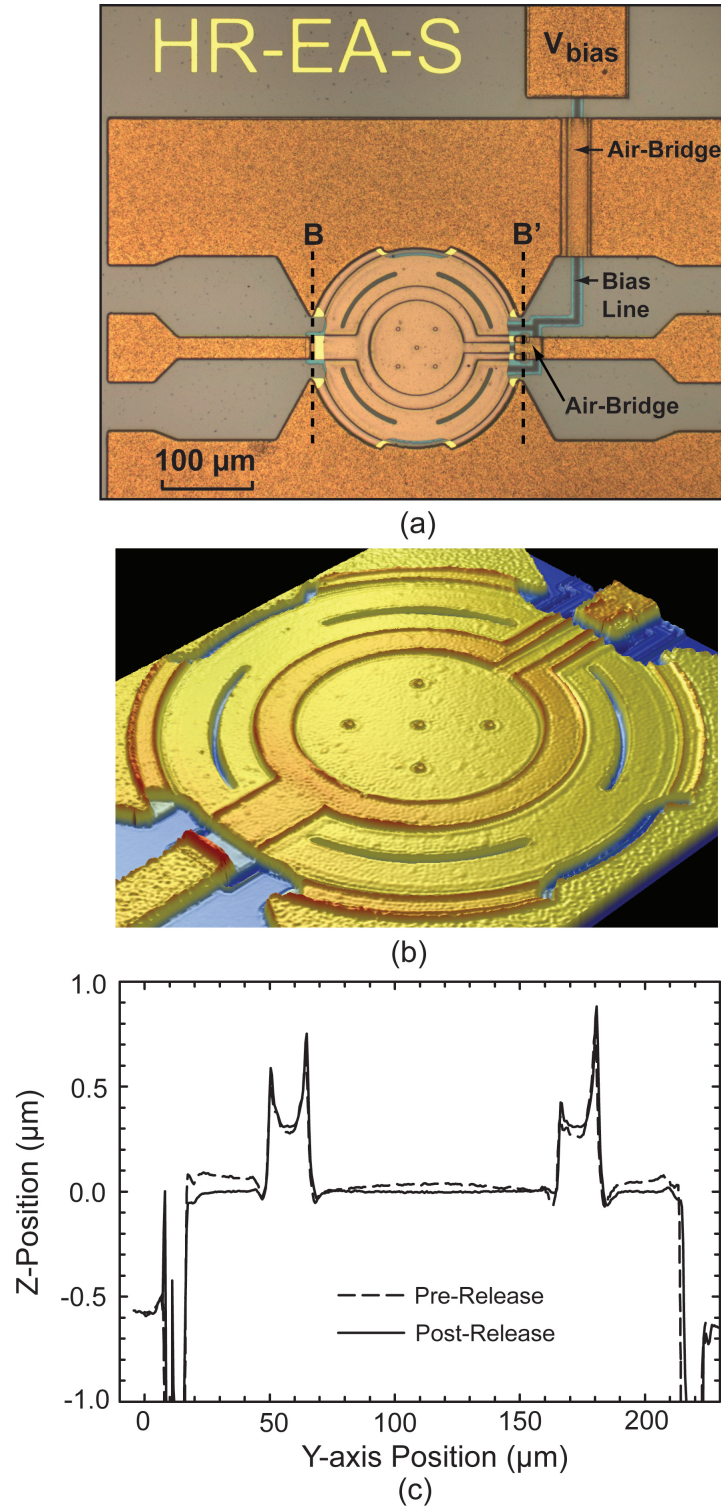
#### 5.4.3 RF Power-Handling

The RF power handling of both standard and circular switched capacitors was tested under continuous power at 10 GHz, and the pull-in and release voltages were monitored versus incident power using the measurement setup shown in Fig. 5.8. In order to measure the pull-in and release voltage, a bipolar triangular waveform with a period of 16 ms and duty cycle of 1.6% is applied to the bias electrode of the switch and the modulated voltage from the diode detector is connected to an oscilloscope and compared to the original bias waveform. The low duty cycle of the bias waveform reduces the effects of dielectric charging, thus increasing the accuracy of the measurement. When

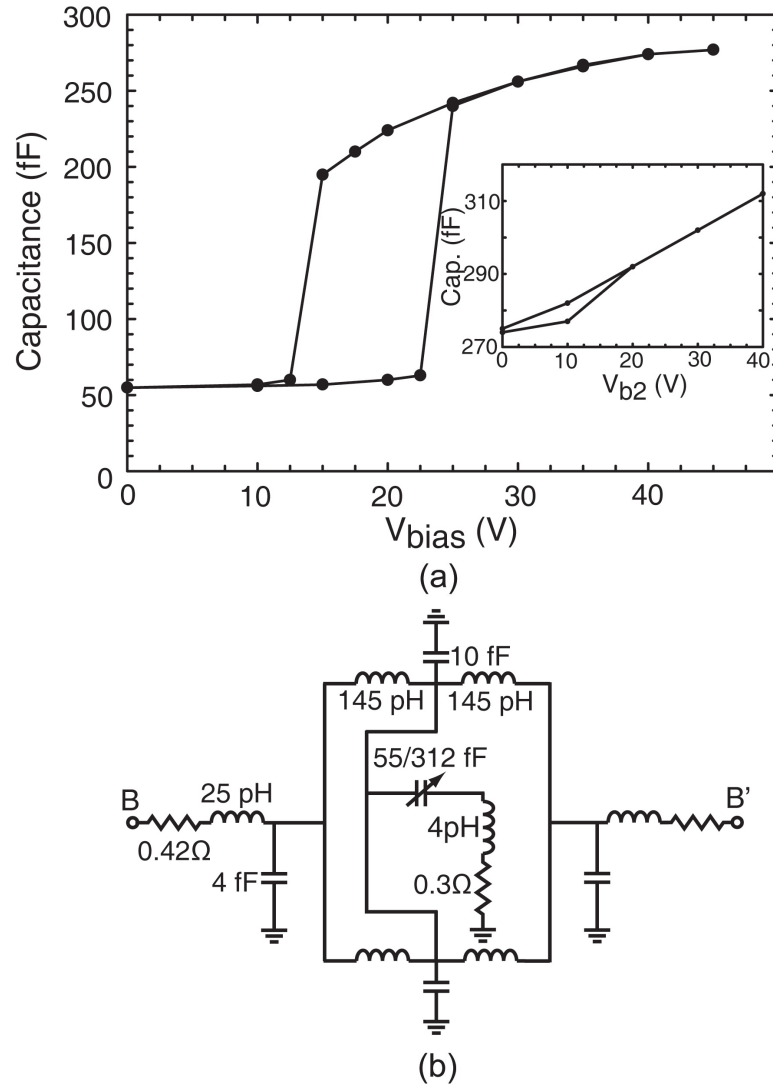


**Figure 5.4:** Simulated spring constant and change in z-displacement in the center of the circular beam versus dissipated power ( $\sigma_{res} = 50$  MPa,  $\Delta\sigma_{linear} = 15$  MPa/ $\mu\text{m}$ ) (a), and peak temperature on the beam in the up-state position (b), and down-state position (c) versus dissipated power.

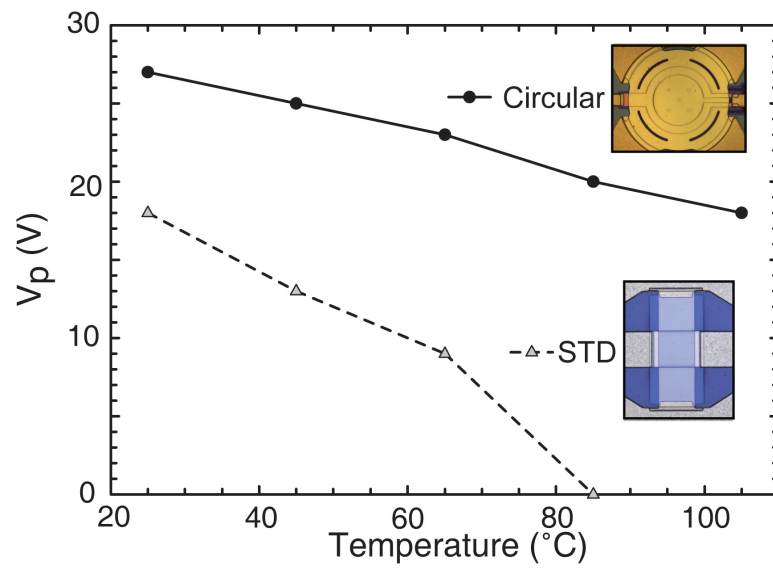




**Figure 5.5:** Micrograph (a), 3-D white light interferometer image (b), and measured pre-and-post beam profile along the y-axis (c), of the high-power RF MEMS switched capacitor.

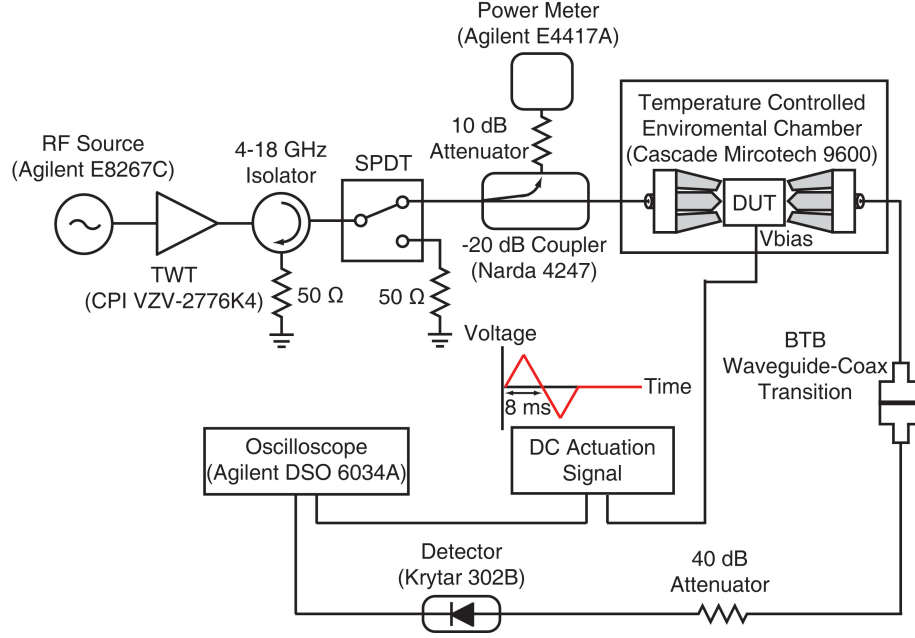


**Figure 5.6:** Measured C-V curve of the switched capacitor with inset showing capacitance vs.  $V_{b2}$  with  $V_{bias} = 40$  V (a), and equivalent symmetric lumped element circuit model (b).



**Figure 5.7:** Measured pull-in voltage vs. ambient temperature from 25-105 $^{\circ}\text{C}$  for both standard and circular designs.

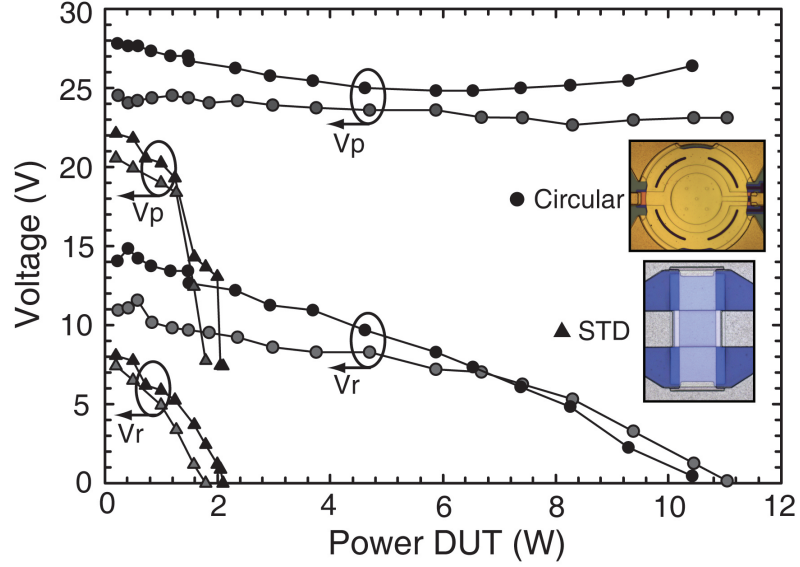
testing the power-handling of the standard switch, a bias-tee is added to the setup before the DUT to accommodate the bias voltage. The SPDT switch is utilized to protect the equipment after the 25 W TWT amplifier from possible power spikes that can occur when turning on or off the RF signal source or the TWT itself. The RF power supplied to the DUT was gradually increased starting at 200 mW, and  $V_p$  and  $V_r$  were recorded at each discrete power level.



**Figure 5.8:** Measurement setup for testing the pull-in and release voltage of the RF MEMS switched capacitor vs continuous RF power at 10 GHz.

The circular switches have initial pull-in and release voltages that range from  $V_p = 24.5\text{--}27.8$  V, and  $V_r = 11\text{--}14$  V, while the standard devices have  $V_p = 20.6\text{--}22.1$  V, and  $V_r = 7.4\text{--}8.1$  V (Fig. 5.9). A non-releasing ("latching") failure due to both a reduction in the restoring force ( $F_r = Kg_o$ ) and the effective  $V_{rms}$  from the incident power occurred between 10.4-11 W and 1.8-2.1 W for circular and standard switches, respectively. As predicted by the thermo-mechanical simulations, the pull-in voltage of the circular switches remained fairly constant with  $< 3$  V change in  $V_p$  from 0.2-10 W. Once "latching" of the switch occurred, the power was reduced to 200 mW, and  $V_p$  and  $V_r$  were re-measured. The high-power circular switches showed  $< 1$  V change in both the pull-in and release voltages from initial measurements. The pull-in voltage of the standard switch decreased by  $\sim 14$  V from 0.2-2.1 W, due to thermally induced reduction

in the spring constant from the RF power dissipation in the beam [44].

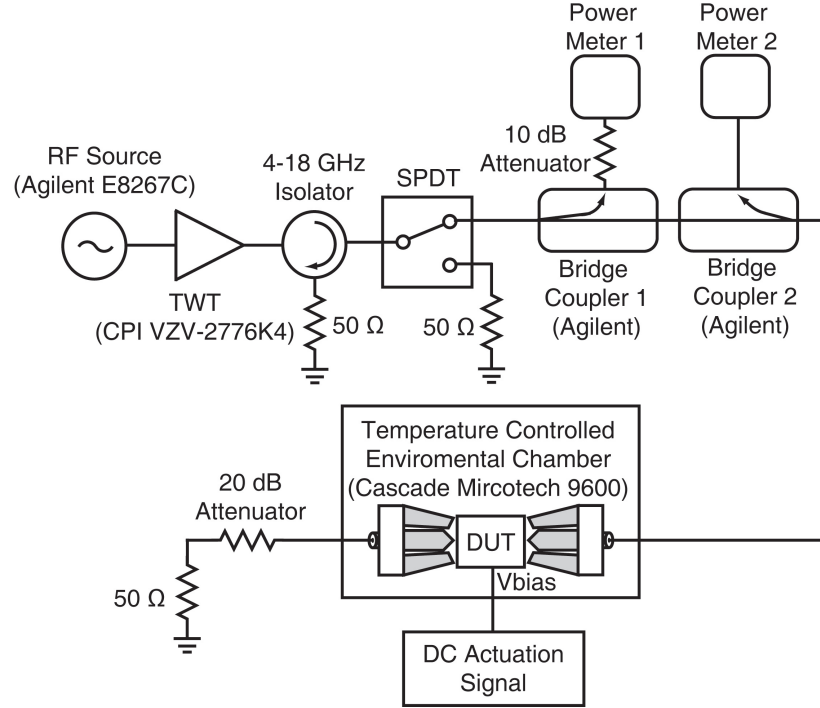


**Figure 5.9:** Measured pull-in ( $V_p$ ) and release voltage ( $V_r$ ) vs. continuous RF power at 10 GHz for both circular and standard switches.

#### 5.4.4 Capacitance vs. Power

Fig. 5.10 presents the measurement setup that is used for characterizing the capacitance of the switch versus incident power at 10 GHz. Two back-to-back directional couplers are used to create a reflectometer to monitor both the incident and reflected power. At 10 GHz the reflectometer has -40 dB isolation between the input and reflection ports with a combined insertion loss of -3.8 dB. The couplers have a power rating of 4 W which limits the maximum power delivered to the switched capacitor to 1.3 W.

In order to relate the reflected power from the device to the capacitance, the switched capacitor is first tested at low power ( $P_{in} = 50$  mW) vs. bias voltage and this data is compared to the C-V curve that is extracted from the S-parameter measurements. The switch used for this measurement has a pull-in and release voltage of  $V_p = 40$  V, and  $V_r = 25$  V, respectively, with  $C_{up} = 58$  fF, and  $C_{down} = 223$  fF with  $V_{bias} = 50$  V (Fig. 5.11a). The device is tested at power levels of 50 mW, 330 mW, 1 W, and 1.3 W, and the reflected power is recorded as a function of bias voltage with 2.5 V steps (Fig. 5.11b). The voltage sweep is repeated twice at each power level to check the consistency of the measurement.

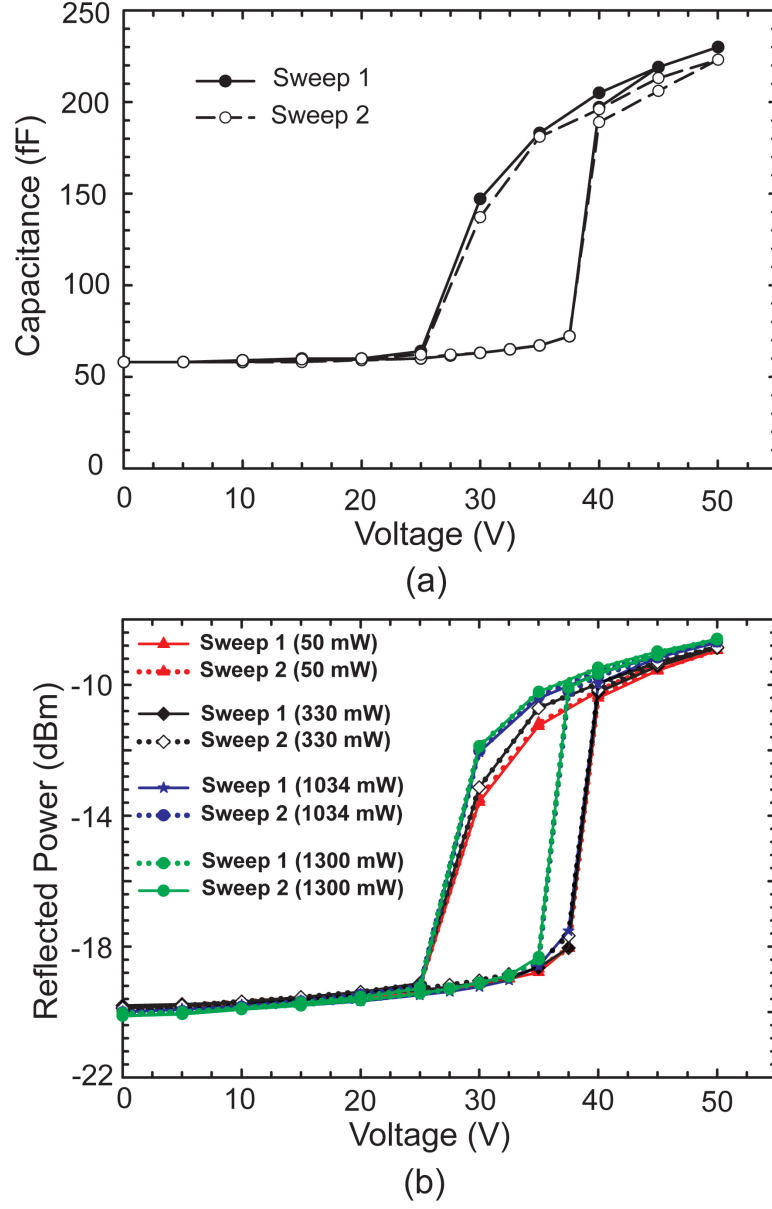


**Figure 5.10:** Measurement setup for monitoring the incident and reflected power of the switched capacitor vs. bias voltage.

Relating the capacitance to the reflected power with  $P_{in} = 50$  mW yields a linear relationship with a slope of 15 fF/dBm. Therefore, the change in capacitance of the device versus reflected power can be calculated using this measured slope. With  $V_{bias} = 0$  V, the up-state capacitance of the switch decreases by  $\sim 2$ -3 fF from 50 mW-1.3 W due to a slight increase in the gap height. In the down-state position with  $V_{bias} = 50$  V, the capacitance increases by  $\sim 5$  fF from 50 mW-1.3 W. With  $P_{in} = 1.034$  W, the pull-in voltage shifted down from 40-37.5 V ( $\pm 1.25$  V accuracy) on the second voltage sweep indicating some dielectric charging. No change in  $V_r$  is observed up to 1.3 W, however, when the switch is in the down-state position with  $V_{bias} = 30$  V, the capacitance increases by  $\sim 24$  fF from 50 mW-1.3 W as a result of the RMS voltage from the incident power.

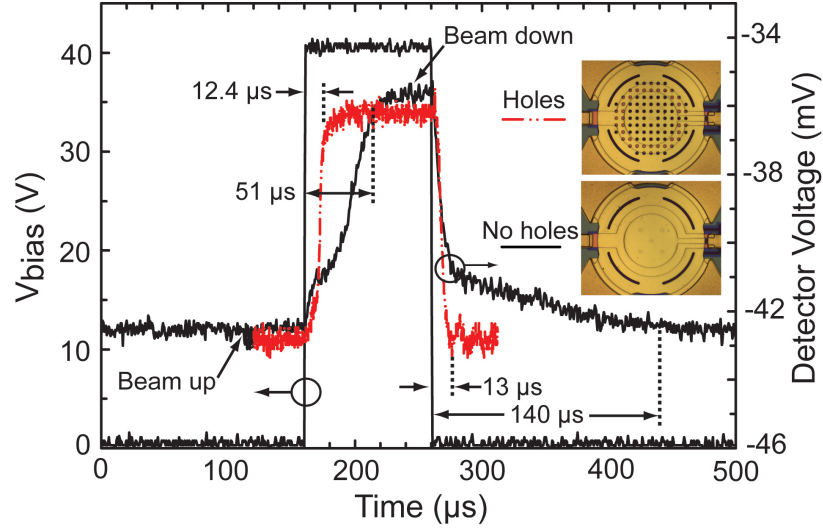
#### 5.4.5 Switching Speed

The switching speed of the circular switch with a without  $5 \times 5 \mu\text{m}$  perforations in the beam is measured with the setup shown in Fig. 2.20. With a 40 V stepped bias voltage, the up-to-down switching time is 12.4  $\mu\text{s}$  and 51  $\mu\text{s}$  for the switches with and



**Figure 5.11:** Measures C-V curve of the switched capacitor with  $P_{in} = -20$  dBm (a), and reflected power vs. bias voltage with  $P_{in} = 50$  mW, 333 mW, 1034 mW, and 1300 mW (b).

with perforations, respectively (Fig. 5.12). The switch with holes has a release time of 13  $\mu$ s, while the switch without holes takes  $\sim 140$   $\mu$ s to return to the full up-state position. The release time of the switch without holes was strongly dependent on the amplitude of the stepped bias voltage which indicates the effects of dielectric charging.



**Figure 5.12:** Measured switching speed of the high-power RF MEMS switched capacitor with and without holes in the beam.

## 5.5 Summary

This chapter presents an RF MEMS switched capacitor with 10.4-11 W of power handling capabilities at 10 GHz under hot switching conditions. This power-handling is achieved with a reasonably low ( $< 30$  V) pull-in voltage. The switch has a capacitance ratio of  $C_r = 5.7$ , which can be increased to 10-11 with improved fabrication processes. The circular switch has pull-in voltage slope of  $-112.5$  mV/ $^{\circ}$ C from 25-105 $^{\circ}$ C. The post-release profile of the switch shows  $< 0.1$   $\mu$ m of deflection compared to the pre-release profile. This switch is well suited for high-power tunable filters and impedance tuners.

**Table 5.4:** Summary of Power-Handling of RF-MEMS Switched Capacitors & Varactors.

<i>Switch/Author</i>	$C_{up}$ (pF)	$C_d$ (pF)	$C_r$	$V_p$ (V)	$P_{cold}$ (W)	$P_{hot}$ (W)	<i>Freq.</i> (GHz)
Toshiba QSC	1.9	5.5	2.89	21	$>5$	5	2
Y. lu	0.095	0.3	3.16	55	$>4$	4	10
C. Palego	0.06	0.425	7.08	115	$> 10$	10	3
D. Peroulis	0.04	0.8	20	—	$>5.5$	$\sim 0.8$	10
Raytheon	0.04	1.6	40	30	4-5	0.5-0.6	10
MIT-LL	0.008	1.2	150	40	10	1-1.7	10
Reines	0.055	0.312	5.7	24-28	$>10$	10.4-11	10

Chapter 5, in part, is mostly a reprint of the material as it appears in 24th IEEE International Conference on Micro-Electro Mechanical Systems, 2011. Isak Reines



and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

## Chapter 6

# Compact Low-Loss Tunable X-Band Bandstop Filter with Miniature RF-MEMS Switches

### 6.1 Introduction

Tunable filters are critical components in communication and radar systems and have the potential to replace switched-filter banks. Bandstop filters provide a high level of rejection over a limited bandwidth, while ideally exhibiting low pass-band loss so as to minimally impact the receiver sensitivity. They are also used to increase the isolation between the transmit and receive paths in high power systems.

The tuning element in planar filters can be realized with solid-state varactors [55], P-I-N diodes, ferro-electric varactors [13], or radio frequency micro-electromechanical systems (RF-MEMS). Solid state varactors have fast switching speeds ( $ns$ ) but suffer from loss and linearity issues at microwave frequencies [16]. RF-MEMS switches consume much less power compared to solid-state devices, exhibit low loss, and have excellent linearity and power handling (two-tone third-order intermodulation intercept point (IIP3)  $> 40$  dBm) [1]. The reliability of RF-MEMS devices has been steadily improving, making them a possible candidate for tunable filter applications.

There is little published work on RF-MEMS tunable notch filters: Adam *et al.* [56] previously demonstrated a 7.4-15.9 GHz RF-MEMS bandstop filter with rejection levels of  $< 10$  dB, and high pass-band loss ( $> 5$  dB below 5 GHz). Karim *et al.* [57]

reported an RF-MEMS bandstop filter with a tuning range from 17.3-19 GHz, and high pass-band loss ( $> 5$  dB above 25 GHz). Yan *et al.* [58] realized a 3-pole notch filter based on large deflection MEMS actuators with a center frequency of 6 GHz and a tuning range of only 500 MHz. Pillans *et al.* [59] reported a 3-pole 8.6-11.75 GHz RF-MEMS filter on a ceramic substrate with folded resonators, but  $\sim 2$  dB dips in  $S_{21}$  are observed at frequencies  $> 13$  GHz. Finally, excellent work was done in tunable absorptive notch filters [60], but this technique requires analog capacitance tuning to achieve exact phase cancellation which is challenging with RF-MEMS devices.

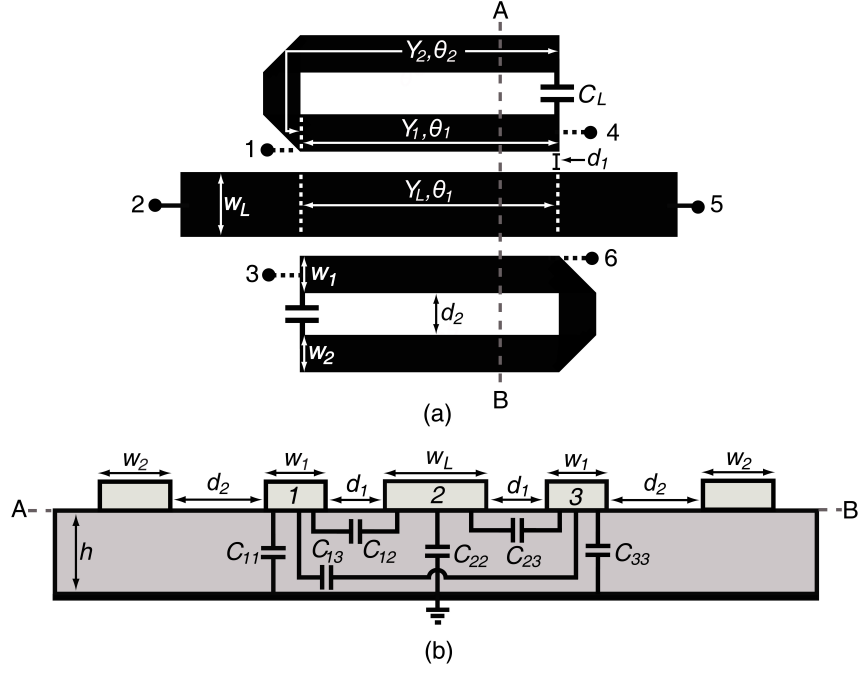
In this chapter, we present a compact low-loss 2-pole tunable X-band bandstop filter based on coupled folded  $\lambda/2$  resonators with capacitive loading. The filter results in high rejection levels ( $> 24$  dB) and low pass-band loss ( $< 0.8$  dB) from DC to 19.5 GHz [61]. The filter is fabricated with fixed interdigital capacitors, miniature RF-MEMS capacitive switches, and GaAs varactors, and the performance of these filters is compared (insertion loss, 1-dB compression point (P-1dB), and IIP3). The notch filter design also includes, for the first time, an analytic solution for the effect of non-adjacent inter-resonator coupling.

## 6.2 Bandstop Filter Design

### 6.2.1 Admittance Matrix for Three-Coupled Lines

The proposed bandstop filter is based on a microstrip-line which is coupled to two folded  $\lambda/2$  resonators loaded with a capacitance  $C_L$  (Fig. 6.1). To minimize the filter size and pass-band insertion loss, one resonator is flipped  $180^\circ$  to allow the inverter to be placed compactly between the resonators. As a result, inter-resonator coupling will occur and is accounted for in the design. Also, this topology increases the inductive coupling between the resonators, resulting in a shift of some of the infinite transmission zeros of the all-pole network from DC to infinity which increases the slope of the upper stop-band. In the filter design only the coupling between microstrip lines 1, 2, and 3 shown in Fig. 1b are considered since  $d_2 \gg d_1$ .

The capacitance distribution matrix  $[C]$  for three coupled-lines above a ground plane (Fig. 6.1b), is extracted using an electro-magnetic (EM) solver [54] and is given



**Figure 6.1:** Equivalent circuit model of the 2-pole bandstop filter (a), and filter cross-section with 3-coupled microstrip-lines and two un-coupled outer resonator sections (note:  $d_2 \gg d_1$  and figures are not to scale) (b).

by

$$[C] = \begin{bmatrix} C_{11} & -C_{12} & -C_{13} \\ -C_{21} & C_{22} & -C_{23} \\ -C_{31} & -C_{32} & C_{33} \end{bmatrix} \quad (6.1)$$

where  $[C]$  has units of capacitance per unit length (F/m).

The corresponding 6x6 admittance matrix for the lossless coupled lines of length  $\theta_1$  is given by [62]

$$[Y_c] = \frac{v_p}{j \tan(\theta_1)} \begin{bmatrix} [C] & -\sec(\theta_1)[C] \\ -\sec(\theta_1)[C] & [C] \end{bmatrix} \quad (6.2)$$

where  $v_p$  is the average phase velocity for the coupled-lines since  $w_1 \neq w_L$ .

### 6.2.2 Filter Admittance Matrix

The 2-port  $Y$ -parameters for an ideal series-connected microstrip line and capacitor  $C_L$ , are

$$Y_{L11} = \frac{jY_2 \sin(\theta_2) + j\omega C_L \cos(\theta_2)}{\cos(\theta_2) - Z_2 \omega C_L \sin(\theta_2)} \quad (6.3)$$

$$Y_{L12} = \frac{j\omega C_L}{Z_2 \omega C_L \sin(\theta_2) - \cos(\theta_2)} = Y_{L21} \quad (6.4)$$

$$Y_{L22} = \frac{j\omega C_L \cos(\theta_2)}{\cos(\theta_2) - Z_2 \omega C_L \sin(\theta_2)} \quad (6.5)$$

where  $Y_2$  and  $\theta_2$  are the admittance and electrical length of the un-coupled microstrip line, respectively. With the port definitions shown in Fig. 6.1, the matrix elements of  $[Y_c]$  corresponding to ports 1, 3, 4, and 6 are modified to include  $[Y_L]$ , and result in a 6x6 filter admittance matrix,  $[Y]$ . Next, ports 1, 3, 4, and 6 are open circuited (i.e.  $i_1=i_3=i_4=i_6=0$ ), and  $[Y]$  is reduced to a 2x2 matrix with

$$\begin{bmatrix} i_2 \\ i_5 \end{bmatrix} = \begin{bmatrix} Y_{X11} & Y_{X12} \\ Y_{X21} & Y_{X22} \end{bmatrix} \begin{bmatrix} v_2 \\ v_5 \end{bmatrix} \quad (6.6)$$

To facilitate the 6x6 matrix reduction let

$$[Y_v] = \begin{bmatrix} Y_{C11}+Y_{L11} & Y_{C13} & Y_{C14}+Y_{L12} & Y_{C16} \\ Y_{C31} & Y_{C33}+Y_{L22} & Y_{C34} & Y_{C36}+Y_{L21} \\ Y_{C41}+Y_{L21} & Y_{C43} & Y_{C44}+Y_{L22} & Y_{C46} \\ Y_{C61} & Y_{C63}+Y_{L21} & Y_{C65} & Y_{C66}+Y_{L11} \end{bmatrix} \quad (6.7)$$

and

$$[A] = [Y_v]^{-1} \quad (6.8)$$

The 2-port  $Y$ -parameters for the bandstop filter can now be expressed as

$$Y_{X11} = QY_{C21} + Y_{C22} + SY_{C23} + UY_{C24} + XY_{C26} \quad (6.9)$$

$$Y_{X12} = RY_{C21} + TY_{C23} + VY_{C24} + Y_{C25} + Y_a Y_{C26} \quad (6.10)$$

$$Y_{X21} = QY_{C51} + Y_{C52} + SY_{C53} + UY_{C54} + XY_{C56} \quad (6.11)$$

$$Y_{X22} = RY_{C51} + TY_{C53} + VY_{C54} + Y_{C55} + Y_a Y_{C56} \quad (6.12)$$

where

$$Q = -[A_{11}Y_{C_{12}} + A_{12}Y_{C_{32}} + A_{13}Y_{C_{42}} + A_{14}Y_{C_{62}}]$$

$$R = -[A_{11}Y_{C_{15}} + A_{12}Y_{C_{35}} + A_{13}Y_{C_{45}} + A_{14}Y_{C_{65}}]$$

$$S = -[A_{21}Y_{C_{12}} + A_{22}Y_{C_{32}} + A_{23}Y_{C_{42}} + A_{24}Y_{C_{62}}]$$

$$T = -[A_{21}Y_{C_{15}} + A_{22}Y_{C_{35}} + A_{23}Y_{C_{45}} + A_{24}Y_{C_{65}}]$$

$$U = -[A_{31}Y_{C_{12}} + A_{32}Y_{C_{32}} + A_{33}Y_{C_{42}} + A_{34}Y_{C_{62}}]$$

$$V = -[A_{31}Y_{C_{15}} + A_{32}Y_{C_{35}} + A_{33}Y_{C_{45}} + A_{34}Y_{C_{65}}]$$

$$X = -[A_{41}Y_{C_{12}} + A_{42}Y_{C_{32}} + A_{43}Y_{C_{42}} + A_{44}Y_{C_{62}}]$$

$$Y_a = -[A_{41}Y_{C_{15}} + A_{42}Y_{C_{35}} + A_{43}Y_{C_{45}} + A_{44}Y_{C_{65}}]$$

### 6.2.3 Design Procedure

The admittance matrix  $[Y_X]$ , given in (9)-(12), represents a bandstop filter centered at  $\omega_0$  with fractional bandwidth  $\Delta$  provided that

$$\text{Im}[Z_r(\omega_0)] = 0 \quad (6.13)$$

$$x = \frac{Z_0}{\Delta g_1} \quad (6.14)$$

$$\text{Im}\left[\frac{Z_x}{x}\right] = k_{12} = \Delta\sqrt{g_1 g_2} \quad (6.15)$$

where

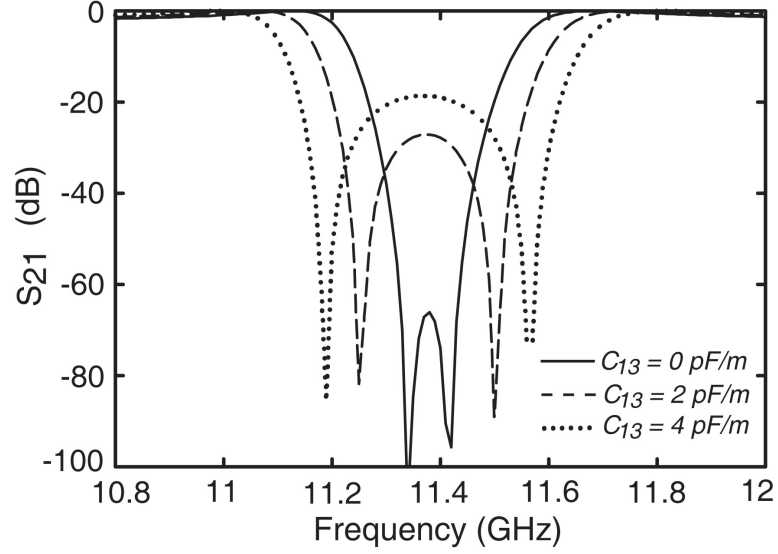
$$Z_r = \frac{1}{Y_{X11}} \quad (6.16)$$

$$Z_x = \frac{1}{Y_{X21}} \quad (6.17)$$

$$x = \frac{\omega_0}{2} \frac{\partial(\text{Im}(Z_r))}{\partial\omega} \quad (6.18)$$

The design procedure is to find the static capacitances given in (1) and the corresponding electrical lengths ( $\theta_1$ , and  $\theta_2$ ) that satisfy the resonance, scaling, and coupling conditions in (13)-(15). The inter-resonator coupling  $C_{13}$  is a by-product of  $C_{12}$  which must be included in the design because it impacts the notch filter performance. A significant increase in the filter bandwidth and diminishing rejection levels occur even for  $C_{13} = 2$  pF/m (Fig. 6.2).

The self-capacitance  $C_{22}$  can be set by choosing  $Y_L = 1/50$  mho and  $\theta_1$  should be  $\sim\lambda/4$ . The overall resonator length ( $\theta_1+\theta_2$ ) is chosen to be  $\sim\lambda/2$  and this sets the

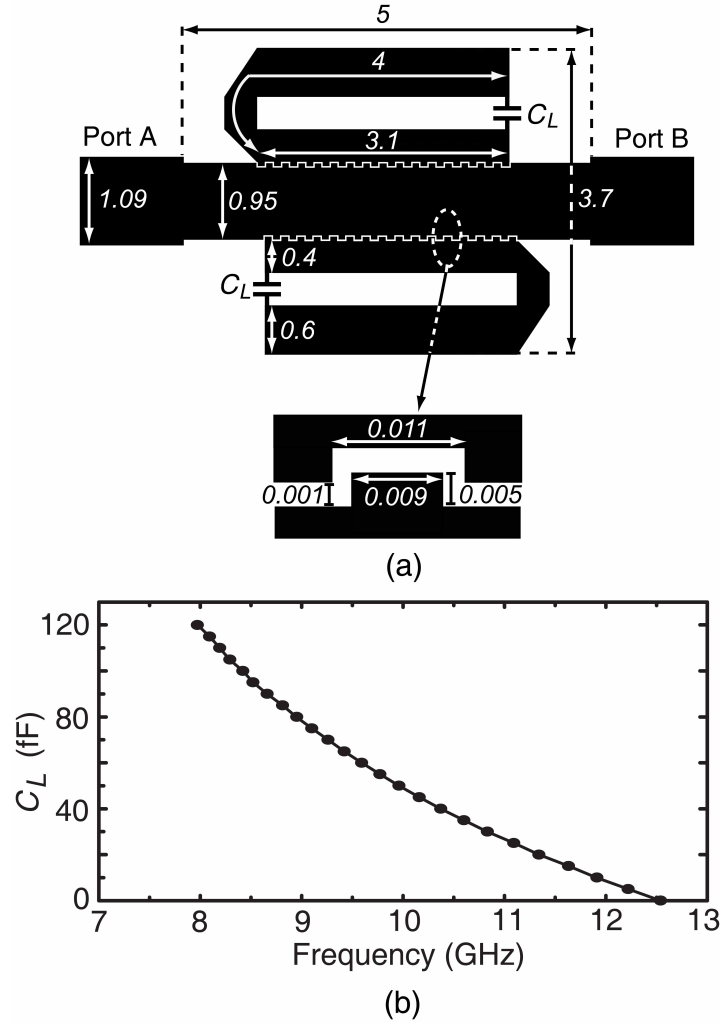


**Figure 6.2:** Calculated filter response showing the effect of inter-resonator coupling  $C_{13}$  ( $C_{11} = 206$  pF/m,  $C_{22} = 115$  pF/m,  $C_{12} = 40$  pF/m,  $C_L = 20$  fF,  $L_1 = 3110$   $\mu\text{m}$ ,  $L_2 = 3700$   $\mu\text{m}$ ,  $\epsilon_{\text{reff}} = 2.88$ ).

highest operating frequency and results in a small loading capacitance  $C_L$ .  $C_{11}$  ( $C_{33}$ ),  $C_{12}$ , and  $C_L$  can be determined by iteratively choosing values that satisfy (13)-(15). Equation (13) is mostly dependent on  $C_{11}$  and  $Y_2$  while equation (15) depends heavily on  $C_{12}$ . Equation (14) depends on both  $C_{11}$  and  $C_{12}$ . In general  $Y_2(w_2)$  is chosen to be greater than  $Y_1(w_1)$  so as to maximize the microstrip resonator  $Q$ , and to increase  $C_{12}$ ,  $Y_1 < Y_L$  ( $w_1 < w_L$ ). After finding the design parameters the physical dimensions ( $w_L$ ,  $w_1$ ,  $w_2$ , and  $d$ ) can be determined.

The lossless bandstop filter admittance matrix  $[Y_X]$  does not include the effects of the two resonator bends and assumes a single phase velocity for all the microstrip-lines, which is not the case since  $w_1 \neq w_L$ . Therefore, a full-wave simulation is performed in SONNET [41] for the final design, and the resulting S-parameters are imported into ADS [63], and loaded with  $C_L$ . The pole splitting is reduced in the final design due to the even and odd-mode phase velocity difference in the coupling which is shown in full-wave simulations. For this design, and in order to increase the coupling coefficient,  $k_{12}$ , while still keeping a realizable coupling gap, the coupling section of each resonator is interdigitated to obtain a higher capacitance per unit length. The final dimensions are obtained by iterating between Sonnet simulations and  $C_L$  loading values.

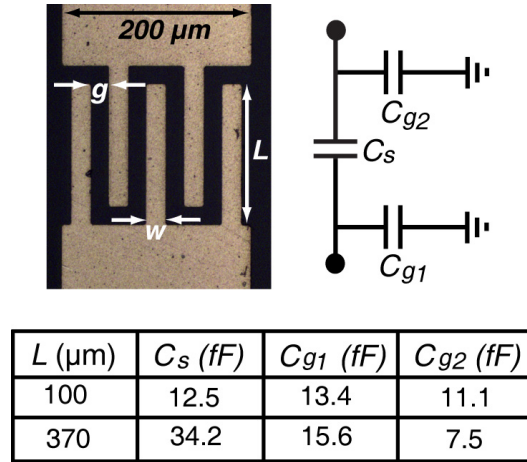
### 6.3 Fixed Frequency Filter



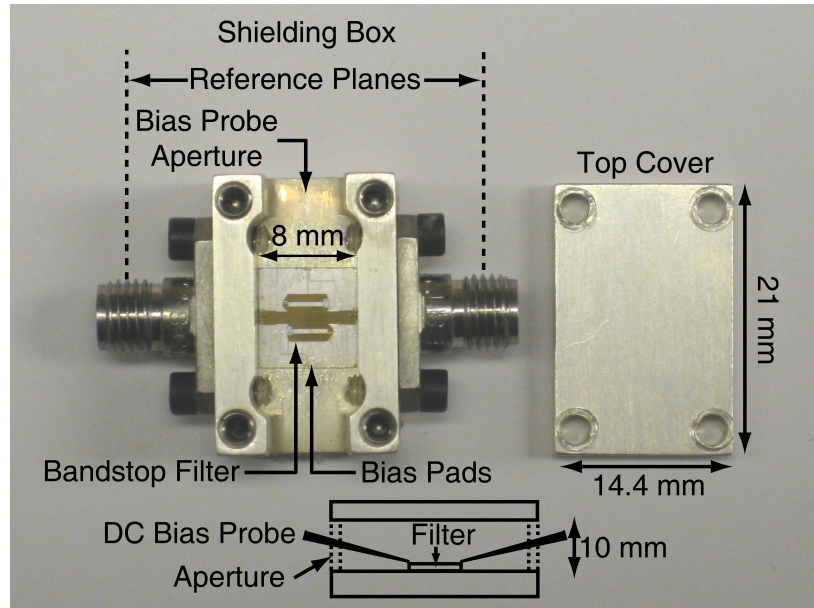
**Figure 6.3:** 2-pole bandstop filter on quartz substrate with all dimensions in mm (a), and the simulated filter center frequency versus ideal loading capacitance (b).

The 2-pole bandstop filter is first implemented with fixed interdigital loading capacitors on a low-loss quartz substrate ( $h = 508 \mu\text{m}$ ,  $\epsilon_r = 3.78$ ,  $\tan\delta = 0.0001$ ) (Fig. 6.3a). Full-wave simulations show that a  $C_L$  of 20-80 fF results in a resonant frequency of 8.95-11.34 GHz (Fig. 6.3b). The microstrip-line width  $w_L$  is slightly inductive ( $Z_L = 54 \Omega$ ) to compensate for the extra capacitance from the interdigitated coupling sections. The equivalent circuit model and corresponding dimensions for the two interdigital capacitors are presented in Fig. 6.4. The model has a  $200 \mu\text{m}$  port width, which is taken into account since it reduces the effective resonator length.

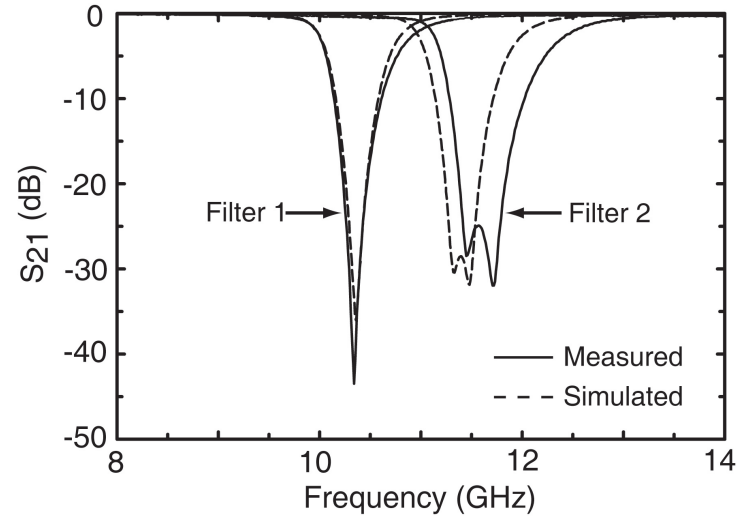




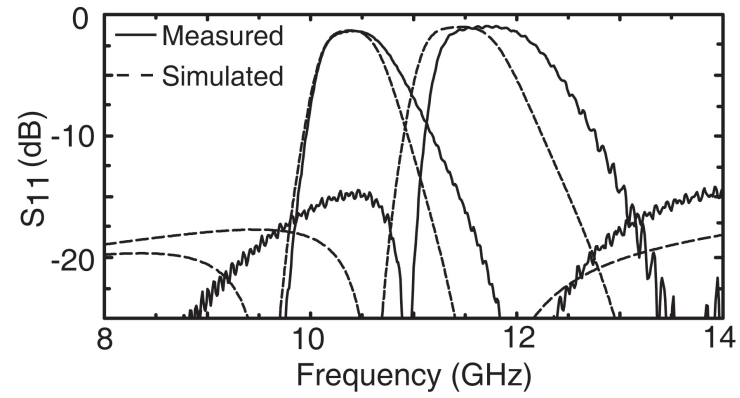
**Figure 6.4:** Micrograph of fabricated interdigital loading capacitor, equivalent circuit model, and simulated capacitance values ( $w = g = 20\ \mu\text{m}$ ).



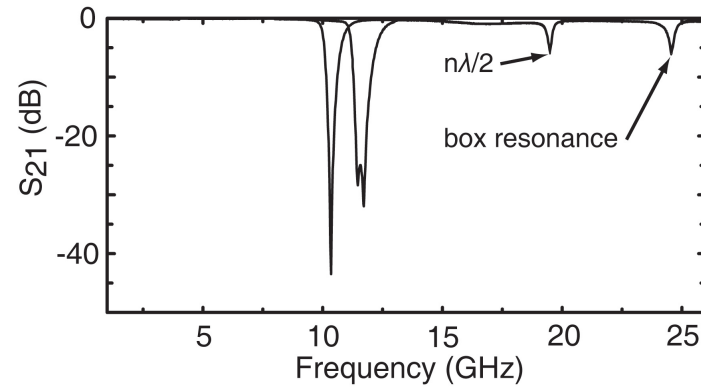
**Figure 6.5:** Shielding box used for the fixed and tunable bandstop filters



(a)



(b)



(c)

**Figure 6.6:** Measured and simulated S-parameters for the interdigital capacitor loaded bandstop filter (a)  $S_{21}$ , (b)  $S_{11}$  (c) spurious response.

The microstrip-lines and interdigital capacitors are electroplated with 4  $\mu\text{m}$  of gold. The filters are placed in a metal shielding box to reduce radiation losses (Fig. 6.5). A pressure contact is used between the SMA connector and microstrip-line, to facilitate multiple chip testing. The shielding box has openings on the north and south sides to accommodate DC-probing access for the tunable filter (see section zzz).

The fixed filters are measured using an E8364B network analyzer with the reference planes defined at the SMA connectors. The measured center frequencies are 11.57 and 10.34 GHz, with rejection levels of 24.9 and 43.8 dB, respectively (Fig. 6.6(a)). The -20 dB and -10 dB absolute bandwidths are 452 and 235 MHz, and 741 and 471 MHz, respectively. In the pass-band, the measured insertion loss is 0.17-0.19 dB at 7 GHz, and 0.34-0.61 dB at 13 GHz for the two filters, respectively. The return loss in the pass-band is better than 14 dB for both filters.

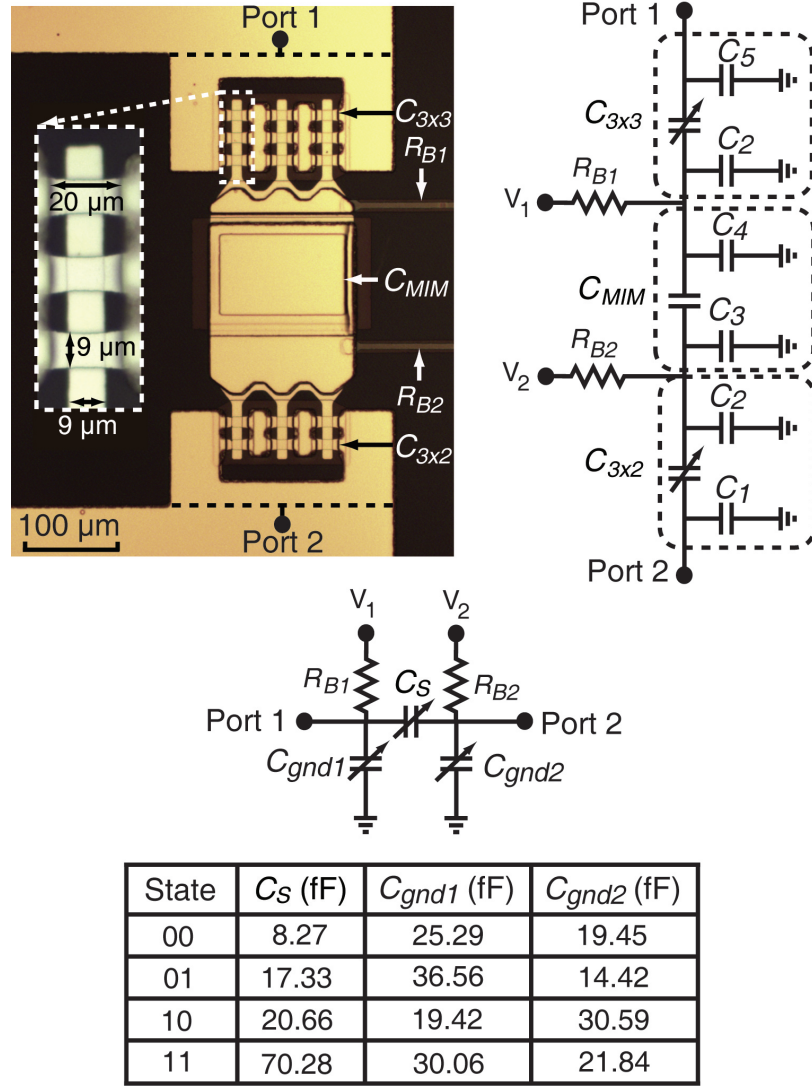
The fitted resonator quality factor is 150 and 130 at 11.57 and 10.34 GHz, respectively. Good agreement is shown between measurement and simulations at 10.34 GHz, and a 157 MHz frequency shift is observed for the higher frequency filter. This can be explained by a difference in  $C_L$  of only 3 fF from simulation. The spurious response of the filter shows the expected  $n\lambda/2$  resonance, and an additional box resonance at 24.56 GHz (Fig. 6.6(c)).

## 6.4 Miniature RF-MEMS Loaded Bandstop Filter

Miniature RF-MEMS switches are an ideal candidate for the X-Band bandstop filter due to the required small values of  $C_L$  as seen in Fig. 6.3b [6]. Each individual miniature RF-MEMS capacitive switch has a typical up and down-state capacitance of  $C_u = 4$  fF,  $C_d = 20$ -30 fF ( $C_r = 5$ -7.5), and the devices can be arrayed to achieve larger capacitance values. Several ( $> 5$ ) miniature RF-MEMS arrays have been tested with 100 mW of RF power at 10 GHz to  $> 60$  billion cycles with no failures.

### 6.4.1 RF-MEMS Loading Network

The proposed 4-state loading network is comprised of back-to-back 3x2 and 3x3 miniature RF-MEMS arrays, which are separated by a 3.65 pF ( $X = -j3.96 \Omega$  at 11 GHz) metal-insulator-metal (MIM) capacitor (Fig. 6.7). The MIM capacitor functions as a DC block to facilitate independent control of each switch array. The silicon-chrome bias-lines have a sheet resistance of 2-5 k $\Omega$ /sq and are placed orthogonally to the high



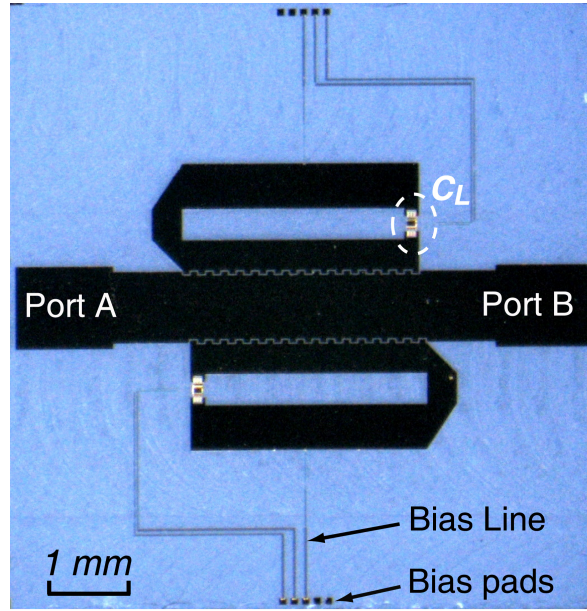
**Figure 6.7:** Micrograph of the 4-state miniature RF-MEMS loading network, and the equivalent capacitance circuit model with associated values. The inset shows a 1x3 miniature RF-MEMS network.

electric field in the resonator to reduce the RF leakage [49]. The bias-lines have an initial width of  $5 \mu\text{m}$  next to the tuner network to minimize the amount of RF-current generated on the line. To avoid accruing too large of a bias resistance, which could impact the switching speed, the bias-line width is gradually increased to from  $5$  to  $40 \mu\text{m}$  at the bias pads. The total bias resistance is 200-500 k $\Omega$ .

The equivalent circuit model for the 4-state RF-MEMS tuner network is shown in Fig. 6.7. Full-wave simulations of the individual switch arrays and MIM capacitor

were used to extract the associated series and shunt capacitances. The resulting loading capacitances of the tuner network versus switch state are given in Fig. 6.7. It should be noted that the parasitic shunt capacitances from the open-ended microstrip resonator and MIM capacitor function to reduce the overall capacitance ratio of the MEMS tuner network.

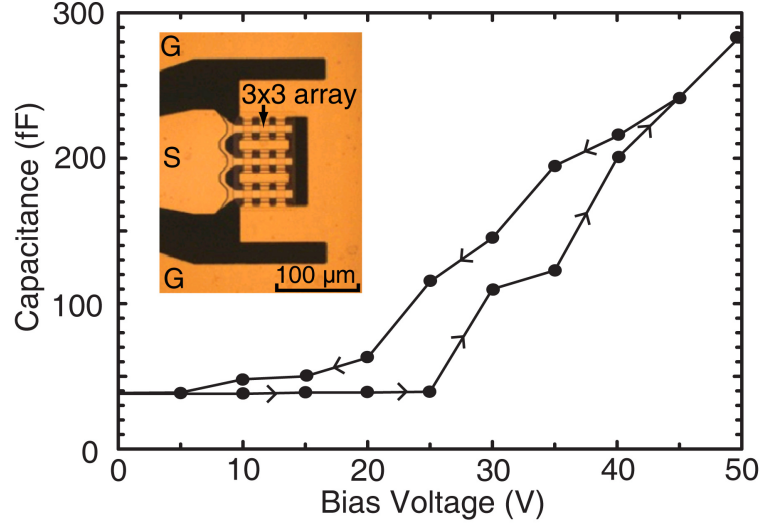
#### 6.4.2 Fabrication and Measurements



**Figure 6.8:** Fabricated RF-MEMS tunable bandstop filter on a quartz substrate.

The miniature MEMS devices are fabricated on a  $508\ \mu\text{m}$  thick quartz substrate using an RF-MEMS process developed at the University of California, San Diego [6]. For this fabrication run, the average gold bottom metal and silicon nitride dielectric thicknesses were  $1850\ \text{\AA}$  and  $1400\ \text{\AA}$ , respectively. The sacrificial layer thickness was  $0.3\ \mu\text{m}$  with a  $\pm 0.05\ \mu\text{m}$  variation across the 3" wafer. The average total thickness of the Ti/Au/Ti mechanical beam was  $0.395\ \mu\text{m}$ , with a variation of  $\pm 0.025\ \mu\text{m}$  across the wafer. In order to increase the spring constant of the beam, the  $200\ \text{\AA}$  Ti adhesion layer was left on both the top and bottom side of the gold beam resulting in an residual in-plane stress of  $\sim 150\ \text{MPa}$ . The microstrip-lines are electro-plated with  $4.5\ \mu\text{m}$  of gold. Lastly, the filters are diced before the miniature MEMS devices are released using a  $\text{CO}_2$  critical point dryer. The final dimensions of the miniature MEMS device, measured using

a white light interferometer, show a mechanical beam and bottom electrode width of  $9\ \mu\text{m}$ , with a beam length of  $20\ \mu\text{m}$ . An optical picture of the fabricated bandstop filter is shown in Fig. 6.8.

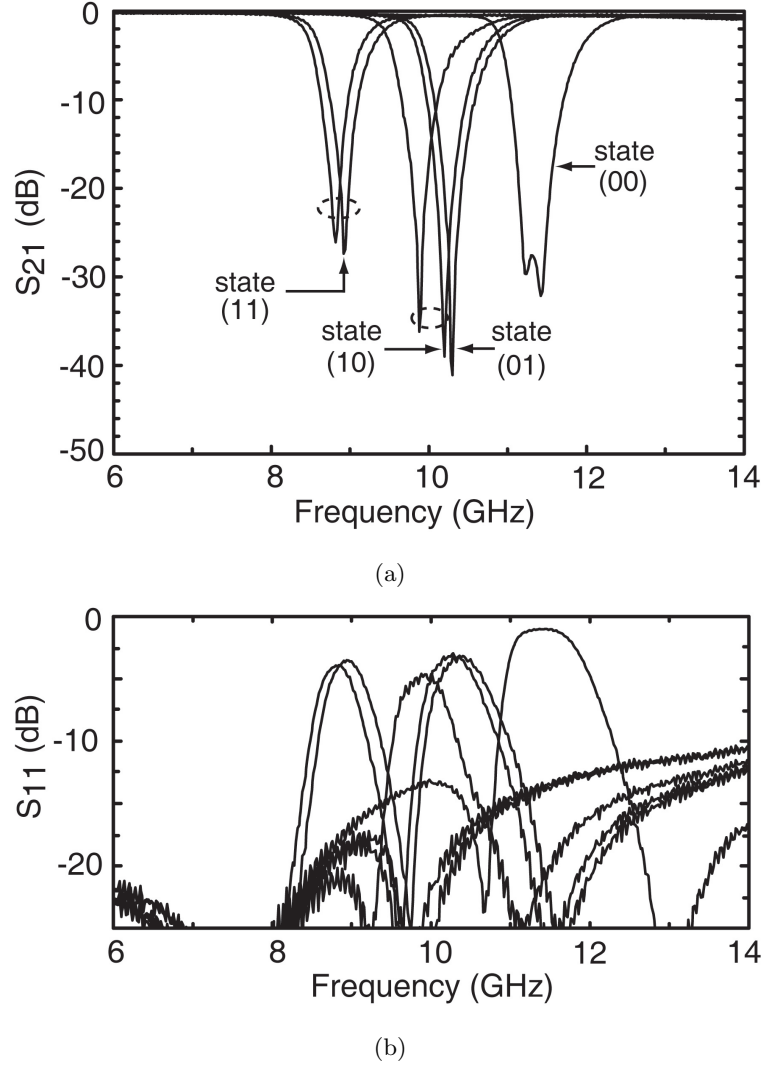


**Figure 6.9:** Micrograph and measured C-V curve of the miniature RF-MEMS 3x3 capacitive switch array.

The measured C-V curve of a 1-port 3x3 miniature MEMS array is obtained using a 10 kHz bi-polar waveform to reduce the effects of dielectric charging (Fig. 6.9). The respective up-and-down-state capacitances are 38 fF and 285 fF ( $C_r = 7.5$ ). Some analog tuning is observed after the individual bridges are pulled-down, which occurs as the overlapping contact area increases with applied voltage. The measured gap height and beam thickness of this particular device are  $0.25\ \mu\text{m}$  and  $0.37\ \mu\text{m}$ , respectively. The measured pull-down voltage is  $\sim 30\ \text{V}$ , which corresponds to a spring constant of  $\sim 156\ \text{N/m}$  [1]. The simulated mechanical resonance frequency and switching time ( $V/V_p = 1.25$ ) are 2.57 MHz and 38 ns, respectively [6].

The measured S-parameters for the X-band tunable filter are shown in Fig. 6.10(a)-(b). The filter tunes from 11.34 GHz (up-state position) to 8.82 (down-state position with analog tuning), and has middle state positions at 10.2 (01 state) and 10.3 GHz (10 state), respectively. The filter rejection is 27-41 dB depending on the state. The effect of analog tuning (5-10 V above  $V_p$ ) is also demonstrated in state (11) (all-down) and state (10) and allows further tuning of the rejection frequency. The pass-band insertion loss, including the SMA connector loss, is between 0.15-0.24 dB, and 0.4-0.71

dB, at 7 GHz and 13 GHz, respectively, and can further be improved by epoxying the SMA connector to the microstrip line (Table 6.1). The filter is well matched with  $S_{11}$  and  $S_{22} < -11$  dB in the pass-band.

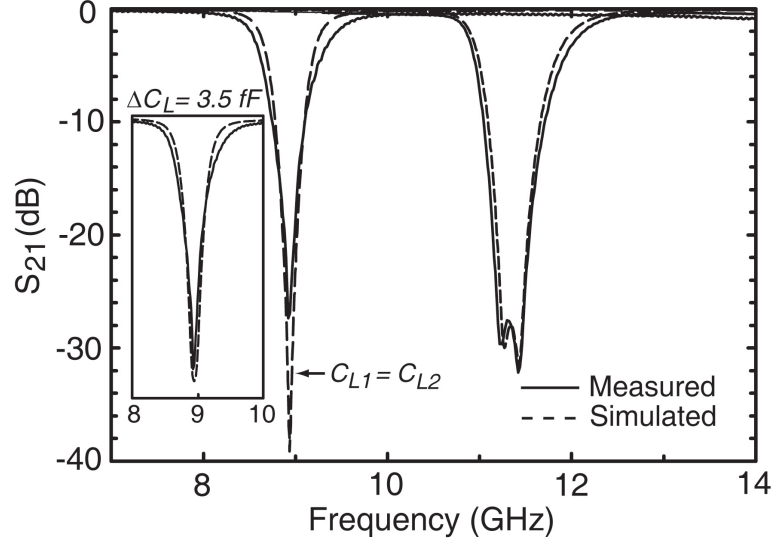


**Figure 6.10:** Measured S-parameters for the miniature RF-MEMS tunable filter, (a)  $S_{21}$ , (b)  $S_{11}$ .

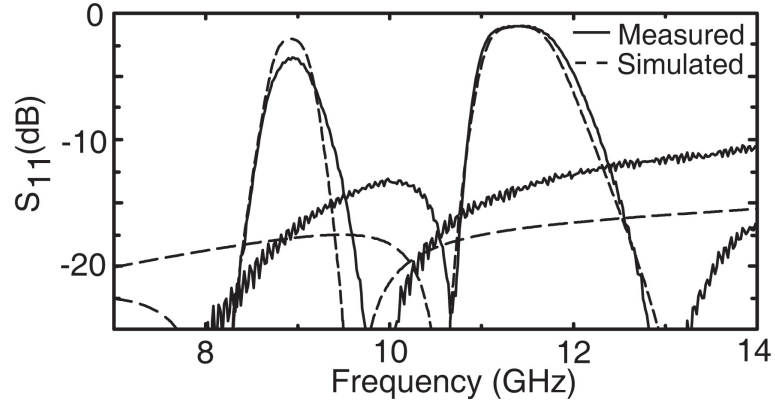
The fitted resonator quality factor is 135 at 11.34 GHz and 60 at 8.82 GHz. Full-wave simulations of a weakly coupled resonator with an ideal loading capacitor, show that the resonator  $Q$  drops from 230 to 115 at 11 GHz for a bias-line resistance of 100 k $\Omega$ /sq and 1 k $\Omega$ /sq, respectively. The resonator quality factor can be improved in future designs by increasing the bias-line sheet resistance to  $> 10$  k $\Omega$ /sq and by increasing the thickness of the thin 1850 Å bottom metal. The exact loading capacitance values



of the switches varies across the wafer and therefore a fitted silicon nitride dielectric permittivity of  $\epsilon_{ref} = 3.45$  is used, and shows good agreement with the measured filter response (Fig. 6.11(a)-(b)). The measured filter rejection level at 8.92 GHz is  $\sim 11$  dB less than simulated due to a non-symmetric loading capacitance of  $\Delta C_L = 3.5$  fF. The difference in return loss from simulations is due to the non-ideal connection between the SMA connector and microstrip line.



(a)



(b)

**Figure 6.11:** Measured and simulated S-parameters of the miniature RF-MEMS loaded filter using a fitted dielectric permittivity of  $\epsilon_{ref} = 3.45$  for states (00) and (11) (a)  $S_{21}$ , (b)  $S_{11}$ .



**Table 6.1:** Measured States of the RF MEMS Tunable Filter.

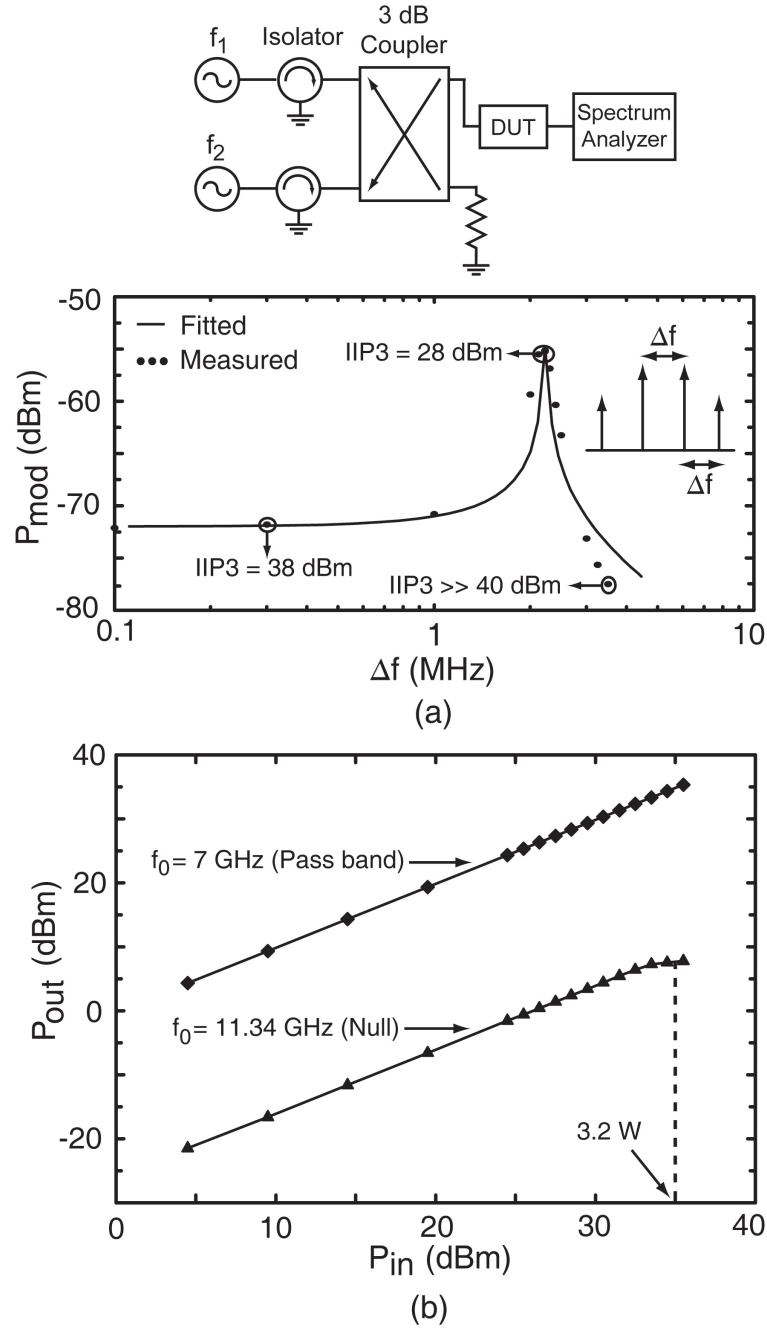
<i>State</i>	(00)	(01)	(10)	(11)
$f_0$ (GHz)	11.34	10.30	10.2	8.92
Rejection (dB)	27.57	41.09	39.01	27.37
B.W. <sub>-10dB</sub> (MHz, %)	665, 5.88	520, 5.05	499, 4.89	354, 3.97
B.W. <sub>-20dB</sub> (MHz, %)	397, 3.51	215, 2.09	220, 2.16	106, 1.18
I.L. at 7 GHz (dB)	0.17	0.15	0.15	0.27
I.L. at 13 GHz (dB)	0.40	0.56	0.51	0.71

### 6.4.3 Non-Linear Measurements

When an RF-MEMS capacitive switch is subject to an incident RF power, an electrostatic force is exerted on the mechanical beam which is  $\propto V_{rms}^2$ . For low voltages, this force modulates the switch capacitance and creates non-linear small-signal distortion. For two incident signals at  $\omega_1$  and  $\omega_2$ , where  $\omega_1 - \omega_2 \ll \omega_m$  ( $\omega_m$  is the mechanical resonance frequency), intermodulation components occur at  $2f_1 - f_2$  and  $2f_2 - f_1$  that can be measured with the experimental setup shown in Fig. 6.12(a) [18].

The non-linear measurements are done at the highest frequency state where all of the MEMS switches are in the up-state position and with the highest filter  $Q$ , and this results in the worst IM3 products. The IIP3 of the filter is measured versus the difference frequency  $\Delta f$ , and results in IIP3 > 37 dBm for  $\Delta f < f_m$ . When  $\Delta f = f_m$  the IIP3 is minimum at 28.3 dBm, and for  $\Delta f > f_m$  the IIP3 level increases at 20 dB/decade and is  $\gg 45$  dBm for  $\Delta f \gg 3$  MHz. The IIP3 measurements in the pass-band and at the -10 dB points on the null were limited by the measurement setup and are > 45 dBm. The intermodulation power shows a mechanical resonance frequency and fitted mechanical quality factor of 2.25 MHz and 7.07, respectively (Fig. 6.12(a)), which agree well with simulations.

The measured input P-1dB of the filter shows that the filter can handle 35 dBm of RF power before self-actuation of the miniature MEMS device occurs (Fig. 6.12(b)). The output power decreases at the P-1dB point due to an increase in the rejection level caused by a center frequency shift of  $\sim 80$  MHz. With higher input power levels, the center frequency will continue to decrease causing the output power to increase as the null rejection diminishes. In the pass-band the P-1dB point was not observed for input power levels up to 35 dBm. Full-wave simulations show that an input power of 35 dBm will result in a  $V_{rms} = 60$  V across the 3x2 miniature array. Given the



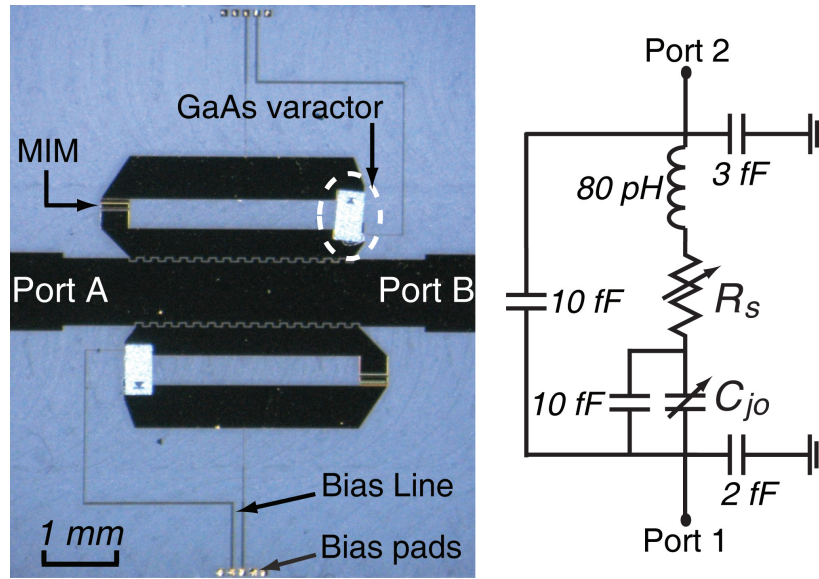
**Figure 6.12:** IIP3 measurement setup and measured mechanical resonance frequency ( $Q_m = 7.07$ ,  $f_m = 2.25$  MHz) of the miniature RF MEMS capacitive switch (a), and P-1dB of the RF-MEMS tunable filter in state (00) (b).

measured non-uniformities of the fabrication process, some miniature MEMS switches had a beam thickness of  $0.42 \mu\text{m}$  and a sacrificial gap of  $0.35 \mu\text{m}$ , which results in a spring constant and pull-down voltage of  $205 \text{ N/m}$  and  $60 \text{ V}$ , respectively, and thus the

35 dBm power handling. For a MEMS switch pull-in voltage of 37 V, simulations predict a corresponding input P-1dB of 30 dBm.

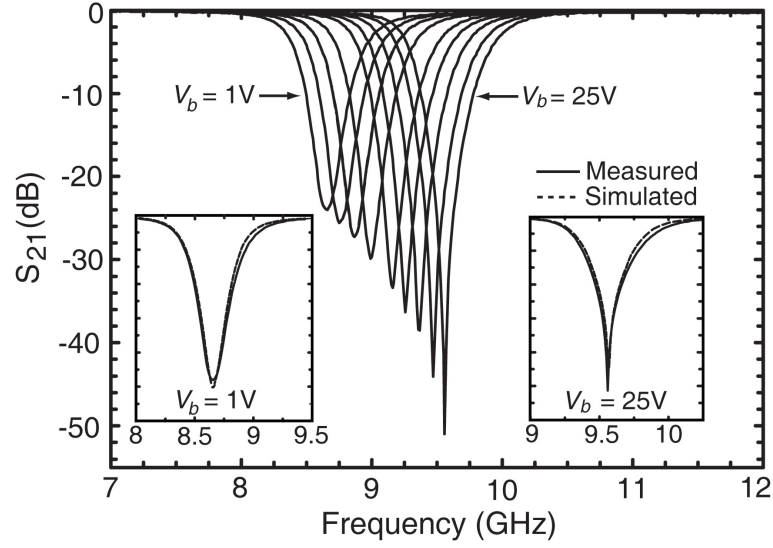
## 6.5 Varactor Loaded Bandstop Filter

The varactor loaded bandstop filter is fabricated on the same quartz wafer as the RF-MEMS tunable filter. To facilitate the varactor biasing, a 14.4 pF ( $X = -j1.23 \Omega$  at 9 GHz) MIM capacitor is placed between the two resonator bends (Fig. 6.13).  $C_L$  is realized using a GaAs flip-chip varactor diode (M\A-COM MA46H146) with a junction capacitance  $C_{jo} = 40$  fF at 4V, and a capacitance ratio of 2.1 from 0-25 V. The series resistance of the varactor is 3.2-1.75  $\Omega$  at 0-25 V. The varactor loaded filter is placed in the shielding box (see Fig. 6.5) and the resulting S-parameters are measured with reverse bias voltages ranging from 1-25 V (Fig. 6.14(a)-(b) and 6.2).

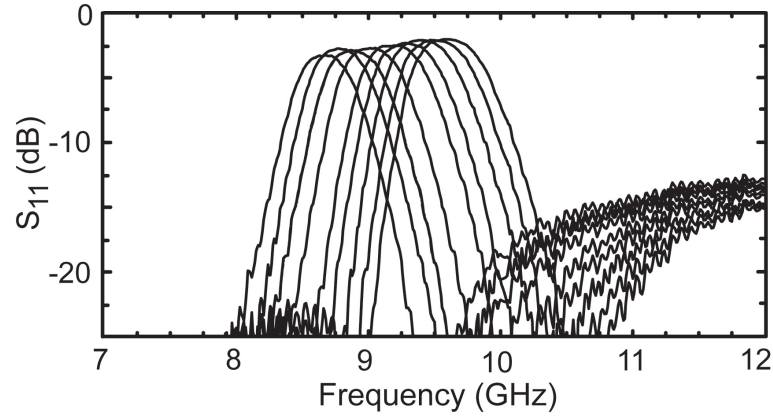


**Figure 6.13:** Fabricated varactor loaded bandstop filter on quartz with equivalent circuit model for the GaAs varactor ( $C_{jo} = 30$ -63 fF and  $R_s = 1.75$ -3.2  $\Omega$  from  $V_b = 0$ -25 V).

The measured filter response covers a tuning range of 8.66-9.56 GHz, with a null rejection and -20 dB bandwidth of 24-51 dB and 143-192 MHz, respectively. The return loss is better than -12 dB from 7-12 GHz in the pass-band. The rejection level of the bandstop filter diminishes at the lower frequencies due to a decreasing coupling coefficient. The fitted resonator quality factor is 90-55 at 9.56-8.66 GHz, and is dom-



(a)



(b)

**Figure 6.14:** Measured  $S_{21}$  of the varactor loaded bandstop filter for  $V_b$  1-25 V and simulation and measurement for  $V_b = 1$  and 25 V (a), and measured return loss (b).

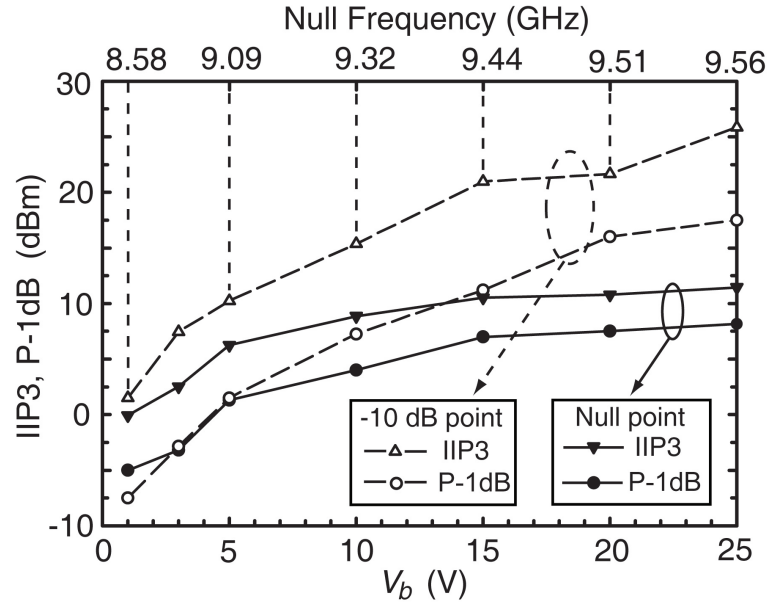
inated by a combination of varactor resistance and RF leakage through the bias lines. The measured and simulated filter responses show excellent agreement (Fig. 6.14(a)).

The IIP3 of the varactor loaded filter is measured using the setup shown in Fig. 12a with  $\Delta f = 1$  MHz, and results in an IIP3 at the null and -10 dB points of 0-11.45 dBm and 1.5-25.8 dBm, respectively, for voltages from 1-25 V (Fig. 6.15). Again, the pass-band IIP3 is  $> 45$  dBm which is the limit of the measurement setup. The measured input P-1dB at the null and -10 dB points are -5.0-8.2 dBm and -7.5-17.5 dBm, respectively, for voltages from 1-25 V. These are significantly lower than the

**Table 6.2:** Measured Response of the Varactor Tuned Tunable Filter.

$V_b(V)$	1	3	25
$f_0$ (GHz)	8.66	9.00	9.56
Rejection (dB)	24.02	29.90	51.32
B.W. <sub>-10dB</sub> (MHz, %)	340, 3.93	361, 4.02	404, 4.23
B.W. <sub>-20dB</sub> (MHz, %)	143, 1.65	169, 1.88	192, 2.0
I.L. at 7GHz (dB)	0.15	0.13	0.10
I.L. at 13GHz (dB)	0.3	0.25	0.16

RF-MEMS implementation.



**Figure 6.15:** Measured IIP3 and P-1dB of the varactor loaded bandstop filter at the null and -10 dB points versus reverse bias voltage ( $\Delta f = 1$  MHz for the IIP3 measurements).

## 6.6 Summary

A compact low-loss 2-pole X-Band tunable bandstop filter was designed, fabricated and measured with fixed interdigital capacitors, miniature RF-MEMS capacitive switches, and GaAs varactors. Non-linear measurements performed at the filter null with  $\Delta f = 1$  MHz show that the RF-MEMS loaded filter results in  $> 25$  dBm higher IIP3 and P-1dB, compared to the GaAs varactor loaded filter. In particular, the RF-MEMS tunable notch filter can handle up to 30-35 dBm of RF power at the null point and

this provides significant protection to the proceeding low noise amplifier. In the case of the RF-MEMS filter, the fitted resonator  $Q$  is 135-60 from 11.34-8.82 GHz and can be maintained above 100 across the tuning range by using a 10 k $\Omega$ /sq bias line process. This compact filter topology results in low pass-band loss  $< 0.8$  dB from DC to the first spurious response at 19.5 GHz.

The filter tuning range is limited by the capacitance ratio of the tuning network and an RF-MEMS implementation can provide a much higher capacitance ratio ( $C_r = 7$ -20), than a GaAs varactor design ( $C_r = 2$ -3). Simulations show that 8-12 GHz tuning with a null rejection  $> 20$  dB can be obtained with  $C_r = 12$  ( $C_L = 10$ -120 fF) which is possible to achieve using an higher  $C_r$  MEMS device. Also, smaller capacitances can be realized with the miniature MEMS device (including all parasitics) which is imperative for X-band and Ku-band filters. This 2-pole filter topology can be extended to higher order designs having an even numbers of poles. Finer tuning resolution can be achieved in the RF-MEMS notch filter by placing an additional 4-state capacitive loading network closer to the short circuit point in the resonator.

Chapter 6 is mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques, May 2010. Isak Reines; Sang-June Park, and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.

# Chapter 7

## Conclusion and Future Work

### 7.1 Summary of Work

Chapter 2 of this thesis presents a thin-film aluminum RF MEMS switched capacitor that exhibits a significant reduction in sensitivity to in-plane bi-axial stress and stress changes versus temperature. The device is designed and built within the Raytheon RF MEMS process to result in  $C_{up} = 50$  fF, and  $C_d = 1$  pF ( $C_r = 20$ ). The switch is very robust versus ambient temperature with a pull-in voltage slope of only  $-55\text{mV}/^\circ\text{C}$  from  $-5$ - $95^\circ\text{C}$ , compared to  $-300\text{mV}/^\circ\text{C}$  for the standard Raytheon capacitive switch. The effects of device topography are discussed in this chapter and are shown to cause the variation in in up-state capacitance versus temperature ( $C_{up} = 43$ - $51$  fF from  $-5$ - $95^\circ\text{C}$ ). The device has a switching speed of  $< 10 \mu\text{s}$  at both  $25^\circ\text{C}$  and  $95^\circ\text{C}$ , and a down-state quality factor of  $Q_d = 85$  at  $3$  GHz.

The symmetry of the circular beam geometry facilitates low series-inductance NxM arrays which lead to very large capacitance values from  $300$  MHz to  $10$  GHz applications. The switch is tested under continuous RF power at  $10$  GHz and both simulations and measurements show that the non-uniform temperature distribution of the bridge under RF power causes a decreasing up-state capacitance and increasing spring constant. This combination results in a switch that does not suffer from self-actuation up to RF power levels of  $5.2$  W.

Chapter 3 is an extension of the work presented in Chapter 2 and shows the second generation of thin-film stress tolerant and temperature stable switched capacitors that are fabricated in the Raytheon RF MEMS process. Results show that if device

arraying is not required, that the symmetric “actuation tabs” should be removed to result in improved capacitance ratio and temperature stability. Without the tabs on this fabrication run, a pull-in voltage slope versus temperature of  $-22 \text{ mV}/^\circ\text{C}$  is achieved. This section also presents a smaller switch with  $C_{up} = 27 \text{ fF}$ , and  $C_d = 0.7 \text{ pF}$ , with a pull-in voltage slope of  $-28.7 \text{ mV}/^\circ\text{C}$ .

Chapter 4 demonstrates a cascadable RF MEMS switched capacitor for 0.1-2 GHz applications. These devices are fabricated at UCSD and have down-state capacitances ranging from 11.22 to 17.49 pF with associated impedances of 144-7  $\Omega$  and 91-4  $\Omega$  at 100-2000 MHz. The impedances are near ideal over a 20:1 frequency range due to the low-series inductance. The down-state Q is  $> 50$  in the VHF range.

Chapter 5 presents an RF MEMS switched capacitor that is designed to handle high-RF power levels ( $\sim 10 \text{ W}$ ). The switch is based on a temperature-stable circular beam, and the RF signal line is routed under the higher spring constant portion of the beam to result in improved restoring force and an increased RF self-actuation voltage. A separate DC bias electrode is used to allow reasonably low ( $< 30 \text{ V}$ ) pull-in voltages. The switched capacitor has an up-and-down state capacitance of  $C_{up} = 55 \text{ fF}$ , and  $C_d = 312 \text{ fF}$  ( $C_r = 5.7$ ), with simulations indicating that  $C_r$  can be increased to 10-11 with improved fabrication processes. The switched capacitor demonstrated 10.4-11W of power handling at 10 GHz under hot-switching conditions. In this design, capacitance density has been traded for power handling. The measured pull-in voltage slope is  $-112.5 \text{ mV}/^\circ\text{C}$  from 25-105 $^\circ\text{C}$ . Post release profile measurements show  $< 0.1 \mu\text{m}$  of beam deflection compared to the pre-release profile. With perforations in the beam, the switching time is  $< 13 \mu\text{s}$  for a 40 V bias. This switch is well suited for high-power tunable filters and impedance tuners.

Chapter 6 presents a compact low-loss 2-pole X-Band tunable bandstop filter that is designed and fabricated with both miniature RF MEMS capacitors and GaAs varactors. The MEMS loaded filter tunes from 11.34-8.82 GHz with a -20 dB rejection bandwidth of 1.18-3.51%, and a filter quality factor of 135-60, that can be maintained above 100 across the tuning range by using a 10 k $\Omega$ /sq bias line process. The varactor loaded filter tunes from 9.56-8.66 GHz with a -20 dB bandwidth of 1.65-2%, and a filter quality factor of 90-55. This compact filter results in low pass-band insertion loss  $< 0.8 \text{ dB}$  from DC to the first spurious response at 19.5 GHz. Non-linear measurements performed at the filter null with  $\Delta f = 1 \text{ MHz}$  show that the RF MEMS loaded filter



results in  $> 25$  dBm higher  $IIP_3$  and P-1 dB, compared to the GaAs varactor loaded filter. The RF MEMS loaded filter handles 30-35 dBm of RF power at the null point, compared to only -5-8 dBm for the varactor loaded filter, and this provides significant protection to the proceeding low noise amplifier.

The tuning range of the filter is limited by the capacitance ratio of the tuning network and an RF MEMS implementation can provide a higher capacitance ratio ( $C_r = 7-20$ ), than a GaAs varactor ( $C_r = 2-3$ ). With a  $C_r = 12$ , simulations show that this filter can tune from 8-12 GHz with  $> 20$  dB rejection. This 2-pole filter topology can be extended to higher order designs having an even number of poles. This chapter also presents an analytic solution for the effect of nonadjacent inter resonator coupling.

Appendix A presents the first suspended 3-pole RF MEMS tunable filter with a frequency coverage of 1.6-2.4 GHz. The filter results in an insertion loss of 1.34-3.03 dB over the tuning range with 3-dB bandwidth of 201-279 MHz, and a  $Q_u$  of 50-150.

Lastly Appendix B details the UCSD RF MEMS fabrication process on high-resistivity silicon.

## 7.2 Future Work

In this thesis, no significant reliability studies have been performed on the presented devices. Although the thin-film aluminum switch fabricated in the Raytheon process was tested up to 100M cycles without failure, it is of interest to rigorously study the long-term reliability of this switch (in a package) and to identify the possible failure mechanisms. It would also be useful to study the effects of elevated temperatures on the device reliability. With more time, the reliability of the high-power switch presented in Chapter 5 should be tested at both low and high power levels. Future improvements for this switch include using a different beam metal such as aluminum to reduce the effects of plastic deformations at elevated temperatures. It would also be of interest to employ this switch in a high power filter or impedance tuner to verify the performance gains in a real application.

# Appendix A

## 1.6-2.4 GHz RF MEMS Tunable 3-Pole Suspended Compline Filter

### A.1 Introduction

Low-loss tunable bandpass filters are crucial components in reconfigurable RF front-ends since they can replace bulky switched filter banks leading to reduced system size, weight, and complexity. Yttrium-iron-garnet (YIG) based tunable filters have demonstrated multi-octave bandwidths with very high  $Q$  but their power consumption, linearity, size, weight, switching speed (typically on the order of 10's ms), and cost are often drawbacks for successful system integration [12].

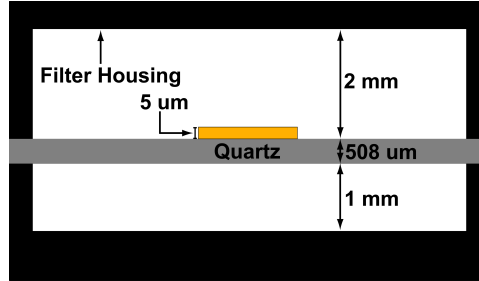
Miniaturized planar tunable filters based on either solid-state or MEMS varactors offer reduced size and weight, quicker switching speed, and a form that is conducive for batch fabrication and reduced cost. Although solid-state varactors have a switching speed that is not rivaled by MEMS, they suffer from loss and linearity issues at microwave frequencies [16]. MEMS switches do not consume any DC power and have excellent linearity ( $IIP3 > 40$  dBm) but will never achieve the high  $Q$  of YIG filters due to their planar nature [1].

Narrow-band filters ( $FBW \leq 5\%$ ) are often required in today's crowded frequency spectrum and these filters should exhibit a high unloaded quality factor to reduce the insertion loss. Some notable examples of RF MEMS tunable filters in the UHF to S bands are found in [64]- [66]. Although no direct mention of the  $Q_u$  was reported in these papers, it was estimated to be between 10-90 given the published filter responses.

In this section, we present a 3-pole tunable filter from 1.65 to 2.34 GHz with an absolute bandwidth of 201-279 MHz and a  $Q_u$  between 150-50. A suspended stripline media combined with low-loss RF MEMS were used to increase the filter Q.

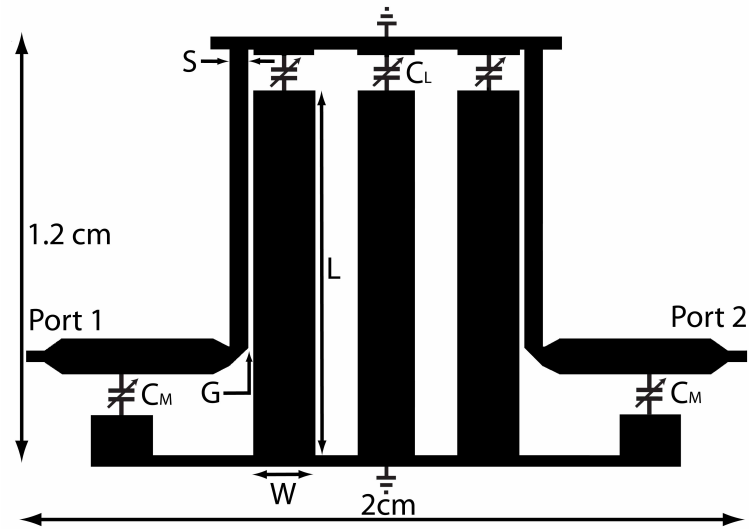
## A.2 Filter Design

A three-pole tunable filter was designed with the primary goals of continuous coverage of a band from 1.5 to 3 GHz with a channel bandwidth of 150-200 MHz and minimum insertion loss across the tuning range. A combline topology was selected due to its wideband tuning characteristics and reasonable capacitance loading [9]. Such a structure allows one to utilize low-loss transmission line media for the distributed resonators and coupling portions, a simplified method of tuning the structure using a quasi-lumped element MEMS tuning network, and a relatively well-behaved absolute bandwidth characteristic over the tuning range [67].

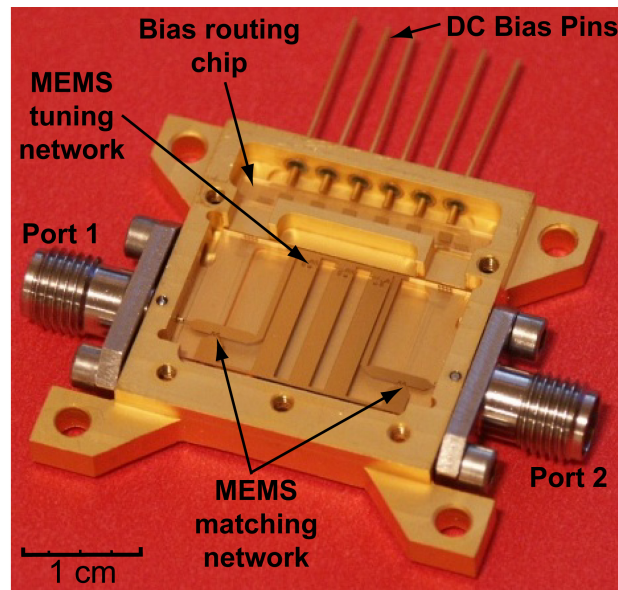


**Figure A.1:** Stripline cross section.

In order to maximize the Q of the resonant element and minimize the overall insertion loss, a suspended stripline medium was used. The stripline cross section consists of 1 mm air, 508  $\mu\text{m}$  fused silica, 5  $\mu\text{m}$  thick plated gold conductors and 2 mm air with gold plated stainless steel ground planes on either side (Figs. A.1). Unlike a conventional combline structure, the input/output feed-lines had to be brought in perpendicular to the resonant elements for connector clearance as well as the addition of the I/O tuner networks Fig. A.2. All grounding was achieved by wire bonding from the filter substrate to the housing. The biasing of the RF MEMS tuning elements was performed by DC package feed-throughs using a bias distribution network chip and wire bonded to the filter die (Fig. A.3). Once on the filter die, the biasing was routed using resistive lines to the individual RF MEMS switches.



**Figure A.2:** 3-pole combline filter with tunable load and matching capacitance networks.



**Figure A.3:** RF MEMS tunable 3-pole combline filter and the associated package. Note the bias distribution network for the RF MEMS switches which is shielded from the resonators using a separating wall.

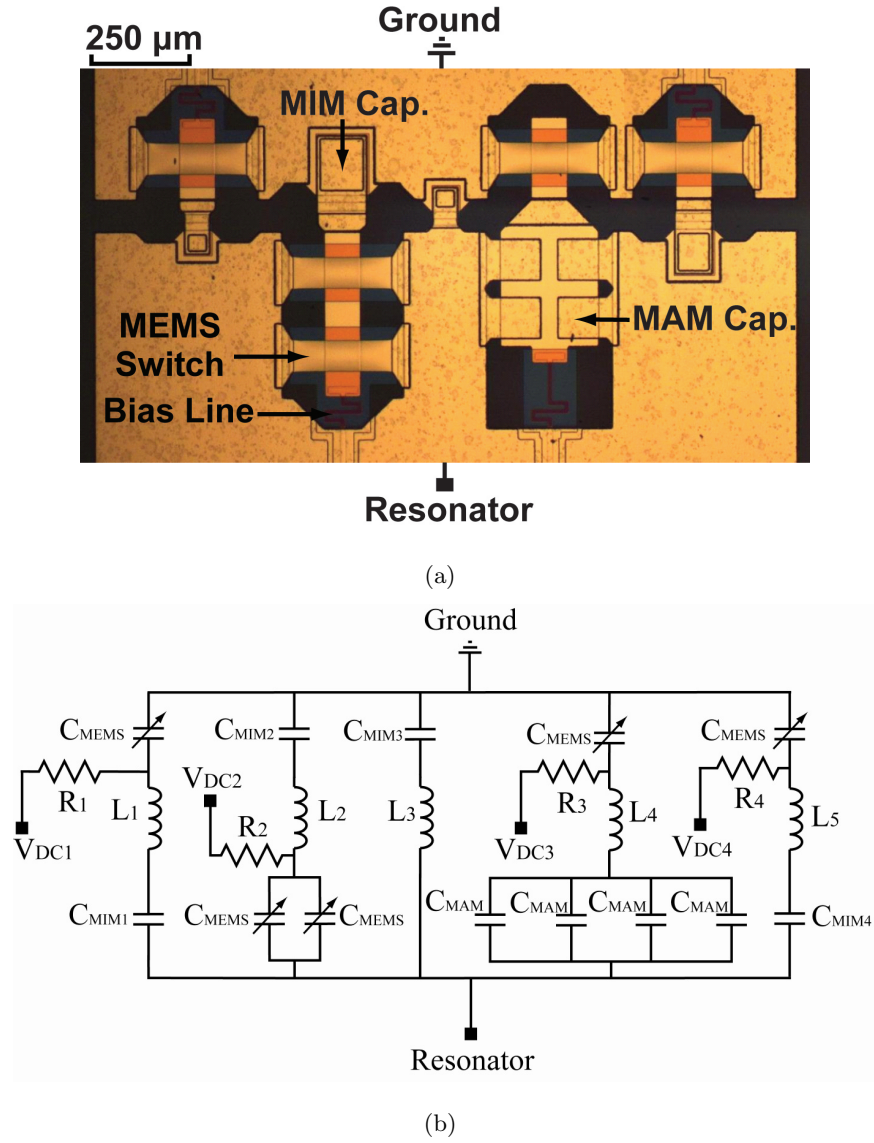
A trade-off study was performed between  $Q$ , tunability, realistic values for the capacitive tuner, and overall filter bandwidth vs. tuning when the resonator was designed. The resonant element width is 1.7 mm with a length of 10.6 mm resulting in an intrinsic stripline impedance of  $90\Omega$  and an electrical length of approximately  $20^\circ$  at 1.5 GHz and  $40^\circ$  at 3 GHz. In order to tune the resonators to different frequencies, a broadband RF MEMS tuning network is required. For a lumped-value capacitance at the open-end of the resonator, the resonant frequency is given by:

$$\omega_r = \frac{1}{\sqrt{Z_r \tan(\theta) C}} \quad (\text{A.1})$$

where  $Z_r$  is the intrinsic impedance of the distributed stripline,  $\theta$  is the effective electrical length of the stripline (note frequency dependence), and  $C$  is the total capacitance of the tuner network. Since the resonant frequency of the overall structure is very nonlinear with respect to the capacitance of the tuner, a simple binary tuner could not be employed and still achieve the desired coverage. Instead, the 4-bit tuner was optimized around a more nonlinear scaling of capacitors. An optimization was performed on the capacitance values to ensure a complete tuning range through the 1.5 to 3.0 GHz band. The resulting capacitive tuner has a fixed capacitance of 0.5 pF, and switchable fixed capacitance of 0.2, 0.5, 2.0, and 4.1 pF using the MEMS capacitive switches. The switch model used an on and off state capacitance of 0.04 and 1.4 pF, respectively. As shown in the equivalent circuit model two switches were required for the most significant bit due to its large size (Fig. A.4(a)-(b)).

While the internal structure of the combline filter has a very broadband response, the I/O admittance inverters have only a moderate bandwidth and limit the overall tuning range of the filter. To reduce the impact of the I/O inverters, a tuning network was implemented to extend the design to 1.5 GHz (without the tuning network, the filter return loss begins to degrade considerably at 1.9 GHz). The tunable matching network consists of a small section of high impedance transmission line and two shunt capacitors forming a simple LC match (Fig. A.5(a)). The equivalent circuit model for the 2-bit matching network is shown in Fig. A.5(b), and consists of shunt MEMS switches in series with fixed 1.5 pF MIM capacitors that result in capacitance values of 0.04/0.74/1.4 pF.

The simulated quality factor of the filter without any bias lines effects is greater than 290-390 from 1.5-3 GHz assuming no tuning element loss, a gold conductivity of  $3.1^7$  S/m for the 5  $\mu$  m lines, and a MIM resistance of 0.1  $\Omega$  (Fig. A.7). However, a

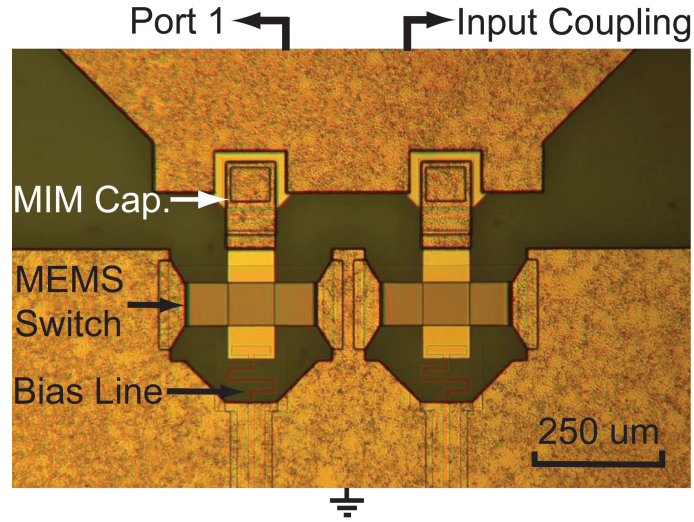


**Figure A.4:** (a) RF MEMS capacitance tuning network at the open-end of each resonator, (b) ideal equivalent circuit model.

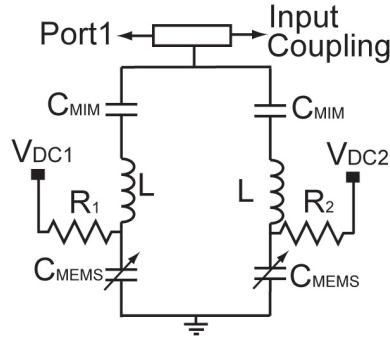
switch resistance of  $1\ \Omega$  drops the filter quality factor to 110 at 1.5 GHz, demonstrating the necessity for a low-loss tuning element.

### A.3 Fabrication

The tunable filter is fabricated on a  $508\ \mu\text{m}$  quartz substrate ( $\epsilon_r = 3.78$  and  $\tan\delta = 0.0001$ ) using a standard RF MEMS capacitive switch process developed at the



(a)

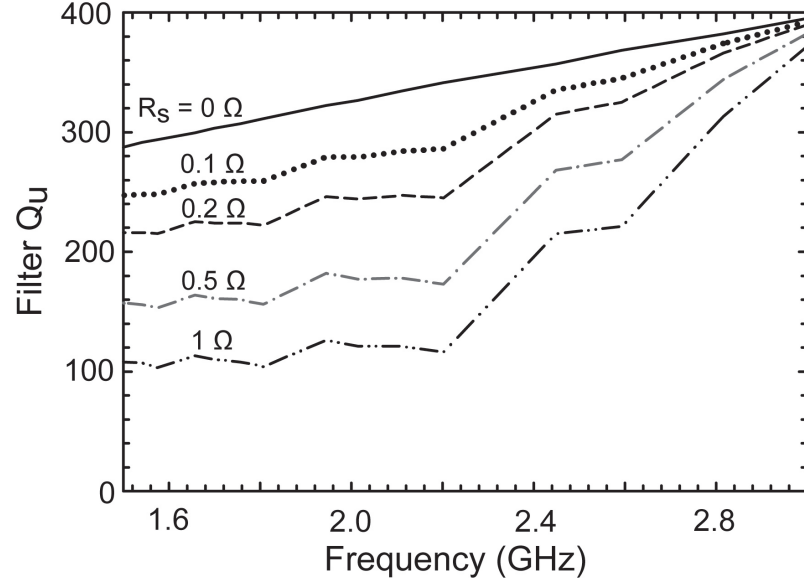


(b)

**Figure A.5:** (a) RF MEMS matching network, (b) ideal equivalent circuit model.

University of California San Diego. The bias lines for the capacitive switch are made of 1100 Å thick SiCr with a sheet resistance of 5 kΩ/sq. The 90 μm wide bottom electrode of the switch is a sputtered layer of Ti/Au (200/3000 Å). An 1800 Å thick layer of PECVD deposited Si<sub>3</sub>N<sub>4</sub> is patterned to form both the dielectric for the switch and the metal-insulator-metal (MIM) capacitors. PMMA with a thickness of 1.8 μm defines the sacrificial layer for the MEMS switch and the metal-air-metal (MAM) capacitors.

The MEMS bridge is made from a low-stress sputtered layer of Ti/Au (200/8000 Å). The transmission lines, bridge anchors, and top electrodes of the MAM capacitors are electroplated with 5 μm thick gold to reduce conductor losses and to provide structural support. The filters are diced for packaging before the sacrificial layer is re-



**Figure A.6:** Simulated quality factor of the filter versus switch resistance and center frequency.

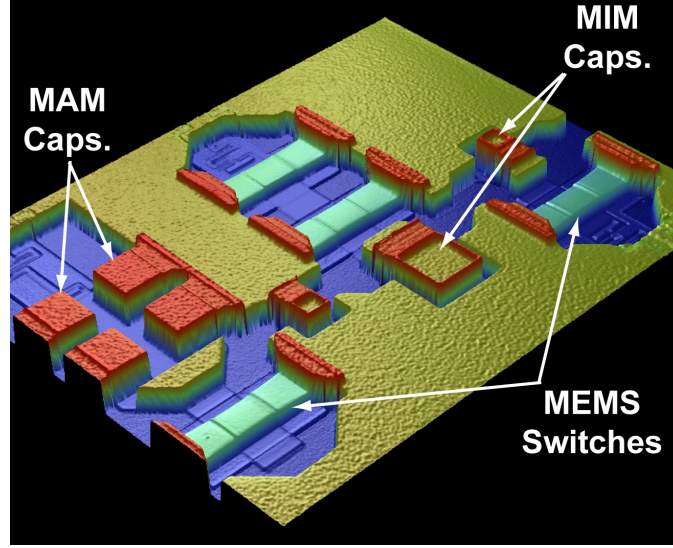
moved in a hot solvent. The MEMS filters are dried using a CO<sub>2</sub> super-critical point drier before they are epoxied into the package and wirebonded at room temperature to avoid thermal damage to the MEMS switches.

The post release height of the MEMS bridges is 2  $\mu\text{m}$  measured with a white light interferometer (Fig. A.8(a)). The measured actuation voltage for the switch is  $V_p = 43$  V which yields an extracted beam spring constant of  $k = 50$  N/m and residual in-plane beam stress of  $\sigma_{res} = 60$  MPa.

## A.4 Measurement Results

S-parameter measurements were taken from 1-4 GHz with an Agilent E5071B Network Analyzer. Actuation of the RF MEMS capacitive switches was accomplished using a 10 kHz bipolar waveform with a magnitude of 45V to reduce the effects of dielectric charging. The filter center frequencies range from 1.65 to 2.34 GHz, demonstrating a tuning range of 34.6% centered at 2 GHz. Measured insertion loss and return loss for the six measured states are shown in Fig. A.8(a)-(b) and summarized in Table A.1. There was a loss of switch yield through the extensive back end packaging which resulted in a limited number of testable states per filter. In order to test the largest number of available states, the measured filter responses were obtained from 3 different filters assemblies





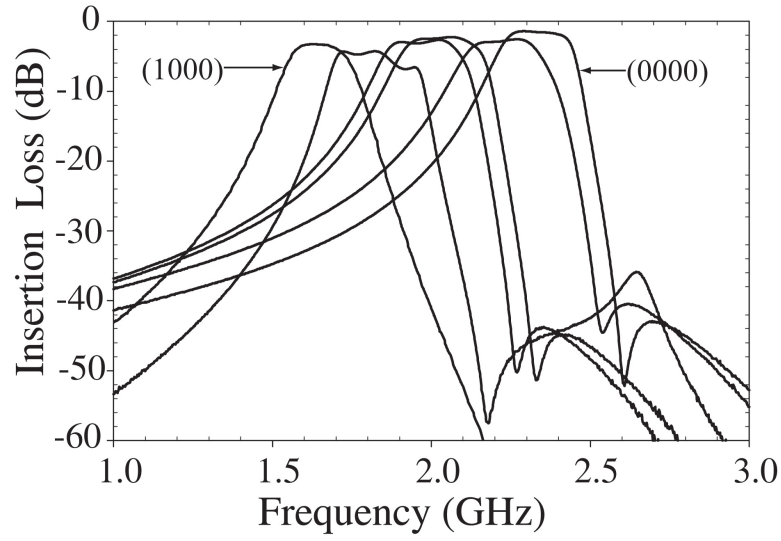
**Figure A.7:** 3-D white light interferometer image of the filter tuning network taken post release.

(each with identical design) from the same wafer run.

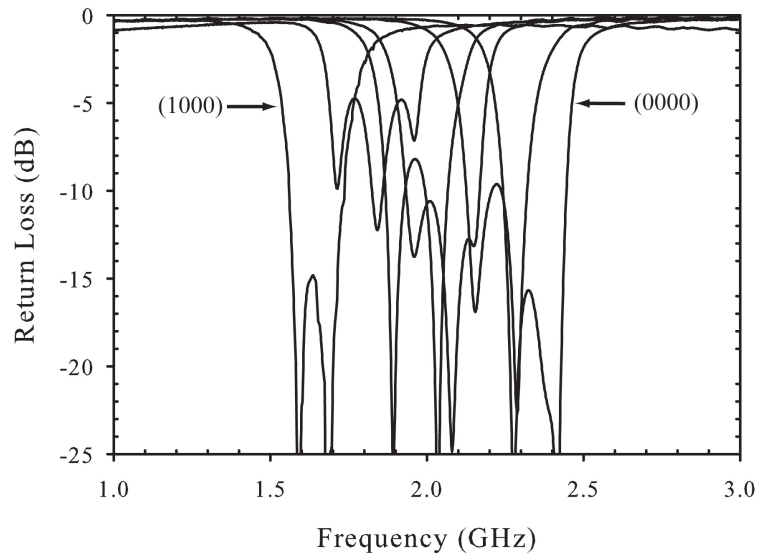
**Table A.1:** Measured Performance of the 34.6% Tunable Filter.

<i>State</i>	$f_0$ (GHz)	$S_{21}$ (dB)	$S_{11}$ (dB)	FBW (%)	BW (MHz)
0000	2.34	1.34	15.67	10.1	238
0001	2.22	2.64	9.7	11.8	262
0010	2.04	2.15	10.58	13.2	269
0011	1.96	2.94	8.2	13.8	271
0100	1.83	—	—	15.3	279
1000	1.65	3.03	14.8	12.2	202

With the exception of state 0100 the insertion loss is 1.34 dB and 3.03 dB at 2.34 and 1.65 GHz, respectively, while the return loss is better than 9.7 dB across the tuning band. Although only the input return loss is shown, the output return loss is also matched well ( $S_{22} \leq -10$  dB). The measured 3-dB fractional bandwidth ranges from 10.1 to 15.3% across the tuning range while the absolute bandwidth varies from 202 to 271 MHz. The filter response yields a  $Q_u$  of 50-150 at 1.65-2.34 GHz, respectively.



(a)



(b)

**Figure A.8:** Measured (a) insertion loss and (b) return loss of the tunable three pole 1.65-2.34 GHz filter.

## A.5 Discussion of Results

The center frequency in the unbiased 0000 state is shifted down from 3 to 2.4 GHz because the MAM and MIM capacitors were 10 and 20% larger than designed respectively. Post release interferometer images of the MAM capacitors showed a 0.1-0.2

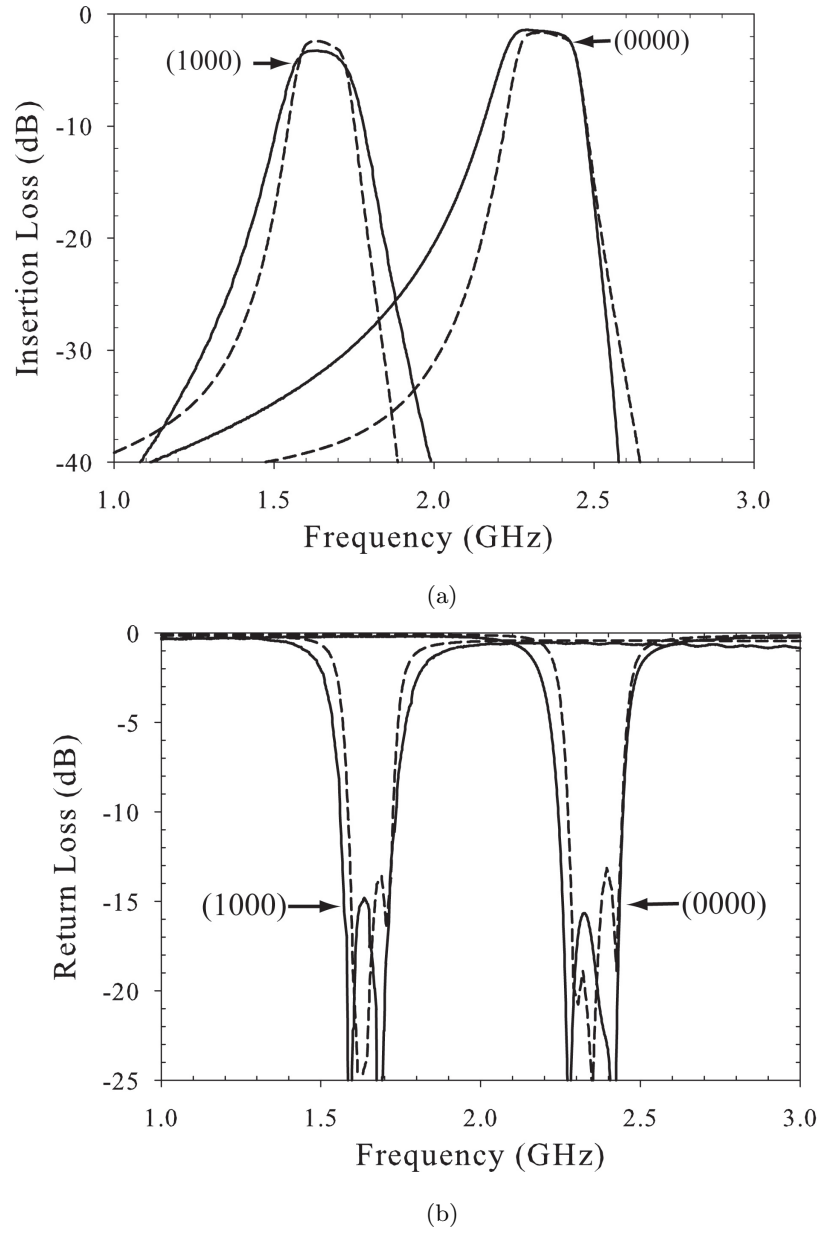
**Table A.2:** UHF-S Band RF MEMS Tunable Filters.

<i>Design</i>	Tuning Range(GHz)	$S_{21}$ (dB)	BW (MHz)	Est. $Q_u$
UCSD(n=3)	1.65-2.34	1.34-3.03	201-279	50-150
NG(n=2)	0.812-1.752	0.6-4	variable	60-90
XLIM(n=2)	1.51-2.26	2.9-5.1	variable	8-17
Raytheon(n=5)	0.880-0.992	6.6-7.3	168-174	$\leq 30$

$\mu\text{m}$  reduction in the gap height due to stress in the electroplated cantilever beam. The increased size of the MIM capacitors was due to a higher dielectric  $\text{Si}_3\text{N}_4$  permittivity and slightly thinner film thickness. The measured bandwidth was higher than predicted across tuning states. The authors believe that this may be the result of package interactions with the circuit that were not accurately modeled in the initial design. Figure A.9(a) shows the measured versus simulated filter response with the larger MIM and MAM capacitance values included in the simulations.

The measured filter response for the 0100 state has only 4.75 dB of return loss because the MEMS switches in the I/O matching networks did not correctly actuate for this measurement. When matched properly simulations predict a return loss of 15 dB. Across the tuning band a  $Q_u$  of 160-100 was measured for weakly coupled resonator test structures. The MEMS capacitive switch has an  $R_s = 0.5 \Omega$  and an  $Q_u=113$  at 2 GHz. The switch resistance is dominated by the thin  $0.3 \mu\text{m}$  bottom metal under the switch which was chosen to reduce the topography in the MEMS bridge area. The measured  $Q_u$  values are 50-150 at 1.6-2.4 GHz, and we believe that the difference is due to leakage through the bias resistors (we had some step coverage issues), especially when the switches are pulled down ( $f_o = 1.6 \text{ GHz}$ ). We believe that with improved fabrication processes this suspended line filter should maintain a  $Q_u$  above 100 across the entire tuning range. Table A.2 shows some other notable tunable RF MEMS filters in the UHF to S bands.

Appendix A is mostly a reprint of the material as it appears in IEEE MTT-S Int. Microwave Symposium, 2008. Isak Reines, Andrew Brown, Mohammed El-Tanani, Alex Grichener, and Gabriel M. Rebeiz. The dissertation author was the primary author of this material.



**Figure A.9:** Measured and simulated (a) insertion loss and (b) return loss for two different states.

# Appendix B

## RF MEMS Capacitive Switch Fabrication Process on High-Resistivity Silicon Substrates

### B.1 Introduction

This appendix details the fabrication process for the high-power RF MEMS switched capacitor that is discussed in detail in chapter 3. This fabrication process was developed at the Nano3 clean room in Calit2 at the University of California San Diego. This fabrication process was modified from the original standard RF MEMS capacitive switch process that was developed at UCSD in 2006 with valuable input from Dr. Balaji Lakshminarayanan, Dr. Kok-Yan Lee, and Dr. Mohammed A. El-Tanani.

### B.2 Fabrication Process

#### B.2.1 Wafer Preparation

(1) Rinse wafer thoroughly with acetone, methanol, and then isopropyl alcohol (IPA) each for 15-30 seconds. Before the IPA dries and creates solvent stains, rinse the substrate in DI water for 30 seconds. Blow dry the wafer with N<sub>2</sub>. Dehydrate the sample for 2

min at 120°C.

(2) Clean flouroware wafer container with acetone, methanol, and IPA to remove any contamination and particles.

### **B.2.2 High-Resistivity Silicon Chrome Bias Lines**

(1) Wafer dehydrate for 2 min at 120°C.

(2) Spin negative photoresist Futurrex NR9-1500PY at 4 krpm for 40 sec, with the acceleration set to 35 rpm/sec.

(3) Bake wafer at 150°C for 90 sec.

(4) Align sample using Karl Suss MA6 contact aligner and expose for 10 sec with a lamp intensity of  $7.5 \text{ mW}/\text{cm}^2$ .

(5) Post-expose bake at 100°C for 1 min.

(6) Develop in undiluted Futurrex RD6 for 7 seconds.

(7) Inspect wafer inspect and record the photoresist resolution by looking at the resolution marks next to each alignment mark.

(8) Sputter SiCrN bias lines using the Denton Discovery 18 tool with the following settings: RF Power = 300 W, Argon = 41 sccm, Nitrogen = 4 sccm, Pressure = 4.1 mT, Time = 30-35 min, Rotation = 60 rpm. The deposition rate is  $33 \text{ Å}/\text{min}$  so the film thickness should be  $1000 \text{ Å}$  with a sheet resistance of 2-5  $\text{K}\Omega/\text{square}$ . Note: The sheet resistance can be increased with more N2 flow. Make sure to run a 30 minute condition run before the real samples so that the SiCrN deposition process can stabilize. In general the sheet resistance of the SiCrN film tends to decrease from run to run given the same deposition parameters. Run a glass slide with each deposition and measure the sheet resistance using the 4-point probe.

(9) Soak wafer in Microposit remover 1165 at 90°C for at least 1 hr. Note: An ultrasonic bath can be utilized to speed up the liftoff process if necessary. Rinse wafer in DI and N2 dry

(10) Wafer inspection.

### **B.2.3 Gold Bottom Electrode**

(1) Wafer dehydrate for 2 min at 120°C.

(2) Sputter Ti/Au/Ti (200/5000/200Å) bottom electrode using the Denton Discovery

18 tool with the following settings: For Ti, DC power = 200 W, Pressure = 4.1 mT, Argon = 43 sccm, Rotation = 60 rpm, Time = 55 sec. For Au, DC power = 200 W, Pressure = 4.1 mT, Argon = 43 sccm, Rotation = 60 rpm, Time: 10-11 min (Run a test sample first to verify the deposition rate). Use the same deposition settings for both the bottom and top Ti layers. Note: the purpose of the top Ti is to reduce the amount of undercut during the subsequent wet etching process of the Au.

- (3) Wafer dehydrate for 2 min at 120°C.
- (4) Spin S1818 at 3 krpm for 40 sec with the acceleration set to 255 rmp/sec.
- (5) Bake at 105°C for 90 sec.
- (6) Align and expose for 10 sec using the MA6 mask aligner.
- (7) Develop in Microposit MF-319 for 30-40 sec.
- (8) Wafer inspect and record photoresist resolution.
- (9) Etch the top 200Å Ti layer with dilute HF acid (1:10 HF:DI). Use a test sample to calibrate the etch time which should be  $\sim$  5-10 sec.
- (10) Etch the 5000 Å Au layer using undiluted KII solution. Again use a test sample to calibrate the Au etch time which should be  $\sim$  1-2 min.
- (11) Wafer inspect to verify that the Au is properly removed.
- (12) Soak wafer in Microposit remover 1165 at 90°C for 30 min to remove the S1818 photoresist. Rinse wafer in DI and N2 dry.
- (13) Etch bottom 200Å Ti layer in the field and top Ti layer on the bottom electrode with dilute HF acid (1:10 HF:DI). Use a test sample to calibrate the etch time which should be  $\sim$  5-10 sec. Rinse wafer in DI and N2 dry.
- (14) Wafer inspection.
- (15) Use Dektak profiler to measure the thickness of the bottom electrode and SiCrN bias lines (Use test structure in the PCM).
- (16) Measure the bottom metal to SiCrN via chains in the PCM to assure a good electrical connection between the 2 layers. Record resistance values from each of the PCM's on the wafer.

#### **B.2.4 Silicon Nitride Capacitor Dielectric**

- (1) Alternating HF/LF PECVD (Plasma Enhanced Chemical Vapor Deposition) with the Oxford Plasmalab tool to deposit 2000 Å of  $Si_3N_4$  with the following settings: Temp

= 350°C, Pressure = 650 mT, LF = 20 W for 7 sec, HF = 20 W for 13 sec,  $SiH_4$  = 400 sccm,  $NH_3$  = 22 sccm,  $N_2$  = 600 sccm, 10 min preheat.

- (2) Run a 15 min condition before running Si calibration sample.
- (3) Run a 10 min deposition on a Si test sample and measure the thickness using the filmetrics tool. Deposition rate is typically  $\sim 130 \text{ \AA}/\text{min}$ .
- (4) Run device sample using the calibrated deposition time, and also include another Si test sample to measure using filmetrics.
- (5) Wafer dehydrate for 2 min at 120°C.
- (6) Spin S1818 at 3 krpm for 40 sec with the accelaretion set to 255 rpm/sec.
- (7) Bake at 105°C for 90 sec.
- (8) Align and expose for 10 sec using the MA6 mask aligner.
- (9) Develop in Microposit MF-319 for 30-40 sec.
- (10) Wafer inspection and record photoresist resolution.
- (11) RIE (Reactive Ion Etch) with the Oxford P80 tool to etch the 2000  $\text{\AA}$   $Si_3N_4$  dielectric using the following settings: Pressure = 75 mT, Power = 100 W,  $CF_4$  = 35 sccm,  $O_2$  = 3 sccm, Temp = 25°C.
- (12) Run a 10 min etch to condition the chamber.
- (13) Run a 30 sec etch test using the test Si sample with the  $Si_3N_4$  coating and measure the  $\sim$  etch rate.
- (14) Etch device sample using calibrated etch time plus a 10% over etch time. Note: This etch recipe will also etch the  $SiO_2$  buffer layer so minimize the over etch to avoid creating additional unwanted device topography.
- (15)  $O_2$  plasma ash the sample using the TEPLA magnetron asher using the following settings:  $O_2$  = 97, Base pressure = 0.005, Process pressure = 0.97, Power = 150 W, Time = 2 min. Note: this step will remove the thin top layer of photoresist that can otherwise be difficult to remove solely with solvents.
- (16) Soak wafer in Microposit remover 1165 at 90°C for overnight to remove the S1818 photoresist. Rinse wafer in DI and  $N_2$  dry.
- (17) Wafer inspection, and measure  $Si_3N_4$  thickness via Dektak. Also remeasure bottom metal thickness and note the amount of etch of the  $SiO_2$  (Use test structure located in the PCM).



### B.2.5 PMMA Sacrificial Layer

- (1) Wafer dehydrate for 2 min at 120°C.
- (2) Dispense HMDS primer to fully coat sample. Wait for 15 sec before spinning with the following settings: Two-step spin, Spin 1 = 500 rpm for 5 sec with acceleration = 5 rpm/sec, Spin 2 = 1900 rpm for 40 sec with acceleration = 35 rpm/sec.
- (3) Dispense 10-15 mL of PMMA A9 on the sample and spin using the same settings as in step 2. Note: This should yield an  $\sim 1.5 \mu\text{m}$ -thick layer.
- (4) Bake on hotplate at 135°C for 10 min.
- (5) Bake on hotplate at 180°C for 2 min. Note: Make sure to go directly into the E-beam chamber after this step to avoid any moisture absorption in the PMMA layer.
- (6) Using Temescal E-Beam 1 deposit a 700Å-thick layer of Ti with the following settings: Current emission = 1.2 (This yields a deposition rate of  $\sim 6\text{-}7 \text{ Å/sec}$ . Note: It is critical that the Ti deposition is quick to avoid excessive heating of the sample which will cause the Ti to come out very rough. The sample should be loaded next the crystal monitor on the center wafer holder using loops of capton tape on the wafer backside to secure its position.
- (7) If Ti layer comes out nice a shiny process to the next step. If not remove Ti with dilute HF:DI (1:10) before removing the PMMA sacrificial layer in Microposit remover 1165 at 90°C for 1-2 hours.
- (8) Wafer dehydrate for 3 min at 105°C.
- (9) Spin S1805 at 3krpm for 40 sec with the acceleration = 255 rpm/sec.
- (10) Bake at 105°C for 90 sec.
- (11) Align sample using MA6 aligner and expose for 10 sec.
- (12) Develop in MF-319 for 20 sec.
- (13) Wafer inspection and record resolution of the S1805 photoresist.
- (14) Wet etch the Ti hard mask with dilute HF:DI (1:10). Calibrate etch time using test sample from identical E-Beam evaporation. Etch time should be  $\sim 10$  sec.
- (15) DI rinse wafer and N2 dry.
- (16) Inspect the wafer to verify that the Ti is properly removed.
- (17) Using the MA6 mask aligner flood expose the sample for 1 min.
- (18) Develop S1805 photoresist with MF-319 developer for  $\sim 30$  sec.
- (19) RIE (Reactive Ion Etch) with the Oxford P80 tool to etch the  $\sim 1.5 \mu\text{m}$ -thick sacrificial layer with the following settings: Power = 150 W, Temp = 30°C,  $\text{O}_2$  = 50 sccm, Pressure = 50 mT.

- (20) Run a 10 min chamber condition before first test sample.
- (21) Etch test sample for 10 min to verify that all PMMA is removed.
- (22) Using calibrated etch time remove PMMA using the RIE. Include another test sample with device sample to verify a proper etch. Note: The Oxford P80 at 150 W will also remove gold and substrate so after the etch the bottom gold may appear rough or redish in color.
- (23) Inspect the wafer before proceeding.
- (24) Remove Ti hard mask with dilute HF acid (1:10 HF:DI).
- (25) Reflow PMMA at 130°C for 4 min. Note: This step should be done just prior to loading the sample into the Denton Discovery 18 tool to avoid any moisture absorption.

### B.2.6 Gold Bridge Deposition

- (1) Sputter Ti/Au/Ti (200/10000/200Å) bottom electrode using the Denton Discovery 18 tool with the following settings: For Ti, DC power = 200 W, Pressure = 4.1 mT, Argon = 43 sccm, Rotation = 60 rpm, Time = 55 sec, Temp = 75°C . For Au, DC power = 300 W, Pressure = 5.3 mT, Argon = 50 sccm, Rotation = 60 rpm, Time: 113 min 20 sec (Run a test sample first to verify the deposition rate). Use the same deposition settings for both the bottom and top Ti layers. Note: the purpose of the substrate heat is to reduce the in-plane stress of the gold.
- (2) Repeat the sputtering deposition on a test wafer that will be used later for electroplating calibration.
- (3) Wafer inspection and measure the thickness of the composite seed metal on the glass slide from the same deposition as the device sample.

### B.2.7 Gold Electroplating

- (1) Wafer dehydrate for 2 min at 120°C.
- (2) Spin SPR-220.3.0 with the following two-step program: Spin 1 = 500 rpm for 5 sec with acceleration = 5 rpm/sec, Spin 2 = 3000 rpm for 40 sec with acceleration = 35 rpm/sec.
- (3) Bake on hotplate at 115°C for 90 sec.
- (4) Manual edge bead removal using acetone and small q-tip applicator.

- (5) Align sample using MA6 aligner and expose for 20 sec.
- (6) Develop in MF-319 for 20 sec.
- (7) Bake on hotplate at 115°C for 2 min.
- (8) Dektak the photoresist mold in 5 locations (top, center, bottom, left, and right).  
Note: Thickness should be between 2.5-3  $\mu\text{m}$ .
- (9) Turn on the hotplate for the heater for the electroplating setup, Temp = 55°C, Stir rod rotation = 200 rpm. If necessary add DI water to the bath. Let the bath stabilize for an hour before running first test sample.
- (10) Wet etch the top Ti layer of the seed metal using dilute HF:DI (1:10). Calibrate etch time using test sample from identical sputter deposition. Etch time should be  $\sim$ 5-7 sec.
- (11) DI rinse wafer and N2 dry.
- (12) Load wafer into the electroplating bath and set the bias current to provide a current density between 1-2  $\text{mA}/\text{cm}^2$  and electroplate sample for 10 min.
- (13) DI rinse and N2 dry test sample.
- (14) Dektak sample and measure the thickness of the electroplated layer to calculate the deposition rate. Note: This is done by comparing the pre and post height of the photoresist mold across the 5 locations. The typical rate is between 75-100nm/min
- (15) Electroplate 1  $\mu\text{m}$  of gold on the device sample, remove from bath DI rinse and N2 dry.
- (16) Flood expose electroplating mold using MA6 aligner for 1 min.
- (17) Develop in MF-319 for 30-40 sec.
- (18) Wafer inspection and measure the electroplated metal thickness.

### **B.2.8 MEMS Beam patterning**

- (1) Wafer dehydrate for 2 min at 105°C.
- (2) Spin S1818 at 3 krpm for 40 sec with the acceleration set to 255 rmp/sec.
- (3) Bake at 105°C for 90 sec.
- (4) Align and expose for 10 sec using the MA6 mask aligner.
- (5) Develop in Microposit MF-319 for 30-40 sec.
- (6) Wafer inspect and record photoresist resolution.
- (7) Etch the top 200Å Ti layer with dilute HF acid (1:10 HF:DI). Use a test sample to

calibrate the etch time which should be  $\sim 5$ -10 sec.

(8) Etch the 51  $\mu\text{m}$  Au layer using undiluted KII solution. Again use a test sample to calibrate the Au etch time which should be  $\sim 3$ -4 min.

(9) Wafer inspect to verify that the Au is properly removed.

(10) Etch the bottom 200 $\text{\AA}$  Ti layer with dilute HF acid (1:10 HF:DI). Use a test sample to calibrate the etch time which should be  $\sim 5$ -10 sec.

(11) Flood expose PR using MA6 aligner for 1 min.

(12) Develop in MF-319 for 30-40 sec.

(13) Prior to the device release take white light interferometer images of the devices and associated test structures.

(14) If wafer dicing is required spin S1818 at 3 krpm for 40 sec with the acceleration set to 255 rmp/sec and bake on a hotplate at 105°C for 2 min.

### B.2.9 MEMS Release

(1) Soak wafer in Microposit remover 1165 at 80°C for 30 min.

(2) While keeping meniscus on the sample transfer the wafer to a fresh beaker of Microposit remover 1165 at 80°C, and let soak for at least 24 hours.

(3) Transfer the sample into DI water at room temperature and let soak for at least 1 min. Repeat this step with two fresh beakers of DI water.

(4) Etch the 200 $\text{\AA}$  Ti layer that is located on top and bottom of the MEMS beam with dilute HF acid (1:10 HF:DI).

(5) Rinse sample in DI water for at least 1 min and repeat this step 2 more times.

(6) Rinse the sample in Methanol for at least 1 min and repeat this step 2 more times.

(7) Transfer the sample into the critical point drier while keeping a methanol meniscus on the sample.

(8) Run the CPD with the following settings: purge = 4, vent = xx, bleed = yy, .....

(9) Take white light interferometer images of the device post-release.

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