UCLA
UCLA Electronic Theses and Dissertations

Title

Nanoscale contact engineering for Si/Silicide nanowire devices

Permalink

https://escholarship.org/uc/item/4gh912r9

Author

Lin, Yung-Chen

Publication Date

2012

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

LOS ANGELES

Nanoscale contact engineering for Si/Silicide nanowire devices

A dissertation submitted in partial satisfaction

of the requirements for the degree Doctor of Philosophy

in Materials Science and Engineering

by

Yung-Chen Lin

2012

ABSTRACT OF THE DISSERTATION

Nanoscale contact engineering for Si/Silicide nanowire devices

By

Yung-Chen Lin

Doctor of Philosophy in Materials Science and Engineering

University of California, Los Angeles, 2012

Professor Yu Huang, Chair

Metal silicides have been used in silicon technology as contacts to achieve high device performance and desired device functions. The growth and applications of silicide materials have recently attracted increasing interest for nanoscale device applications. Nanoscale silicide materials have been demonstrated with various synthetic approaches. Solid state reaction wherein high quality silicides form through diffusion of metal atoms into silicon nano-templates and the subsequent phase transformation caught significant attention for the fabrication of nanoscale Si devices. Very interestingly, studies on the diffusion and phase transformation processes at nanoscale have indicated possible deviations from the bulk and the thin film system. Here we studied growth kinetics, electronic properties and device applications of nanoscale silicides formed through solid state reaction.

We have grown single crystal PtSi nanowires and PtSi/Si/PtSi nanowire heterostructures through solid state reaction. TEM studies show that the heterostructures have atomically sharp interfaces free of defects. Electrical measurement of PtSi nanowires shows a low resistivity of ~28.6 $\mu\Omega\cdot$cm and a high breakdown current density beyond 10^8 A/cm2. Furthermore, using single-crystal PtSi/Si/PtSi nanowire heterostructures with atomically clean interfaces, we have fabricated p-channel enhancement mode transistors with the best reported performance for intrinsic silicon nanowires to date. In our results, silicide can provide a clean and no Fermi level pinning interface and then silicide can form Ohmic-contact behavior by replacing the source/drain metal with PtSi. It has been proven by our experiment by contacting PtSi with intrinsic Si nanowires (no extrinsic doping) to achieve high performance p-channel device.

By utilizing the same approach, single crystal MnSi nanowires and MnSi/Si/MnSi nanowire heterojunction with atomically sharp interfaces can also been grown. Electrical transport studies on MnSi nanowire shows an abrupt resistance reduction due to the spin ordering at ~29.7 K. A negative magnetoresistance (MR) ~1.8% under 5 Tesla at 1.6 K is achieved, demonstrating the ferromagnetic behavior of MnSi. Furthermore, using the MnSi/p-Si/MnSi heterostructure, we have studied the charge injection at various temperatures via the Schottky barrier, and the spin scattering was observed through magnetotransport studies of MnSi/p-Si/MnSi heterojunction. Our results represent the first report of magnetic contact fabrication through the formation of single crystal heterojunction nanowires and the first demonstration of spin injection and detection in such Si nanowire devices. The magnetic silicides approach thus opens a new pathway to create ferromagnetic/semiconductor junction with clean and sharp interface, and maysignificantly impact the future of spintronics.

Beyond those applications, silicide phase control at nanoscale is investigated. Three nickel phases, $Ni_{31}Si_{12}$, Ni_2Si and $NiSi_2$ are observed in one step annealing at 550 ^{o}C. $NiSi_2$ grows initially through the Si NW and then the area close to nickel pad transforms into the nickel-rich phase, $Ni_{31}Si_{12}$. With prolonged annealing over 5 minutes, the Ni_2Si starts to show up in between $Ni_{31}Si_{12}$ and $NiSi_2$. The growth sequence is different from the thin film system where Ni_2Si usually appears as the initial phase in the beginning as the annealing temperature is higher than 400 ^{o}C. Interfacial energy differences and surface free energy are believed to play an important role here at the nanoscale, which lead to the formation of normally unfavorable silicide phases in Si NWs. In addition, Si/SiOx core/shell NW structure is used to explore the phase transformation of silicides in the structure-confined nano environment. Nickel silicides in the structure-confined core/shell Si NW shares the similar phase formation sequences as those appeared in the bared SiNWs, while the growth rate is significantly retarded. This may be attributed to the high compressive stress built-in in the core/shell NW structure that retards the diffusion of the nickel atom as well as limits the volume expansion of the metal-rich phases. As a result, the high stress at this finite scale hinders the continuous growth of $Ni_{31}Si_{12}$ into the core/shell NWs and totally eliminates the formation of Ni_2Si in core/shell NWs with thick oxide shells (~ 50 nm). Through these studies, we have demonstrated first time the phase formation sequences of nickel silicides in Si and Si/SiOx NW structures, which is of great importance for reliable contact engineering for Si NW devices. Furthermore, we have provided a clear picture of the hindered nickel silicide growth in confined nanoscale environment and showed the deviated behavior of silicides growth under stress. The information rendered here will be useful for Si NW device applications as well as for the silicon device engineering at nanoscale in general.

To further investigate the oxide shell effect, Mn_5Si_3 and Fe_5Ge_3 NW were grown within various oxide thickness to explore the nucleation and growth in the nanowire structure. A oxide shell exerted a compressive stress on the silicide or germanide materials will make those materials with single-crystal properties. Interestingly, single-crystal growth of contact materials can be also implemented for germanide materials. The iron-rich germanide, Fe_5Ge_3, was successfully grown with single-crystal properties. It shows ferromagnetic properties with a Curie temperature above the room temperature verified by magnetic force microscope (MFM). Two different epitaxial relations found at germanide/germanium interface due to the different sizes of the germanium NW templates. These two different crystal structures exhibited magnetic anisotropy in magnetic force microscope (MFM) measurement, showing differently preferred domain orientations. In-plane and out-of-plane magnetization in the Fe_5Ge_3 NWs are observed in our experiment. The crystal orientation or engineering stress may have influence on the magnetic domain structure. This ferromagnetic contact material may open the way for spintronics to grow the magnetic materials on the semiconducting materials and control the direction of magnetization in the future.

Those silicide studies indicated silicide metal-heterojunction field effect transistor has excellent device performance. In addition, Si channel region can be shrunk to less than 10 nm and also keep semiconducting properties without high leakage current. This approach has the potential for future nanoelectronics. However, silicide phase transformation shows a deviated behavior from the studies in bulk system. It may be associated with stress effect or nucleation behavior at nansclae, leading the different formation phase or sequence. For those interesting phenomena, it has attracted more and more attention and may gain more insight studies in the near future.

The dissertation of Yung-Chen Lin is approved.

King- Ning Tu

Kang L. Wang

Yang Yang

Yu Huang, Committee Chair

University of California, Los Angeles

2012

Dedicated to my son, Bruce Lin

my wife, I-Fang Lee

TABLE OF CONTENTS

Chapter 1: Introduction

Chapter 2: Single Crystalline PtSi Nanowires, PtSi/Si/PtSi Nanowire Heterostructures, and

Nanodevices

Chapter 3: Detection of Spin Polarized Carrier in Silicon Nanowires with Single Crystal MnSi

as Magnetic Contact

Chapter 4: The Growth of Nickel Silicides in Si and Si/SiOx Core/Shell Nanowires

Chapter 5: Control the Pollycrystalline and Single-Crystal Growth of Manganese Silicide & Iron Germanide NWs in the Confined Oxide Shell

Chapter 6: Self-Aligned Nanolithography in a Nanogap

LIST OF TABLES

LIST of FIGURES

ACKNOWLEDGEMNETS

VITA

December 11, 1979	Born in Taichung, Taiwan
2002	B.S., Materials Science and Engineering
	National Tsing-Hua University
	Hsin-Chu, Taiwan
2004	M.S., Materials Science and Engineering
	National Tsing-Hua University
	Hsin-Chu, Taiwan
2012	Ph.D., Materials Science and Engineering
	University of California, Los Angeles
	Los Angeles, California

PUBLICATIONS AND PRESENTATIONS

1. <u>Lin, Y. C.</u>, Chen, Y. and Huang Y., The growth and applications of silicides for nanoscale devices., **Nanoscale**, 4 (5), 1412-1421, (2012).

2. Wu, W. W., K. C. Lu, Chen, K. N., Yeh, P. H., Wang, C. W., <u>Lin, Y. C.</u>, Huang, Y., Controlled large strain of Ni silicide/Si/Ni silicide nanowire heterostructures and their electron transport properties,. **Applied Physics Letters**, 97(20), 203110, (2010).

3. <u>Lin, Y. C.</u>, Y. Chen, Di, Xu, Huang, Y. Growth of Nickel Silicides in Si and Si/SiOx Core/Shell Nanowires., **Nano Letters,** 10(11), 4721-4726, (2010).

4. <u>Lin, Y. C.</u>, Chen, Y., Shailos, A. and Huang, Y., Detection of spin polarized carrier in silicon nanowire with single crystal MnSi as magnetic contacts, **Nano Letters**, 10 (6), 2281–2287 (2010).

5. <u>Lin, Y. C.</u>, Bai, J. W., & Huang, Y., Self-aligned nanolithography in a nanogap., **Nano Letters**, 9 (6), 2234-2238, (2009).

6. <u>Lin, Y. C.</u>, Lu, K. C., Wu, W. W., Bai, J. W., Chen, L. J., Tu, K. N., & Huang, Y., Single crystalline PtSi nanowires, PtSi/Si/PtSi nanowire heterostructures, and nanodevices., **Nano Letters**, 8 (3), 913-918, (2008).

1.   Introduction

1.1. The challenges of modern transistor for contact engineering

As addressed by the scaling rule, the device dimensions of complementary metal-oxide-semiconductor (CMOS) transistors have been shrunk to improve the performances for ultra-large-scale integrated circuits (ULSI). The shrinkage of the contact feature size or carrier channel size has caused the increase of resistances in both source/drain regions, leading to the degradation of electrical characteristics.[1, 2] This degradation becomes unavoidable in the advanced short-channel devices and thus new design strategies need to be imposed to current nanotechnology. In 1925, a field effect transistor (FET) device structure with only conducting channel (no junctions) was proposed. (Figure 1-1) The FET was only a resistor that could be depleted of charge carriers by gate modulation. To turn the device completely off, the device need to fully deplete its body of carriers. Therefore, it required a very thin nanoscale channel for which the technology did not exist at the time. Recent explorations of NW or thin-film transistor architectures (SOI) have raised practical interest in these simple gated resistors. Especially for the NW transistors, the thin body structure displaying better gate control, allowing researchers to explore diverse device structures and to investigate new operation functions. However, for this type of thin body transistor or NW FET, the contact or sheet resistance is still high. The silicided NW FET utilizes the low resistance properties of silicides in place of the source/drain contacts and has attracted broad research interest. By combining the NW structure and silicide technology, it is possible to solve the short-channel problem and achieve high device performance for ultra-short channel device in the future.

1.2. NW transistor and silicided NW transistor[3]

NW FET poses as a potential candidate to resolve the short-channel effect issue since the thin body of NW excludes large depletion region. Hence, degradation of gated control and source/drain leakage can be avoided. The charge carriers in the NW can be fully depleted and thus the NW FET can be operated as junctionless FET (Figure 1-2b) or metal heterojunction FET, having no source/drain implantation compared with conventional junction FET (Figure 1-2a). Moreover, the contact resistance can be effectively reduced when silicides are used as the contact materials, making silicided NW FET promising candidate to achieve high performance transistor operation.

To fabricate the NW FET, silicon NWS are often grown by vapor-liquid-solid (VLS) method. The diameter of NWS can be controlled by the size of the metal catalyst such as gold. In addition, the silicon NW doping can be done by using the in-situ doping which flows the doping elements in gas phase in the growing process. For simplicity, the NW transistor usually functions as junctionless FET (no source/drain implantation). To achieve high performance, the doping concentration of NWS is usually at the level of $\sim 10^{17} \sim 10^{18}$ cm^{-3}. In these doping ranges, the source/drain contact resistance will not be too large to limit the current. Therefore, in this operation mode, the device is always in the on-state and the accumulation-mode operation is applied to reach higher on-current and lower subthreshold voltage (Vt). The same charge voltage is applied to deplete the NW to reach the off-state. If NWS are doped with even higher doping concentration, the NW device can be operated with body current (carrier flows in the whole NW body) flowing in the on-state and also rely on the reverse voltage to turn the device off. By this design, it is not necessary to attract the carrier to the surface and then is not strongly dependent of the oxide thickness scaling. Therefore, it is better for the ultra-short channel devices.

To reduce the contact resistance further, the metal heterojunction FET can also be fulfilled in the NW structure. With the silicide technology, nickel and platinum silicide has been proposed to grow in the silicon NW and form the silicide/silicon/silicide heterjunction. With various doping concentration of silicon, the device can function in the normal-on or normal-off mode, and in both modes the NW transistor can achieve high performance, due to the better gated control in the NW structure.

1.3. The properties and applications of metal silicides

Silicide materials with diversified properties (Table 1-1) have been widely used in electronics such as device contacts (NiSi, $TiSi_2$, $CoSi_2$),[4-10] optical light emitting diode (β-$FeSi_2$, $CrSi_2$),[11, 12] thermoelectrics ($MnSi_{1.7}$),[13] photovoltaic devices ($BaSi_2$)[14-16] and spintronics devices ($Fe_xCo_{1-x}Si$, Fe_3Si, Co_2MnSi)[17-19] shown in Fig 1-3.[20-21] Silicides with low contact resistivity, good interface property and better thermal stability are candidates for device contact application. Some metallic silicides are also magnetic which draw considerable interest for its potential application in spintronics due to its compatibility with current Si technology.

1.4. The growth and applications of silicon NWS

Silicon NWS are grown through metal-catalyzed chemical vapor deposition process. The gro

wth is generally to follow the vapor-liquid-solid mechanism. In the beginning, the catalyst, mostly Au, forms a eutectic droplet at low temperature on a heated Si [111] substrate (Fig 1-4a). In the following step, gas precursors containing reactant material (Si) are introduced and then catalytically decomposed to incorporate into the liquid droplet near the eutectic temperature.

This liquid droplet continues to adsorb decomposing Si atoms from the vapor, leading to a supersaturated state (Fig. 1-4b), at which point crystallization of Si occurs at the liquid-solid interface resulting in one-dimensional (1D) NW growth (Fig. 1-4c).

Silicon based devices are wildly used in integrated circuit devices for lots of decades due to its excellent electronic properties, chemical stability, mechanical strength and other solvable process issues such as good insulating oxidation product and etching friendly. Thus, for the nanotechnology, there are lots of efforts, been made, to discover the new functionality of SiNWs. For the capability of transporting electrons and holes, silicon NWS can be function units for nanoscale electronics constructed without complicated and expensive fabrication equipments. Si NWS also have potential applications in chemical sensors, field-emeission devices, spintronics and photonics. Physical properties of Si NWS are addressed as follows: The electronic energy gaps of Si NWs have been investigated by scanning tunneling spectroscopy, found to increase with the decrease of the Si NW diameter from 1.1 eV for 7 nm to 3.5 eV for 1.3 nm. This is coherent with previous theoretical predictions. The Young's Modulus of the VLS-synthesized Si NWS have been characterized by atomic force microscopy to be 186 and 207 GPa, respectively, for single- and double-clamped Si NWS, which are close to the Si (111) bulk value of 169 GPa. The average fracture strength of the Si NWs that are VLS-grown on a [111] Si substrate has been calculated to be around 12 GPa.

The thermal conductivity of individual single-crystal intrinsic Si NWS with diameters of 22-115 nm has been found to be two orders smaller than that of bulk Si in magnitude. The increased phonon-boundary scattering and possible phonon-spectrum modification result in the strong diameter dependence of thermal conductivity in NWS. This is also indicated by molecular dynamics simulation studies based on increased surface-scattering effects/Nevertheless, due to

the phonon-confinement effect, the thermal conductivity was predicted to increase at very small diameter, smaller than 1.5 nm.

For electrical properties, the carrier mobility of single crystalline n-type and p-type Si NWs has been estimated to be coherent with diffusive transport. Also, studies show that Si NWs are expected to be able to be heavily doped and become metallic. Silicon NWS have been demonstrated to be efficient thermoelectric materials that could be applied to waste heat utilization, power generation and refrigeration. The efficiency of the materials is determined by the thermoelectric figure of ZT, which is a function of the Seeback coefficient, electrical resistivity, thermal conductivity and absolute temperature. Since optimizing one parameter of ZT often degrades another, it has been challenging to maximize ZT. However, it is possible to fabricate nanostructures of one or more dimensions, smaller than the mean free path of the phonons but larger than that of electrons and holes. This can greatly reduce thermal conductivity but maintain electrical resistivity, enabling ideal thermoelectric materials. ZT=0.6 at room temperature in rough Si NWS of about 50 nm in diameter has been demonstrated through a wafer-scale processing technique. Additionally, ZT~1 at 200K, has been reported from the single-component system of Si NWS for cross-sectional areas of 10 nm x 20 nm and 20 nm x 20 nm through adjusting impurity doping levels and the nanowire size. The optical properties of oxygen- and hydrogen-terminated Si NWs have been studied by time-resolved photoluminescence spectroscopy, cathodoluminescence spectroscopy and imaging. Interface states in the Si core and oxygen-based defects at the oxide cladding layer respectively contribute to the red- and the blue-emission bands from these NWs, characterized by homogeneous broadening. Additionally, quantum confinement effects are excluded for being the cause of these emission bands based on the results. The Erbium-doped Si NWs show photoluminescence at

room temperature at a wavelength of 1.54 μm, which is ideal for optical communication. Additionally, Si NWs have notably larger piezoresistance effect than bulk Si, related to strain-induced carrier mobility change and surface modifications. This may be important for nanowire-based flexible electronics and nano-electromechanical systems.

1.5. Synthetic approaches to nanoscale silicides

Various approaches have been developed to grow nanoscale silicide structures, which can be summarized to three categories: (1) endotaxy, (2) chemical vapour deposition (CVD) and (3) solid state reaction (Figure 1-5). For the endotaxial growth, transition metals, rare-earth (RE) metals or noble metals were deposited onto a heated Si substrate and subsequently reacted with the substrate to form self-assembled silicide nanostructures. In order to have the lowest strain energy against the substrate, silicide materials adjusted their shape into nanostructures with small anisotropic lattice mismatch ($\sim$ 0%) in the larger (longitudinal) direction and larger mismatch ($\sim$> 3%) in the smaller (axial) direction. Figure 1-5a, b showed $CoSi_2$ NW (NWs) islands grown on Si(100) substrate at 750°C. Cobalt was deposited by sublimation onto a heated substrate and reacted with Si to form $CoSi_2$.[30] $CoSi_2$ would self-assemble into two distinct shapes, rectangular and NW (NWS) shape in Fig. 2b. For rectangular shape, $CoSi_2$ adopts A-type epitaxial relation, Si(111)//$CoSi_2$(111), with the Si substrate; for NW shape, B-type epitaxial relation appeared on one side of interface, Si(111)//$CoSi_2$(-11-1) and Si(1-51)//$CoSi_2$(1-11) epitaxial relation shows on the other side. These interface configurations correspond to the coherent interface relations between $CoSi_2$ nanostructures and Si(100) substrate with lower interfacial energy. A variety of metals such as Ti, Mn, Fe, Co, Ni and Pt have been reported to form silicide nanostructures on the Si substrate through endotaxy growth.[31-34] However, no effective control methods are

available so far over the growth length, growth position of the silicide NWs or NW diameter with this approach.

Chemical vapour deposition (CVD) is a popular synthetic route to form silicide nanostructures which is implemented through the reactions between metal and/or Si precursors. CVD method could be conducted with versatile precursors, reactions between silicon vapour precursor (SiH_4) and metal thin film (e.g. nickel), metal vapour precursors (e.g. metal halogen precursors such as metal chlorine or metal iodine vaporized at high temperature) with Si substrate, reaction with both Si and metal vapour precursors or reactions from a single source of precursor containing both Si and metal. Fig. 1-5c and d demonstrate the use of a single vapour precursor (*trans*-$Fe(SiCl_3)_2(CO)_4$)[35] as the iron and Si source to grow FeSi NWs in a CVD setting. The precursor decomposed at elevated temperatures to form a NW structure on the SiO_2/Si substrate. In this manner, a wider range of single-crystal silicide NWs can be synthesized and used to explore the properties of various silicide materials. In a CVD setting, vapour precursor can be supplied continuously to synthesize abundant free standing silicide NWs which may be scaled up to mass production. In addition, the silicide growth is not limited to the growth substrates. (e.g. Si, sapphire, SiO_2 substrates) since the metal and Si source can be both supplied through vapour precursors. But as the precursors may under different decomposition routes at different temperature zones and/or growth pressures, mixed product of silicon, silicide thin film, different silicide nanostructures, and sometimes metal film, metal particles can be found in the same reaction chamber.[37-40] Therefore the CVD reaction conditions need to be strictly controlled in order to obtain desired silicide products.

Solid state reaction is another approach to silicide nanostructures and, because of its reaction nature, to form silicide/Si interface which can be explored as contacts for various device

applications based on Si NWs. This approach has been used extensively in microelectronic industry to form metallic silicide contacts to Si through the interface reaction of Si and the metal. In short, metal is deposited as thin film on top of Si NWs and then at elevated temperatures metal atoms diffuse into and react with Si to form silicides, which normally adopt an epitaxial relation with the Si lattice. A variety of silicide contacts with excellent performance by solid state reaction method have been demonstrated such as $NiSi_2/Si$, $NiSi/Si$, Ni_2Si/Si, $CoSi_2/Si$, $PtSi/Si$ and $MnSi/Si$ for nanoelectronics.[36, 41-46] Figure 1-5e shows the schematic of a typical solid state reaction set up. Ni contacts were deposited on top of Si NWs, which were then subject to annealing at elevated temperatures. Ni atoms would diffuse into Si NW template and transform Si into Ni silicides. $NiSi_2$ was found to form at 550^oC,[43] which maintains a sharp clean epitaxial interface with Si lattice ($Si[1-10]//NiSi_2[1-10]$ and $Si(111)//NiSi_2(111)$) as show in the high resolution transmission electronic microscopic (HRTEM) image in Figure 1-5f. The smooth and high quality epitaxial interface between silicides and Si achieved in solid state reactions makes this approach desirable for device fabrication at nanoscale, which is also compatible with current microelectronic processing techniques.

1.6. Contact formation through solid state reaction

1.6.1. Introduction of silicide/Si heterostructure by solid state reaction

While Si NW devices have caught increasing attention for future device applications, it has been difficult to achieve low resistance, high stability or less defective contacts at this scale due to the small contact area, surface traps or non-conformal coverage between electrodes and NW structure.[47, 48] For solid state reactions confined in Si NW structures, the silicides form directly on the silicide/Si interface resulting in a fresh and few-defect metal/Si interface that may

contribute to high device performance. With lithographically patterned metal pads, silicide/Si/silicide structures can be achieved with two silicide regions serving as source and drain electrodes, and the Si as the transistor channel. It has also been demonstrated that silicides can grow up to ~µm's length into the Si NW from the metal contacts, which has been explored for device scaling to achieve short channel devices.[44, 45, 49] Studies indicate that the junction leakage is small (~60 nA at the 0.5 V) in the Ni silicide/Si/Ni silicide heterostructure even with an ultrashort Si channel of ~5 nm, which may be attributed to the perfect Ni silicide/Si interface and the low concentration of Ni atoms existing in the Si channel.[50] The current-voltage (I-V) measurement across the ultrashort channel silicide/Si heterostructure device shows a rectified curve which indicates the existence of Schottky barrier in the Ni silicide/Si/Ni silicide hetero-junction. This suggests that the semiconducting properties of Si are preserved and the flat interface does not enhance thermal emission or current tunnelling which are normally observed at a rough or spike-like interface, even though the semiconducting channel is less than 10 nm. The impressive results imply that the Ni silicide/Si/Ni silicide heterostructure can be applied for ultrashort channel devices.

1.6.2. The growth of silicide NWs by solid state reaction

Wu et al.[49] first demonstrated the idea to implement the silicide technology at nanoscale for making silicide NWs by solid state reaction. As illustrated in Figure 6a, Si NWs were grown by vapour liquid solid (VLS) method and then Ni films were deposited with comparable thickness to the average NW diameter. The Ni-coated Si NWs were then annealed at $550^{o}C$ to form NiSi. The excess Ni was etched away by acid and followed by the post-annealing at $600^{o}C$ at forming gas (N_2:H_2=90:10). This process will render fully silicided NWs that are single crystal in nature

as shown in the figure 3b and c. The different NiSi NW growth directions, NiSi[1-11] (Fig. 1-6b) and NiSi[001] (Fig. 1-6c) may be explained by different growth directions of the starting Si NWs.

1.6.3. Forming Silicide/Si NW heterostructure by solid state reaction

To achieve the growth of silicide/Si heterostructure, it is crucial that metal elements possess higher diffusivity in Si. Due to the fast diffusion of metal atom into the Si NWs, silicides can grow into the NWs, forming silicide/Si heterojunction. Several silicide/Si heterostructures have been investigated with the metallic contacts such as Ni, Pd, Pt, Co and Mn to the Si NWs.[36, 41, 43-45, 51] The heterostructures are generally formed by patterning the Si NW template with metal pads followed by annealing at elevated temperatures to perform the silicidation (Fig. 1-7a). The silicide/Si/silicide heterostructure or fully silicided NW can be controlled through the annealing time (Fig. 1-7a,b-d). There are various material systems that have demonstrated such heterostructures such as NiSi/Si, CoSi$_2$/Si, NiSi$_2$/Si, PtSi/Si and MnSi/Si.[36, 44-46, 49] In these systems, epitaxial relations are all observed between silicide and Si with atomically sharp interface and few interface defects, which is desirable for high performance nanoelectronics. Taken PtSi and MnSi as the examples, both silicide systems can form the silicide/Si heterostructure. Surprisingly, although accompanied with large lattice mismatch (~ 8.8% in PtSi/Si, ~24.5% in MnSi/Si), both silicides mange to keep the epitaxial relation and a flat interface with Si when advancing into the Si NWs (Fig. 1-7e-h).[36, 44] Even though the Si region is below 10 nm (Fig. 1-7e), the silicide regions will not merge and a clear interface is maintained. The excellent interface properties and junction properties allow silicide heterojunction to potentially work as ultra-short channel devices.

1.7. New technical approaches or structures for low contact resistance FET and short-channel device

1.7.1. The challenging for the low device junction resistance

The conventional FET can be classified as the junction FET. The opposite type of doping for the source/drain and channel is necessary for this device structure. As the device scales down, the main issue is the short-channel effect due to the depletion region across the channel. Other issues such as degradation of sub-threshold slopes, drian-induced-barrier-lowering (DIBL) and source/drain leakage all come from the similar reasons related to the source/drain junction. Industry has several approaches to achieve the shallow junction which relieves the short-channel effect. However, the p-n junction around source and drain still has higher sheet resistance, which may become a current limit for ultra-short channel device. Therefore, major architectural changes have been proposed to facilitate downsizing toward the perceived limit of ~30 nm. Recently, several groups have suggested that short-channel effects can be suppressed by imposing a junctionless structure or a metal heterojunction barrier at the source/drain in place of heavily doped junctions.

1.7.2. Comparison of junction FET, junctionless FET and metal heterojunction FET

For the junctionless FET (Fig 1-8a), the conduction in the junctionless gated transistor is based on the transport of majority carriers in the bulk of the device, through a body channel from source to drain. Therefore, drain current in the on-state is proportional to the channel doping and the carrier mobility and not dependant on the gate oxide capacitance (dielectric constant or thickness). Speed (or 'intrinsic delay') is also independent of the gate oxide thickness. The

extreme efforts currently underway to reduce gate oxide thicknesses can therefore be avoided. This junctionless FET needs a thinner body or one-dimensional wire structure to provide the better gated control. The complete depletion is necessary for the junctionless FET to behave as the off-state. Therefore, the junctionless FET can only be fulfilled for the SOI technology or in a NW structure.

Metal heterojunction FET is another new structure to alleviate the short-channel effect (without source/drain doping) and reduce the source/drain sheet resistance. A heterolayer, silicides, grows at the source/drain in place of a heavily doped homojunction (Fig. 1-8b). The Schottky barrier which forms naturally between a metal silicide source/drain and the silicon channel offers a number of advantages such as alleviating shallow source/drain extensions, junction capacitance, parasitic bipolar and latch-up phenomena, and fluctuations due to finite number of randomly placed dopants in the channel. A conventional self-aligned silicide process is employed to create the Schottky barrier MOSFET (SBMOSFET) structure. Gate-induced electric fields then render the source barrier nearly transparent to tunneling in the on-state, Vg>Vt, as in Fig. 1-8c, while carriers remain to be confined by the Schottky barrier in the off state, Vg<Vt as in Fig. 1-8c. A low barrier height of ~0.2-0.3 eV (Table 1-2) is needed at the source in order to induce large tunnel currents in the on-state at practical gate voltage or electric field. Conversely, a relatively high barrier is needed to suppress ''reverse'' tunneling by opposite type of carriers at the drain. Because the Fowler–Nordheim transmission probability for internal field emission is exponentially dependent upon barrier height as $\Phi b^{3/2}$, very large on/off ratio can be achieved at low temperatures in metal heterojunction MOSFETs.

According to the literatures, PtSi and ErSi$_2$[44, 52] have successfully experimented as the p and n-type metal heterojunction FET on bulk Si substrate. PtSi source/drain p-MOSFETs show excellent scaling to ~25 nm channel length with greatly simplified processing and reduced contact, sheet and parasitic resistance. Junction capacitance is effectively eliminated, and much smaller. Complementary *n*-type devices have also been demonstrated recently based on the low ~0.39 eV n-barrier of ErSi$_2$. Due to the high doping concentration in the channel, the off-current is still the limitation for this device structure. However, for the NW structure, the fully depleted characteristic may suppress the strong source/drain leakage. Therefore, it may be more practical for NWs to achieve the metal heterojunciton FET.

1.8. Reference

1. J. P. Colinge,I. Ferain,A. Kranti,C. W. Lee,N. D. Akhavan,P. Razavi,R. Yan and R. Yu, *Sci Adv Mater*, 2011**, 3**, 477-482.

2. J. P. Colinge,C. W. Lee,A. Afzalian,N. D. Akhavan,R. Yan,I. Ferain,P. Razavi,B. O'Neill,A. Blake,M. White,A. M. Kelleher,B. McCarthy and R. Murphy, *Nat Nanotechnol*, 2010**, 5**, 225-229.

3. A. M. Ionescu, *Nat Nanotechnol*, 2010**, 5**, 178-179.

4. F. Deng,R. A. Johnson,P. M. Asbeck,S. S. Lau,W. B. Dubbelday,T. Hsiao and J. Woo, *J Appl Phys*, 1997**, 81**, 8047-8051.

5. H. Iwai,T. Ohguro and S.-i. Ohmi, *Microelectron Eng*, 2002**, 60**, 157-169.

6. H. Jiang,C. M. Osburn,Z. G. Xiao,G. McGuire and G. A. Rozgonyi, *J Electrochem Soc*, 1992**, 139**, 211-218.

7. J. M. Larson and J. P. Snyder, *Ieee T Electron Dev*, 2006**, 53**, 1048-1058.

8. P. G. McCafferty,A. Sellai,P. Dawson and H. Elabd, *Solid State Electron*, 1996**, 39**, 583-592.

9. T. Morimoto, *IEEE Trans. Electron Devices*, 1995**, 42**, 915-922.

10. K. N. Tu,W. N. Hammer and J. O. Olowolafe, *J Appl Phys*, 1980**, 51**, 1663-1668.

11. V. Bellani,G. Guizzetti,F. Marabelli,A. Piaggi,A. Borghesi,F. Nava,V. N. Antonov,O. Jepsen,O. K. Andersen and V. V. Nemoshkalenko, *Phys Rev B*, 1992**, 46**, 9380-9389.

12. D. Leong,M. Harry,K. J. Reeson and K. P. Homewood, *Nature*, 1997**, 387**, 686-688.

13. Q. R. Hou,Z. M. Wang and Y. J. He, *Appl Phys a-Mater*, 2005**, 80**, 1807-1811.

14. Y. Ichikawa,M. Kobayashi,M. Sasase and T. Suemasu, *Appl Surf Sci*, 2008**, 254**, 7963-7967.

15.   T. Saito,Y. Matsumoto,M. Suzuno,M. Takeishi,R. Sasaki,T. Suemasu and N. Usami, *Appl Phys Express*, 2010**, 3**.

16.   T. Suemasu,K. Morita and M. Kobayashi, *J Cryst Growth*, 2007**, 301**, 680-683.

17.   J. Herfort,H. P. Schonherr and K. H. Ploog, *Appl Phys Lett*, 2003**, 83**, 3912-3914.

18.   Y. Sakuraba,M. Hattori,M. Oogane,Y. Ando,H. Kato,A. Sakuma,T. Miyazaki and H. Kubota, *Appl Phys Lett*, 2006**, 88**.

19.   J. P. DeGrave,A. L. Schmitt,R. S. Selinsky,J. M. Higgins,D. J. Keavney and S. Jin, *Nano Lett*, 2011**, 11**, 4431-4437.

20.   E. Bucher,S. Schulz,M. C. Luxsteiner,P. Munz,U. Gubler and F. Greuter, *Appl Phys a-Mater*, 1986**, 40**, 71-77.

21.   S. P. Murarka, *J Vac Sci Technol*, 1980**, 17**, 775-792.

22.   Q. Huang,A. S. Tan,J. M. Tan,I. S. Goh,Z. Z. Dong,C. K. Ong and T. Osipowicz, *Appl Phys a-Mater*, 2003**, 76**, 439-443.

23.   M. Eizenberg and K. N. Tu, *J Appl Phys*, 1982**, 53**, 6885-6890.

24.   M. Q. Huda and K. Sakamoto, *Mat Sci Eng B-Solid*, 2002**, 89**, 378-381.

25.   S. J. Oh,J. W. Allen and J. M. Lawrence, *Phys Rev B*, 1987**, 35**, 2267-2272.

26.   K. Friemelt,J. F. DiTusa,E. Bucher and G. Aeppli, *Ann Phys-Leipzig*, 1996**, 5**, 175-183.

27.   J. Thomas,J. Schumann,H. Vinzelberg,E. Arushanov,R. Engelhard,O. G. Schmidt and T. Gemming, *Nanotechnology*, 2009**, 20**.

28.   Z. A. He,D. J. Smith and P. A. Bennett, *Phys Rev Lett*, 2004**, 93**.

29.   P. A. Bennett,Z. He,D. J. Smith and F. M. Ross, *Thin Solid Films*, 2011**, 519**, 8434-8440.

30.   H. C. Hsu,W. W. Wu,H. F. Hsu and L. J. Chen, *Nano Lett*, 2007**, 7**, 885-889.

31.   Y. Ohira,T. Tanji,M. Yoshimura and K. Ueda, *Jpn J Appl Phys*, 2008**, 47**, 6138-6141.

32.   R. T. Tung, *Mater Chem Phys*, 1992**, 32**, 107-133.

33.   A. L. Schmitt,M. J. Bierman,D. Schmeisser,F. J. Himpsel and S. Jin, *Nano Lett*, 2006**, 6**, 1617-1621.

34.   Y. C. Lin,Y. Chen,A. Shaios and Y. Huang, *Nano Lett*, 2010**, 10**, 2281-2287.

35.   K. Kang,S. K. Kim,C. J. Kim and M. H. Jo, *Nano Lett*, 2008**, 8**, 431-436.

36.   Y. Q. Qu,J. W. Bai,L. Liao,R. Cheng,Y. C. Lin,Y. Huang,T. Guo and X. F. Duan, *Chem Commun*, 2011**, 47**, 1255-1257.

37.   K. Seo,S. Lee,H. Yoon,J. In,K. S. K. Varadwaj,Y. Jo,M. H. Jung,J. Kim and B. Kim, *Acs Nano*, 2009**, 3**, 1145-1150.

38.   K. Seo,H. Yoon,S. W. Ryu,S. Lee,Y. Jo,M. H. Jung,J. Kim,Y. K. Choi and B. Kim, *Acs Nano*, 2010**, 4**, 2569-2576.

39.   Y. C. Chou,W. W. Wu,L. J. Chen and K. N. Tu, *Nano Lett*, 2009**, 9**, 2337-2342.

40.   Y. C. Chou,W. W. Wu,S. L. Cheng,B. Y. Yoo,N. Myung,L. J. Chen and K. N. Tu, *Nano Lett*, 2008**, 8**, 2194-2199.

41.   Y. C. Lin,Y. Chen,D. Xu and Y. Huang, *Nano Lett*, 2010**, 10**, 4721-4726.

42.   Y. C. Lin,K. C. Lu,W. W. Wu,J. W. Bai,L. J. Chen,K. N. Tu and Y. Huang, *Nano Lett*, 2008**, 8**, 913-918.

43.   K. C. Lu,K. N. Tu,W. W. Wu,L. J. Chen,B. Y. Yoo and N. V. Myung, *Appl Phys Lett*, 2007**, 90**.

44.   W. M. Weber,L. Geelhaar,A. P. Graham,E. Unger,G. S. Duesberg,M. Liebau,W. Pamler,C. Cheze,H. Riechert,P. Lugli and F. Kreupl, *Nano Lett*, 2006**, 6**, 2660-2666.

45.   J. Appenzeller,J. Knoch,M. I. Bjork,H. Riel,H. Schmid and W. Riess, *Ieee T Electron Dev*, 2008**, 55**, 2827-2845.

46.   M. Zhang,J. Knoch,J. Appenzeller and S. Mantl, *Ieee Electr Device L*, 2007**, 28**, 223-225.

47.   Y. Wu,J. Xiang,C. Yang,W. Lu and C. M. Lieber, *Nature*, 2004**, 430**, 61-65.

48.   W. W. Wu,K. C. Lu,K. N. Chen,P. H. Yeh,C. W. Wang,Y. C. Lin and Y. Huang, *Appl Phys Lett*, 2010**, 97**.

49.   Y. C. Chou,W. W. Wu,C. Y. Lee,C. Y. Liu,L. J. Chen and K. N. Tu, *J Phys Chem C*, 2011**, 115**, 397-401.

50.   J. Kedzierski,P. Xuan,E. H. Anderson,J. Bokor,K. Tsu-Jae and H. Chenming In *Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime*, Electron Devices Meeting, 2000. IEDM Technical Digest. International, 2000; 2000; pp 57-60.

1.9. List of Figures
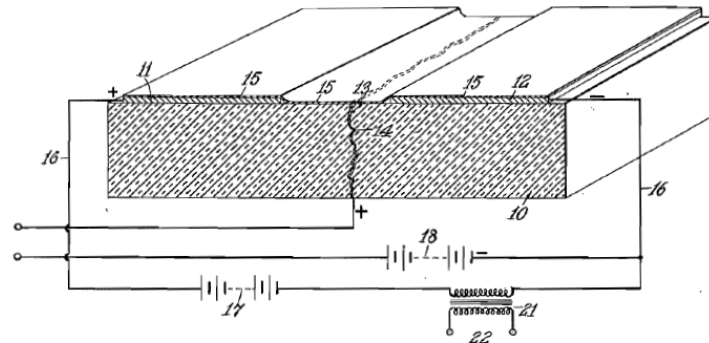
Figure 1-1. Lilienfeld, J. E. Method and apparatus for controlling electric current. US patent 1,745,175 (1925).
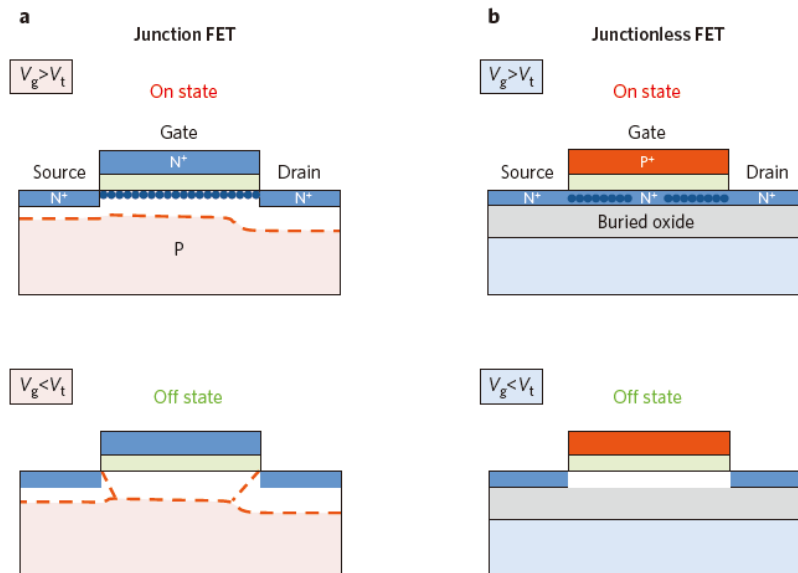
Figure 1-2. Cross sections and operation principles for an n-type junction FET and a junctionless FET. (a) A junction FET is turned on in the (strong) inversion condition, when a channel of minority carriers is formed just under the gate, and junction barriers to their flow are

reduced. (b) In contrast, the on state of a junctionless FET is obtained in 'flat band' conditions, with majority carriers travelling through a highly doped fi
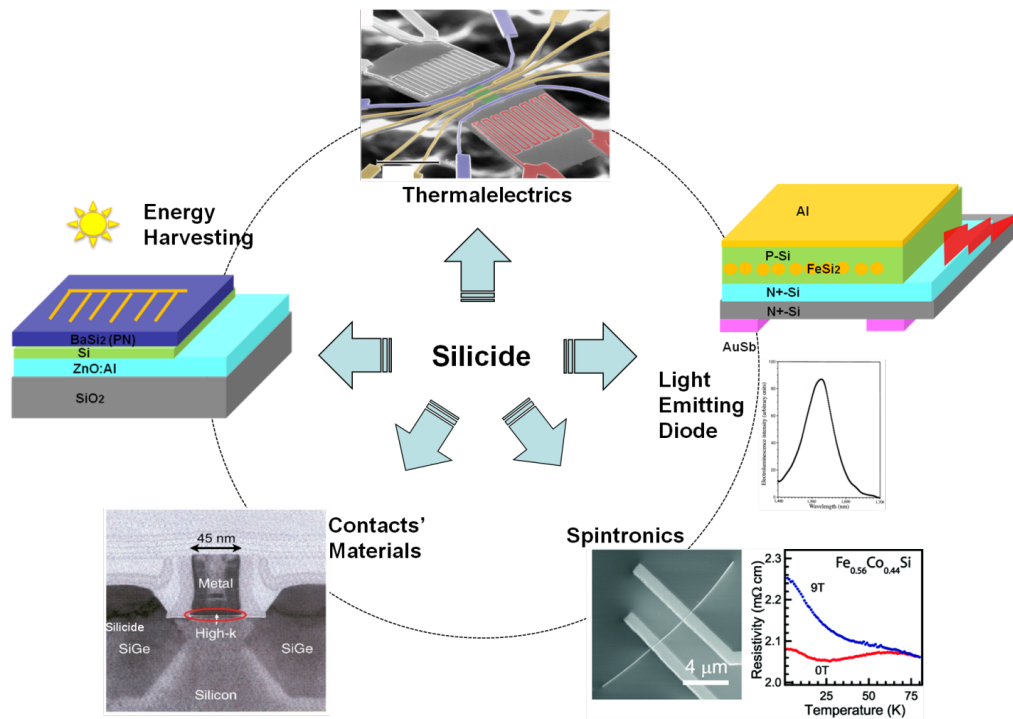
Figure 1-3. Applications of silicide materials.
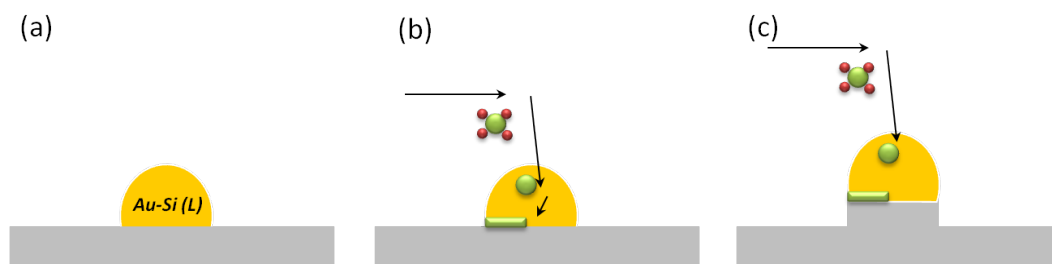
Figure 1-4. Schematic illustration of the Vapor-Liquid-Solid (VLS) process for Si NWs. (a) The formation of An eutectic molten nanoparticle on a heated Si[111] substrate. (b) Introduction of gas precursors (SiH_4 or $SiCl_4$) decompose at the particle surface and Si atoms diffuse into the

nanoparticle which reaches a supersaturated state leading to the onset of ledge nucleation. (c) Continuation of ledge nucleation and propagation at the liquid-solid interface leads the growth of a Si NW with a diameter set by the starting Au nanoparticle diameter.
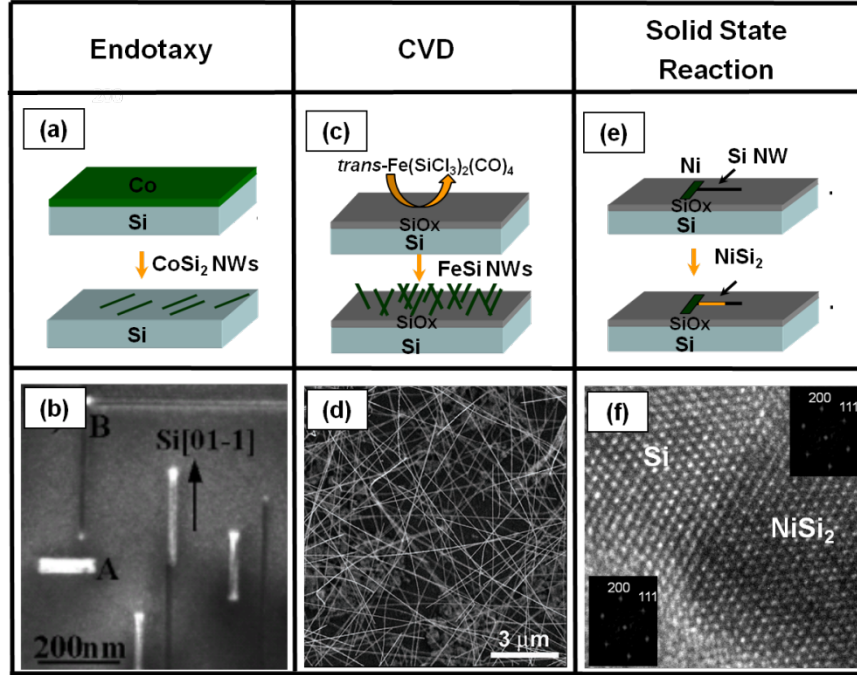
Figure 1-5. Growth technologies of silicide materials: Endotaxy: (a) Formation of NW islandson a heating substrate. (b) Plane-view TEM showing silicide nanostructures with rectangular and NW shapes.[31] (c) Schematic of chemical vapour deposition (CVD) method: FeSi NW was grown from single-source precursor $trans$-Fe(SiCl$_3$)$_2$(CO)$_4$ by chemical vapour deposition. (d) Representative SEM images of FeSi NWs.[35] (e) Formation of Ni silicide NWs by Solid state reaction method. (f) HRTEM image of NiSi$_2$/Si epitaxial interface. Inset images show the fast Fourier transform (FFT) of Si[0-11] zone axis and NiSi$_2$[0-11] zone axis.[36]
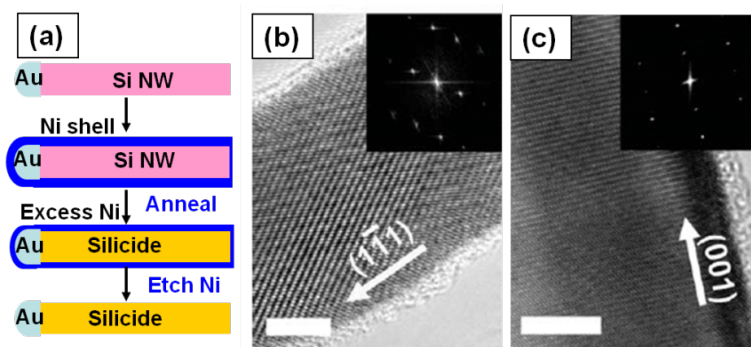
Figure 1-6. Schematic of Ni silicide NW growth by solid state reaction.[49] (a) Growth of fully-silicided NWs: deposit Ni film to cover the Si NW and then annealing at 550°C to transform Si NW into silicide NW. Then remove the excess Ni metal. (b) TEM image of a 20-nm NiSi NW. Inset, Fourier transform of the image showing the [10-1] zone axis of NiSi. (c) TEM image of a 32-nm NiSi NW. Inset, Fourier transform of the image indicating the [2-10] zone axis of NiSi. The scale bars in (b) and (c) are 5 nm.
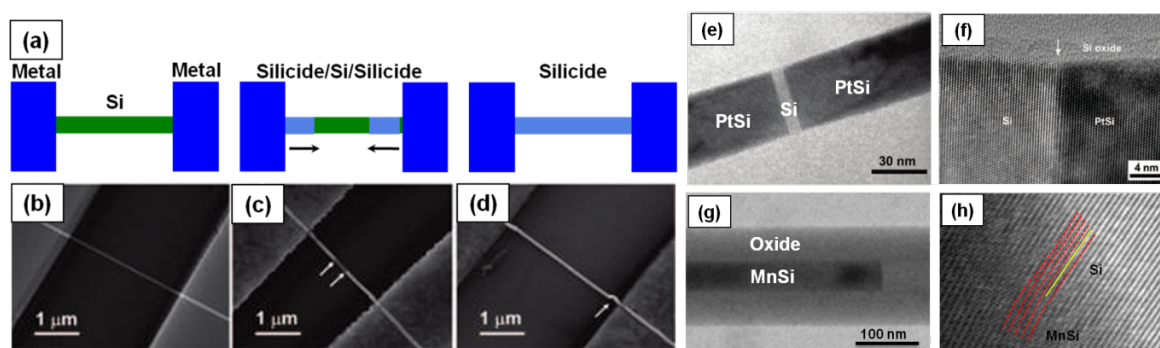
Figure 1-7. TEM analysis for silicide/Si/silicide heterostructure. [36, 44 36, 44 36, 44 36, 44] (a) A schematic shows to form a silicide/Si heterostructure and silicide NWs. (b)(c)(d) show SEM images of a patterned Si NW, partially silicided NW and fully silicided NW, respectively. (e) A TEM image of a PtSi/Si/PtSi heterostructure with only ~8 nm Si region. (f) A higher

1-21

magnification image of a PtSi/Si interface. (g) TEM image of MnSi NW and MnSi/Si interface wrapped in the oxide shell. (h) HRTEM image of MnSi/Si interface.
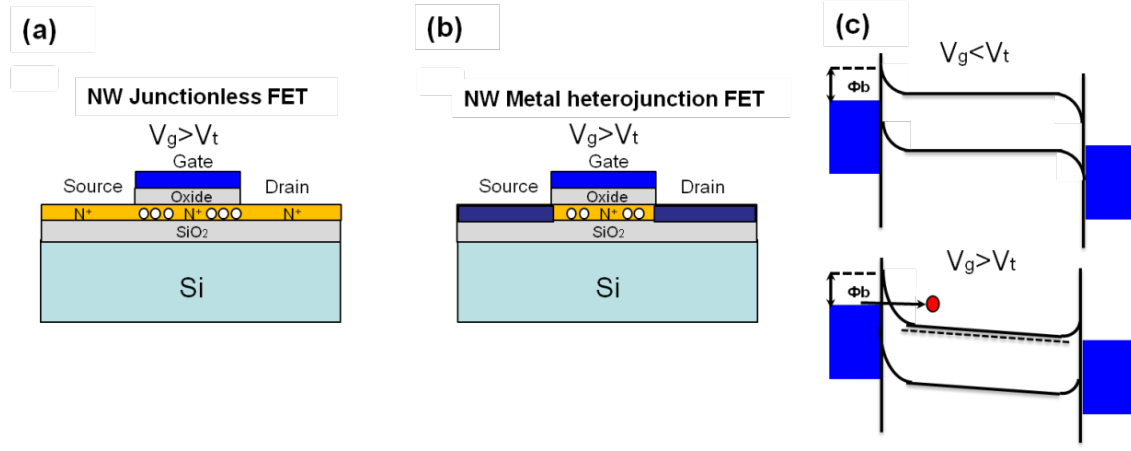
Figure 1-8. Junctionless FET and metal heterojunction FET based on SOI or NW structures**. (a) The junctionless FET(b) Metal heterojunction FET: the source and drain regions are replaced by the metal contact (silicides) ErSi2 is used for n-channel contact. (c) Band diagrams of n-channel metal heterojunction device. With low gate bias (Vg < Vt), source barrier width is too wide for tunneling. With high gate bias (Vg>Vt), large electric fields induce tunneling from the source.

1.10. List of Tables

Materials	Properties	Resistivity ($\mu\Omega$ cm)	Bandgap (eV)
δ-Ni_2Si	Metallic [22]	22	
NiSi	Metallic [22]	10-18	
$NiSi_2$	Metallic [23]	50	
C54-$TiSi_2$	Metallic [22]	14	
Co_2Si	Metallic (Ferromagnet) [24]	40	
CoSi	Metallic (diamagnetic semimetal) [22]	120	
$CoSi_2$	Metallic [22]	24	
Pd_2Si	Metallic [22]	30	
$MoSi_2$	Metallic [22]	100	
WSi_2	Metallic [22]	70	
MnSi	Metallic (Helicalmagnet) [25]	220	
$MnSi_{1.7}$	Semiconducting [25]	4100	0.45-0.47 Indirect 0.78-0.83 Direct
PtSi	Metallic [22]	28	
Pt_2Si	Metallic [22]	6.5	
$ErSi_2$	Metallic [26]	30	
$CrSi_2$	Semiconducting [22]	600	0.35-0.67 Indirect 0.5-0.9 Direct
β-$FeSi_2$	Semiconducting [12]	> 1000	0.83-0.89 Indirect 0.5-0.9 Direct
FeSi	Semiconducting [27,28]	300	0.05
Fe_3Si	Metallic (Ferromagnet) [29]	70	

Table 1-1. Electronic and optical properties of silicide materials.[22-29]

Materials	Schottky Barrier Height (eV)	Materials	Schottky Barrier Height (eV)
$TiSi_2$	0.60	HfSi	0.53
VSi_2	0.64	$TaSi_2$	0.59
$CrSi_2$	0.57	WSi_2	0.65
MnSi	0.65	$ReSi_2$	0.77
$MnSi_{1.7}$	0.67	$OsSi_{1.8}$	0.85
$FeSi_2$	0.68	IrSi	0.93
CoSi	0.68	Ir_2Si_3	0.85
$CoSi_2$	0.64	$IrSi_3$	0.94
Ni_2Si	0.66	Pt_2Si	0.85
NiSi	0.65	PtSi	0.88
$NiSi_2$	0.66	SiAu	0.80
$YSi_{1.7}$	0.39	$GdSi_2$	0.37
$ZrSi_2$	0.55	$DySi_2$	0.37
$NbSi_2$	0.63	$HoSi_2$	0.37
$MoSi_2$	0.65	$ErSi_2$	0.39
Ru_2Si_3	0.72	$ErSi_{1.7}$	0.40
RhSi	0.75		
Pd_2Si	0.71		

Table 1-2. Work function of silicide materials to the n-type silicon.[22]

Chapter 2: Single Crystalline PtSi Nanowires, PtSi/Si/PtSi Nanowire Heterostructures, and Nanodevices

2.1. Introduction

One-dimensional nanostructures, such as nanotubes and nanowires, are attractive building blocks for nanoelectronics since their morphology, size, and electronic properties make them suitable for fabricating both active nanodevice elements and device-to-device interconnects.[1–7] In particular, substantial efforts have been made for the development of nanoscale transistors based on silicon nanowires[8,9] due to their potential to replace conventional planar metal-oxide-semiconductor field-effect transistors (MOSFET) in integrated circuits[10,11] or to open new opportunities in flexible macroelectronics[12–14] and highly sensitive biosensors.[15,16] Making reliable electrical contact to individual nanowire devices is one of the key factors that determine the device performance and reliability. Lithographically defined metal contacts are most often used in silicon nanowire transistors, which is, however, limited in at least two respects: (1) the much larger size scale of lithographically defined metal contact limits the scaling potential of the silicon nanowire devices; (2) the interface states between the silicon nanowire and metal contact often lead to Fermi-level pinning and result in a relatively large Schottky barrier for the device.[17] As a result, doped nanowires with a certain doping concentration (e.g., >10^{17}/cm3) are typically used in order to make satisfactory source drain contact, which prevent one from making high-performance transistors based on intrinsic silicon nanowires. The formation of metal silicide nanowires and silicide/ silicon heterostructures represents an interesting approach to address the above problems. Nickel silicide has been reported[18–20] and is being used as a contact material for

silicon nanowire transistors.[18,21,22] Being chemically stable in ambient or oxidizing environment, platinum is an interesting interconnecting material for nanoscale electronics where surface to volume ratio is large and the surface chemical stability is important. Additionally, the formation of platinum silicide (PtSi) is of interest because it has a very low barrier height of ~0.2 eV on the valence band of silicon and is an attractive choice for ohmic contacts to p-channel Si nanowire transistors.[23] Platinum silicide nanowires have been reported recently, but without detailed characterization of their properties.[24] Here, we report the formation of single crystal PtSi nanowires, PtSi/Si/PtSi nanowire heterostructures, and nanodevices from such heterostructures. Scanning electron microscopy (SEM) studies show that silicon nanowires can be converted into single crystal PtSi nanowires through controlled reactions between lithographically defined Pt pads and Si nanowires. High-resolution transmission electron microscope (HRTEM) studies show that PtSi/Si/PtSi heteorstructure has clean, atomically sharp interfaces with an epitaxial relationship of Si[1-10]//PtSi[010] and Si(111)// PtSi(101). Electrical measurements show that the pure PtSi nanowires have a low resistivity of ~28.6 $\mu\Omega\cdot$cm, and high failure current density >10^8A/cm2. Furthermore, using single crystal PtSi/Si/PtSi nanowire heterostructures with low PtSi/Si energy barrier, we have fabricated high-performance p-channel enhancement mode field-effect transistors from intrinsic silicon nanowires, in which the source and drain contacts are defined by the metallic PtSi nanowire regions and the gate length is defined by the Si nanowire region.

2.2. Experimental

Silicon nanowires were prepared on a silicon wafer by the vapor–liquid–solid method using Au clusters as the catalyst.[25–27] The silicon nanowires are typically single crystals with diameters

ranging from 30 to 60 nm, lengths greater than 10 μm, and growth axes along [111] directions. The Si nanowire device with platinum contacts was fabricated on Si/Si$_3$N$_4$ substrate using e-beam lithography and e-beam evaporation (Figure 2-1a). Prior to platinum deposition, the sample was etched in buffered hydrofluoric acid for 5 s to remove native oxide in the contact region. To allow platinum to diffuse into the silicon nanowire and form partially (Figure 2-1b) or fully silicidized (Figure 2-1c) PtSi nanowire, the device was annealed in forming gas at 520 °C with a rapid thermal processor for various periods of time. Before annealing, a SEM image of the device shows a uniform contrast along the axis of the nanowire (Figure 2-1d). After the device was annealed in forming gas for 30 s, clear contrast developed along the wire axis with two brighter sections emerging from both ends of the nanowire near the platinum pads (Figure 2-1e). A darker section remains between the two brighter sections, corresponding to the unreacted silicon nanowire. These results suggest that a PtSi/Si/PtSi nanowire heterostructure is formed through reaction between the silicon nanowire and two platinum contact pads. This is attributed to the fact that many platinum atoms are able to dissolve into silicon through the contacts between silicon nanowire and platinum pads so that supersaturation can be reached; thereby, nucleation and growth of platinum silicide occur at both platinum pads. Upon further annealing, the two brighter sections (PtSi) converged, and the darker section (Si) disappeared. At this point, all silicon is consumed and a silicon nanowire is fully transformed into a PtSi nanowire (Figure 2-1f). Occasionally, a curved section is seen near the contact pads (Figure 2-1f), which can be attributed to strain resulting from the volume expansion during the silicidation process. Transformation of Si nanowire into PtSi nanowires roughly increases the volume by 50%. However, our studies indicate that no significant diameter increase is observed (<10%). For mass conservation, this means that the silicon atom back diffusion is present in our system, in which

silicon atoms diffuse toward platinum pads and get consumed in or near the pads. Additional studies are required to further understand this phenomenon.

2.3. Results & Discussion

2.3.1. Epitaxial relationship of PtSi formation within a silicon nanowire

To understand the formation and structure of the PtSi/Si/PtSi nanowire heterostructure, we have used lattice resolved transmission electron microscopy (TEM) images to determine the crystal structure and atomic epitaxial relationships. To prepare TEM samples, silicon nanowires devices were prepared on silicon grids with a square opening covered with a window of a glassy Si_3N_4 film. The thickness of the Si_3N_4 film is about 30 nm so that it is transparent to the electron beam and does not interfere with the imaging of the nanowires. Lattice resolved images were taken with a JEOL 3000F high-resolution transmission electron microscope. A high-resolution TEM (HRTEM) image (Figure 2-2a) shows that there are clean interfaces between PtSi/Si with an approximately 2 nm silicon oxide shell surrounding both the silicon and platinum silicide regions, suggesting the growth of platinum silicide nanowire is confined in the preformed native silicon oxide shell. On the basis of the TEM studies, the silicide material is identified to be single crystal PtSi phase with an orthorhombic structure with lattice constants $a=0.5939$ nm, $b=0.5596$ nm, and $c=0.3604$ nm. A HRTEM image and its fast Fourier transform (FFT) (Figure 2b and insets) show the Si/PtSi epitaxial interface is parallel to the (111) plane of Si as well as the (101) plane of PtSi. Thus, the growth direction of PtSi is normal to the (101) plane. The crystallographic orientation relationships between Si and PtSi are Si[1-10]//PtSi[010] and

Si(111)//PtSi(101). Across the epitaxial interface, the largest lattice mismatch is between the Si(002) plane (d= 0.271 nm) and the PtSi(200) plane (d=0.297 nm) with a relative mismatch of about 8.8%. Notably, despite this exceedingly large lattice mismatch, no apparent dislocations or other defects are seen across the interface. These results demonstrate that a sharp and atomically smooth interface is obtained in our Si/PtSi nanowire heterostructure. In stark contrast, atomically uneven interfaces are often seen in previously reported PtSi thin films grown on silicon (111) surfaces due to large lattice mismatch. The clean and sharp interface in nanowire heterostructures might be attributed to increased tolerance of lattice strain and the difficulty to nucleate a dislocation at nano-scale, which is an interesting subject for further investigations. The formation of atomically sharp PtSi/Si/PtSi heterostructures can open many exciting opportunities in nanoscale device engineering. For example, through controlled reactions, the length of the silicon region in nanowire PtSi/Si/PtSi heterostructures can be precisely controlled down to the sub-10-nm regime (Figure 2-2c). This is significant since the sub-10-nm length scale here is defined by controlled chemical reaction rather than by lithography and thereby can open new opportunities for sub-10-nm device engineering when the process is further optimized. To explore single-crystal PtSi nanowires and atomically sharp PtSi/Si/PtSi nanoheterostructures in nanoscale electronics, it is important to understand their electrical transport characteristics.

2.3.2. Electrical transport properties of single crystal PtSi nanowires

We have carried out the electrical transport studies on individual nanowires before and after PtSi formation. Current–voltage (I-V) measurements show that as-fabricated intrinsic Si nanowire devices with platinum contacts and partly silicidized nanowires exhibit exceedingly high resistance essentially beyond our instrument measurement range (>1 TΩ) (black line in Figure 2-

3a). Importantly, the fully silicidized nanowires exhibit perfect linear current-voltage relation, with current typically exceeding 100 μA at 100 mV of bias voltage. The two-terminal linear *I-V* curve of a 50 nm PtSi nanowire device gives a linear resistance of 627 Ω (red line in Figure 2-3a). At this low resistance, contact resistance and electrical lead resistance may start to contribute to a significant fraction of the total resistance. To exclude this extrinsic series resistance and accurately determine the PtSi nanowire resistance, we have carried out four-terminal measurement (inset and blue line in Figure 2-3a), which gives a resistance of 376 Ω for the device. The high current and low resistance observed in the annealed device clearly suggests the metallic behavior of PtSi nanowires. Indeed, calculation of the PtSi resistivity based on four-terminal measurement gives a value of 28.6 $\mu\Omega\cdot$cm. Significantly, this value compares favorably to the previously reported values in PtSi thin film materials (45–68 $\mu\Omega\cdot$cm),[30] which can be attributed to the single crystalline and virtually defect-free structure in our PtSi nanowires as opposed to polycrystalline and defect-prone PtSi films. To explore the PtSi nanowire as metallic interconnects for silicon nanodevices, it is also important to characterize the maximum current density of individual nanowires. Our measurement shows that an individual PtSi nanowire can typically carry more than 1 mA current before electrical breakdown. For example, the current–voltage curve of a 45 nm PtSi nanowire at large bias shows that the current reaches 2.7 mA before electrical breakdown (Figure 2-3b). This high current through a single nanowire corresponds to a current density 2×10^8A/cm^2, comparable to recently reported values in nickel silicide nanowires.[18] SEM observation of the failed device shows the breakdown occurs around the center of the nanowire (inset Figure 2-3b), where one expects the least heat dissipation and highest temperature.

2.3.3. PtSi/i-Si/PtSi nanowire heterostructures as high performance p-channel enhancement mode transistors

The excellent electrically conductive characteristics and high breakdown current density make PtSi a natural candidate as conductive interconnects in silicon nanoelectroncs. Additionally, PtSi has a work function of 4.97 eV, aligning well with the silicon valence band with a small energy barrier of ~0.2 eV and, therefore, can be used as nearly perfect ohmic contact for p-channel Si nanowire transistors (Figure 2-4a). Additionally, the formation of atomically clean Si/PtSi interfaces prevents Fermi level pinning and helps to maintain a low Schottky barrier determined by work function rather than by interface states. This has enabled us to fabricate high-performance nanowire transistors from intrinsic silicon naowires using PtSi as the source and drain contacts. To make the device (Figure 2-4b), a 7 nm thick layer of HfO_2 was deposited on the surface of the partially silicidized PtSi/Si/PtSi device using atomic layer deposition process to form gate dielectrics, and a top Cr/Au electrode was defined with e-beam lithography and deposited using e-beam evaporation. Electrical transport measurement on the device shows nearly perfect transistor characteristics. Figure 2-4c shows drain current (I_D) versus drain-source bias voltage (V_D) relations at various gate voltages (V_G) in steps of 0.25 V. The device shows typical p-channel enhancement mode (normally off) transistor behavior.[17] I_D increases linearly with V_D at low V_D and saturates at higher V_D. It is important to note that a nearly perfect linear relationship is observed in the I_D-V_D plot in the low bias region, which suggests that a satisfactory Ohmic contact is achieved for hole transport in the intrinsic silicon nanowire device due to a very low Schottky barrier. The plot of I_D versus V_G (Figure 2-4d) at constant V_D=-0.2, -0.4, -0.6, -0.8, and -1.0 shows little current can pass through the device when the gate voltage is

below a threshold voltage of approximately -2.0 V, and I_D increases nearly linearly when the gate voltage increases in the negative direction beyond the threshold voltage.

To gauge the device performance, it is important to analyze some key device parameters including: transconductance, mobility, on/off current ratio, and subthreshold swing. High transconductance is a critical measure of transistor performance and determines voltage gains of transistor-based devices including amplifiers and logic circuits. The maximum transconductance of our device in the saturation region is ~12 μS. Assuming the effective channel width equals the nanowire diameter (40 nm), we obtain a normalized transconductance of ~0.3 mS/μm. Importantly this value is significantly better than those reported previously for chemically synthesized silicon nanowire devices and is nearly comparable to the state-of-the-art MOSFET devices (~0.6 mS/μm). We note a superior value has been reported recently on nanowire transistors, which is however based on intrinsically higher mobility material (Ge/Si core-shell structure). Additionally, considering the present device has a relatively long channel length (2.3 μm), the transconductance can be further improved by reducing the channel length. To estimate the carrier mobility in our nanowire device, we have modeled the device using standard MOSFET equations. In the low bias linear region of the I_D-V_G curves, the field-effect mobility μ_h for holes can be deduced from $dI_D/dV_G = \mu_h C_G V_D/L$,[2,17] where C_G is the gate capacitance and L is the channel length. Using calculated C_G of 2.3 fF for the device, we obtain a field-effect hole-mobility of 168 cm^2/V·s, which is closely comparable to p-type single crystal silicon materials such as silicon-on-insulator MOSFET devices (~180 cm^2/V·s). The plot of the -I_D-V_G curve in the logarithmic scale (inset, Figure 2-4d) shows that I_D decreases exponentially below the threshold voltage, and upon reaching a minimum of ~0.2 pA, it increases again upon further sweeping the gate voltage toward the positive direction. This behavior suggests ambipolar

transport, with the left branch corresponding to hole transport (p-type) and the right branch corresponding to electron transport (n-type). The ambipolar transport is typical of a metal-contacted Schottky barrier MOSFET and has been previously observed in silicide contacted silicon on insulator devices and nanowire devices. [33,35,36] The plot shows that the transistor has a maximum on/off current ratio greater than 7 orders of magnitude. The exponential decrease in current defines a key transistor parameter, the subthreshold swing $S= -dV_G/d \log I_D$. For the hole transport branch (left), the subthrehold swing ranges from 110 mV/decade near the current minimum to 220 mV/ decade near the threshold, and for the electron transport branch (right), a constant subthreshold swing of 320 mV/ decade is observed. In conventional MOSFETs, subthreshold transport is dominated by thermal emission with the swing S determined by $S= (k_BT/e) \ln[(10)(1 + \alpha)]$, where T is temperature, k_B is Boltzmann's constant, e is elementary charge, and α depends on capacitances in the devices and is 0 when the gate capacitance is much larger than other capacitances such as interface trap state capacitance.[17] The lowest theoretical limit for S is therefore $S= (kBT/e) \ln(10) \sim 60$ mV/decade at room temperature. The existence of trapping states in gate dielectrics can lead to a larger than ideal substhreshold swing. Additionally, it is also often seen that a Shottky barrier MOSFET has a larger subthreshold swing due to Schottky barrier limited carrier injection. Both gate dielectric (native silicon oxide and HfO_2) interface trapping states and the Schottky barrier may contribute to the nonideal subthreshold swing observed in our devices. In hole transport branch (p-branch), the transport near the current minimum (with subthreshold swing of ~110 mV/ decade) is dominated by the thermal emission, and the transport near the threshold (with swing ~220 mV/decade) is probably more also affected by the existence of a small Schottky barrier. Therefore, the subthreshold swing can be improved by reducing the interface trapping states with improved gate dielectrics

and by further reducing the effective Schottky barrier with alternative contact materials (e.g., IrSi)[23] or dopants near the contact region.[35,36] The significant larger swing (~320 mV/decade) in the electron transport branch (n-branch) is due to a much larger Schottky barrier for electron transport.[35,36] The existence of a larger Schottky barrier for electrons than for holes can also be seen from output characteristics. The linear I_D-V_D relation (in low bias region) in hole transport (Figure 2-4c) suggests that a satisfactory Ohmic contact is achieved due to a very small Schottky barrier. In contrast, the output characteristics of electron transport show a highly nonlinear I_D-V_D relation due to a much larger Schottky barrier. Furthermore, the on-current for electron transport is at least 1 order of magnitude smaller than the that for hole transport, suggesting a Schottky barrier limited electron transport. These studies signify that PtSi indeed has a very small barrier for hole transport and much larger barrier for electron transport in our nanowire device, consistent with the expected Schottky barrier height of ~0.2 eV for holes and ~0.9 eV for electrons.[23] The experimental determination of the exact barrier height, however, requires additional variable temperature measurements in future studies. These results clearly demonstrate a high-performance p-channel enhancement mode transistor has been obtained from a PtSi/Si/PtSi heterostructure using intrinsic silicon nanowires. We note the silicon nanowire transistors have been reported in a number of previous publications.[8–15,18,21,22] However, in most of these reports, chemically doped silicon nanowires are used in order to ensure a reasonable source-drain contact and decent transistor characteristics. Therefore, most of these devices are normally on devices. Transistors based on instrinsic nanowires have been reported occasionally,[8,21,22] but often with nonlinear I-V characteristics and/or limited performance due to significant energy barrier at the contact. The recently reported nanowire transistors from Si/Ge core-shell nanowires did not involve chemical doping but did use Si/Ge core-shell structure for

modulation doping to ensure a good source-drain contact and high device performance.[33] The fabrication of a normally off device from intrinsic materials is important for low-power consumption and can lead to better device performance (e.g., higher mobility) due to the reduced number of ionized scatter centers. Notably, our results represent the first report of high performance normally off transistors from intrinsic silicon nanowires.

2.4 Conclusion

We have grown single crystal PtSi nanowires and PtSi/Si/PtSi nanowire heterostructures. TEM studies show that the heterostructures have atomically sharp interfaces free of defects. Electrical measurement of PtSi nanowires shows a low resistivity of $\sim$28.6 $\mu\Omega\cdot$cm and a high breakdown current density beyond 10^8 A/cm2. Furthermore, using single-crystal PtSi/Si/PtSi nanowire heterostructures with atomically clean interfaces, we have fabricated p-channel enhancement mode transistors with the best reported performance for intrinsic silicon nanowires to date. The ability to form single-crystal PtSi nanowires and defect-free PtSi/Si/PtSi heterostructures with controlled nanoscale dimension can open new opportunities in nanoscale device engineering.

2.5. References

(1) McEuen, P. L.; Fuhrer, M. S.; Park, H. *IEEE Trans. Nanotechnol.* **2002**, *1*, 78–85.

(2) Avouris, P. *Acc. Chem. Res.* **2002**, *35*, 1026–1034.

(3) Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. J. *Nature* **2003**, *424*, 654–657.

(4) Huang, Y.; Lieber, C. M. *Pure Appl. Chem.* **2004**, *76*, 2051–2068.

(5) Yang, P. *MRS Bull.* **2005**, *30*, 85–91.

(6) Wang, Z. L. *Adv. Mater.* **2007**, *19*, 889–892.

(7) Lu, W.; Lieber, C. M. *Nat. Mater.* **2007**, *6*, 841–850.

(8) Cui, Y.; Duan, X.; Hu, J.; Lieber, C. M. *J. Phys. Chem. B* **2000**, *104*, 5213–5216.

(9) Zheng, G.; Lu, W.; Jin, S.; Lieber, C. M. *Adv. Mater.* **2004**, *16*, 1890–1893.

(10) Huang, Y.; Duan, X.; Cui, Y.; Lauhon, L.; Kim, K.; Lieber, C. M. *Science* **2001**, *294*, 1313–1317.

(11) Zhong, Z.; Wang, D.; Cui, Y.; Bockrath, M. W.; Lieber, C. M. *Science* **2003**, *302*, 1377–1379.

(12) Duan, X.; Niu, C.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. *Nature* **2003**, *425*, 274–278.

(13) Duan, X. *MRS Bull.* **2007**, *32*, 134–141.

(14) Javey, A.; Nam, S.; Friedman, R. S.; Yan, H.; Lieber, C. M. *Nano Lett.* **2007**, *7*, 773–777.

(15) Patolsky, F.; Zheng, G.; Hayden, O.; Lakadamyali, M.; Zhuang, X.; Lieber, C. M. *Proc. Natl. Acad. Sci. U.S.A.* **2004**, *101*, 14017–14022.

(16) Patolsky, F.; Timko, B. P.; Zheng, G.; Lieber, C. M. *MRS Bull.* **2007**, *32*, 142–149.

(17) Sze, S. M. *Physics of Semiconductor Devices*; John Wiley & Sons: New York, 1981.

(18) Wu, Y.; Xiang, J.; Yang, C.; Lu, W.; Lieber, C. M. *Nature* **2004**, *430*, 61–65.

(19) Lu, K. C.; Tu, K. N.; Wu, W. W.; Chen, L. J.; Yoo, B. Y.; Myung, N. V. *Appl. Phys. Lett.* **2007**, *90*, 253111.

(20) Lu, K. C.; Wu, W. W.; Wu, H. W.; Tanner, C. M.; Chang, J. P.; Chen, L. J.; Tu, K. N. *Nano Lett.* **2007**, *7*, 2389–2394.

(21) Weber, W. M.; Geelhaar, L.; Graham, A. P.; Unger, E.; Duesberg, G. S.; Liebau, M.; Pamler, W.; Cheze, C.; Riechert, H.; Lugli, P.; Kreupl, F. *Nano Lett.* **2006**, *6*, 2660–2666.

(22) Byon, K.; Tham, D.; Fischer, J. E.; Johnson, A. T. *Appl. Phys. Lett.* **2005**, *87*, 193104.

(23) Bucher, E.; Schulz, S.; Lux-Steiner, M. C.; Munz, P.; Gubler, U.; Greuter, F. *Appl. Phys. A: Mater. Sci. Process.* **1986**, *40*, 71–77.

(24) Liu, B.; Wang, Y.; Dilts, S.; Mayer, T. S.; Mohney, S. E. *Nano Lett.* **2007**, *7*, 818–824.

(25) Morales, A. M.; Lieber, C. M. *Science* **1998**, *279*, 208–211.

(26) Cui, Y.; Lauhon, L. J.; Gudiksen, M. S.; Wang, J.; Leiber, C. M. *Appl. Phys. Lett.* **2001**, *78*, 2214–2216.

(27) Hannon, J. B.; Kodambaka, S.; Ross, F. M.; Tromp, R. M. *Nature* **2006**, *440*, 69–71.

(28) Kawarada, H.; Ishida, M.; Nakanishi, J.; Ohdomari, I.; Horiuchi, S. *Philos. Mag. A* **1986**, *54*, 729–741.

(29) Kästner, G.; Gösele, U. *Philos. Mag.* **2004**, *84*, 3803–3824.

(30) Xu, D. X.; Xu, J. P.; McCaffrey, S. R.; Das, G. C.; Aers, L. E. *Appl. Phys. Lett.* **1996**, *68*, 3588–3590.

(31) Freeouf, J. L. *Solid State Commun.* **1980**, *33*, 1059–1061.

(32) Chau, R. *IEEE Electron Device Lett.* **2004**, *25*, 408–410.

(33) Xiang, J.; Lu, W.; Hu, Y.; Wu, Y.; Yan, H.; Lieber, C. M. *Nature* **2006**, *441*, 489–493.

(34) Mizuno, T.; Sugiyama, N.; Kurobe, A.; Takagi, S. *IEEE Trans. Electron Devices* **2001**, *48*, 1612–1618.

(35) Zhang, M.; Knoch, J.; Zhao, Q. T.; Breuer, U.; Mantl, S. *Solid State Elecron.* **2006**, *50*, 594–600.

(36) Knoch, J.; Zhang, M.; Appenzeller, J.; Mantl, S. *Appl. Phys. A* **2007**, *87*, 351–357.

2.6. List of Figures
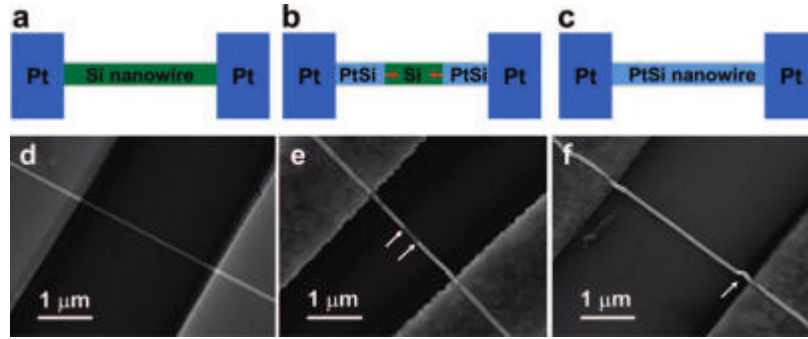
Figure 2-1. Formation of PtSi nanowire and PtSi/Si/PtSi nanoheterostructures. (a-c) Schematic illustrations depicting growth of a PtSi/Si/PtSi nanoheterostructure and PtSi nanowires through controlled reaction between silicon nanowires and platinum contact pads. (d) SEM image of a silicon nanowire device with two platinum contact pads before reaction. (e) SEM image of a PtSi/Si/PtSi nanoheterostructure obtained through partial silicidation of the silicon nanowire after annealing at 520 °C for 30 s. Two arrows highlight two PtSi/Si interfaces. (f) SEM image of a PtSi nanowire after complete silicidation by annealing at 520 °C for 60 s. The arrow highlights a curved section near the contact pads due to strain resulting from volume expansion.
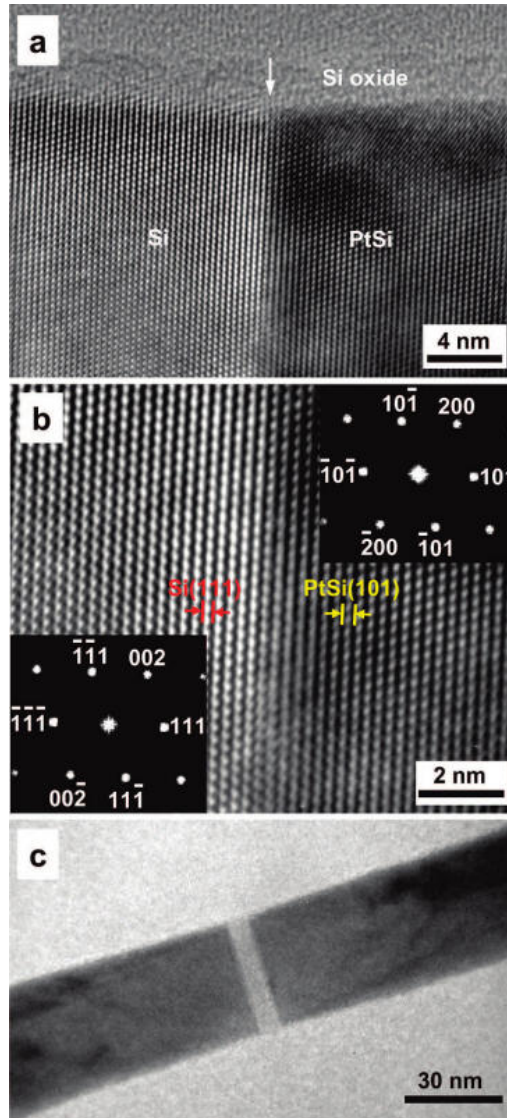
Figure 2-2. Epitaxial relationship of PtSi formation within a silicon nanowire. (a) A HRTEM image showing clean and sharp interfaces between PtSi and Si. The arrow highlights the Si/PtSi interface. (b) A higher magnification image of a PtSi/Si interface illustrating the epitaxial relationship. The insets are fast Fourier transform (FFT) patterns confirming the Si[1-10] zone axis and PtSi[010] zone axis, respectively. (c) A TEM image of a PtSi/Si/PtSi heterostructure with only an 8 nm silicon region.
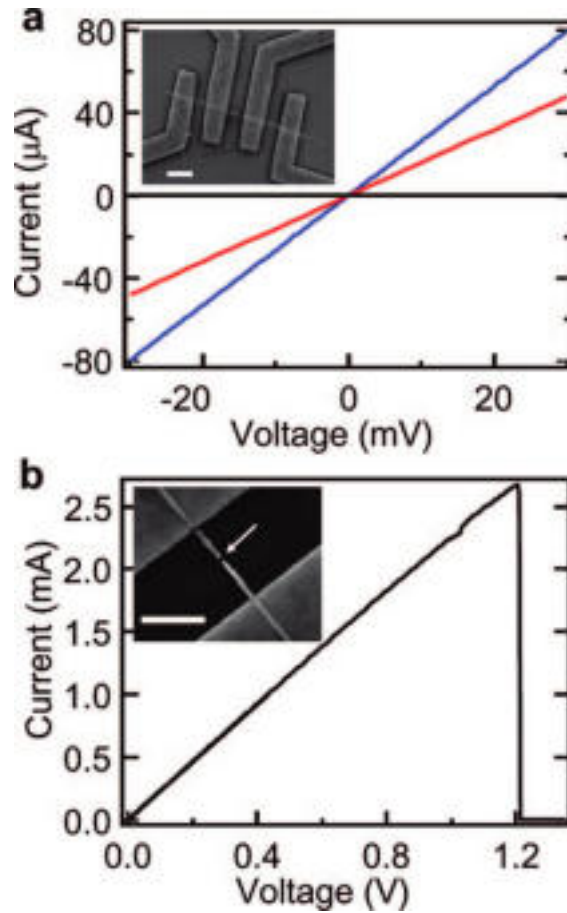
Figure 2-3. Electrical transport properties of single crystal PtSi nanowires. (a) Current–voltage relation recorded on a 50 nm diameter nanowire device, with the black line corresponding to the device before annealing and red line to the device after complete formation of PtSi nanowire, and the blue line to the *I-V* relation of a four-terminal measurement which excludes the contact and lead resistance. The inset shows an SEM image of the device used for four-terminal measurement (scale bar equals 3 μm). (b) *I-V* recorded with large applied bias voltage. The rapid drop in current at 1.2 V corresponds to the breakdown point of the PtSi nanowire device. Inset: SEM image of the nanowire after breakdown. The arrow highlights the point where breakdown occurred (scale bar equals 1 μm).
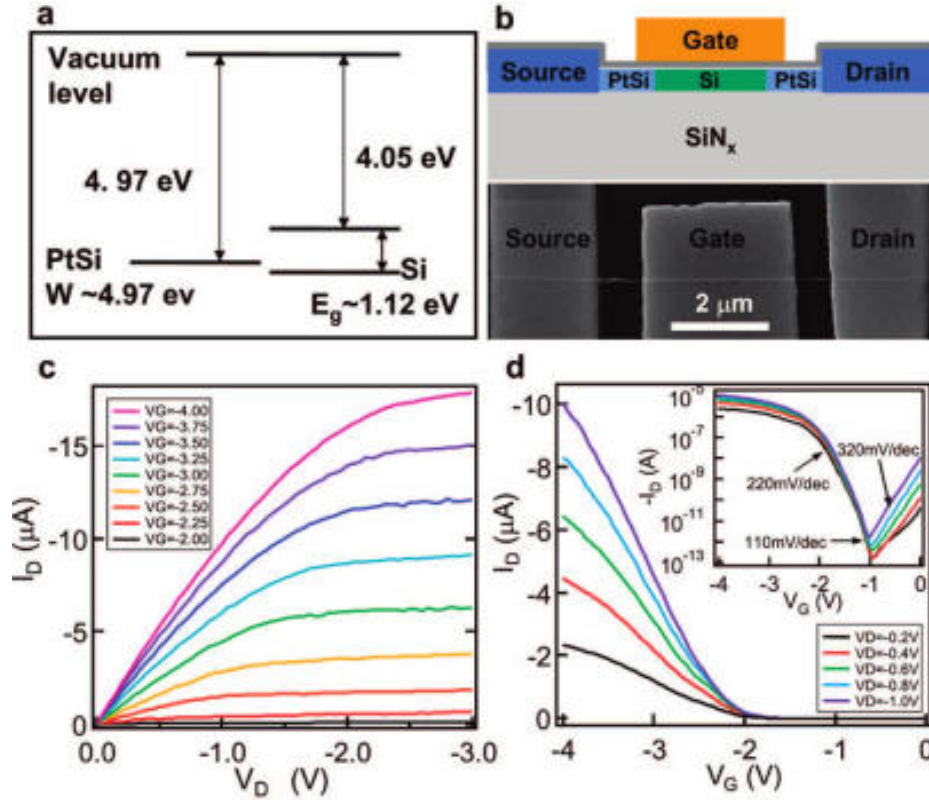
Figure 2-4. PtSi/i-Si/PtSi nanowire heterostructures as high performance p-channel enhancement mode transistors. (a) Relative energy band alignment between PtSi and Si. (b) (top) Schematic of PtSi/i-Si/PtSi nanowire heterostructure device with HfO_2 as gate dielectrics. (bottom) SEM images of a device (scale bar, 2 μm). (c) Drain current (I_D) vs drain-source voltage (V_D) at increasing negative gate voltages (V_{GS}) in steps of 0.25 V starting from the bottom at V_G= -2.0 V. (d) I_D vs V_G at V_D= -0.2, –0.4, –0.6, –0.8, –1.0 V. The inset shows $-I_D$ vs V_G in the exponential scale, highlighting the on/off ratio $>10^7$, and ambipolar transport with a subthreshold swing of 110–220 mV/decade for hole transport and 320 mV/decade for electron transport.

Chapter 3: Detection of Spin Polarized Carrier in Silicon Nanowires with Single Crystal MnSi as Magnetic Contact

3.1. Introduction

The spin injection, transport and detection in semiconductors is crucial to spintronics which aims to use spin orientation instead of electron charges for information processing.[1-4] Compared to the conventional planar metal-oxide-semiconductor field-effect transistors (MOSFET), a spin FET controls charge current through flipping spin orientations with the gate voltage or controlling the relative magnetization configuration of the ferromagnetic contacts instead of by depleting charge carriers in the conducting channel.[5] Therefore a spin FET has the potential to operate with less power consumption, at much faster speed and with more degrees of freedom. However, it is non-trivial to achieve effective spin injection and detection in a spin FET device.[6-8] A main obstacle in achieving an effective spin injection is the conductivity mismatch between the ferromagnetic contact and the semiconductor.[9] This can be circumvented by introducing a spin-dependent interfacial layer, in the form of a Schottky barrier or insulating tunneling layer, e.g., MgO or Al_2O_3.[1-2] In addition, how to avoid the spurious noise to detect the spin is another key issue. Recently, spin injection and detection in the silicon bulk material has been carried out by nonlocal technique,[1-4] where a four-terminal device configuration was employed to separate the spin detecting terminals away from the applied electrical field to avoid local Hall effect and to obtain clear spin signals. However, the device structure of nonlocal technique (four terminals) is still far from application due to the challenges in scaling. A spinFET structure with ultra-short channel (~30 nm silicon channel) similar to a conventional MOSFET, has been proposed by

replacing the source and drain contacts with ferromagnetic materials.[10,11] This device structure represents a promising design for spin transistors and has attracted considerable attentions to search for suitable ferromagnetic contacts with fewer interface defects to achieve effective spin injection.

Various materials have been explored as the spin conducting channel in spinFET applications, including: common semiconducting materials (silicon or germanium), III-V materials such as GaAs or InAs that have high carrier mobility and stronger spin-orbit coupling,[12,13] dilute magnetic semiconducting (DMS)[14-16] materials such as transition metal doped ZnO or GaN with higher Currie temperature (> 300 K). Additionally, a range of nanomaterials such as nanowires[17,18] or quantum dots[19] have also recently been explored for spin electronic applications. Among these materials, Si-based spintronics attracts much interest for its excellent properties such as long spin relaxation time, large diffusion length,[20,21] as well as its compatibility with industrial process. Despite these possible advantages, there are limited studies on the spin transport in the silicon nanostructure to date, largely due to the lack of suitable magnetic contact materials for effective spin injection and detection in nanoscale silicon devices.

On the other hand, the formation of single crystalline silicide/silicon/silicide nanowire heterostructure has been reported as an interesting approach to make nearly perfect Ohmic and Schottky contact to silicon nanowires.[22-24] Previous studies have demonstrated that single crystalline metal silicide can be readily obtained in the nanowire structure with nearly perfect silicide/silicon interface. In addition, the silicon channel length is scalable and can be controlled down to a few nanometers in the silicide/silicon/silicide nanowire heterostructure. Exploiting ferromagnetic silicide, such as manganese monosilicide (MnSi), the nanosilicide technique can be used to create single-crystal MnSi/Si/MnSi nanowire heterostructure with nearly perfect

ferromagnetic-semiconductor interface and variable silicon channel length, and therefore allow the spin transport studies in short-channel silicon nanowire devices with Schottky tunneling junction. Manganese silicide, (MnSi) is an intermetallic compound with a cubic B20 structure (a=0.4556 nm),[25,26] and a paramagnetic to ferromagnetic transition at Currie temperature (T_c) ~29.6 K. Density of states (DOS) calculation has also suggested that considerable spin polarization up to 45% can be achieved in MnSi thin films.[27] Manganese silicide thus represents an interesting material to explore as the ferromagnetic contacts in nanoscale silicon spintronic devices.

Here, we report the formation of single crystal MnSi nanowires, MnSi/Si/MnSi nanowire heterostructures, and nanodevices from such heterostructures. Scanning electron microscopy (SEM) studies show that silicon nanowires can be converted into single crystal MnSi nanowires through controlled solid state reaction. High-resolution transmission electron microscope (HRTEM) studies show that MnSi/Si/MnSi heterostructure has clean, atomically sharp interfaces with an epitaxial relationship of Si $[3\bar{1}\bar{1}]$ //MnSi $[1\bar{2}0]$ and Si(345)//MnSi $(\bar{2}\bar{1}4)$. Magnetoresistance (MR) studies show that the single crystal MnSi nanowire exhibits lower resistance at high magnetic field (negative MR). Furthermore, using single crystal MnSi/p-Si/MnSi nanowire heterostructures, we have studied carrier tunneling via the Schottky barrier, spin injection and spin detection in ultra short channel silicon devices.

3.2. Experimental

Silicon nanowires were prepared on a silicon wafer by the vapor–liquid–solid method using gold clusters as the catalyst.[28] The silicon nanowires are typically single crystals with diameters ranging from 30 to 50 nm, length greater than 15 μm, and growth axes along [111] direction. To

better confine the solid state reaction, the silicon nanowires were oxidized to produce silicon/silicon oxide core/shell nanowires prior to device fabrication. The nanowire devices with manganese contacts (65 nm manganese/2 nm titanium /20 nm platinum) were fabricated on Si/Si$_3$N$_4$ substrate using e-beam lithography and e-beam evaporation (Fig. 3-1a). Platinum metal acts as a protection layer to prevent manganese from oxidation. Prior to metal deposition, the sample was etched in buffered hydrofluoric acid to remove oxide layer in the contact region. MnSi/Si/MnSi nanowire heterostructure was formed through solid state reaction between the silicon nanowire and two manganese contact pads. To allow manganese atoms to diffuse into the silicon nanowire to form partially (MnSi/Si/MnSi heterostructure) or fully silicidized MnSi nanowire, the device was annealed in vacuum at 650 ^{o}C for various durations of time.

3.3. Results & Discussion

3.3.1. Manganese silicide nanowire growth and analysis

After the annealing process, SEM images show that a clear contrast developed along the wire axis with two brighter sections emerging from both ends of the nanowire near the metal pads, corresponding to the formation of silicide structure (Fig. 3-1b). A darker section remain between the two brighter sections corresponds to the unreacted silicon nanowire.

To analyze the crystal structure of manganese silicide, the silicon nanowire devices were fabricated on the rigid silicon grids with a square opening covered with a window of a glassy Si$_3$N$_4$ film. The thickness of the Si$_3$N$_4$ film is about 50 nm and thus transparent to the electron beam. High resolution images were taken with FEI Titan 300 KV high-resolution transmission electron microscope. TEM studies show a single-crystal silicide nanowire (darker region) growing into the template structure of silicon/silicon oxide core/shell nanowire with a sharp

silicide/silicon interface (Fig. 3-1c). The silicide phase is identified as the MnSi single crystal by electron diffraction pattern (inset, Figure 3-1c). A high-resolution TEM image further shows lattice relation across the interface between MnSi and Si (Figure 3-1d). The zone axis of silicon is identified as [110] with several degrees tilted and that of MnSi is as $[0\bar{2}3]$. The epitaxial relations between MnSi and silicon are $Si[3\bar{1}\bar{1}]//MnSi[1\bar{2}0]$ and $Si(345)//MnSi(\bar{2}\bar{1}4)$. An inverse FFT image shows a coherent interface (Figure 3-1d and Figure 3-S1). Interestingly, the epitaxial relation observed here is different from the reported thin film system that usually have an epitaxial relation of $Si(111)//MnSi(111)$ and $Si[\bar{1}10]// MnSi[\bar{1}\bar{1}2]$ with ~3 % lattice mismatch. In our nanowire system, the interface of MnSi/Si has a lattice mismatch as big as ~24.5 %. Nonetheless, a coherent and atomically flat interface still forms instead of polycrystalline structure. Careful examination of the HRTEM image shows there is one misfit plane (Si semi-plane) every four $Si(3\bar{1}\bar{1})$ planar spacing to release the stress (Figure 3-S1) which keeps the interface coherent. The clean and sharp interfaces in nanowire heterostructures might be attributed to the increased tolerance of lattice strain at nano-scale. With this special epitaxial relation the MnSi/Si interface keeps coherent during the MnSi growth, which prevents the existence of a large amount of defects at the interface. Therefore, the formation of single crystal MnSi contact in MnSi/Si/MnSi nanowire heterostructures with coherent interface (MnSi/Si) may minimize spin scattering across the interface and uniquely enable effective spin injection and detection in nanoscale silicon devices.

3.3.2. Electrical characterization of MnSi nanowire

We have next examined the fundamental electrical transport and magnetic properties of single crystal MnSi nanowires. Four-probe measurement of fully-silicidized MnSi nanowires was carried out to eliminate the contact resistance (R_c) and to extract the resistivity value (Figure 3-2a inset). The low temperature measurement was carried out with Oxford cryogenic system ($\pm 8T$ and 1.6 K). Current-voltage (*I-V*) measurement shows that a fully-silicidized nanowire exhibits a perfect linear *I-V* behavior from 300 K to 1.6 K (Figure 3-2a), indicating metallic nature of the MnSi nanowires. The two-terminal linear *I-V* measurement of a 50 nm MnSi nanowire device gives a resistance of 3,517 Ω at 1.6 K (dark line in Figure 3-2a).To exclude the contact resistance, four-terminal measurement shows a resistance of 805 Ω at 1.6 K (red line in Figure 3-2a). The derived resistivity is about 81.4 $\mu\Omega$.cm, which is comparable to the values previously reported for bulk materials (25~100 $\mu\Omega$.cm).[25,26] In addition, it is expected that the itinerant ferromagnet, MnSi, will undergo a transition from paramagnetic to ferromagnetic state at its Currie temperature, $T_c \sim 29.6$ K, and there will be an abrupt resistance change near T_c due to the spin ordering. Indeed, temperature dependent measurement shows that a significant change in resistance in MnSi nanowires near 30 K (Figure 3-2b top). The differential resistance (*dR/dT)* was applied to locate the exact transition temperature (Figure 3-2b, bottom). The onset temperature of the device at which resistance begins to reduce is 29.7 K, corresponding to the magnetic phase transition temperature (T_c) of MnSi.

3.3.3. Magnetoresistance measurement (MR) of MnSi nanowire

Electrical transport measurements under the various magnetic fields show a clear resistance difference among 0, 1, and 5 Tesla below Currie temperature (Figure 3-3a). A lower resistance

can be observed at higher magnetic field, suggesting a negative magnetoresistance (MR) in the MnSi nanowire device. The negative MR can be attributed to the enhancement of spin ordering under magnetic field. This measurement further demonstrates that the resistance change near 30 K is indeed due to spin ordering at the low temperature.

The magnetotransport properties are further probed by sweeping the magnetic field (+5 T to -5 T) at various temperatures. The MR curves almost overlap for the temperature regime below 10K, with a maximum observed MR of approximately -1.8% at 5 Tesla at 1.6 K (Figure 3-3b). As the temperature increases to 30 K close to the Currie temperature (T_c) ~29.7 K, a smaller value of MR ~ -0.4% is observed (Figure 3-3b). If we sweep the magnetic field back and forth (from +3 T to -3 T and from -3 T to +3 T), a small hysteresis is observed at 1.6 K (Figure 3-3c), suggesting the ferromagnetic properties of the MnSi nanowires. The MR hysteresis may result from the remnant magnetization (Mr) of MnSi nanowires which displays the ferromagnetic properties of our MnSi nanowire. Our MnSi nanowire shows magnetic properties somewhat deviated from the reported results of the bulk system[29] and the large chemically synthesized single crystal MnSi wires[30] (diameter ~254 nm). In these bulk MnSi systems, the transition of helical ordering to conical ordering and to the induced ferromagnetic state is usually observed, and the ferromagnetic state only shows up at high external field ~0.6 T. However, in our MR studies of the MnSi nanowires these magnetic transition regions have not been observed. Instead, our small MnSi nanowire ~30-50 nm demonstrated only ferromagnetic properties. These ferromagnet-like behaviors in MnSi nanowires resemble the magnetic properties of epitaxial MnSi thin film with finite thickness. Recent studies have shown a small magnetic hysteresis (M-H) measured by SQUID in the epitaxial MnSi thin film of ~24 nm with coercive field (Hc ~180 Oe).[31] Theoretical simulations have also suggested that Mn atoms in MnSi materials at the

surface and interface with silicon possess larger spin polarization at the Fermi level and larger magnetic moments at surface and interface than Mn atoms in bulk MnSi.[32] These calculations predict a deviated behavior of MnSi nanowire or thin film from the bulk materials due to the reduced dimension and large surface/interface to volume ratio.

3.3.4. Band diagram of MnSi/p-Si/MnSi heterostructure and transport behavior

Theoretical studies have suggested that up to 45 % spin polarization can be achieved in MnSi ferromagnetic state,[27] suggesting that this material may function as an effective ferromagnetic contact for spin injection in nanoscale silicon devices. To explore the spin injection and detection in the silicon nanowires, we have fabricated a MnSi/p-Si/MnSi heterostructure device and investigated their spin transport properties. The equivalent circuit of a MnSi/p-Si/MnSi nanowire heterostructure comprises of two Schottky diodes (contact between MnSi/Si) connected back to back (Figure 3-4a). The work function difference suggests a large Schottky barrier ~0.45 eV between MnSi and p-type silicon (Figure 4a).[33] The device displays typical charge transport characteristics across a barrier and the transport behavior do not vary much throughout the experimental temperature range (Figure 3-4b).

To achieve the effective spin-polarized current injection via the Schottky barrier, the carriers need to be injected through the tunneling mechanism. The equivalent circuit of the MnSi/Si/MnSi heterostructure can be regarded as the back-to-back Schottky diodes in series. In MnSi/p-Si/MnSi heterostructure, holes are the majority charge carriers and can only see one Schottky barrier (MnSi/Si interface) near the positive biasing side.[34,35] A positive bias applied to one MnSi contact can cause hole injection through the MnSi/Si Schottky barrier in the reverse bias regime (Figure 3-4c). We note that the overall reverse bias current (I_{rev}) is extremely large

with little temperature dependency. The measurements of the I_{rev} as a function of temperature dependence at variable V_{bias}= +0.01 to +1 V show some interesting characteristics (Figure 3-4c). In the low bias regime (+0.01, 0.05, and 0.1 V), the I_{rev} decreases exponentially with the reducing temperature, suggesting a thermal emission process dominates the charge transport. When the biasing voltage is large enough (> 0.5 V), the I_{rev} shows little dependence on temperature, indicating that the thermal emission mechanism is no longer the dominant factor. Instead, the tunneling mechanism takes over in charge transport. When thermal emission formula is applied to fit the charge transport behavior in the heterostructure, an Arrhenius plot can be used to extract the effective Schottky barrier height of MnSi/p-silicon interface (Figure 3-4d). The effective Schottky barrier height in the low bias regime is ~0.103 eV for V_{bias} = +10 mV, ~0.049 eV for $V_{bias=}$ 0.05 V and only ~0.008 eV for V_{bias} = +0.1 V, respectively (Fig. 3-S2). The effective Schottky barrier height is significantly lower than the expected value in a thin film system. It may be attributed to the image charge force at the interface which reduces the Schottky barrier.[35] In addition, higher doping concentration (~10^{18-19} cm^{-3}) in silicon nanowire will make the barrier thinner which leads to higher carrier tunneling probability and hence reduces the temperature dependence of current at high bias.

3.3.5. Magnetoresistance and resistance change of MnSi/Si/MnSi heterostructure tunneling junction under magnetic field sweeping

The above studies demonstrate that a Schottky tunneling barrier exists across the MnSi/Si interface, and suggest that spin injection through tunneling mechanism may be achievable under higher biasing condition. We then studied spin injection and spin detection in ultra short channel silicon devices using the single crystal MnSi/p-Si/MnSi nanowire heterostructures, where the p-

Si region was scaled down to ~20 nm through the control of the solid state reaction. By measuring the device resistance as a function of magnetic field, the heterostructure device shows an overall positive MR in which resistance increases at high magnetic field at 1.6 K (Figure 3-5a). The positive MR represents the behavior of electron transport in the non-ferromagnetic materials, e.g., MnSi/Si interface and silicon, as reported in ferromagnetic contact/Si/ferromagnetic contact heterojunction device.[36] The measurement demonstrates that the transport behavior of this device is dominated by MnSi/Si/MnSi heterojunction (including MnSi/Si interface and silicon section), and the resistance change at various magnetic fields is attributed to the MnSi/Si/MnSi heterojunction rather than MnSi nanowire nanowire itself, which shows a negative MR.

Interestingly, when the bias is higher ~+1.0 V, a region with higher resistance is observed at low magnetic field (Figure 3-5a, black curve, highlighted by the arrow). As discussed previously (Figure 3-4), in this high bias regime, spin carriers can tunnel directly through the MnSi/Si Schottky barrier. The electrical field strength across the silicon region is ~5×10^5 V/cm with 1 volt bias if we assume uniform potential drop across the Si region is ~20 nm. Considering the non-uniform potential distribution, the field strength across the MnSi/Si Schottky barrier region is expected to be higher, and may readily reach ~10^6 V/cm for typical Fowler-Nordheim (F-N) tunneling.[37,38] Therefore, the transport mechanism of our device under the +1 V bias should be dominated by tunneling mechanism. The tunneling carriers usually have the same spin orientation with the injection electrode. Therefore, if the spin magnetization of source/drain contacts differs, a high resistance will be detected as seen in our measurement (Fig. 3-5a black curve). This behavior is similar to the giant magnetoresistance (GMR) effect reported in Ni/Si/Ni Schottky tunneling junction due to the spin carriers scattering.[39] Interestingly, in the low bias

regime ~0.1 V where there is a lack of effective tunneling for carriers, no such behavior is observed (Fig. 3-5a red curve), confirming that the resistance change shown up at the high bias regime can be tied to spin scattering in MnSi/Si/MnSi structure. In addition higher current density at the high bias regime can lead to more spin scattering and enhance signal of the spin scattering to the background ratio.

Figure 3-5b shows the resistance of such a MnSi/Si/MnSi device as a function of magnetic field at +1 V bias within ± 1.5 T. A resistance hysteretic behavior is clearly seen as the external magnetic field swept back and forth. The observed resistance hysteresis in the nanowire heterostructure is believed to be caused by the different coercive fields of source/ drain contacts. The different coercive field might be caused by the different length or diameter of MnSi nanowire source/drain (geometry effect) contacts. As the spin carriers are injected into silicon material, they will adopt the same spin orientation with the injection ferromagnetic contact. If the spin orientation of the injection and detection contact is the same, spin carriers will flow through the device without being scattered, leading to a lower resistance. Otherwise, if the spin carriers in the silicon encounter a different spin orientation at the detection ferromagnetic contact, they will be scattered at the detection contact, leading to an abrupt increase in resistance. Specifically in our device, temporary spin orientation deviated from parallel directions results in the higher resistance between ± 0.75 Tesla. The resistance hysteresis behavior can be detected up to 20 K. In addition, it is important to note that there are discontinuous resistance changes at -0.09 T and 0.27 T in the forward magnetic field sweeping direction and at 0.12 T and -0.26 T in the backward direction. It is related to stronger switching of spin magnetization of the two ferromagnetic contacts. If the magnetic field is larger than 0.27 T or smaller than -0.26 T, the resistance decreases immediately which may be attributed to the parallel spin magnetization of

the two contact at higher magnetic field. Notably, this switching magnetic field (+0.27/-0.26 T) is also consistent with the coercive field of full-silicidized nanowire ~0.18 T (Figure 3-5c). According to these studies, the hysteresis and spin scattering (GMR) signal clearly demonstrate electrical spin injection and detection in Si nanowire devices via a Schottky tunneling barrier with the ferromagnetic MnSi contact.

3.4. Conclusion

We have grown single crystal MnSi nanowires and MnSi/Si/MnSi nanowire heterojunction with atomically sharp interfaces. Electrical transport studies on MnSi nanowire shows an abrupt resistance reduction due to the spin ordering at ~29.7 K. A negative magnetoresistance (MR) ~1.8% under 5 Tesla at 1.6 K is achieved, demonstrating the ferromagnetic behavior of MnSi. Furthermore, using the MnSi/p-Si/MnSi heterostructure, we have studied the charge injection at various temperatures via the Schottky barrier, and the spin scattering was observed through magnetotransport studies of MnSi/p-Si/MnSi heterojunction. Our results represent the first report of magnetic contact fabrication through the formation of single crystal heterojunction nanowires and the first demonstration of spin injection and detection in such Si nanowire devices. The magnetic silicides approach thus opens a new pathway to create ferromagnetic/semiconductor junction with clean and sharp interface, and maysignificantly impact the future of spintronics.

3.5. Reference

1.   Zutic, I.; Fabian, J.; Das Sarma, S. *Rev Mod Phys* **2004**, *76*, 323-410.

2.   Dash, S. P.; Sharma, S.; Patel, R. S.; de Jong, M. P.; Jansen, R. *Nature* **2009**, *462*, 491-494.

3.   Schliemann, J.; Egues, J. C.; Loss, D. *Phys. Rev. Lett.* **2003**, *90*, 146801-1-146801-4.

4.   Dery, H.; Dalal, P.; Cywinski, L.; Sham, L. J. *Nature* **2007**, *447*, 573-576.

5.   Datta, S.; Das, B. *Appl. Phys. Lett.* **1990**, *56*, 665-667.

6.   Lou, X. H.; Adelmann, C.; Crooker, S. A.; Garlid, E. S.; Zhang, J.; Reddy, K. S. M.; Flexner, S. D.; Palmstrom, C. J.; Crowell, P. A. *Nat. Phys.* **2007**, *3*, 197-202.

7.   Ando, Y.; Hamaya, K.; Kasahara, K.; Kishi, Y.; Ueda, K.; Sawano, K.; Sadoh, T.; Miyao, M. *Appl. Phys. Lett.* **2009**, *94*, 182105-1-182105-3.

8.   Chappert, C.; Fert, A.; Van Dau, F. N. *Nat. Mater.* **2007**, *6*, 813-823.

9.   Rashba, E. I. *Phys Rev B* **2000**, *62*, R16267-R16270.

10.   Sugahara, S.; Tanaka, M. *J. Appl. Phys.* **2005**, *97*, 10D503-1-10D503-3.

11.   Sugahara, S.; Tanaka, M. *Appl. Phys. Lett.* **2004**, *84*, 2307-2309.

12.   Ohno, H.; Chiba, D.; Matsukura, F.; Omiya, T.; Abe, E.; Dietl, T.; Ohno, Y.; Ohtani, K. *Nature* **2000**, *408*, 944-946.

13.   Hall, K. C.; Lau, W. H.; Gundogdu, K.; Flatte, M. E.; Boggess, T. F. *Appl. Phys. Lett.* **2003**, *83*, 2937-2939.

14.   Dietl, T.; Ohno, H.; Matsukura, F.; Cibert, J.; Ferrand, D. *Science* **2000**, *287*, 1019-1022.

15.   Liu, C.; Yun, F.; Morkoc, H. *J Mater Sci-Mater El* **2005**, *16*, 555-597.

16.   Yang, Z.; Beyermann, W. P.; Katz, M. B.; Ezekoye, O. K.; Zuo, Z.; Pu, Y.; Shi, J.; Pan, X. Q.; Liu, J. L. *J. Appl. Phys.* **2009**, *105*, 053708-1- 053708-6.

17.   Liang, W. J.; Yuhas, B. D.; Yang, P. D. *Nano Lett.* **2009**, *9*, 892-896.

18.   Hangarter, C. M.; Myung, N. V. *Chem. Mater.* **2005,** *17,* 1320-1324.

19.   Xiu, F.; Wang, Y.; Kim, J.; Hong, A.; Tang, J.; Jacob, A. P.; Zou, J.; Wang, K. L. *Nature Materials* **2010**, *9*, 337-344.

20.   Appelbaum, I.; Huang, B. Q.; Monsma, D. J. *Nature* **2007**, *447*, 295-298.

21.   Min, B. C.; Motohashi, K.; Lodder, C.; Jansen, R. *Nat. Mater.* **2006**, *5*, 817-822.

22.   Lin, Y. C.; Lu, K. C.; Wu, W. W.; Bai, J. W.; Chen, L. J.; Tu, K. N.; Huang, Y. *Nano Lett.* **2008**, *8*, 913-918.

23.   Chou, Y. C.; Wu, W. W.; Chen, L. J.; Tu, K. N. *Nano Lett.* **2009**, *9*, 2337-2342.

24.   Burchhart, T.; Lugstein, A.; Hyun, Y. J.; Hochleitner, G.; Bertagnolli, E. *Nano Lett.* **2009**, *9*, 3739-3742.

25.   Manyala, N.; Sidis, Y.; DiTusa, J. F.; Aeppli, G.; Young, D. P.; Fisk, Z. *Nature* **2000**, *404*, 581-584.

26.   Pfleiderer, C.; Julian, S. R.; Lonzarich, G. G. *Nature* **2001**, *414*, 427-430.

27.   Wu, H.; Hortamani, M.; Kratzer, P.; Scheffler, M. *Phys. Rev. Lett.* **2004**, *92*, 237202-1-237202-4.

28.   Hannon, J. B.; Kodambaka, S.; Ross, F. M.; Tromp, R. M. *Nature* **2006**, *440*, 69-71.

29.   Ishikawa, Y.; Arai, M. *J. Phys. Soc. Jpn.* **1984**, *53*, 2726-2733.

30.   Higgins, J. M.; Ding, R.; Degrave, J. P.; Jin, S. *Nano Lett.* **2010**, ASAP, DOI: 10.1021/nl904042m.

31. Eagnano, E.; Bondino, F.; Cepek, C.; Parmigiani, F.; Mozzati, C. Appl. Phys Lett **2010**, *96*.32.

32. Hortamani, M.; Sandratskii, L.; Kratzer, P.; Mertig, I.; Scheffler, M. *Phys Rev B* **2008**, *78*, 104402.

33. Eizenberg, M.; Tu, K. N. *J. Appl. Phys.* **1982**, *53*, 6885-6890.

34. Nam, C. Y.; Tham, D.; Fischer, J. E. *Nano Lett.* **2005**, *5*, 2029-2033.

35. Sze, S. M. *Physics of Semiconductor Devices*; Wiley: New York, 1981.

36. de Araujo, C. I. L.; Munford, M. L.; Delatorre, R. G.; da Silva, R. C.; Zoldan, V. C.; Pasa, A. A.; Garcia, N. *Appl. Phys. Lett.* **2008**, *92*, 222101-1- 222101-3.

37. R.H. Fowler and L. Nordheim, *Proc. Roy. Soc.***1928**, *119* , 173 (London) Ser. A.

38. Davids, P. S.; Kogan, S. M.; Parker, I. D.; Smith, D. L. *Appl. Phys. Lett.* **1996**, *69*, 2270-2272.

39. Jia, Y. Q.; Shi, R. C.; Chou, S. Y. *IEEE Trans. Magn.* **1996**, *32*, 4707-4709.

3.6. Supporting Information

Figure 3-S1 shows a high-resolution TEM image of MnSi/Si interface. The lattice mismatch between $Si(3\bar{1}\bar{1})$ and $MnSi(1\bar{2}0)$ is about 24.5%. An extra Si semi-plane can be observed every four planes, which is believed to release stress built-up in the crystal, leading to a coherent interface between MnSi and Si.
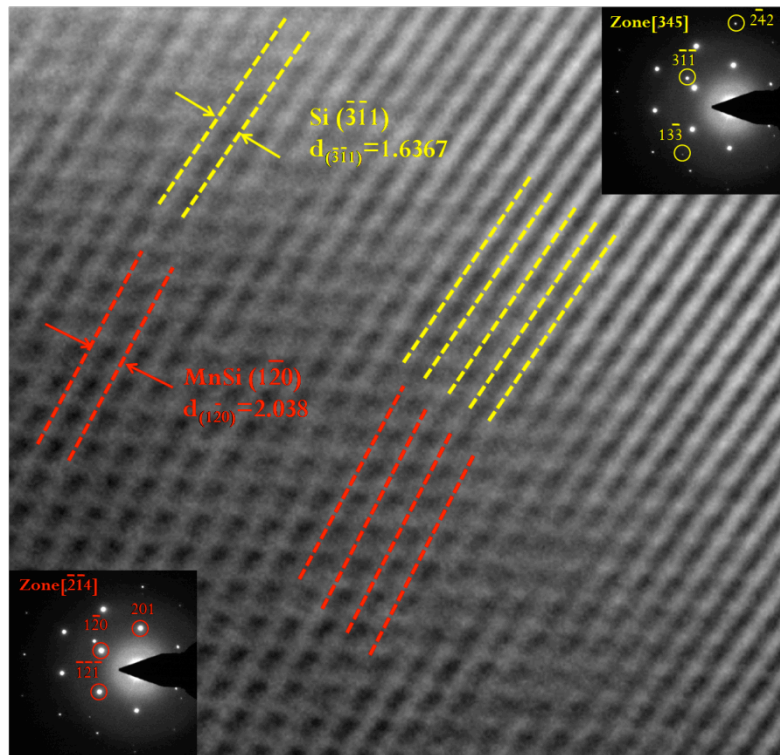

Figure 3-S1. High-resolution TEM image of MnSi/ Si interface. Insets are the diffraction patterns of $MnSi[\bar{2}\bar{1}4]$ and $Si[345]$ zone axis. Measured lattice mismatch at interface is ~24.5 % which is consistent with one-planar spacing between $MnSi(1\bar{2}0)$ and $Si(3\bar{1}\bar{1})$. There is an extra Si semi-plane every four planes.
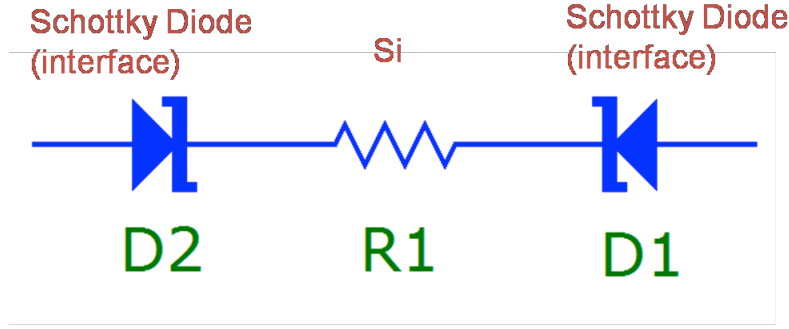
Figure 3-S2. The equivalent circuit of MnSi/Si/MnSi heterostructure. The heterostructure can be treated as two Schottky diodes (interface) connected back to back and in series with a resistance (silicon region). To determine the Schottky barrier height (SBH) of the MnSi/Si interface, a model of two back-to-back Schottky contacts have been proposed to address the nonlinear *I-V-T* curves of semiconductor nanowire junction. Regarding thermionic emission behavior, the *I-V-T* relation of a reverse-biased Schottky diode can be described by the following equation:

$$I = AA^{**}T^2 \exp\left(-\frac{q\varphi_B}{k_B T}\right)$$

where *A* is the contact area, *A*** is the effective Richardson constant, and φ_B the effective Schottky barrier height. φ_B can be obtained from the slope of Figure 3-4d which is an Arrhenius plot of $\ln(I/T^2)$ versus $1/T$ in the low bias regime. Slope of Arrhenius plot is equal to $-q\varphi_B/k_B$. Therefore, the effective Schottky barrier height φ_B can be extracted. This holds only for high temperatures at which *A*** and φ_B are temperature independent.[s-1, s-2]

Reference:

s-1.   Nam, C. Y.; Tham, D.; Fischer, J. E. *Nano Lett.* **2005,** *5*, 2029-2033.

s-2.   Sze, S. M. *Physics of Semiconductor Devices*; Wiley: New York, 1981.

3.7. List of Figures
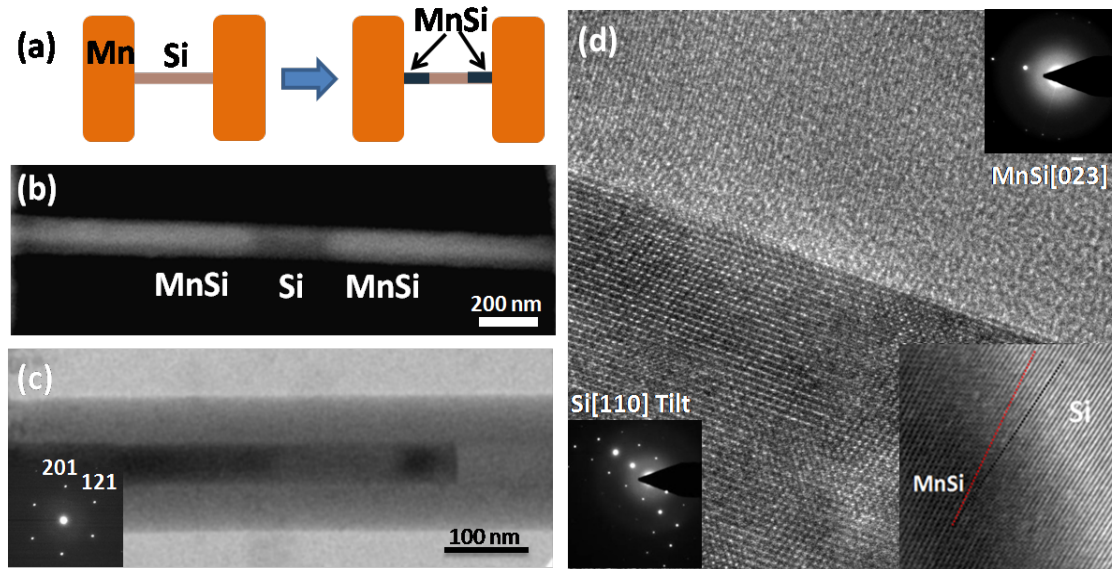
Figure 3-1. Manganese silicide nanowire growth and analysis (a) A schematic of MnSi formation through the solid state reaction between a silicon nanowire and its Mn contact pads. (b) SEM image of MnSi grows into Si/SiO$_2$ nanowire template. (c) TEM image of MnSi nanowire and MnSi/Si interface. The inset is selective area diffraction pattern (SADP) which is identified with MnSi[$\bar{2}\bar{1}4$] zone axis. (d) High resolution TEM images. It shows the sharp interface of MnSi/Si. The inset diffraction patterns show the MnSi[$0\bar{2}3$] zone axis and Si[110] zone axis ,and the Si[110] zone axis is several degrees tilted. The lower right inset image is an inverse FFT image of MnSi/Si interface. It shows an epitaxial interface corresponding to MnSi [$\bar{2}\bar{1}4$] and Si[345] zone axis.
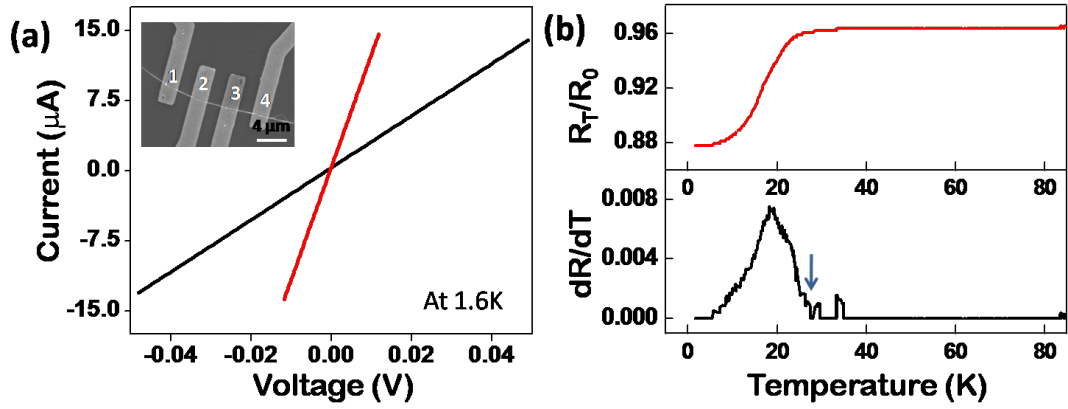
Figure 3-2. Electrical characterization of MnSi nanowire. (a) Red line represents the four-terminal measurement and dark line represents two-terminal measurement (which is between 2 and 3). The measurement is performed at 1.6 K. The resistivity is ~81.4 $\mu\Omega$.cm. (b) Resistance change versus temperature of 700-nm length MnSi nanowire. There is an abrupt resistance change which occurs around 29.7 K. The red curve (top) displays temperature dependence measurement (R_T/R_0 versus temperature). R_0 represents nanowire resistance at 200 K. The dark curve (bottom) displays a differential resistance (dR/dT). The arrow indicates the on onset temperature of abrupt resistance change.
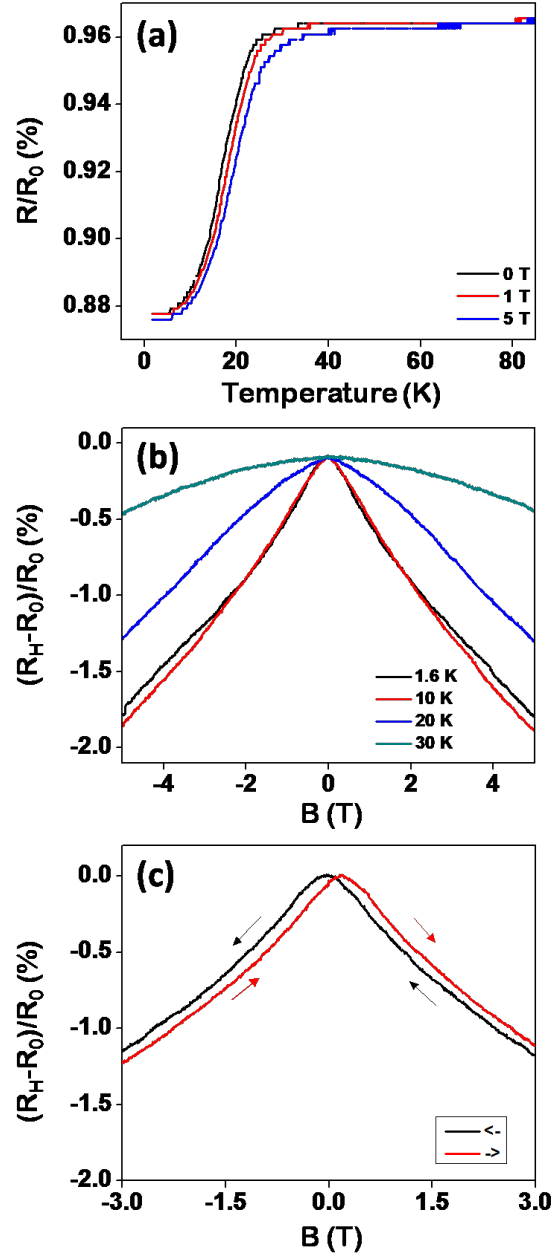
Figure 3-3. Magnetoresistance measurement (MR) of MnSi nanowire. (a) Resistance changes versus temperature at various magnetic fields (0, 1, 5 Tesla). (b) Magnetoresistance of MnSi nanowire at different temperatures. R_H is the resistance of the nanowire at the certain magnetic field. R_0 represents the nanowire resistance at the zero field. (c) Magnetoresistance hysteresis of MnSi nanowire at 1.6 K. The arrows indicated the sweeping direction of magnetic field.
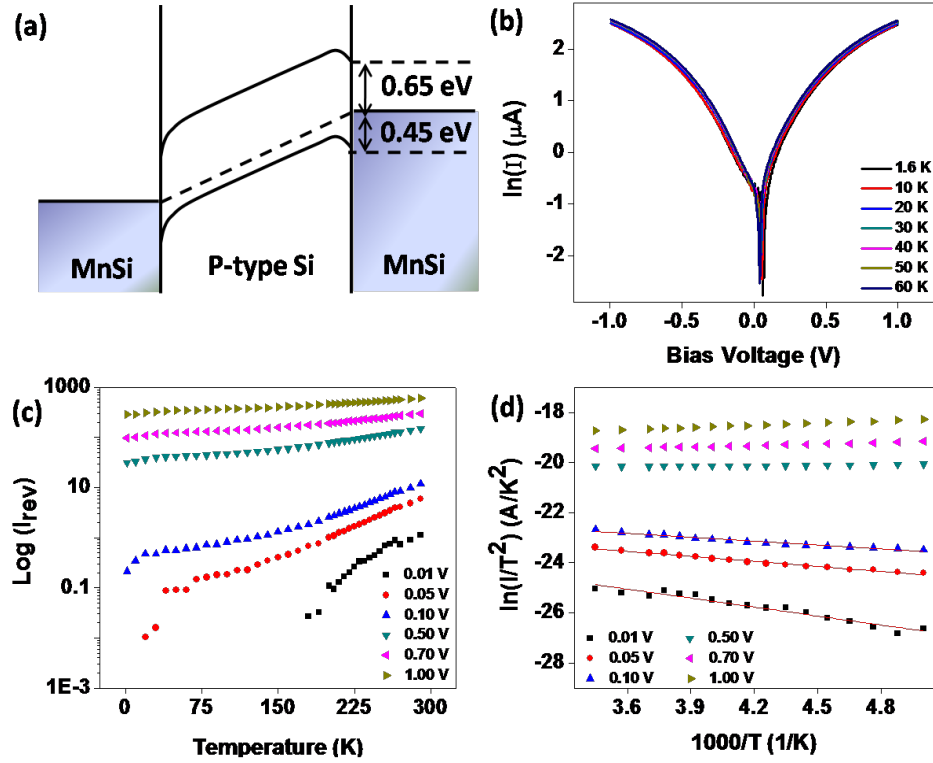
Figure 3-4. (a) Band diagram of MnSi/p-Si/MnSi heterostructure. The positive bias is applied at the left end of MnSi. A Schottky barrier ~0.45 eV is predicted for hole injection into p-Si. (b) *I-V* characteristics of heterostructure at various temperatures. (c) Current versus temperature dependence at different reverse biasing voltages. (d) Arrhenius plot for heterostructure at various biasing voltages between 200 K and 290 K.
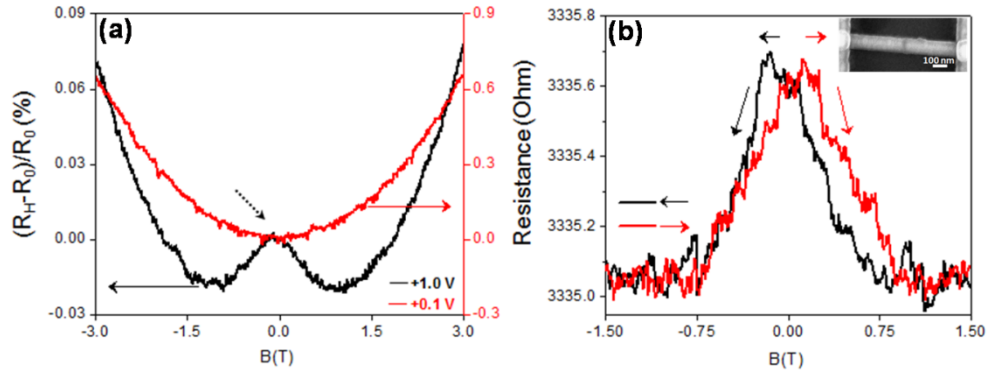
Figure 3-5. Magnetoresistance and resistance change of MnSi/Si/MnSi heterostructure tunneling junction under magnetic field sweeping. (a) Magnetoresistance of heterostructure versus magnetic field. The red curve shows positive magnetoresistance (MR) under +0.1 V biasing voltage across the heterostructure. The black curve shows also a positive MR at high field and a negative MR at the low field under +1.0 biasing voltage. The dash arrow indicates the region of negative MR. R_H is the resistance of the heterostructure device at the certain magnetic field. R_0 represents the device resistance at the zero field. The arrows indicate the individual scale axis. (b) Resistance change of heterostructure as a function of magnetic field. The inset shows an SEM image of the MnSi/p-Si/MnSi heterojunction device. The length of silicon region is ~20 nm and the diameter of silicon nanowire is ~ 50 nm. The doping concentration of p-type nanowire is ~10^{18-19} cm^{-3}. The resistance measurement is performed at +1 V bias voltage. Magnetic field is swept from +1.5 T to -1.5 T and then in the backward direction.

Chapter 4: The Growth of Nickel Silicides in Si and Si/SiOx Core/Shell Nanowires

4.1. Introduction

Silicon nanowires (Si NWs) have attracted much interest for a variety of applications including integrated electronics,[1-3] chemical and biological sensors[4] and energy applications.[5, 6] Forming reliable contacts to these devices is one of the most important issues in achieving optimal device performance.[7,8] To this end, various metal silicides have been utilized as they offer low contact resistance and few interfacial defects with Si. To identify and control the phase formation of suitable silicide materials in nanoscale is of high importance to Si NW devices. In some silicide systems, e.g. $TiSi_2$ and $CoSi_2$, high temperature activation is necessary for the nucleation to happen, which limits the processing window of following steps.[9-12] In addition, high-resistive silicide phases usually forms in small dimensions for these silicides.[12-14] Nickel silicides are used in current semiconductor industry as they can form low resistive phase at lower processing temperature and in small dimensions. For example, the low resistive nickel monosilide (NiSi) is used as the contact materials for Si based devices.[14-15] Other nickel silicide phases, e.g. $Ni_{31}Si_{12}$, Ni_2Si and Ni_3Si, have also been used as the gate metals to tune the work function of nanoscale devices.[16,17] Therefore, the nickel silicides are promising to be exploited for silicon nanowires device applications. There have been considerable efforts in studying the formation and properties of nickel silicides in nanoscale since Wu *et al.* first demonstrated the formation of single-crystal NiSi metallic nanowire and NiSi/Si/NiSi nanowire heterostructure devices by solid state reaction.[7] Lu *et al.* found that NiSi formed under annealing conditions in the range of 500-650 ^{o}C by silicidizing Si [111] nanowire with nickel metal diffusing across the thin oxide barrier.[18] Weber *et al.* reported the formation of single-crystalline $NiSi_2$ by silicidizing Si[110] nanowire at 480 °C.[19] Dellas *et al.* studied the nickel silicide formation dependence on Si NW orientations (Si [112] vs. Si[111] nanowires) and suggested

that interfacial energy reduction plays a significant role in silicide phase transformation in silicon NWs.[20] These work shared valuable information on nickel silicide formation at nanoscale, although there is still a lack of systematic studies on the formation of different silicide phases at different conditions, or geometries. Importantly, it has also been suggested that the silicide phase transformation temperature may vary under the influence of stress in the finite dimensions.[21-23] This phenomenon will become increasing important at nanoscale where the interfacial energy and stress pile-up may play an important role to induce the formation of different phases. Herein, we report the systematic studies on the phase formation of nickel silicides in Si NWs and Si/SiOx core/shell NWs to explore the phase formation sequences and the stress influence on silicides formation in one-dimensional nanostructures. We expect these studies will contribute to the better understanding of the growth mechanism for various nickel silicides at finite scales for Si NW device engineering.

4.2. Experimental

In our experiment, silicon nanowires are synthesized on a silicon wafer by the vapor–liquid–solid method using gold clusters as the catalyst. The silicon nanowires are typically single crystals with growth axes along [111] direction. The oxide shell is grown by oxidizing the silicon nanowire at $900^{o}C$ in ambient for various durations of time to control the shell thickness. Bare silicon nanowires (~50-70 nm in diameter) with 1~2 nm native oxide and silicon/silicon oxide core/shell nanowires (~50-70 nm silicon core) with 5~50 nm oxide shell are used in our experiment to react with nickel metal. Different oxide shell thickness is chosen to explore the oxide confinement effect on the silicide growth. The growth of silicides is directly observed in transmission electron microscope (TEM). Nanowires ([111] growth direction) with nickel pads are fabricated on glassy silicon nitride membrane with ~50 nm thickness which allows electron beam to penetrate. 3 μm wide, 70 nm thick Nickel pads are patterned on nanowires with ebeam lithography, followed by ebeam evaporation of Ni that covers the nanowires. Before the evaporation, BHF (Buffered Hydrofluoric Acid) dip is performed to remove the native oxide or oxide shell on Si nanowires to allow direct contact between nickel and the silicon core. The samples

are then annealed at 550 $^{\circ}$C with the ramping rate of 10 $^{\circ}$C/s in JEOL CX100 TEM equipped with GATAN heating stage at vacuum of 10^{-6} torr, and the nickel silicide formation is observed in situ. The reactions are stopped at specific times and structure characterizations are performed with FEI 300 KV high resolution TEM.

4.3. Results & Discussion

4.3.1. TEM study of nickel silicide growth

In our studies, both bare Si NWs (diameter ~ 50-70 nm) and Si/SiOx core/shell NWs (core diameter~ 50-70 nm) are contacted with nickel metal pads,[8] which are then annealed at 550 $^{\circ}$C for different durations to study the phase formation sequences. All annealing processes were carried out and observed using in situ TEM and were stopped at different times. In all samples, it was observed that the nickel silicides grow from the Ni pad and continuously into the NW laterally. The initial phases of the silicides are identified from samples annealed at 550 $^{\circ}$C for 60 seconds. TEM images of the nickel silicides formed in a bare SiNW and a SiOx/Si NW are shown in Figure 1a and b, respectively. At this stage, the silicide region can be clearly divided into two sections: one section close to the Ni pad with expanded volume and the other of similar volume to the original Si NW core close to the Si/silicide interface. At the interface, the silicide phase is identified as NiSi$_2$ for both bare and core/shell Si NWs. High resolution TEM (HRTEM) studies and Fourier Transforms (FTs) identify the epitaxial relations to be $NiSi_2[1\bar{1}0]//Si[1\bar{1}0]$ and $NiSi_2(111)//Si(111)$ (Figure 4-1c-d). And this epitaxial relation maintains throughout the silidice growth stage as long as there is a Si/silicde interface. In our experiments carried out between 400 $^{\circ}$C and 700 $^{\circ}$C, NiSi$_2$ always forms at the interface. This observation is different from what has been reported in the thin film system, where NiSi$_2$ usually forms at ~700 $^{\circ}$C while between 400 and 700 $^{\circ}$C NiSi phase is usually observed .[24,26]

First principle calculation gives the formation energies of NiSi and NiSi$_2$ from silicon and nickel to be ~ -0.488 eV/molecule and -0.314 eV/molecule, respectively. NiSi has the lower formation energy

and should be energetically more favorable. However, the interplanar spacing at the $NiSi_2(111)/Si(111)$ and $NiSi(131)/Si(111)$ interfaces are ~0.9% and ~5.62%, respectively. Here, the smaller interfacial lattice mismatch between $NiSi_2$ and Si may lead to lower interfacial energy. We suggest that the interfacial energy is the dominating factor that determines the first nucleated silicide phase in this one dimensional nanosystem. Therefore in our experiments, the lower interfacial energy leads to the formation of the high temperature phase $NiSi_2$ at lower temperatures.

4.3.2. Silicide growth in various duration of annealing time

To explore the growth mechanism and phase formation sequence, snap shots of nickel silicides at different growth stages are taken for the case of bare Si NWs with 1-2 nm native oxide (Figure 4-2) and for the Si/SiOx core/shell NWs (Figure 4-3), respectively. In bare SiNWs (Figure 4-2) two different morphologies of nickel silicides are observed after annealing at 550 ^{o}C in vacuum. About 5 seconds into annealing at 550 ^{o}C, the initial as-grown silicide near the metal pad is identified as $NiSi_2$, which keeps epitaxial growth into the Si NWs (Fig. 4-2a, Fig. 4-S1). When the annealing time increases from 5 seconds to 60 seconds, 2 minutes and 8 minutes (Figures 4-2b, c, d respectively), nickel silicide with larger volume compared to the original Si NW is clearly observed. The phase with larger volume close to the nickel pad in Fig. 4-2b-d is identified as $Ni_{31}Si_{12}$ by selected electron diffraction (SAD) patterns shown in Fig. 4-2e-f. The silicide phase formed under the Ni pad is also identified as $Ni_{31}Si_{12}$ (see Supporting Information, Fig. 4-S2). The interface phase (Si/Silicide) grows as $NiSi_2$ which maintains epitaxial relation with Si (Figure 4-2g). These observations suggest that in this one dimensional silicide growth system, $NiSi_2$ forms as the initial phase and continues to grow into Si nanowires while maintaining the epitaxial relationship at the silicide/Si interface throughout the growth period. As the annealing time increases, $NiSi_2$ region close to the Ni source will transform into the metal rich $Ni_{31}Si_{12}$ with the continued supply of nickel atoms. These two phases are usually observed in the initial growth stage and thus are kinetically favorable phases at 550 ^{o}C in our growth system. With further annealing beyond 5 minutes, another metal-rich phase, Ni_2Si starts to appear in between $Ni_{31}Si_{12}$ and $NiSi_2$ (Fig 4-

2h). As Ni_2Si phase are not observed at the initial growth stage (Fig. 4-2 and Fig. 4-3), we suggest that Ni_2Si forms only at the later stage of the annealing process by transforming the $NiSi_2$ phase with the abundant Ni atom supply from the Ni pads.

4.3.3. Snap-shot TEM images of nickel silicide growth in the Si/SiOx core/shell NW for various annealing durations

Silicide formation sequence is also observed in Si/SiOx core/shell NWs with ~40-50 nm shell (Figure 4-3a-d). Before Ni deposition BHF dip is usually performed to remove the oxide shell, which leaves an undercut of the oxide shell in the NW region next to the Ni pad. The undercut region essentially behaves as a bare SiNW. Annealing this structure we can observe how the silicides transform in the bare region and how the transformation process is altered when the silicides grow into the core/shell structure. In the bare region (without the oxide shell) of the nanowire, the $NiSi_2$ grows initially similar to that observed in bare nanowires (Fig. 4-3a). As the growth time increases, the second phase, $Ni_{31}Si_{12}$ begins to grow from the Ni pad region as shown in Fig. 4-3b. When it reaches the NW region with the oxide shell, the growth is hindered. As shown in Figure 4-3d, after 8 minutes' annealing at 550 ^{o}C, $Ni_{31}Si_{12}$ grows as long as ~790 nm with ~380 nm into the oxide shell region. In stark contrast, in bare SiNW $Ni_{31}Si_{12}$ usually grows for microns in length after 8 minutes' annealing as shown in Figure 4-2d.

4.3.4. Nickel silicide growth in Si/SiOx core/shell NWs with various oxide shell thickness

The observations are consistent over various samples. To examine the effect of the oxide shell on silicide formation, we have compared the growth length of the $NiSi_2$ and $Ni_{31}Si_{12}$ phase in the bare and core/shell NWs over different bathes of samples, after 4 minutes' annealing at 550 ^{o}C. The condition is chosen so that the only silicide phases existing in the NWs are $Ni_{31}Si_{12}$ and $NiSi_2$, and that when there is always a silicide/Si interface (or, the Si NW has not been completely consumed). After 4 minutes annealing, for both structures, the metal-rich phase, $Ni_{31}Si_{12}$ forms near the Ni pad area and

NiSi$_2$ forms near the silicide/Si interface. The length of Ni$_{31}$Si$_{12}$ is measured from end the Ni pad to the two silicide interface where a clear volume difference is observed. The length of NiSi$_2$ is measured from the silicide/silicide interface to the silicide/silicon interface where a clear contrast is observed. Total of 28 data points were taken for both cases. In bare SiNW, the average length for NiSi$_2$ and Ni$_{31}$Si$_{12}$ is ~2610 nm and ~761 nm, respectively. And in the core/shell Si/SiOx NWs, the average length of silicide for NiSi$_2$ and Ni$_{31}$Si$_{12}$ is ~1652 nm and ~582 nm, respectively. We note that the average oxide undercut length in the core/shell NWs is ~418 nm, which translates to an adjusted Ni$_{31}$Si$_{12}$ length that grows into the core/shell NW to be around 164 nm, significantly shorter than those observed in the bare Si NWs. It is apparent that the growth rate for both silicides, NiSi$_2$ and Ni$_{31}$Si$_{12}$, is slower in Si/SiOx core/shell NWs, and the difference is more pronounced in the case of Ni$_{31}$Si$_{12}$. As often observed, the growth of Ni$_{31}$Si$_{12}$ usually does not go far beyond the oxide undercut region. Instead, Ni$_{31}$Si$_{12}$ stops growing into the core/shell NW structure after a fairly short penetration length as shown in Figure 4-3d. It appears that the existence of the oxide shell will limit the volume expansion accompanied with the formation of Ni$_{31}$Si$_{12}$ phase, and hence deter its growth in the core/shell structure.

In addition, a compressive stress has been reported to exist in the core/shell Si/SiOx NW structure,[27,28] which can slow down the diffusion rate of the atoms and hence lead to the observed retarded growth rate for silicides in core/shell Si/SiOx NWs.[29,30] In a stressed structure, if we consider the diffusivity (D) of atoms in a material with cubic crystallography as described by equation (1).

$$D = \frac{1}{6}a^2 \nu f \ \exp(\frac{-G^*}{k_B T}) \qquad\qquad (1)$$

$$(G^* = G^f + G^m)$$

where a is the jumping distance, n is an effective vibrational frequency, G^* is the Gibbs free energy of activation, G^f is the Gibbs free energy of formation of the mobile species, G^m is the Gibbs free energy of migration of the mobile species, and jumping events away from a true random-walk are accounted for

by the correlation factor f. We can transform the equation (1) to equation (2), which can be used to describe the relation between the compressive stress (p) and the diffusivity.

$$V^* = \frac{\partial G^*}{\partial p} = -k_B T \frac{\partial \ln(D)}{\partial p} \qquad (2)$$

where V* is the activation volume, which represents the volume change when the one diffusion atom migrates in the crystal structure. In this diffusion system, V* represents the change of volume as the nickel atom diffuses into the silicon lattice. It has been proved that nickel atoms diffuse in the silicon lattice through the interstial sites, which will enlarge the silicon crystal lattice and hence leads to a positive V*. And Δp can be viewed as the change in pressure due to the external force or residual stress in the material. Therefore, if we apply higher compressive stress on the silicon materials, the diffusion rate of nickel atoms will be retarded (smaller diffusivity). In the NWs with oxide shells a residual compressive stress exists in the Si core, which results in the slower diffusion rate of nickel atoms than that observed in the bare NWs. This explains why nickel silicides grow slower in the Si/SiOx core/shell NWs, and hence the observed slower growth rate for both $NiSi_2$ and $Ni_{31}Si_{12}$ in the core/shell Si NWs. On top of that, slower Ni diffusion rate will also contribute to the unfavorable formation of the metal-rich silicide phases in the core/shell NWs, as they need more nickel atoms to form, consistent with our observations that the formation of $Ni_{31}Si_{12}$ is further deterred in the core/shell Si/SiOx NW structure.

Various thicknesses of the oxide shells are exploited to examine their effect on the phase transformation of metal-rich silicides. It was found that extrusion structures will appear with prolonged annealing in bare Si NWs and core/shell NWs with thin or moderate oxide thickness, which may be the result of the large volume expansion and stress pile-up found in the $Ni_{31}Si_{12}$ and Ni_2Si regions as shown in Figure 4-4a,b. The extrusion normally adopt the same crystal structure (silicide phase) with its surrounding phase (Fig. 4-S3). Figure 4a shows a NW with oxide shell thickness ~5-15 nm after 8

minutes annealing at 550°C. The three phases, $Ni_{31}Si_{12}$ close to pad region (Fig. 4-4), Ni_2Si away from pad (Fig. 4-4) are found with extrusion structures and also $NiSi_2$ around the silicide/Si interface is found with epitaxial relation. The atomic volume of Si is 20.01 Å^3 per Si atom, and those of $Ni_{31}Si_{12}$ and Ni_2Si are 39.46 Å^3 and 32.15 Å^3, respectively. Therefore upon transformation to the metal-rich silicides, the volume of the Si NW will expand several times, which lead to significant stress pile-up in the confined NW core. The extrusion structures are then formed in these phase region to release local stress by expanding out of the thin oxide shell (~5-15 nm). As the oxide shell becomes slightly thicker, ~25 nm, under the same annealing condition the same three phases including the metal-rich phases, $Ni_{31}Si_{12}$ and Ni_2Si, and $NiSi_2$ near the Si/Silicide interface form and the total length of the silicided length is comparable, but $Ni_{31}Si_{12}$ and Ni_2Si grow at a lower speed (Figure 4-4b). Small extrusion structures (highlighted by arrows) are also present but much less obvious and appear with fewer frequency.

When silicide grows within the Si/SiOx core/shell NW with really thick oxide shell ~50 nm under the same conditions, no extrusion structures are found (Figure 4-4c). In addition, in most core/shell NWs with thick shells (~50nm) no Ni_2Si is observed even after 8 minutes of annealing and only small portion of $Ni_{31}Si_{12}$ can grow into Si/SiOx core/shell NW. We believe that the strong confinement of the thick oxide shell seriously retards the diffusion rate of nickel atoms to an extent that it completely annihilates the formation of Ni_2Si.

4.4. Conclusion

Three nickel phases, $Ni_{31}Si_{12}$, Ni_2Si and $NiSi_2$ are observed in one step annealing at 550 $^{\circ}$C. $NiSi_2$ grows initially through the Si NW and then the area close to nickel pad transforms into the nickel-rich phase, $Ni_{31}Si_{12}$. With prolonged annealing over 5 minutes, the Ni_2Si starts to show up in between $Ni_{31}Si_{12}$ and $NiSi_2$. The growth sequence is different from the thin film system where Ni_2Si usually appears as the initial phase in the beginning as the annealing temperature is higher than 400 $^{\circ}$C. Interfacial energy differences and surface free energy are believed to play an important role here at the nanoscale, which lead to the formation of normally unfavorable silicide phases in Si NWs. In addition, Si/SiOx core/shell

NW structure is used to explore the phase transformation of silicides in the structure-confined nano environment. Nickel silicides in the structure-confined core/shell Si NW shares the similar phase formation sequences as those appeared in the bared SiNWs, while the growth rate is significantly retarded. This may be attributed to the high compressive stress built-in in the core/shell NW structure that retards the diffusion of the nickel atom as well as limits the volume expansion of the metal-rich phases. As a result, the high stress at this finite scale hinders the continuous growth of $Ni_{31}Si_{12}$ into the core/shell NWs and totally eliminates the formation of Ni_2Si in core/shell NWs with thick oxide shells (~ 50 nm). Through these studies, we have demonstrated first time the phase formation sequences of nickel silicides in Si and Si/SiOx NW structures, which is of great importance for reliable contact engineering for Si NW devices. Furthermore, we have provided a clear picture of the hindered nickel silicide growth in confined nanoscale environment and showed the deviated behavior of silicides growth under stress. The information rendered here will be useful for Si NW device applications as well as for the silicon device engineering at nanoscale in general.

4.5. Reference

1. Duan, X.; Niu, C.; Sahi, V.; Chen, J.; Parce, J. W.; Empedocles, S.; Goldman, J. *Nature* **2003**, *425*, 274.

2. Javey, A.; Nam, S.; Friedman, R. S.; Yan, H.; Lieber, C. M. *Nano Letters* **2007**, *7*, 773.

3. Heath, J. R. *Accounts Chem Res* **2008,** *41*, 1609-1617.

4. Patolsky, F.; Zheng, G. F.; Hayden, O. H.; Lakadamyali, M.; Zhuang, X. W.; Lieber, C. M. *Proc. Natl. Acad. Sci. U. S. A.* **2004**, *101*, 14017.

5. Hochbaum, A. I.; Chen, R. K.; Delgado, R. D.; Liang, W. J.; Garnett, E. C.; Najarian, M.; Majumdar, A.; Yang, P. D. *Nature* **2008,** *451*, 163-U5.

6. Chan, C. K.; Peng, H.; Liu, G.; McIlwrath, K.; Zhang, X. F.; Huggins, R. A.; Cui, Y. *Nature Nanotech.* **2008***, 3*, 31-35.

7. Wu, Y.; Xiang, J.; Yang, C.; Lu, W.; Lieber, C. M. *Nature* **2004**, *430,* 61.

8. Lin, Y. C.; Lu, K. C.; Wu, W. W.; Bai, J. W.; Chen, L. J.; Tu, K. N.; Huang, Y. *Nano Lett.* **2008**, *8*, 913.

9. Tu, K. N.; Thompson, R. D.; Tsaur, B. Y. *Appl. Phys. Lett.* **1981**, *38*, 626.

10. Jeon, H.; Sukow, C. A.; Honeycutt, J. W.; Rozgonyi, G. A.; Nemanich, R. J. *J. Appl. Phys.* **1992**, *71*, 4269.

11. Maex, K. *Mater. Sci. Eng. R-Rep.* **1993,** *11*, 53-153.

12. Lasky, J. B.; Nakos, J. S.; Cain, O. J.; Geiss, P. J. *IEEE Trans. Electron Devices* **1991,** *38*, 262-269.

13. Vonkanel, H. *Materials Science Reports* **1992**, *8*, 193.

14. Iwai, H.; Ohguro, T.; Ohmi, S. *Microelectron. Eng.* **2002**, *60*, 157.

15. Chen, J.; Colinge, J. P.; Flandre, D.; Gillon, R.; Raskin, J. P.; Vanhoenacher, D. *J. Electrochem. Soc.* **1997**, *144*, 2437.

16. Kittl, J. A.; Pawlak, M. A.; Lauwers, A.; Demeurisse, C.; Opsomer, K.; Anil, K. G.; Vrancken, C. van Dal, M. J. H.; Veloso, A.; Kubicek, S.; Absil, P.; Maex, K.; Biesemans, S. *IEEE Electron Device Lett.* **2006**, *27*, 34.

17. Tan, S. Y. *J. Electron. Mater.* **2009,** *38*, 2314-2322.

18. Lu, K. C.; Wu, W. W.; Wu, H. W.; Tanner, C. M.; Chang, J. P.; Chen, L. J.; Tu, K. N. *Nano Lett.* **2007**, *7*, 2389.

19. Weber, W. M.; Geelhaar, L.; Graham, A. P.; Unger, E.; Duesberg, G. S.; Liebau, M.; Pamler, W.; Cheze, C.; Riechert, H.; Lugli, P.; Kreupl, F. *Nano Lett.* **2006**, *6*, 2660.

20. Dellas, N. S.; Liu, B. Z.; Eichfeld, S. M.; Eichfeld, C. M.; Mayer, T. S.; Mohney, S. E. *J. Appl. Phys.* **2009**, *105*.

21. Cheng, L. W.; Lo, H. M.; Cheng, S. L.; Chen, L. J.; Tsai, C. J. *Materials Science and Engineering a-Structural Materials Properties Microstructure and Processing* **2005**, *409*, 217.

22. Mangelinck, D.; Hoummada, K. *Appl. Phys. Lett.* **2008**, *92*.

23. Chen, S. Y.; Chen, L. J.; Tzeng, S. D.; Gwo, S. *Journal of Vacuum Science & Technology B* **2005**, *23*, 1905.

24. d'Heurle, F. M. in *Diffusion in Ordered Alloys*, edited by Fultz, B., Cahn, R. W. and Gupta, D. (The Minerals, Metals and Materials Society, Warrendale, PA, **1993**), p. 185.

25. Nicolet, M. A. and Lau, S. S. in *VLSI Electronics Microstructure Sciences*, edited by N. G. Einsprich and G. B. Larrabee (Academic, New York, **1983**), Vol. 6, Chap. 6, p. 343.

26. Lauwers, A.; Steegen, A.; de Potter, M.; Lindsay, R.; Satta, A.; Bender, H.; Maex, K. *Journal of Vacuum Science & Technology B* **2001**, *19*, 2026.

27. Ohta, H.; Watanabe, T.; Ohdomari, I. *Japanese Journal of Applied Physics Part 1-Regular Papers Brief Communications & Review Papers* **2007**, *46*, 3277.

28. Uematsu, M.; Kageshima, H.; Shiraishi, K.; Nagase, M.; Horiguchi, S.; Takahashi, Y. *Solid-State Electron.* **2004**, *48*, 1073.

29. Murarka, S. P. *Metallization: Theory and Practice for VLSI and ULSI*, Butterworth-Heinemann, Boston, **1993**.

30. Shewmon, P. G. *Diffusion in Solid, second ed.*, The Metallurgical Society, Warrendale, PA, **1989**.

4.6. Supporting Information

The initial phase is identified as the NiSi$_2$, which maintains the epitaxial growth into the silicon nanowires.
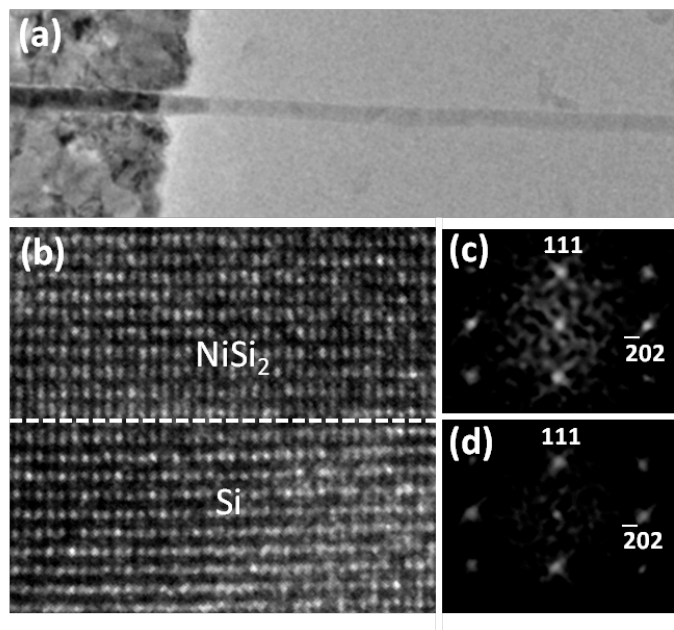

Figure 4-S1. (a) Silicide grows in bared nanowire at 550 $^\circ$C for 5 seconds. (b) High resolution images of (a) at the interface. (c-d) are FFTs of (b) which are NiSi$_2$ [1$\bar{2}$1] and Si[1$\bar{2}$1].

Si NWs were covered with Ni pad on nitride membrane and annealed at 550 $^{\circ}$C for 4 minutes. After annealing, Ni pad was completely removed by etching (TFG, Transene) for one hour at 50 $^{\circ}$C.
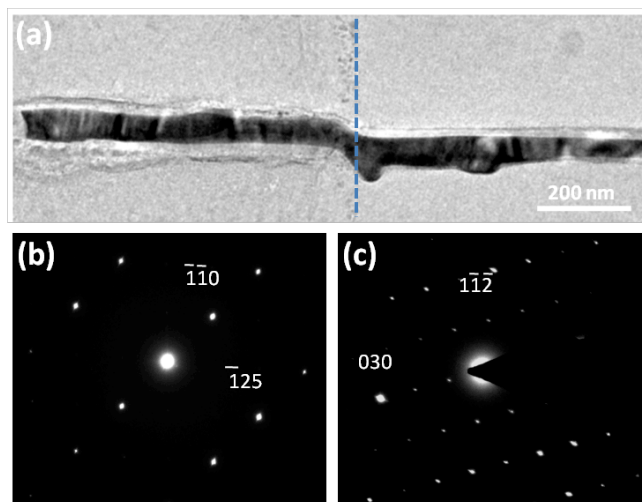

Figure 4-S2. Silicide phase analysis under metal pad. (a) TEM bright field image after removing the Nickel pad. At left of dash line, it is the original position of Nickel pad. (b) and (c) are diffraction patterns of Nickel silicide under metal pad. They are $Ni_{31}Si_{12}[5\bar{5}3]$ and $Ni_{31}Si_{12}[201]$ zone axis, respectively.

It was found that extrusion structures will appear with prolonged annealing in bare SiNWs and core/shell NWs with thin or moderate oxide thickness, which may be the result of the large volume expansion and stress pile-up found in the silicide NWs. The extrusion normally adopt the same crystal structure (silicide phase) with its surrounding phase.
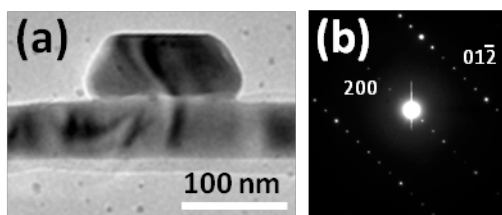
Figure 4-S3. Silicide grows in a silicon nanowire with 5~15 nm oxide at 550 $^{\circ}$C for 8 minutes (a) TEM bright field image of extrusion around Ni$_2$Si region. (b) Selected area diffraction near extrusion. It is indentified as Ni$_2$Si[021] zone axis.
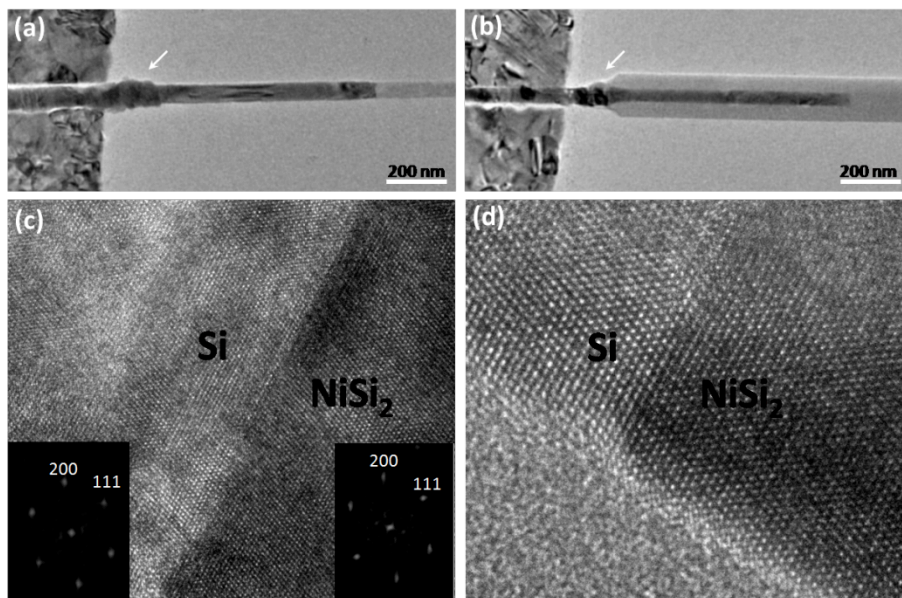
4.7. List of Figures

Figure 4-1. (a) TEM image of nickel silicide growth in bare silicon nanowire after annealing at 550 $^{\circ}$C for 60 seconds. (b) TEM image of nickel silicide growth in Si/SiOx core/shell nanowire after annealing at 550 $^{\circ}$C for 60 seconds. Arrows indicate the section of the silicide phase with larger volume. (c) High resolution TEM image of the silicide/silicon interface. The inset FFTs are identified as the NiSi$_2$[01$\bar{1}$] zone axis and the Si[01$\bar{1}$] zone axis. (d) Enlarged images of (c) showing atomic resolution around the interface.
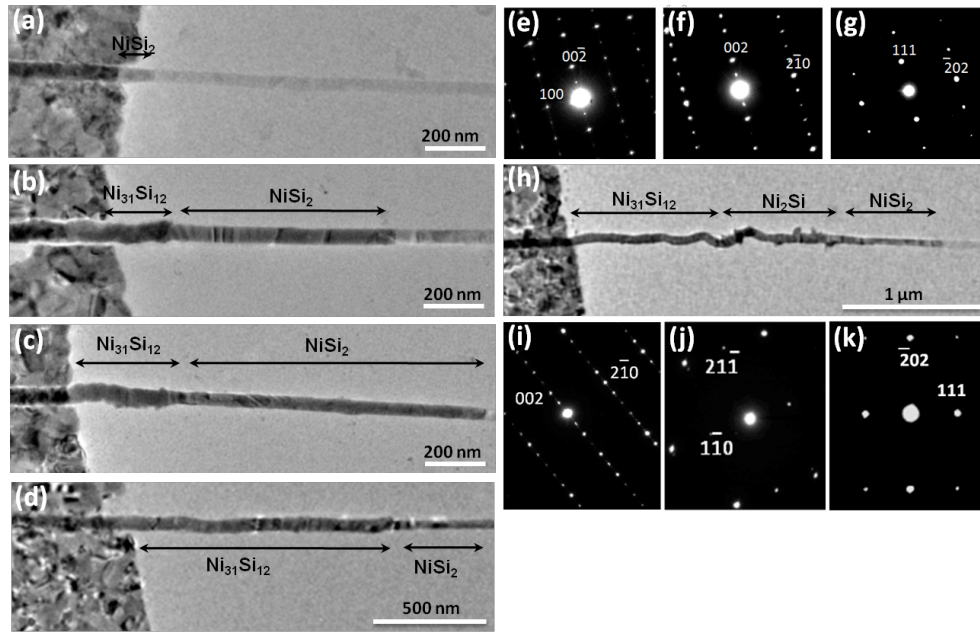
Figure 4-2. Silicide growth in various duration of annealing time at 550 °C. (a) Anneal for 5 seconds. The phase is identified as $NiSi_2$. (b) Anneal for 60 seconds. Two phases exist in the nanowire. They are $Ni_{31}Si_{12}$ and $NiSi_2$. (c) Anneal for 2 minutes. Two phases exists in the nanowire. (d) Anneal for 8 minutes. (e-f) are diffraction patterns of silicide with larger volume in (d). They represented the $Ni_{31}Si_{12}[010]$ and $Ni_{31}Si_{12}[120]$ zone axis, respectively. (g) Diffraction pattern of silicide with small volume in (d). It is $NiSi_2[1\bar{2}1]$ zone axis. (h) Anneal for 8 minutes. Another metal-rich phase, Ni_2Si is found and indicated. (i-k) diffraction patterns of (h): they are identified as $Ni_{31}Si_{12}[120]$, $Ni_2Si[113]$, and $NiSi_2[1\bar{2}1]$, respectively.
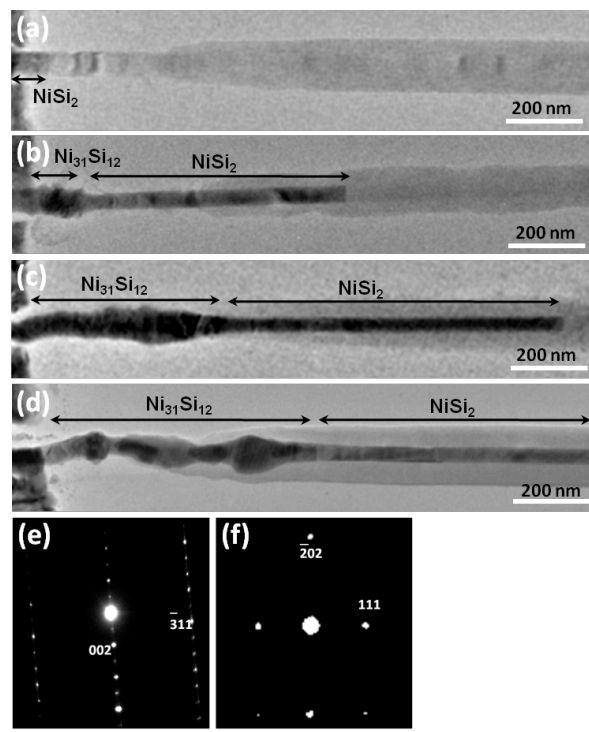
Figure 4-3. Snap-shot TEM images of nickel silicide growth in the Si/SiOx core/shell NW for various annealing durations at 550 $^\circ$C. (a) Anneal at 550 $^\circ$C for 5 seconds. The initial phase is identified as NiSi$_2$. (b) 60 seconds. (c) 2 minutes. (d) 8 minutes. In (b-d), there are two phases in the formed silicide NW, Ni$_{31}$Si$_{12}$ and NiSi$_2$, the same as those appear in bare Si NW. (e) Diffraction pattern from the large volume silicide area in (d). It is identified as Ni$_{31}$Si$_{12}$ [130] zone axis. (f) Diffraction pattern of the silicide with smaller volume in (d). It is identified as NiSi$_2$[1$\bar{2}$1] zone axis.

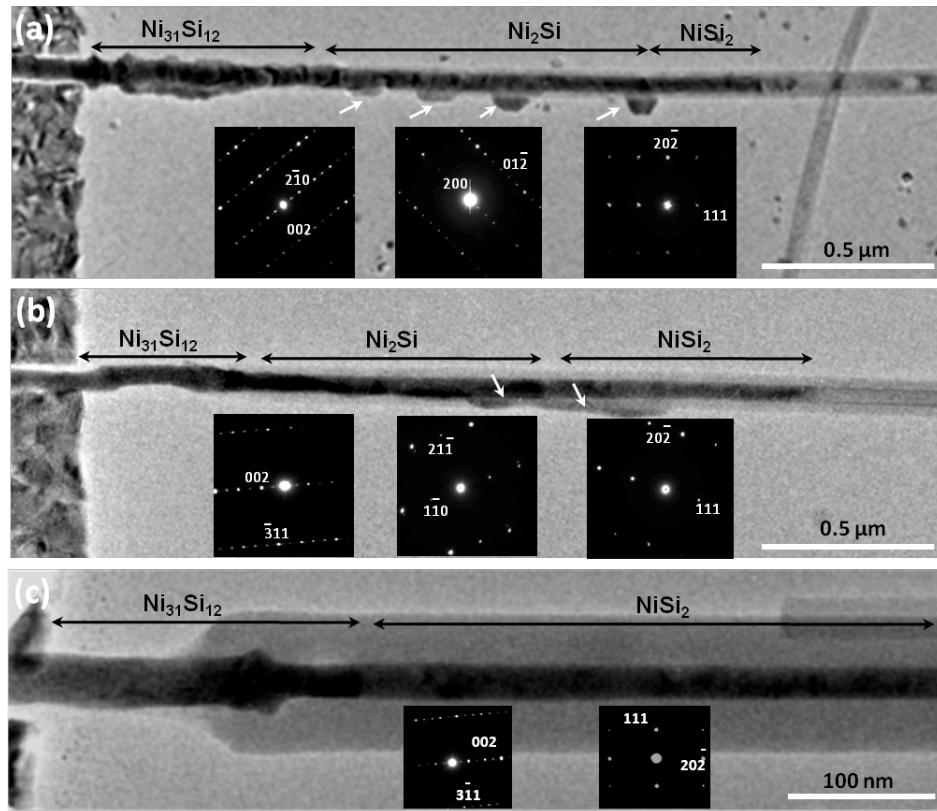**Figure 4-4.** Nickel silicide growth in Si/SiOx core/shell NWs with various oxide shell thickness. (a) Silicide growth in a Si/SiOx with 5~15 nm oxide shell at 550 °C for 8 minutes. Inset diffraction patterns represent $Ni_{31}Si_{12}$[120], Ni_2Si[021] and $NiSi_2[\bar{1}2\bar{1}]$ zone axis, respectively, showing the three phases are $Ni_{31}Si_{12}$ close to the pad, Ni_2Si in the middle and $NiSi_2$ at interface. Extrusion structures are frequently observed with the same crystal structure to its surrounding silicide phase. (b) Silicide growth in the Si/SiOx NW with ~25 nm oxide shell thickeness at 550 °C for 8 minutes. The inset electron diffraction patterns show that the phases are identified as $Ni_{31}Si_{12}$[130] close to the pad, Ni_2Si[113] in the middle and $NiSi_2[\bar{1}2\bar{1}]$ at interface, respectively. (c) Silicde growth in a Si/SiOx core/shell NW with ~50 nm oxide shell at 550 °C for 8 minutes. The silicide phases identified by electron diffraction are $Ni_{31}Si_{12}$[130] and $NiSi_2[\bar{1}2\bar{1}]$. The growth of the $Ni_{31}Si_{12}$ in Si/SiOx is limited to a short length, and Ni_2S is not present.

Chapter5: Control the Pollycrystalline and Single-Crystal Growth of Manganese Silicide & Iron Germanide NWs in the Confined Oxide Shell

5.1. Introduction

Silicides and germanides in the morden era are crucial for nanoelectronics technology, where they serve as contact materials or interconnections.[1-3] Those electrical contacts forming through solid reaction can improve the contact performance by reducing the interface defects, contaminations, and electrical insulating layer (interface oxide). Thus, upon utilizing Si or Ge technology, silicide and germanide contacts are the most important part for high performance devices. For current ultra-small devices or NW (NW) devices, with relatively smaller contact area, few grain boundaries (GBs) in silicide or germanide contact materials will cause serious degradation to device reliability such as test fails of stress migration or electromigration.[4, 5] For other small signal device applications, few GBs may serve as free carriers' traps, leading to losing of carrier polarization, increasing of background noise or larger signal hysteresis.[6, 7] To gauge the above issues, single-crystal growth of contact materials attracts more and more attention in those technologies.

Spintronics is one of the fields that require high quality of magnetic contacts and interface.[8-10] For those magnetic contacts, they have attracted intense research since been a crucial part to realize the spintronics with higher signal-to-noise ratio due to their high spin polarization and better interfacial properties between ferromagnetic materials (FM) and channel materials. However, ferromagnetic metals (Fe, Co) on silicon or germanium usually form a non-magnetic

dead layer, nonmagnetic silicide, germanide or alloying during high temperature process, leading to low spin polarized injection.[11] In order to solve this issue, one possible way is to grow the magnetic silicide or germanide directly as the ferromagnetic contacts with good interfacial properties. Up to now, only Fe_3Si and Mn_5Ge_3 thin intermetallic films have been epitaxially grown on Ge due to the smaller lattice mismatch. In addition, the growth of those materials relies on the molecular beam expitaxy (MBE)[12-15]. To date, rare research is regarding other robust growth methods for ferromagnetic germanide or silicide nanostructures. For the nano-contact engineering, the compatible processes with current device structures and the growth of nanoscale contact materials (contacting in the small via-hole < 100 nm) have been regarded as the most important aspects in the future. [16, 17]

Here, we report on controlling the growth of single crystal, Mn_5Si_3 and Fe_5Ge_3 NWs to form nano-contacts with Si or Ge NWs by solid reaction method. The crystal structure of Mn_5Si_3 is of the $D8_8$ type (space group $P6_3/mcm$) and the manganese atoms are located in two different crystallographic sites. This silicide has been reported as antiferromagnetic materials and also can be converted to room-temperature ferromagnetic material by carbon implantation. For the iron germanide (Fe_5Ge_3), they can adopt $InNi_2$ ($B8_2$) structure, a hexagonal structure (space group $P6_3/mmm$), with various composition ratio for iron and germanium. According to the literature, the Currie temperature of the iron germanide (Fe_5Ge_3) is above the room-temperature up to 450 K.

5.2. Experimental

Si and Ge NWs were grown by vapor-liquid-solid (VLS) method and used as the growth template for silicide and germanide NWs. First, Si or Ge NWs suspended in alcohol were drop

on the SiO_2 substrate (or on glassy SiNx membranes for TEM analysis). Then the NWs were patterned by ebeam lithography. Manganese or iron metal was deposited on the patterning area and followed by lift-off process. Aluminum oxide ~10-30 nm was grown to wrap the Si or Ge NWs (Fig. 5-1 schematic). The oxide confinement structure was used to limit the void formation or break of NWs during the silicide and germanide growing process. The oxide-wrapped NWs were annealing at 600-700°C to form the single crystal silicide (germanide) NWs and silicide/Si (germanide/Ge) NW heterostructure.

5.3. Results and Discussion

5.3.1. Manganese silicide formation in the oxide/Si core-shell NW with various oxide thickness

Si NWs patterned with Mn pad and wrapped with 10-nm shell, 30-nm shell are shown in the figure 5-1 schematics. After rapid thermal annealing process (RTP) for 30 seconds at 650^{0}C, manganese silicide, Mn_5Si_3, starts to grow into the Si NWs. For the small Si NWs ~20-30 nm, single-crystal silicide is grown into Si NWs (Fig 5-1a. & Supporting Fig 5-1a, b). Increasing the diameter of Si NWs to 50 and 80 nm, polycrystalline silicide is observed with transverse grain boundaries and void forms near the silicide/Si interface. For 50-nm Si NWs with oxide shell, 10-nm shell can only suppress the void formation near the silicid/Si interface (Supporting Fig 5-4a) but the grain boundaries across the silicide NWs is still observed (Fig 5-1e). As the oxide is thicker than 30 nm (Fig 5-1f & Supporting Fig 5-3a), single-crystal grain is formed in the 50-nm NWs with flat interface (no voids). If the diameter of Si NWs increases to 80 nm, with 30-nm oxide silicide still grows as polycrystalline structure but oxide shell can eliminate the voids near the interface or silicide (Fig 5-1g & Supporting Fig 5-3b). In Fig 5-1b, c, e, it shows that

manganese polycrystalline silicide forms with irregular shape and the volume expands for two times compared to original Si NWs. However, the volume expansion doesn't seriously happen in the 20-nm NWs (Fig 5-1a,d). It indicates that single-crystal silicide growth adopts the original shape of Si NWs and releases the strain (volume expansion) in the axial direction but for polycrystalline silicide, the grain growth is randomly oriented, causing the rough morphology. With thicker oxide shell (30 nm), it shows an effect, leading to a single grain growth and adopting original Si NW shape for silicide growth. The oxide confinement effect causes single-crystal growth, which is similar to the growth by reducing the NW's diameter. Thus, we propose that oxide shell can suppress the numbers of nucleation nuclei in the cross-section area and significantly influence on the single-crystal grain growth.

5.3.2. Manganese silicide formation in the oxide/non-oxide region

To verify the confinement effect of oxide shell, the oxide notch (without oxide shell) is created in the Si NWs. It is shown in the figure 5-2a, where a Si NW is partially wrapped with oxide shell. Thus, manganese silicide can grow in the oxide region initially, then through the no-oxide region and finally back to the oxide shell region. This experiment can reduce the sample-to-sample difference and temperature variation. In Fig 5-2b & 5-2c, comparing the bright field and dark field TEM images, the grain boundaries, polycrystalline and single-crystal growth area can be clearly indentified (Fig 5-2 , Supporting Fig 5-5 & Supporting Fig 5-6). In TEM analysis, it indicates that once manganese grows out of oxide shell, more grain boundaries are generated in the no-oxide region, where grain size in the axial direction is around 200-300 nm. For manganese silicide in the oxide shell, the grain can grow for more than 500 nm in the axial direction. All the grain boundaries in the figure 5-2 are across the NW diameter, not transverse

grain boundaries (Fig 5-1e). This indicates the oxide shell can suppress the formation of silicide grain boundaries, causing the larger critical grain size in the NW axial direction.

The nucleation of a silicide will be driven by the free-energy change for transformation, ΔG, and will be opposed by the surface energy associated with the increase in area of the interface, σ. As the silicide formed in the oxide shell, for most of metal-rich silicides, it will be associated with the volume expansion. The strain will be set up due to the volume change of transformation. Even though the compressive stress in the oxide shell may have influence on the crystal orientation, the volume of metal-rich silicide is still larger than original Si. It will cause silicide in the oxide shell structure to suffer high stress. If the strain energy per unit volume is ΔGs, it needs to incorporate into the free energy change, ΔGv. Therefore, a nucleus of average radius r will have a free energy per unit volume given by;

$$\Delta Gn = br^2\sigma - ar^3(\Delta Gv - \Delta Gs)$$

Where a and b are geometrical terms that account for the shape of the nucleus. With increasing radius of the nucleus, the free energy of the nucleus increase first (due to the increasing of surface energy) and then decreases (due to the decreasing in the free energy), passing a maximum at a critical size, r^*. Nuclei smaller than the critical size will exist in an equilibrium distribution, whereas those larger than the equilibrium size will tend to grow. Since the strain energy, ΔGs, is always positive, it leads to the driving force, $\Delta Gv - \Delta Gs$, for the nuclei to grow is lower (Supporting materials, **Strain energy calculation for silicide in the core-shell NW**). Thus, the critical radius, r^*, and the free energy of critical nuclei, ΔG^*, will increase due to the strain energy in the oxide shell. Considering the rate of nucleation, ρ^* which is proportional to the concentration of critical nuclei, it can be expressed as

$$\rho^* = K exp\left(-\frac{\Delta G^*}{kT}\right) \exp\left(-\frac{Q}{kT}\right)$$

Where K is a constant and Q is related to the activation energy for diffusion. Under strain the nucleation rate will decrease due to the increase of the nucleation barrier energy, ΔG^*. Single-crystal growth can attribute to the lower nucleation rate in the core-shell NWs. This explains why the single-crystal growth of manganese silicide is observed in the thicker oxide shell (Fig 5-1f).

5.3.3. Growth of iron germanide NW and germanide/germanium heterostructure

The oxide shell assisted single-crystal materials' growth can be extended to other material systems by reducing the nucleation rate in the stressed shell. Here, we try to grow germanide in the oxide (~ 20-30 nm)/Ge core-shell NWs. By the TEM analysis, iron germanide can grow into the germanium NW with automatically sharp interface shown in Fig 3a,b. The selective electron diffraction pattern in Fig. 3a, inset, showed a single-crystal property near the interface with grain size ~ 1 μm long in the NW axial direction and corresponding to the Fe_5Ge_3 lattice structure. The energy dispersion spectrum (EDS) analysis (Fig 5-3c) verified iron-rich composition and the iron-to-germanium ratio was ~1.5 ± 0.15 for most germanide NWs (more than 20 NWs).

In order to investigate the crystal structure, high-resolution TEM was used to analyze the crystal properties of germanide NWs. Two different diameters of germanium NWs, ~50 nm and ~30 nm, wrapped in 30-nm oxide shell were used as the germanide growth templates. For NWs with ~50 nm diameter, the epitaxial relation, $Ge[\bar{1}10]$ // $Fe_5Ge_3[11\bar{2}0]$ and $Ge(111)$// $Fe_5Ge_3(0001)$, was observed with a lattice mismatch ~0.5 % in Fig. 5-3d-f. The same epitaxial relation was often observed in thin film growth, single-crystal Fe_5Ge_3 thin film grown

on Ge(111) substrate. The schematic of the germanide crystal orientation related to the NW was shown in Fig. 3j. The c-axis of hexagonal germanide was parallel to the germanium NW growth direction. Interestingly, for the NWs with ~30 nm diameter, another epitaxial relation, Ge[$\bar{1}$10]// Fe$_5$Ge$_3$[01$\overline{\bar{1}\ 1}$2] and Ge(111)// Fe$_5$Ge$_3$($\bar{2}$201), was adopted. This epitaxial relation was with larger lattice mismatch ~1.8% in Fig. 5-3g-i.

Germanide NWs usually grew faster in the smaller diameter of germanium NWs. While the constant metal source was assuming, the growth rate of germanide NW may be simplified as $\propto 1/r$ (r is the diameter of NWs). With the fast growth rate, the interface of the small germanide NW may become difficult to arrange in the more cross-packed structure. It may be the reason that the epitaxial relation in Fig. 5-3k was observed in the small NWs. Other possible reasons for existing the two different epitaxial relations may be due the occurrence chances of the nucleation events or surface energy dominating at nanoscale. These interesting phenomena need more detail experiment and analysis to examine. The germanide crystal orientation of Fig. 5-3g was shown in the Fig. 5-2k; the c axis of germanide crystal was deviated from the axial direction for ~70.9°. In this tilting condition, the Fe$_5$Ge$_3$ crystal structure can adjust atoms into an new arrangement with a hexagonal shape to contact with Ge(111) with less lattice mismatch (Supporting Fig. 5-7). These two epitaxial relations, c axis // axial axis and c axis tilted from axial axis, were observed in the ~50-nm and ~30-nm NWs, respectively.

5.3.4. The magnetic properties of germanide NW

To investigate the magnetic properties of the single-crystal germanide NWs, the magnetic force microscope (MFM) was utilized to explore the magnetic domains at the room temperature.

In Fig. 5-4a, after annealing at 600°C for 20 seconds, there was a clear contrast difference between Fe_5Ge_3 and Ge in the ~30 nm NW in the SEM image. The same sample was then scanned by atomic force microscope (AFM) in Fig. 5-4b; there was no obvious volume change after the germanide formed. The diameter of the NW was ~28 nm which was verified by the height information ~48 nm to deduct ~20 nm ALD oxide shell. By the MFM analysis, a clear phase contrast can be distinguished between germanide and germanium. Only germanide showed a phase shift in the interleave mode; it represented that the portion of germanide NW was ferromagnetic at room temperature. The length of germanide NW was consistent with the observation in SEM (Fig. 5-4a). A region near the interface showed a bright contrast with a long-strip shape ~ 1 μm long (Fig. 5-4c & Supporting Fig. 5-8). It was corresponding to a single-domain region with out-of-plane magnetization and the enlarged image was shown in the figure 5-4d. Further, in Fig. 5-4e the counterpart image was used to verify the ferromagnetic properties of the germanide NW by reversing the magnetization of the MFM tip. It also showed a single domain near the interface with dim contrast. For the ~50 nm NW, the AFM and MFM images were shown in the figure 5-4f,g (Supporting Fig. 5-9). The region near the pad showed a more random domain structure (Fig. 4g) which is also observed in the 30-nm NWs and the volume expanded in the corresponding AFM images (Fig. 5-4f). The germanide NW near the pad grew as the polycrystalline structure verified by TEM analysis (Supporting Fig. 5-10). The region near the interface showed an in-plane magnetization; the magnetization direction was parallel to the NW axial direction. The schematics shown in Fig. 5-4h (out-of-plane magnetization) & 5-4i (in-plane magnetization), were clearly utilized to describe the magnetization direction corresponding to 30-nm NWs (Fig. 5-4d) and 50-nm NWs (Fig. 5-4g).

The magnetic domains of the germanide NWs show an out-of-plane and in-plane magnetization for ~30 nm and ~50 nm germanide NWs. For the magnetic anisotropy, it may be induced by three mechanisms: shape anisotropy, magnetocrystalline anisotropy and stress anisotropy. In our results, the shape anisotropy may play a minor role since the magnetization of ~50 nm germanide NWs lies in the NW axial direction. However, the magnetization of ~30 nm germanide NWs is toward the out-of-plane direction. Thus, the shape anisotropy should not dominate. In addition, the region close to the pad is polycrystalline with random orientations (Supporting Fig. 5-10). In the same region, the magnetic domains display more random domains (Fig. 5-4 & Supporting Fig. 5-8 & 5-9). This also verifies that the crystal orientation plays a more important role than shape anisotropy. To gauge the magentocrystalline anisotropy (related to crystal structure) in germanide NWs, crystal orientations are compared with the magnetic domains (Fig. 5-3 and Fig. 5-4). Now the magnetization of 50-nm NWs is in-plane with c-axis lying in the axial direction; the magnetization of 30-nm NWs is out-of-plane with tilted c axis ~70.9° from NW axial direction.

According to the literatures, c-axis is the magnetic hard axis for Fe_5Ge_3 and the easy axis is on the hexagonal basal plane (a axis). The magnetization aligned with c axis will lead to the higher energy. Thus, the spontaneous magnetization will tend to lie on the basal plane, called magnetocrystalline anisotropy. The magnetocrystalline anisotropy properties for Fe_5Ge_3 have been experimented and proved in the bulk (single-crystal ingot) and thin film structure to change magnetization to c axis by applying the compressive stress on the basal plane. In our results, MFM analysis for 50-nm germanide NW in Fig. 5-4g shows an in-plane magnetization and the c-axis also lies in the axial (in-plane) direction (Fig. 5-3d-f). This behavior is deviated from the result that the magnetization polarization will be away from c axis for Fe_5Ge_3. Thus, another

anisotropy effect may also influence the resulting magnetic domains in our germanide NWs. The stress effect may need to be considered in the core-shell germanide NWs. For the stress, the oxide shell will provide the compressive stress (or residual stress) in the radial direction after the annealing or germanided processes. The stress anisotropy is related with spin-orbit coupling called magnetostriction. Upon magnetization, a previously demagnetized crystal experiences a strain that can be measured as a function of applied field along the principal crystallographic axes. A magnetic material will therefore change its dimension when magnetized. The inverse effect, or the change of magnetization with stress also occurs. A uniaxial stress can produce a unique easy axis of magnetization if the stress is sufficient to overcome all other anisotropies. Theoretically, the stress-induced anisotropy field is given by $3\lambda\sigma/M_s$, in which $\lambda(001,100)\sim -20\times10^{-6}$ is the magnetostriction coefficient ($\lambda(001,100)$ means the strain measured along [100] when the magnetization is parallel to [001]), $\sigma = Y\varepsilon$ is a uniaxial stress, Ms is the saturation magnetization, Young's modulus $Y\sim1.1\times10^{12}$ dyn/cm^2 and the strain value, ε). Regarding the magnetocrystalline anisotropy field of $2K_1/M_s$ with the magnetocrystalline anisotropy constant, $K_1 = 5.1\times10^6$erg/cm^3. Assuming that the compression strain ε ~5% to 10%, it results that the stress-induced anisotropy field is $\sim3.3\times10^6/M_s - 6.6\times10^6/M_s$ which is comparable to magnetocrystalline field $\sim 10.2\times10^6/M_s$. The theoretical calculation only considers the uniaxial stress in the materials. In the core-shell NWs, the wrapped oxide may provide larger stress to contribute to the stress-induced anisotropy field. Therefore, the stress anisotropy may dominate the magnetic anisotropy.

For the core-shell (oxide/germanide) NWs, a compressive stress usually exists around the NW in the radial directions. For both 50-nm and 30-nm NW, the wrapped oxide shell will exert a compressive stress on the germanide NW during the growth. The magnetization of 50-nm

Fe$_5$Ge$_3$ NW may tend to align with c-axis since the materials has been reported to have positive magnetostriction constant in c-axis direction and negative magnetostriction constant in a-axis direction. It means that if the compressive stress is applied on the basal plane, the c axis may replace as the unique easy axis to reduce the total crystalline energy. Therefore, for 50-nm NW since the a-axis and hexagonal basal plane is stressed compressively by the oxide shell, the magnetization lying in the c-axis direction will lower the energy and thus in the NW axial direction. For the 30-nm germanide NW, it adopts the out-of-plane magnetization. If considering the tilted c axis, the stress distribution related to basal plane and c-axis is more complicated. However, for stress anisotropy dominating system, only basal plane perpendicular to NW axial direction will lead to the in-plane magnetization. Thus, for 30-nm NW, due to the tilted c-axis the out-of-plane magnetization is a rational result. The further experiments are necessary to prove and verify which anisotropic effects dominate in the stressed core-shell germanide NWs, leading to the interesting anisotropic domains. However, stress effect may provide us the rational explanation for the magnetic anisotropy in both 30-nm and 50-nm NW.

5.4. Conclusion

In conclusions, Mn$_5$Si$_3$ and Fe$_5$Ge$_3$ NW were grown with single-crystal properties and germanide/germanium heterostructure were grown to have two kinds of epitaxial interface relation in the oxide shell. In addition, Mn5Si3 single-crystal or polycrystalline growth has been systematically studied with various oxide thickness and Si NW diameters. Single-crystal growth of Mn5Si3 can be achieved by reducing the Si NW diameter to 20-30 nm or applying the thick oxide shell ~30 nm. Single-crystal growth of contact materials can be also implemented for germanide materials. The iron-rich germanide, Fe$_5$Ge$_3$, was successfully grown with single-

crystal properties. It shows ferromagnetic properties with a Curie temperature above the room temperature verified by magnetic force microscope (MFM). Interestingly, two different epitaxial relations found at germanide/germanium interface due to the different sizes of the germanium NW templates. These two different crystal structures exhibited magnetic anisotropy in magnetic force microscope (MFM) measurement, showing differently preferred domain orientations. In-plane and out-of-plane magnetization in the Fe_5Ge_3 NWs are observed in our experiment. The crystal orientation or engineering stress may have influence on the magnetic domain structure. This ferromagnetic contact material may open the way for spintronics to grow the magnetic materials on the semiconducting materials and control the direction of magnetization in the future.

5.5. References

1.   J. P. Gambino and E. G. Colgan, *Mater Chem Phys*, 1998**, 52**, 99-146.

2.   C. Lavoie,F. M. d'Heurle,C. Detavernier and C. Cabral, *Microelectron Eng*, 2003**, 70**, 144-157.

3.   S. Y. Zhu,R. Li,S. J. Lee,M. F. Li,A. Y. Du,J. Singh,C. X. Zhu,A. Chin and D. L. Kwong, *Ieee Electr Device L*, 2005**, 26**, 81-83.

4.   T. Jarmar ,J. Seger,F. Ericson,D. Mangelinck,U. Smith and S. L. Zhang, *J Appl Phys*, 2002**, 92**, 7193-7199.

5.   Y. Koubuchi,J. Onuki,M. Suwa,S. Fukada,S. Moribe and Y. Tanigaki, *J Vac Sci Technol B*, 1990**, 8**, 1232-1238.

6.   D. M. Fleetwood,P. S. Winokur,R. A. Reber,T. L. Meisenheimer,J. R. Schwank,M. R. Shaneyfelt and L. C. Riewe, *J Appl Phys*, 1993**, 73**, 5058-5074.

7.   J. E. Evetts,M. G. Blamire,N. D. Mathur,S. P. Isaac,B. S. Teo,L. F. Cohen and J. L. Macmanus-Driscoll, *Philosophical Transactions of the Royal Society of London Series a-Mathematical Physical and Engineering Sciences*, 1998**, 356**, 1593-1613.

8.   A. Schmehl,V. Vaithyanathan,A. Herrnberger,S. Thiel,C. Richter,M. Liberati,T. Heeg,M. Rockerath,L. F. Kourkoutis,S. Muhlbauer,P. Boni,D. A. Muller,Y. Barash,J. Schubert,Y. Idzerda,J. Mannhart and D. G. Schlom, *Nat Mater*, 2007**, 6**, 882-887.

9.   B. T. Jonker, *P Ieee*, 2003**, 91**, 727-740.

10.   A. Anguelouch,A. Gupta,G. Xiao,D. W. Abraham,Y. Ji,S. Ingvarsson and C. L. Chien, *Phys Rev B*, 2001**, 64**.

11.   L. N. Tong,M. H. Pan,J. Wu,X. S. Wu,J. Du,M. Lu,D. Feng,H. R. Zhai and H. Xia, *Eur Phys J B*, 1998**, 5**, 61-66.

12.   F. T. Lin,D. M. Jiang,X. M. Ma and W. Z. Shi, *Thin Solid Films*, 2007**, 515**, 5353-5356.

13.   A. Sellai,A. Mesli,M. Petit,V. Le Thanh,D. Taylor and M. Henini, *Semicond Sci Tech*, 2012**, 27**.

14.   A. Spiesser,M. T. Dau,L. A. Michez,M. Petit,C. Coudreau,A. Glachant and V. L. Thanh, *Int J Nanotechnol*, 2012**, 9**, 428-438.

15.   T. Miyoshi,T. Matsui,H. Tsuda,H. Mabuchi and K. Morii, *J Appl Phys*, 1999**, 85**, 5372-5374.

16.   T. Morimoto,T. Ohguro,H. S. Momose,T. Iinuma,I. Kunishima,K. Suguro,I. Katakabe,H. Nakajima,M. Tsuchiaki,M. Ono,Y. Katsumata and H. Iwai, *Ieee T Electron Dev*, 1995**, 42**, 915-922.

17.   H. Iwai,T. Ohguro and S. Ohmi, *Microelectron Eng*, 2002**, 60**, 157-169.

5.6. Supporting Information

**Manganese silicide growth with various oxide shell:**
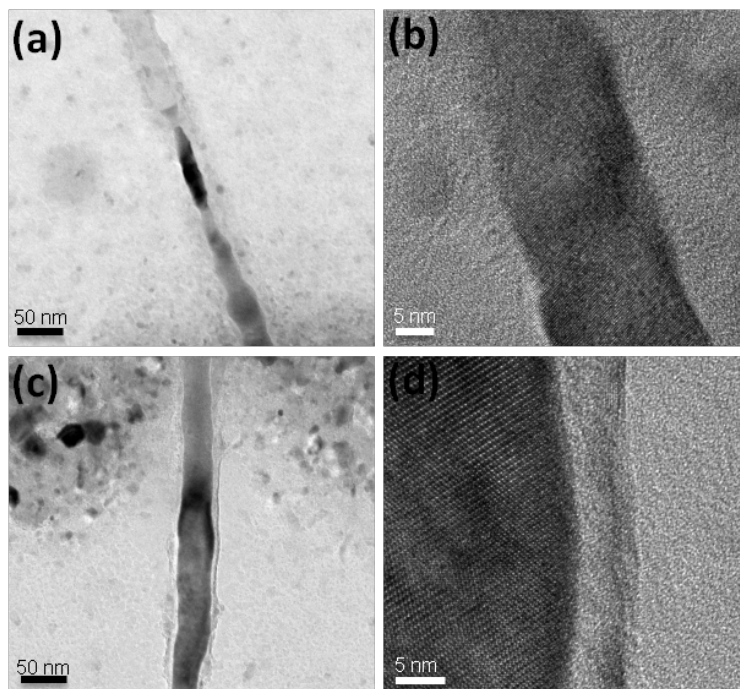
Supporting Figure 5-1. Manganese silicide grown in the small Si NWs ~20-30 nm. (a-b) Manganese silicide growns in the bared Si NWs. It shows a single-crystal property. (c-d) Manganese silicide grows in the 10-nm Si-oxide core-shell NWs. It shows a single-crystal property.
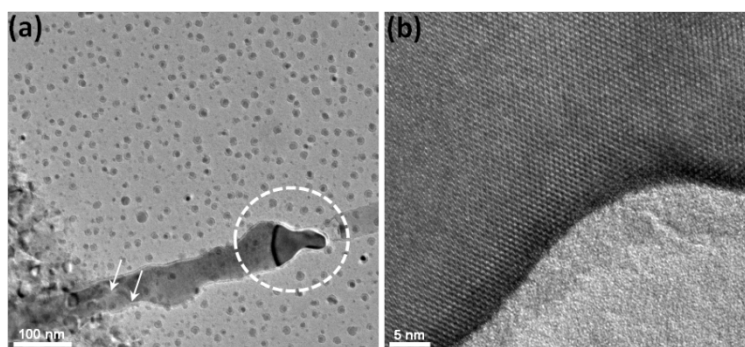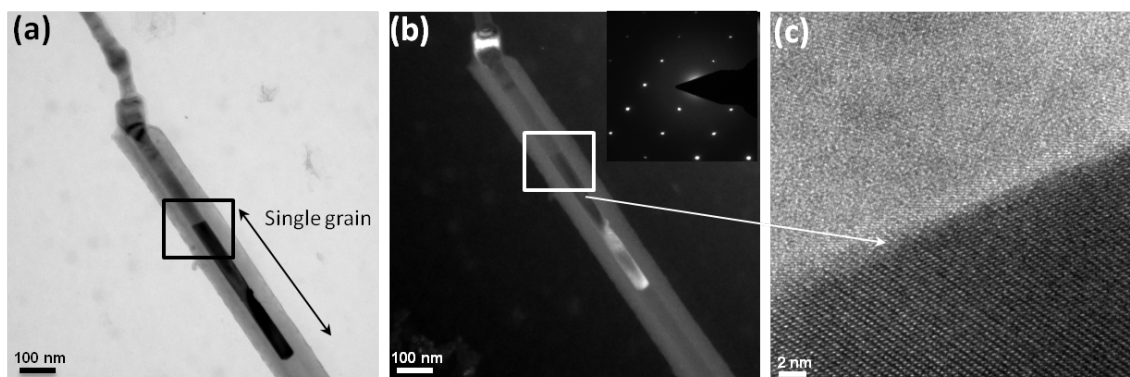
Supporting Figure 5-2. Manganese silicide grown in the Si NWs ~50 nm. (a) A TEM bright field image shows manganese silicide grows in the 50 nm Si NW. An arrow indicates a grain boundary. The circular area shows a grain near Silicide/Si interface and a void formed around the interface. (b) a high resolution images of the grain near the interface.
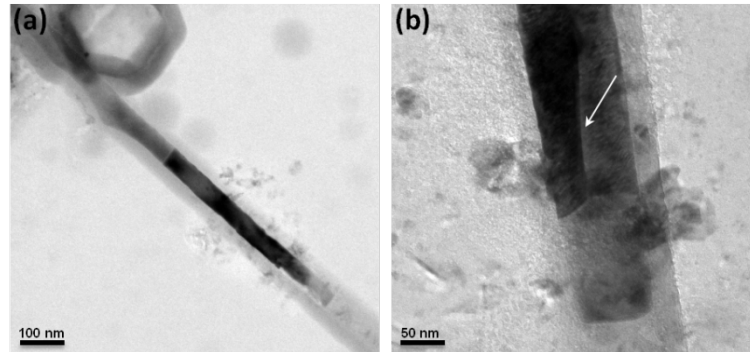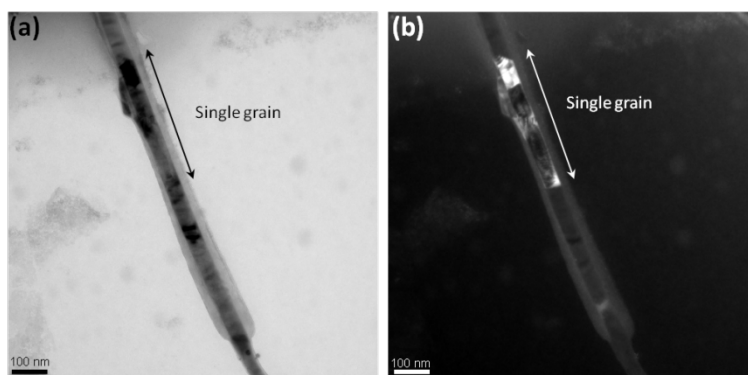

Supporting Figure 5-3. Manganese silicide grown in the 50 nm (a) and 80 nm (b) NWs with 30 nm oxide shell. (a) It shows a single-crystal property. (b) It shows a poly-crystalline property. A transverse grain boundary is indicated by an arrow.
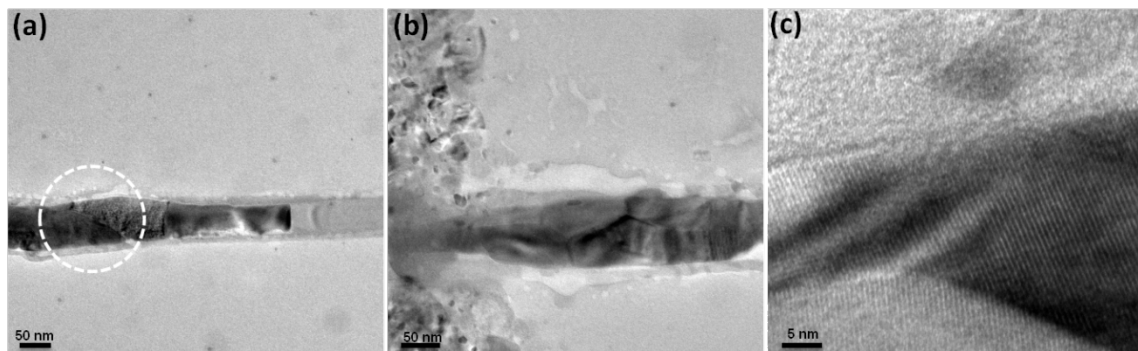
Supporting Figure 5-4. Manganese silicide grown in the 50 nm Si NW with 10 nm oxide shell. (a-b) Silicide NWs show polycrystalline properties. (c) A high resolution image of circular area in (a).

Supporting Figure 5-5. Manganese silicide formation in the oxide/non-oxide NW. (a) A bright field image of manganese NW. (b) A dark field image of (a). (c) A high resolution image of grain boundary region.

Supporting Figure 5-6. Manganese silicide formation in the oxide/non-oxide NW. (a) A bright field image of manganese NW. (b) A dark field image of (a). It indicates a single grain can grow for more than 0.5 µm.

Epitaxial relation analysis for Fig 3g:
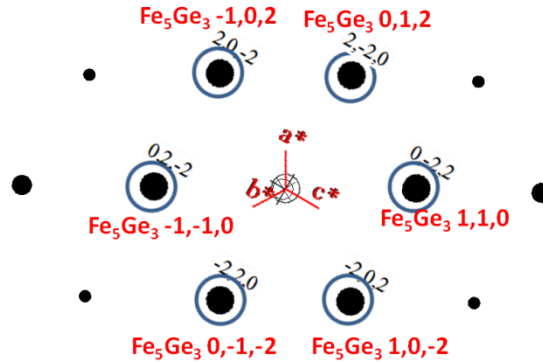
Supporting Figure 5-7. Electron diffraction for epitaxial relation around the interface in the 30 nm NW. The high resolution TEM (cross-section) is shown in Fig. 2d. The electron diffractions of Ge(111) and Fe_5Ge_3(-22-1) are simulated. This is similar to the plane-view electron diffraction (germanide on germanium). The germanide and germanium can maintain epitaxial relation with Ge[220]//Fe_5Ge_3[012] and Ge(111)//Fe_5Ge_3(-22-1) relation. The blue circle represents the Ge diffraction spots and black spots represents the germanide diffraction spots.

Observation of Magnetic Anisotropy in Iron Germanide NWs

MFM measurement for 30 nm NWs: they all show an out-of-plane magnetization.
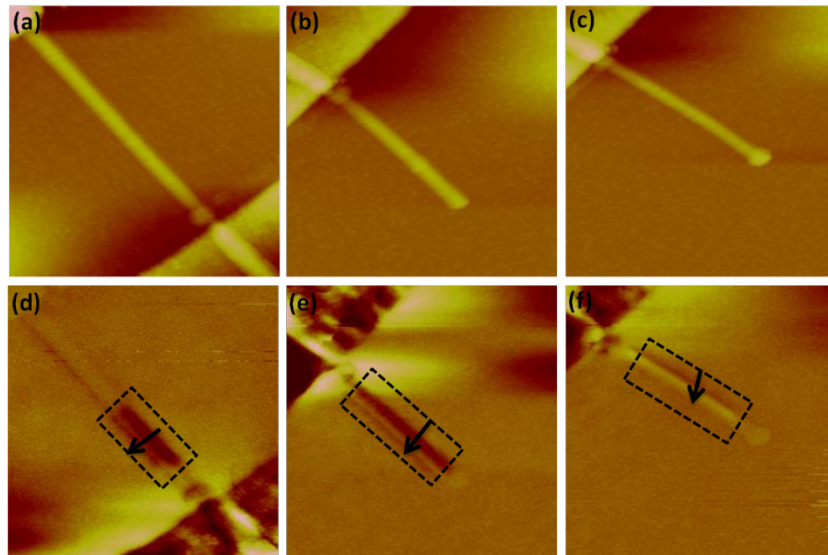
Supporting Figure 5-8. The analysis of magnetic force microscope for ~30 nm germanide/germanium heterostrucuture NW. (a~c) are AFM images for three different NW. From the height, the nanowrie diameter is ~30 nm. The germanide NW shows a out-plane magnetization near the germanide/gemanium interface. The regions close to the pad are multiple domians. The dash rectangular indicates a single domain region.

MFM measurement for 50 nm NWs: they all show an in-plane magnetization and the regions close to pad show random domains.
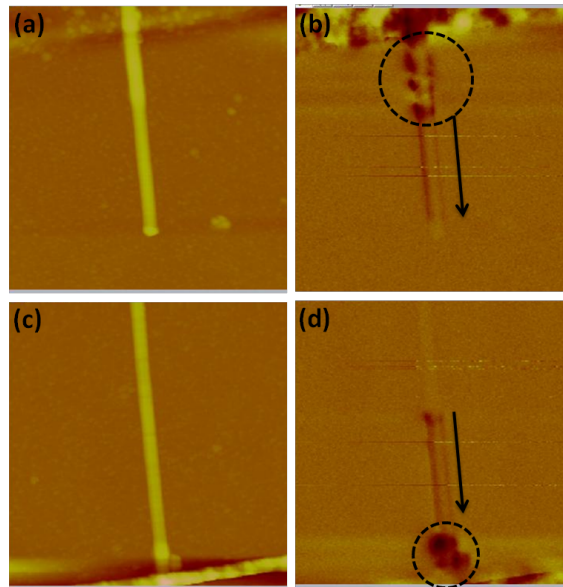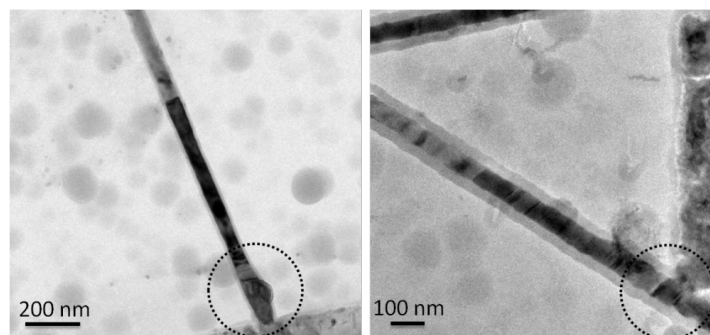

Supporting Figure 5-9. The analysis of magnetic force microscope for ~50 nm germanide/germanium heterostrucuture NW. (a) (c) are AFM images of two different NWs. (b) (d) are MFM images. The germanide NW shows a in-plane magnetization near the germanide/gemanium interface. The regions close to the pad are multiple domains.

TEM analysis for germanide NW:

Supporting Figure 5-10. TEM bright field images. The germanide NWs are polycrystalline close to the pad. The dash circle indicates polycrystalline region.

Strain energy calculation for silicide in the core-shell NW:

We assume the oxide/Sicide core-shell nanowire is under biaxial stress. The strain energy is given by

$$E_{elastic} = \int \sigma_r \, d\varepsilon_r = \frac{1}{2}\frac{Y}{1-v}(\epsilon x^2 + \epsilon y^2) \text{.....cylindrical model}$$

Case 1:

Where Young's modulus, $Y=1.98*10^{12}$ dyne/cm^2 for manganese; Poisson's ratio, $v=0.24$ for manganese. If we assume that in the NW silicide can tolerate the 10% elastic strain, the strain energy is around 0.19 eV/atom. For Manganese silicide, Mn_5Si_3, the formation energy, ΔH is around -41.6 kJ/mol /at. (0.43 eV/atom). Under 10% strain, the strain energy will have the strong influence on the silicide nucleation.

Case 2:

If the silicide is under the 0.2% strain, similar to the $NiSi_2$/Si interface, the strain energy is around $7.8*10^{-5}$ eV/atom. For this case, strain energy is around 3 order magnitude smaller than the silicide formation energy. It indicates that $NiSi_2$ in the oxide shell will not change its nucleation behavior.

In the thin film system, elastic strain with 10% is hard to build for the silicide/Si interface since the misfit dislocation is easy to generate to reduce the high strain. However, in the nanoscale, high strain is possible to exist. It has been observed in the several material systems such as NiSi/Si, PtSi/Si and MnSi/Si. Under the high strain, the strain energy is elevated and it leads to dramatic decreasing on the nucleation rate.
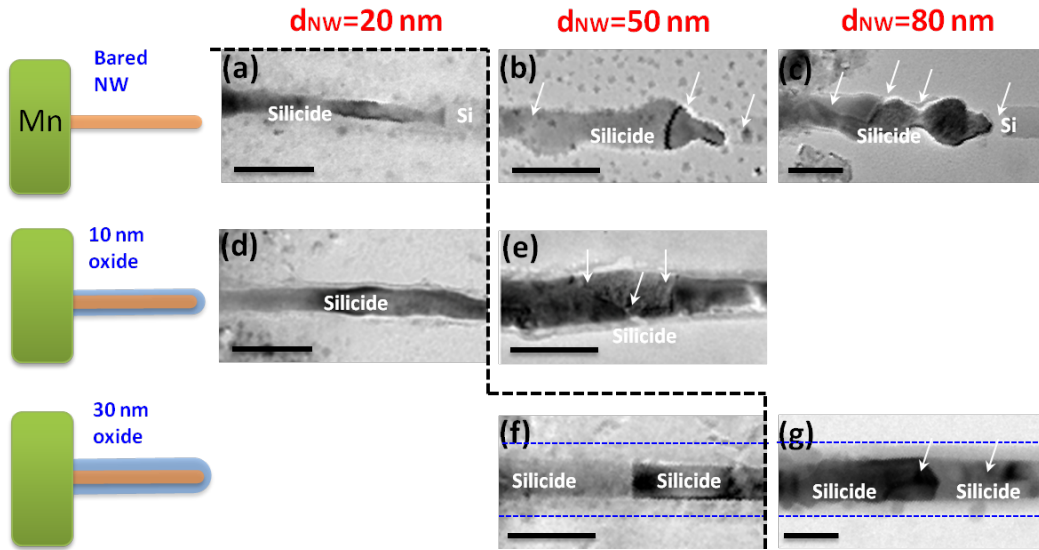
Figure 5-1. Manganese silicide formation in the oxide/Si core-shell NW with various oxide thickness. (a-c) Manganese silicide grows into bared silicon NWs with 20-nm, 50-nm, 80-nm diameter, respectively. (d-e) Manganese silicide with 20-nm and 50-nm diameter, respectively, grows into 10-nm oxide-Si core-shell NWs. (f-g) Manganese silicide with 50-nm and 80-nm diameter, respectively grows into 30 nm Si-Oxide core-shell NWs. The scale bar is 100 nm. Arrows indicate the grain boundaries and voids. At the left area of dash line, silicide grows with single-crystal properties.
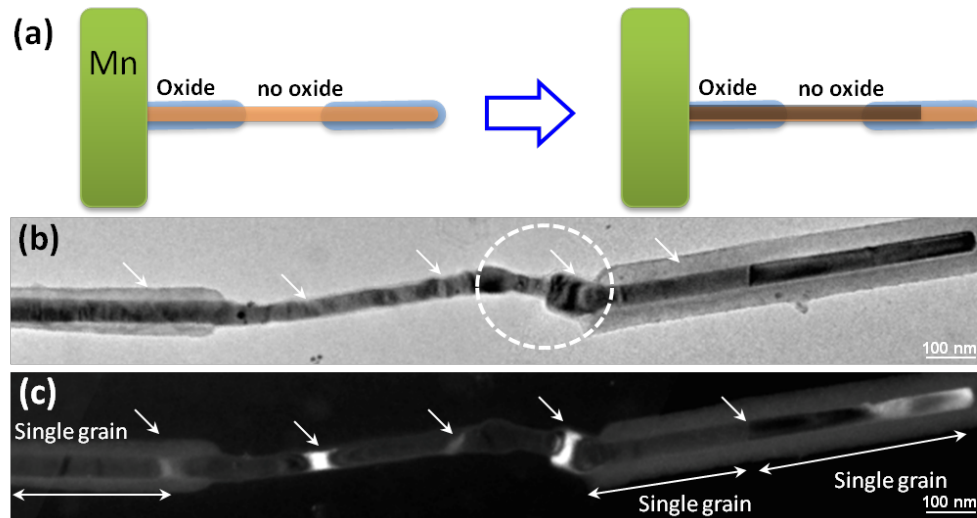
Figure 5-2. Manganese silicide formation in the oxide/non-oxide region. (a) A schematic of a manganese metal pad and silicon NW diffusion couple patterned with oxide and non-oxide region. (b) A bright field image shows a single-crystal grain in the oxide region and polystalline grains in the non-oxide region. Arrows indicate the grain boundaries. (c) A dark field image. Arrows indicate grain boundary regions . Double-side arrows indicate single-crystal grains. A selected area by a circle indicates a area with larger volume expansion. There are only few grains in the oxide region but in the bared region, the grains are more randomly oriented.
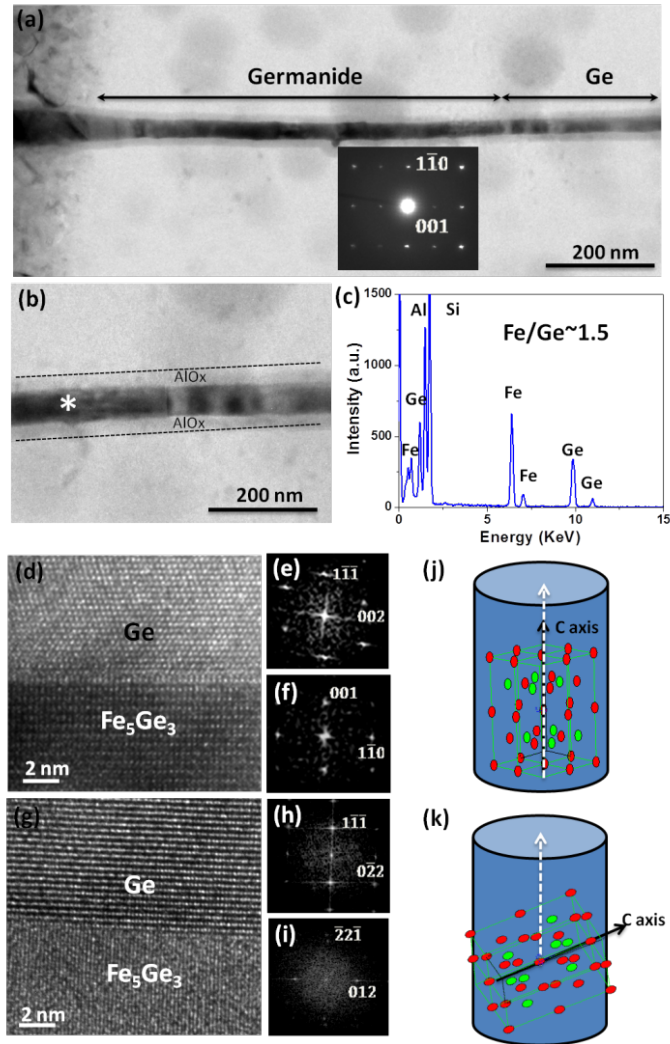
Figure 5-3. Growth of iron germanide NW and germanide/germanium heterostructure. (a) Bright field image of iron germanide/germanium NW heterostrucutre. The inset image show a germanium NW was patterned with iron pad and wrapped with AlOx shell. The structure was annealed at 600^0C to grow the germanide NW. Selective area electron diffraction pattern (SEAD,inset) indicates Fe_5Ge_3[110] zone axis. (b) A enlarged image around the interface. The dash line indicates the thickness of ALD AlOx. (c) The energy dispersion spectrum (EDS) of germanide NW. The analyzing point is indicated by the star symbol. (d) High resolution TEM image of the germanide/germanium, Fe5Ge3/Ge epitaxial interface. The diameter of germanium

NW is ~50 nm. (e) (f) are the FFT of Ge[110] zone axis and Fe_5Ge_3[110] zone axis, respectively. (g) High resolution TEM images of germanide/germanium, Fe_5Ge_3/Ge epitaxial interface. The diameter of germanium NW is ~27 nm. (h) (i) are the FFT of Ge[211] zone axis and Fe_5Ge_3[54-2] zone axis, respectively. (j) it shows the c axis of Fe_5Ge_3 NW is paralleled to the NW axial direction (white dash arrow). It represents the germanide crystal orientation for the interface relation (d). (k) it shows the c axis of Fe_5Ge_3 crystal is tilted 70.9^0 related to NW axial axis (white dash arrow). It represents the germanide crystal orientation for interface relation (g).
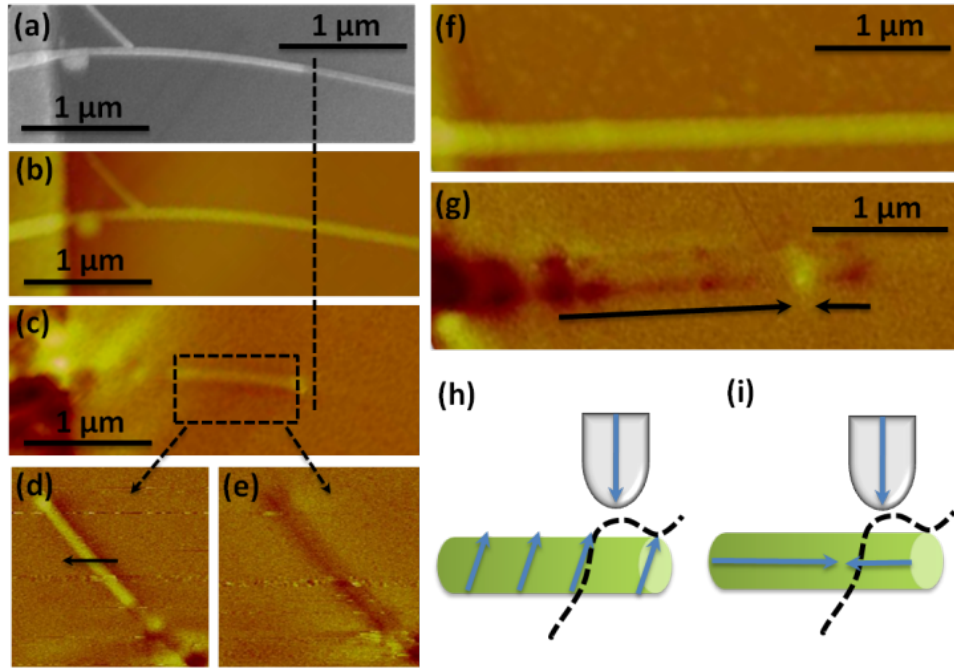
Figure 5-4. The magnetic properties of germanide NW (a) SEM image of ~30 nm germanide/germanium NW heterostructure. Bright contrast of the NW was the germanided portion. (b) The corresponding AFM image of (a). (c) The corresponding MFM phase image of (b). It showed an out-of-plane magnetization. (d) The enlarged MFM image of (c). It indicated a single domain and out-of-plane magnetization close to the interface. The length of single domian was ~1 μm. The arrow indicated out-of-plane magnetization. (e) The MFM image corresponding to (d) with reversed tip magnetization. (f) A typical AFM image of 50 nm germanide/germanium heterstructure NW. (g) The corresponding MFM image of (f). It showed an in-plane magnetization close to the germanide/germanium interface. The magnetic polarization was indicated by arrows. (h) (i) Schematic of the MFM measurement geometry which led to the out-of-plane magnetization (d) and in-plane magnetization (g), respectively. The yellow-bright color in MFM images represented the opposite magnetization between germanide NW and magnetic tip.

Chapter 6: Self-Aligned Nanolithography in a Nanogap

6.1. Introduction

Nanoscale electronics is an area of great interests due to their potential to enable computers and a variety of miniaturized electronic devices with unparalleled speed, storage and size reduction and the promise to enable totally new technologies.[1-6] To fabricate nanoelectronic devices, a critical task is to make reliable electrical contacts in the nanoscale.[7-9] The formation of nanoscale gaps represents an interesting approach to bridge individual nanostructures with macroscopic world. Nanogap structure can be used to study the charge transport in the nanometer scale such as molecular conduction,[10,11] single electron devices[12-14] and other photonic devices[15,16] that are of considerable interests due to their fundamentally new physical properties, and potential applications in future electronics. However, how to exactly align with nanostructure or reliably establish the electrical connection remains to be a significant challenge. Electron beam lithography represents a powerful approach to create nanostructures as small as 10-20 nanometers. However, the inter-layer alignment of sequential lithography steps in e-beam lithography usually comes with much less precision. State-of-the-art e-beam machine have a manufacturer specified alignment error of ±25 nanometers.[17] In addition, the inter-layer alignment in e-beam lithography is also limited by the planarization of the substrate and design of the alignment keys. These limitations make it often challenging to reliably fabricate nanodevices from individual nanostructures with alignment accuracy better than 50 nm using direct e-beam lithography. Alternatively, several methods have been demonstrated for placing the nanostructures on the exact position using assembly approaches that exploiting electrical field,[18,19] magnetic field,[20] microfluids,[21,22] selective growth,[23] surface functionalization,[24,25] or template technologies.[26,27] These assembling methods represent interesting advancements in nanotechnology. They are, however, often limited to a certain specific nanostructures in each case, and sometimes have limited yield.

Here, we report a general nano-patterning method for self-aligned nanolithography within the nanogap between two electrodes. The method can be used to precisely integrate functional nanostructures with contacting nanoscale electrodes. In this method, field emission between two opposite electrodes of a nanogap is used to expose the polymethylmethacrylated (PMMA) resist within the nanogap region. A self-aligned via hole pattern forms in the nanogap area after the exposure process, with the diameter of the via hole controllable by varying the nanogap width. This self-aligned nanolithography essentially have zero alignment error, and can be used to deposit functional nanostructures into the nano via hole aligned exactly with the metal electrodes. To demonstrate its potential for nanoelectronic device fabrication, this approach is used to form electrode-island-electrode tunneling junction devices by controlled deposition of nanostructures in exposed area.

The key concept here is to selectively remove the polymer resist materials in the nanogap. A wide range of approaches have been reported for high resolution patterning polymer resists in the past decades.[28,29] One interesting approach is to modify the surface morphology of polymer resists using atomic force microscope electrostatic nanolithography,[30,31] in which a film of polymer resists heated above the glass-transition temperature (Tg) becomes highly unstable with regard to small perturbations. A variety of topological feature, including developable, raised features or ablation of the polymers, can form in this process depending on emission current levels. However, this approach requires an external tip for planar fabrication. In this work, we develop an on-chip self-aligned nanolithography using the metal nanoelectrodes. The via hole patterns spontaneously form by ablating the polymer resists within a nanogap between two nanoelectrodes upon applying a certain bias voltage. We report the exposure features and demonstrate the metal deposition and trapping of nanoparticles in the nanogap for the potential application in nanoelectronic devices.

6.2. Experimental

A schematic for self-aligned local area patterning within the nanogap is illustrated in the Figure 6-1. The first step starts with the metal nanogap which is fabricated by electron beam lithography (Fig. 6-1a).

The nanogaps of different width were directly written by electron beam writer on 600 nm SiO_2 substrate. Titanium (5 nm) and gold (25 nm) metal electrodes were deposited using electron beam evaporation on the patterned samples followed by a lift-off process. The nanogaps are then coated with PMMA resist with the thickness controlled to be comparable to that of metal electrodes (Fig. 6-1b). A DC bias is then applied to the nanogap electrodes to induce current emission across the nanogap and expose PMMA in the nanogap area (Fig. 6-1c) to form a via hole pattern (Fig. 6-1d). The samples are characterized using scanning electron microscope (SEM, JEOL JSM-6700F).

6.3.   Results & Discussion:

6.3.1. SEM images of self-aligned nanogap area patterning

Figure 6-2a shows an SEM image of a typical nanogap used in this study. The width of the gap can be controlled from 20 nm to more than 100 nm using electron beam lithography. Figure 6-2b-d shows the SEM images of via holes of variable sizes (~20, 30, 150 nm) formed in the nanogap area after the exposure process described in Figure 6-1. Figure 6-2e-g shows the arrays of via hole patterns obtained using self-aligned exposure process, demonstrating the high yield of the self-aligned nanolithography process. The via holes have a circular shape with the diameter comparable to the nanogap width. These features are formed after the localized exposure process through direct ablation of PMMA by emission current.[30,31] The current in our exposure process is controlled in the range of 1-10 nA. When current is below this regime, no obvious exposure features can be observed and the PMMA in the exposure area isn't developable either. When the current is much higher, catastrophic breakdown of metal electrode happens. Importantly, the via hole patterns are self-aligned within the nanogap electrodes, opening a new opportunity to precisely place molecular nanostructures within the via holes to bridge the nanogap electrodes and obtain functional molecular nanodevices.

6.3.2. Electrical characteristics and simulation of nanogap structure coated with PMMA

To understand the nanogap junction behavior, the current-voltage (I-V) characteristics of the PMMA coated nanogap are recorded and analyzed for the gap width of 25, 45 and 100 nm (Fig. 6-3a,b). The current across the nanogap increases abruptly upon reaching a certain threshold voltage. The I-V characteristics can be modeled by Fowler-Nordheim (FN) conduction (field emission) mechanism. The FN relation[32-34] can be written as

$$I_{FN}=1.54*10^{-6}\alpha S\ (\beta^2 V^2/\varphi d^2) * exp[-6.87 * 10^9(\varphi^{3/2}d/\beta V)]$$

The effective electric field E* and current density J* are given by E*=βV/d, J*=I/αS, where S is the cross-sectional area of the electrodes, φ is work function of the emitter, α is area factor and β is field enhancement factor which is greater than one (e.g., the parallel-plate in the vacuum β~1). The FN plot (ln(I/V^2) v.s. 1/V) and the linear fit (Fig. 6-3b) show that FN conduction can be used to effectively interpret the I-V characteristics in the nanogap junction. The insert in Figure 6-3b shows the correlation of ln(I/V^2)/d and 1/V, in which the slope is inversely proportional to the field enhancement factor β in the FN relation. The field enhancement factor for 25, 45 and 100 nm nanogap is 40, 42 and 24 respectively. These values of field enhancement factor in the nanogap structure are comparable to those reported previously (β =12-100 for 70 nm and 90 nm gap).[32] The smaller value for 100-nm-gap may be attributed to the difference in emitter shape since field enhancement factor strongly depends on the shape of the emitter.[34] To further understand the field strength and spatial distribution in the nanogap, the finite element method is used to simulate the electric field distribution in the nanogap area (Fig. 6-3c). The DC bias resulted in 1 nA current is taken as the potential difference in the 100 nm nanogap width. The maximum field strength in the gap is around 10^9 V/m, and the field strength is 5x10^8 V/m in the centre region. The extreme electric field estimated within the polymer is on the same order of magnitude as the intrinsic dielectric strength of PMMA (10^9 V/m).[35] In addition, the dark line in the Figure 6-3c shows the current flow path. The maximum field strength is at the corner of the electrodes

where electrons are easy to emit due to sharp corners. These analyses are consistent with the round shape via-hole patterns observed in our nanogap structure (Fig. 6-2b-d).

The ability to fabricate nanoscale via holes that are self-aligned with the nanogaps opens many exciting opportunities for nanodevice engineering. The self-aligned nanolithography approach can be used to deposit a variety of functional nanostructures that are precisely aligned with the nanogap electrodes. As an example, we have explored the exposed nanogap to deposit the metal or trap the gold nanoparticles to form electrode-island-electrode tunneling junction structures. Using the self-aligned via nanohole patterns in PMMA as template, nanodots can be directly created in the nanohole through a vacuum metal deposition and lift-off process. Figure 6-4a shows an array of the electrode-dot-electrode device obtained in this way. A magnified image of a single device is shown in Figure 6-4b. In order to create a tunneling barrier between the nanogap electrodes and nanodot, a 2-nm silicon oxide was deposited prior to metal deposition. Current-voltage measurement of such device shows typical tunneling behavior, demonstrating that the 2-nm oxide can effectively work as the tunneling barrier to insolate the electrodes and metal dots.

6.3.3. Self-aligned vial holes as template for nanoparticle deposition obtain electrode-island-electrode tunneling device

Additionally, the self-aligned vial nanohole patterns can also be used to deposit colloid nanoparticles in the nanogap through a solution assembly process. To this end, the silicon oxide surface of exposed vial hole patterns was first modified with with 3-ainopropyl-trimethoxysilane (APTES) to terminate SiO_2 substrate with -NH_2 group.[21] The partial positive charge of -NH_2 group can facilitate the absorption of Au nanoparticles (with negative surface charges) in the vial holes. A drop of gold nanoparticle solution was then placed on the chip to allow the gold nanoparticles to settle down and attached to the surface by electrostatic force. The sample was lastly rinsed with acetone to remove the PMMA and extra gold particles on PMMA, leaving gold nanoparticles only in the exposed gap area to form a clean electrode-island-electrode tunnel junction (Fig. 6-4d,e). Our studies show that the gold

nanoparticles can be readily deposited into the via hole pattern in this fashion. Single or a few nanoplarticles can be trapped in the nanogap, depending on the relative size of nanoparticles and via holes. The current-voltage characteristic of a single gold nanoparticle trapped in the gap shows typical electrons tunneling behavior at room temperature (Fig. 6-4f). These studies demonstrate the self-aligned nanolithography approach can be readily used to fabricate clean nanoelectronic devices.

6.4. Conclusions:

In conclusion, we have developed a reliable approach to create nanoscale via holes that are self-aligned with the gap electrodes. The via hole patterns spontaneously form by ablating the polymer resists within a nanogap between two nanoelectrodes upon applying a certain bias voltage. The diameter of the exposure patterns can be controlled to have comparable dimension of nanogap width. Single or arrays of via holes have been demonstrated with variable diameters from 20 nm to over 100 nm..The exposed features can be used to deposit functional nanostructures in the nanogap for nanodevice engineering.

6.5. References

1. Goldhaber-Gordon, D.; Montemerlo, M. S.; Love, J. C.; Opiteck, G. J.; Ellenbogen, J. C. *Proc. IEEE* **1997**, *85*, 521-540.

2. Lieber,C.M. *Sci. Am.* **2001**, 285, 50-56.

3. Heath, J. R.; Ratner, M. A. *Phys. Today* **2003**, *5*, 43-49.

4. Wang, Z. L.; Song, J. H. *Science* **2006**, *312*, 242-246.

5. Lin, Y. C.; Lu, K. C.; Wu, W. W.; Bai, J-W.;Chen, L. J.; Tu, K. N.; Huang, Y. *Nano Lett.* **2008**, *8*, 913-918.

6. Xia, Y. N.; Yang, P. D.; Sun, Y. G.; Wu, Y. Y.; Mayers, B.; Gates, B.; Yin, Y. D.; Kim, F.; Yan, Y. Q. *Adv. Mater.* **2003**, *15*, 354-389.

7. Bumm, L. A.; Arnold, J. J.; Cygan, M. T.; Dunbar, T. D.; Burgin, T. P.; Jones, L.; Allara, D. L.; Tour, J. M.; Weiss, P. S. *Science* **1996**, *275*, 1705-1707.

8. Donhauser, Z. J.; Mantooth, B. A.; Kelly, K. F.; Bumm, L. A.; Monnell, J. D.; Stapleton, J. J.; Price, D. W.; Rawlett, A. M.; Allara, D. L.; Tour, J. M.; Weiss, P. S. *Science* **2001**, *292,* 2303-2307.

9. Cui, X. D.; Primak, A.; Zarate, X.; Tomfohr, J.; Sankey, O. F.; Moore, A. L.; Moore, T. A.; Gust, D.; Harris, G.; Lindsay, S. M. *Science* **2001**, *294*, 571-574.

10. Liu, S. H.; Tok, J. B. H.; Bao, Z. *Nano Lett.* **2005**, *5*, 1071-1076.

11. Mahapatro, A. K.; Ying, J. W.; Ren, T.; Janes, D. B. *Nano Lett.* **2008**, *8*, 2131-2136.

12. Ray, V.; Subramanian, R.; Bhadrachalam, P.; Ma, L. C.; Kim, C. U.; Koh, S. J. *Nature Nanotechnology* **2008**, *3*, 603-608.

13. Negishi, R.; Hasegawa, T.; Terabe, K.; Aono, M.; Tanaka, H.; Ogawa, T.; Ozawa, H. *Appl. Phys. Lett.* **2007**, *90*, 223112.

14. Klein, D. L.; Roth, R.; Lim, A. K. L.; Alivisatos, A. P.; McEuen, P. L. *Nature* **1997**, *389*, 699-701.

15. Hoshino, K.; Yamada, K.; Matsumoto, K.; Shimoyama, I. *J. Micromech. Microeng.* **2006**, *16*, 1285–1289.

16. Fiore, A.; Chen, J. X.; Ilegems, M. *Appl. Phys. Lett.* **2002***, 81*, 1756-1758.

17. Leica VB6 HR and Jeol JBX 9300 FS EBL Equipment Capability.

18. Smith, P. A.; Nordquist, C. D.; Jackson, T. N.; Mayer, T. S.; Martin, B. R.; Mbindyo, J.; Mallouk, T. E. *Appl. Phys. Lett.* **2000**, *77*, 1399-1401.

19. Ma, L. H.; Subramanian, R.; Huang, H. W. ; Ray, V.; Kim, C. U.; Koh, S. J. *Nano Lett.*, **2007**, 7, 439-445.

20. Tanase, M.; Bauer, L. A.; Hultgren, A.; Silevitch, D. M.; Sun, L.; Reich, D. H.; Searson, P. C.; Meyer, G. J. *Nano Lett.* **2001**, 155-158.

21. Huang, Y.; Duan, X.; Wei, Q.; Lieber, C. M. *Science* **2001**, *291*, 630-633.

22. Tsukruk, V. V.; Ko, H.; Peleshanko, S. *Phys. Rev. Lett.* **2004**, 92, 065502.

23. Wang, X.; Summers, C. J.; Wang, Z. L. *Nano Letters*, **2004**, 4, 423-426.

24. Rao, S. G.; Huang, L.; Setyawan, W.; Hong, S. H. *Nature* **2003**, 425, 36-37.

25. Kumagai, S.; Yoshii, S.; Yamada, K.; Matsukawa, N.; Fujiwara, I.; Iwahori, K.; Yamashita, I. *Appl. Phys. Lett.* **2006**, 88, 153103.

26. Zheng, J. W.; Constantinou, P. E.; Micheel, C.; Alivisatos, A. P.; Kiehl, R. A.; Seeman, N. C. *Nano Lett.* **2006**, 6, 1502-1504.

27. Warner, M. G.; Hutchison, J. E. *Nat. Mater.* **2003**, 2, 272-277.

28. Majumdar, A.; Oden, P. I.;Carrejo, J. P.; Nagahara, L. A.; Graham, J. J.; Alexander, J. *Appl. Phys. Lett.* **1992**, *61*, 2293-2295.

29. Lercel, M. J.; Craighead, H. G.; Parikh, A. N.; Seshadri, K.; Allara, D. L. *Appl. Phys. Lett.* **1996**, *68*, 1504-1506.

30. Lyuksyutov, S. F.; Paramonov, P. B.; Sharipov, R. A.; Sigalov, G. *Phys. Rev. B.* **2004**, *70*, 174110.

31. Lyuksyutov, S. F.;Vaia, R. A.; Paramonov, P. B.; Juhl, S.; Waterhouse, L.; Ralich, R. M.; Sigalov, G.; Sancaktar, E. *Nature Materials* **2003**, *2*, 468-472.

32. Bhattacharjee, S.; Vartak, A.; Mukherjee, V. *Appl. Phys. Lett.* **2008**, *92*, 191503.

33. Fowler, R. H.; Nordheim, L. *Proc. R. Soc. London. Ser. A.* **1928**, *119*. 173.

34. Hunt, C. E.; Trujillo, J. T.; Orvis, W. J. *IEEE Trans. Electron Devices* **1991**, *38*, 2309-2313.

35. Kroschwitz, J. I. *Electrical and Electronic Properties of Polymers: A State-of-the-Art Compendium*, John Wiley & Sons.: New York **1998**, 116–119.

36. Osswald, T. A.; Menges, G. *Material Science of Polymers for Engineers*, Hansen & Gardner.: New York, **1996**, 384–403.
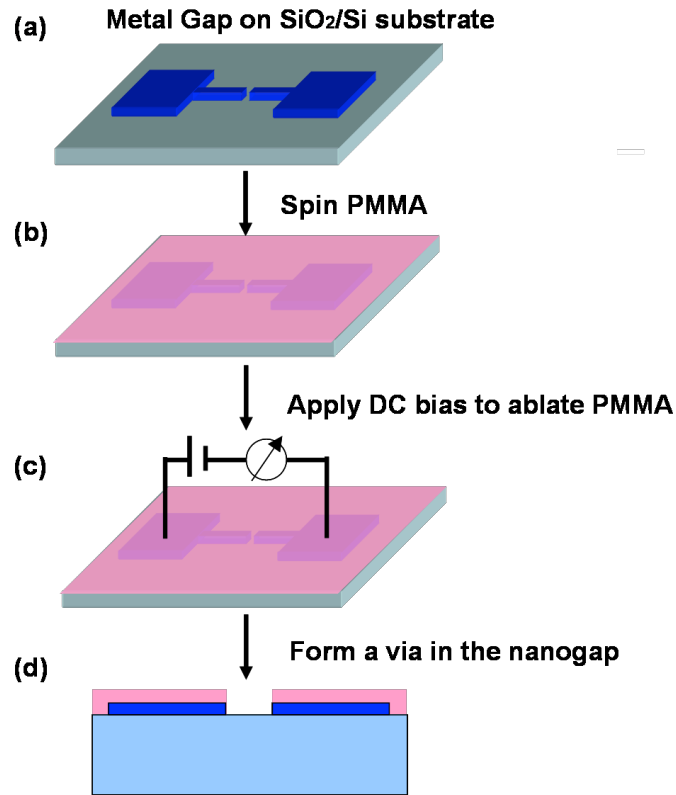
6.6. List of figures

Figure 6-1. Schematic of self-aligned nanolithography in a nanogap. (a) Fabrication of a nanogap with two opposite electrodes (Ti/Au 5-nm/25-nm) on SiO$_2$/Si substrate. (b) Spin coating of PMMA resist (30 nm). (c) Apply DC bias to the nanogap electrodes coated by PMMA to ablate the PMMA in the nanogap area. (d) Formation of a via hole pattern in the nanogap area. The bias voltage is applied to control the current in ablating process around 1-10 nA and time duration is typically 1 Sec.
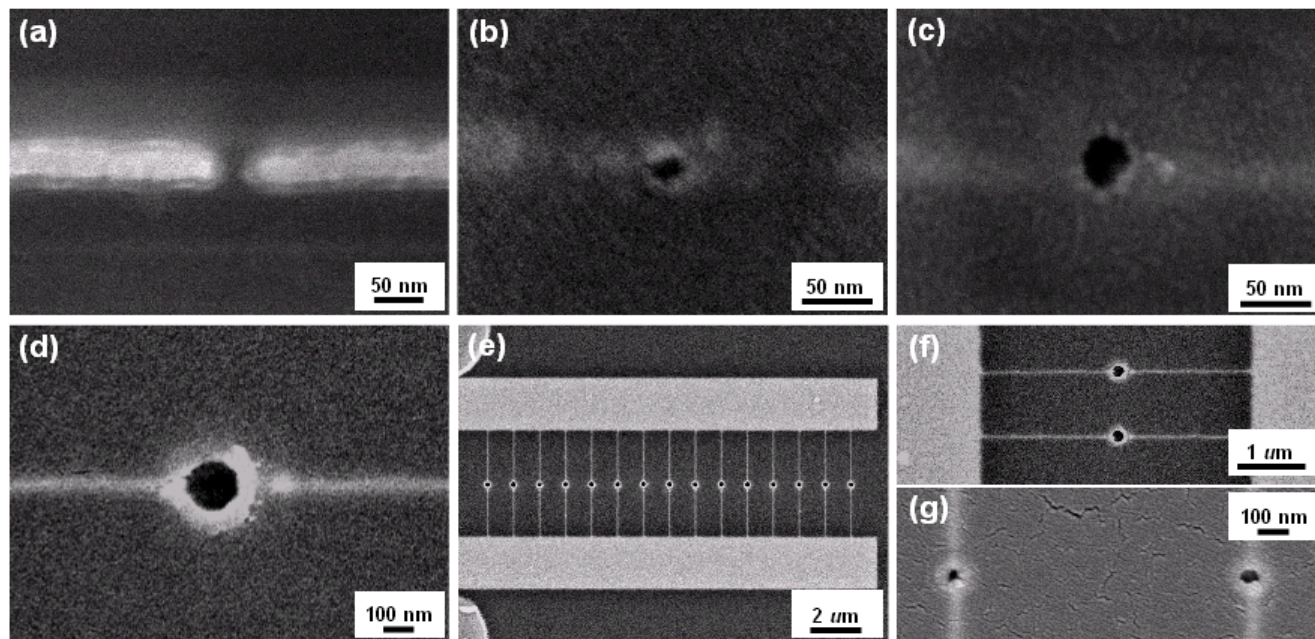
Figure 6-2. SEM images of self-aligned nanogap area patterning. (a) SEM image of a pair of typical nanogap electrodes. (b, c, d) SEM images of exposed via hole patterns of variable diameters from different electrode gap width coated with PMMA. The patterned via hole diameters are 21 nm (b), 33 nm (c), 150 nm (d), respectively. (e) An array of 15 via hole patterns. The average diameter is 110 nm. (f) Enlarged image of (e). (g) Two pairs of 50 nm via hole patterns. The average exposure current of the single pair is ~1-10 nA.
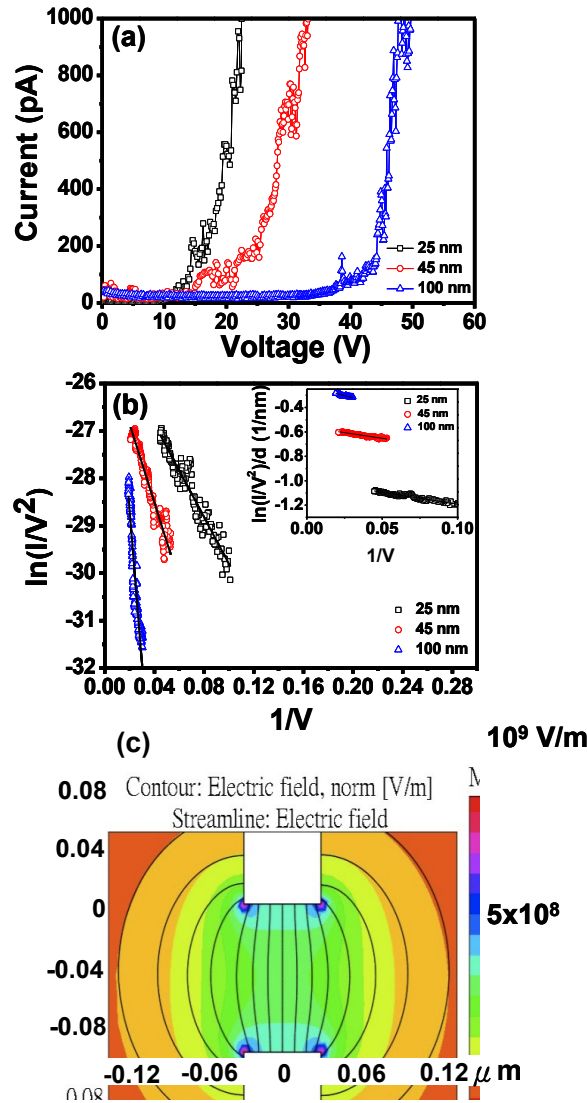
Figure 6-3. Electrical characteristics of nanogap structure coated with PMMA. (a) I-V characteristics of three different nanogap width, 25 nm, 45 nm and 100 nm, respectively. (b) FN plot for the 25, 45 and 100 nm nanogaps. Voltage is measured in volts and current is measured in ampere. The insert shows the $\ln(I/V^2)/d$ v.s. $1/V$. The slope is inversely proportional to the field enhancement factor β. ($E = \beta V/d$ is defined in the FN relation). (c) The electrical strength simulation result of the nanogap: the gap width is 100 nm and electrode width is 60 nm. The dielectric constant ε_r of PMMA is around 3.[36] The spatial distribution of the field strength id is represented in color scale, and the dark lines (streamline) represent the direction of the electric field.
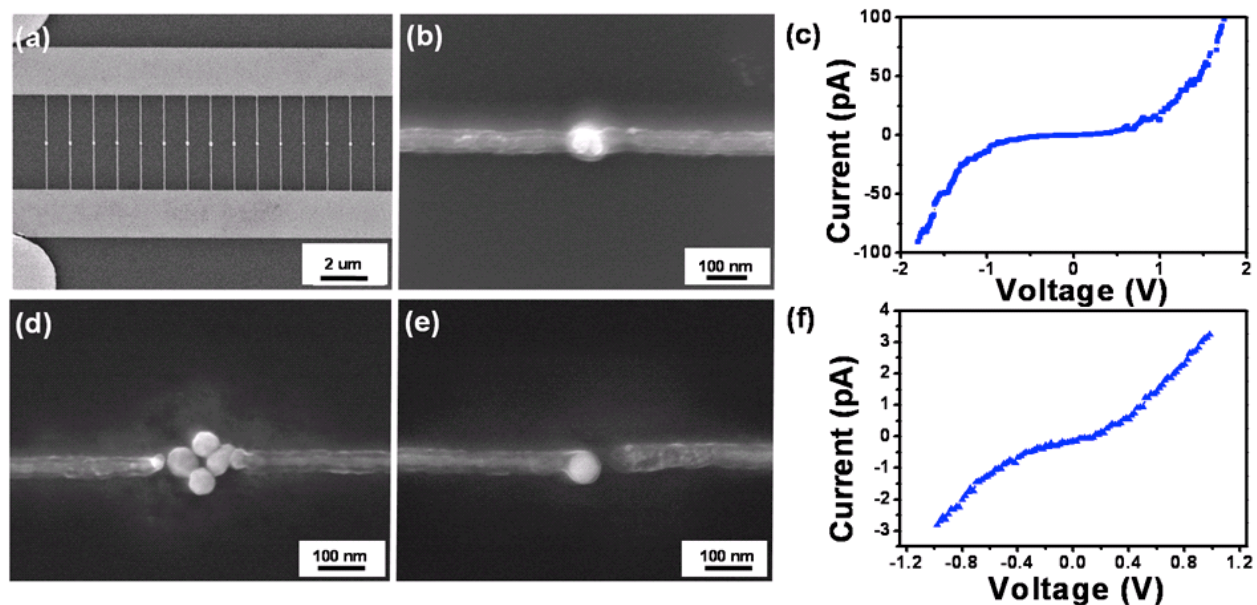
Figure 6-4. Self-aligned vial holes as template for nanoparticle deposition obtain electrode-island-electrode tunneling device. (a) An array of metal dot deposited in the nanogap using vacuum metal deposition followed by a lift-off process. (b) SEM image of a single device. (c) I-V characteristic of the electrode-dot-electrode device obtained this way. (d) SEM image of few gold nanoparticles trapped in the nanogap. (The diameter Au particle is around 60 nm) (e) SEM image of a single gold nanoparticle trapped in the nanogap. (f) I-V characteristic of single particle trapped in the nanogap.

Chapter 7: Summary

Nanoscale metal silicides have garnered significant interest during the past few years. The fact that silicides can form a clean, flat and sharp single crystal epitaxial interface with Si NWs through solid state reaction mechanism especially gained them fame for their superior function as the perfect contact material for Si NW based devices. Within this framework, various silicide/Si/silicide heterostructures have been fabricated through lateral diffusion of metal atoms from the metal contacts into Si NWs and the subsequence transformation of Si to silicides. Exploring this structure, high performance p-MOSFET has been demonstrated with intrinsic Si NWs with high work function PtSi contact, spin transport has been detected in the MnSi/p-Si/MnSi heterostructures. These works demonstrate the bright future lying ahead for nanosilicide technology, as well as raise the need for better understanding and control of the silicide formation at nanoscale. Therefore, we demonstrate a control method for the single-crystal silicide growth with the aid of oxide shell. Due to the compressive stress exerted on the silicide or germanide by the oxide shell, the nucleation rate of silicide or germanide materials will decrease. Thus, few nuclei growth leads to the single-crystal grain growth.

To date, studies on the diffusion and phase transformation processes of silicides in Si NWs have indicated possible deviations from the well-established silicide formation techniques in bulk and the thin film system. Although a few mechanisms have been proposed, a systematic understanding is not yet available to explain all observed experimental results. While advances in Si NW device applications is much desired, systematic study and rational control of the grow kinetics of nanosilicides is equally important.