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Envelope Amplifier Design for Wireless Base-Station Power Amplifiers

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Chin Hsia

Committee in charge:

Professor Peter M. Asbeck, Chair
Professor Prabhakar Bandaru
Professor William Griswold
Professor Lawrence E. Larson
Professor Paul Yu

2010

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The dissertation of Chin Hsia is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2010

DEDICATION

To my parents, my family
for their endless love and support

EPIGRAPH

The Tao can be explained, but not in a normal way

— Laozi

TABLE OF CONTENTS

Signature Page iii

Dedication iv

Epigraph v

Table of Contents vi

List of Figures ix

List of Tables xiv

Acknowledgements xv

Vita xvii

Abstract of the Dissertation xx

Chapter 1 Introduction 1

1.1 Base Station Power Amplifiers 1

1.2 High Efficiency Techniques for Non-Constant Envelope Signals 5

1.2.1 Doherty Power Amplifier 5

1.2.2 LINC Power Amplifier 7

1.2.3 EER Power Amplifier 7

1.2.4 ET Power Amplifier 9

1.3 Scope of Dissertation 10

Chapter 2 Envelope Tracking Power Amplifier 12

2.1 Introduction 12
2.2 Envelope Tracking Techniques 12
2.3 ET Power Amplifier Efficiency 15
2.4 Envelope Amplifier Architecture 17
2.5 Envelope Amplifier Modeling 18
2.6 Envelope Amplifier Efficiency 27
2.7 Summary 38
2.8 Acknowledgements 40

Chapter 3 Envelope Amplifier Design for High Voltage Applications 41
3.1 Introduction 41
3.2 Design Issues for High Voltage Envelope Amplifier 42
3.3 High Voltage Envelope Amplifier Design 44
3.3.1 Wideband High Voltage Op-Amp Design and Implementation 47
3.3.2 Wideband High Voltage Linear Stage 64
3.3.3 Wideband High Voltage Sensor Stage 66
3.3.4 High Voltage Switcher Stage 70
3.4 High Voltage ET PA Experimental Results 74
3.4.1 High Voltage Envelope Amplifier Measurement . . . 74
3.4.2 High Voltage Envelope Tracking Power Amplifier Measurement 76
3.5 Summary 81
3.6 Acknowledgements 84

Chapter 4 Dual-switcher Envelope Amplifier 85
4.1 Introduction 85

4.2 DSP Switcher Control 86
4.3 Dual-switcher Envelope Amplifier 93
4.3.1 Dual-switcher Envelope Amplifier Architecture . . . 93
4.3.2 Dual-switcher Design Synthesis 95
4.3.3 Experimental results 99
4.4 Envelope Tracking Power Amplifier Measurement 106
4.5 Summary 114
4.6 Acknowledgements 116

Chapter 5 Conclusion and Future work 117
5.1 Dissertation Summary 117
5.2 Future Work 119
5.2.1 Envelope Tracking System Modeling 119
5.2.2 Fully Integrated High Voltage Linear Stage 119
5.2.3 A Multi-switcher Envelope Amplifier with Closed-loop Control 120
5.2.4 Hybrid Envelope Amplifier Architecture for Other Applications 120

References 122

LIST OF FIGURES

Figure 1.1: Single Carrier Combined Power Amplifier [1] 3

Figure 1.2: Multiple Carrier Power Amplifier Architecture [2] 4

Figure 1.3: Multiple Carrier RF signal 5

Figure 1.4: Doherty Power Amplifier [3] 6

Figure 1.5: LINC Power Amplifier [1] 7

Figure 1.6: Envelope Elimination and Restoration (EER) PA [4] 8

Figure 1.7: Envelope Tracking (ET) PA [5, 6] 9

Figure 2.1: Envelope Tracking System [6] 14

Figure 2.2: W-CDMA Envelope Signal Power Spectrum Before and After Detroughing and Decresting 14

Figure 2.3: Comparison of Simulated Efficiency versus Output Power between Class B Power Amplifier and Class B with Ideal ET Operation . . . 17

Figure 2.4: Envelope Amplifier Architecture [6] 19

Figure 2.5: W-CDMA Envelope Signal Characteristics 19

Figure 2.6: Envelope Amplifier Matlab/Simulink Model: (a) System Block Diagram (b) Implementation in Simulink 21

Figure 2.7: EDGE signal: (a) IF signal (b) Envelope signal. 22

Figure 2.8: Envelope Amplifier Running EDGE Signal: (a) Simulation (b) Simulation (c) Experimental results (Ch1,Ch4: 10 mV = 100 mA) (d) Switching Frequency Distribution comparison. 24

Figure 2.9: Envelope Amplifier Running WCDMA Signal: (a) Simulation (b) Simulation (c) Experimental results (Ch1,Ch4: 10 mV = 100 mA) (d) Switching Frequency Distribution Comparison. 26

Figure 2.10: Envelope Amplifier Start-up Condition: (a) EDGE signal (b) W-CDMA signal. 28

Figure 2.11: (a) Switcher Stage Schematic; (b) High Side switch-FET Gate Charge Diagram [7] 31

Figure 2.12: Envelope Amplifier Loss Estimation: (a) EDGE signal (3.2 dB PAR) (b) W-CDMA signal (7.7 dB PAR) 36

Figure 2.13: Envelope Amplifier Hybrid PCB Design [6, 8, 9] 38

Figure 2.14: Simulated and Measured Performance Comparisons of the Envelope Amplifier using W-CDMA signals (a) Efficiency; (b) Power loss 39

Figure 2.15: Measured Efficiency versus PAR of the Envelope Signals 40

Figure 3.1: High Voltage Envelope Amplifier Schematic 43

Figure 3.2: High Voltage Envelope Amplifier Simulation 44

Figure 3.3: High Voltage OTA Toptology: (a) Folded-cascode Input Stage (b) Source Cross-coupled Differential Pairs. 48

Figure 3.4: High Voltage OTA Cross-couple Input Stage 52

Figure 3.5: High Voltage OTA Driver and Output Stage 53

Figure 3.6: High Voltage OTA Full Schematic 54

Figure 3.7: High Voltage OTA Loop Gain 56

Figure 3.8: High Voltage OTA Frequency Response 57

Figure 3.9: High Voltage OTA Transient Step Simulation 59

Figure 3.10: High Voltage OTA Transient Simulation using a 7.7 dB PAR W-CDMA Signal 60

Figure 3.11: High Voltage OTA Transient Simulation Input/Output Comparisons 61

Figure 3.12: High Voltage OTA Layout 61

Figure 3.13: High Voltage OTA Package and Test Fixture 62

Figure 3.14: High Voltage OTA Transient Step Measurement 63

Figure 3.15: High Voltage OTA Frequency Response: Measurement versus Simulation 65

Figure 3.16: High Voltage Linear Stage Schematic 66

Figure 3.17: Measured High Voltage Linear Stage Frequency Response 67

Figure 3.18: High Voltage Current-sense Stage Schematic 68

Figure 3.19: Simulated High Voltage Current-sense Stage Differential Gain . . . 69

Figure 3.20: Simulated High Voltage Current-sense Stage CMRR 69

Figure 3.21: Measured High Voltage Current-sense Stage Performance 70

Figure 3.22: High Voltage Switcher Full Schematic 73

Figure 3.23: Measured High Voltage Switcher Efficiency and Power Loss 74

Figure 3.24: High Voltage Envelope Amplifier 75

Figure 3.25: High Voltage Envelope Amplifier Output versus Input Signal Spectrum (W-CDMA) 76

Figure 3.26: High Voltage Envelope Amplifier with W-CDMA signal: (a) Measurement; (b) Simulation results 77

Figure 3.27: High Voltage Envelope Amplifier Switching Frequency Distribution 78

Figure 3.28: Eudyna EGN21A090IV-A Power Amplifier Test Fixture [10] 79

Figure 3.29: Envelope Tracking Power Amplifier Instantaneous Efficiency Measurement Setup [6] 81

Figure 3.30: Envelope Tracking RF Power Amplifier Performance Comparison: (a) 30 V peak Envelope Tracking [10], (b) 45 V peak Envelope Tracking; Test Signal: W-CDMA 7.7 dB PAR 82

Figure 4.1: Simulated Envelope Amplifier Behaviors with 1.3 μH Inductor: (a) Hysteresis: 0.025 V, (b) Hysteresis: 0.5 V; Test Signal: W-CDMA 7.7 dB PAR; Peak Envelope: 30 V; Load: 5 ohm 88

Figure 4.2: Simulated Envelope Amplifier Behaviors with 1.3 μH Inductor and Switcher Control Delay Adjustment 90

Figure 4.3: (a) Simulated Overall Linear Stage Power Consumption and (b) Average Switching Frequency versus Switcher Control Signal Delay Adjustment for Different Output Power with using 1.3 μH Inductor in the Switcher 91

Figure 4.4: Digital Signal Generation for Switcher Control 92

Figure 4.5: Simulated DC Current Imbalance at the Output of Envelope Amplifier 93

Figure 4.6: Dual-switcher Envelope Amplifier Schematic 94

Figure 4.7: Simulated Dual-switcher Envelope Amplifier Behaviors with 1.3 μH and 25 μH Inductor for the Switchers, respectively 95

Figure 4.8: Normalized Linear Stage Power Consumption of the Envelope Amplifier versus Hysteresis Value 97

Figure 4.9: (a) Main Switcher Average Switching Frequency, and (b) Auxiliary Switcher Average Switching Frequency versus Hysteresis Value . . 98

Figure 4.10: (a) Normalized Linear Stage Power Consumption of the Envelope Amplifier, (b) The Main Switcher Average Switching Frequency, versus Inductance Value 100

Figure 4.11: Dual-switcher Envelope Amplifier Hybrid Integration on PCB . . . 101

Figure 4.12: Measured Switcher Power Loss and Efficiency Performance versus Switching Frequency 102

Figure 4.13: Recorded Waveform of Dual-switcher Envelope Amplifier Before Delay Adjustment (a) Simulation, (b) Measurement (Ch1,Ch4: 10 mV = 100 mA) 103

Figure 4.14: Recorded Waveform of Dual-switcher Envelope Amplifier After Delay Adjustment (a) Simulation, (b) Measurement (Ch1,Ch4: 10 mV = 100 mA) 104

Figure 4.15: Measured Switching Frequency Distributions between Different Switcher Stages 105

Figure 4.16: Efficiency Measurement and Comparisons between Two Envelope Amplifiers 106

Figure 4.17: TriQuint Gen 1 GaAs HVHBT RF Device [9, 11] 108

Figure 4.18: TrQiuint Gen 1 GaAs HVHBT RF Power Amplifier Test Fixture Schematic [9] 108

Figure 4.19: TriQuint Gen 2 GaAs HVHBT RF Power Amplifier Test Fixture [12] 109

Figure 4.20: TriQuint Gen 1 GaAs HVHBT RF Device CW Measurement [9] . . 109

Figure 4.21: TriQuint Gen 2 GaAs HVHBT RF Device Pulse CW Measurement [13] :(a) Collector Efficiency, (b) Power Gain, versus Collector Voltage 110

Figure 4.22: Measured: (a) AM-AM, (b) AM-PM Performance Before Predistortion [13] 112

Figure 4.23: Measured: (a) AM-AM, (b) AM-PM Performance After Predistortion [13] 113

Figure 4.24: Normalized Output Spectrum of ET Power Amplifier Before and After DPD using TriQuint Gen 2 GaAs HVHBT RF Device 114

LIST OF TABLES

Table 1.1: Power Amplifier Power Range and its Applications 2

Table 2.1: Envelope Amplifier Simulation and Measurement comparisons (30 V Envelope Amplifier) 37

Table 3.1: High Voltage Envelope Amplifier Specifications 44

Table 3.2: OP-amp and Key Parameters for the Linear Stage 45

Table 3.3: Difference Amplifier and Key Parameters for the Current-sense Stage 46

Table 3.4: High Voltage OTA Specifications 47

Table 3.5: Device Performance in STMicroelectronics BCD Process 49

Table 3.6: Summary of High Voltage OTA Simulation Results 50

Table 3.7: Summary of high voltage OTA measurement results 58

Table 3.8: Tabulated Switch-FET Candidates for High Voltage Switcher Stage . 72

Table 3.9: Tabulated Schottky Diode Candidates for High Voltage Switcher Stage 73

Table 3.10: Summary of High Voltage Envelope Amplifier Performance 75

Table 3.11: Summary of EGN21A090IV/-A Constant Drain Measurement Results 78

Table 3.12: Summarized Measurement Results of the Two Envelope Tracking Power Amplifiers with Single Carrier W-CDMA Signal Before and After Memory-less Digital Pre-distortion 83

Table 4.1: Summarized simulated peak current distribution of envelope amplifiers with single and dual switcher stages using W-CDMA signal . . 96

Table 4.2: Summarized Performance of Power Amplifier with Single Carrier W-CDMA and WiMAX Signal Before and After Digital Pre-distortion, MM: Memory mitigation 115

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ABSTRACT OF THE DISSERTATION

Envelope Amplifier Design for Wireless Base-Station Power Amplifiers

by

Chin Hsia

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2010

Professor Peter M. Asbeck, Chair

In order to deliver high data rates, modern wireless communication systems transmit complex modulated signals with high peak-to-average ratio, which demands wide bandwidth and stringent linearity performance for power amplifiers. To satisfy spectral mask regulations and achieve adequate error vector magnitude, power amplifiers typically operate at 6 to 10 dB back-off from the maximum output power, leading to low efficiency. To overcome the low efficiency problem, the envelope tracking power amplifier architecture has been proposed for this type of application due to its feature of high efficiency over a wide power range.

The overall efficiency of an envelope tracking system relies not only on performance of the RF power amplifier but also on that of an envelope amplifier that provides a dynamically varying power supply voltage. This dissertation focuses on envelope amplifier design for efficiency enhancement of envelope tracking power amplifiers. First,

the envelope tracking power amplifier architecture is analyzed, and the efficiency of a RF transistor in the envelope tracking technique is described. Then envelope amplifier behavior is investigated and a general purpose simulator is developed for analyzing and designing an envelope amplifier. Power loss and efficiency of the envelope amplifier is analyzed and compared with experimental results.

The design of envelope amplifiers for high voltage (> 30 V) envelope tracking applications is described. A high voltage envelope amplifier is designed, implemented and verified. The overall envelope tracking system employing a GaN-HEMT RF transistor is demonstrated.

Finally, a new architecture is developed for the efficiency enhancement of envelope amplifiers, using a digitally assisted controller design. Digital control is utilized to mitigate delay in the control loop inside the envelope amplifier, leading to lower overall power dissipation. A novel envelope amplifier architecture with dual-switcher stages based on the digitally-assisted control strategy is proposed, designed and implemented. The strategy is demonstrated to improve the efficiency of envelope amplifier as well as the system overall efficiency. The resulting performance of envelope tracking system employing a GaAs high voltage HBT with a single carrier W-CDMA input demonstrated state-of-the-art efficiency with good linearity performance.

Chapter 1

Introduction

Today's base-station transmitters require highly linear amplifiers to transmit complex modulation signals in order to provide wireless services with high throughput and large capacity. The design of power amplifiers therefore needs special attention to the amplifier output, which usually contains non-ideal spurious signals. In order to provide cost-effective and high performance solutions, a variety of architectures have emerged for the design of power amplifier for base station applications [3, 14]. In the following, a brief review is conducted of base station power amplifier architectures and design considerations for current and future wireless applications.

1.1 Base Station Power Amplifiers

Table 1.1 categorizes power amplifiers and associated applications based on different power ranges. For cellular base station applications, the average output power is between 10 to 100 W. Two different power amplifier architectures are widely used in this power range. One is single-carrier-combined (SCC) architecture shown in Fig. 1.1, which consists of multiple, low or medium power amplifiers [1]. In this architecture,

single-carrier modulated signals are generated in baseband separately and combined together at the output of each power amplifier. The advantages of implementing a SCC base station amplifier include ease of manufacture, high yields and suitability for mass-production [2]. However, the outputs of multiple single-carrier power amplifiers are combined passively with frequency-selective combiners of very exacting design, which introduces losses and reduces overall efficiency. Furthermore, each individual amplifier requires linearization to optimize its output power and efficiency, further increasing the system complexity.

Table 1.1: Power Amplifier Power Range and its Applications

PA average power	Applications
$\geq$ 100 W	Digital TV broadcast Radio broadcasting transmitters
10 $\sim$ 100 W	Cellular infrastructure (2G/3G/4G) Mobile TV (DVB-T/H) Military and Public safety
1 $\sim$ 10 W	Micro BTS Military handset
$\leq$ 1 W	Cellular handset Modems Wireless backhaul (LOS)

A multi-carrier power amplifier (MCPA) is another architecture for cellular base station applications. In a modern MCPA shown in Fig. 1.2, the transmitted signals are combined in the digital domain and permits evolutionary technologies such as predistortion [15, 16, 17] and waveshaping to be employed which further reduce manufacturing costs and eliminate analog design complexity [2]. The output is up conversion by employing a RF transmitter and then drives a high power, high linear final stage power amplifier. The power amplifier output does not require a combiner therefore maximally

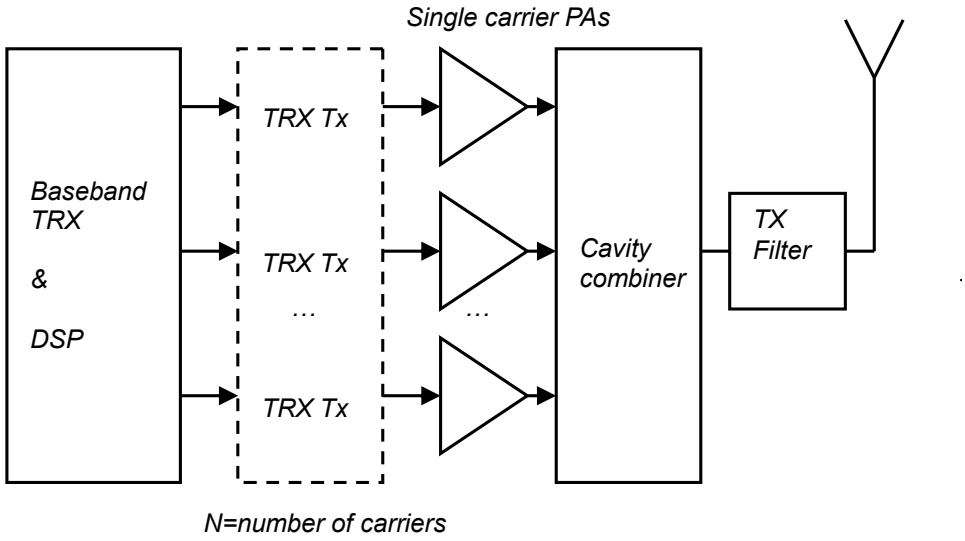


Figure 1.1: Single Carrier Combined Power Amplifier [1]

utilizing the amplifier's performance. MCPA becomes more and more popular now-days due to its capability of handling multi-mode, multi-standard and multi-band signals better than SCC architecture [18].

For designing a base-station power amplifier, the Federal Communication Commission (FCC) standards require the linearity performance beyond the capabilities of conventional class A/AB linear amplifiers. The reason is the amplification of multi-carrier signals yields inter-modulation distortion (IMD) and results in unacceptable spectral regrowth in the adjacent channels. The FCC imposes, therefore, adjacent channel power ratio (ACPR) specifications on multi-carrier communication systems, on the order of -45 to -55 dBc [19]. To ensure the performance meet the specifications, a linearization technique is generally developed for the overall system. Linearization is a systematic procedure for reducing an amplifier's distortion. Linearity improvement of a power amplifier, however, often leads to a trade-off with efficiency. For example, for amplifying

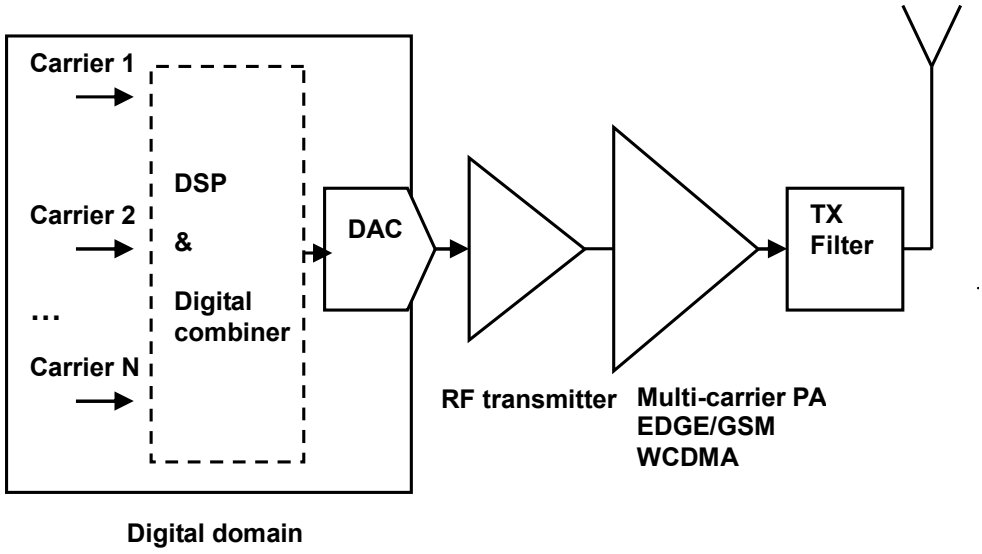


Figure 1.2: Multiple Carrier Power Amplifier Architecture [2]

a multi-carrier non-constant envelope signal shown in Fig. 1.3 with large crest factor (high peak-to-average ratio), backing off the average power can linearize a power amplifier in order to avoid signal clipping at the peak amplitude, which will significantly impacts the linearity. However, the approach usually results in an unacceptable decrease in DC to RF efficiency because the efficiency of power amplifiers generally decreases from the maximum power the amplifier can provide. (1.1) shows the class B amplifier drain/collector efficiency, η_{PA}, as a function of output power [1].

$$\begin{aligned} \eta_{PA} &= \frac{P_{out}(rf)}{P_{DC}} \\ &= \sqrt{\frac{P_{out}(rf)}{P_{max}(rf)}} \cdot \frac{V_{max} - V_{min}}{V_{max} + V_{min}} \cdot \frac{\pi}{4} \end{aligned} \tag{1.1}$$

Where $P_{out}(rf)$ is the average output power, P_{DC} is the DC input power, $P_{max}(rf)$ is the maximum output power, V_{max} is the maximum voltage swing of RF transistor, and V_{min} is the minimum voltage swing of RF transistor. The efficiency drops from its peak

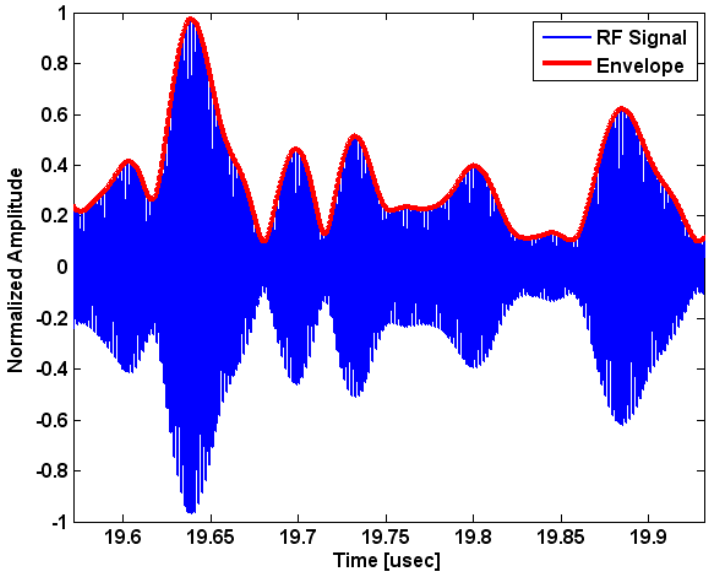


Figure 1.3: Multiple Carrier RF signal

value in a square root manner with output power. Backing off 6 dB output power, for instance, reduces power amplifier's efficiency from the peak to nearly half, which results in a dramatic performance degradation.

In order to preserve the performance of power amplifier running non-constant envelope signals, efficiency enhancement techniques are proposed to improve the average efficiency of power amplifiers, especially at power back-off [14, 20, 21, 22, 23]. A brief review on different topologies is discussed in the next section.

1.2 High Efficiency Techniques for Non-Constant Envelope Signals

1.2.1 Doherty Power Amplifier

Doherty amplifier was proposed by William H. Doherty [24] and was originally employed for high power transmitter using vaccum-tubes. Doherty amplifier uses

"active load pull" techniques to improve efficiency at power back-off. The simplest configuration of a Doherty amplifier is shown in Fig. 1.4, which consists of two amplifiers, the carrier and peak amplifier. The carrier amplifier generally is biased in Class AB, and the peak amplifier biased in Class C. The amplifiers are connected in parallel with the outputs joined by a quarter-wave transmission line, which performs impedance transformation. At low powers, the carrier amplifier is operated with a relatively high load impedance, which allows it to achieve high efficiency. The peak amplifier delivers current as the carrier amplifier saturates; therefore reduces the impedance seen at the output of the carrier amplifier. This maintains high efficiency without hard saturation of the carrier amplifier. Recently, Doherty amplifiers using high power RF devices gradually emerge for wireless base-station applications, especially replaced for low-efficiency linear amplifiers in Feed-forward architectures [20]. There are various types of Doherty circuits demonstrated to extend the high efficiency over a broad power range [3, 11, 25]; however, modulation bandwidth, linearity and adaptability are challenges for Doherty amplifiers towards wide-band, high efficiency base-station applications.

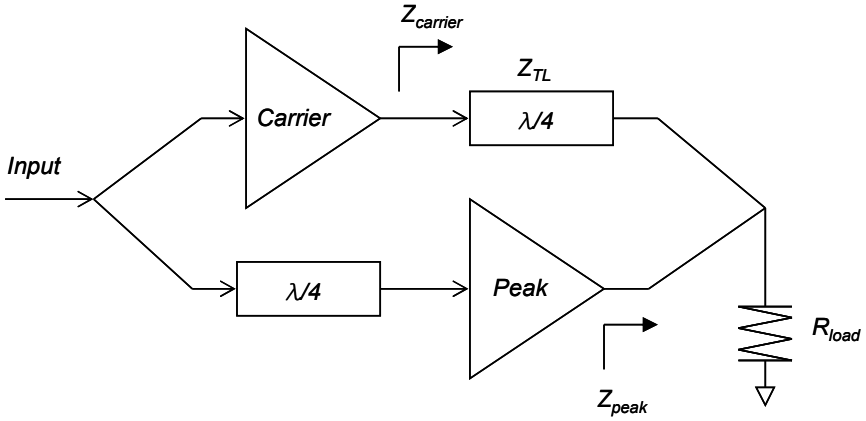


Figure 1.4: Doherty Power Amplifier [3]

1.2.2 LINC Power Amplifier

LINC (Linear Amplification with Nonlinear Components) is another efficiency improvement technique, which employs a combination of high efficiency switch-mode power amplifiers to produce the linear output. In a LINC amplifier system shown in Fig. 1.5, Signal component separator unit generates signals with constant envelope to encode complex signals such that two switch-mode amplifies can be driven by constant envelope signals to maintain high efficiency. This technique has demonstrated over 48% efficiency with good linearity performance in terminal applications [21]. For base-station power amplifier which requires at least 20 W output power, however, system mismatch, power combiner loss, and high switching loss degrade the overall system performance compared to other techniques [26].

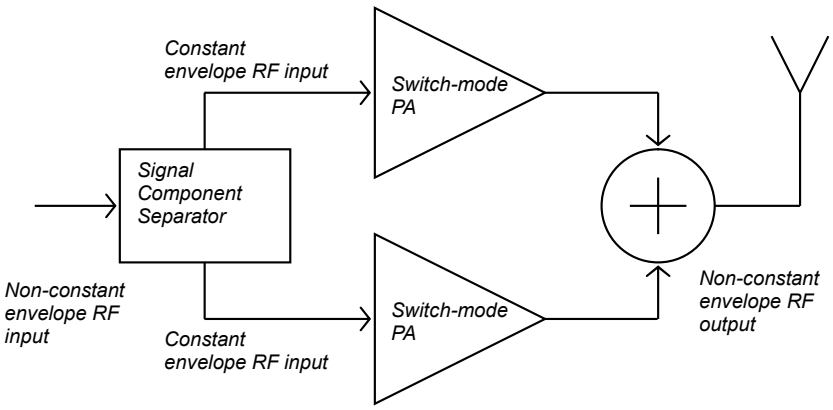


Figure 1.5: LINC Power Amplifier [1]

1.2.3 EER Power Amplifier

Envelope elimination and restoration (EER) was proposed to linearize a power amplifier in an efficient manner. It was first developed by Leonard R. Kahn in 1952 [27] and later enhanced by others [5, 22]. EER technique, shown in Fig. 1.6, combines a

switch-mode amplifier and a highly efficient envelope amplifier. The system typically consists of a limiter to eliminate the envelope. The resulting constant amplitude phase modulated carrier is then amplified by a switch-mode PA like Class E [22] or Class F [28]. A constant envelope signal enables driving the switch-mode amplifiers with high efficiency without performance degradation by high PAR signals. Finally, the envelope is restored by modulating the supply voltage at the amplifier. The efficient combination output inside a RF transistor is linearly dependent on the input signal, and clipping at the peak power is avoided because the bias supply moves with signal's envelope. Therefore, EER technique theoretically can achieve very high efficiency and high linearity [29]. However, it faces several implementation issues for base-station power amplifiers, such as 1.) the linearity is stringently dependent on the time-alignment between RF input and dynamic envelope voltage [4], and 2.) the envelope eliminated input signal will have extreme bandwidth such that a high power input driver is typically required, which lowers the system overall performance.

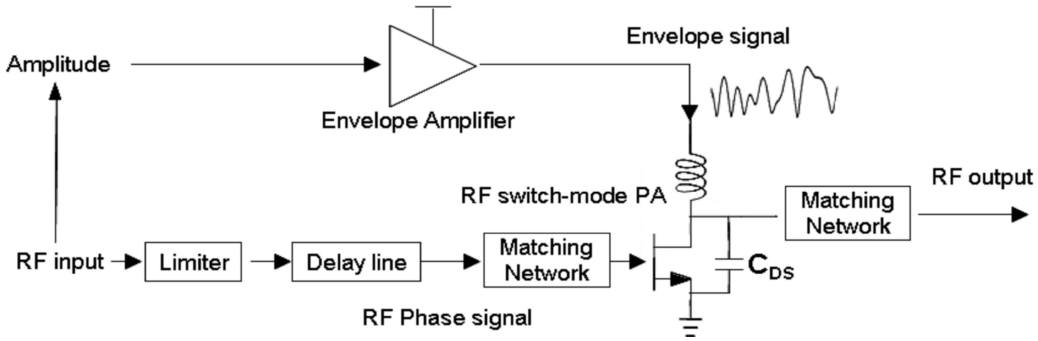


Figure 1.6: Envelope Elimination and Restoration (EER) PA [4]

1.2.4 ET Power Amplifier

Envelope Tracking (ET) technique, which is the main focus of this dissertation, is a method to improve the power amplifier efficiency while dealing with high PAR input signals [6, 23, 30]. Similar to EER, the ET technique dynamically varies the drain or collector voltage of the RF transistor to track the RF signal's envelope. However, the difference between ET and EER leads to some advantages of applying it for base-station power amplifier. First, shown in Fig. 1.7, the RF power amplifier is operated in quasi-linear mode with class A/AB gate/base bias [14] such that the power amplifier pre-driver does not have to reach a saturated power level. In other words, ET technique does not limit the amplitude modulation of the RF signal as is in the EER case. The RF input power contains both amplitude and phase information, which eases system implementation and time-alignment [5, 6]. Moreover, the ET technique permits the supply voltage variation to be somewhat less accurate to the RF signal's envelope than EER, which provides flexibility of designing narrow band envelope amplifier for wide band systems [31]. A more detailed description of the ET system will be described in chapter 2.

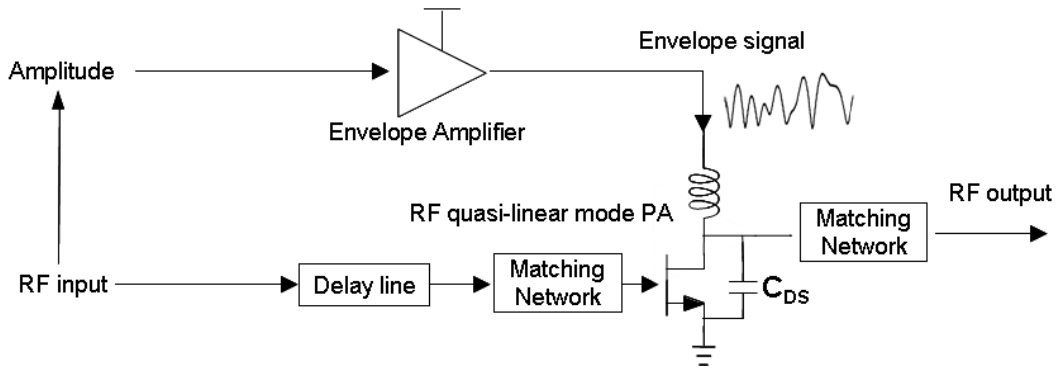


Figure 1.7: Envelope Tracking (ET) PA [5, 6]

1.3 Scope of Dissertation

The ET amplifier structure has been focus of many research papers [4, 6, 28, 30]. However, more research needs to be done to improve efficiency and linearity performance, both in the area of optimization of RF power amplifier as well as envelope amplifier. This thesis is dedicated to exploring the development of envelope amplifiers used in envelope tracking technique applied for wireless communication systems. The main challenge is to design a high efficiency envelope amplifier to improve the overall efficiency while meeting the system linearity requirements. The objective of this dissertation is to analyze practical design issues for an envelope amplifier and provide solutions for high efficiency and good linearity performance.

First, the envelope tracking power amplifier is analyzed, and envelope amplifier architectures are investigated. Based on the study, design and implementation of envelope amplifiers for different RF transistor technologies is presented and analyzed for maximizing the performance of ET amplifier.

The dissertation is organized as follows:

In chapter 2, the ET technique is reviewed to give a clear picture of ET system architecture and requirements. Design challenges are developed and addressed for the envelope amplifier. A general purpose simulator is presented for analyzing the behavior of the envelope amplifier and modeling the overall performance. Based on the model, an implementation strategy towards high efficiency envelope amplifier is introduced. Experimental results are presented for comparison with the model.

In chapter 3, an envelope amplifier design for high voltage applications is addressed in detail. A hybrid envelope amplifier design based on Bipolar-CMOS-DMOS (BCD) technology is designed and implemented. The demonstration is conducted by

using a high voltage envelope amplifier together with a high voltage GaN-HEMT RF transistor. Effect of maximum absolute supply voltage on ET power amplifier performance is analyzed and verified by experiments.

Chapter 4 proposes an efficiency improvement strategy for an envelope amplifier, using a dual-switcher architecture. A digital signal processing (DSP) control switcher is designed, implemented and utilized to improve the efficiency of envelope amplifiers. Efficiency measurement of the ET power amplifier using GaAs high voltage HBT devices together with a dual-switcher envelope amplifier achieves the record-high efficiency with good linearity performance.

Chapter 5 concludes the dissertation and possible future investigation areas are suggested.

Chapter 2

Envelope Tracking Power Amplifier

2.1 Introduction

High power amplifier (HPA) efficiency improvement for W-CDMA base stations is an ongoing area of research. HPA efficiency determines the power consumption, size, cost, and cooling requirements of a base-station. As we discussed in chapter 1, the envelope tracking architecture is designed to improve HPA average efficiency at power back-off. In this chapter, the envelope tracking technique will be first discussed in Section 2.2. Its influence on efficiency of a RF transistor will be reviewed and analyzed in Section 2.3. The envelope amplifier architecture is then studied in Section 2.4, and a general purpose simulator is proposed to provide for guidelines for envelope amplifier design in Section 2.5. Finally, envelope amplifier efficiency measurement together with simulation results are presented for comparison in Section 2.6.

2.2 Envelope Tracking Techniques

ET power amplifiers share important features with polar transmitter systems which employ phase and amplitude signals instead of I/Q modulation directly. There

are different variations of ET architecture proposed in the literature [4, 6, 30]. Fig. 2.1 shows the envelope tracking system diagram [6]. An analog envelope signal as well as in-phase (I) and quadrature (Q) baseband signals are generated in the digital domain. After up-conversion, the resultant RF signal provides the time varying input signal to the RF amplifier after a suitable driver amplifier. The supply voltage for the RF amplifier is modulated by the amplified envelope signal through an efficient wide-band envelope amplifier such that the RF amplifier keeps operating close to its saturated power region for all envelope amplitudes to improve average efficiency. A detroughing function (2.1) is used to fit the envelope of the RF input signal into a voltage waveform, which avoids RF transistor gain collapse at zero drain/collector voltage.

$$V_{env}(t) = V_{max} \cdot (x_{in}(t) + b \cdot e^{\frac{-x_{in}(t)}{b}}) \tag{2.1}$$

Where $x_{in}(t)$ is the normalized input IF signal, V_{max} is the maximum DC power supply, and b is the detroughing factor. The detroughing process also helps reduce high frequency components of the envelope signal [6]. Fig. 2.2 shows the power spectrum of the envelope before and after detroughing. The high frequency component can be manipulated to within certain limited bandwidth.

To reduce the extent of back-off needed for the time varying envelope, a decresting function (an adjustment of the PAR) is performed digitally on the baseband signal to favor improve efficiency by increasing the average output power, as well as to help meet the ACPR and error vector magnitude (EVM) requirements [6]. To minimize distortion caused by the time-delay difference between envelope and RF paths, synchronization is performed by maximizing the amplitude and phase correlation between the input and

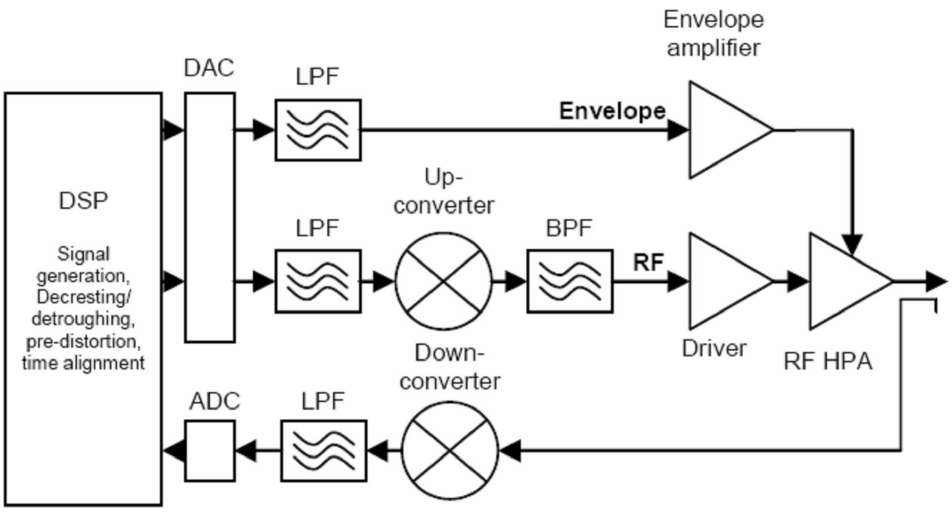


Figure 2.1: Envelope Tracking System [6]

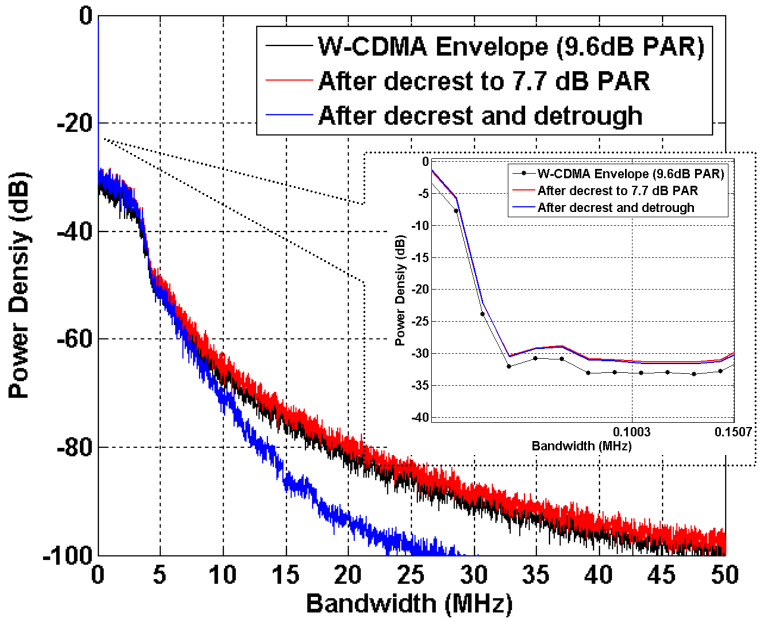


Figure 2.2: W-CDMA Envelope Signal Power Spectrum Before and After Detroughing and Decresting

down-converted output signals [4]. In addition to the delay, there are other sources of nonlinearity in the ET amplifier such as RF transistor trans-conductance nonlinearity and output capacitance variations with varying envelope voltage. To minimize the distortion caused by the RF amplifier, pre-distortion is carried out in the digital domain. The pre-distorted input signal is created by the inverse function of the measured AM/AM and AM/PM characteristics of the overall system (including the driver), such that the stringent linearity requirements imposed by the FCC can be fully satisfied [6, 15, 32].

2.3 ET Power Amplifier Efficiency

The overall ET power amplifier efficiency η_{ET}, neglecting the DSP unit power consumption, is determined by both RF power amplifier's efficiency, η_{PA}, and the wide-band envelope amplifier's efficiency, η_{env}, as described in (2.2).

$$\eta_{ET} = \eta_{PA} \cdot \eta_{env} \tag{2.2}$$

η_{PA} in ET operation, for a class B gate/base bias, can be calculated in (2.3) [1]:

$$\begin{aligned}
\eta_{PA} &= \frac{P_{out}(rf)}{P_{DC}} \\
&= \frac{V_{dd} - V_{min}}{V_{dd}} \cdot \frac{\pi}{4} \\
P_{out}(rf) &= \frac{1}{2} \cdot V_{fund} \cdot I_{fund} \\
P_{DC} &= V_{dd} \cdot \frac{I_{rf}}{\pi} \\
V_{fund} &= R_L \cdot \frac{I_{rf}}{2} \\
I_{fund} &= \frac{I_{rf}}{2} \\
V_{dd} &= V_{min} + I_{rf} \cdot \frac{R_L}{2}
\end{aligned} \tag{2.3}$$

Where $P_{out}(rf)$ is the RF fundamental output power, V_{fund} is the RF fundamental output voltage, I_{fund} is the RF fundamental output current, P_{DC} is the DC input power, R_L is the power amplifier load line, I_{rf} is the dynamic RF current, V_{dd} is the dynamic supply voltage, and V_{min} is the minimum voltage swing of RF transistor. This treatment describes the ideal case for an ET power amplifier with class B gate/base bias in which the envelope amplifier provides the ideal dynamic voltage supply with unlimited bandwidth to the RF transistor. For a constant drain/collector bias class B RF power amplifier, the efficiency varies with output power as described in (1.1). However, from (2.3), the power amplifier's efficiency no longer scales with output power, which is a dramatic improvement for efficiency at power back-off regime. Fig. 2.3 plots the efficiency comparison between a constant drain/collector class B power amplifier and an ideal ET power amplifier versus normalized output power. In the ideal ET case, the RF power amplifier efficiency degrades only with the factor, V_{min}. In other words, the efficiency of RF power amplifier can be maintained within a wide power range (voltage range) in ET operation and rolls off only due to RF transistor's intrinsic knee voltage [10, 33].

From (2.3), it is seen that the larger value of V_{dd}/V_{min}, the more efficiency RF amplifier can achieve ideally. We can define an efficiency degradation factor, η_{RF} in (2.4) [10, 33].

$$\begin{aligned} \eta_{RF} &= 1 - \frac{V_{min}}{V_{dd}} \\ &\approx 1 - \frac{R_{on}}{R_{load}} \end{aligned} \tag{2.4}$$

Where R_{load} can be approximated as the RF amplifier fundamental load line [10] and R_{on} is the intrinsic "ON" resistance of RF transistor. For the ET operation, V_{dd} changes continuously with input RF signal and can be generated by a detroughing function in

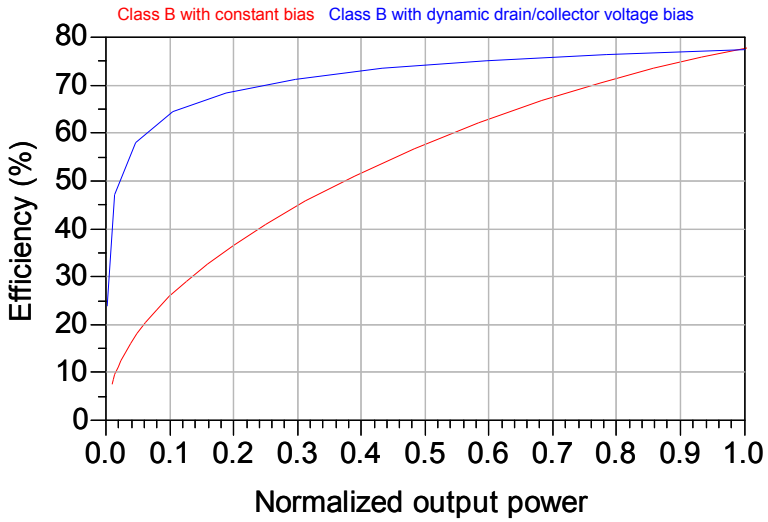


Figure 2.3: Comparison of Simulated Efficiency versus Output Power between Class B Power Amplifier and Class B with Ideal ET Operation

(2.1). (2.4) illustrates a crucial factor in designing an envelope amplifier for the corresponding RF transistors. While using a RF transistor with higher V_{min}, the dynamic range of the envelope amplifier has to be extended to preserve the high efficiency of RF amplifier in ET operation [33]. In other words, for a RF transistor with a fixed R_{on} value, the higher the R_{load}, the better the efficiency. Increasing the dynamic voltage swing of the RF transistor is helpful in choosing larger R_{load}. To verify the above analysis, in chapter 3, two different dynamic range envelope amplifiers are employed separately in an ET system with the same RF transistor technology for performance comparison.

2.4 Envelope Amplifier Architecture

The envelope amplifier topology we discuss in this section is shown Fig. 2.4 [23]. It was originally proposed for hybrid amplifiers used in various instrument applications [34] and then enhanced by Mara and Kimball, et. al for the ET power amplifier.

In Fig. 2.4, the envelope amplifier includes a linear stage in conjunction with a switching buck converter (switcher). The reason for using the hybrid amplifier architecture relies on the characteristics of the signal the amplifier has to handle. The W-CDMA envelope signal power spectrum, shown in Fig. 2.5, has a large portion of power at low frequency, roughly between DC to 100 kHz, and a smaller high frequency component of the signal beyond 100 KHz. The low frequency component contains more than 85% of the signal power. This suggests an architecture where the high efficiency switcher provides a current output and handles the majority of the envelope power. The linear stage provides a voltage output, which is an amplified replica of the input voltage, V_{in}, to ensure high accuracy of the output signal. The switcher and the linear stage are coordinated by using a current-sense hysteretic controller, which is used to turn on/off the switcher by sensing the current flowing out of the linear stage through a current-sense resistor. The switching noise introduced in the switcher can be attenuated by the loop filter inside the linear stage. The disturbances introduced by the switcher at the output of envelope amplifier are therefore reduced [13, 35]. To better understand the behavior of the envelope amplifier, a general purpose model based on Matlab/Simulink has been developed and is described in the following section.

2.5 Envelope Amplifier Modeling

Fig. 2.6(a) shows the systematic block diagram of the envelope amplifier and Fig. 2.6(b) presents the implementation blocks in Matlab/Simulink environment. For simplified analysis without loss of generality, the load line of RF power amplifier is modeled as a constant load impedance, R_{load}. In Fig. 2.6(a), V_{in} represents the envelope

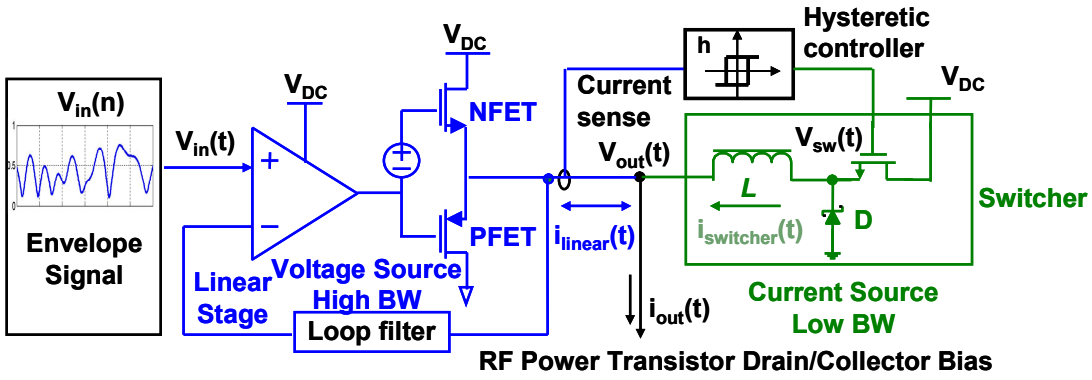


Figure 2.4: Envelope Amplifier Architecture [6]

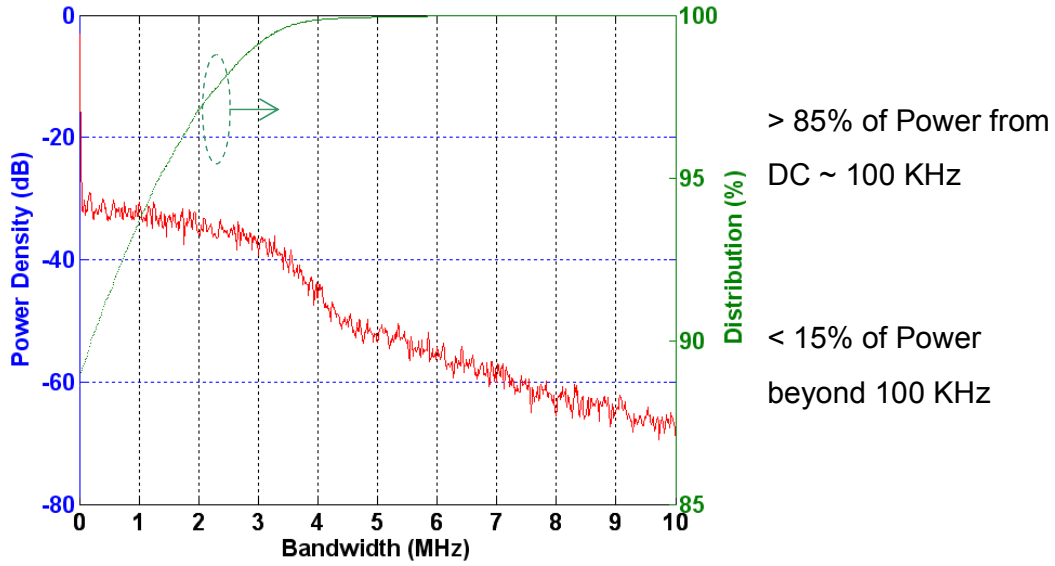
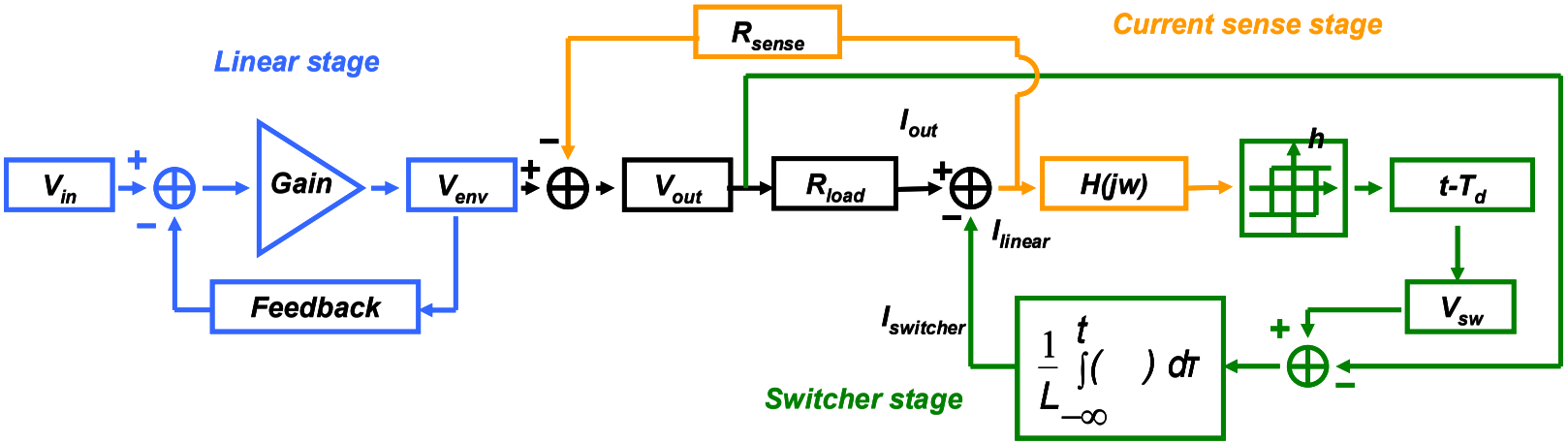


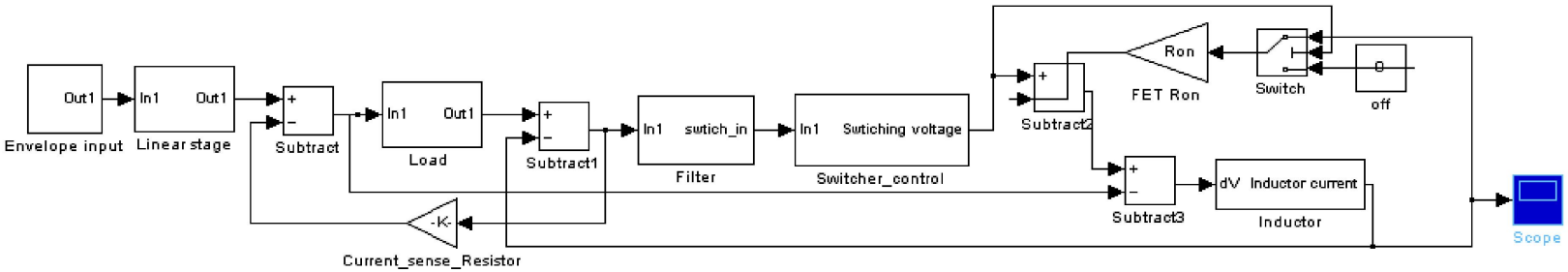
Figure 2.5: W-CDMA Envelope Signal Characteristics

input voltage, V_{env} represents the linear stage output, $Gain$ represents the linear stage voltage gain with certain bandwidth (set around 50 MHz), V_{out} represents the envelope amplifier output voltage, I_{out} represents the amplifier output current, and $I_{switcher}$ represents the switcher output current. The hysteretic comparator is modeled as a relay. The difference current, I_{linear}, between I_{out} and $I_{switcher}$, which the linear stage has to provide, is directed into the relay, which represents the current-sense feedback path together an comparator used in the hardware implementation. I_{linear} also feeds back to the linear stage output through a current-sense resistor, R_{sense}. $H(jw)$ represents a second order low pass filter to limit the bandwidth of the difference signal before going into the comparator. The relay output is the switching waveform, V_{sw}. For simplicity, the model neglects the actual switcher driver circuits and uses a delay block, T_d to represent any possible delay in the switcher driver circuits. The switcher current, $I_{switcher}$, is generated by the voltage difference between V_{sw} and a feed-forward envelope output signal, V_{out}, across an inductor, L. The overall system modeling is similar to a feed-forward delta modulator. Based on the simulation results of V_{out}, I_{out}, I_{linear}, V_{sw}, and $I_{switcher}$ generated from the simulator, the envelope amplifier's dynamic behavior is predictable while operating with different signals and at different power levels, which eases the design and analysis.

We use an EDGE signal as the input to begin to illustrate the envelope amplifier modeling results. The 8PSK modulation of an EDGE system uses linear modulation techniques and generates amplitude varying signals with a PAR of 3.2 dB. The spectrum of EDGE signals is shown in Fig. 2.7(a); the signal bandwidth is around 200 KHz. The envelope signal power spectrum is shown in Fig. 2.7(b). Its bandwidth, though

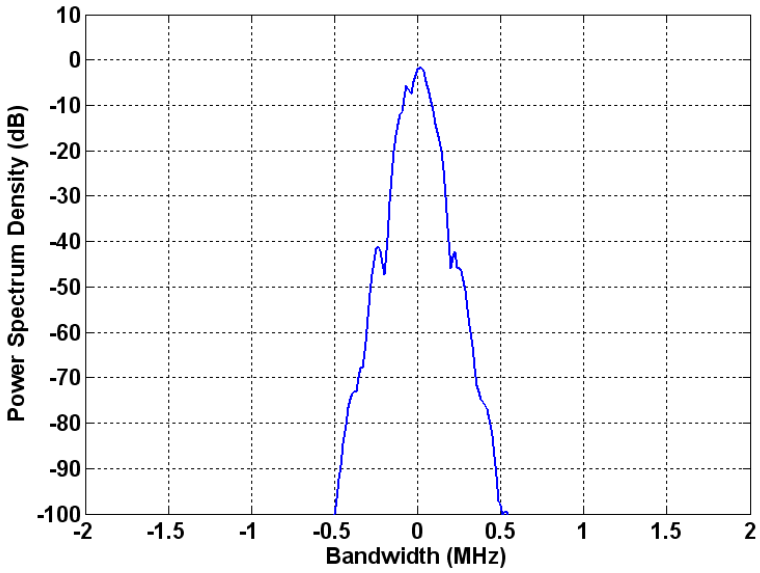


(a)

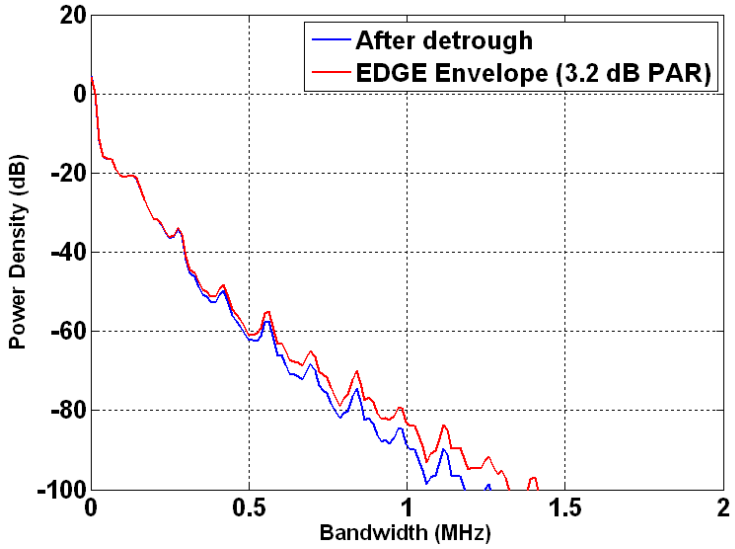


(b)

Figure 2.6: Envelope Amplifier Matlab/Simulink Model: (a) System Block Diagram (b) Implementation in Simulink



(a)

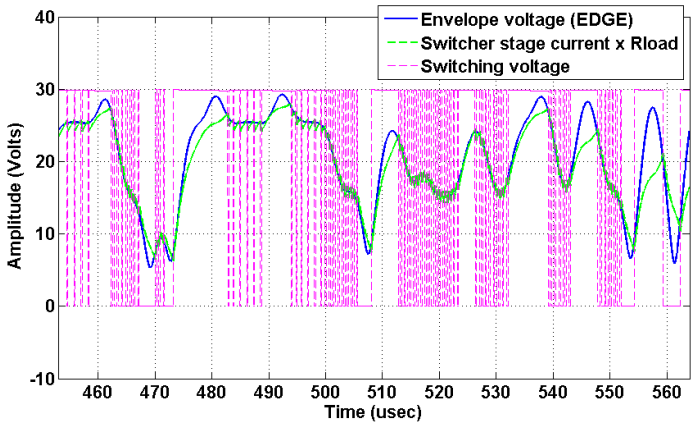


(b)

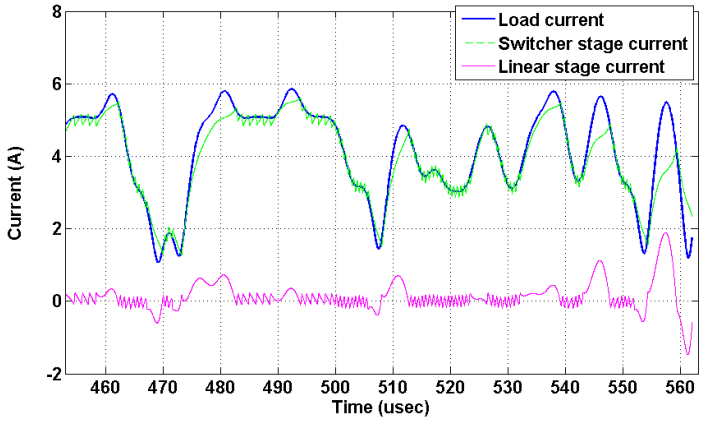
Figure 2.7: EDGE signal: (a) IF signal (b) Envelope signal.

broaden than the IF or RF signal, is also within several hundreds KHz. Fig. 2.8(a) and Fig. 2.8(b) present the steady state simulations, including envelope output voltage, the switching waveform (Fig. 2.8(a)), the envelope output current and switcher's output current (Fig. 2.8(b)). In this example, the peak envelope voltage is scaled to 30 V, the load impedance is set at 5 ohm and the inductor value is set at 25 μH. The V_{rms} of the envelope signal is around 20$\sim$21 Volts. In Fig. 2.8(b), due to the condition that the switcher's current slew rate is higher than the output current average slew-rate [5], $I_{switcher}$ tracks the I_{out} closely and the linear stage only corrects the switcher output error. For this, it only consumes a small fraction of total input power. The peak current the linear stage has to provide is less than 2 A and this happens only when the instantaneous slew-rate of the switcher is lower than that of the output current. At this moment, the linear stage is required to supply the rest of power. Fig. 2.8(c) shows the experimental results for the same section of EDGE waveform, and the same behavior is observed. Fig. 2.8(d) shows the switching frequency distribution both from the simulation and the measurement results. Here experimental results were obtained by data collections on switching pulses of total 500 μsec period with 5 nsec resolution (more than 1 Mega samples) using 4 GS/sec sampling oscilloscope. The switching frequency is around 1$\sim$2 MHz, which is higher than EDGE signal's bandwidth.

Fig. 2.9 shows the steady state simulation using a W-CDMA signal with 7.7 dB PAR. The peak envelope voltage, the load, and the inductance value are set the same as in Fig. 2.8. The V_{rms} of envelope signal is around 11$\sim$12 Volts. In this example, $I_{switcher}$ tracks around the moving average of the I_{out} due to the condition that average slew-rate of envelope current, I_{out} is larger than that of switcher current [5]. The switching pulses shown in Fig. 2.9(a) shows lower switching frequency than the envelope signal band-



(a)



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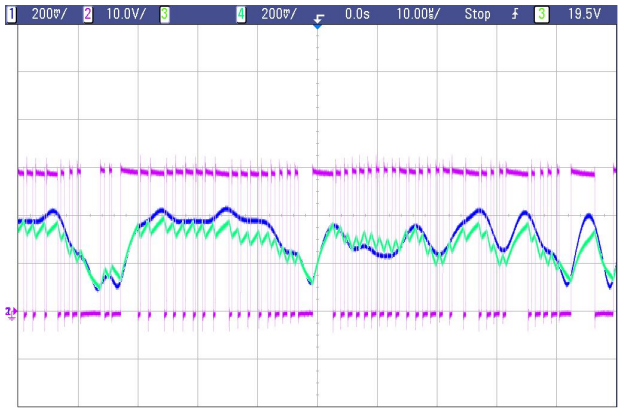
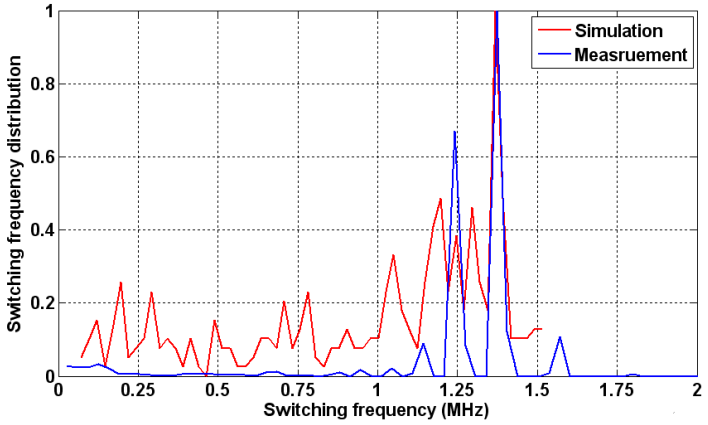


(c)



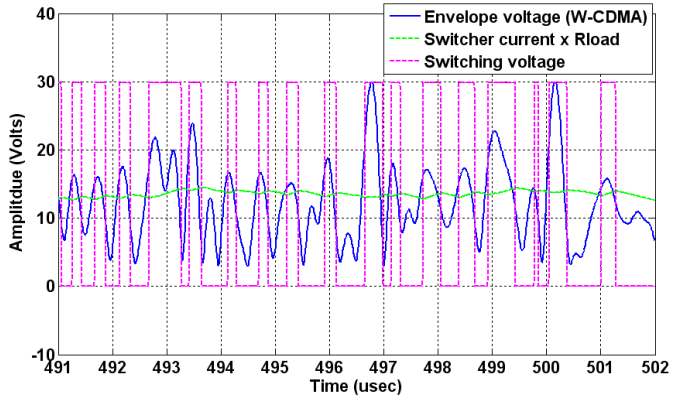
(d)

Figure 2.8: Envelope Amplifier Running EDGE Signal: (a) Simulation (b) Simulation (c) Experimental results (Ch1,Ch4: 10 mV = 100 mA) (d) Switching Frequency Distribution comparison.

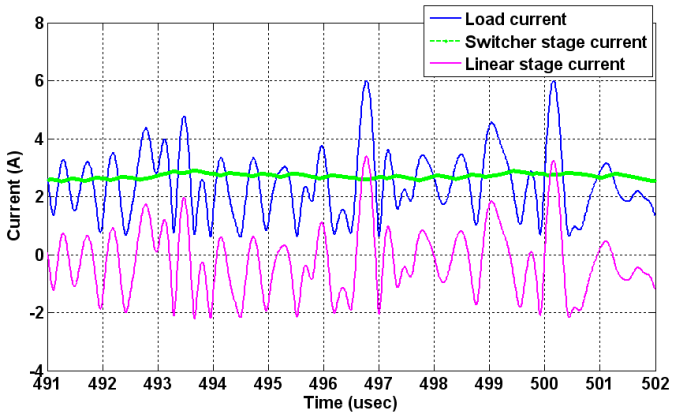
width shown in Fig. 2.5. In this case, the switcher does not provide the full current to the load but only approximately the average of the signal. I_{linear} sources and sinks the high frequency current shown in Fig. 2.9(b). The peak current the linear stage has to provide is around 3.5 A. Fig. 2.9(c) shows the experimental results. These exhibit the same behavior (except some rare high frequency switching pulses due to the noise.) Fig. 2.9(d) compares the switching frequency distribution between the simulation and measurement results, illustrating the good accuracy of the model. The switching frequency is around $1\sim2$ MHz.

From the simulation results, the envelope amplifier architecture shows different behaviors depending upon the envelope signal's slew rate compared to the switcher's slew rate. In Fig. 2.8(b) with the EDGE signal, the power is mainly produced from the switcher stage. Therefore, even though the peak load current is around 6 A, the peak current provided from the linear stage is small. However, in Fig. 2.9(b) with the W-CDMA case, the peak current the linear stage has to provide is about 3.5 A and therefore, the linear output stage has to be sized large enough to support such high power handling. In order to use the envelope amplifier in different scenarios, the device size and power handling capability of the linear stage should in general follow the case represented by the W-CDMA signals. The magnitude of switcher current shown in Fig. 2.8(b) and Fig. 2.9(b), together with the switching frequency distribution in Fig. 2.8(d) and Fig. 2.9(d), can be used to estimate the switcher's loss, and to design the size of the switch-FETs for implementing a high efficiency switcher. The overall power loss and efficiency performance of the envelope amplifier is described in Section 2.6.

Another important result observed from the simulation is the start-up (or transient) condition. Fig. 2.10(a) and 2.10(b) shows the start-up simulation running EDGE



(a)



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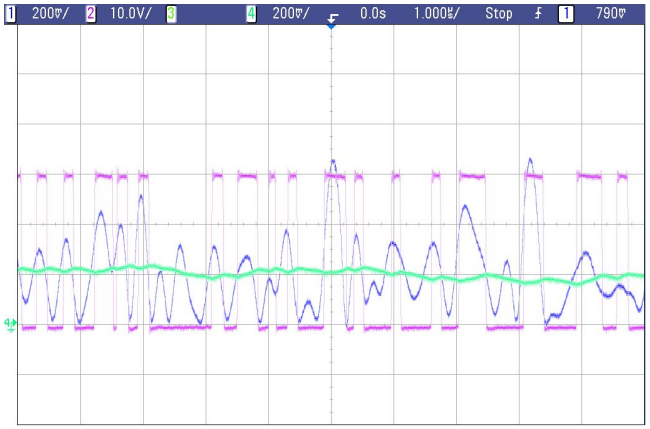
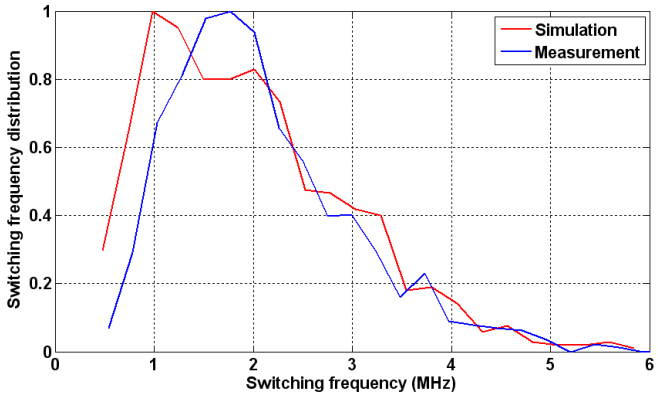


(c)



(d)

Figure 2.9: Envelope Amplifier Running WCDMA Signal: (a) Simulation (b) Simulation (c) Experimental results (Ch1,Ch4: 10 mV = 100 mA) (d) Switching Frequency Distribution Comparison.

and W-CDMA signals, respectively. For the case of an EDGE signal, the switcher catches up to the output current quickly such that the linear stage only needs to support a small amount of power. However, in the case of a W-CDMA signal, the linear stage has to provide the majority of current before the switcher moves into its steady-state. The duration of this setting period depends on the time constant of the switcher. In Fig. 2.10(b), the transient time is about 5 μsec. During this period, the linear stage is highly stressed, which potentially leads to overheating or damage of the envelope amplifier if the linear stage power handling capability is not enough. In this case, either small time-constant of the switcher or appropriate protection circuits have to be designed.

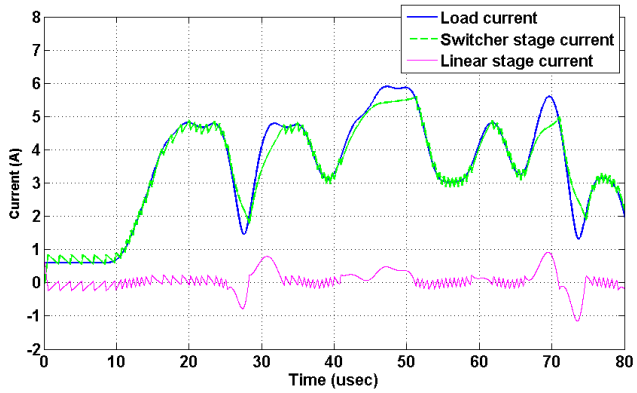
2.6 Envelope Amplifier Efficiency

In this section, we will incorporate an estimator into the simulator to model efficiency of the envelope amplifier. The overall efficiency of the amplifier can be described in (2.5):

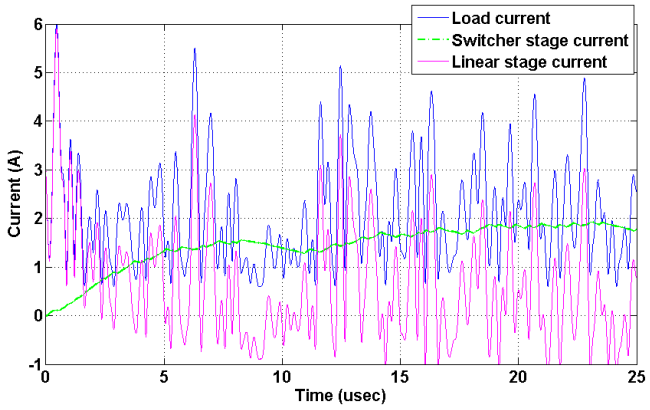
$$\eta_{env} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{2.5}$$

Where P_{out} represents the amplifier average output power while the P_{loss} represents total power loss inside the amplifier. The power loss can be easily estimated using the simulator by extracting the current and voltage transient information at each stage. There are three main power losses inside the amplifier: 1.) The static power loss, 2.) The linear stage dynamic power loss, and 3.) The switcher stage dynamic power loss.

The static power loss refers to any loss independent of the amplifier's output power. For example, bias current of the linear stage introduces static power loss. The



(a)



(b)

Figure 2.10: Envelope Amplifier Start-up Condition: (a) EDGE signal (b) W-CDMA signal.

switcher driver also require several mA bias current [36], and the current-sense stage power loss which includes the comparator's static power consumption, etc. By properly selecting low power devices (Section 3.3), the static power loss can be reduced.

Referring to Fig. 2.4, the linear stage dynamic power loss can be estimated by (2.6) [5].

$$P_{loss_{linear}} = P_{loss_{NFET}} + P_{loss_{PFET}} \tag{2.6a}$$

$$\text{where} \quad P_{loss_{NFET}} = (V_{DC} - V_{out}) \cdot (I_{out} - I_{switcher}) \tag{2.6b}$$

for Switcher turn-on

$$P_{loss_{PFET}} = (V_{out}) \cdot (I_{switcher} - I_{out}) \tag{2.6c}$$

for Switcher turn-off

The loss ignores the driver's power consumption and regards it as a static power loss. Using the transient simulation results in Fig. 2.8(b) and Fig. 2.9(b), the linear stage power loss can be easily calculated. The loss is highly related to the envelope signal's amplitude probability distribution and the envelope peak voltage magnitude (headroom). In addition, as we discuss in Section 2.5, the magnitude of linear stage current, I_{linear} is highly correlated with the switcher's output current, $I_{switcher}$. For example, the linear stage using W-CDMA signals has to provide larger current compared to the case with EDGE signals. Therefore the power loss of the linear stage using W-CDMA signals increases. Proper design of the switcher control can reduce the linear stage output current and hence the power loss to help resolve this issue.

The loss inside the switcher stage is more complicated than the other loss mechanisms of the amplifier. Fig. 2.11(a) shows the schematic of the switcher, which is

composed of a switcher high-side driver, a switch-FET, M_s, a Schottky diode, D_s and a power inductor, L. The power loss in any switch-FET and Schottky diode is the combination of the switching losses and the conduction losses. Each loss mechanism is presented in (2.7a) [7].

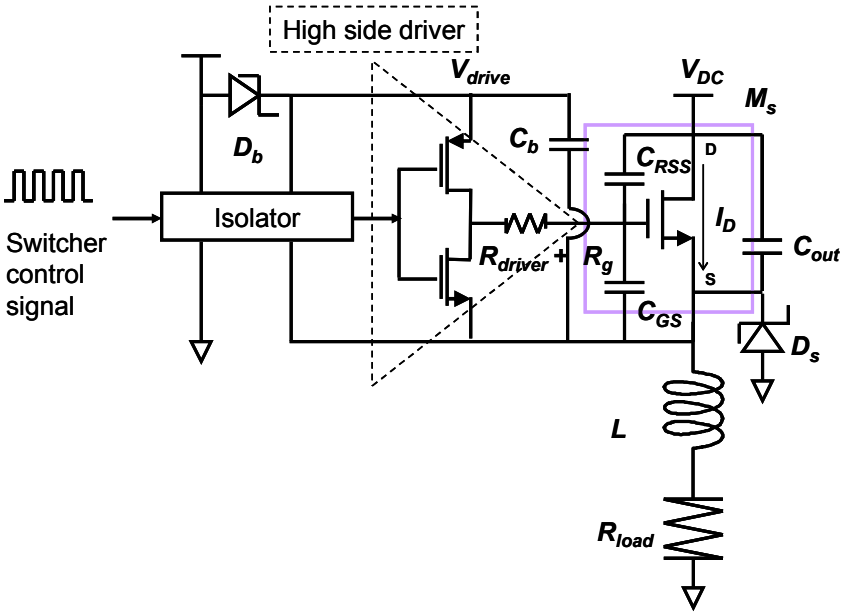
(2.7b) estimates gate charge loss of the switch-FET. The loss is proportional to gate charge of the device and the switching frequency. Generally, the larger size of the device, the larger the gate charge and therefore the loss increases.

(2.7c) estimates commutation loss of the switch-FET during switching. t_{on} and t_{off} can be estimated through the gate-charge diagram provided from the the device data-sheet [37, 38, 39]. Fig. 2.11(b) illustrates the gate charge diagram, and associated t_{on} and t_{off} can be estimated by (2.8) [7]. The loss consumes a large portion of power in the hard switching, especially with inductance as the load of the switch-FET [40].

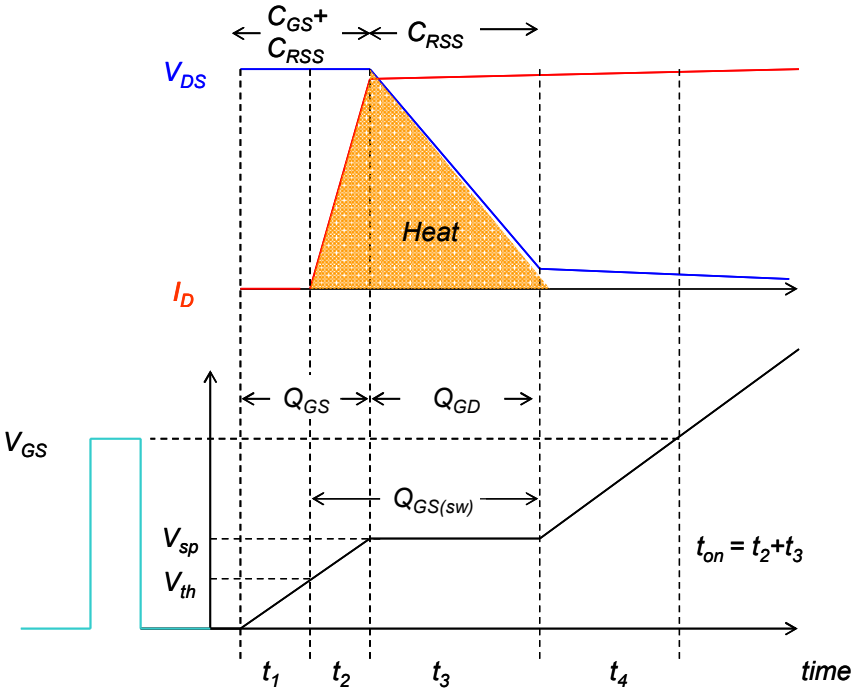
(2.7d) estimates the output capacitance switching loss. The loss depends on output capacitance of the switch-FET, diode and associated paralleled parasitics. The loss is proportional to the area of the switch-FET and the diode as well as the switching frequency.

(2.7e) estimates the switch-FET's conduction loss. The magnitude of R_{on} of the switch-FET is the dominate power loss factor. The conduction loss is generally inverse proportional to the switch-FET size and scales with the switcher's output power.

(2.7f) estimates the conduction loss of Schottky diode, D_s. The maximum forward voltage drop, V_F, of the diode dominates the major power consumption. The lower the forward voltage drop, the lower the power loss during the operation.



(a)



(b)

Figure 2.11: (a) Switcher Stage Schematic; (b) High Side switch-FET Gate Charge Diagram [7]

$$P_{loss_{switcher}} = P_{loss_{Switching}} + P_{loss_{Conduction}}$$

$$= (P_{loss_{Driver}} + P_{loss_{Commutation}} + P_{loss_{C_{out}}}) + P_{loss_{R_{on}}} + P_{loss_{Diode}} \tag{2.7a}$$

$$\approx Q_g \cdot V_{gs} \cdot f_{sw} \tag{2.7b}$$

$$+ \frac{1}{2} \cdot I_D \cdot V_{DC} \cdot (t_{on} + t_{off}) \cdot f_{sw} \tag{2.7c}$$

$$+ \frac{1}{2} \cdot C_{out} \cdot V_{DC}^2 \cdot f_{sw} \tag{2.7d}$$

$$+ D \cdot I_D^2 \cdot R_{on} \tag{2.7e}$$

$$+ (1 - D) \cdot I_L \cdot V_F \tag{2.7f}$$

where Q_g is switch-FET total gate charge

V_{gs} is switch-FET gate-to-source turn-on votlage

f_{sw} is the average switching frequency

I_D is the drain current while switch-FET is on

t_{on} is switch-FET turn-on time

t_{off} is switch-FET turn-off time

C_{out} is total output capacitance around source node of switch-FET

D is average duty ratio of switching pulses

R_{on} is switch-FET turn-on resistance

V_F is Schottky diode forward voltage

$$t_{on} = \frac{Q_{G(sw)}}{I_{driver(L \longrightarrow H)}} \tag{2.8a}$$

$$t_{off} = \frac{Q_{G(sw)}}{I_{driver(H \longrightarrow L)}} \tag{2.8b}$$

$$Q_{G(sw)} \approx Q_{GD} + \frac{Q_{GS}}{2} \tag{2.8c}$$

$$I_{driver(L \longrightarrow H)} = \frac{V_{drive} - V_{sp}}{R_{driver(L \longrightarrow H)} + R_g} \tag{2.8d}$$

$$I_{driver(L \longrightarrow H)} = \frac{V_{sp}}{R_{driver(H \longrightarrow L)} + R_g} \tag{2.8e}$$

$$V_{sp} \approx V_{th} + \frac{I_D}{G_M}$$

where $Q_{G(sw)}$ is the approximated gate charge for a switch-FET to move through a switching interval

Q_{GS} is switch-FET gate-to-source charge

Q_{GD} is switch-FET gate-to-drain ("Miller") charge

$I_{driver(L \longrightarrow H)}$ is the switcher driver current in the rising time

$I_{driver(H \longrightarrow L)}$ is the switcher driver current in the falling time

$R_{driver(L \longrightarrow H)}$ is the switcher driver pull-up resistance

$R_{driver(H \longrightarrow L)}$ is the switcher driver pull-down resistance

R_g is the switch-FET gate resistance

V_{sp} is the approximated switching point voltage (Fig. 2.11(b))

V_{th} is the typical gate threshold voltage

I_D is the drain current when switch-FET is on

G_M is the switch-FET trans-conductance

The overall envelope amplifier's power loss can be estimated by using (2.6)$\sim$(2.8). Fig. 2.12(a) shows the simulated percentage of each power loss as a fraction of the overall DC input power of the amplifier using EDGE signal, operating at around 70 W output power. In this example, the linear stage consumes less than 2% of total input power due to the majority power contributed by the switcher. The switcher loss takes about $5\sim6\%$ of the total input power. The results enable high efficiency performance for EDGE signals. Fig. 2.12(b) shows the percentage of each loss as a fraction of the total DC input power using a W-CDMA 7.7 dB PAR signal at similar output power level in Fig. 2.12(a). For this case, the switcher dynamic loss takes about $7\sim8\%$ of the total DC power. The high percentage of Schottky diode turn-on loss can be improved by designing a synchronous switching buck converter [7] for the switcher. The linear stage loss takes about $18\sim19\%$ of the total input power. This accounts for the high frequency power fully provided by the linear stage with this signal. In both examples, the commutation loss of the switch-FET plays an important role due to high switching frequency. A switch-FET chosen for low gate charge and low gate resistance is, therefore, preferable to a low on-resistance device for this application. Reducing the linear stage power loss using W-CDMA signals is discussed in chapter 4.

A 30 V peak voltage envelope amplifier, shown in Fig. 2.13, was assembled to verify the efficiency estimation results [6, 8, 9]. The comparison is carried out experimentally with constant resistance as the load of envelope amplifier. Table 2.1 summarizes the comparisons of simulated and measurement performance of the envelope amplifier for EDGE and W-CDMA signals. Good agreements are obtained between the model and the measurement results. The efficiency estimator neglects some small frac-

tion of dynamic power loss, such as switching ringing loss [41], power inductor core loss [42] and Schottky diode reverse recovery power loss.

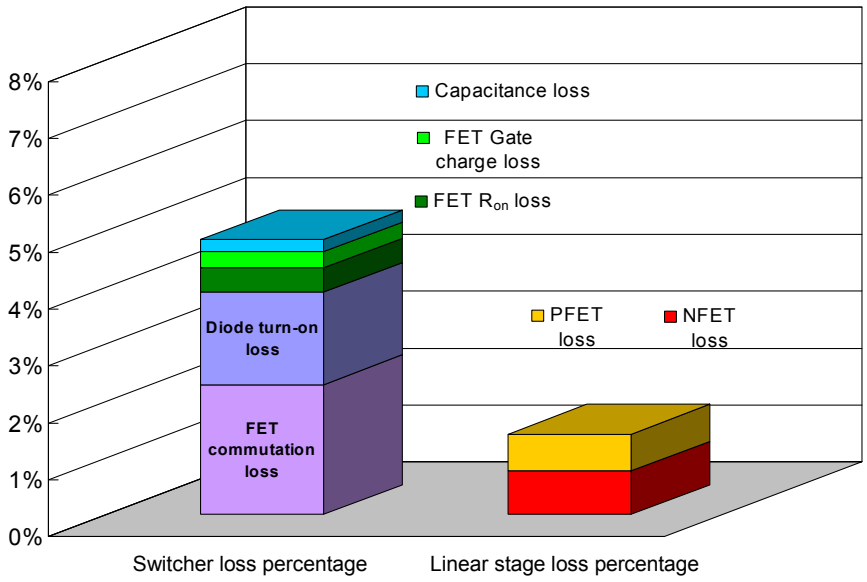
The envelope amplifier shown in Fig. 2.13 can be designed for a wide output power range, eg. 10 W $\sim$ 100 W. However, once the components of the amplifier are designed and assembled, the overall efficiency of amplifier is not a constant value while operating with different signals and load impedances (Table 2.1). The efficiency of the amplifier fluctuates mainly due to two reasons:

1. Some inherent power loss is constant, independent of output power and signal characteristics

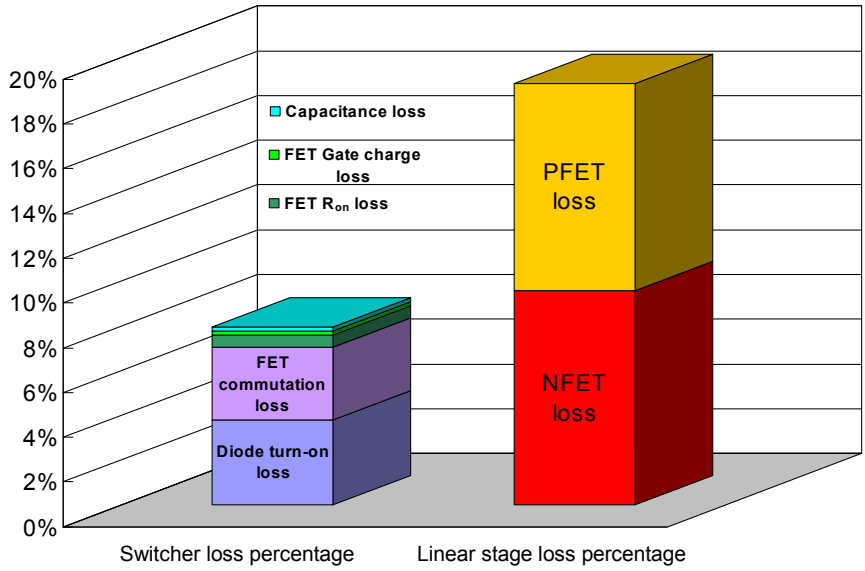
As described earlier, the bias current for each stage is constant and independent of the output power. As the output power reduces, the static loss becomes a higher portion in calculating the efficiency. In addition, part of switching loss, such as (2.7b) and (2.7d) are independent of the output power.

Fig. 2.14(a) shows comparisons of the simulated and measured efficiency results of the envelope amplifier using the same W-CDMA signals (7.7 dB PAR) but operated at different power level. This is done by connecting the envelope amplifier output with different magnitude of load impedances. Due to the static power loss, the efficiency degrades when the output power decreases. Fig. 2.14(b) shows the power loss versus output power both with simulated and measurement results. A static power loss around 2 W is assumed in the model. The measurement result shows somewhat higher than the assumed value.

2. The PAR of envelope signal increases



(a)



(b)

Figure 2.12: Envelope Amplifier Loss Estimation: (a) EDGE signal (3.2 dB PAR) (b) W-CDMA signal (7.7 dB PAR)

Table 2.1: Envelope Amplifier Simulation and Measurement comparisons (30 V Envelope Amplifier)

	W-CDMA 7.7 dB PAR						EDGE 3.2 dB PAR	
	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.
Output power (W)	51.45	53.34	38.59	39.31	25.73	26.46	71.42	70.45
V_{rms} (V)	12.42	12.65	12.42	12.54	12.42	12.6	20.7	20.56
Total DC input power (W)	72.48	74.72	54.86	56.33	37.31	39.23	78.09	78.79
Efficiency ($\%$)	70.99	71.38	70.33	69.79	68.96	67.44	91.45	88.4
Ave. switching frequency (MHz)	1.45	1.57	1.46	1.57	1.48	1.57	1.48	1.41
Switcher stage dynamic loss (W)	5.74	-	4.37	-	3.04	-	3.77	-
Switch-FET loss (W)	2.99	-	2.30	-	1.65	-	2.5	-
Gate charge loss (W)	0.22	-	0.22	-	0.22	-	0.22	-
Commutation loss (W)	2.35	-	1.77	-	1.19	-	1.78	-
Conduction loss (W)	0.25	-	0.14	-	0.06	-	0.33	-
Output capacitance loss (W)	0.17	-	0.17	-	0.17	-	0.17	-
Schottky diode loss (W)	2.75	-	2.07	-	1.39	-	1.27	-
Switcher output power (W)	47.42	-	35.70	-	23.89	-	70.26	-
DC power into switcher stage (W)	53.16	54.86	40.07	40.94	26.93	28.21	74.03	72.98
Switcher efficiency ($\%$)	89.2	-	89.1	-	88.7	-	95	-
Linear stage dynamic loss (W)	13.49	-	10.10	-	6.74	-	1.1	-
Linear NFET loss (W)	6.74	-	4.98	-	3.29	-	0.597	-
Linear PFET loss (W)	6.75	-	5.12	-	3.45	-	0.503	-
Linear stage output power (W)	4.03	-	2.89	-	1.84	-	1.16	-
Static power (W)	1.8	-	1.8	-	1.8	-	1.8	-
DC power into linear stage (W)	19.32	19.86	14.79	15.39	10.38	11.02	4.06	5.81

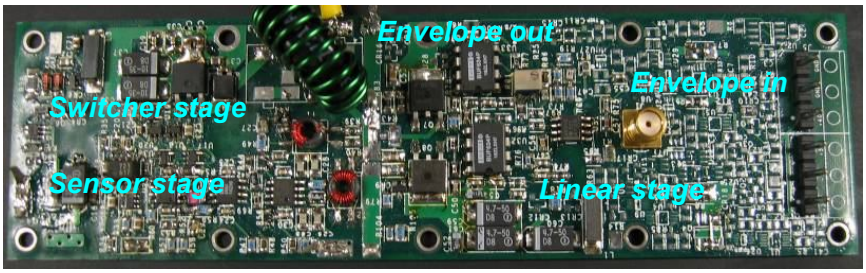
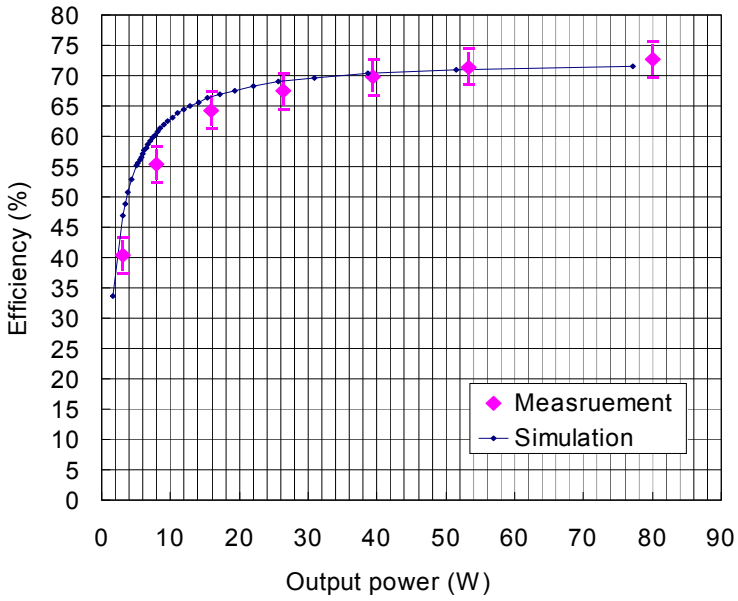


Figure 2.13: Envelope Amplifier Hybrid PCB Design [6, 8, 9]

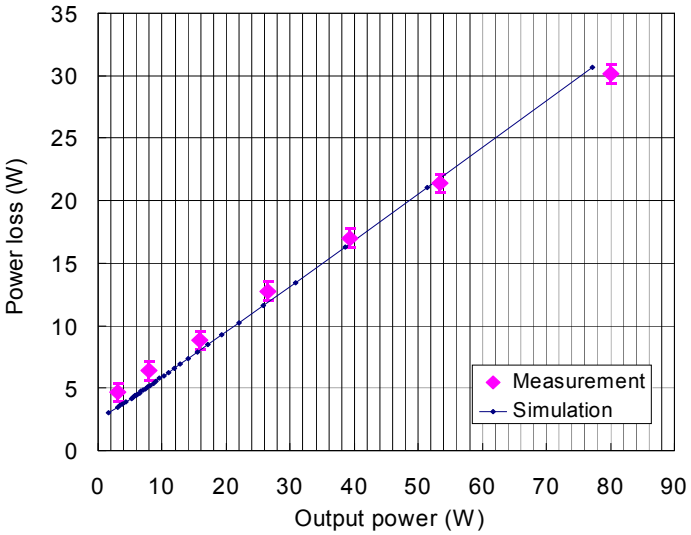
The efficiency of the envelope amplifier degrades with higher PAR input signals. One of the reasons is that the average output power of the amplifier decreases with higher PAR signals. The ratio of static power loss over the output power increases and therefore the overall efficiency drops. More importantly, the linear stage contributes a higher percentage of power loss while dealing with high PAR signals (Fig. 2.12(a) vs. Fig. 2.12(b) and Table 2.1). Fig. 2.15 shows the measured efficiency of the 30 V envelope amplifier (Fig. 2.13) with different PAR signals by connecting the output to the same load impedance (4 ohm). The higher PAR the signal, the lower the efficiency. To counter this efficiency degradation, one of the ideas is to use smaller inductance for the switcher to improve its output current bandwidth, match the envelope signal's slew-rate, and hence reduce the linear stage output current and power consumption. In chapter 4, we will illustrate this idea and propose a novel switcher design to improve the amplifier efficiency.

2.7 Summary

An envelope tracking system is discussed in this chapter. ET power amplifier efficiency degradation factors are reviewed. Understanding the efficiency degradation



(a)



(b)

Figure 2.14: Simulated and Measured Performance Comparisons of the Envelope Amplifier using W-CDMA signals (a) Efficiency; (b) Power loss

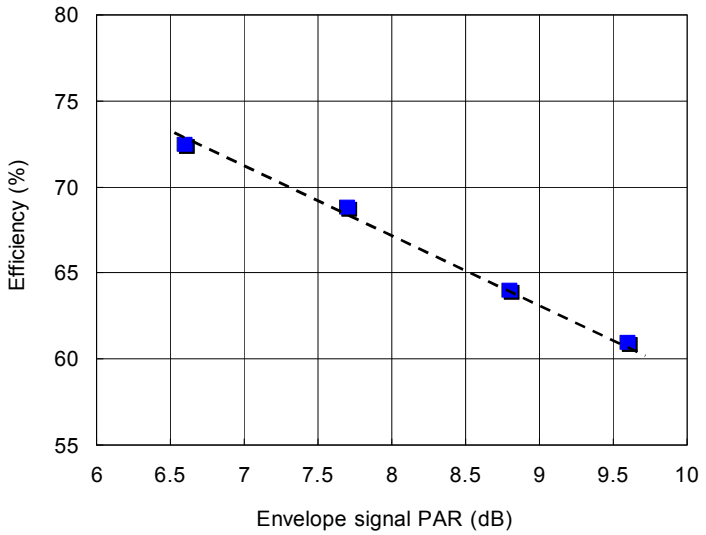


Figure 2.15: Measured Efficiency versus PAR of the Envelope Signals

factors helps in designing the envelope amplifier for different system requirements. An envelope amplifier behavior model and efficiency estimation is presented. A general-purpose envelope amplifier model based on the hybrid amplifier architecture is proposed and demonstrated to provide accurate behavior and efficiency results compared to the experiments.

2.8 Acknowledgements

The author is very grateful to Nokia-Siemens Networks for valuable discussions, and to Nokia-Siemens Networks for partial funding support. Some of the material in this chapter is as it will appear in "Dual-switcher Envelope Amplifier with Digitally-assisted Control for Envelope Tracking Power Amplifiers", C. Hsia, D. Kimball and P. M. Asbeck, submitted to *IEEE Trans.on MTT.,* 2011 (in review). The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for these publications.

Chapter 3

Envelope Amplifier Design for High Voltage Applications

3.1 Introduction

In the previous chapter, the performance of ET power amplifiers and envelope amplifiers was discussed. Various transistor technologies, such as GaAs high voltage HBT, GaN HEMTs and LDMOS, etc. can be incorporated into an ET system to improve power amplifier efficiency according to devices' characteristics [10, 33, 35]. Since GaN-HEMT RF transistors feature high voltage, high power density ($>$ 2 W/mm) and high reliability [30, 43, 44], development of a high performance GaN-HEMT based power amplifier for broad band wireless cellular base-station applications is attractive. In this chapter, an envelope amplifier designed for high voltage operation, particularly useful for ET power amplifiers using GaN-HEMT RF transistors, is presented in detail. As discussed in Section 2.3, an ET power amplifier using higher knee voltage RF transistors requires larger dynamic bias voltage swing in order to maintain the high efficiency operation of the RF transistor. This is the case for the GaN-HEMT device we use to

demonstrate the ET power amplifier performance [10, 33].

The general requirements for a good envelope amplifier design involve considerations of form factor, cost, efficiency, fast response (wide bandwidth) and low ripple with acceptable noise. The hybrid amplifier topology takes advantage of a linear amplifier with high output fidelity as well as a switching amplifier with high efficiency such that the amplifier can be designed to provide a broadband voltage supply and efficient power for the RF power amplifier. However, in order to design a high voltage envelope amplifier, the circuit implementation poses many design challenges. The major design issues and considerations are first reviewed in Section 3.2, and then the circuit design, modeling and implementation of a high voltage envelope amplifier is discussed in Section 3.3. High voltage ET power amplifier system measurement results are presented in Section 3.4.

3.2 Design Issues for High Voltage Envelope Amplifier

A more detailed high voltage envelope amplifier circuit topology is shown in Fig. 3.1. Here, ”high voltage” refers to having the maximum output voltage from the amplifier higher than 30 V. In order to reach the goal, several circuit implementation issues have to be resolved. The first question lies in which device technology we should use for building the circuit components. Fig. 3.2 shows, in simulation, that for 48 V peak voltage level, the peak current that the amplifier has to provide is about 8 A for 6 ohm resistive load. This amounts to peak power that the amplifier has to provide is more than 380 W, and the linear stage in this case has to provide up to 6 A peak current as well. Due to the fact that high voltage envelope amplifier requires high frequency response as well as being exercised over a large voltage and current range at the maxi-

mum power levels, fully integrated IC technology would be difficult to provide such a solution with wide bandwidth. Therefore, a hybrid printed circuit board (PCB) implementation of the amplifier which utilizes advantages of different device technologies, such as CMOS, VDMOS, LDMOS, BJT, Schottky diode, and optical couplers has been developed. However, off-the-shelf devices may not provide exact solutions to match with amplifier performance requirements. Particularly, the driver inside the linear stage (Fig. 3.1) is required to provide wideband performance with high slew-rate ($>$ 1000 V/μsec) in large dynamic ranges (50 V peak to peak) such that the device is not easily available [45, 46, 47]; therefore, a customized design for the driver inside the linear stage has to be implemented. Table 3.1 summarizes the design specification for the envelope amplifier, including dynamic range, power handling capability, band-width and efficiency performance.

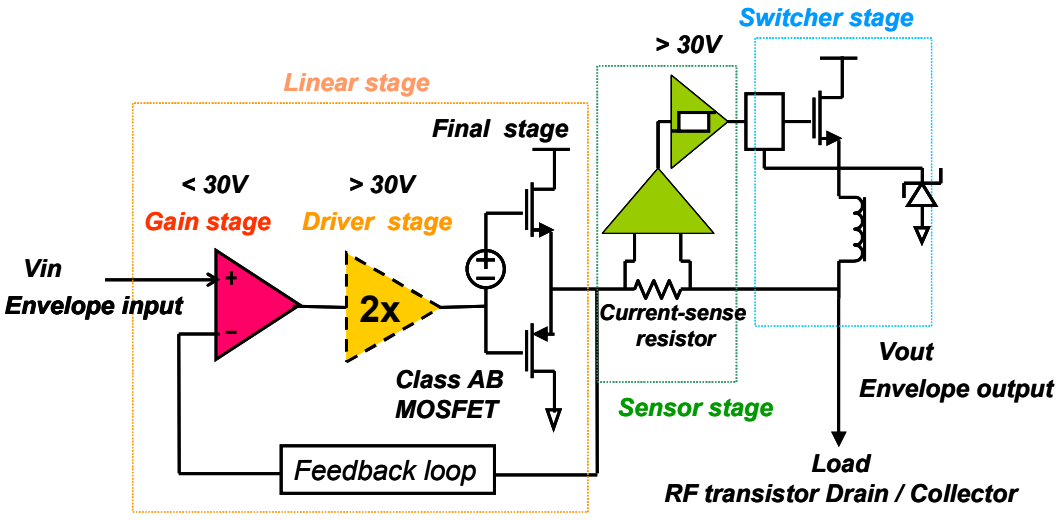


Figure 3.1: High Voltage Envelope Amplifier Schematic

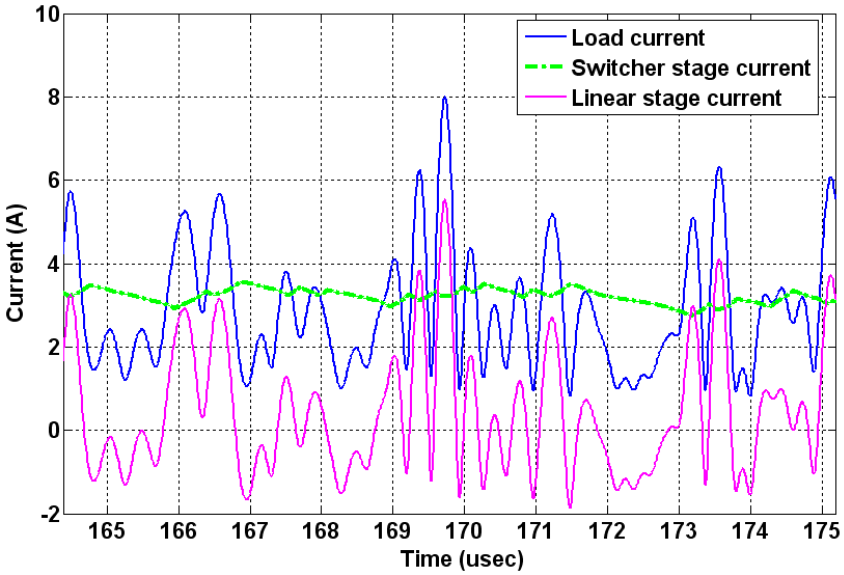


Figure 3.2: High Voltage Envelope Amplifier Simulation

Table 3.1: High Voltage Envelope Amplifier Specifications

Specifications	Range	unit
Output voltage	$3 \sim 45$	Volts
Bandwidth	>20	MHz
Average output power	60	W
Average input power	100	W
Peak output current	10	A
Efficiency	>70	%

3.3 High Voltage Envelope Amplifier Design

High voltage envelope amplifier shown in Fig. 3.1 comprises a high voltage linear stage, a high voltage switcher stage and a high voltage wideband current-sense stage. A high voltage linear stage requires techniques to ensure high slew-rate, high linearity with good stability all the way down to DC, while maintaining the amplifier high gain performance for low distortion at the desired signal bandwidth. The high voltage linear stage comprises a high speed op-amp as a gain stage, a high voltage op-amp as a driver

and a high voltage buffer as a final stage. The final stage is implemented with high power VDMOS transistors [37, 38, 39] as a source follower pair to supply current to the power amplifier. Because of the bootstrapped characteristics of the source follower, the transistors in the final stage is operating with unity voltage gain and therefore extra high speed performance device is not required. However, the envelope output requires a sizeable voltage gain given by the desired output voltage level divided by the DAC output voltage; therefore a high speed component for the gain and driver stage is necessary due to the gain-bandwidth trade-off. Several off-the-shelf op-amps are listed in Table 3.2. From the lists, THS3001 is chosen for the gain stage due to its high slew rate and wideband performance; however, none of the devices can satisfy the requirements for the high voltage driver stage, which serves to supply larger than 30 V peak to peak absolute voltage with wide-band performance (>20 MHz). Therefore, we developed a high voltage op-amp, the missing component, as the driver stage. A detailed design of the high voltage op-amp will be described in Section 3.3.1 and the high voltage linear stage design will be in Section 3.3.2.

Table 3.2: OP-amp and Key Parameters for the Linear Stage

Part #	Type	Technology	Maximum voltage (V)	Slew rate (V/μsec)	GBP (MHz)	Iout (mA)
THS3001	CF	BJT	33	6500	400	100
OP552	VF	FET	60	200	1	100
PA85	VF	FET	400	1000	10	100
AD811	CF	FET	36	2500	140	100

The current-sense stage mainly detects the linear stage output current by sensing the voltage difference across a small current-sense resistor (Fig. 3.1); sensing current can be positive and negative (Fig. 3.2). For high voltage current-sense stage design, a wide-

band sensor capable of detecting small voltage difference embedded in a large common mode voltage swing is required. A high common-mode rejection ratio (CMRR) difference amplifier is, therefore, used to sense the voltage difference. Table 3.3 summarizes several candidates for such an application. INA146 would be our choice due to its low quiescent current, adjustable gain and high common-mode input voltage range. However, the amplifier's bandwidth for such an application is quite narrow, and it would introduce delay and distortion while dealing with wideband input signals. In order to reduce the distortion, we used a transformer in parallel to assist INA146 to improve the frequency response [48]. Section 3.3.3 describes the design in more detail.

Table 3.3: Difference Amplifier and Key Parameters for the Current-sense Stage

Part #	Input Common-mode Voltage	Gain range	-3B Bandwidth (KHz)	CMRR (dB)	Supply range Vs (V)	Quiescent current (mA)
INA143	$\pm$Vs	10	1500	96	$\pm$15	0.95
INA146	$\pm$100	0.1$\sim$100	50$\sim$500	74$\sim$80	$\pm$18	0.57
AD628	$\pm$120	0.1$\sim$100	600	75	$\pm$15	1.6
AD629	$\pm$270	1	500	90	$\pm$15	1.0

For high voltage switcher stage design, a switching buck converter topology (Fig. 2.11(a)) is adopted for its easy implementation and high efficiency. Selections of switch-FET and Schottky diode for high efficient switcher design are based on the discussion in Section 2.6. Section 3.3.4 describes the circuit implementation in more detail.

3.3.1 Wideband High Voltage Op-Amp Design and Implementation

Op-Amp Design Considerations

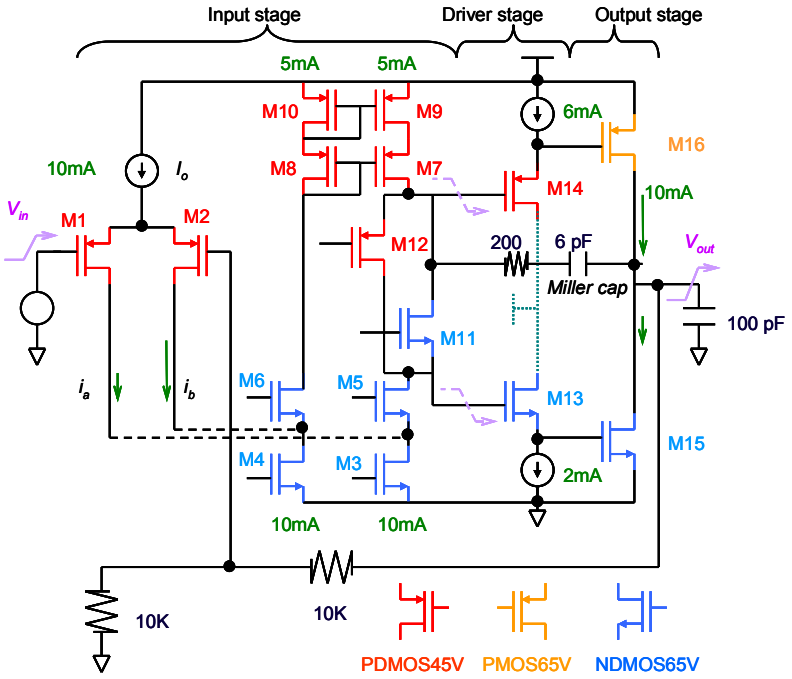
A high voltage op-amp was designed for the driver inside the linear stage shown in Fig. 3.1. Since the load of op-amp is capacitive, the op-amp functions as an operational trans-conductance amplifier (OTA). Table 3.4 summarizes the high voltage OTA design specifications.

Table 3.4: High Voltage OTA Specifications

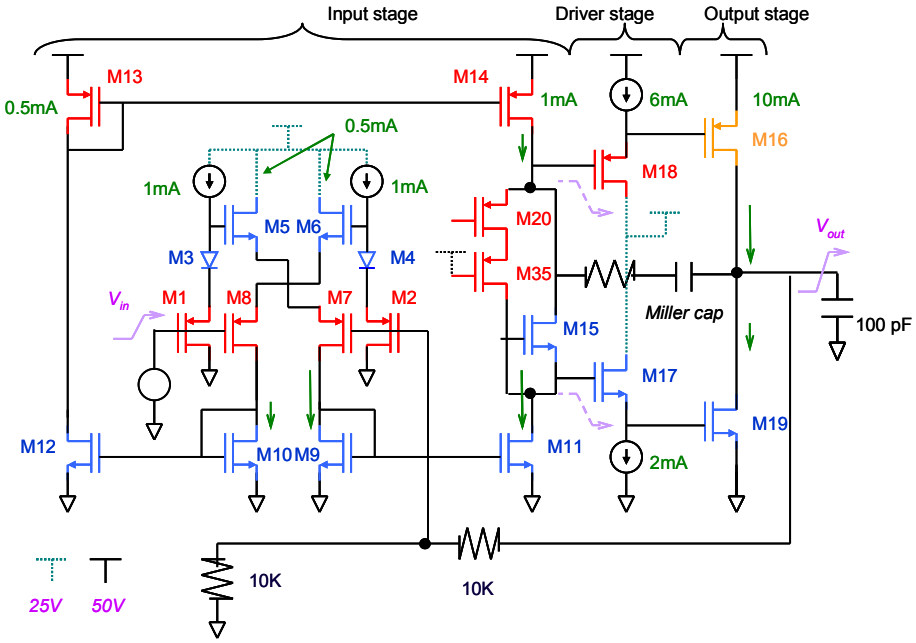
Parameters		units
Supply voltage	> 45	Volts
Unity gain bandwidth	> 30	MHz
Phase-margin	> 45	degree
Closed-loop gain	6	dB
-3 dB bandwidth	> 60	MHz
Slew-rate	> 1000	V/μsec
DC power	< 3	W

Fig. 3.3 shows two different OTA topologies. Both are three-stage OTA designs, which include an input stage, a driver stage and a rail-to-rail output stage. STMicroelectronics high voltage Bipolar-CMOS-DMOS (BCD) 350nm process was used as the device technology. 65 V NDMOS (blue) and 45 V PDMOS (red) were chosen as the major circuit components. For the common-source class AB output stage, a drain extension 65 V PMOS (M16) was used to allow for the high voltage stress on the PMOS device due to high supply voltage rail ($>$ 45 V). Table 3.5 summarizes the device information.

The major difference between two circuits in Fig. 3.3 lies in the input stage architecture. In Fig. 3.3(a), the input stage is a folded-cascode amplifier while in Fig. 3.3(b), the input stage is a source cross-coupled transistor pair [49, 50]. Table 3.6 compares



(a)



(b)

Figure 3.3: High Voltage OTA Toptology: (a) Folded-cascode Input Stage (b) Source Cross-coupled Differential Pairs.

Table 3.5: Device Performance in STMicroelectronics BCD Process

Device	Rail rating (Volts)	f_T (GHz)	V_{th} (Volts)	R_{on} $m\Omega * mm^2$
NDMOSFET65V	65	3.2 $@V_{gs} \approx 1$ V $V_{ds} \approx 25$ V	0.86	133.4 $@V_{gs} = 3.3$ V
PDMOSFET45V	45	3.67 $@V_{gs} \approx$ -1 V $V_{ds} \approx$ -25 V	-0.853	121 $@V_{gs} = 3.3$ V
PMOS65V	65	0.323 $@V_{gs} \approx$ -1.36V $V_{ds} \approx$ -30 V	-1.09	1339 $@V_{gs} = 3.3$ V

two amplifier's simulated performance. The bandwidth and slew rate are quite similar but the amplifier with folded-cascode stage costs more than 1.5 times DC power than the amplifier using source cross-coupled pair. The reason is that drain current of the differential output, i_a and i_b, in the folded-cascode stage (Fig.3.3(a)) is constrained to the magnitude of bias current, I_o [51]. The output current is slew limited for wide dynamic range input signals if the bias current is not properly configured. In this application, I_o is biased up to 10 mA in order to satisfy the internal slew rate requirement of the OTA. The drain current of source cross-coupled pair, on the other hand, is not saturated for the wide dynamic range input signals even though the trans-conductance of this stage is generally lower than that of the folded cascode input stage [52, 53]. In this application, the bias current can be set about 1.5 mA to reduce the input stage bias power consumption. Therefore the overall DC power consumption is lower. To reduce the overall static power consumption inside the linear stage, the amplifier with source cross-coupled pair input stage was designed and implemented in this work.

Table 3.6: Summary of High Voltage OTA Simulation Results

OTA input stage	Folded-cascode	Cross-coupled pairs	units
Supply voltage	50	50	Volts
DC open-loop gain	74	102	dB
Unity gain bandwidth	35	32	MHz
Phase-margin	53	52	degree
Closed-loop gain	6	6	dB
-3dB bandwidth	69	66	MHz
Slew-rate	1650	1525	V/μsec
DC power (SPICE)	2.35	1.41	W

High Voltage OTA Design and Analysis

Fig. 3.4 shows the input stage of high voltage OTA in more detail. With zero differential input, a translinear loop across M1, M3, M5 and M7, together with a bias current supplied through M22 and M23, develop a small class AB quiescent bias current by the gate-to-source voltage drop across M5 and M7. The PDMOSFET pairs, M7 and M8, with cross-coupled source degeneration NDMOSFETs, M5 and M6, transform the input voltage into current. The gate-to-source voltage of both cross-coupled pairs is biased slightly higher than the threshold voltage (Table 3.5) to achieve high efficiency operation. The sizes of M5 and M7 are 25 μm and 50 μm respectively, together with the V_{gs} of both devices biased approximated at 1 V; g_m of both devices is nearly 2 mS. The currents in M7 and M8 are delivered to the output via current mirrors. As V_{in} increases, the sum of V_{gs} of M5(M6) and M7(M8) increases (decreases), and the drain currents $i_{M9}(i_{M10})$ increases (decreases) and gets mirrored into the output device, M11(M14) [50]. The pull-down current, i_{M11}, is directly generated by mirroring M9 to M11. On the other side, the pull-up current, i_{M14} is generated by mirroring the drain current of M10 to the drain of M14 via M12 and M13. Since the current mirror stages require high density (small area) devices in order to reduce parasitic capacitance,

complementary MOS devices are used to replace the high voltage devices (LDMOS) in the current-mirror stages, M9-M14. Moreover, to improve the gain and provide better device matching, 700 nm channel length instead of 350nm CMOS devices are used. In addition, M21 (65 V NDMOS) is inserted between M12 and M13 to reduce the rail-to-rail voltage stress on the CMOS devices.

Fig. 3.5 shows another half of the circuits, including the driver and output stages. A floating bias, composed of M15, M20 and M35, is placed between M11 and M14 to bias the class AB output stage [54]. M35 is biased through a fixed output voltage and mainly used to reduce the voltage stress of M20. The biasing of M16 and M19 is therefore controlled by two translinear loops, M16, M18, M20, M30, M28, M26 and M19, M17, M15, M25, M27, M29, respectively, producing a well-defined quiescent current [55]. The translinear loop is biased for rail-to-rail operation and the maximum output voltage swing is limited to R_{on} of the output stage devices. To match the output slew rate requirement, the biasing of M16 and M19 is set to about 10 mA (with the capability of pulling current up to 150 mA to drive 100 pF output capacitance), and therefore the size of M16 and M19 is rather large (8 mm for M16 and 4 mm for M19). The driver stages, composed of M17, M18 (with the size of 1.6 mm and 0.4 mm), and M31-M34, are biased at 6 mA and 2 mA, respectively to source and sink the ac current, which drives M19 and M16. To reduce the power consumption and voltage stress of M17 and M18, the drain of two devices are connected together and supplied by an external voltage source with the value roughly set at half of the rail-to-rail voltage supply.

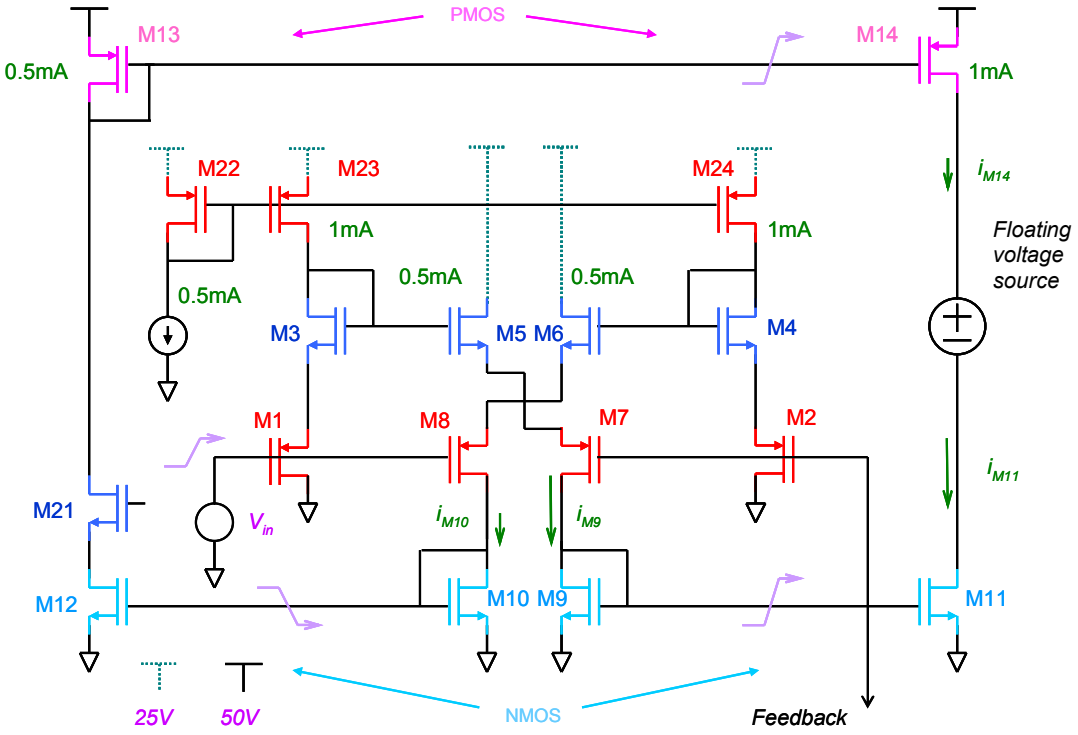


Figure 3.4: High Voltage OTA Cross-couple Input Stage

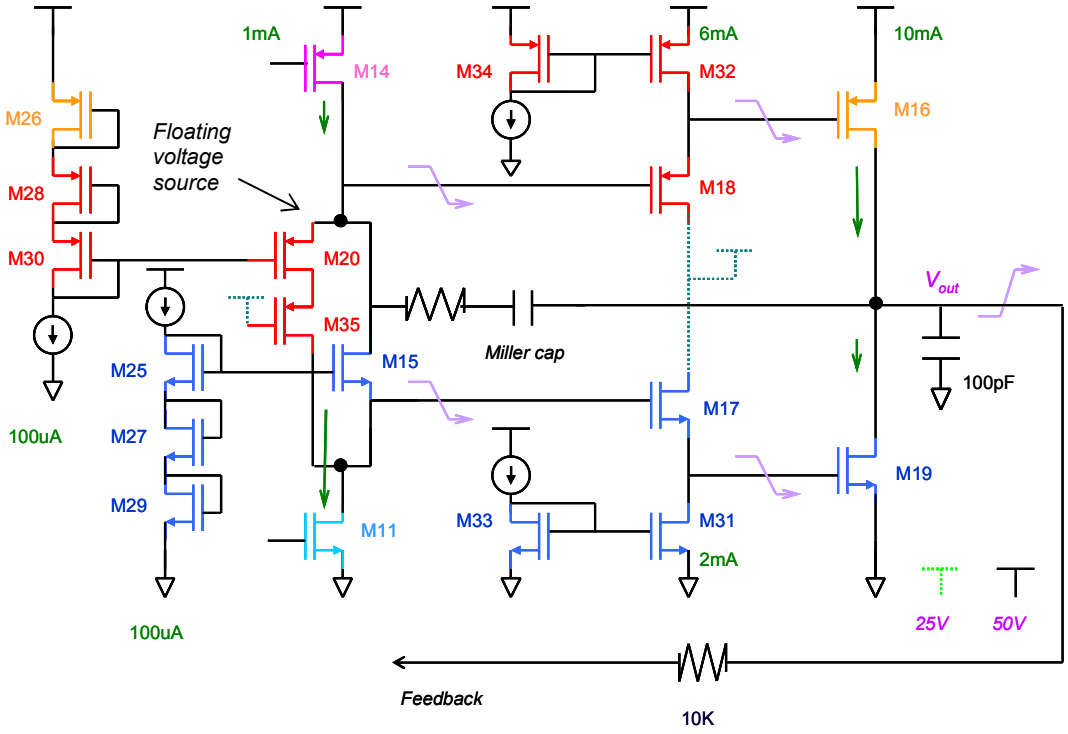


Figure 3.5: High Voltage OTA Driver and Output Stage

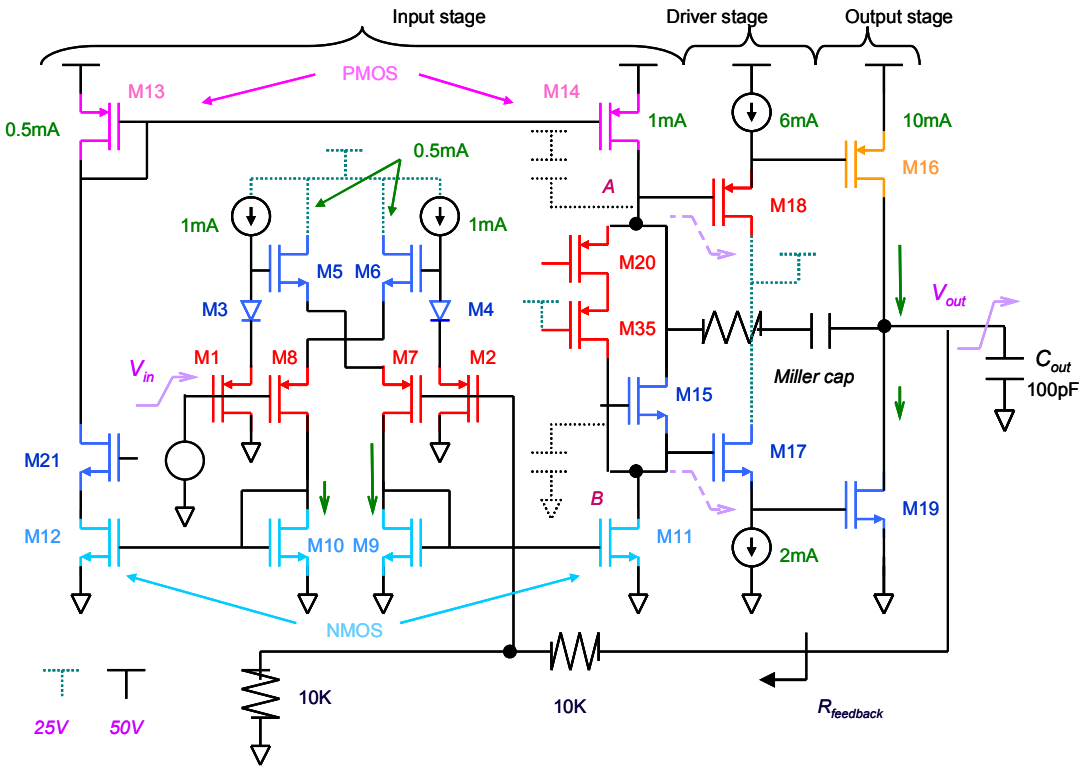


Figure 3.6: High Voltage OTA Full Schematic

High Voltage OTA Simulation and Measurement

Fig. 3.6 shows the high voltage OTA schematic. The open loop DC gain can be estimated as follows:

$$A_v \approx [\frac{g_{m8}}{(1+\frac{g_{m8}}{g_{m6}})} \cdot \frac{W_{m12}}{W_{m10}} \cdot \frac{W_{m14}}{W_{m13}} \cdot r_A \cdot g_{m16} + \frac{g_{m7}}{(1+\frac{g_{m7}}{g_{m5}})} \cdot \frac{W_{m11}}{W_{m9}} \cdot r_B \cdot g_{m19}] \cdot R_{out} \tag{3.1a}$$

where $R_{out} \approx r_{o16} \parallel r_{o19} \parallel R_{feedback}$ (3.1b)

$r_{A,B}$ is total resistance around node A and B

g_{mX} is the transconductance of transistor MX

W_{mX} is the width of transistor MX

The dominant pole is at the output node, expressed in (3.2). The non-dominant pole, which limits the unity-gain frequency of OTA, is at floating voltage source nodes, A and B, due to their high impedances. Therefore, a Miller capacitance is used to compensate OTA between the floating voltage source and output node. Fig. 3.7 shows the simulated loop gain of OTA. The closed-loop unit-gain frequency is around 32 MHz with 52 degree phase margin. Fig. 3.8 shows the simulated frequency response of OTA. The gain is 6 dB and exhibits larger than 65 MHz bandwidth (at -3 dB).

$$p_d \approx R_{out} \cdot C_{out} \tag{3.2}$$

For envelope tracking applications, the slew rate is an important factor which influences the accuracy of the envelope signal, especially at peak voltage. Fig. 3.9 shows

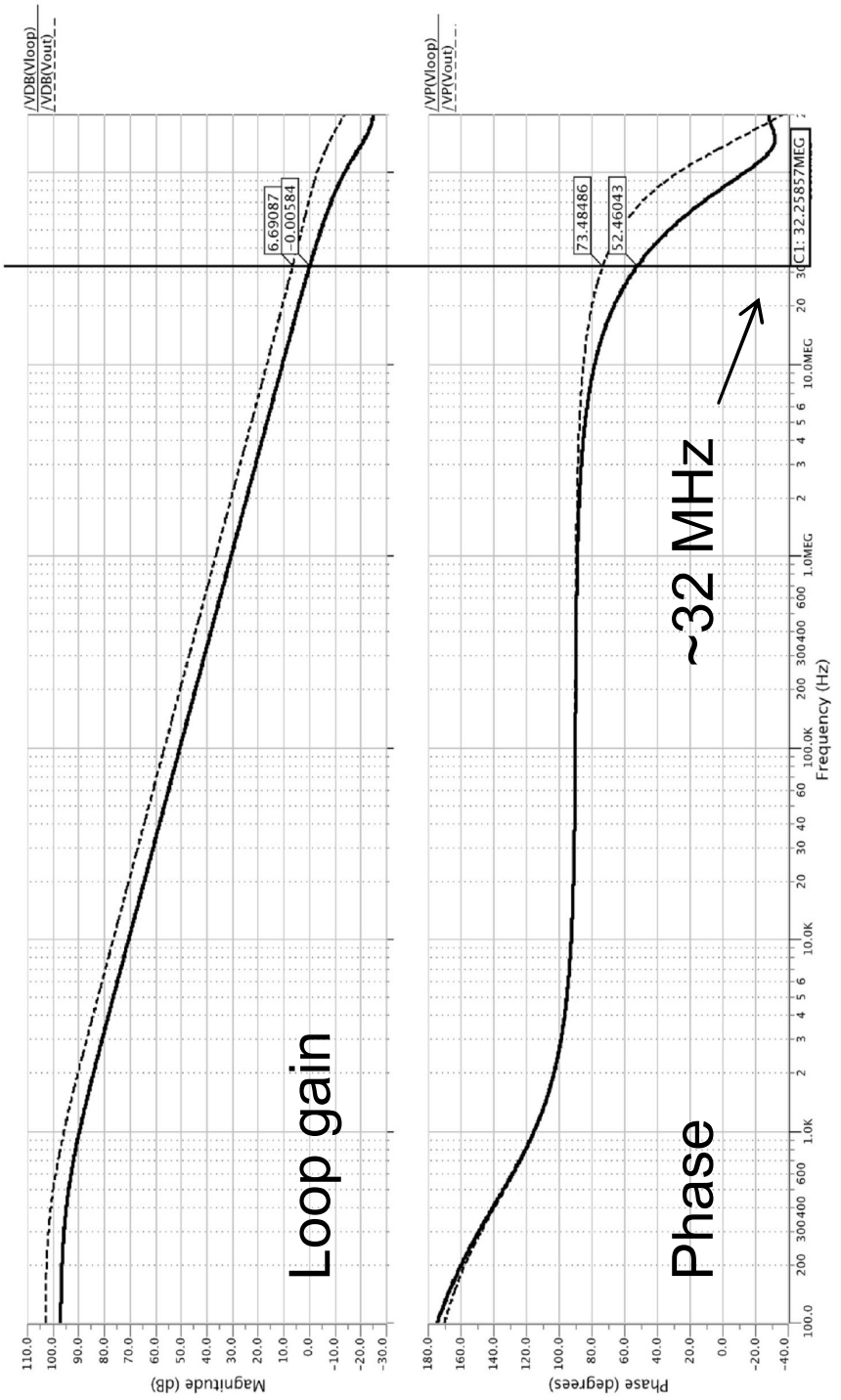


Figure 3.7: High Voltage OTA Loop Gain

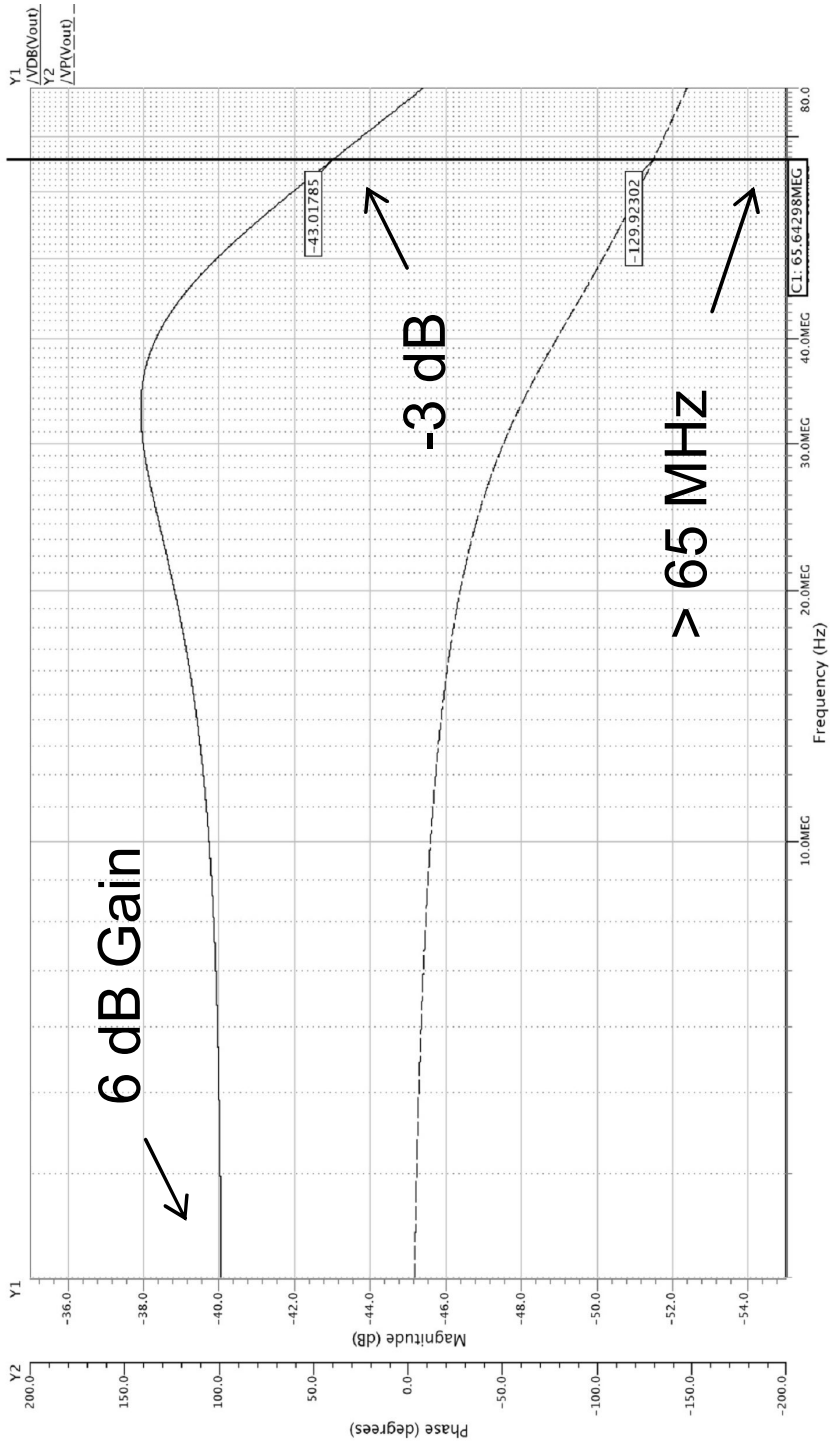


Figure 3.8: High Voltage OTA Frequency Response

the transient step simulation of OTA with 100 pF load at output. The slew rate is around 1200$\sim$1525 V/μsec. A large signal transient simulation conducted by using a W-CDMA signal is shown in Fig. 3.10. After doing time alignment of V_{out} and V_{in}, the error signal can be calculated by (3.3). Fig. 3.11 shows the error signal power spectrum density. The normalized root-mean-square error NRMSE) is about 0.6%.

$$Error(t) = \frac{V_{in}(t)}{RMS(V_{in}(t))} - \frac{V_{out}(t)}{RMS(V_{out}(t))} \tag{3.3a}$$

$$NRMSE = RMS(Error(t)) \tag{3.3b}$$

Fig. 3.12 shows the OTA full chip layout. The total area of the OTA, including ESD protection circuitry, is 1450 μm $\times$ 1150 μm. PowerSO-20 was used for the chip package. The performance of the OTA was measured stand-alone on a custom designed PCB board. Fig. 3.13 shows the test fixture and the packaged OTA. Fig. 3.14 shows the transient step measurement of the OTA. The output is attenuated by matching to 50 ohm. The measured slew rate is about 1175 V/μsec. Table 3.7 summarizes the measurement performance.

Table 3.7: Summary of high voltage OTA measurement results

Supply voltage	48	Volts
-3dB bandwidth	63	MHz
Slew-rate	1175	V/μsec
DC power	1.81	W

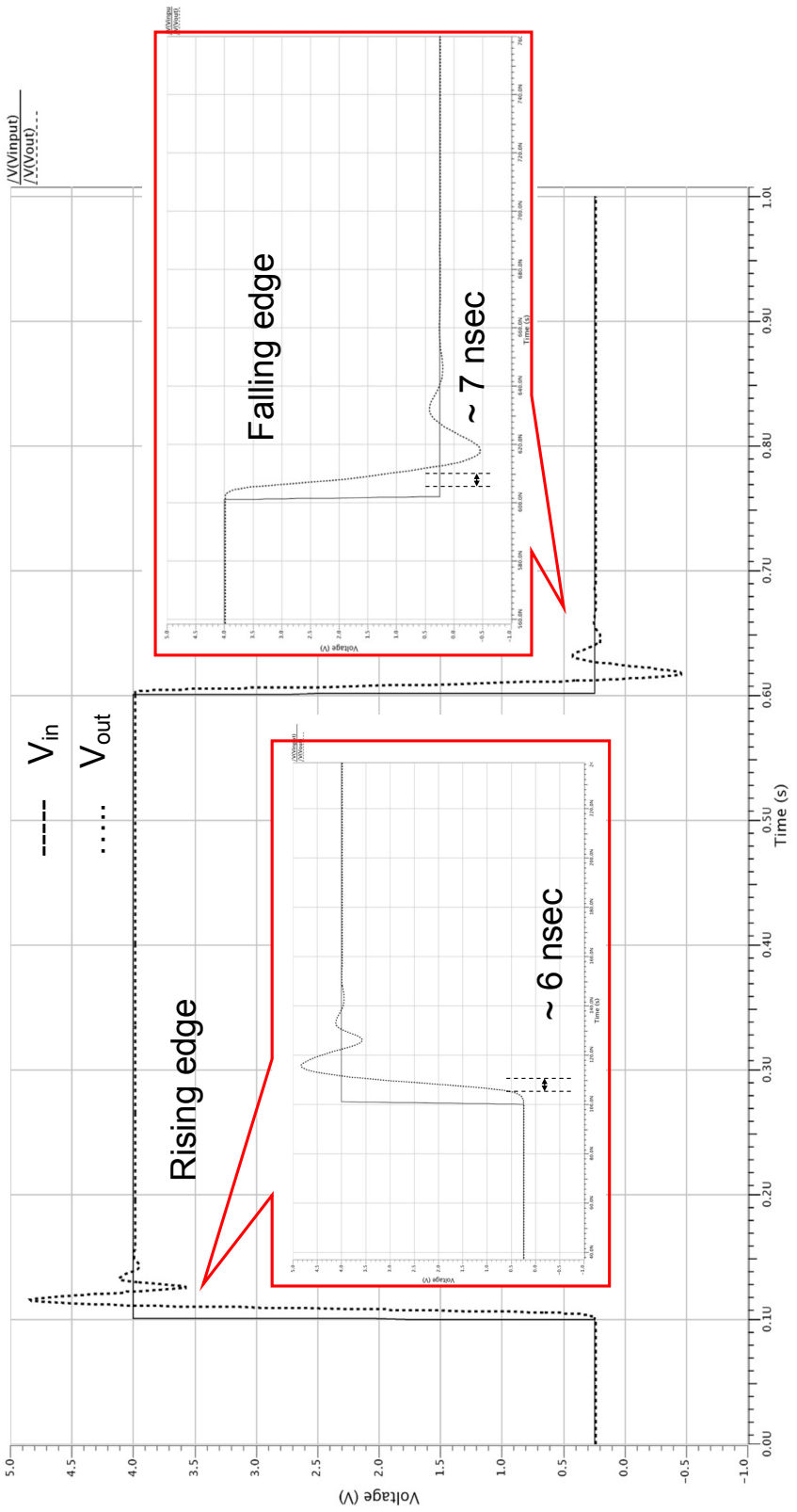


Figure 3.9: High Voltage OTA Transient Step Simulation

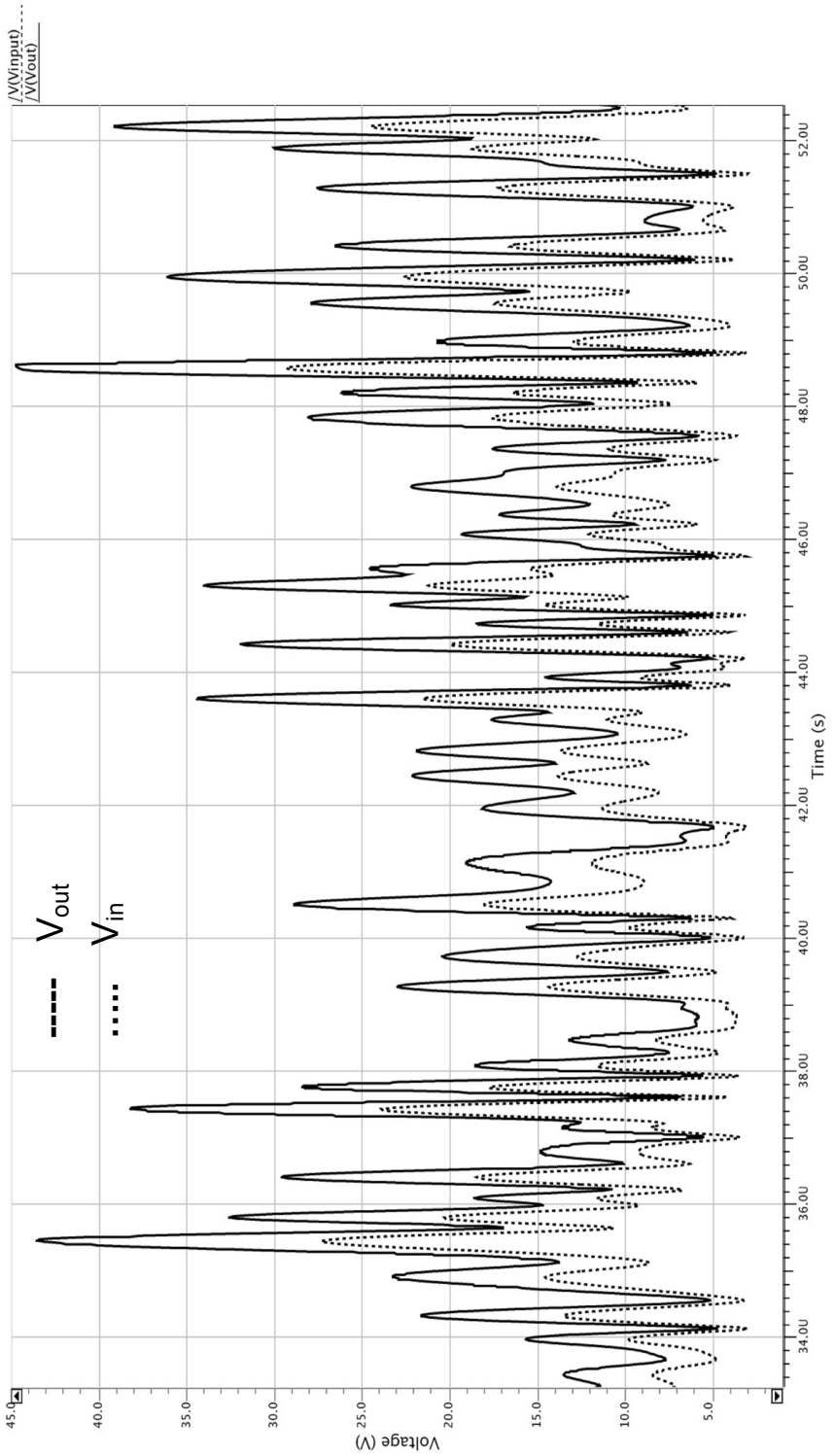


Figure 3.10: High Voltage OTA Transient Simulation using a 7.7 dB PAR W-CDMA Signal

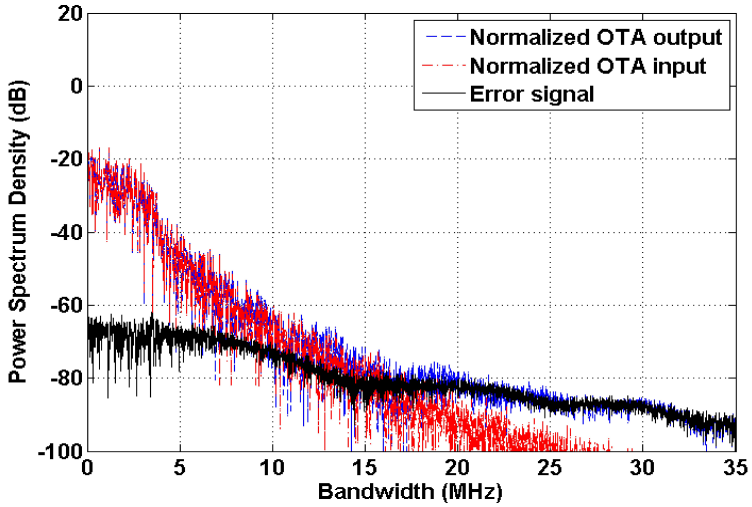


Figure 3.11: High Voltage OTA Transient Simulation Input/Output Comparisons

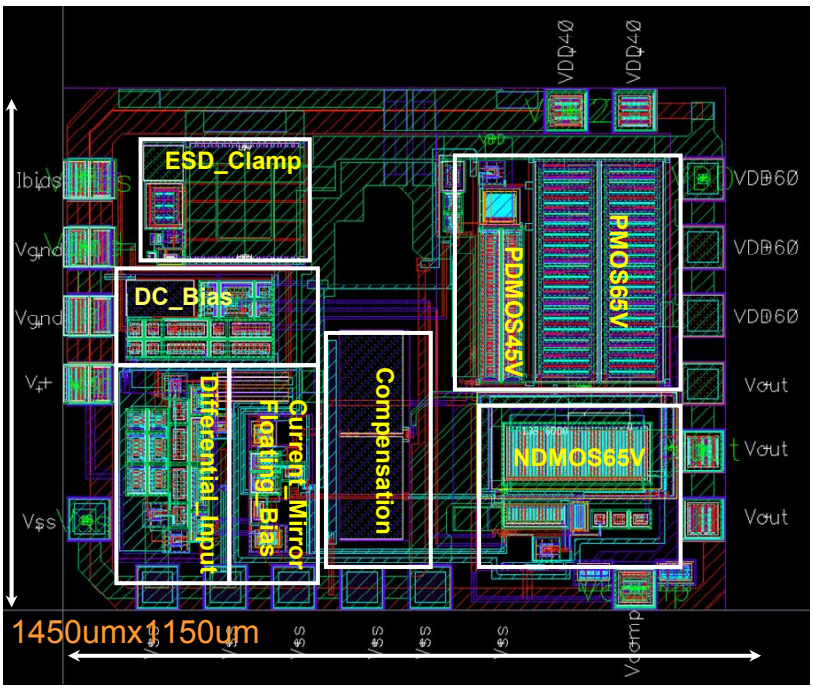


Figure 3.12: High Voltage OTA Layout

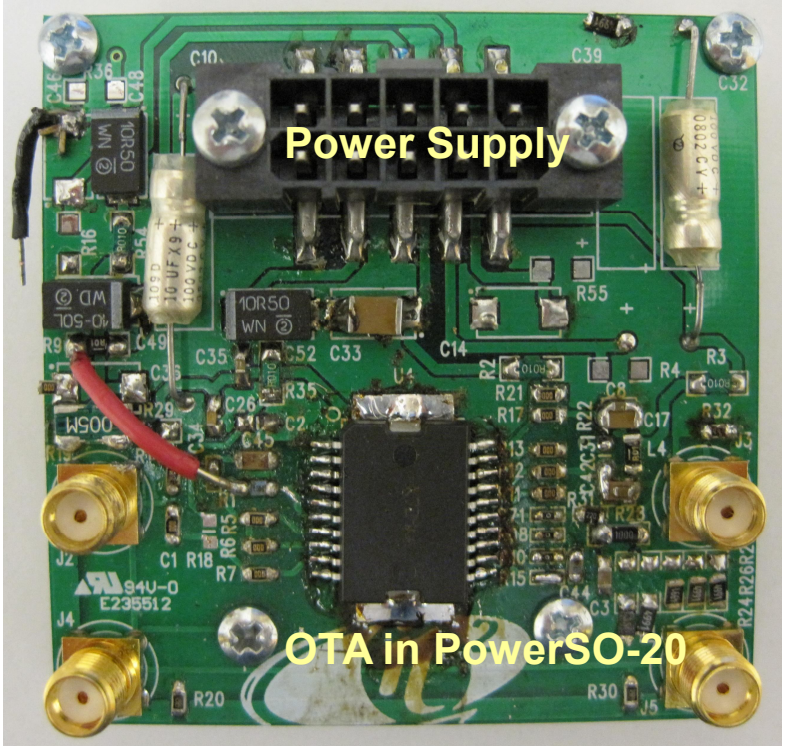


Figure 3.13: High Voltage OTA Package and Test Fixture

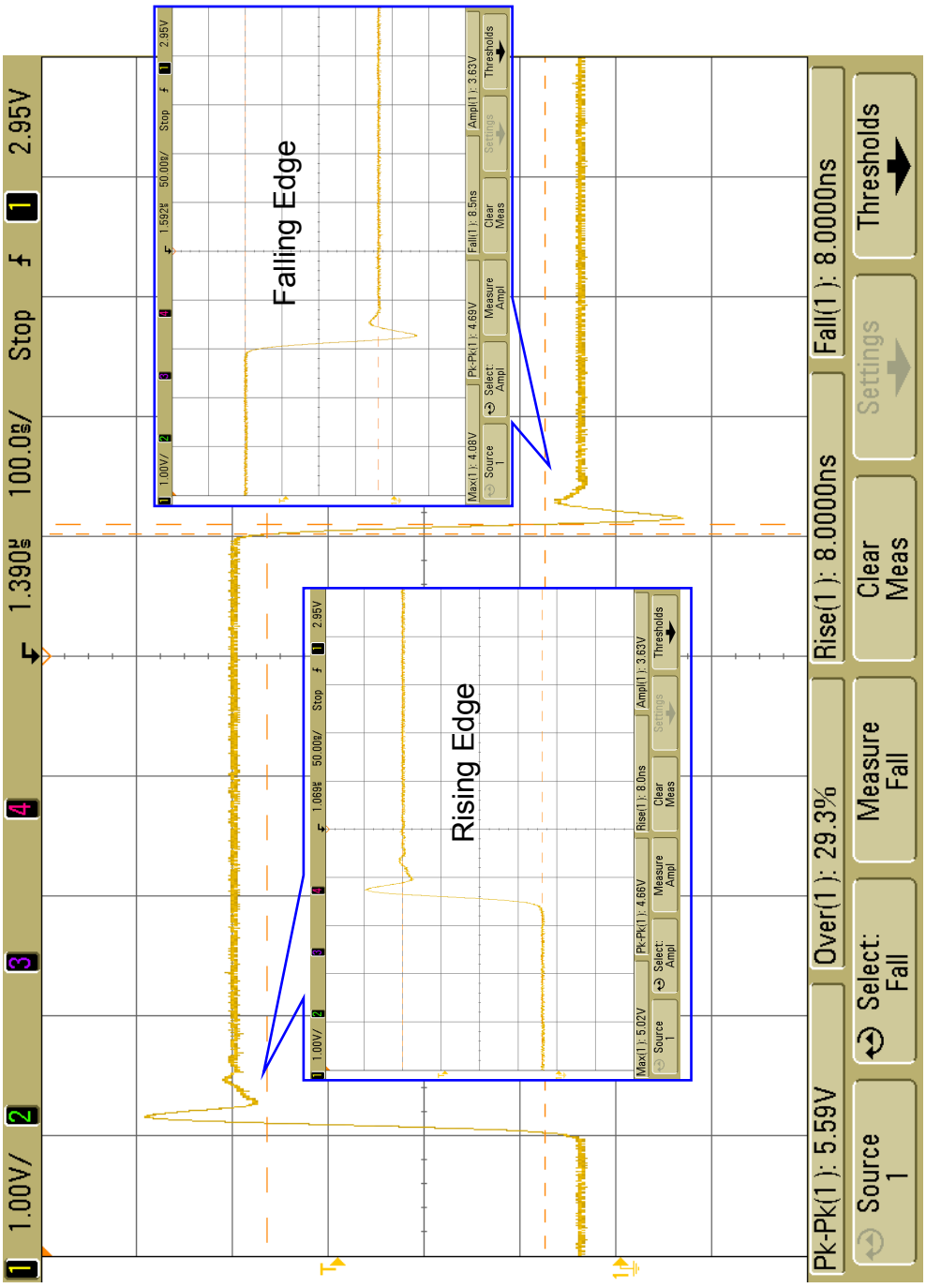


Figure 3.14: High Voltage OTA Transient Step Measurement

From the measurement results, the frequency response shows lower than the simulation results. One of the reasons is under-estimation of the capacitance at the floating voltage source node. Fig. 3.15 shows the simulated results with an added parallel pseudo-capacitance at the node A and B in Fig. 3.6. The bandwidth of the OTA decreases with the added pseudo-capacitance in the simulation. The simulation matches to the experimental result while the capacitance is set around 5 pF.

3.3.2 Wideband High Voltage Linear Stage

Fig. 3.16 shows the high voltage linear stage schematic; it is a linear amplifier which includes three cascade stages, which include a gain stage, a driver stage, a final stage, and a feedback network. The gain stage utilizes THS3001 current-feedback op-amp for its wide bandwidth and high slew rate capability. The driver stage uses the high voltage OTA developed in Section 3.3.1. Due to the fact that peak current supplied from the linear stage is up to 6 A (Fig. 3.2), a power MOSFET source follower pair, which is implemented by using SUD15N06 [56] and FDD5614P [57] transistors, is used as a final stage to supply current to output load. A floating constant current voltage source, $I_b \cdot R_5$, is used to bias the final stage in class AB mode. A nested Miller compensation network (dual-feedback) [58] is used to stablize the linear stage. The network is functioned as a cross-over passive filter. The gain of linear stage, together with design of the filter cut-off frequency, is shown in (3.4). The high frequency noise and disturbances from the switcher can therefore be attenuated by the exterior filter with cut-off frequency of $\frac{1}{R_1 \cdot C_1}$. The delay in the feedback path due to the exterior filter is compensated by the interior high pass filter, which comprises C_2 and R_4. The filter is functioned as a feed-forward phase compensation network. R_6 is used to attenuate the system loop gain if necessary.

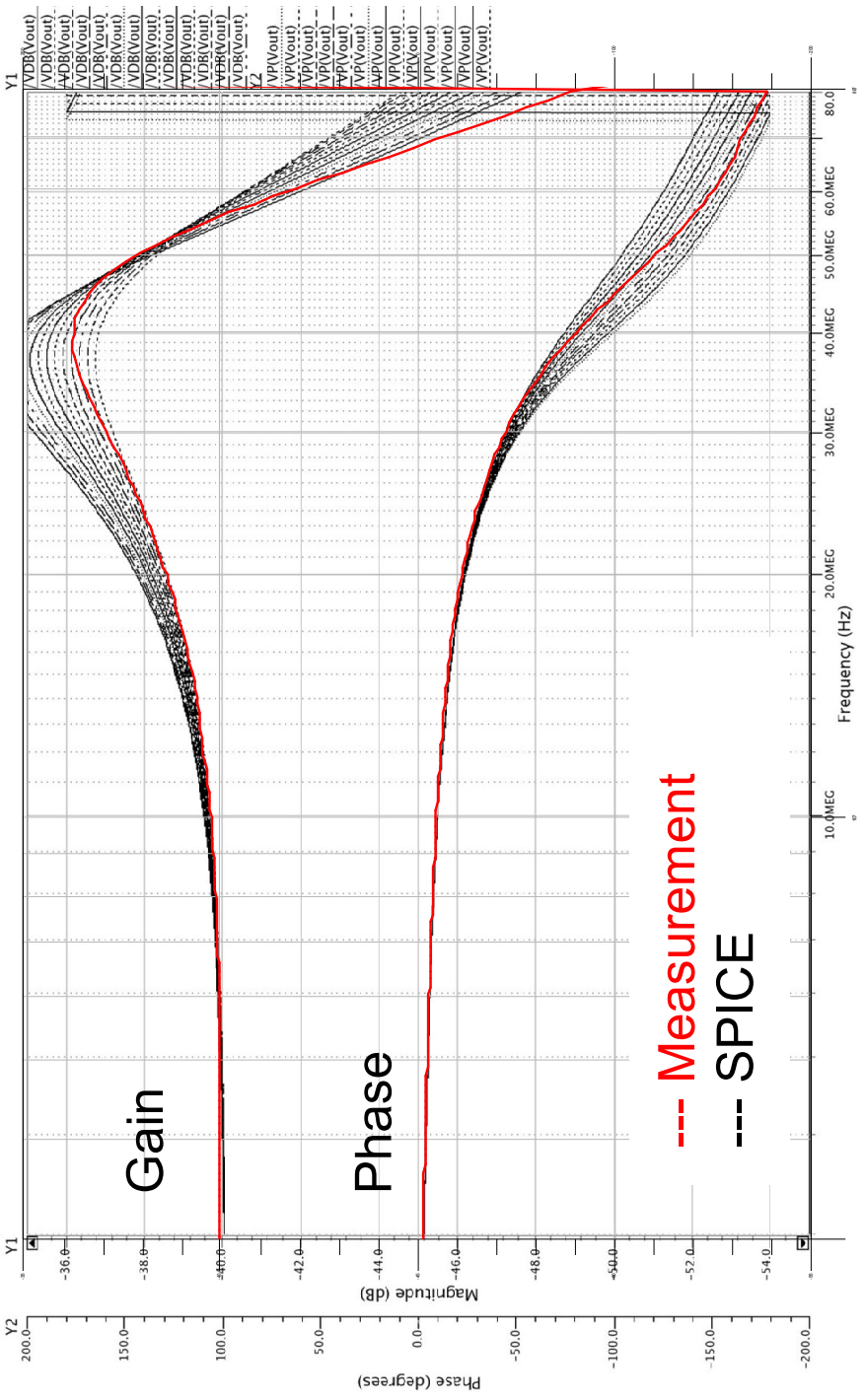


Figure 3.15: High Voltage OTA Frequency Response: Measurement versus Simulation

Fig. 3.17 shows the measured frequency response of high voltage linear stage. 24 dB gain is achieved with larger than 30 MHz bandwidth (at -3 dB).

$$\text{At low band:} \quad A_v = 1 + \frac{R_1 + R_2}{R_3} \tag{3.4a}$$

$$\text{At high band:} \quad A_v = 1 + \frac{R_4 + R_2 \parallel R_3}{R_2 \parallel R_3} \tag{3.4b}$$

$$\text{Cut-off frequency:} \quad \frac{1}{R_1 \cdot C_1} \approx \frac{1}{C_2 \cdot R_4} \tag{3.4c}$$

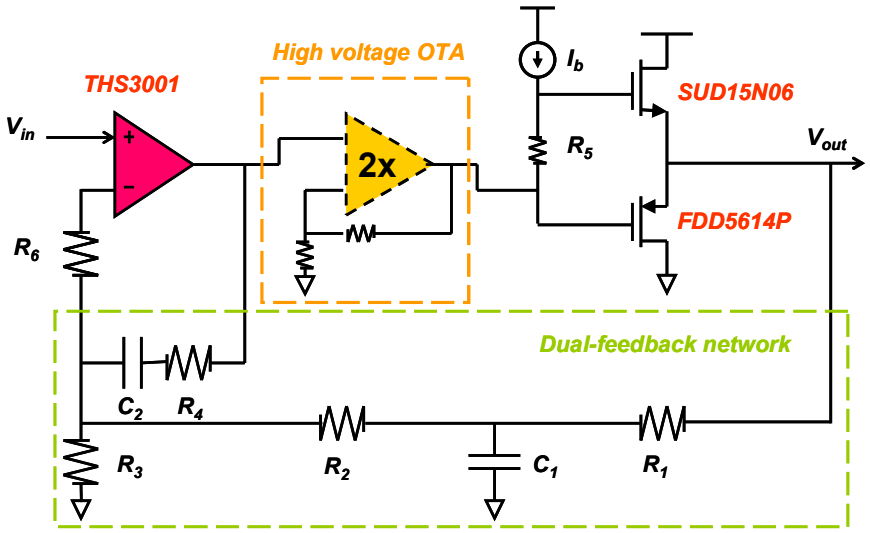


Figure 3.16: High Voltage Linear Stage Schematic

3.3.3 Wideband High Voltage Sensor Stage

A precision difference amplifier can be applied to sense current flowing through a resistance between two electrical nodes. However, the devices are generally narrow-band [59, 60]. For envelope amplifier applications, the current with larger than several MHz bandwidth (Fig. 3.2) has to be detected at the linear stage output. In order

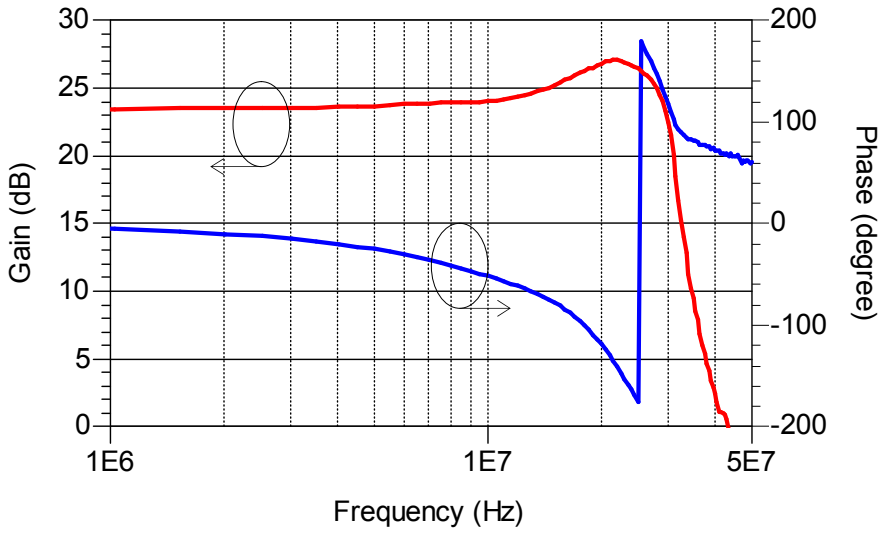


Figure 3.17: Measured High Voltage Linear Stage Frequency Response

to acquire high frequency information, a transformer assisted difference amplifier is used [48]. Fig. 3.18 shows the current-sense stage schematic. The transformer, T_2, is paralleled with the difference amplifier to reject high common-mode voltage, and sense high band signals through a small resistor, R_{sense}. The difference amplifier, on the other side, is used to sense low band signals. A common-mode filter, implemented by using T_1, R_7, R_8, C_3 and C_4, is used to reject high frequency and high common-mode signal before going into the difference amplifier. R_6, C_5 and cut-off frequency, f_d, of the filter outside the difference amplifier are properly set in order to generate a flat cross-over frequency response across the high band and low band signal path. The cross-over frequency, which is about 30 KHz, is set by the characteristics of magnetic cores used for the transformer. Fig. 3.19 shows the simulated differential gain response of current-sense stage. The overall frequency response is better than using the difference amplifier alone. Fig. 3.20 shows the simulated CMRR of current-sense stage. Compared to the performance of standalone difference amplifier, CMRR of the current-sense stage can

reach a wider frequency range.

The combination of high band and low band signals should be proportional to the voltage difference across the current-sense resistor regardless of the envelope output voltage swing. In order to verify the results, Fig. 3.18 indicates the measurement setup, in which the high voltage linear stage is used to drive a nominal load impedance in series with a current-sense resistor. The sensed current, i_{sense} is amplified to generate the current-sense voltage, V_{sense}. Fig. 3.21 shows the corresponding measurement results. V_{sense} is linearly dependent on the average load current, $\langle V_{out}/R_{load} \rangle$, for different magnitudes of output signal, V_{out}, from the linear stage.

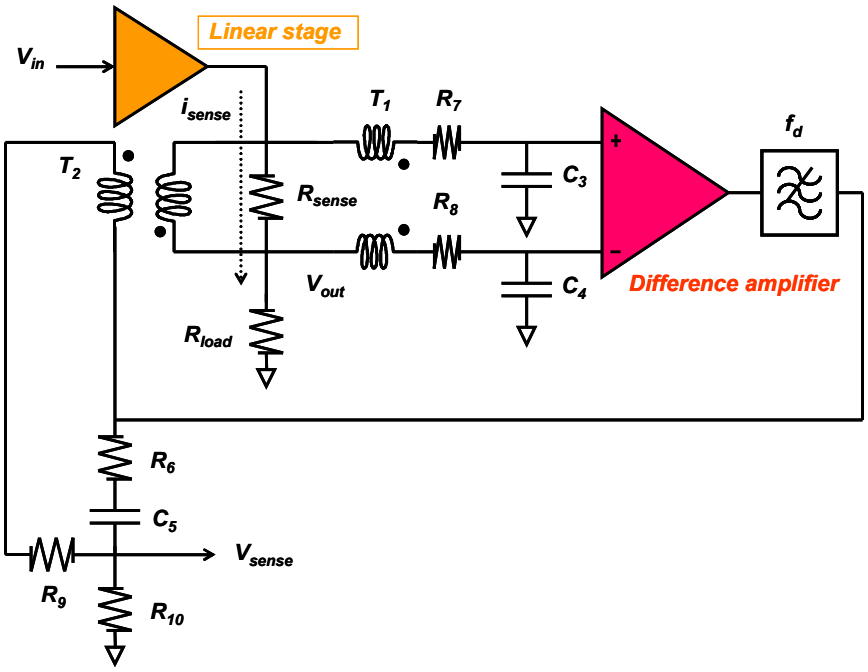


Figure 3.18: High Voltage Current-sense Stage Schematic

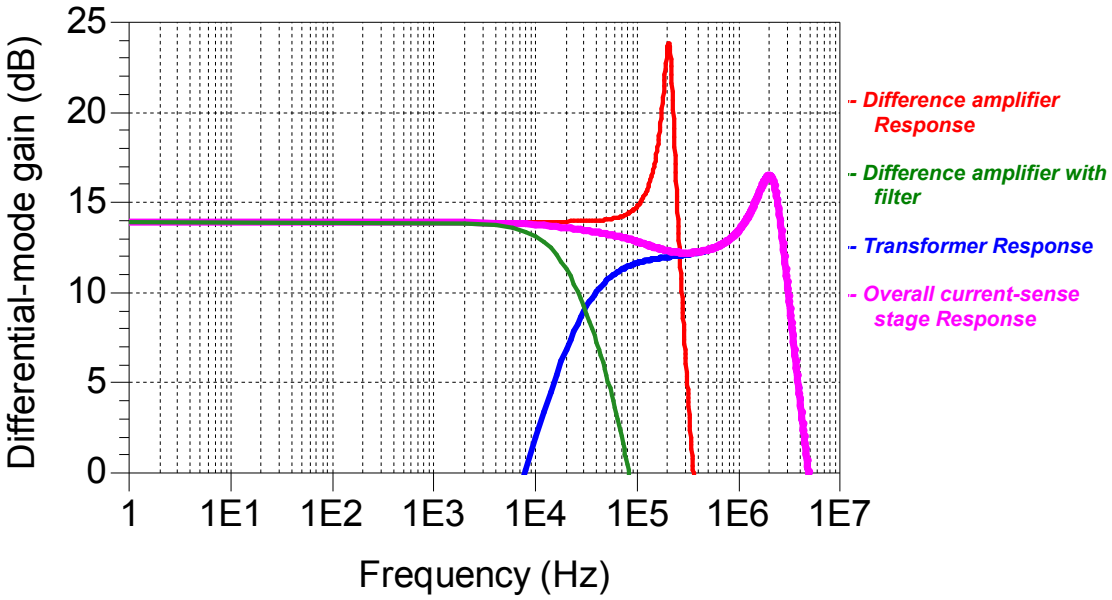


Figure 3.19: Simulated High Voltage Current-sense Stage Differential Gain

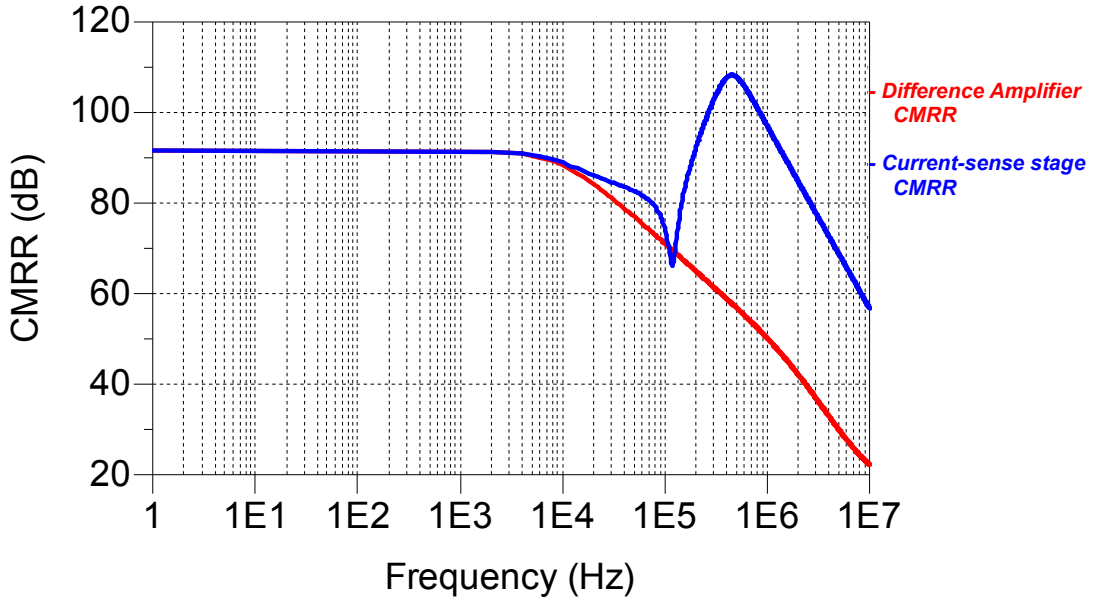


Figure 3.20: Simulated High Voltage Current-sense Stage CMRR

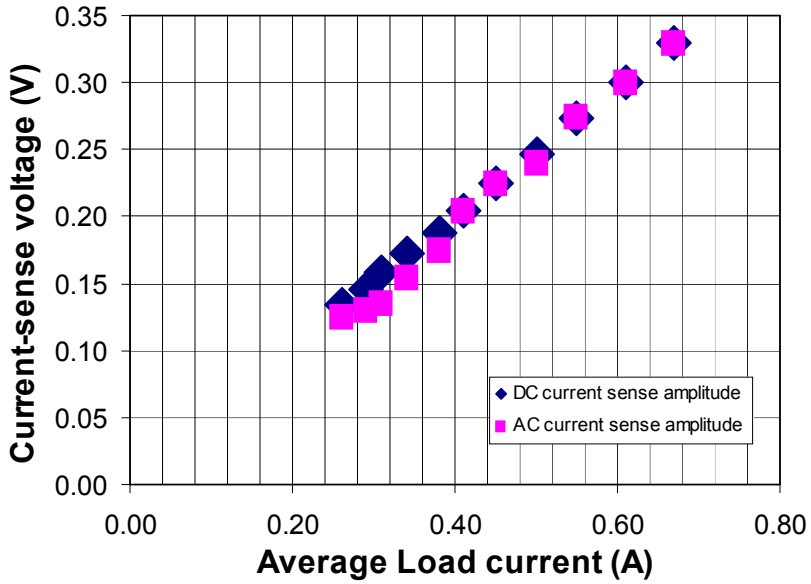


Figure 3.21: Measured High Voltage Current-sense Stage Performance

3.3.4 High Voltage Switcher Stage

Fig. 3.22 shows a more detailed high voltage switcher stage schematic, including a comparator, a high-side switcher driver, a switching MOSFET, a Schottky diode and a power inductor. For comparator design, a high speed, low power comparator, MAX9203, is used [61]. To avoid un-necessary switching noise, a 50 mV hysteresis is added externally. A digital isolator, ISO7221M, is used to isolate the high-side switcher driver from the comparator output [62]. A roughly 10$\sim$20 nsec propagation delay was observed from the measurement. For high-side switcher driver design, an important feature of the driver is its current driving capability. Since the total gate charge of switch-FET is around 20$\sim$30 nC, the driver current has to supply 4$\sim$6 A in order to drive the gate voltage within 5 nsec. To reduce the rising and falling time of the driver, three MOSFET drivers are paralleled together to drive the switch-FET. In addition, the high side driver requires a charge storage capacitor (C_b) and a Schottky diode (D_b) to

form a bootstrapped circuit as shown in Fig. 3.22. The bootstrap capacitor must have a voltage rating that is able to handle the maximum supply voltage, V_{DC} plus a boosted drive voltage ($\sim$5 V). The capacitance is determined using (3.5) [63]:

$$C_b = \frac{Q_G}{V_{droop}} \tag{3.5}$$

Where Q_G is the total gate charge of the selected switch-FET and V_{droop} is the voltage droop allowed on V_{drive}.

The bootstrap Schottky diode, D_b in Fig. 3.22, must have a minimum V_{drive} rating to withstand the maximum boosted supply voltage. The average forward current, I_F can be estimated by (3.6) [63]:

$$I_F = Q_G \cdot f_{max} \tag{3.6}$$

Where f_{max} is the maximum switching frequency of the high-side driver.

Table 3.8 lists several switch-FETs [37, 38, 39]. Based on the discussions in Section 2.6, SUD23N06 for its low gate charge (short rise/fall time) and low gate resistance was chosen even though its on-resistance is little higher than others. As for Schottky diode, Table 3.9 lists several possible candidates as well [64]. UPS3100 was selected based on its low capacitance and low forward voltage.

Fig. 3.23 shows the measured performance of high voltage switcher for high voltage envelope amplifier applications. The experiment was conducted by using periodic pulse signals with roughly 40% duty ratio as input, load equal to 6 ohm, which is similar to RF device output load impedance. The switcher efficiency is over 80%

Table 3.8: Tabulated Switch-FET Candidates for High Voltage Switcher Stage

Parameters	Symbol	SUD23N06	SUD50N06	IRLR2705	IRLR2405	FDD5612	FQD20N06
Drain-to-source (V)	V_{DS}	60	60	55	55	60	60
Switch-on resistance (mohm)	R_{on}	37	7	51	12	42	63
Miller charge (nC)	Q_{GD}	3	20	14	19	3	4.5
@ V_{GS} (V)		4.5	10	5	10	10	10
Gate resistance (ohm)	R_G	1.6	1.5	6.5	6.8	6	25

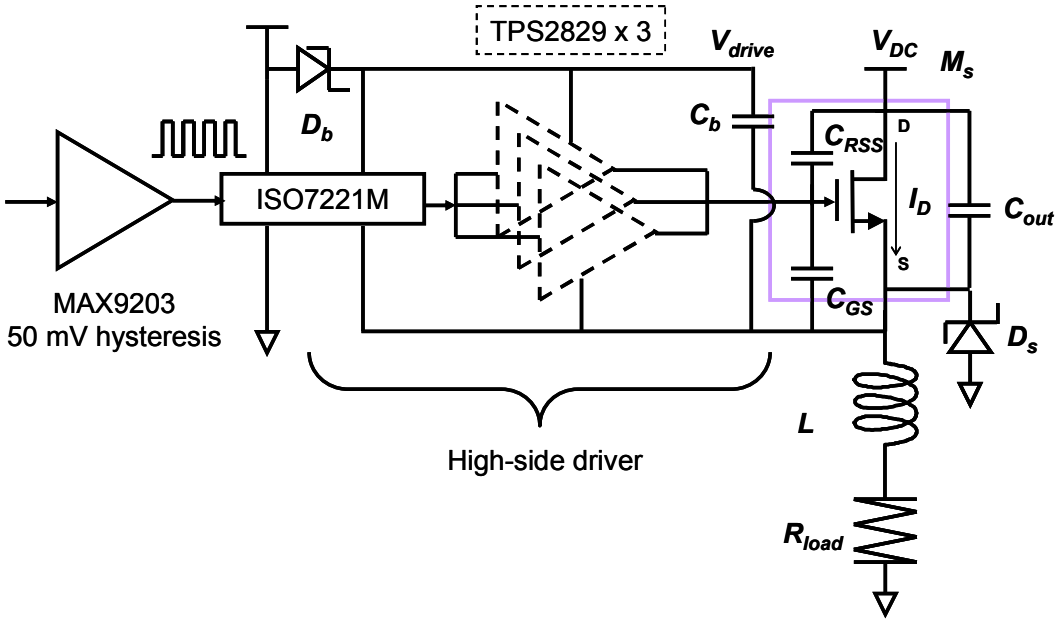


Figure 3.22: High Voltage Switcher Full Schematic

Table 3.9: Tabulated Schottky Diode Candidates for High Voltage Switcher Stage

Parameters	Symbol	UPS5100	UPS3100	UPS560
Reverse voltage (V)	V_R	70	70	60
Average output current (A)	I_o	5	3	5
Forward voltage (V)	V_F	0.5∼0.7	0.5∼0.7	0.5∼0.7
Capacitance (pF)	C_T	150	85	150

between 1∼3 MHz switching frequency with 65∼70 W average output power.

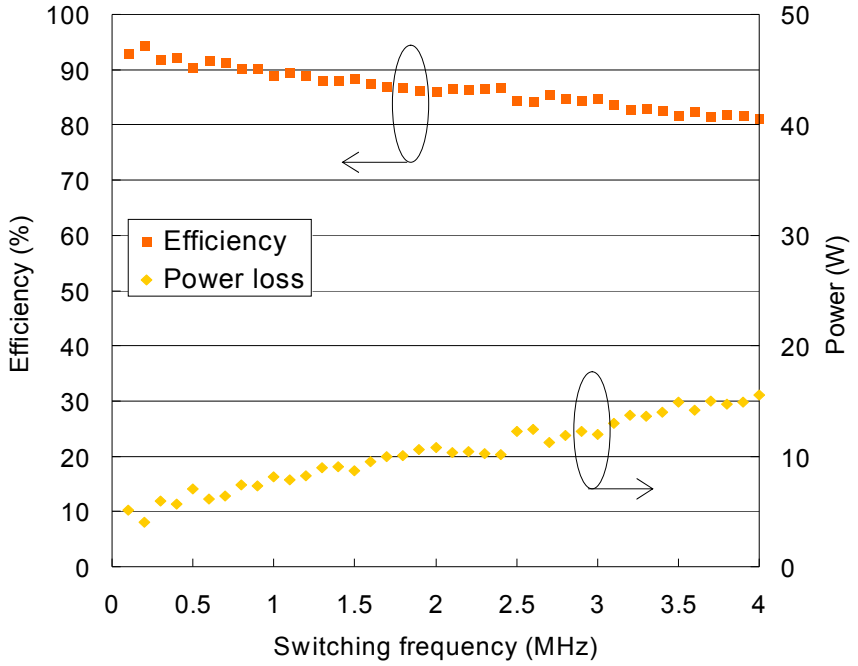


Figure 3.23: Measured High Voltage Switcher Efficiency and Power Loss

3.4 High Voltage ET PA Experimental Results

3.4.1 High Voltage Envelope Amplifier Measurement

A high voltage envelope amplifier was assembled on a single PCB board. Fig. 3.24 shows the picture of the amplifier. The PCB board with 2 o.z. copper enables the amplifier to provide more than 60 W average output power. The amplifier was tested using a 7.7 dB PAR W-CDMA signal with a 6 ohm resistive load for efficiency and accuracy verification. The output envelope waveform is time-aligned and compared with the input to generate the error signal by (3.3). Fig. 3.25 shows the measured normalized power spectrum of input and output envelope and associated error signal. The NRMSE is about

1.5%. The RMS of envelope voltage is about 18.5 V, and efficiency is approximately 73% with 57.5 W output power. Fig. 3.26(a) shows the recorded waveform from the experiments; top trace represents the output envelope voltage, and associated switching pulses are shown in the bottom trace. Fig. 3.26(b) shows the comparable simulated results using the same W-CDMA signal. Fig. 3.27 shows the normalized switching frequency distribution. Switching frequency is between 500 KHz to 6 MHz, and centered around 2 MHz. Table 3.10 summarizes the overall performance of high voltage envelope amplifier.

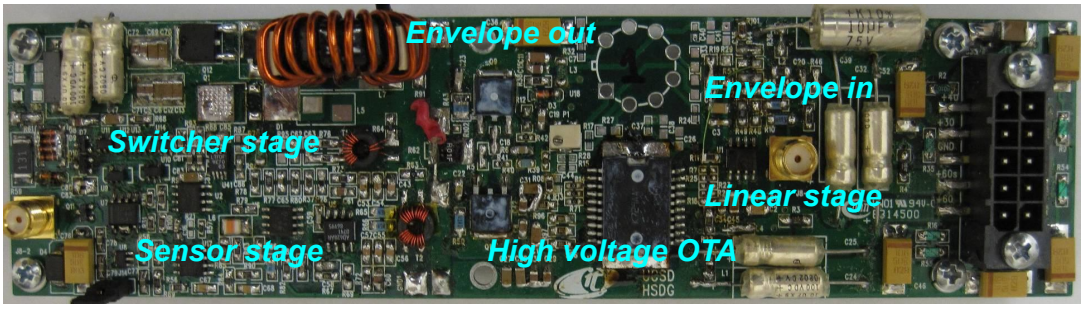


Figure 3.24: High Voltage Envelope Amplifier

Table 3.10: Summary of High Voltage Envelope Amplifier Performance

Supply voltage	48	Volts
Dynamic range	$3 \sim 45$	Volts
Voltage gain	24	dB
Bandwidth	> 30	MHz
Average output power	> 60	W
Average input DC power	> 100	W
Peak output current	10	A
Switching frequency	$0.5 \sim 6$	MHz
Efficiency	> 70	%

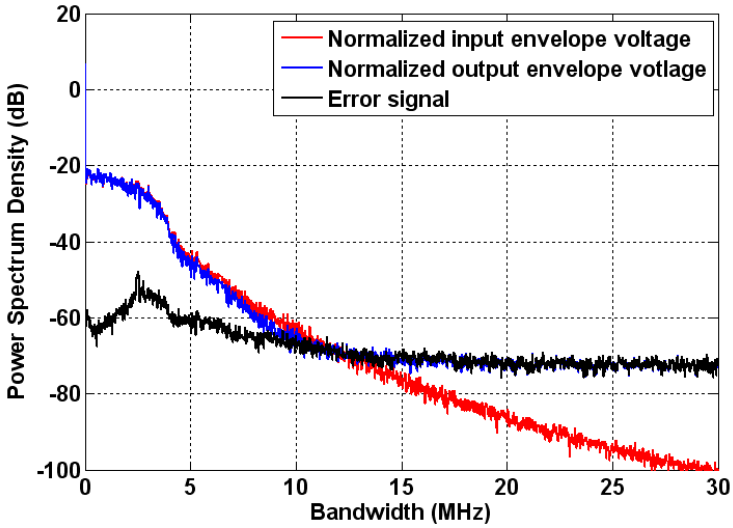


Figure 3.25: High Voltage Envelope Amplifier Output versus Input Signal Spectrum (W-CDMA)

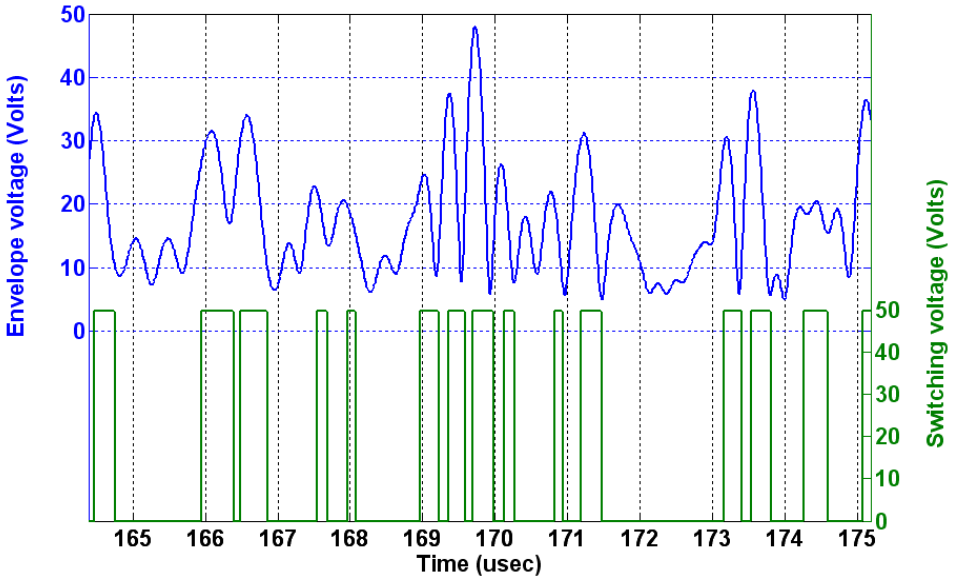
3.4.2 High Voltage Envelope Tracking Power Amplifier Measurement

RF Transistor Characteristics

A GaN-HEMT-based RF transistor, EGN21A090IV-A, which was fabricated by Eudyna Corp. (now - Sumitomo Electronic Device Innovations) high voltage GaN-HEMT process, is used as a RF stage for demonstration of high voltage envelope tracking power amplifier. The GaN-HEMT power amplifier is biased in class AB mode. The device has internal pre-match circuits which allow up to 100 W CW output (50 dBm) at P-3dB with 50 V constant voltage supply. The device can achieve 42 dBm output power with 33% efficiency [65] for a W-CDMA signal with a constant drain supply voltage (50 V). Table 3.11 summarizes the performance of amplifier under constant drain bias operation.

To apply the RF device in envelope tracking, the amplifier performance was re-

(a)



(b)

Figure 3.26: High Voltage Envelope Amplifier with W-CDMA signal: (a) Measurement; (b) Simulation results

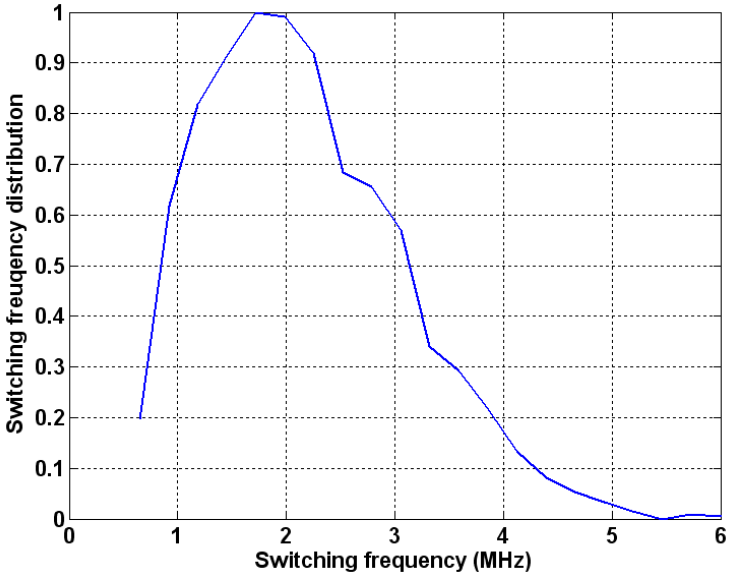


Figure 3.27: High Voltage Envelope Amplifier Switching Frequency Distribution

Table 3.11: Summary of EGN21A090IV/-A Constant Drain Measurement Results

WCDMA BTS	Frequency G(Hz)	P3dB (dBm)	Pout (dBm)	Gain (dB)	η @Pout(%)	IM3 (dBc)
ENG21A090IV	$2.11 \sim 2.17$	50	42	16	33	-33

optimized by tuning the fundamental inside the internal pre-match circuits. The second harmonic tuning was achieved by varying the length of the bias line on the input and output on-board matching circuits [10]. Fig. 3.28 shows the RF power amplifier test fixture and bias line adjustment setup.

ET Power Amplifier Measurement

Two envelope tracking power amplifiers with different dynamic voltage swing (30 V peak versus 45 V peak) were configured for performance comparison. The same RF GaN-HMET transistor was used in the experiment, except that the input and output impedances of RF power amplifier were tuned to achieve the best performance under

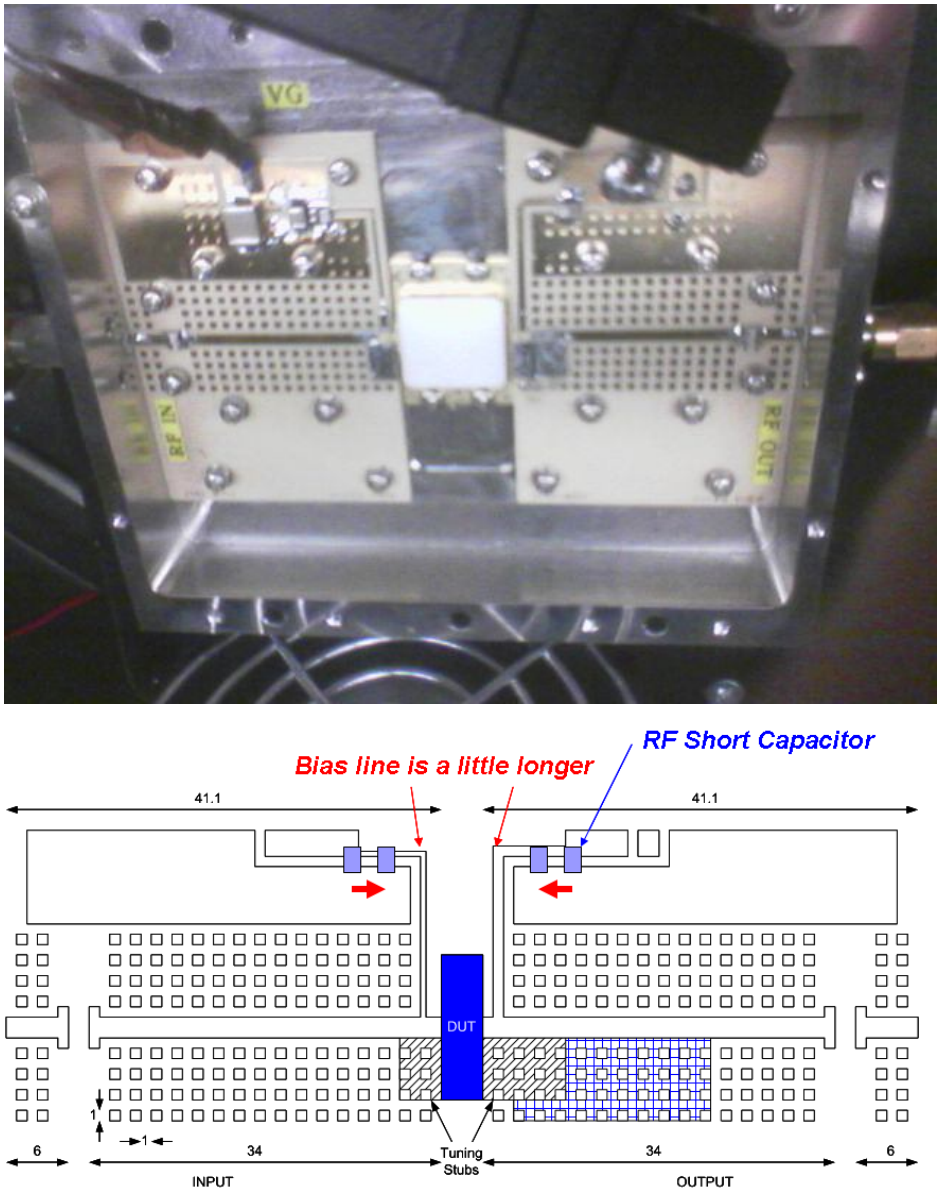


Figure 3.28: Eudyna EGN21A090IV-A Power Amplifier Test Fixture [10]

envelope tracking operation. The envelope tracking power amplifier measurement was carried out together with DPD. The overall measurement system diagram is shown in Fig. 2.1, which includes a digital IF and envelope signal generator, up-converter, down-converter, DAC/ADC, a driver, RF transistor and an envelope amplifier. A W-CDMA signal with 3.84 MHz bandwidth, 7.7 dB PAR is used at 2.14 GHz frequency band throughout the experiments. The RMS value of envelope voltage for 30 V peak signal is around 10$\sim$12 V, and for 45 V peak envelope signal, the RMS voltage is around 18$\sim$20 V.

In order to verify the performance of RF power amplifier itself in two dynamic range envelope tracking power amplifiers, the instantaneous dc voltage and current at output of the envelope amplifier were probed using a high-speed digitizing oscilloscope, as shown in Fig. 3.29, under conditions roughly comparable to those used for best efficiency. Time-delay differences between instantaneous voltage and current waveforms were calibrated to permit accurate calculation of RF power-amplifier characteristics [6].

Fig. 3.30 compares the measured RF power amplifier instantaneous drain efficiency versus dynamic drain voltage with 30 V peak envelope tracking and 45 V peak envelope tracking amplifier by the setup in Fig. 3.29, respectively. The efficiency presented in Fig. 3.30(a) [10] shows around 65% above 12 V to 30 V, while in Fig. 3.30(b), the power amplifier drain efficiency is up to 70% above 20 V to 45 V with 45 V peak envelope tracking amplifier. The RF power amplifier performance is improved for higher dynamic voltage swings. In terms of average efficiency performance, Table. 3.12 summarizes the ET system performance with signals before and after memory-less digital pre-distortion (ML-DPD). For 45 V peak envelope tracking power amplifier, the average drain efficiency (DE) including dissipation in the envelope amplifier, is as high as

50.3% with average output power of 32.1 W. The gain and NRMSE are 13.7 dB and 2.3% after pre-distortion, respectively. The efficiency is significantly improved compared to the measurements results of 30 V peak envelope tracking amplifier, which the maximum drain efficiency is 45%. A 3 dB power gain increase was also obtained with higher operating voltage, along with similar linearity performance. The efficiency improvement for different voltage supply dynamic ranges proves the effect of adjustment of load impedance of RF power amplifier with higher dynamic range power supply in envelope tracking can increase the overall performance.

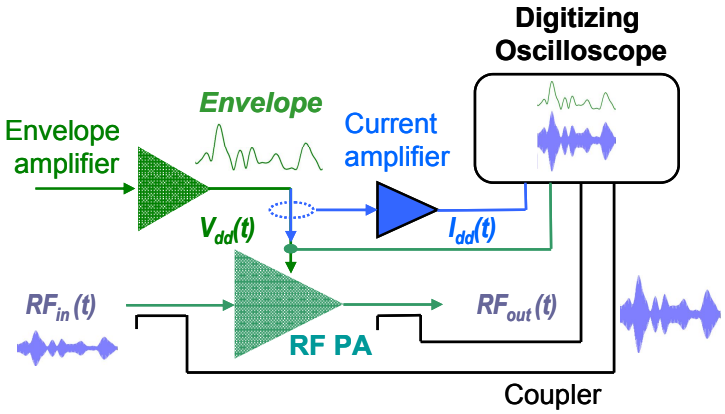
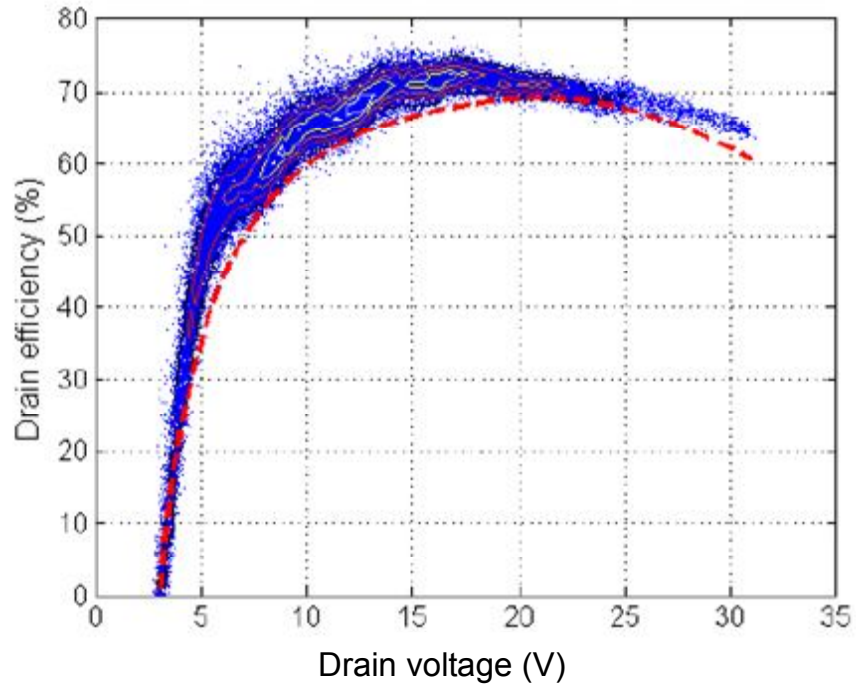


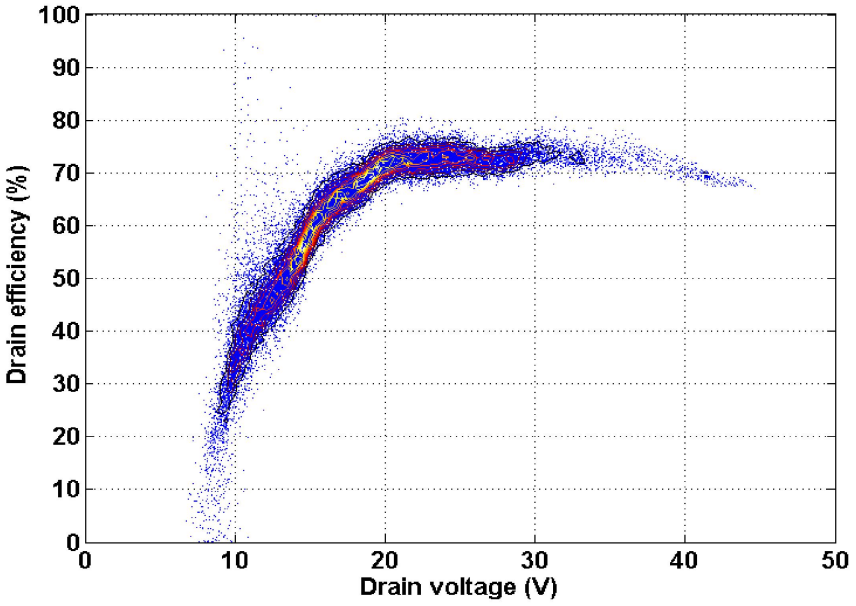
Figure 3.29: Envelope Tracking Power Amplifier Instantaneous Efficiency Measurement Setup [6]

3.5 Summary

A high voltage envelope amplifier for envelope tracking base-station power amplifiers is presented, demonstrating high efficiency and linearity performance. The performance comparison between 45 V peak and 30 V peak envelope tracking power am-



(a)



(b)

Figure 3.30: Envelope Tracking RF Power Amplifier Performance Comparison: (a) 30 V peak Envelope Tracking [10], (b) 45 V peak Envelope Tracking; Test Signal: W-CDMA 7.7 dB PAR

Table 3.12: Summarized Measurement Results of the Two Envelope Tracking Power Amplifiers with Single Carrier W-CDMA Signal Before and After Memory-less Digital Pre-distortion

ET Dynamic Range	DPD	Gain (dB)	Pout (W)	Drain efficiency (%)	PAE (%)	NRMSE (%)	ACP1 (dBc)	ACP2 (dBc)
45 V peak	Before	13.8	31.0	48.6	46.6	25.31	-27.84	-44.84
	After	13.7	32.1	50.3	48.1	2.28	-45.24	-54.59
30 V peak	Before	10.8	18.7	44.3	40.6	31.47	-26.51	-43.45
	After	10.7	19.1	44.8	41.0	3.25	-45.14	-51.69

plifiers using GaN-HEMT devices for base-station applications is described. For 45 V peak ET amplifiers using GaN-HEMT and W-CDMA signals with a PAR of 7.7 dB, an average PAE of 48.1% is achieved, which is 1.17x efficiency improvement compared to the 30 V peak ET amplifiers using the same RF device with similar linearity performance. The results illustrate the potential of the wide dynamic range envelope tracking amplifier in combination with advanced RF device technologies to enhance the base-station ET power amplifier performance.

3.6 Acknowledgements

The author is very grateful to ST Microelectronics for providing foundry service in this work, to Nokia-Siemens Networks for valuable discussions and partial funding support, to Eudyna Corp. (Sumitomo Electric Innovation Devices) for power amplifier test fixture support, and to Mr. Don Kimball, Dr. Calogero Presti, Dr. Antonino Scuderi and Mr. Carmelo Santagati for valuable discussions and suggestions.

Some of the material in Chapter 3 is as it appears in "Effect of Maximum Power Supply Voltage on Envelope Tracking Power Amplifiers Using GaN HEMTs", C. Hsia, D. Kimball, and P. Asbeck, *IEEE Radio Wireless Symposium.,* 2011.(accepted), "Envelope Amplifier Design for Higher Than 50 V Envelope Tracking Applications", C. Hsia, D. Kimball and P. Asbeck, to be submitted to *IEEE Trans.on MTT.,* 2011, and "Envelope Tracking Power Amplifier Efficiency Performance for Different Supply Voltage Dynamic Ranges", C. Hsia, D. Kimball and P. Asbeck, to be submitted to *IEEE Trans.on MTT.,* 2011. The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for these publications.

Chapter 4

Dual-switcher Envelope Amplifier

4.1 Introduction

In previous chapters, envelope amplifier design for envelope tracking power amplifiers has been discussed. The overall efficiency performance of ET power amplifiers has been shown to be advantageous in base-station applications where the output power varies over a wide range (such as found with high PAR signals). The overall efficiency results from factors involving both the RF stage and the envelope amplifier. However, the envelope amplifier efficiency degrades with increasing PAR of the envelope signal as discussed in Section 2.6. To address this problem, in this thesis, a novel envelope amplifier design is proposed and demonstrated. The idea is based on using a smaller value of inductor for the switcher to operate at the same output power level. The reduced L/R time constant helps improve the switcher's output current bandwidth in order to match the slew rate of envelope signal, thereby reducing the linear stage's output current and power consumption. This idea has been realized by designing a novel envelope amplifier based on a digital signal processing (DSP) control dual-switcher architecture discussed in this chapter. DSP is utilized for delay compensation, which can not be easily adjusted

by using an analog controller, and used to generate the switcher control signal in a more efficient way. The control signal generation methodology is discussed in Section 4.2. The dual-switcher envelope amplifier design and measurement results are presented in Section 4.3. The ET power amplifier measurement results are presented in Section 4.4.

4.2 DSP Switcher Control

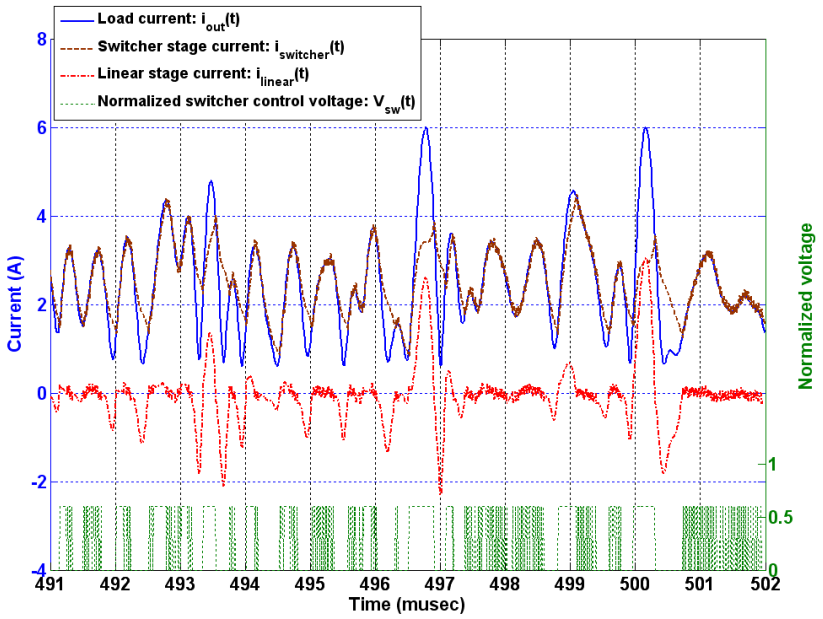
DSP has been widely applied to base station power amplifiers to improve linearity performance [6, 15, 66, 67]. In most instances, DSP is used as means of providing digital pre-distortion at the baseband. Alternatively, DSP can be used to monitor and control other aspects of the amplifier such as the gate bias control of power amplifiers [17]. The idea of using DSP in this section for generating the digital signal, however, is to control the switcher and to enable the switcher to provide more efficient power to the load. The linear stage output current is, therefore, reduced and so also the power consumption because most of envelope power (including high frequency portion) is provided by the switcher.

One of the key challenges in designing the digital control signal for the switcher is how we distribute the current produced between the switcher and the linear stage to maximize the overall efficiency. In general, the control signal can be generated with various types of digital modulation schemes, such as pulse width modulation (PWM) [68, 69], pulse density modulation (PDM) [70], or sigma-delta ($\Sigma\Delta$) modulation [71, 72]. However, the switching frequency of the digital signal generated from such modulation schemes is often very high, which leads to high switching loss and reduces the efficiency.

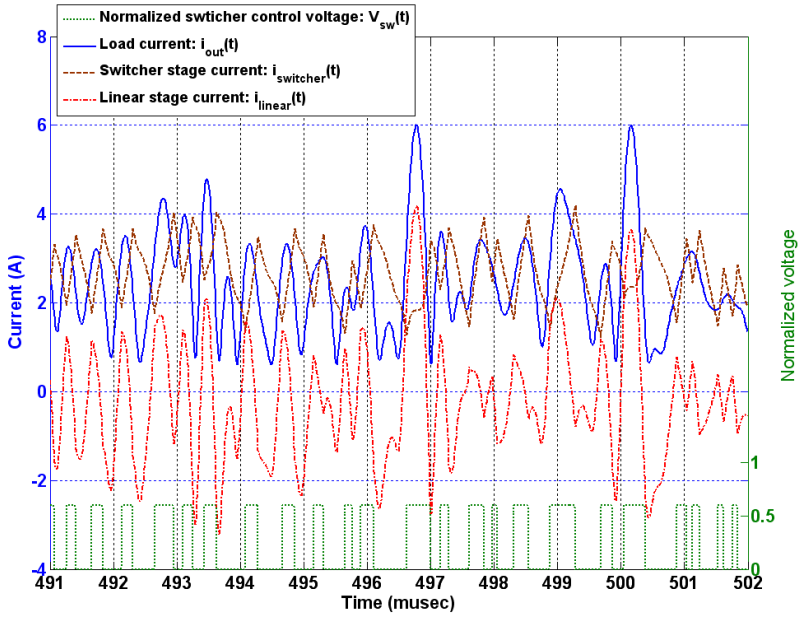
Before we discuss our DSP controller design, we model several scenarios with a smaller value of inductor in the envelope amplifier by utilizing the simulator developed

in Section 2.5. Fig. 4.1 compares two different envelope amplifier's behaviors by modifying the inductance to a 20 times smaller than the case used in Fig. 2.9. In Fig. 4.1(a), the slew rate of the switcher increases because of using the smaller inductor; however, the average switching frequency is much faster than the envelope signal's bandwidth. In this case, the switcher provides the majority of output power (including high frequency portion), which is similar to the case with the envelope amplifier operating EDGE signals in Section 2.5. For the case with EDGE signals shown earlier in Fig. 2.8, the average switching frequency is around 1$\sim$2 MHz; however, for W-CDMA signal, the average switching frequency increases to over 10 MHz, which results in performance degradation of the switcher even though the linear stage's current is minimized. On the other hand, Fig. 4.1(b) shows another simulation result of using a small inductor in the switcher with the same output power. However, the switching frequency is not dramatically increased and the switching patterns are similar to the case in Fig. 2.9. This can be achieved by using a larger hysteresis value in the comparator. In this case, the switcher's slew rate is improved compared to the case in Fig. 2.9 without degrading the efficiency. However, the linear stage's output current magnitude is not reduced compared to Fig. 2.9(b).

From simulation results in Fig. 4.1(b), one observation for reducing the linear stage output current is to align the switcher current with the load current by minimizing the delay between the switcher control signal and envelope signal. In this case, the linear stage output current can be reduced. For analog feedback controller, it would be difficult to do so by adjusting the delay in the feedback loop. However, DSP control can use an external digital control unit in open loop fashion, which provides freedom to compensate any possible delays generated in the analog components, such as



(a)



(b)

Figure 4.1: Simulated Envelope Amplifier Behaviors with 1.3 μH Inductor: (a) Hysteresis: 0.025 V, (b) Hysteresis: 0.5 V; Test Signal: W-CDMA 7.7 dB PAR; Peak Envelope: 30 V; Load: 5 ohm

switcher driver propagation delay, L/R time constant delay as well as any group delay in the amplifier. In this work, we chose to generate the switcher control signal by using a pseudo-hysteretic control approach in digital domain, which emulates the switching signal generation mechanism in the analog hysteretic controller. Fig. 4.2 shows the simulated switcher current aligned with the load current by properly adjusting delay of the control signal in Fig. 4.1(b). In this case, the linear stage output current in Fig. 4.2 is reduced compared to the case in Fig. 4.1(b) and the switching frequencies are similar to each other. Fig. 4.3(a) shows the simulated results of total linear stage dynamic power loss ($P_{losslinear}$ in (2.6)) versus delay adjustment of the switcher control at different output power, and Fig. 4.3(b) shows the average switching frequency variations versus delay adjustment. The linear stage power consumption can be reduced more than 30% with proper delay compensation, and average switching frequency of the switcher increases less than 10%.

Generating the switcher control signal in the digital domain, however, has to incorporate practical circuitry parameters of the switcher. Fig. 4.4 shows the DSP switcher control flow chart. $V_{in}(n)$ is the digitized envelope input signal, A is the ratio of the L/R_{load} of the switcher shown in Fig. 2.4, $V_r(n)$ is the digitized voltage, which is equivalent to the product of load impedance, R_{load}, and inductance current in real circuits, $V_c(n)$ is the digital switcher control pulse, and D is the unit delay. To compensate the delay in the hysteretic controller, Dh, and switcher driver delay, T_d in the real circuits, instead of using the present envelope waveform, we use the future envelope samples as the reference to generate the switching pulse, which is possible because of the open loop configuration. As shown in Fig. 4.4, assuming the number of delay samples is k, h

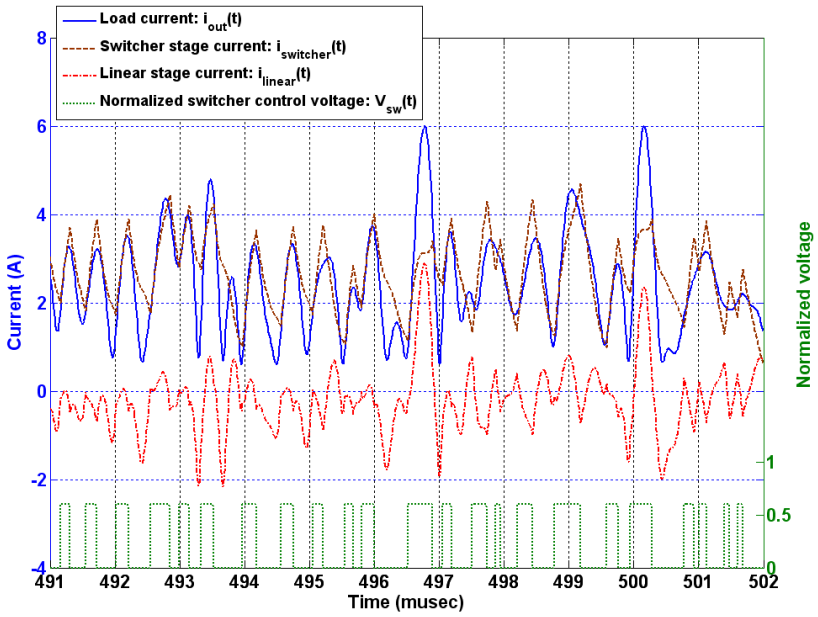


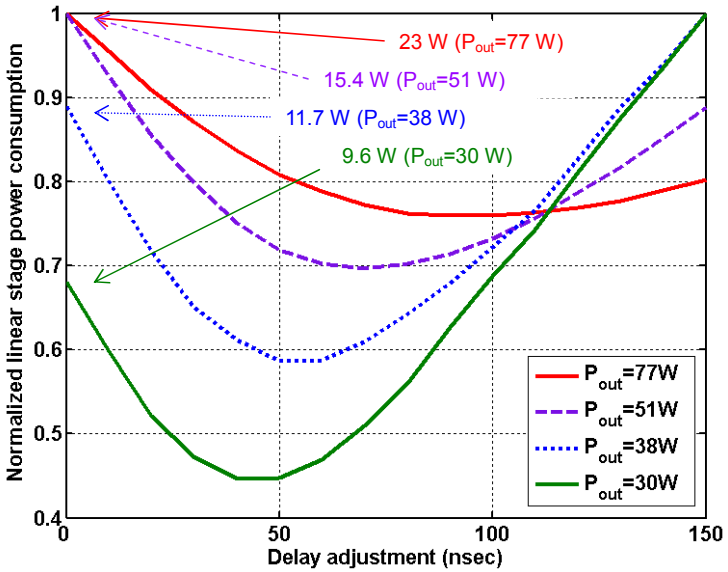
Figure 4.2: Simulated Envelope Amplifier Behaviors with 1.3 μH Inductor and Switcher Control Delay Adjustment

represents the hysteresis value, the pulse signal, $V_c(n)$, can be generated as follows:

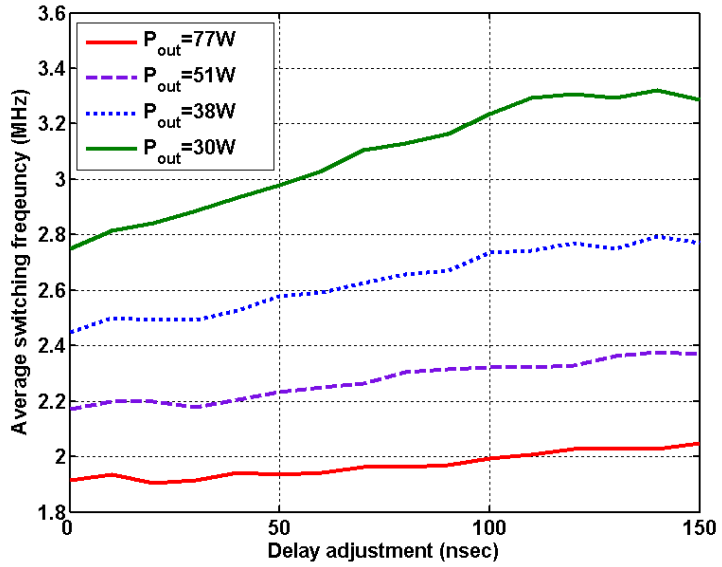
$$\begin{aligned} \text{If} \quad & V_r(n) < V_{in}(n+k) - h \\ & V_c(n) = 1 \quad \text{(switcher turn-on)} \\ \text{else if} \quad & V_r(n) > V_{in}(n+k) + h \\ & V_c(n) = 0 \quad \text{(switcher turn-off)} \\ \text{else} \quad & V_c(n) = V_c(n-1) \end{aligned}$$

By adjusting the delay k, the current generated from the main switcher is aligned with the envelope waveform, as shown in Fig. 4.2, which can reduce output current required from the linear stage.

Ideally, the DSP switcher control enables the open-loop switcher current assist



(a)



(b)

Figure 4.3: (a) Simulated Overall Linear Stage Power Consumption and (b) Average Switching Frequency versus Switcher Control Signal Delay Adjustment for Different Output Power with using 1.3 μH Inductor in the Switcher

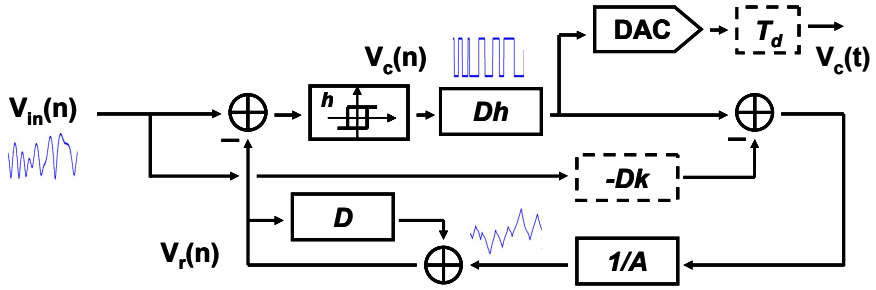


Figure 4.4: Digital Signal Generation for Switcher Control

the linear stage. However, in practical implementation of the circuits, the DC energy balance between the switcher and the linear stage is not always guaranteed by the open-loop control. Fig. 4.5 shows the simulation for the scenario that the switcher generates DC energy imbalanced with the linear stage. The linear stage current is likely going very large and in practice, the circuits would be overheating and probably damaged. Therefore, a feedback sensor, which returns any DC offset error information between the open-loop switcher and the linear stage, should be incorporated into the system for energy balance purpose.

Another way to compensate DC error between the open-loop switcher and the linear stage is by utilizing the current-sense analog feedback, which has been designed in the amplifier, to control another switcher to provide any DC imbalance current. In this configuration, the analog feedback signal is the magnitude difference between the load current and two switcher's current. Once the magnitude of feedback signal exceeds to certain level, which is in the case that the linear stage has to provide more power to compensate the offset, the current-sense stage would trigger another switcher to turn on to support the DC imbalance current, which could happen at the envelope amplifier output. Due to the fact that DC imbalance is low frequency, the analog control switcher does not require high speed and high slew rate performance, which eases the switcher

driver design. Section 4.3 will discuss how to design two switchers for the envelope amplifier.

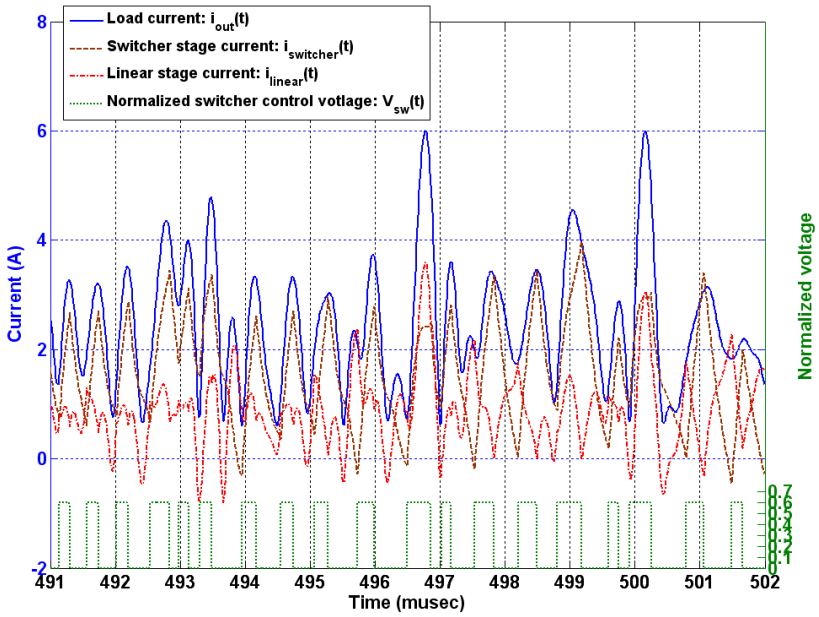


Figure 4.5: Simulated DC Current Imbalance at the Output of Envelope Amplifier

4.3 Dual-switcher Envelope Amplifier

4.3.1 Dual-switcher Envelope Amplifier Architecture

Based on previous discussions on the switcher control, a new envelope amplifier architecture, shown in Fig. 4.6, is proposed, which comprises one linear stage and two switcher stages in parallel [73]. The current supplied to the collector/drain of the RF power amplifier results from the combined outputs of the linear stage and the two switchers. The main switcher is digitally controlled by a DSP unit, while the auxiliary switcher employs analog current-sense hysteretic control. The main switcher provides the majority of current, including some high frequency portion, to the RF power ampli-

fier, while the auxiliary switcher acts as an assistant switcher to provide some part of low frequency current and to provide any possible DC current imbalance between the linear stage and the DSP-controlled main switcher. The linear stage is still functioned as a voltage source to correct any disturbances provided by the two switcher stages with the internal loop filter, so that the tracking error is minimized.

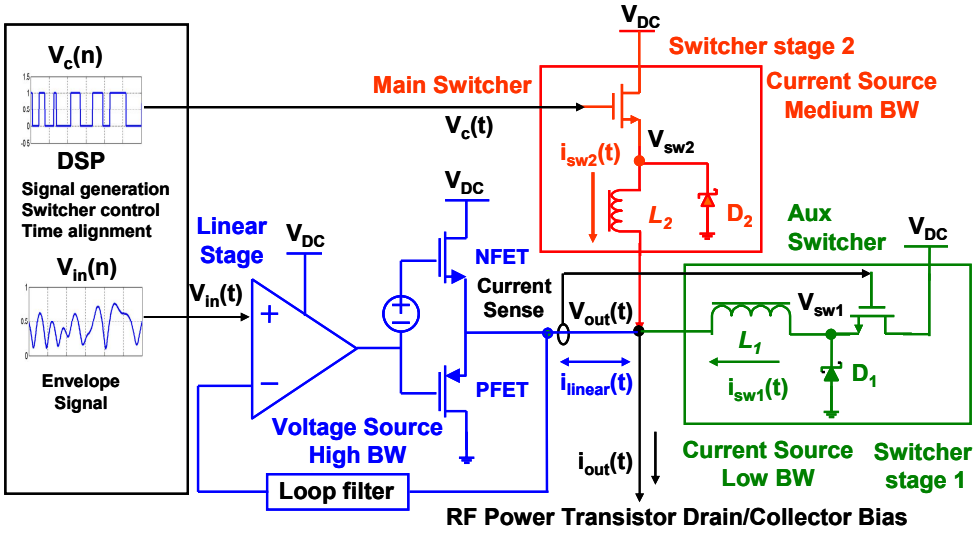


Figure 4.6: Dual-switcher Envelope Amplifier Schematic

Fig. 4.7 shows the dual-switcher envelope amplifier simulation results. The auxiliary switcher produces low DC current together with the main switcher's wideband current to help reduce linear stage's output current compared to the case in Fig. 2.9. Table 4.1 summarizes the simulated peak current magnitude the linear stage and the switcher stage have to provide in the dual-switcher and single-switcher case (30 V peak, 5 ohm load) using the same W-CDMA signal, respectively. The linear stage peak current is reduced in the dual-switcher case. One of the advantages is that the size of linear output stage of the dual switcher can be smaller than the single switcher for the similar

output power.

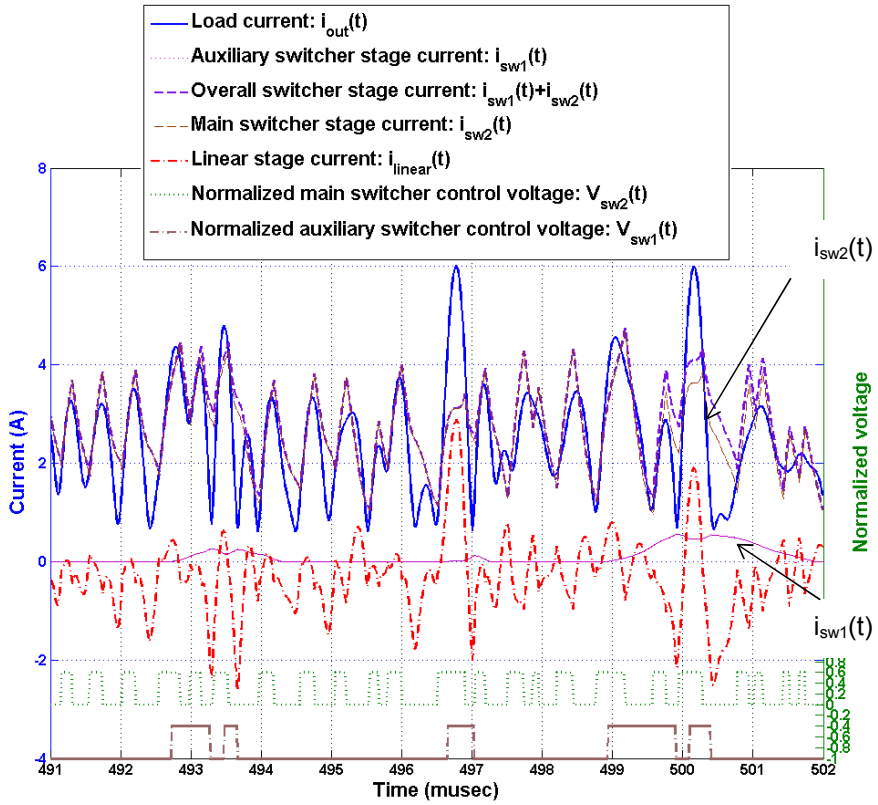


Figure 4.7: Simulated Dual-switcher Envelope Amplifier Behaviors with 1.3 μH and 25 μH Inductor for the Switchers, respectively

4.3.2 Dual-switcher Design Synthesis

Besides delay adjustment for the main switcher to help reduce the linear stage power consumption (Section 4.2), other two important design factors also influence the performance of the dual-switcher envelope amplifier. One is the selection of hysteresis and the other is the inductor value for the main switcher.

Fig. 4.8 shows the simulated linear stage power loss versus the hysteresis value, h, of the switcher stages taken to be equal for the two stages, while Fig. 4.9(a) and 4.9(b)

Table 4.1: Summarized simulated peak current distribution of envelope amplifiers with single and dual switcher stages using W-CDMA signal

	Amplifier output maximum current: 6 A / minimum current: 0.6 A					
	Linear stage pull-up (A)	Switcher stage 1 (A)	Switcher stage 2 (A)	Linear stage pull-down (A)	Switcher stage 1 (A)	Switcher stage 2 (A)
Single-switcher (Fig. 2.9)	3.5 (58%)	2.5 (42%)	–	-2.1 (35%)	2.7 (45%)	–
Single-switcher (Fig. 4.1)	4.2 (70%)	1.8 (30%)	–	-2.9 (48%)	3.5 (58%)	–
Dual-switcher (Fig. 4.7)	2 (33%)	0.5 (8%)	3.5 (58%)	-2.5 (42%)	0.2 (3%)	1.7 (28%)

shows the switching frequency of the main and the auxiliary switcher, respectively. We can clearly find that the linear stage power loss will drop as we use small hysteresis values for the switcher; however, the switching frequency of the switchers will rise. This implies that a design trade-off between the switcher power loss and the linear stage power loss needs to be considered in choosing an appropriate hysteresis value [5]. For optimum results, we find that the main switcher will switch at around 2$\sim$3 MHz for a single-carrier WCDMA signal once we set the hysteresis value around 0.5 V with a fixed inductance in the range 1$\sim$2 μH. The auxiliary switcher will switch around 0.4$\sim$0.6 MHz with larger inductance value (around 20$\sim$50 μH). This guideline provides a specification to optimize the switcher performance based on the switching frequency distribution.

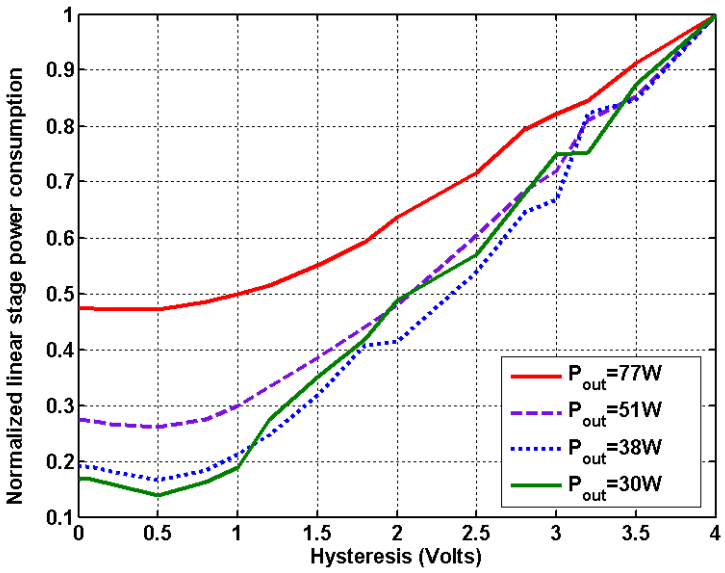
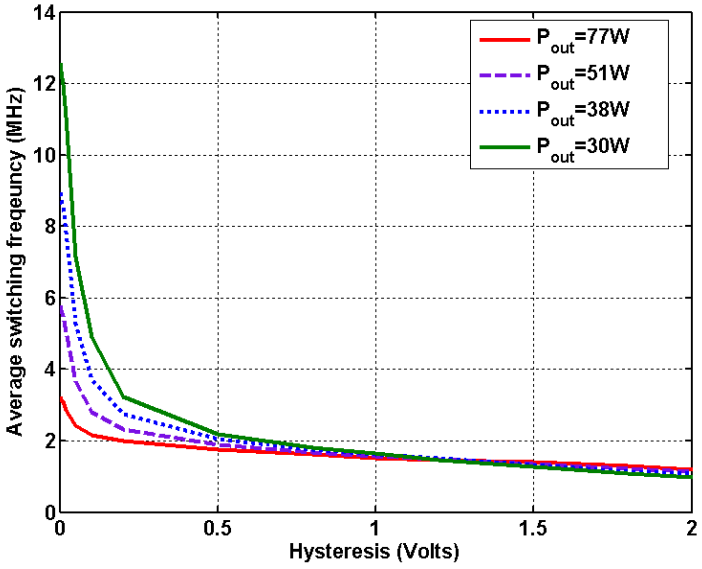
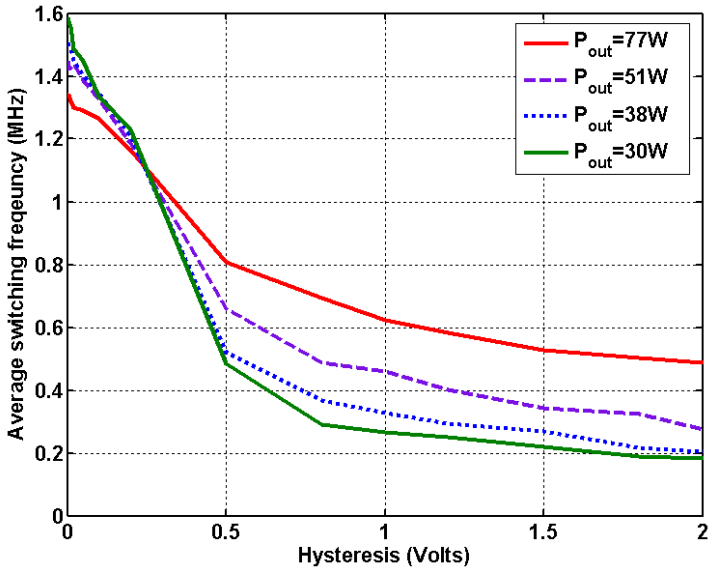


Figure 4.8: Normalized Linear Stage Power Consumption of the Envelope Amplifier versus Hysteresis Value

Another important design parameter is the ratio of the inductance, L_2 of the



(a)



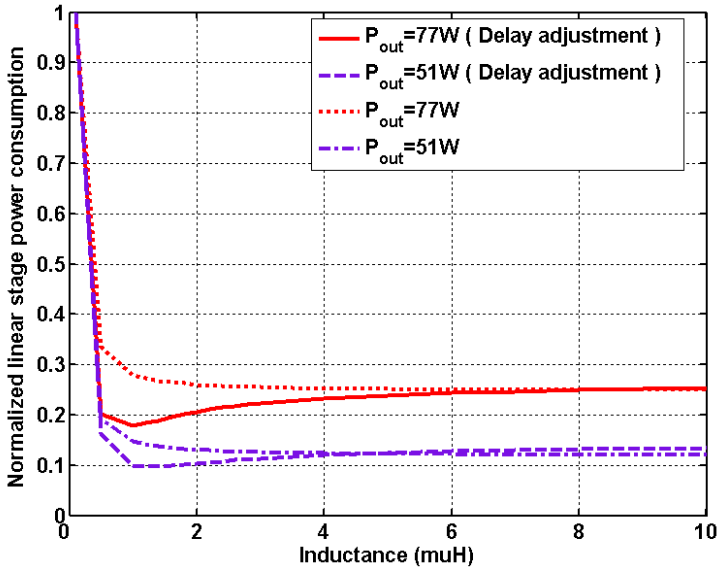
(b)

Figure 4.9: (a) Main Switcher Average Switching Frequency, and (b) Auxiliary Switcher Average Switching Frequency versus Hysteresis Value

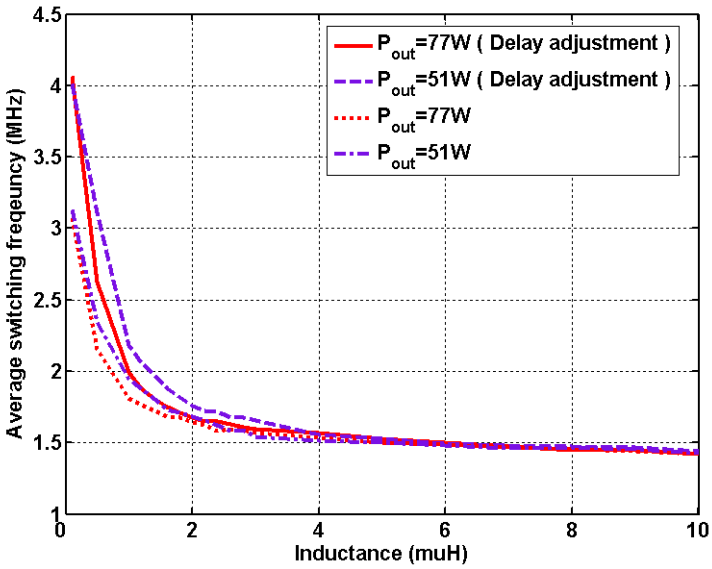
main switcher to the load impedance of envelope amplifier (Fig. 4.6), which would lead to different dynamic response (slew rate) of the main switcher. Fig. 4.10(a) shows the linear stage power consumption as we sweep the main switcher's inductance value with a fixed hysteresis under the same scenario as in the earlier discussions. Ideal lossless inductance is assumed. Red curves show that the linear stage power loss can be reduced by using a smaller L/R ratio with proper delay adjustment. In this scenario, the switching buck converter can introduce high slew rate current to take over high frequency linear stage output (Fig. 4.2). However, without delay adjustment, the linear stage power consumption will increase due to inductor current tracking delay so that the linear stage has to provide extra power (Fig. 4.1(b)). Therefore, for efficiency consideration, the better design without delay adjustment should adopt larger inductance [5]. Fig. 4.10(b) shows the average switching frequency of main switcher. The switching frequency will continue to rise with smaller L/R time constant and therefore reduces the switchers' efficiency. The optimal inductance obtained at the power level of interest in our experiments is in the range 1$\sim$2 μH. For the auxiliary switcher, there is no requirement to adjust the control of the switcher current since we use a relatively large inductance.

4.3.3 Experimental results

The dual-switcher envelope amplifier was assembled for 30 V peak envelope amplifier applications. The main switcher's average switching frequency was confined to around 2$\sim$3 MHz by using a small L/R (1.6 μH/ 4 ohm) value, together with properly chosen hysteresis (0.5 V). A larger L/R (25 μH/ 4 ohm) value was chosen for the auxiliary switcher because it is designed to switch relatively slowly compared to the main switcher. Once the average switching frequency and the L/R time constant of



(a)



(b)

Figure 4.10: (a) Normalized Linear Stage Power Consumption of the Envelope Amplifier, (b) The Main Switcher Average Switching Frequency, versus Inductance Value

the switcher are determined, the switcher's performance can be easily optimized by properly selecting switch-FET and Schottky diode as discussed in Section 2.6. In this design, IRLR120N fast switch-FET was selected for the main switch and IRFR3518 switch-FET was for the auxiliary switch. UPS3100 Schottky diode was selected for both switchers. Fig. 4.11 shows the picture of the assembled envelope amplifier. The performance of each switcher stage was optimized for its average switching frequency and then verified experimentally.

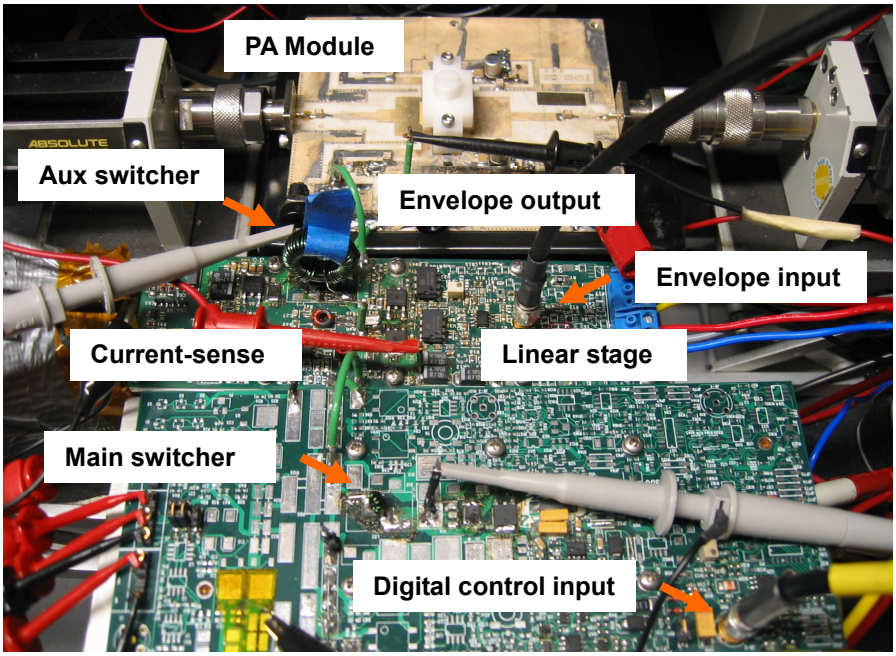


Figure 4.11: Dual-switcher Envelope Amplifier Hybrid Integration on PCB

Fig. 4.12 shows the measurement results of the two switchers optimized for different switching frequency ranges. The experiment was conducted by using periodic pulse signals with roughly 50% duty ratio as input, load equal to 4 ohm (which is about RF device output load impedance [9, 73]). The main switcher can reach over 80% efficiency around 2∼3 MHz switching frequency with 50∼60 W average output power,

while the performance of auxiliary switcher can reach over 90% efficiency with less than 1 MHz switching frequency for about 10 W output power under the same test conditions (roughly 20% duty ratio for input).

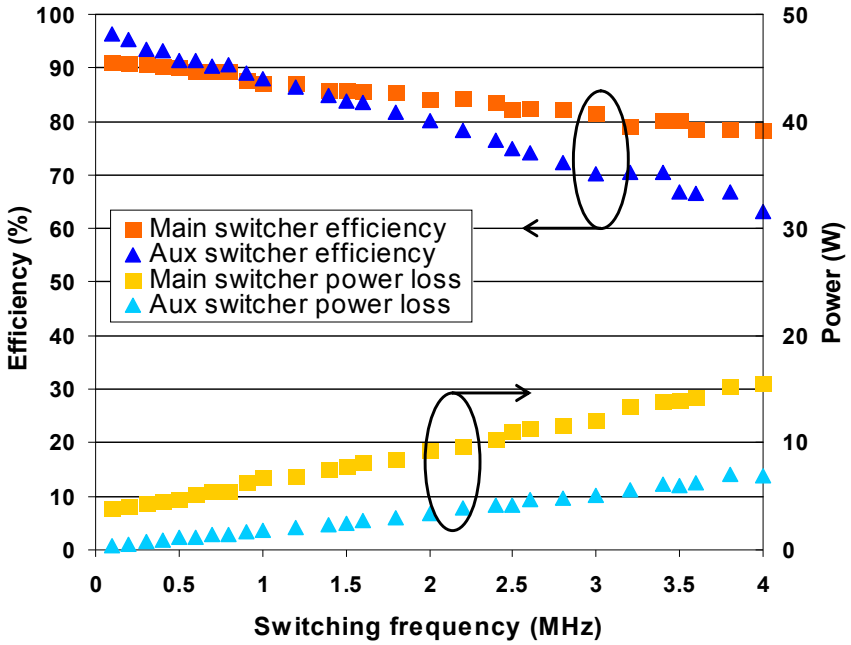
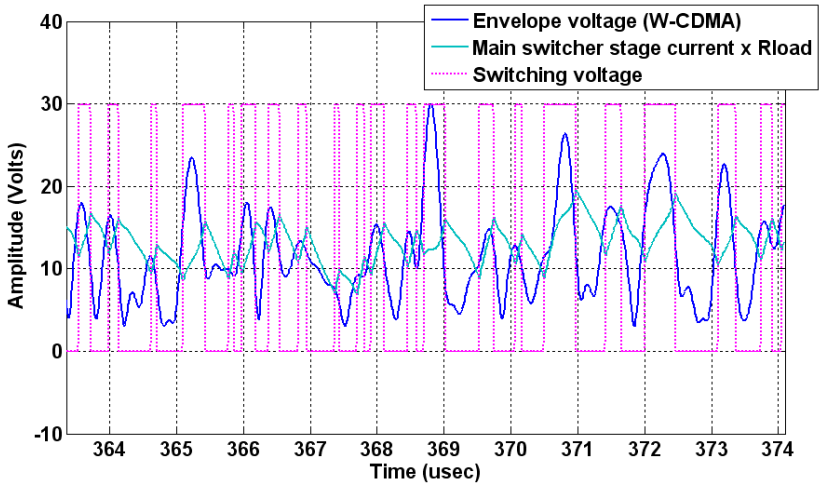


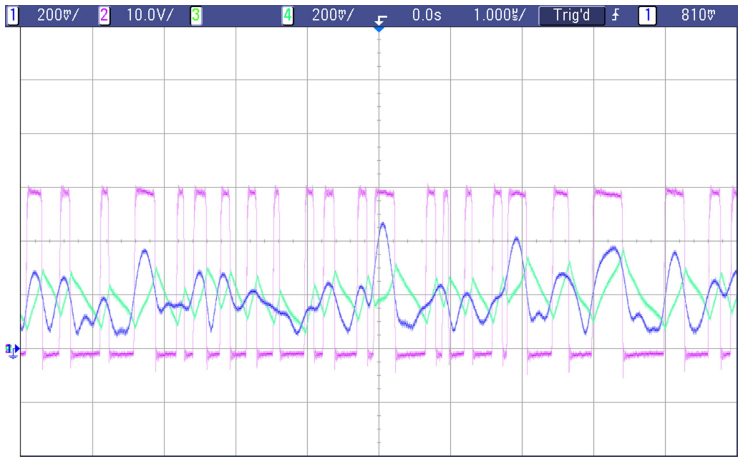
Figure 4.12: Measured Switcher Power Loss and Efficiency Performance versus Switching Frequency

The envelope amplifier was tested with 4 ohm constant load impedance. Fig. 4.13 shows the recorded waveforms before delay adjustment both in simulation and measurement, while Fig. 4.14 shows the recorded waveforms after delay adjustment both in simulation and measurement, respectively. The delay between the main switcher current and the load current can be easily reduced from the DSP-driven switcher control.

Fig. 4.15 shows the switching frequency distributions recorded from the experiment. The distributions are scaled to their peak values for two different amplifiers with the same W-CDMA input signal. The envelope amplifier for the dual-switcher case

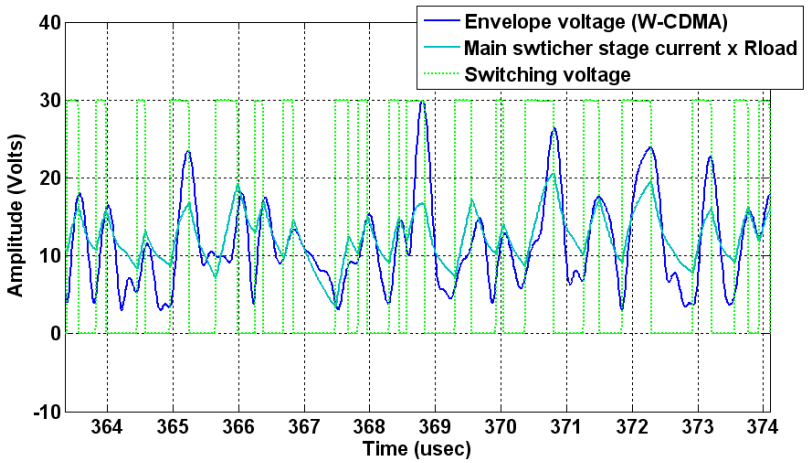


(a)

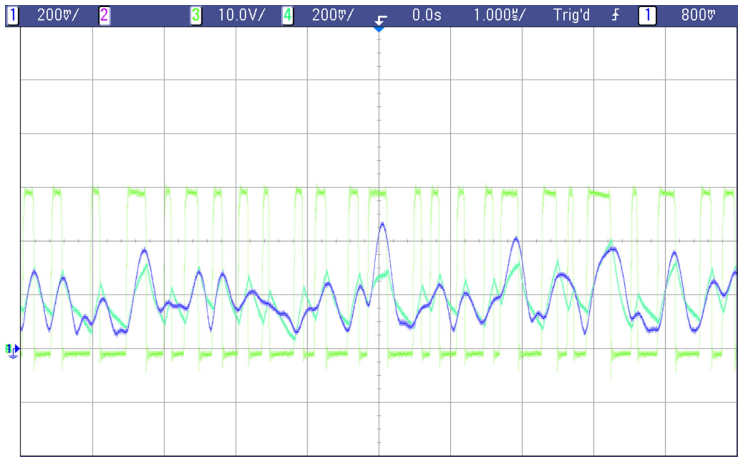


(b)

Figure 4.13: Recorded Waveform of Dual-switcher Envelope Amplifier Before Delay Adjustment (a) Simulation, (b) Measurement (Ch1,Ch4: 10 mV = 100 mA)



(a)



(b)

Figure 4.14: Recorded Waveform of Dual-switcher Envelope Amplifier After Delay Adjustment (a) Simulation, (b) Measurement (Ch1,Ch4: 10 mV = 100 mA)

shows two separate switching frequency distributions while the single switcher envelope amplifier's switching frequency spreads between them.

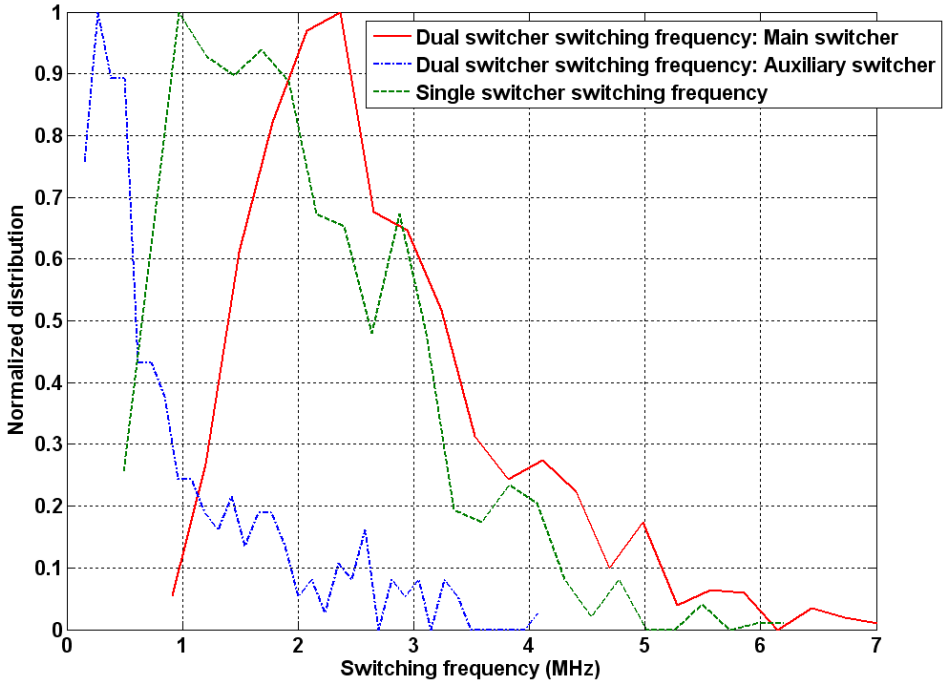


Figure 4.15: Measured Switching Frequency Distributions between Different Switcher Stages

Fig. 4.16 shows efficiency measurement results of two types of envelope amplifier over different PAR of envelope signals (using optimized inductance, hysteresis and delay adjustment for each case). The efficiency of the dual-switcher envelope amplifier is higher than that of the single-switcher envelope amplifier, especially with higher PAR signals.

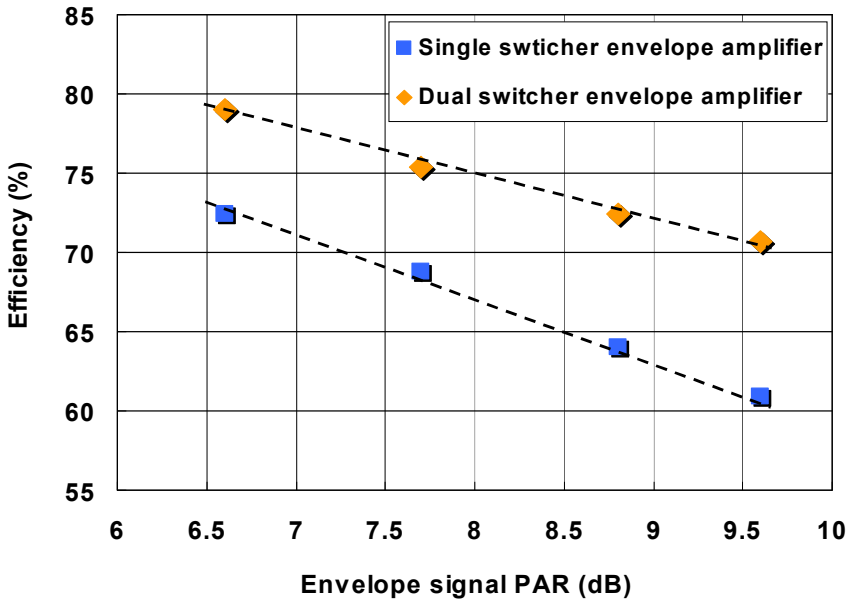


Figure 4.16: Efficiency Measurement and Comparisons between Two Envelope Amplifiers

4.4 Envelope Tracking Power Amplifier Measurement

RF Transistor Characteristics

To demonstrate the envelope tracking system with the dual-switcher envelope amplifier, GaAs high voltage HBTs (HVHBTs) were used as the RF transistor technology since they can provide high breakdown voltage (70∼80 V, suitable for 30 V ET applications), high power density, and high efficiency at potentially low cost [11]. Recently, GaAs HVHBTs have been reported showing 250 W output peak power and 57% collector efficiency with 6.5 dB PAR signal for WCDMA base-stations in a Doherty configuration [11]. For envelope tracking, the performance reaches more than 60% collector efficiency with similar signals [9].

The GaAs HVHBT devices used in this work were fabricated using a TriQuint Gen 1 and Gen 2 high voltage InGaP/GaAs HBT process, respectively. For higher break-

down voltage, a thick lightly doped collector layer and a heavily doped p-type base layer have been used in the epitaxial growth process. The transistors exhibit BVCBO $>$ 70 V for Gen 1, BVCBO $>$ 80 V for Gen 2, and BVCEO $>$ 40 V for both generations [74]. The Gen 1 device exhibits larger than 130 W CW output power while the Gen 2 device can achieve more than 250 W. The devices are properly ballasted to prevent thermal run-away and ensure good RF performance and stability [9, 11, 74]. Fig. 4.17 shows a top view of a single-ended HVHBT device and package that achieves 130 W (51.1 dBm) at P1dB [11]. The packaged device consists of two HVHBT transistor dies combined in a CuW-ceramic package. Pre-match circuits within the package provide an impedance of at 2.14 GHz at the output and at the input. Impedance matching via micro-strip lines and second harmonic traps were used on the input and output as shown in Fig. 4.18 [9, 11]. The DC bypass capacitor (1 μF) on the collector bias line was removed for envelope tracking applications. For Gen 2 device, the higher harmonic terminations were designed inside the package together with an outside board tuning on the feed-line of the envelope termination port, shown in Fig. 4.19 [12]. The RF devices were tuned to achieve best performance for a wide voltage dynamic range. Fig. 4.20 shows the output power, gain and collector efficiency measurement results of Gen 1 RF power amplifier under CW operation at 2.14 GHz with different constant collector biases [9]. The base of HVHBT is biased at 1.26 V. A collector efficiency of 77% and a gain of 10 dB is maintained for a wide rage of collector voltages and the measured peak output power reaches 151 W (51.8 dBm) [9]. For Gen 2 device, due to its high output power feature, the efficiency of RF device over a wide range of constant collector voltages was tested by a pulse CW measurement [13]. The duty cycle was set at 12.5% and around 300 nsec pulse width signals were used in the measurement. Fig. 4.21 shows the measurement

results. The collector efficiency is more than 80% from 10∼28 V and peak power is up to 54.5 dBm. The gain is more than 15 dB from 15∼28 V with the base bias set at around 1.26 V (class AB).

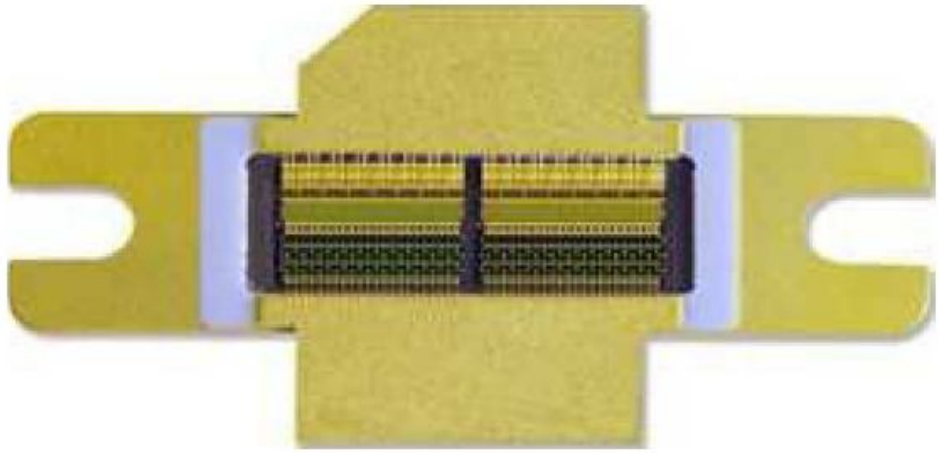


Figure 4.17: TriQuint Gen 1 GaAs HVHBT RF Device [9, 11]

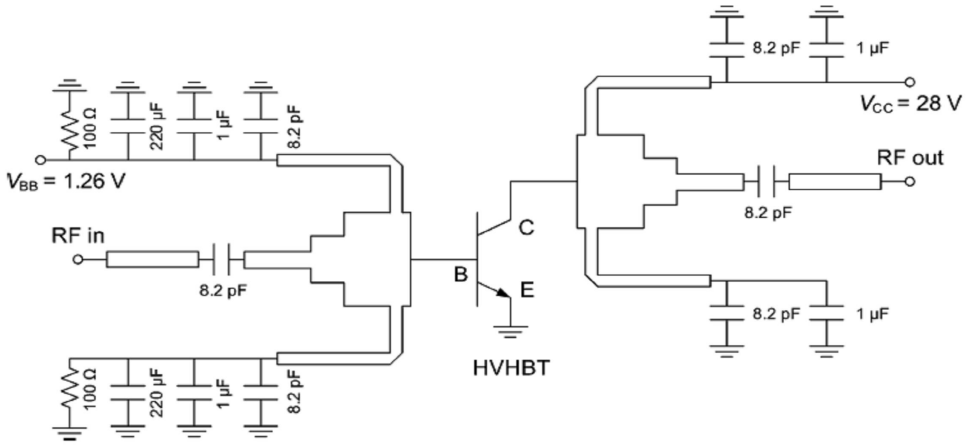


Figure 4.18: TrQiuint Gen 1 GaAs HVHBT RF Power Amplifier Test Fixture Schematic [9]

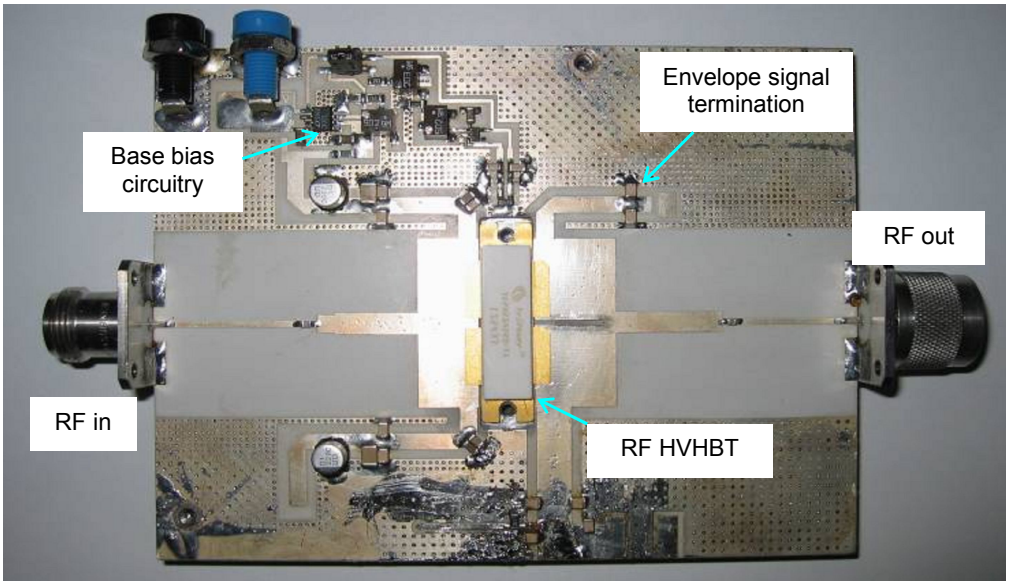


Figure 4.19: TriQuint Gen 2 GaAs HVHBT RF Power Amplifier Test Fixture [12]

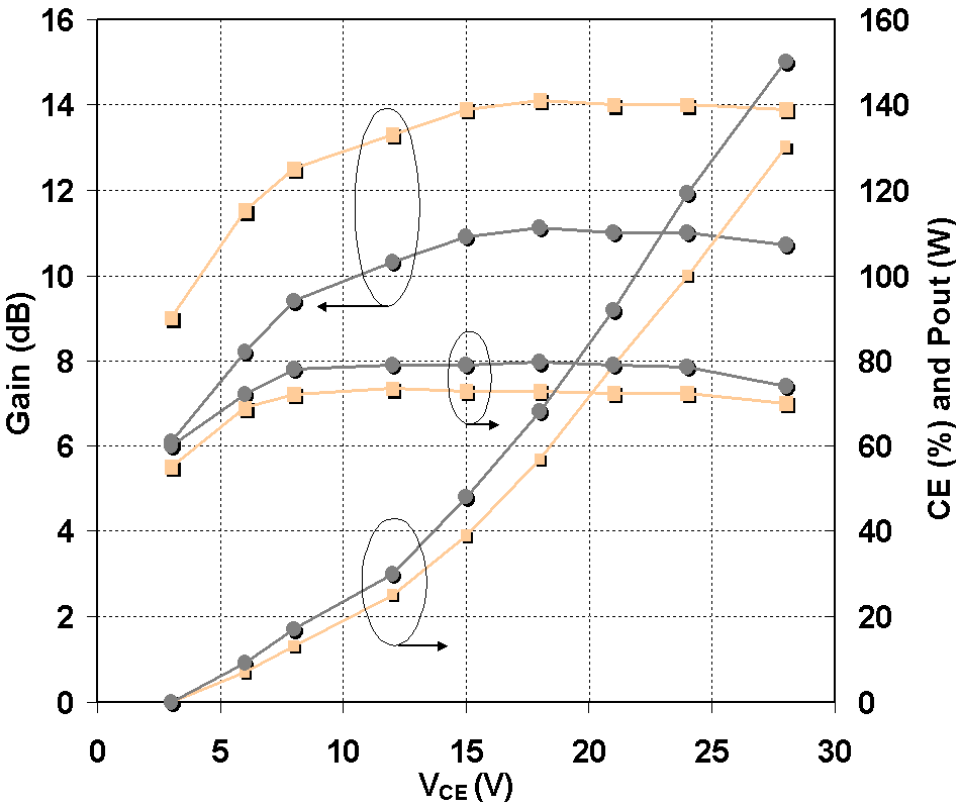
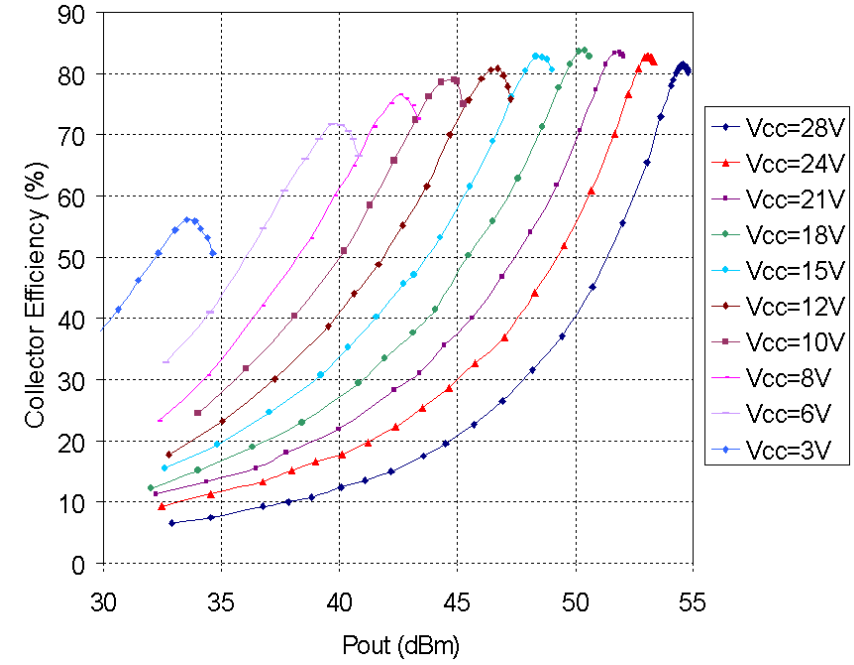
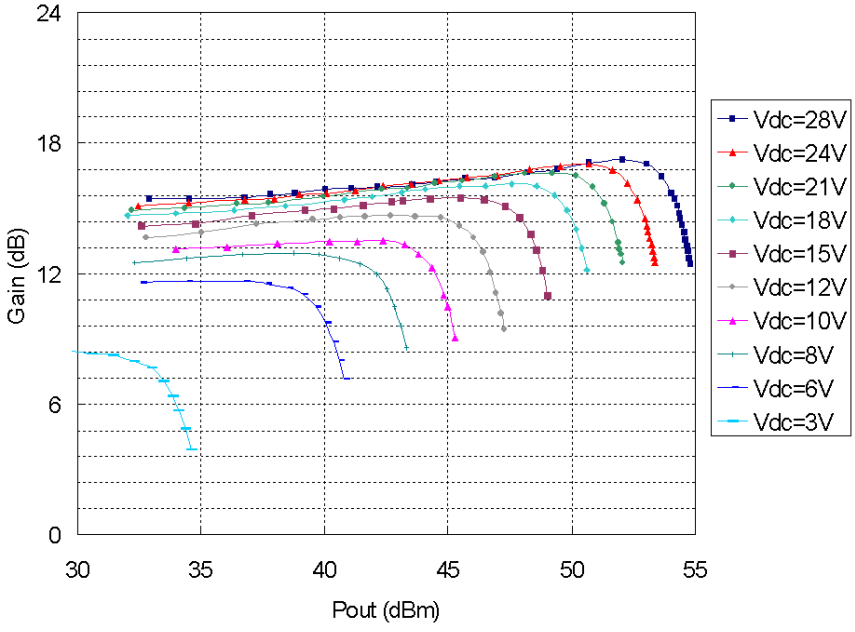


Figure 4.20: TriQuint Gen 1 GaAs HVHBT RF Device CW Measurement [9]



(a)



(b)

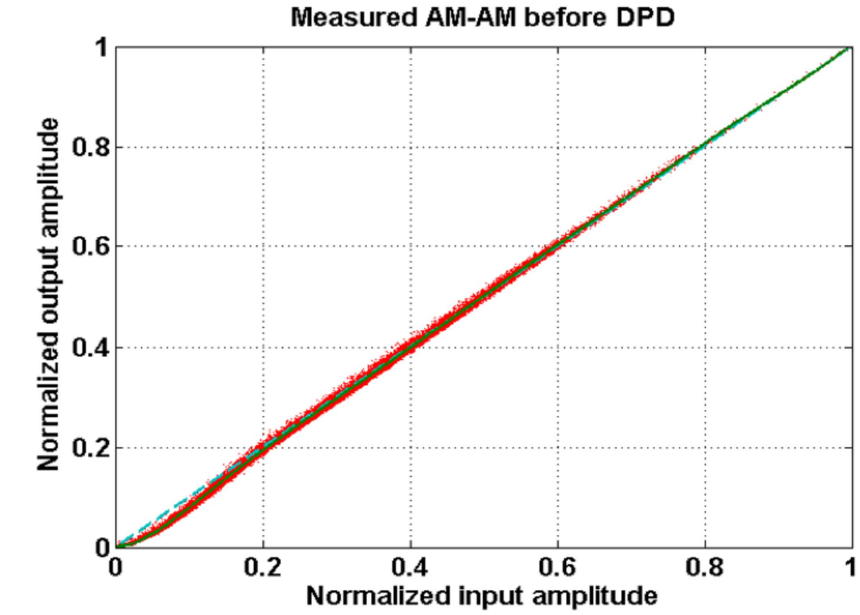
Figure 4.21: TriQuint Gen 2 GaAs HVHBT RF Device Pulse CW Measurement [13] :(a) Collector Efficiency, (b) Power Gain, versus Collector Voltage

ET Power Amplifier Measurement

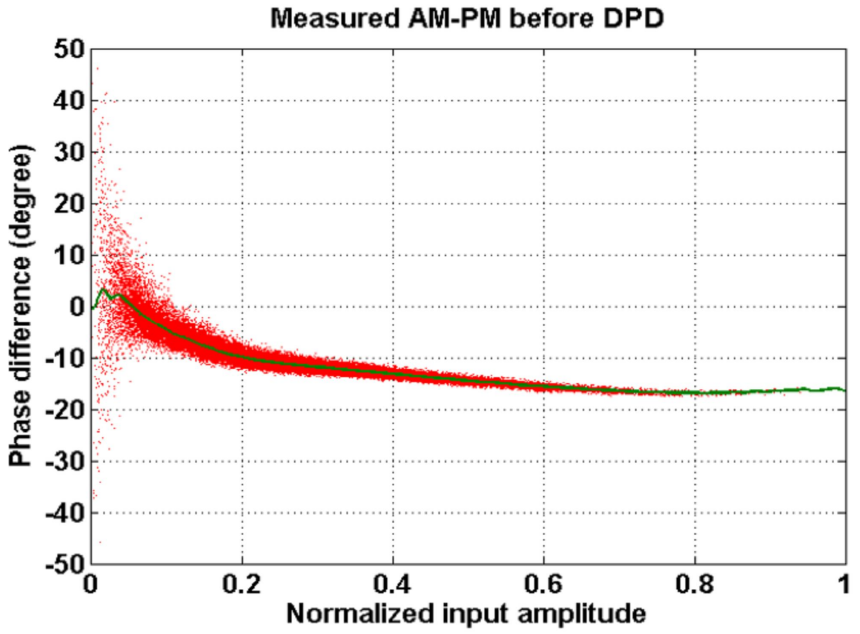
The overall measurement system diagram is shown in Fig. 2.1. The RF path uses a digital IF frequency of 26.88 MHz and up-convert to 2.14 GHz frequency band throughout the experiments, together with a single carrier W-CDMA signal with 3.84 MHz bandwidth, which was decrested to 6.6 dB, 7.7 dB, 8.8 dB and 9.6 dB, respectively. The dual-switcher envelope amplifier peak voltage is set at 28 V and the RMS value of envelope voltage is around 10$\sim$12 V.

Fig. 4.22 and 4.23 shows the measured AM-AM and AM-PM performance for a W-CDMA waveform, before and after DPD, expressed in terms of the output signal envelope, plotted versus the corresponding instantaneous input signal envelope value [13]. In this case, the AM-AM distortion is almost non-existent, and the AM-PM distortion is less than 10 degrees phase shift. This minimal AM-PM distortion corresponds to the fact that the HVHBT has nearly voltage independent output capacitance [10]. The scattering of dots in the figure for the different values of input power indicates a modest memory effect and phase distortion.

Table 4.2 summarizes the ET system performance with the signals before and after DPD. For testing with HVHBT Gen 1 RF power devices, the average collector efficiency, including dissipation in the envelope amplifier, is as high as 64% with average output power of 43.5 W at 6.6 dB PAR. For testing with HVHBT Gen 2 RF power amplifier, the average collector efficiency is as high as 65.6% with average output power of 66.9 W at the same W-CDMA test signal. The corresponding power added efficiency (PAE) is as high as 61.7%. This is the highest efficiency among the reported W-CDMA base-station power amplifiers [9, 13, 73]. The gain and NRMSE are 12.3 dB and 2.04%,

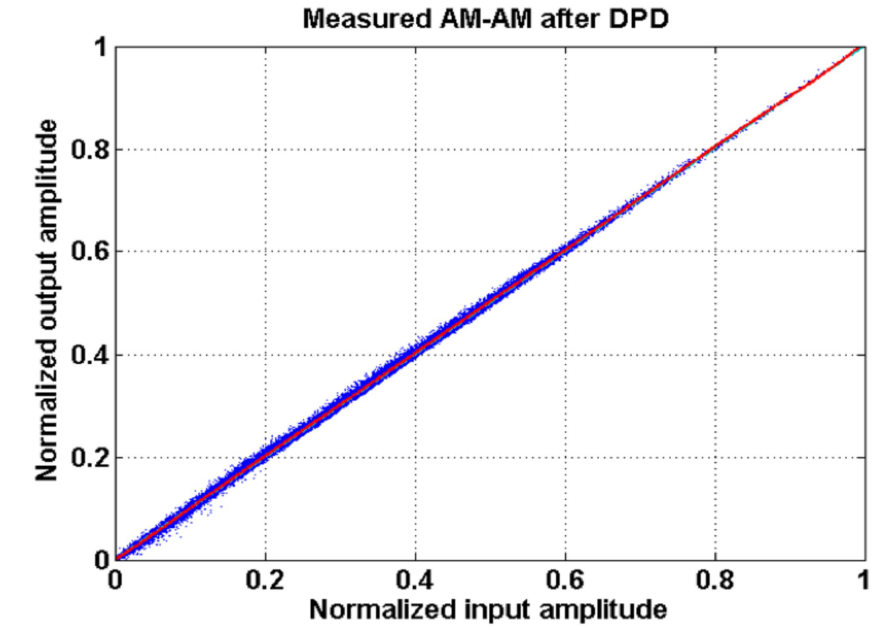


(a)

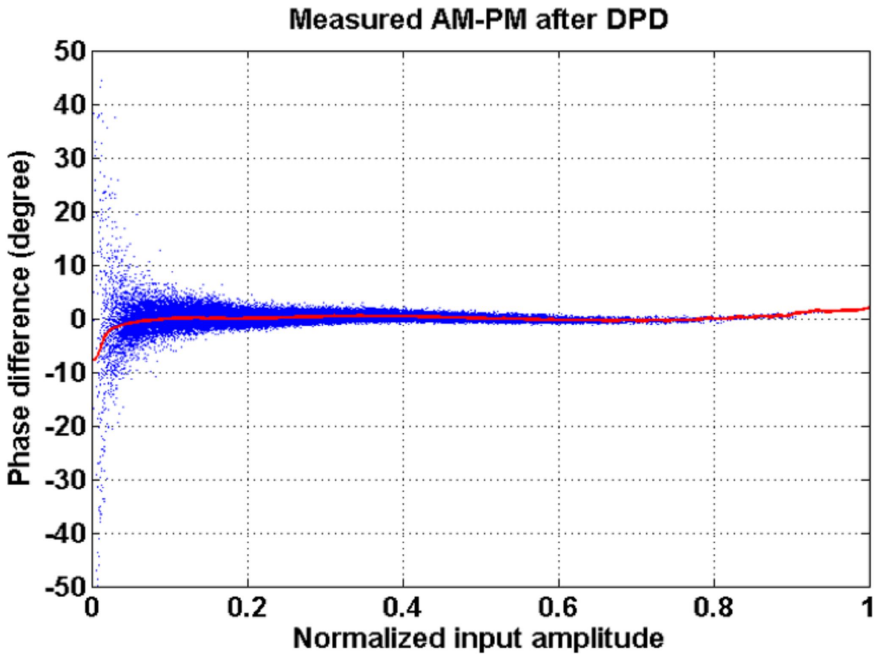


(b)

Figure 4.22: Measured: (a) AM-AM, (b) AM-PM Performance Before Predistortion [13]



(a)



(b)

Figure 4.23: Measured: (a) AM-AM, (b) AM-PM Performance After Predistortion [13]

respectively. The ACPR after memory mitigation [32] is down to below -55 dBc with the similar efficiency performance [13]. Fig. 4.24 shows the ACPR performance before, after DPD and after memory mitigation. Table 4.2 also summarizes the measured performance of the ET amplifier with higher PAR W-CDMA and WiMAX signals. The overall amplifier PAE remains higher than 51.7% even with higher PAR of above 8.8 dB and 10 MHz bandwidth signals, which is a rather significant improvement to previously presented results [9].

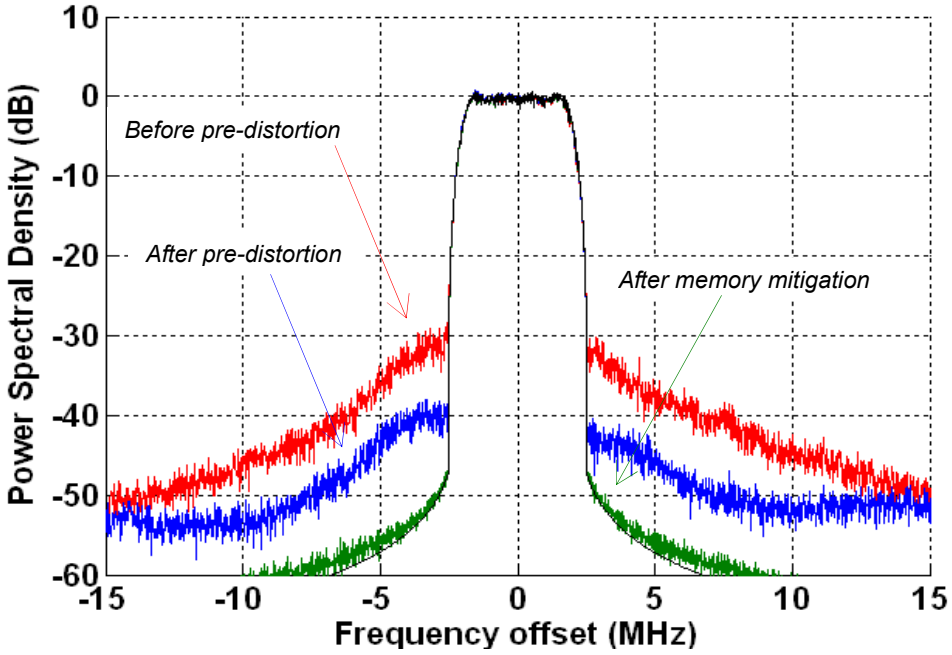


Figure 4.24: Normalized Output Spectrum of ET Power Amplifier Before and After DPD using TriQuint Gen 2 GaAs HVHBT RF Device

4.5 Summary

This chapter presents a novel envelope amplifier architecture to improve the overall efficiency of wideband high linearity envelope tracking power amplifiers. The

Table 4.2: Summarized Performance of Power Amplifier with Single Carrier W-CDMA and WiMAX Signal Before and After Digital Pre-distortion, MM: Memory mitigation

Signal Type	DPD	Gain (dB)	P_{out} (W)	CE (%)	PAE (%)	η_{PA} (%)	η_{env} (%)	NRMSE (%)	ACPR1 (dBc)	ACPR2 (dBc)
	Gen 1 HVHBT									
W-CDMA	Before	10.5	43.1	62.9	57.3	-	-	7.1	-35.6	-43.9
6.6 dB PAR	After	10.3	43.5	64.2	58.2	82.1	78.2	1.9	-45.5	-50.3
W-CDMA	Before	10.7	34.6	62	56.7	-	-	6.9	-35.6	-44
7.7 dB PAR	After	10.5	35.4	62.8	57.3	83.4	75.3	2.0	-45.7	-50.5
W-CDMA	Before	10.7	26.2	59.5	54.4	-	-	6.9	-35.5	-44
8.8 dB PAR	After	10.6	26.8	60.2	55.0	83.2	72.4	1.9	-45.3	-50.3
W-CDMA	Before	10.7	21.9	57.2	52.3	-	-	6.5	-35	-44
9.6 dB PAR	After	10.6	22.2	58.1	53.0	82.2	70.7	2.0	-45	-50.1
Wi-MAX	Before	10.8	26.1	55.7	51.1	-	-	9.3	-28	-32
8.8 dB PAR	After	10.6	26.4	57.0	51.7	81.3	70.1	4.9	-33.3	-38.6
	Gen 2 HVHBT									
W-CDMA	Before	12.4	66.2	64.5	60.8	-	-	6.8	-35.6	-44.8
6.6 dB PAR	After	12.3	66.9	65.6	61.7	82.1	79.9	2.41	-45.1	-50.5
	MM	12.3	66.8	65.5	61.6	-	-	0.7	-55.5	-60.2

technique utilizes DSP control in conjunction with analog hysteretic feedback. Two high efficiency buck switching stages are coordinated to provide the wideband envelope power to the RF stage; a wide bandwidth linear stage is also used at low power to maintain the envelope signal accuracy. The technique improves the efficiency of envelope amplifier, especially for applications requiring high peak-to-average power ratio (PAR) signals. The overall system was demonstrated by using a GaAs high voltage HBT power amplifier. For a variety of signals ranging from 9.6 dB to 6.6 dB PAPR and up to 10 MHz RF bandwidth, the overall system power added efficiency reaches above 50%, with a normalized power root mean square error below 5% and the first adjacent channel leakage power ratio (ACLR1) of -55 dBc after digital predistortion with memory mitigation, at an average output power above 20 W and gain above 10 dB.

4.6 Acknowledgements

The author is very grateful to Nokia-Siemens Networks for valuable discussions, and to Nokia-Siemens Networks for partial funding support. Some of the material in this chapter is as it will appear in "Dual-switcher Envelope Amplifier with Digitally-assisted Control for Envelope Tracking Base-Station Power Amplifiers", C. Hsia, D. Kimball and P. M. Asbeck, *IEEE Trans.on MTT.,* 2011 (in review). The contributions from the co-authors are appreciated. The author of this dissertation was the primary investigator and primary author for these publications.

Chapter 5

Conclusion and Future work

5.1 Dissertation Summary

Recent progress in wireless communications has led to highly spectrum efficient modulation schemes. These modulation schemes impose stringent linearity requirements on wireless transmitters, especially for base-station power amplifiers. On the other hand, the high PAR, wideband, and stringent linearity requirements pose several design challenges on implementation of high efficiency power amplifiers. The envelope tracking amplifier structure has attracted research interest for this type of applications due to its high efficiency over an broad power range.

In this dissertation, a broad range of envelope amplifier design considerations for envelope tracking power amplifier systems have been investigated, including envelope amplifier modeling, high voltage envelope amplifier design and implementation, and a novel digital control methodology for efficiency enhancement of envelope tracking systems. The study of the characteristics of envelope amplifiers both in simulation and experiment arrived at solutions leading to efficiency improvement of the overall envelope tracking system with good linearity performance.

At the beginning of this thesis, a Matlab/Simulink-based envelope amplifier model was developed for studying the envelope amplifier's behavior and efficiency. The simulator enables analyzing the envelope amplifier in detail with different input signals at different power levels. The results contribute to the understanding of the design requirements for envelope amplifiers.

Secondly, in an effort to find a circuit solution for efficiency improvement for high voltage envelope tracking power amplifiers, this dissertation delved into the high voltage BCD process to implement a high voltage OTA. The OTA was incorporated into a high voltage linear stage to improve the dynamic range of the envelope amplifier (from 30 V peak to 45 V peak). This resulted in efficiency improvement of RF amplifiers using envelope tracking. In the experimental work, two different dynamic range envelope amplifiers were assembled for overall system efficiency improvement verification based on the same RF transistor.

Finally, the thesis also demonstrated the possibility of using DSP control applied to the envelope amplifier. DSP is utilized to mitigate delay in the control loop and to reduce the power consumption of the linear stage through a novel switcher control. It has been shown experimentally that, with a W-CDMA single carrier envelope signal, the DSP-controlled envelope amplifier can achieve close to 80% efficiency while maintaining high accuracy. The envelope tracking power amplifier system based on the DSP-controlled envelope amplifier demonstrated state-of-the-art efficiency (PAE $>$ 60%) performance over an extended output power range ($>$ 6.6 dB PAR).

5.2 Future Work

5.2.1 Envelope Tracking System Modeling

The envelope amplifier model based on Matlab/Simulink has been verified in chapter 2. However, the model assumes the load line of the power amplifier during envelope tracking is a constant impedance. To utilize the model to simulate a more complete envelope tracking system, the actual RF power amplifier nonlinear model can be incorporated into the simulator to model a more realistic response of the amplifier. It can also help predict more accurately the nonlinearity performance of the envelope amplifier to assist in developing a more robust DPD algorithm for envelope tracking systems (including both RF signal path and envelope signal path.) The goal will be to generate a clear picture of the envelope tracking system performance, including both linearity and efficiency.

5.2.2 Fully Integrated High Voltage Linear Stage

A high voltage envelope amplifier has been designed, implemented and demonstrated in chapter 3. However, the bandwidth of the amplifier is limited to around 30 MHz. Part of the reasons for this limitation is that the linear stage is implemented using a PCB board with different device technologies. The parasitics inside the packages for the different components affect overall phase delay of the output signals. The frequency response of the high voltage linear stage is, therefore, somewhat compromised. With proper consideration of the linear stage gain, slew-rate requirements, and power handling capability, a fully integrated high voltage linear stage can be designed in the future without sacrificing the performance benefits obtained from on-board tweaking for best

gain and stability.

5.2.3 A Multi-switcher Envelope Amplifier with Closed-loop Control

In chapter 4, we have demonstrated the advantages of applying DSP control for improving the efficiency of envelope amplifier running W-CDMA with different PAR signals. However, with more demanding requirements on RF signal's bandwidth for current and future base-station power amplifiers, the envelope signal's bandwidth is going to be extremely wide. Wider bandwidth envelope signal increases the switching frequency of the amplifier, which unavoidably leads to overall efficiency degradation. To mitigate the issue, in addition to two switchers applied in our system, a multi-switcher envelope amplifier architecture can be fully utilized. Each switcher can deal with a part of the wide-band signal and their output an be combined together. In this case, to reduce the DC imbalance between each stages, a closed-loop feedback has to be developed to provide more effective control for each switcher. A potentially suitable solution for the multi-switcher envelope amplifier is to use an envelope ADC to monitor the output current of the amplifier and feed back the information to either the DSP controller or switcher control signal generator.

5.2.4 Hybrid Envelope Amplifier Architecture for Other Applications

In this dissertation, hybrid amplifiers have been utilized for envelope amplifier design. However, potential applications for hybrid architectures should not be limited. The amplifier structure should also be an promising candidate for other power supply

system, which requires fast speed, quick response, and high efficiency applications such as LED power supply, modems, or audio amplifier applications, etc. With recent high voltage device processes, such as GaN-based or LDMOS-based technologies, suitable solutions to fully integrate the hybrid amplifier on chip should be anticipated in the near future. The need for creative designs of integrated amplifiers remains a key for maintaining high efficiency performance. Further innovations will be required in the future.

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