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DESIGN, FABRICATION AND CHARACTERIZATION OF MICRO-ELECTRO-MECHANICAL FABRY-PEROT INTERFEROMETER FOR USE IN MID-WAVE INFRARED

A dissertation submitted in partial satisfaction
of the requirements for the degree of

DOCTOR OF PHILOSOPHY

In

ELECTRICAL ENGINEERING

By

Dmitry Alexander Kozak

JUNE 2013

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Vice Provost and Dean of Graduate Studies

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Abstract

DESIGN, FABRICATION AND CHARACTERIZATION OF MICRO-ELECTRO-MECHANICAL FABRY-PEROT INTERFEROMETER FOR USE IN MID-WAVE INFRARED

Dmitry Alexander Kozak

Micro-Electro-Mechanical Systems (MEMS) allow scaling down and integration of conventional scientific instrumentation. In particular, advancements in fabrication have made possible the creation of small, precise and inexpensive versions of optical components and systems.

Optical components for the use in mid-wave infrared (MWIR) range, 3-5 μm wavelength, are of particular interest for their ability to detect various organic chemical compounds and to determine the temperature of objects based on their radiation emission. High sensitivity, but low spectral resolution of optical detectors in the MWIR region requires addition of optical filters to provide spectral information.

In this thesis we describe the design, fabrication, and testing of a MEMS-based optical filter that combines a Fabry-Perot interferometer with dielectric Bragg reflectors, using magnetic actuation.

The research started with identification of the problem, complete literature search to identify the existing solutions. A novel design for an improved optical filter was proposed. Optical and mechanical models were created, and materials were chosen that correlated to the optical model. Fabrication flow was developed for robust and

wafer-scale process that achieves high yield and improves optical performance.

Three iterations of fabrication cycle resulted in improvement of optical characteristics of the devices by three orders of magnitude.

Mechanical method of magnetic actuation was developed that allows precise movement across the entire range of MWIR. Optical results from the first device were shown to correlate with mechanical and optical models.

To my wife Victoria

Acknowledgements

This work is dedicated to everyone who has helped me along the way, my family, colleagues and mentors.

Especially I would like to thank the members of the dissertation reading committee: Professor John Vesecky, Professor David Koo, and Professor Nobuhiko Kobayashi for their support and help throughout this work.

Many thanks to my adviser Dr. Kubby for his mentoring along the way.

I would like to thank EPIR Technologies for sponsoring this project and all of their support.

Special thanks to Dr. Grbovic, Dr. Alves, Dr. Kearney and Dr. Karunasiri at Naval Post-graduate School for all the help with optical set-up, testing and analysis.

Chapter 1 : Introduction

1.1 Introduction

This thesis is but one part of the research performed over the past seven years at UCSC. Other projects worked on by Dmitry A. Kozak include

- Wafer-scale fabrication of NEMS switch based on carbon nano-fiber, done in collaboration with NASA Ames research center.
- Design and fabrication of MEMS-based electric eel battery, in collaboration with Dr. Kubby and Dr. Fernandez.
- Electric Eel Project in collaboration with Dr. Isaacson and Dr. Pantchenko.
- Design, modeling and fabrication of Lamellar grating optical filter, sponsored by EPIR.

This thesis describes only the most complete and most important project done over the years.

The Mid-wave infrared (MWIR) spectral range from 3-5 μm has recently been of great interest due to its variety of applications in chemical sensing [1,2] and astronomy [3], as numerous gases have distinct absorbance bands in this range [4]. MWIR detectors can have a very high sensitivity, but due to their wide-band response, the spectral resolution is very low [5]. Large mechanically controlled optical filters have been added to the system [6], although these high resolution optical filters are expensive and hard to adapt for all the desired applications. Availability of individually controlled pixel detectors allows for high-density focal

plane arrays, but requires a device that can provide individually controlled filtering for each pixel for fast narrow waveband scanning. It is our goal to create technology that would combine the highest quality detector and filter components to create low-cost, easy to manufacture optical devices that have high sensitivity and spectral resolution for in a wide variety of applications.

1.2 Optical filters

The first optical filter that broke down the incoming light into its spectral components is, arguably, a prism. Science has come a long way from using these devices as mere toys to realizing that there is great amount of information that could be obtained from the observation of different spectral lines. Amount of emission or absorption at specific wavelength can provide information about the relative composition of a gas [7] or can be used to determine the temperature of an object [8].

For many applications the detectors can be made to respond to a very narrow wavelength range [9]; therefore reading from an array of detectors, each centered on a specific region of absorption, can give the required spectral information. This approach, however, is very expensive.

Another approach would be to have a wide-band, sensitive detector and a tunable filter that allows only certain wavelength of input light to reach it. The basic diagram of such a device is shown below in Fig. 1.1. A wide-band emitter source, which can be either a black body or an LED, is used to provide the input light across all the wavelengths of interest. A tunable filter, controlled by electronics, selectively passes

only a narrow band of incoming light. A detector that is designed for a specific region is placed immediately after the filter, and provides read-out of the signal strength.

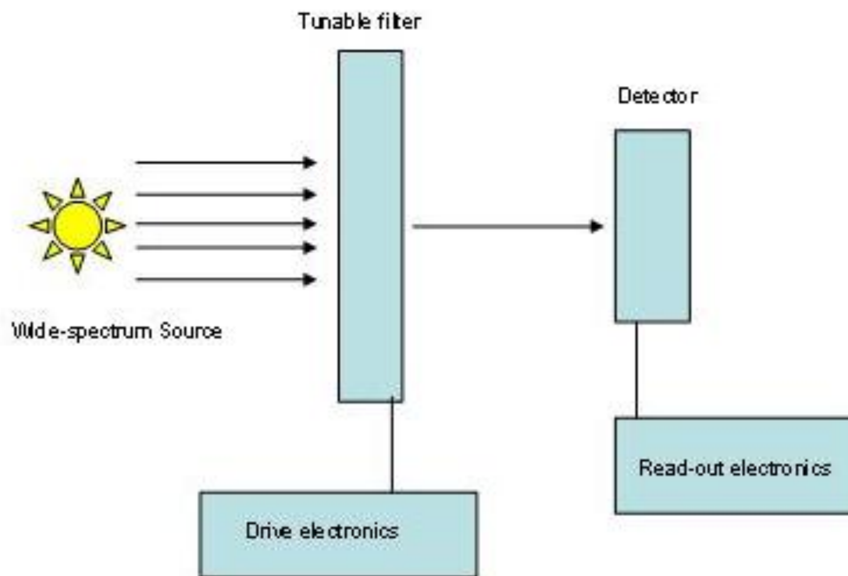


Figure 1.1: Basic schematic of an optical filter

Filters can be either static or dynamic. Static filters, such as Bragg reflectors, are designed to pass or reflect only a narrow bandwidth of light [10]. This approach suffers from the same problems as having arrays of narrowly tuned detectors: they are expensive, can take up large areas and require multiple redundant elements. Dynamic filters overcome these problems by having just one filter and one detector. With the ability to tune the filter, spectral information can be obtained. An example of the most commercially popular optical filter is a motor driven diffraction grating, which is an integral part of such scientific instruments as monochromators [11].

1.3 Interferometry in the MWIR

The region of 3-5 μm, known as mid-wave infrared, has been of interest, in particular to chemists, for several decades [12]. In this region most organic compounds have very distinct absorption lines, and interferometry allows for easy identification of components and their relative composition [2]. The most common instrument used in chemistry labs for this purpose is the Fourier Transform Infrared Spectroscope (FTIR) [13]. This device uses a mirror moved by a mechanical motor to obtain spectra. While very precise, these devices are very large, expensive and consume large amounts of power.

The usefulness of these devices for chemists has driven extensive work to find an alternative that would be smaller and cheaper, while still providing the same accuracy and spectral range [14].

With the emergence of micro-electro-mechanical systems (MEMS), it was realized that the combination of mechanical movement, low cost, small size, and precision afforded by MEMS would be a good fit for making MWIR spectroscopes more efficient. Most of the projects involve scaling down existing spectroscopic instruments, such as Michelson interferometer, Lamellar grating interferometer, and Fabry-Perot interferometer [9, 15].

1.4 Previous work on Fabry-Perot interferometers

Large Fabry-Perot interferometers have been used in astronomy since the 1950s [16]. Lately there has been work on creating small, light and inexpensive filter/detector devices, starting with NIR and moving into MWIR and LWIR [17].

Scaling down infrared detectors allows them to be coupled with MEMS-based optical filters in several ways. Integration in a package has been done by the InfraTec Corporation, which has created a commercial product based on a Fabry-Perot filter made out of several layers of bonded silicon wafers, with Bragg stack mirrors made out of silicon and silicon dioxide layers [18]. Schuler et al. gives an excellent summary of the theory and an extensive overview of several technologies [19].

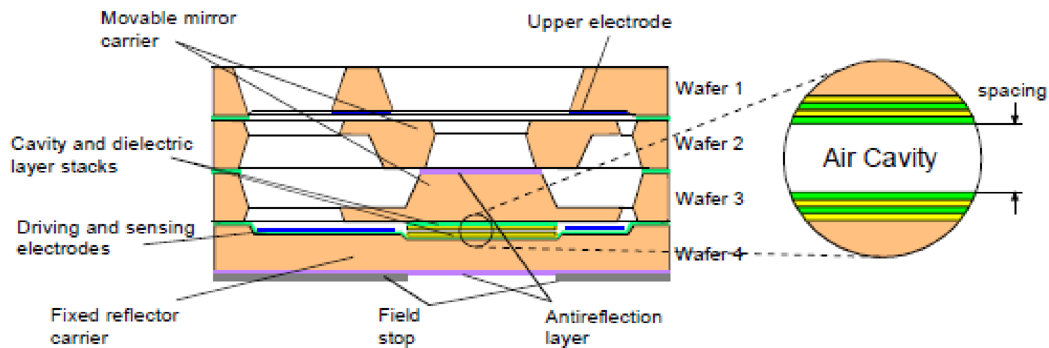


Figure 1.2: FPI device by Infra Tec

Monolithic integration has been done by Martyniuk, Antoszewski, Musca, Dell, and Faraone at the University of Western Australia, who have worked on the monolithic integration of a HgCdTe detector with a MEMS filter, that uses a Bragg stack composed of germanium and silicon oxide layers on a silicon nitride structural layer [20-22].

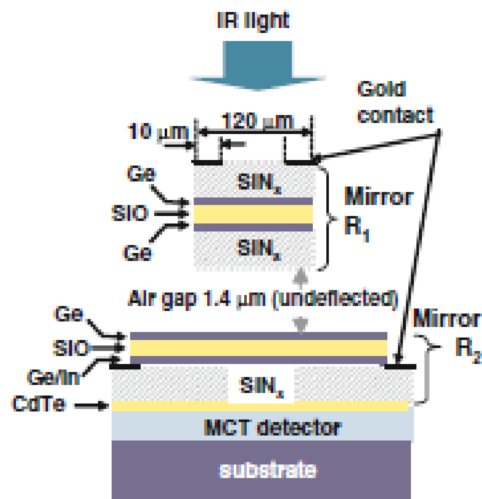


Figure 1.3: FPI device by UWA

1.5 Motivation of dissertation

While the work done by the InfraTec and the UWA group has been extensive and has also resulted in a commercial device by InfraTec, there is room for improvement. The InfraTec devices have low travel distance, requiring two separate devices to cover the 3-5 mm range [23]. Also, their integration with the detector in a package makes assembly cost high and reduces the yield. Such devices cannot be cheaply integrated into large multi-channel arrays to provide fast and efficient finger-printing of chemical agents or FPGA arrays for vision.

By partnering with the manufacturer of HgCdTe detectors, EPIR Technologies, we were able to create a device that is highly selective in optical filtering and allows integration into large arrays.

This dissertation describes the development of an optical filter that has a narrow bandwidth, can be controlled over large spectrum, and can be integrated into single-pixel devices for chemistry applications and large arrays for vision applications. The overall flow of the project follows the cycle shown in Fig. 1.4, with multiple iterations of the cycle described in this work. Starting from the identification of the problem and existing solutions, requirements from optical and mechanical design have to be brought together. Materials have to be analyzed that would accomplish the goals of optical and mechanical behavior and also fit the fabrication requirements. Fabrication flow has to be designed, executed and analyzed, with consequent testing of the devices. Following the identification of problems, the process has to be repeated again.

1.6 Contributions of the Thesis

This dissertation describes in detail three iterations of the cycle described above.

- The problem of tunable optical filters in MWIR that can be integrated into arrays has been identified.
- Solution of tunable MEMS filter based on the principle of Fabry-Perot interferometer has been proposed.
- Optical and mechanical theoretical analysis has been performed, resulting in optical and mechanical models of the proposed devices.
- Materials that can be used to fabricate the tunable filter have been identified.

- Fabrication flow that uses equipment available at Stanford Nanofabrication Facility has been designed.
- A series of short-loop tests to verify the possibility of the proposed fabrication flow have been performed.
- Three iterations of the project have been performed, resulting in at least one order of magnitude improvement in optical characteristics with each iteration.
- Novel method of mechanical actuation of the devices has been proposed and executed, resulting in devices that can provide filtering over the entire region of MWIR.
- Optical testing of the devices has confirmed the correlation between models of the devices and observations with the first working prototypes.

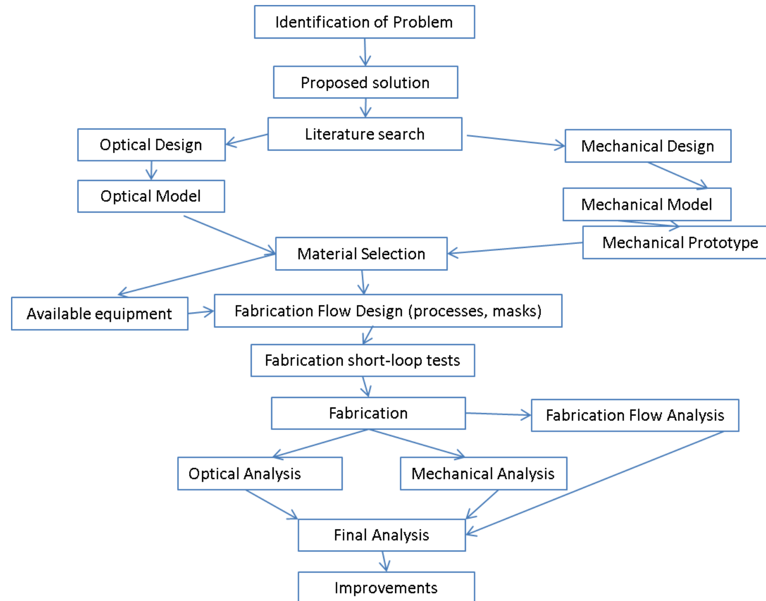


Figure 1.4 Flow chart of the project

Chapter 2 : Fabry-Perot Interferometer Principles and Bragg Reflectors

2.1 Introduction

In this chapter, a short overview of an optical filter known as a Fabry-Perot interferometer is given. Figures of merit and filtering behavior is discussed for ideal devices, as well as changes in filtering behavior due to defects. Theory and design of dielectric Bragg reflectors is presented.

2.2 Short review of Fabry-Perot interferometer principles

A typical Fabry-Perot device, consisting of two partially transmitting and partially reflecting parallel mirrors separated by an air gap, is illustrated in Fig. 2.1 [24-26]. Light with intensity I_i is incident on a thin film of thickness *t*, with angle of incidence θ. Some of the light is reflected, I_r, and some of the light is transmitted, I_t. The two mirrors have reflectivity R, and are separated by an air gap of distance *d*. Constructive and destructive interference of light as it passes through multiple interfaces and is refracted within each layer produces a filtering effect, allowing light of wavelength *md/2* (*m* is an integer) to pass through, while reflecting all other wavelengths.

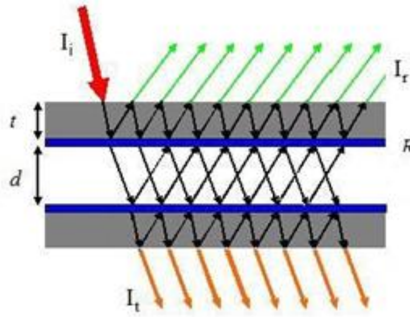


Figure 2.1: Illustration of a Fabry-Perot interferometer

The principle of this device is the change in phase of the incoming beam based on the transmission and reflection from each surface. In the same medium, upon reflection from a boundary, parallel lines have phase difference of δ, given by

$$\delta = \frac{2\pi}{\lambda} 2nd\, cos\theta \tag{2.1}$$

Where n is the refractive index of the medium and λ is the wavelength of the light. Multiple reflections produce beams that interfere constructively, if they are in phase, or destructively, if they are out of phase.

In order to achieve the maximum constructive interference, the following condition has to be satisfied, where *m* and *n* are integers:

$$nd\, cos\theta = \frac{m\lambda}{2} \tag{2.2}$$

If the medium of cavity is air, and the incident angle is zero, this condition is met when the wavelength is equal to m multiples of 2*d*.

Summing up the intensities of all the reflected and transmitted beams yields the intensity of the transmitted light, I_t, as follows:

$$I_T = \frac{T^2}{(1-R)^2} \times \frac{1}{1+\left[\frac{4R}{(1-R)^2}\right]\sin^2\frac{1}{2}\delta} \qquad (2.3)$$

Where R is the reflectivity of the mirrors in Fig. 2.1, T is the transmissivity of the mirrors, and δ is defined in Eq. 2.1. The main figure of merit of a Fabry-Perot interferometer is reflective finesse, N_R, given by

$$N_R = \frac{\pi\sqrt{R}}{1-R} \qquad (2.4)$$

The bandwidth, or full width at half maximum (FWHM), of the Fabry-Perot interferometer is

$$\mathbf{FWHM} = \frac{\lambda_c}{mN_R} \qquad (2.5)$$

where λ_c is the central wavelength of interest. For the majority of applications, it is of particular interest to decrease the bandwidth, as this would allow for higher spectral resolution, and for that one needs to increase the finesse.

2.3 Defects in Fabry-Perot Interferometers

Compared to the ideal FPI, with perfectly parallel, infinite plates with zero roughness, fabricated interferometers have several common defects that make their behavior deviate from theory.

Hernandez [24] in his fundamental book introduced analysis of these defects and their treatment, and others [27-31] have simplified this treatment for use by engineers developing and characterizing the devices. In this treatment, one of the plates is assumed to be perfect, and all the defects are transferred to the second plate. Three types of defects are shown in Figure 2.2.

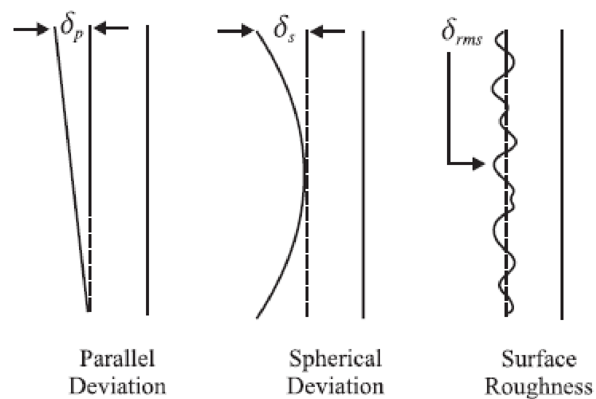


Figure 2.2: Defects in FPIs. Adapted from Atherton [28]

The parallel deviation results from non-parallelism due to difference in plate separation, the spherical deviation results from bowing of the plate, and the surface roughness deviation results from a non-ideal surface.

The treatment of both parallel and spherical deviations can be understood by first breaking up the non-ideal surface into infinitesimal areal elements of width d_x and d_y.

Each of these elements can then be considered to be perfectly parallel to the opposite perfect surface, creating a separate Fabry-Perot interferometer, with its own gap d_g. Bandwidth of each of these elements is calculated and then summed up.

The method for calculating the effects of defects for non-ideal devices is to use contributions to modify the finesse of the ideal device (F_R), which is dependent only on the reflectivity of the surfaces for the ideal case, by introducing the term defect finesse,

$$\frac{1}{F_E^2} = \frac{1}{F_R^2} + \frac{1}{F_D^2} \tag{2.6}$$

where F_E is the effective finesse of the imperfect device. The defect finesse term is composed of three terms associated with each type of defect,

$$\frac{1}{F_D^2} = \frac{1}{F_P^2} + \frac{1}{F_S^2} + \frac{1}{F_{rms}^2} \tag{2.7}$$

Each term is defined as

$$F_p = \frac{\lambda}{3^{3/2}\ \delta_p} \tag{2.8}$$

$$F_S = \frac{\lambda}{2\ \delta_s} \tag{2.9}$$

$$F_{rms} = \frac{\lambda}{4.7\ \delta_{rms}} \tag{2.10}$$

As can be seen from the equations 2.6 and 2.7, just as in the case of resistors in parallel the smallest resistor dominates, the smallest finesse term dominates the effective finesse of the device. In order to predict the filtering behavior of non-ideal

devices, the effective finesse is substituted for reflective finesse in equation 2.5 to produce

$$FWHM = \frac{\lambda(1 - R_E)}{n\,\pi\,\sqrt{R_E}} = \frac{\lambda}{n\,F_E} \qquad (2.11)$$

Therefore, in design and fabrication of Fabry-Perot interferometers, it is necessary to increase the effective finesse by increasing the reflectivity of the plates and reducing the defects. This would produce the smallest bandpass filtering necessary for accurate detection of absorption peaks and emissions.

Unlike other types of optical filters, the Fabry-Perot interferometer can be designed not to be polarization dependent. As described in the literature [32], the polarization dependence of FPI depends on the incidence angle. If the device and the whole system is designed to have normal incidence on the reflective surface of the interferometer, then the filter is completely polarization independent. This feature is extremely useful when using the non-polarized emission from thermal sources such as black bodies for spectroscopy.

2.4 Bragg Reflectors

Reflectors usable in the MWIR have to be composed of dielectric Bragg reflectors, which consist of pairs of alternating materials with high and low index of refraction, thickness of each layer equal to a quarter of central wavelength [33].

The basic principle of the Bragg reflectors is the same as the Fabry-Perot interferometer, the destructive and constructive interference of beams within each

stack based on the change of phase with each boundary [34]. Traditional dielectric Bragg reflectors are designed so that the thickness of each layer is equal to multiples of the quarter wavelength of the central wavelength of interest [35].

The reflectivity, R, of such a stack is given by Eq. 2.12 [35],

$$\mathbf{R} = \left[\frac{\mathbf{n_0}(\mathbf{n_2})^{2N} - \mathbf{n_s}(\mathbf{n_1})^{2N}}{\mathbf{n_0}(\mathbf{n_2})^{2N} + \mathbf{n_s}(\mathbf{n_1})^{2N}}\right]^2 \tag{2.12}$$

where n_0 is the index of refraction of the incident media, n_1 and n_2 are indices of refraction of the two materials that make up the stack, and n_s is the index of refraction of the substrate. The reflectivity is increased with a higher number (N) of high-low refraction pairs and an increase in the difference in the index of refraction of the two materials.

As was stated in the previous section, the optical filter part would have to consist of a tunable Fabry-Perot interferometer. Such a device includes two mirrors separated by distance d_{cav}, and primarily wavelengths of $\lambda = 2*d_{cav}$ are transmitted.

To make the fabrication of the devices less complex, standard MEMS materials (silicon, silicon dioxide, silicon nitride) as well as germanium have to be used. Refractive indices of these materials in MWIR range, 2-7 µm, are shown in the Figure 2.3 below:

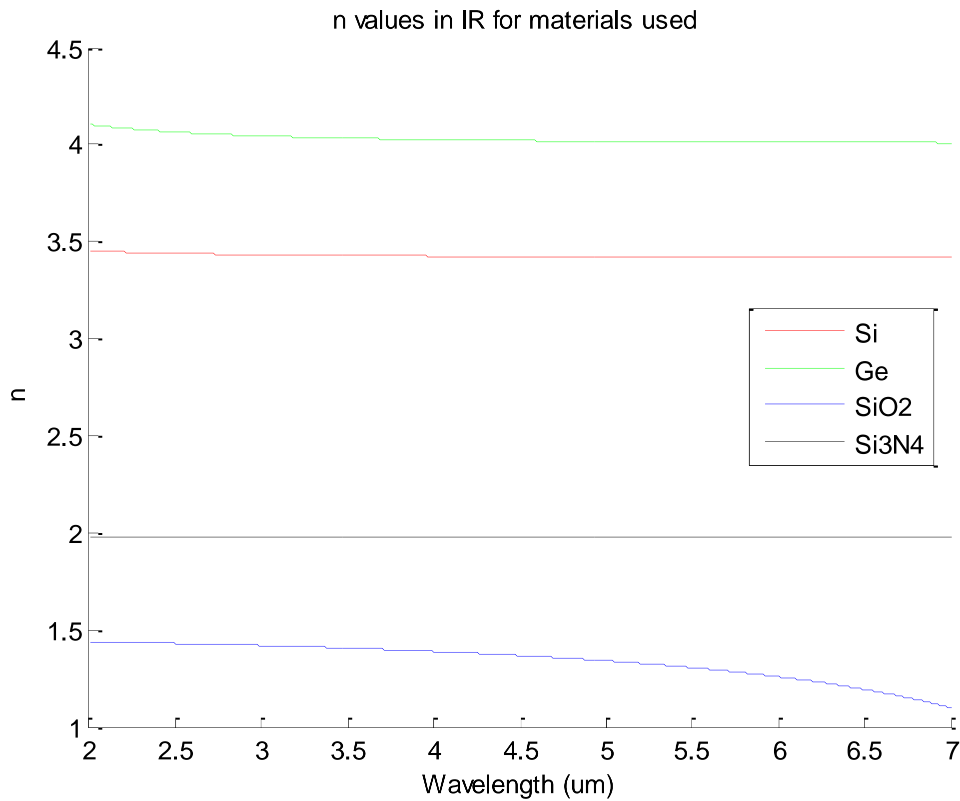


Figure 2.3: Indices of refraction of common materials

For the Fabry-Perot interferometer to have the best characteristics (such as selectivity, width of operational range, and maximum transmittance at the desired wavelength) it is best to have the reflectivity of mirrors shown in Figure 2.1 as high as possible. Although some groups have tried to use thin metal coatings for the mirrors of a Fabry-Perot Interferometer (FPI), they have found that performance is greatly non-linear and absorption is quite high [36]. For the materials above, index of refraction does not change that greatly in the wavelength region of interest, and absorption for all materials (with exception of Ge) is quite negligible.

So, if metal coatings are not to be used as reflective surfaces, then Bragg stacks have to be used. Bragg stacks are stacks of alternating high and low index materials. For the highest reflectivity, several conditions have to be met. One is that difference in index between successive layers is as high as possible. Second, layers have to be of quarter-wavelength thick – this means $d = \lambda/(4*n)$ (here, one has to take index of refraction into account – geometric thickness of $\lambda/4$ is different from optical thickness $\lambda/(4*n)$).

Utilizing the requirements above, Bragg stack has to be made with layers of lowest n material – in this range, silicon dioxide – and highest n material, germanium. Thicknesses used for trial design around 4 μm wavelength are d_{SiO2}=0.720 μm and d_{Ge}=0.248 μm, thicknesses that are easy to deposit using standard IC processing equipment.

Insertion losses can be quite high for Bragg stacks, mainly due to reflectance resulting from difference in n of incident medium (air) and first layer of Bragg stack. To counteract this effect, an anti-reflection coating (ARC) is utilized. Such coatings should have n of geometric mean of two indices, and be of $\lambda/2$ thickness.

For the Bragg stack in our design, insertion from air (n=1) into Ge (n=4.0249 @ λ=4 μm) would require ARC with n=2 @ λ=4 μm, and this is almost precisely the index of refraction of silicon nitride (n=1.974 @λ=4 μm).

Chapter 3 : Device Design

3.1 Introduction

This chapter will transition from general overview of optical filters, and particularly filters for the use in the mid-wave infrared region, 3-5 μm, to the considerations of the particular device that was developed. It will describe the choice of components and overall design of the device, especially integration of optical and mechanical requirements. Optical simulations are presented, as well as fabrication and modeling of the first prototype using commercial foundry.

3.2 Requirements

The overall goal of this project is the fabrication of the Fabry-Perot filter integrated with HgCdTe detector and CMOS circuitry, as shown in the Fig.3.1. The device that was fabricated as filter is a MEMS interferometer based on mechanical parts consisting of one movable membrane, supported by springs at the corners (X-beam) and one stationary membrane [37].

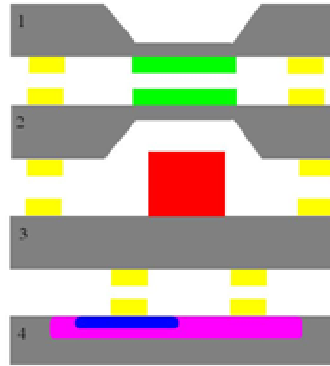


Figure 3.1: Proposed integration mechanism to create a complete device out of filter layers (1 and 2), HgCdTe detector layer (3) and CMOS control and logic layer (4).

The cavity length is changed by electrostatically moving the suspended membrane with respect to the stationary one. In electrostatic actuation, the maximum usable voltage of actuation, pull-in voltage, is defined in Eq. 3.1 [38, 39], where t is the thickness of the membrane and springs.

$$V_{PI} = \sqrt{\frac{4\,x_o^2}{9\,C}\frac{Ewt^3}{l^3}} \;\propto\; t^{\frac{3}{2}} \tag{3.1}$$

The actuation voltage increases with increased thickness of the springs. It is the goal of this project to create devices that can be actuated with the lowest possible voltages, preferably under the range of CMOS circuitry. Therefore, the thickness of the springs has to be minimal.

The absorption losses in the FPI devices depend on the absorption coefficients of materials used and the thickness of layers. The optical design dictates that the

thickness of the silicon layer, which serves only as a mechanical and stress-absorption layer, should be kept to a minimum.

3.3 Optical Design

Following the design steps described above, reflectivities of several configurations have been calculated using λ=4 μm as a design parameter. These spectra are presented in the figure 3.2 below. The spectra were computed using a matrix method for dielectric Bragg reflectors [40], and the MATLAB code is presented in Appendix A.

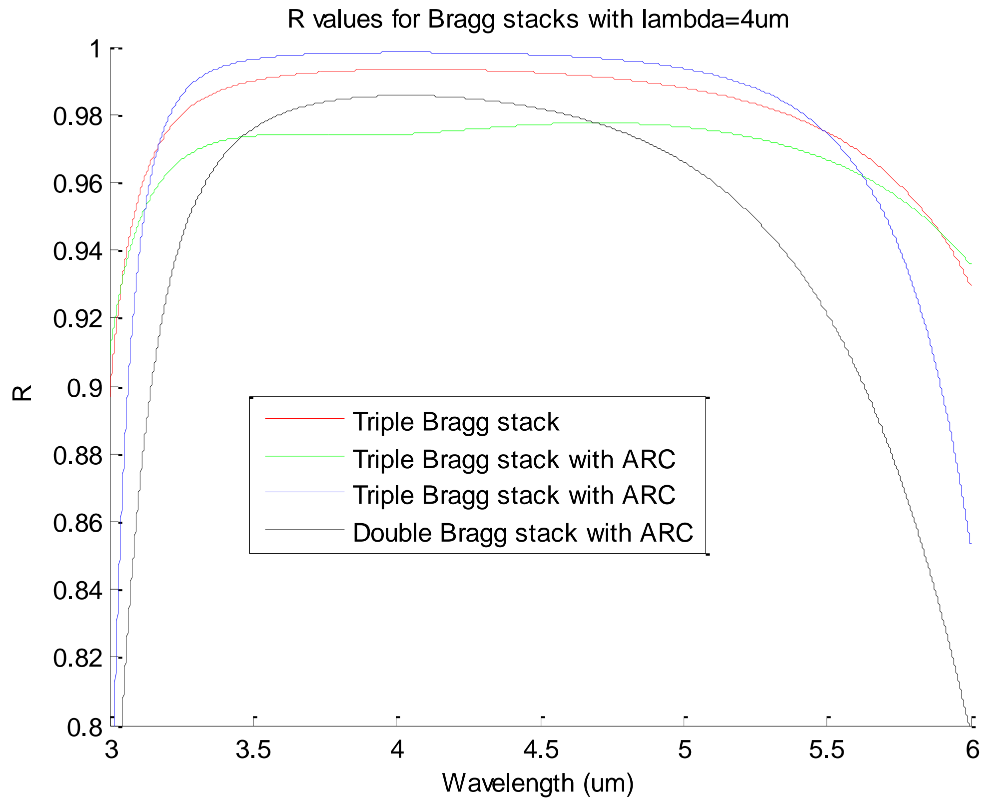


Figure 3.2: Simulations of Bragg reflectors

The first curve (red) is triple stack of Ge-SiO_2 quarter-wave layers, with germanium thickness of 250 nm and silicon oxide thickness of 720 nm. Second curve (green) shows effect of adding ARC next to Ge layer– the curve is slightly widened. Third curve, blue, represents effect of adding ARC next to SiO_2 layer – the curve is significantly widened and is more uniform in the range. If it is impossible to utilize triple stack (fabrication constraints), double stack was modeled as the final curve, black.

Figure 3.3 below provides cross-sections of these stacks:

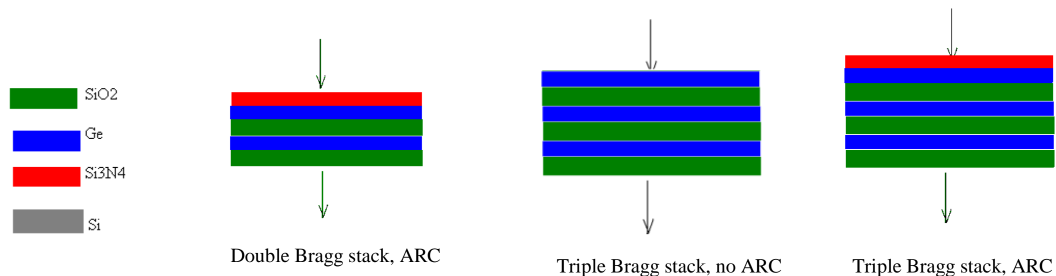


Figure 3.3: Bragg reflectors

Using this data and Bragg stacks designed around λ=4 μm, the entire Fabry-Perot device was modeled.

3.4 Optical Simulations

The perfect Fabry-Perot interferometer can be approximated as a dielectric Bragg reflector, with one of the layers (the gap) being air. Therefore, to study the optical behavior of Fabry-Perot interferometers, the code used to compute reflectivities of the Bragg stacks was modified. While modeling the Airy function as a separate program with input of calculated reflectivities based on Bragg stack simulations is possible, the best effect is achieved by putting all the system in a single simulation. This requires addition of the silicon layers to the Bragg stack calculations, and treating the air gap as just another layer with index of refraction of air. The code is included in Appendix A.

From the reflectivity data obtained in the simulations, R=98% over 3-5 μm region, the finesse is calculated to be 155, with the FWHM at λ=4 μm, calculated using Eq. 2.11 to be 27 nm.

If the device consists of nothing more than two Bragg stacks (with appropriate ARCs) and a mechanically tuned cavity, performance is quite good, as expected from literature [24]. Simulations of this device with cavity length d_{Cav}=2 μm is in the figure 3.4 below:

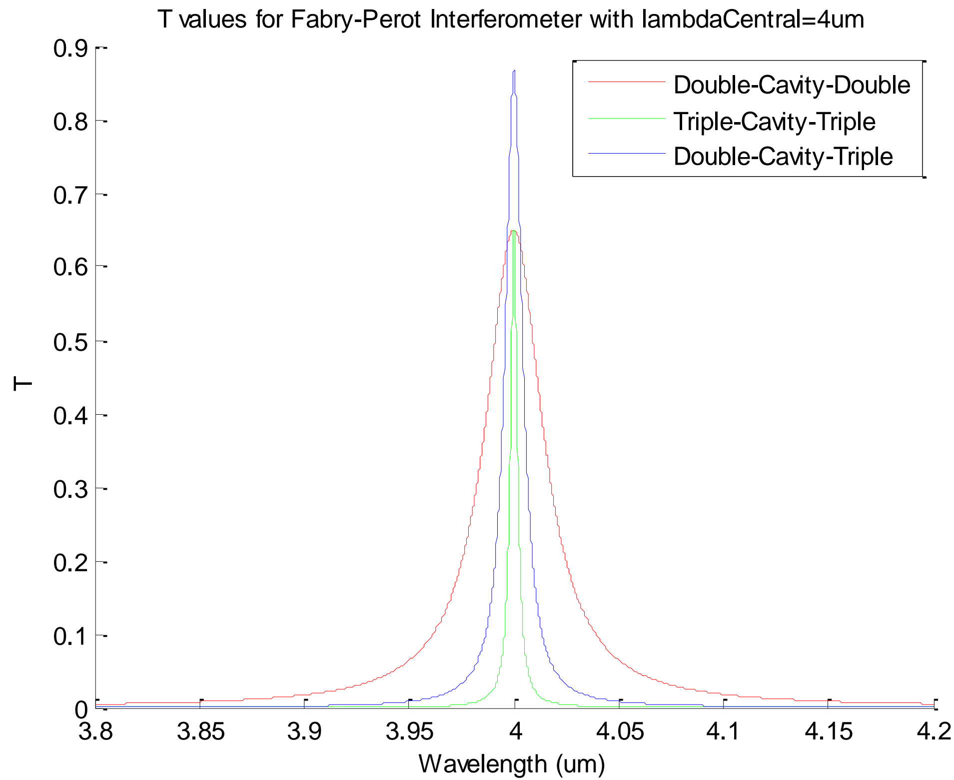


Figure 3.4: FPI simulations

The red line represents FPI using double Bragg stacks as reflectors. Green line represents same device, but Bragg stacks are triple. Blue line represents FPI using asymmetrical, double-triple Bragg stacks. As can be seen from these curves, selectivity improves greatly when using triple stacks over double stacks. The most interesting figure is asymmetrical FPI, as literature states that best transmissions are achievable when mirrors are perfectly equal. In this case, transmission and selectivity were improved by using an asymmetrical stack.

Cross-section of Double-Cavity-Triple FPI used to generate blue line of the Figure 3.4 is below in figure 3.5.

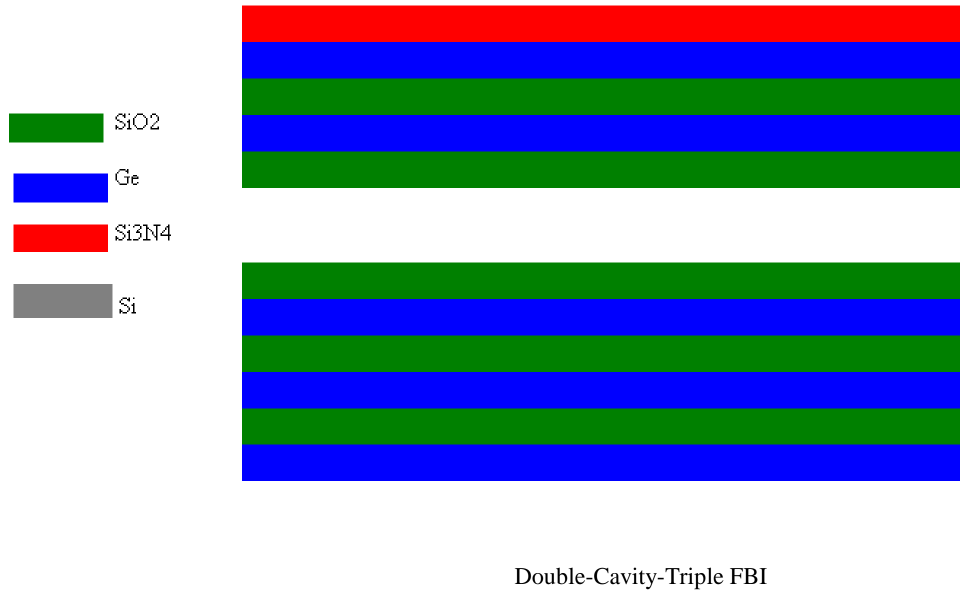


Figure 3.5: Layers in Double-Triple cavity FPI

Utilizing design inputs described below, in the mechanical section, it was determined that silicon is to be utilized as the structural material. Addition of this layer might degrade performance of the FPI. As described below, SOI wafers with structural layer thickness of d_{struct}=10 μm are to be used (at this stage of design). From initial analysis, introduction of this element might be tolerable, as this thickness is a multiple of half design wavelength, λ=4 μm: $d=(4/(2n))*m=(4/(2*3.425))*17$.

Curves below are simulation of device performance, with cavity width = 2 μm:

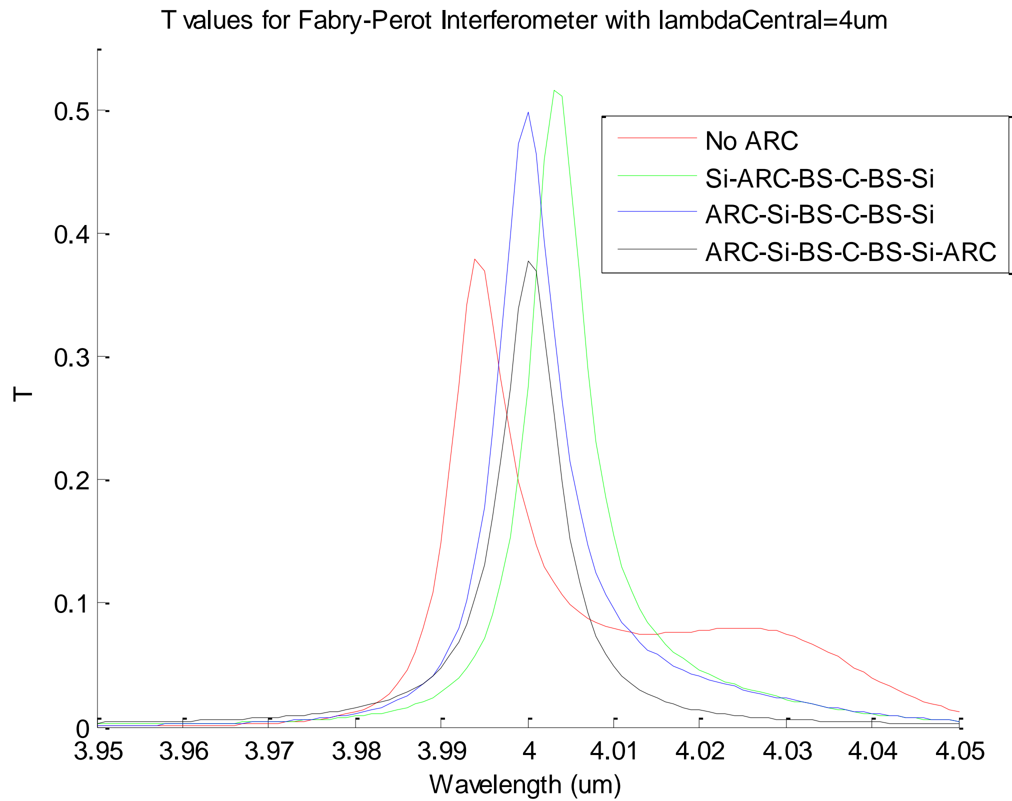
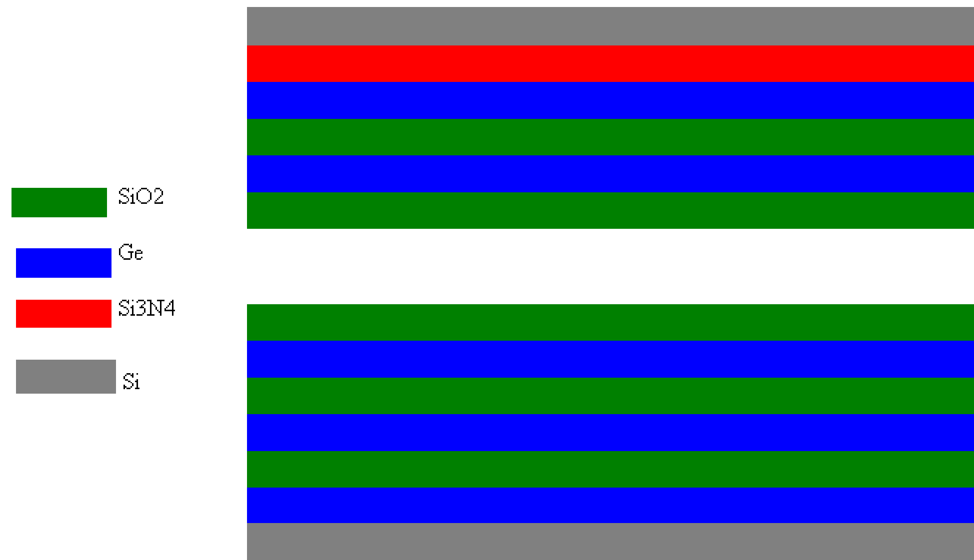


Figure 3.6: FPI simulations with addition of silicon layer

The red curve is 2-3 stack without Si_3N_4 ARC added between diaphragm and Bragg stack; green curve is 2-3 stack with ARC added after the diaphragm; blue curve is 2-3 stack with ARC added before the diaphragm; black curve shows addition of ARC to the back side of the FPI.

Analysis of the simulations above demonstrates that although silicon structural layers do degrade peak transmittance of FPI (FWHM of 0.5µm vs 0.89µm without silicon), ARC coating prevents further degradation.

Cross-section of Si-ARC-BS-C-BS-Si is below in Fig. 3.7:



Si-ARC-BS-C-BS-Si FPI

Figure 3.7: Layers for FPI device

The results from the optical simulations above that include the effect of the silicon layer don't correspond to the finesse-based calculations of FWHM because the finesse based calculation does not include the filtering effect provided by the silicon layer. The silicon layer acts as its own Fabry-Perot etalon, and its effect can be seen only by the comprehensive optical simulation developed here.

The final simulation run for this design is the simulation of changing cavity length (done mechanically) for the FPI designed with central wavelength of $\lambda=4$ µm. Results are presented in Fig. 3.8:

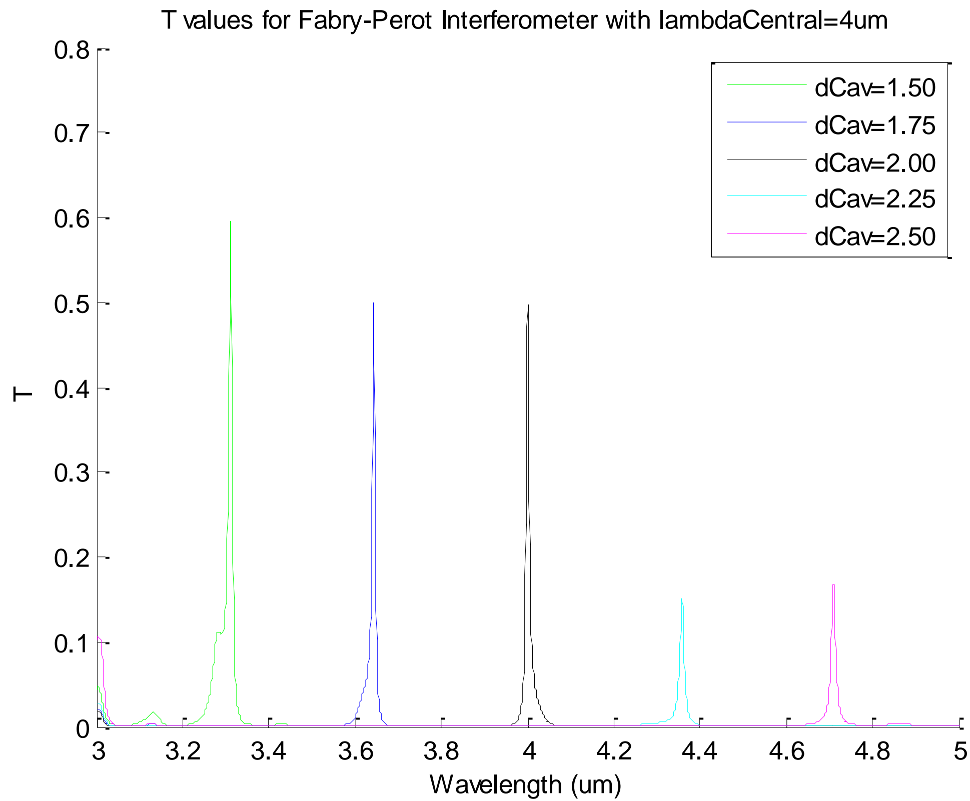


Figure 3.8: Transmission simulations for FPI device

These curves represent changing the cavity width from 1.50 μm (green) to 2.5 μm (magenta) in steps of 0.25 μm. This would effectively cover the range from 3 μm to 5 μm. As expected, wavelength selectivity is demonstrated in transmission. For this design, at d=2 μm, FWHM is 0.007 μm, comparable to 0.1 μm claimed by InfraTec [23].

3.5 Conclusion

In conclusion, software has been written that allows simulation of FPI and Bragg stacks, separately and then as an integrated device. This allows fast design checks and optimization of the optical part of the device. This project design of a FPI with central wavelength of 4 µm, and performance of this device has been shown to be acceptable as a narrow-band tunable filter for the MWIR, to be utilized as a chemical sensor or thermal imaging.

Chapter 4 Mechanical Design

4.1 Introduction

While there are multiple ways of supporting a membrane by springs, traditionally in MEMS, cantilever beams are used [38]. The deformation of these beams is widely studied [39], and allows useful design, given mechanical constants. While folded spring designs would provide a low mechanical constant and therefore low actuation forces, in order to increase defect finesse of the Fabry-Perot interferometer the surfaces have to be kept as parallel as possible [41], which folded spring design fails to do [42]. In previous work in our group [43], it has been determined that the X-beam arrangement of springs provides the best uniformity of movement, at the expense of high actuation forces. Therefore, for this project, the mechanical design was chosen as a square plate suspended by four cantilever beams at the corners. By varying the length and width of the beams different mechanical stiffness can be achieved, as described in Eq. 4.1. For best optical performance, it is necessary to keep the plate as flat as possible. The plate acts as a spring by itself, and can be deformed upon actuation; therefore it was necessary to find a design that provides for the most mechanical deformation of the springs while keeping the plate sufficiently stiff, balanced with minimizing actuation voltage given by Eq. 3.1.

$$k = \frac{E\,w\,t^3}{l^3} \tag{4.1}$$

4.2 Electrostatic actuation

One of the most common means of actuating MEMS devices composed of large parallel plates is the electrostatic actuation [39]. This method is based on charge accumulation on two electrically separated plates that compose a capacitor. When a voltage source is connected to the plates, charges of opposite polarity accumulate on two separated surfaces, as shown in Fig. 4.1.

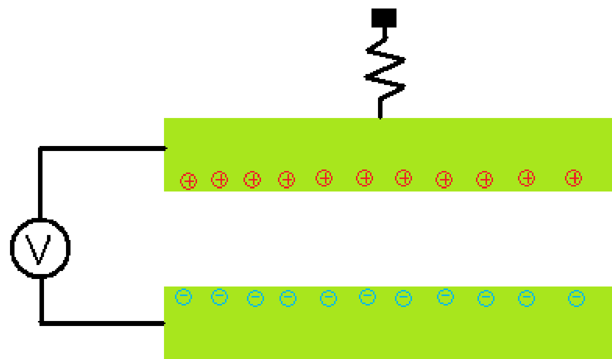


Figure 4.1 General view of electrostatic actuation

The attraction of opposite charges, described by the Coulomb equation [44], creates mechanical force from electrical input. When one of the plates is fixed, and the other is suspended by linear springs, the electrostatic force creates attractive force that pushes the plates together, while the mechanical force of the springs creates mechanical restoring force that opposes the movement. When the two forces are equal, equilibrium is reached and the system is stable. The mechanical restoring force is based on deformation of the spring and follows linear Hooke's law, while the attractive electrostatic force follows Coulomb's equation. Up until the distance of a third of the gap, in any configuration, the mechanical linear force dominates, and the

movement is linear. Past the distance of a third of the gap electrostatic force dominates over the restoring force, producing effect of “pull-in”, or uncontrollable collision of the two plates. Therefore, electrostatic actuation is limited to only one third of the original gap. For the design of FPI device with starting gap of 2.5 μm, this translates into controllable movement over 0.833 μm, to final gap of 1.67 μm.

4.3 MUMPS Prototype

4.3.1 MUMPS process

In order to study the mechanical behavior of the proposed device and develop realistic mechanical models, a high-level mechanical prototype is used. Also, the fabrication process used for the prototype would be a good starting point for development of custom fabrication process for complete devices.

The process for the fabrication of the prototype is the commercial MUMPS (Multi-User MEMS Processes) SOI (Silicon-on-Insulator) process, developed by MEMSCAP, that uses silicon-on-insulator wafers as the substrate [45]. The fabrication process was developed to address as many needs of designers as possible by allowing them to change only the geometry of devices, but not the layer thicknesses. The diagram that indicates all the layers of devices produced by this process is shown in Fig. 4.2.

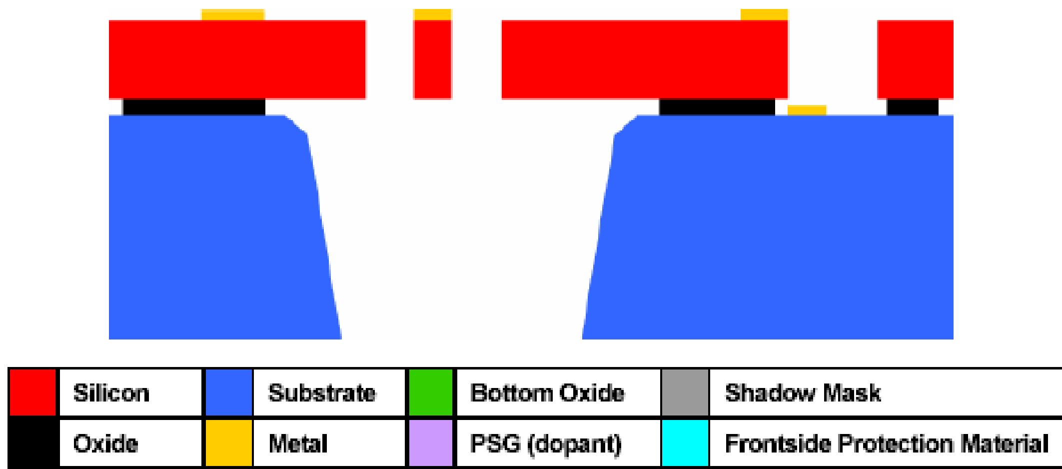


Figure 4.2: MUMPS SOI process [45]

4.3.2 Layout

Taking into consideration the requirements of the project and the limitations of the MUMPS process, the initial device was designed to act as a high-level mechanical prototype.

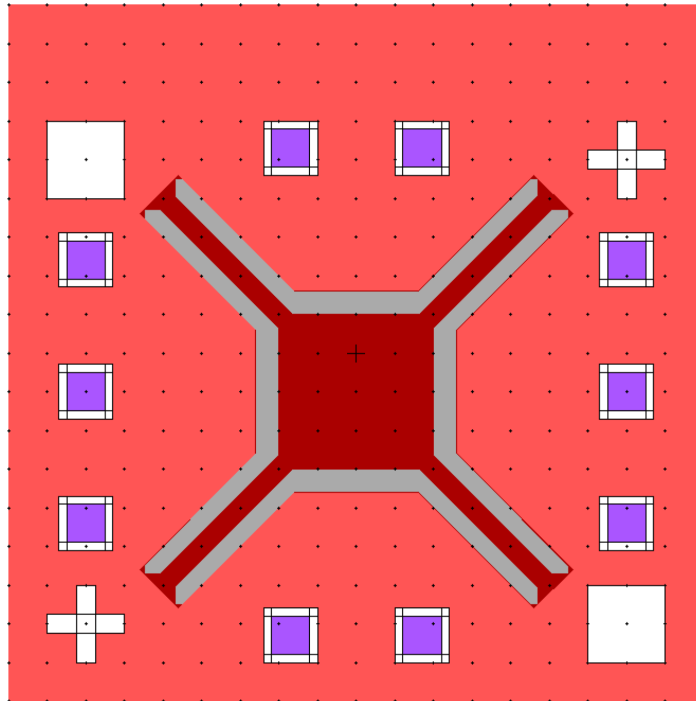


Figure 4.3: Layout for MUMPS device

The method of making these parts into a mechanical prototype of the device involves bonding two identical chips. This is made possible by the metal pads (purple color in the figure above) that are 1.6 μm thick. Therefore, if the chips are aligned with each other, the separation between them would be 3.2 μm, allowing a test in the MWIR range.

4.3.3 Mechanical modeling and testing

Although this prototype would not be a perfect optical filter, it would provide us with information about the realistic deformation of the plate. In our simulations, the best variation that could be achieved was 600 nm from center to edge in the 2 mm square plate. A figure of this simulation is below.

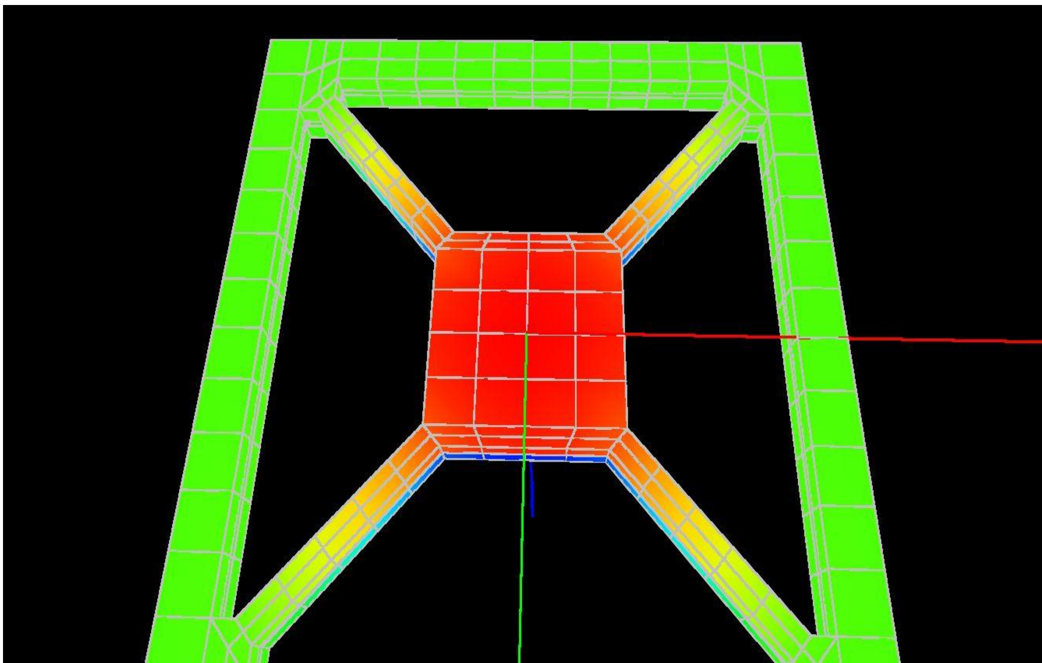


Figure 4.4: FEA model of X-beam

Although the plate curvature does not seem significant, it could introduce unwanted optical effects into the filter. From the curvature of the plates, the reflective finesse is 3.3, the finesse term due to curvature is 0.181, and the effective finesse is 0.18, resulting in FWHM= 22 μm.

The optical behavior of the prototype has been simulated using Matlab software, and the behavior is shown in the figure below:

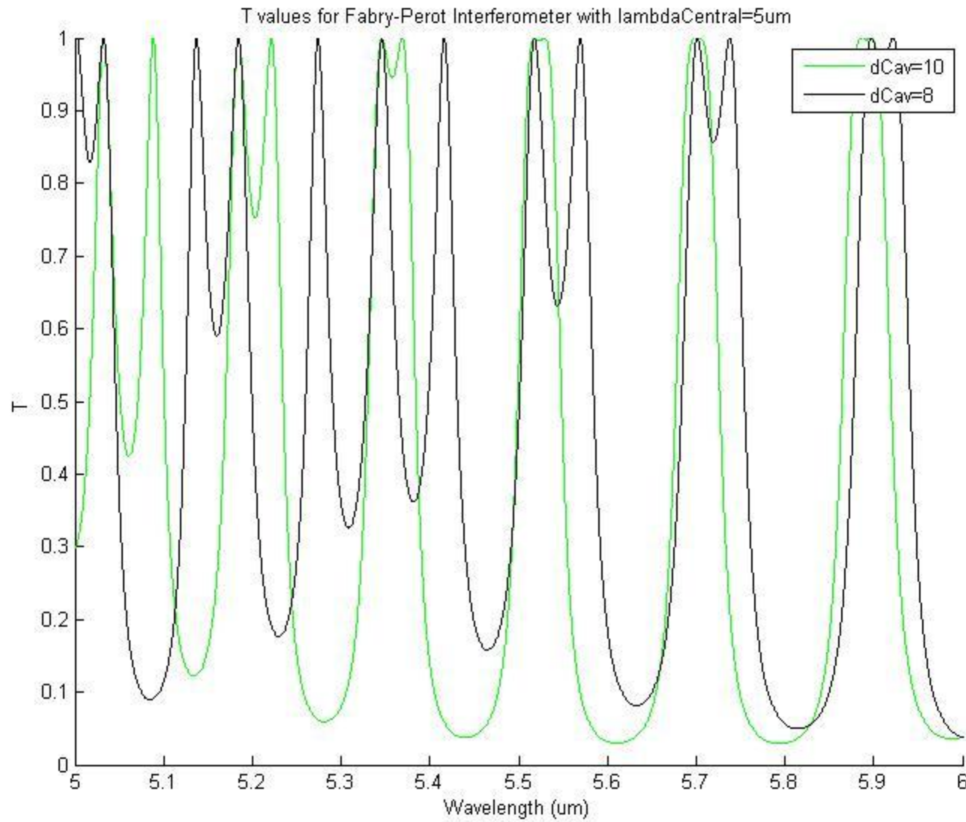


Figure 4.5: Simulation of optical behavior of MUMPS X-beam

This figure represents behavior of the filter as the wavelength is scanned from 5 μm to 6 μm, with the undeformed cavity length being 10 μm (green line) and 8 μm (black line).

The design, analysis and simulation of the first mechanical prototype has given valuable insight into the mechanical behavior of plates suspended by springs fabricated on SOI wafers. Low reflectivity of silicon surfaces and high curvature of

the membrane makes this an unacceptable optical prototype. To create a device that would have good optical performance, a custom process needs to be developed that addresses these issues, by incorporating highly reflective surfaces and minimizing the curvature of the membrane.

Chapter 5 : First fabrication run

5.1 Introduction

In the previous chapters, it was determined that the best materials for the Bragg reflectors are to be germanium and silicon oxide. This chapter will describe how by using several different methods of deposition, it was determined that the lowest stress per dielectric pair is 100 MPa of compressive stress. With a thin supporting membrane, this leads to bowing of the mirrors and decreases resolution of the device. The thickness of the silicon layer has to be thick enough to reduce the stress bowing to a minimum.

The experiments were performed at Stanford Nanofabrication Facility (SNF). The main point of this part of the project was finding the fabrication flow that combines the least expensive methods (i.e. wet etching instead of dry etching) and the substrate thickness that will be just thick enough to reduce the stress bowing, but will not increase significantly the actuation voltages and absorption losses of the device.

5.2 Considerations for process development

Although silicon nitride has been used as structural material in UWA group [46-48], other materials have to be used, as silicon nitride has good optical properties, but has too much stress for use as structural layer. Instead of spending time and funds developing low-stress silicon nitride deposition process (UWA), we decided to use a

more well-known and more widely available (equals less expensive) materials, such as silicon layer in SOI wafers. Also, as X-Beams have been finalized as springs for the mechanical design, this requires material that is more inelastically deformable, and silicon is a better candidate.

As was stated in the previous chapter, the optimal Bragg stack would be double-triple Bragg stack with germanium and silicon oxide alternating layers, with silicon membrane and silicon nitride anti-reflective coating.

Research has been conducted into determining what methods of deposition of these materials would be best for optical device.

In general, there are several tools available for deposition of dielectric layers [49]: CVD (chemical vapor deposition), PECVD (plasma-enhanced CVD), epitaxial (slow growth of single-crystal layer), sputtering, and other more exotic methods. Almost all of these methods are available to us through SNF [50].

Although UWA group has deposited all of the layers by PECVD [51], personal experience with PECVD (used extensively in previous project [52]) and literature shows that this method is not acceptable for optical-quality films. PECVD produces thick films in relatively short time, but these films are usually extremely prone to having bubbles and gradients in film quality. Such film would cause scattering and reflections, and introduce unpredictable behavior.

Epitaxial growth produces extremely uniform films, but might introduce large stress into the stack, if subsequent layers are mismatched.

There are two tools that allow deposition of germanium at the SNF. One of them, "tylansige", is a low-pressure chemical vapor deposition (LPCVD) tool that allows deposition of germanium and silicon films [53]).

Another tool that is capable of depositing germanium films is epitaxial tool, "epi" [54]. This tool is an epitaxial chamber.

Apart from the method of deposition, the main difference between these two machines is the temperature range of the processes. LPCVD tool deposits in the range of 400-650C, while epi tool uses 600-1200C range. While epitaxial tool might give superior quality film, it might not be usable for our process. High temperatures are not significant if only one film is grown, and even then substrate and deposited film have to be very carefully thermally matched. In case of our process, we are depositing consequent layers of several materials, and coefficients of thermal expansion of these films are sufficiently different as to almost guarantee problems at high temperatures (such as lamination, cracking, etc.)

After some consideration, it has been determined that the optimal deposition method is LPCVD, which is a standard IC fabrication method and therefore would have more standard recipes.

Silicon oxide could be deposited on several tools, but considerations of contamination between machines, as established by SNF guidelines, guide towards use of the "teos" tool [55]. This is a standard tool, and used a low-temperature recipe.

Silicon nitride can be deposited on “tylannitride” [56]. This is a standard tool, and numerous recipes have been developed by SNF staff, including low-stress nitride film.

Patterning of various films used in the process can be done in one tool, “p5000etch” [57], which is a versatile tool used for deep reactive ion etching of various materials.

Photolithography was done on the standard track at SNF, utilizing the KarlSuss aligner for exposure (resolution and alignment precision down to 0.5 microns).

Contamination rules at SNF are as follows [58]: all tools are split into three groups, “clean”, “semiclean” and “contaminated”. Wafers usually start off as “clean”, and move down the rating depending on the processing. Once a wafer is processed on “semiclean” tool, it cannot be processed on “clean”, and so on. The process flow that has been designed follows these contamination rules.

5.3 Initial process

Process flow has been designed that would allow one to fabricate a Fabry-Perot interferometer that would replicate the device designed previously. In the process of design, several things were taken into effect: capability of tools at SNF, quality of films produced, and simplicity of the process. The simpler the process, the more robust it is. The more standard processes are used, that much easier to transfer fabrication from research facility to commercial fab, and therefore lower costs. As many common steps as possible have been used, and number of masks has been minimized.

Figures 4.1-4.8 below have been generated using SoftMems, commercial add-on to LEdit.

Step 1: we are starting off with two SOI wafers, with substrate thickness of 400 microns, 1 micron of silicon oxide as the isolation layer, and 25 microns of "device" layer. (Layer thicknesses are intentionally not to scale, as 400 microns of substrate layer would make 0.4 microns of germanium invisible). Legend for material colors is included.

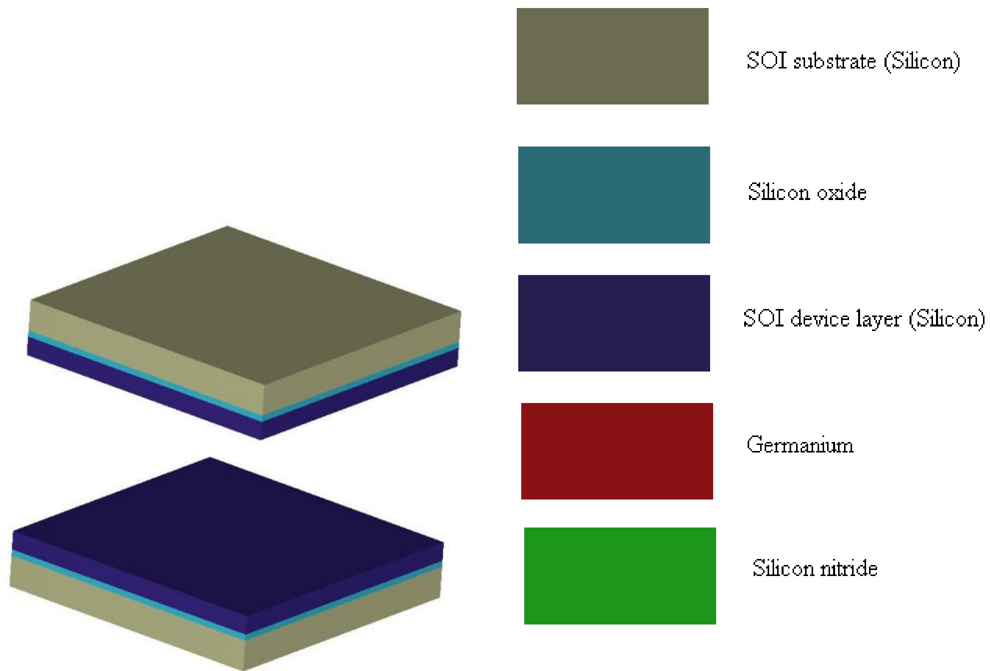


Figure 5.1: Starting SOI substrate

Step 2: (Next series of steps are combined into Step 2) deposits consequent germanium and silicon oxide layers on appropriate sides of the wafers:

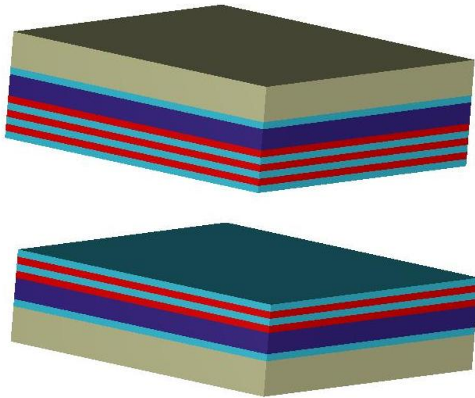


Figure 5.2: SOI with Bragg stacks

Step 3: uses Mask1 to etch the Bragg stack on lower wafer, leaving the layers only in the area of the active device:

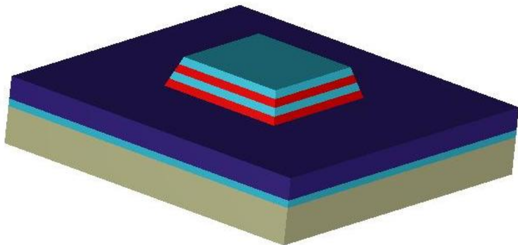


Figure 5.3: Substrate with etched Bragg stack

Step 4: uses Mask2 to etch the backsides of both wafers. Here, same mask and same etching process are utilized.

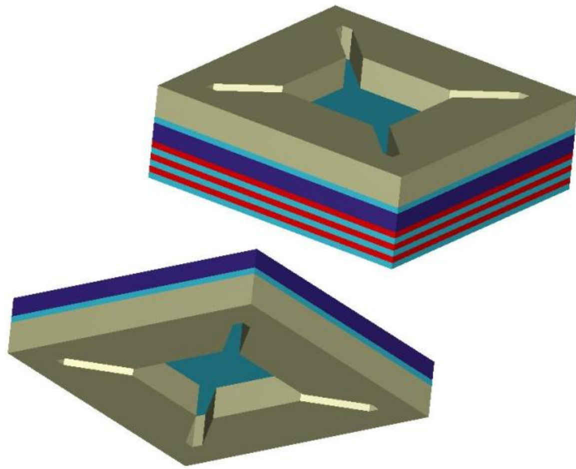


Figure 5.4: Backside etching

Step 5: uses Mask3 to etch the top of lower wafer to produce the device:

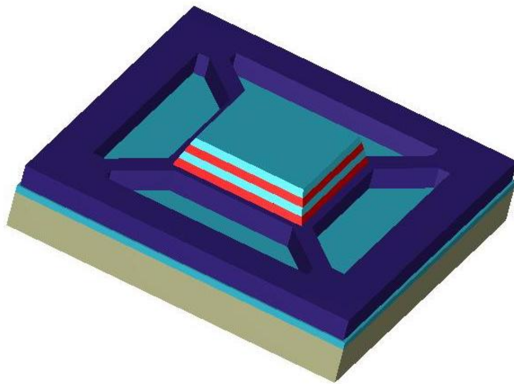


Figure 5.5: Unreleased X-beam

Step 6: uses wet etch on top wafer to etch away the exposed silicon oxide:

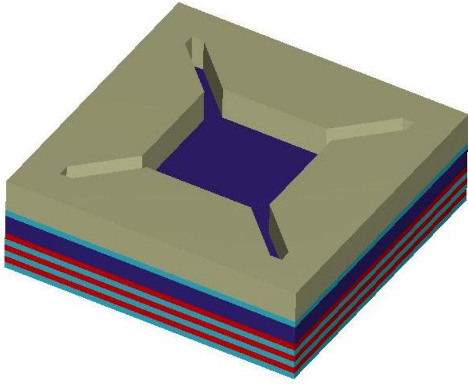


Figure 5.6: Released X-beam

Step 7: deposits silicon nitride on top wafer, creating anti-reflective coating:

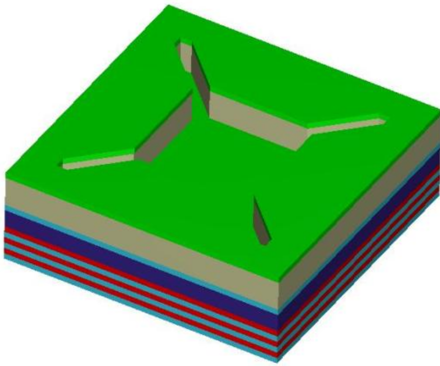


Figure 5.7: Addition of silicon nitride layer

Step 8: bonding of the wafers:

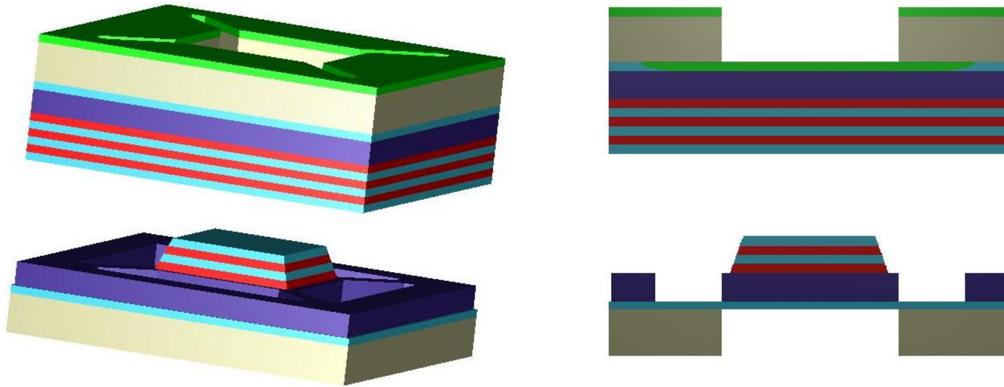


Figure 5.8: Two parts of the Fabry-Perot interferometer

Step 9: following dicing of the wafer, the membrane is released using HF bath.

In Step 8, the method of bonding was omitted. It was our plan to use simple dry-resist bonding for the first batch of devices, and move on to metal-to-metal or anodic bonding in the final fabrication process, requiring one additional mask. Also, for bonding to detector, additional metal layers would have to be deposited and patterned on the back side of the wafer.

Although this process sounds simplistic, it would require a series of short-loop tests that verify correctness and compatibility of each step. It has been my experience in the past that even such simple process as deposition of a layer might go wrong, and serious verification is needed.

These short-loop tests are:

- Layer deposition – stress in the deposited layers, adhesion, quality
- Layer compatibility – deposition of the entire Bragg stack and verification that no peeling, cracking or other defects are present
- Proper process for back-side etching that would not damage deposited Bragg stack
- Process for membrane etching that would not damage any other layers
- Bonding
- Membrane release – usually the hardest part of any MEMS process

This process has been submitted to SNF staff and determined to be realistic and to follow SNF guidelines.

5.4 SNF Process development

After consultation with several employees at SNF, it was determined that the proposed process does not violate their procedures and use of equipment. There have been several changes, as some of the steps had to be done on other tools than originally projected. The germanium layer, as part of the Bragg stack, would not be mono-crystalline, it would be poly-crystalline or amorphous, due to its deposition on top of mis-matched silicon oxide layer. This might introduce some slight changes to the optical response of the filter.

The goals for the initial round of fabrication were primarily fabrication of Bragg stacks of single, double and triple thickness for optical testing, development of key

processes for the fabrication, and testing of commercially available SOI wafers. For the region of MWIR, the original design was centered around wavelength of 4 microns. This required germanium layers to be 250 nm thick, and silicon oxide layers to be 720 nm thick.

The final device would have this configuration:

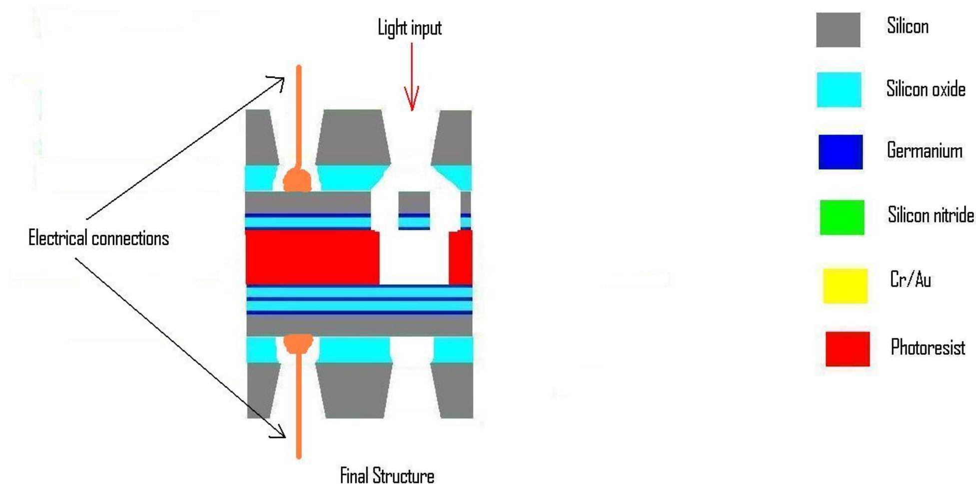


Figure 5.9: Diagram of two bonded parts with electrical connections

5.5 Mask design and layout

For the start of this process, two major masks are needed: one mask for the etching of optical windows into the backside of the wafers, and second mask for the definition of X-beam to be released.

The first mask, “Backside etch” (Fig. 5.10), consists of 20 chips, each 2 cm by 1 cm, with the following pattern: two squares, each 5.6 mm on the side. The reason for this

size is that when through-wafer etching is done on the backside, the entire device area should be open. Also, this mask could be re-used for defining thick resist used for bonding. This mask defines openings in the backside of the wafer and is used for through-wafer etching to the device layer. One of the openings is used for optical testing, and another to provide electrical contact to the device layer, as shown in the picture above. Global alignment marks are on the edges of the wafer, and each chip has four sets of local alignment marks.

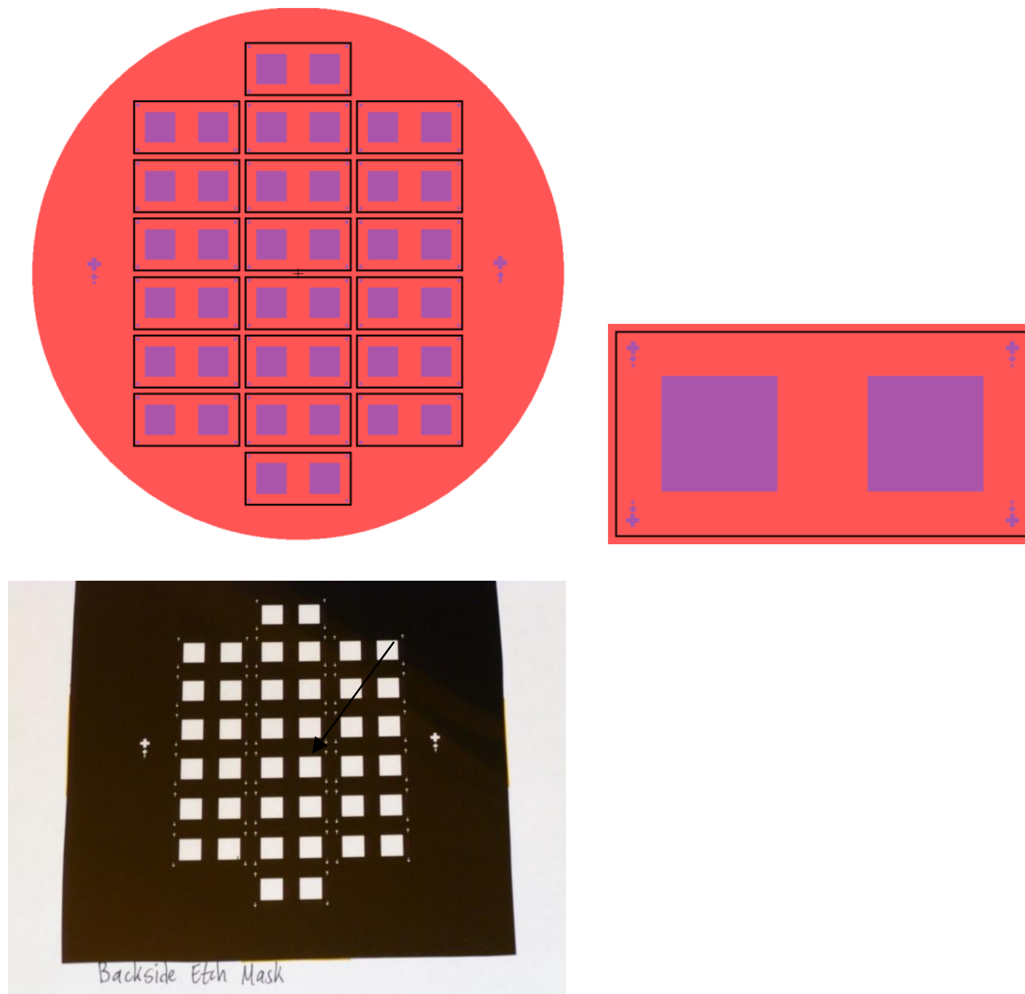


Figure 5.10: First mask layout with chip detail and actual mask

Second mask, “X-beam etch” (Fig. 5.11), follows the layout of the backside mask, and defines X-beam mechanical element to be etched through Bragg stack and device layer.

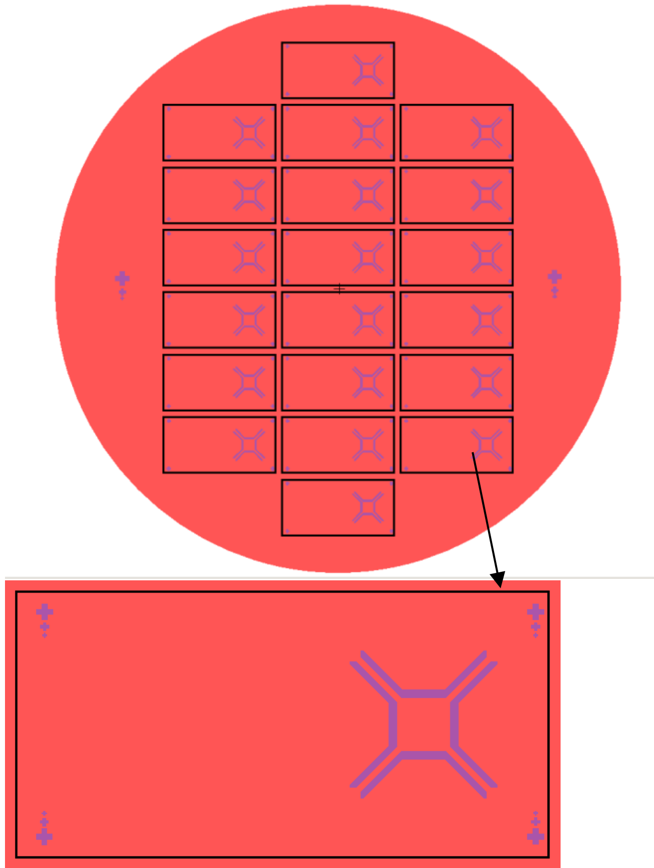


Figure 5.11: Second mask layout with chip detail

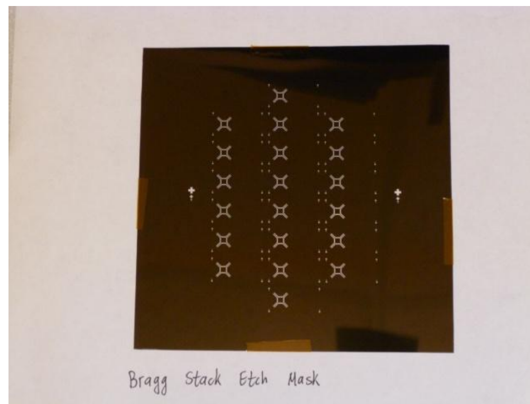


Figure 5.12: Actual mask

These two masks have been laid out using L-Edit software, and fabricated on Mylar transparent film. This provides for a quick and inexpensive trial for masks.

5.6 Fabrication requirements

The main goal was to start process development and verify separate steps, which will be used to fabricate the final device. Although at this point the focus is on obtaining samples to verify optical and mechanical designs, the eventual goal of developing a technology that can be used for multiple applications at a commercial foundry should be kept in mind. Therefore, process should be robust, wafer-scale, and able to transfer from current scale of devices (somewhat large, detector side being 2 mm square) to much smaller scale, with scale reduction by at least a factor of ten. Standard IC and MEMS fabrication steps should be used throughout, with keeping special processes to a minimum. Robustness means allowing for slight variations in

wafer thickness and uniformity, as well as chemical concentrations and etch rates. Photolithography, layer depositions, and etching should be consistent from wafer to wafer and across each wafer. Such process should be transferable to a commercial large-scale foundry for future production, so all the steps would become a standard process.

The work has two main approaches, the optical design part and the mechanical design part. The optical design involves deposition of optical component, the Bragg stack. The mechanical part is the fabrication of the carrier, the X-Beam parallel plate actuator.

5.7 Layer deposition

The Bragg stack requires alternating layers of germanium and silicon oxide. For the design of filter in MWIR (3-5 μm), the filter was designed with center wavelength of 4 μm, and that required the following layer thicknesses: germanium 250 nm, silicon oxide 720 nm, silicon nitride 500 nm. For optical purposes, such films should be as uniform and defect-free as possible. All optical design was done for monocryistalline germanium.

There are several methods for depositions of these materials, as was described above. From my previous project, the CNF-based NEMS switch, I was already trained on the metal evaporator, that allowed deposition of germanium, and the PECVD system that allowed depositions of silicon oxide and silicon nitride. Although the UWA group deposited all their dielectric layers by PECVD [51], films produced by this method have high defect density (pinholes, globules, cavities) and CVD furnaces produce

higher quality films. Advantages of PECVD systems is that they are quick (single deposition lasts 30 min to 90 min) and allow quick changing of parameters. CVD furnace systems deposit films on both sides, requiring extra steps of etching undesired films.

At SNF, there are several furnace systems for deposition of high-quality dielectric systems and epitaxial germanium films with controllable doping. Another benefit of using a CVD furnace to deposit germanium was its ability to deposit single-crystalline layers on substrates with appropriate lattice size, resulting in high-quality film. After consultation, it was determined that germanium deposited over silicon oxide would never be monocrystalline after the first layer, therefore introducing variations into the optical performance.

Figure 5.13 is the SEM image of a double Bragg stack with gold-chromium mask on top (this sample was used for etch tests).

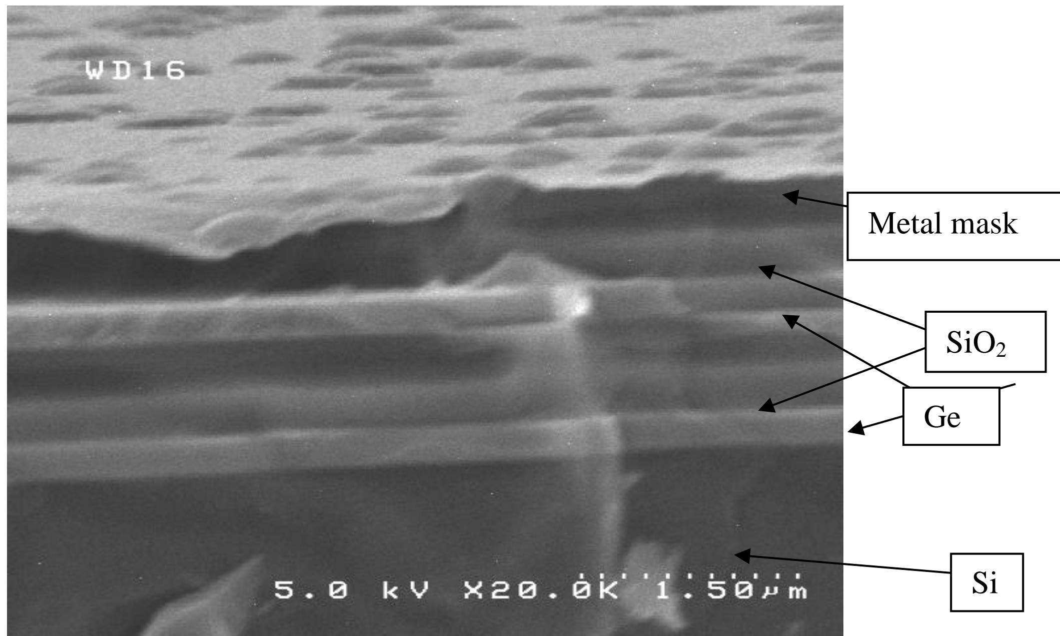


Figure 5.13: SEM image of the deposited Bragg stack

As can be seen, the layers are very uniform (no visible crystalline borders, islands, or dislocations). The only visible defect is present in the form of small bumps on the top layer of silicon oxide. These islands can be seen more clearly in Fig. 5.14.

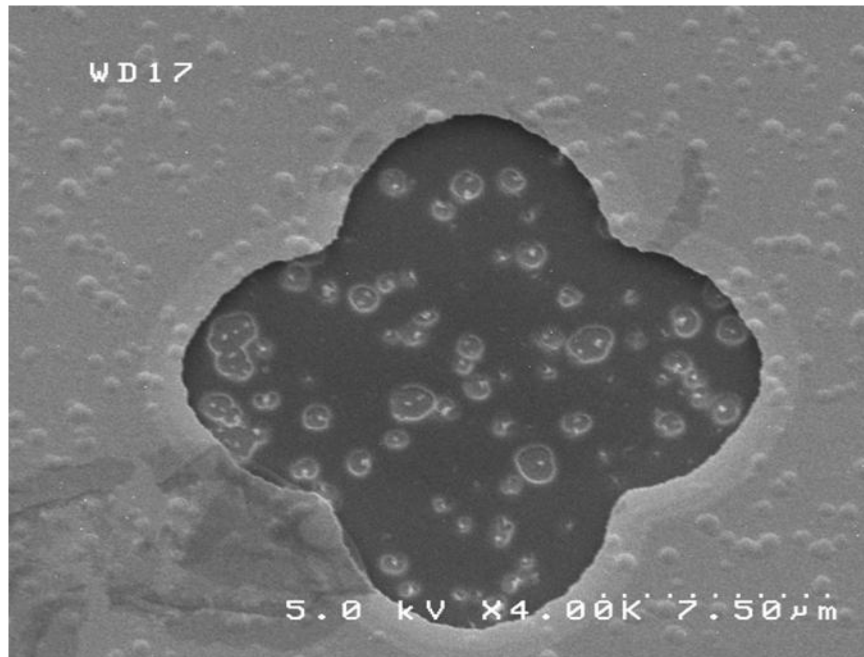


Figure 5.14: SEM image of the alignment feature after metal etch

These dots have an average diameter of 50 nm and appear evenly distributed along the surface. In the image above, one can see small “seeds” in centers of these bumps. After several attempts, I was able to get a cross-section of one of these bumps, shown in Fig. 5.15.

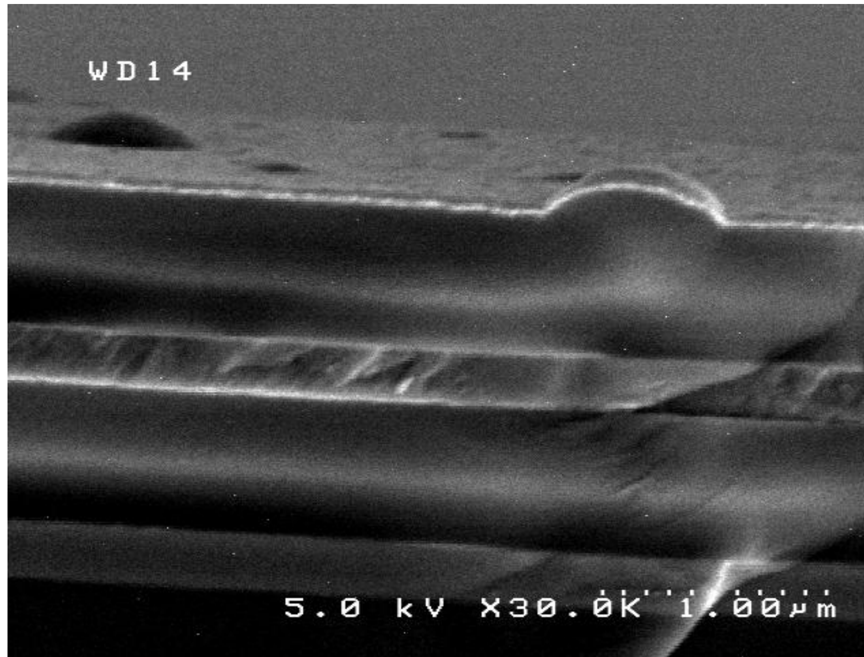


Figure 5.15: SEM image of the defects in Bragg stack

The bump appears extremely uniform; therefore it is not a hydrogen bubble which is common in PECVD systems. After several etching tests, the image below was obtained.

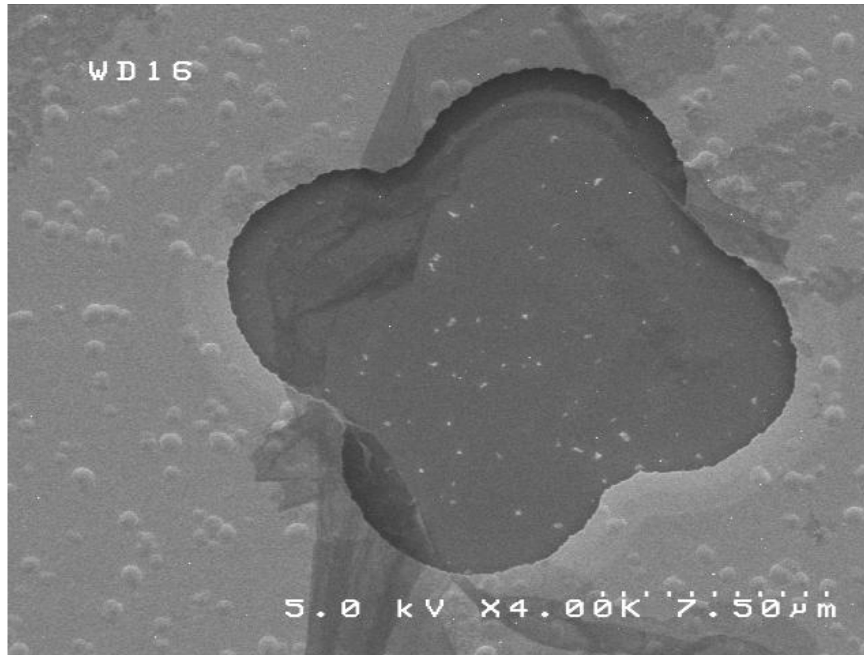


Figure 5.16: SEM image of alignment feature following Bragg stack etch

The image is the same sample as above, with silicon oxide layer etched all the way down to the germanium layer. The specks are most likely debris that settled on the surface of the wafer, and resulted in nucleation of thicker layer over them.

These bumps would be a greatly deteriorating defect in optical devices designed for smaller wavelength, but being an order of magnitude less than wavelength of interest, they might not be detrimental to the operation of our device, but could lead to differences between simulations and experimental results (see chapter 9).

Several samples have been produced, with single, double and triple Bragg stacks, with and without nitride anti-reflective coating. These samples were sent to EPIR for reflectance testing to determine if the layers are of sufficient optical quality. The results are reported later in this chapter, section 5.20.

An interesting effect of thick layer deposition was the change in the appearance of the wafer, as demonstrated in Fig. 5.17.

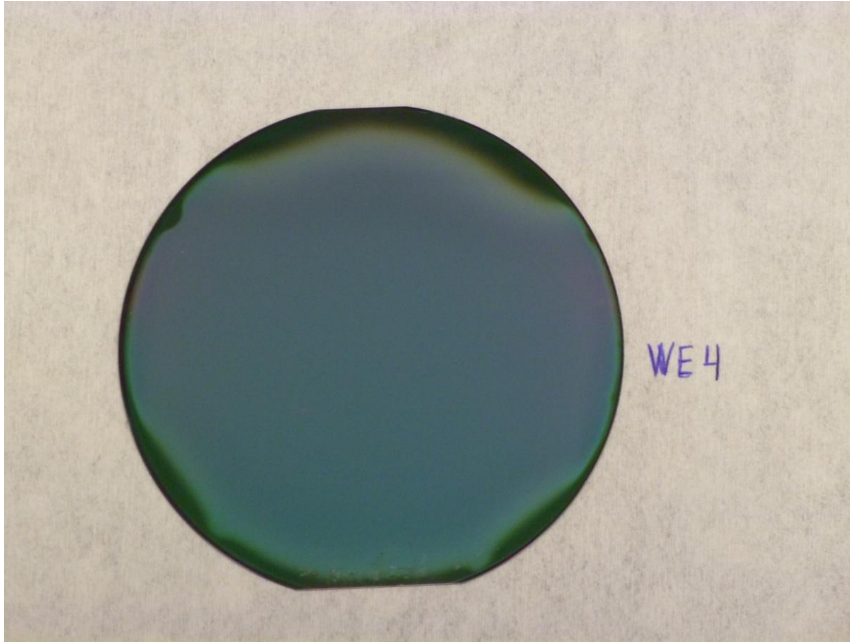


Figure 5.17: Silicon wafer with triple Bragg stack

The wafer above has triple Bragg stack. The discoloration at the edges is caused by the difference in germanium deposition area (it has 3 mm lip at the edge of wafer, artifact of the deposition system) and silicon oxide deposition area (entire wafer). No other defects except for visual have been observed.

5.8 Stress analysis

The stress in the device layer turned out to be a great defect in the MUMPS SOI chips. In my previous project, deposition of thick layers with too much stress has

resulted in partial and complete delaminations of layers and other defects. Stress in the Bragg stack was therefore of extreme interest in the design.

To measure the stress in deposited layers, I used the Flexus 2320 Stress Gage [59], a tool that uses a laser beam to determine the curvature of wafer before film is deposited, scans the curvature of the wafer after the film is on the wafer, and uses Stoney's formula [60] (with substrate dimensions and material parameters as input) to calculate the stress in the film.

For all the tests, curvature of silicon wafer was measured from three different angles (0 degrees, 60 degrees, and 120 degrees) before and after film deposition.

Several methods were used to deposit silicon oxide. As was discussed above, a CVD reactor with high temperatures would produce the best optical quality films.

After several trials with CVD deposition on clean silicon wafers, removing film from one side and measuring curvature, the data listed in Table 5.1 was obtained for measure of stress in silicon oxide film of 720 nm thickness.

Table 5.1 Stress in Materials

Temperature of deposition	Stress
680^0 C	450 MPa, compressive
600^0 C	430 MPa, compressive
560^0 C	410 MPa, compressive
510^0 C	378 MPa, compressive
450^0 C	320 MPa, compressive

Compared to the stress calculated in SOI wafer, these values of compressive stress were high and would result in large mechanical deformations. As alternative, silicon oxide was also deposited using the STS PECVD system. After several tests, it was determined that silicon oxide deposited in current conditions and of the desired thickness resulted in an average of 190 MPa of compressive stress. An experiment with low-temperature (125 degrees vs. standard 350 degrees) resulted in a stress of 160 MPa compressive, not significantly lower. Germanium layer has resulted in average of 100 MPa of tensile stress.

Depositing Bragg stacks of alternating germanium and silicon oxide layers would result in net stress of 90 MPa of compressive stress per pair. If there is one more germanium layer on top of the stack, it would result in almost zero net stress. Addition of one more layer would improve the optical performance by increasing the number of quarter-wavelength thick layers.

Experiments with different deposition parameters led me to deposit silicon nitride of either compressive, tensile or almost-zero stress.

The key to obtaining low-level nitride layers in PECVD is using mixed-frequency deposition. When nitride is deposited using a "low" plasma frequency, the films are compressive. When using "high" frequency, the films are tensile. Finding the right combination of alternating low and high frequency depositions can give films of almost any desirable stress.

The initial tests that I have performed were these: three depositions of 30 minutes each, and frequency mixes as follows: 3 seconds high, 3 seconds low; 6 seconds high,

3 seconds low; 3 seconds high, 6 seconds low. The results were as follows: thicknesses of each deposition were almost the same, with 276 nm, 255 nm, and 280 nm. The stresses were: 260 MPa compressive, 140 MPa compressive and 620 MPa compressive. Consecutive test was of high 5s, low 2s, and resulted in film of 334 nm thick, and stress of 43 MPa compressive. Test of 6s high/ 2s low resulted in thickness of 20 MPa compressive. Last test of 8s high/2s low resulted in thickness of 350 nm, and 10 MPa tensile stress. This data is shown in plot below, with the ratio between high/low plasma time plotted versus stress in MPa (compressive stress given positive value for convenience).

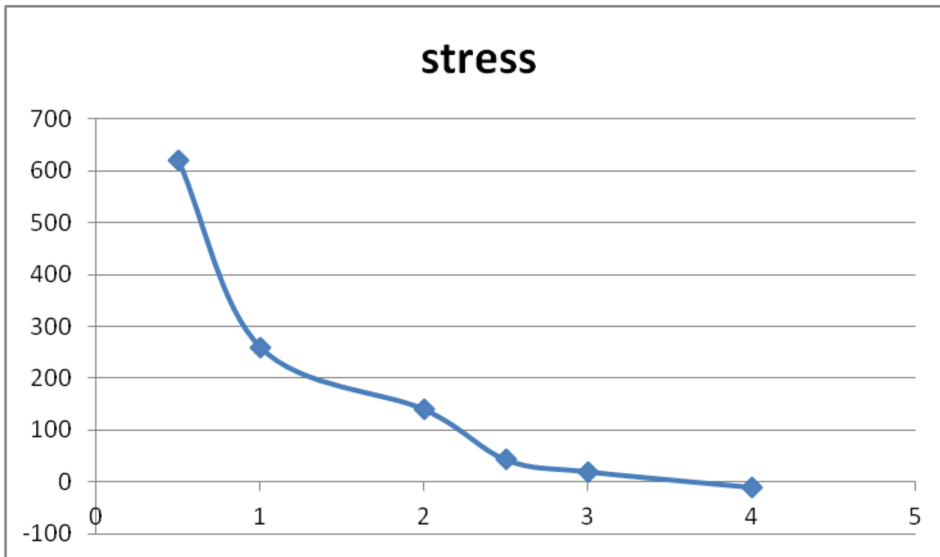


Figure 5.18: Stress in 500 nm silicon nitride layer with different deposition conditions. Ordinate is stress in MPa and the abscissa is the ratio between high and low frequency plasma deposition.

Therefore, stresses in silicon oxide and germanium somewhat compensate, and deposition of silicon nitride layer would allow me to compensate for almost any stress in the SOI wafer.

As a test of surface deformations resulting from the stress in Bragg stack materials, a triple Bragg stack was deposited on a 350 μm thick silicon wafer and optical windows were etched into the back of the wafer, the etch stopping on the silicon oxide layer of the Bragg stack. The windows measured 2 mm by 2 mm. A photograph of the resulting shape and the cross-section are shown in Fig. 5.19.

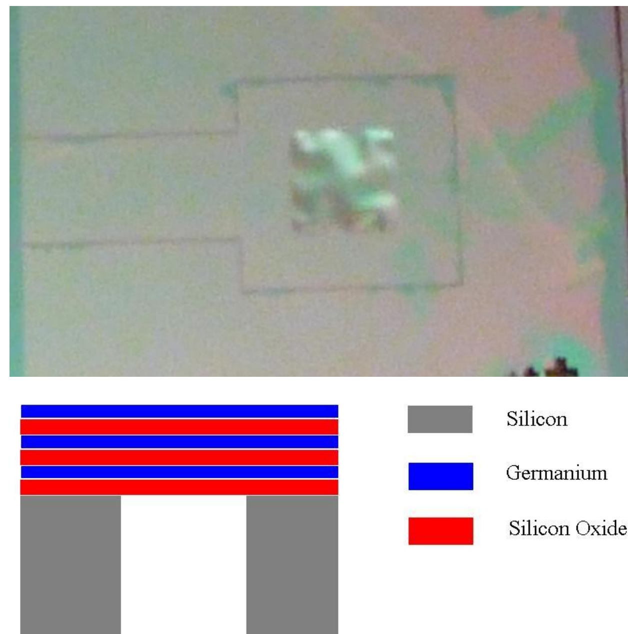


Figure 5.19 Triple Bragg stack without silicon support

The resulting shape was consistent across the wafer, and while the deformation could not be measured using white-light interferometry, the peak to bottom difference was determined to be more than 500 μm. This demonstrates that in order to produce a usable reflective surface, the Bragg reflectors have to be deposited on a silicon layer.

Table 5.2 summarizes the stresses measured in the deposited films as well as stress in the silicon device layer of the SOI wafer.

Table 5.2 Stress in layers used in first fabrication run

Material	Method of deposition	Thickness	Stress
Silicon Oxide	CVD	720 nm	600 MPa – 300 MPa compressive
Silicon Oxide	PECVD	720 nm	190 MPa compressive
Germanium	E-beam evaporation	250 nm	90 MPa tensile
Silicon Nitride	PECVD	500 nm	600 MPa compressive – 450 MPa tensile
Membrane silicon	SOI wafer	10 μm	200 MPa compressive

5.9 Bragg stack etching processes

One reflective mirror would require etching of the Bragg stack to mesa shape. Therefore, a process needed to be developed. In my previous project, I have extensively worked on dry etching, and this process has generated many challenges, such as micromasking and undercuts. That project required very deep trenches

without much undercutting, so wet etching, which is mostly isotropic, was not possible. After considering the feature size versus layer thicknesses for this device, I determined that it would not be detrimental to have small undercutting and therefore widening of features.

All of the etches that were developed were wet etches. Much experimental work has gone into the following results, which are summarized.

Silicon oxide layers were etched using 6:1 buffered oxide etch (BOE), with published etch rate of PECVD oxide of 490 nm/min [61]. Experimentally, it took 3 minutes to completely clear a layer.

Germanium was etched using hydrogen peroxide solution at 75 degrees. Published etch rates are 150 nm/min [61], but experimentally, it took 5 min to completely clear the layer, giving etch rate of 50 nm/min.

Silicon nitride was etched using hot (160 degrees) phosphoric acid, with 500 nm being etched in 30 min, giving etch rate of 17 nm/min.

All of the etches are extremely selective to consecutive layers, and don't produce significant undercutting. Picture below is a SEM image of etched feature.

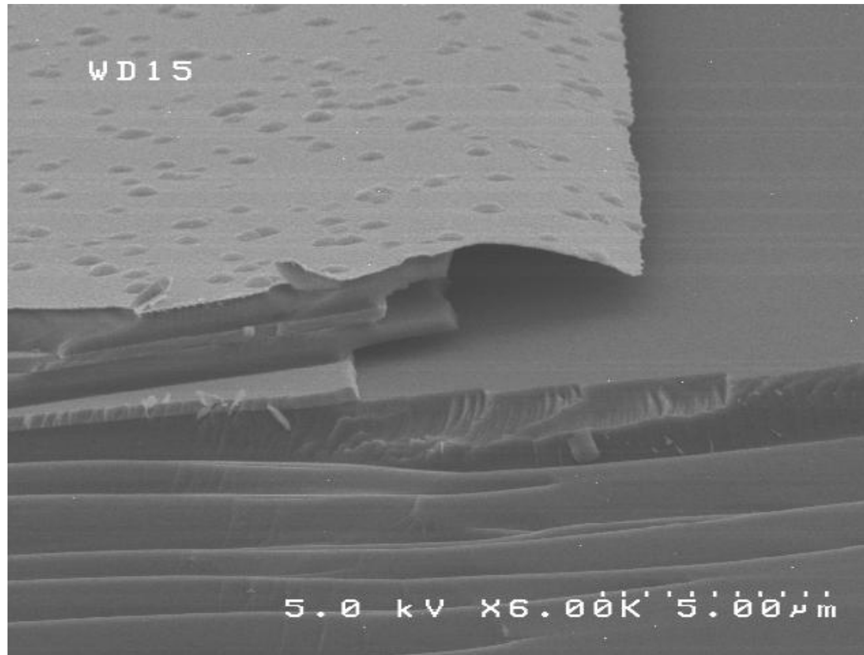


Figure 5.20: SEM image of Bragg stack etched using consequtive wet etch

As can be seen from the image above, the metal hard mask is severely undercut (3 μm). The first silicon oxide layer is undercut by 3 μm, and the first germanium layer is undercut by 5 μm. The second silicon oxide layer undercut by 3 μm, and the last germanium layer by 5 μm. Therefore, one can expect 10 μm widening of features as defined by top mask, which is easily compensated for in the design. If needed, for the future small-scale high-precision devices, these processes can be dialed in to minimize undercutting (minimum undercut should be 2 μm). Figure 5.21 is a top-down image of feature widened by the undercutting, next to the same feature before etching. (Note: scales are not the same)

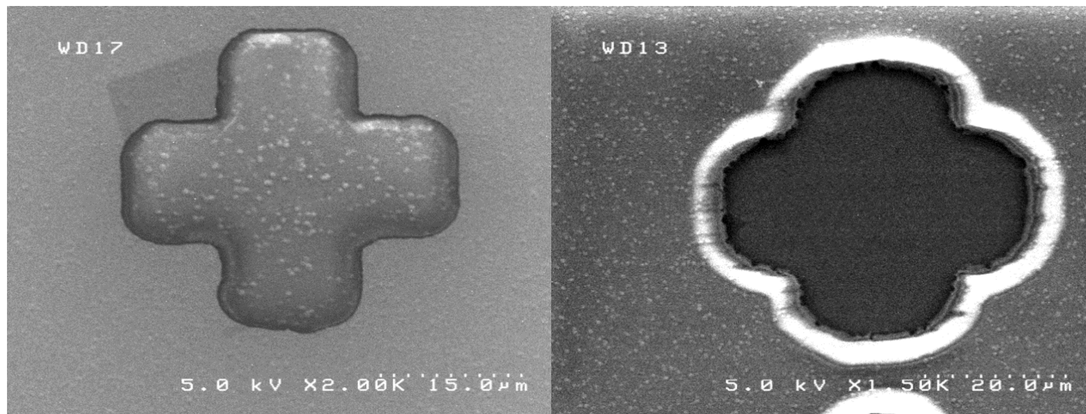


Figure 5.21: SEM image of alignment mark mask demonstrating widening of features

After removal of the hard metal mask, the protected surface did not show any signs of etching or defects, and a smooth underlying silicon wafer.

5.10 Silicon membrane etching

To produce the X-beam feature, we need to etch through the device layer of silicon using the top layers of gold, chromium, germanium and silicon oxide as hard masks. The final shape would be the same as etched in Bragg stack.

Etching using anisotropic wet etchants like KOH and TMAH is impossible here, as these etches are very selective to crystalline orientation and would not allow complex mask geometries.

The etchant that was recommended to me was HNA etch, which stands for HF (Hydrofluoric Acid), Nitric acid, and Acetic acid. The mechanism of the etch is [62]: nitric acid oxidizing silicon, HF removing oxide, and acetic acid acting as buffer. This etch is used for silicide stripping and surface polishing. While this is an

extremely fast etchant (etch rates of bulk silicon can be as high as 500 microns/minute), a mix of 20% HF (49% concentration), 40% nitric acid, and 40% acetic acid has reasonable etch rates of approx. 1 micron/minute. To verify this, I have run several tests on silicon wafer with chromium/gold as hard mask, patterned with one of my old masks. Figs. 5.22-5.26 below are of trenches etched after 5 minutes and 10 minutes, respectively. Bulk silicon wafer with chromium/gold hard mask was used for all the experiments.

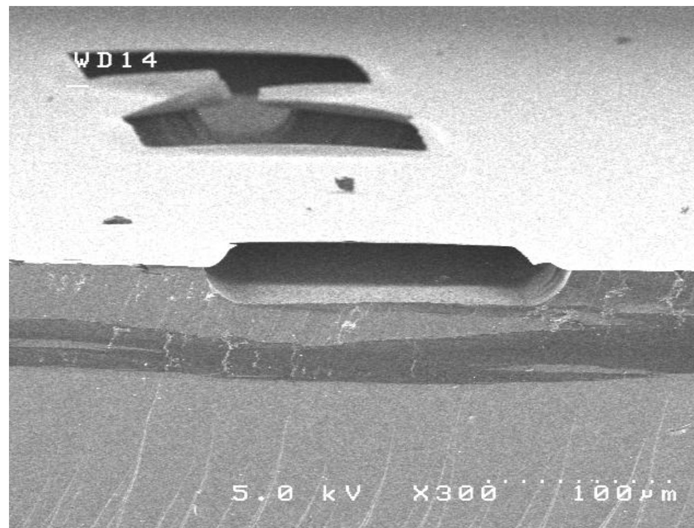


Figure 5.22: SEM image of silicon etch after 5 minutes using HNA, showing severity of undercut in narrow bridge device

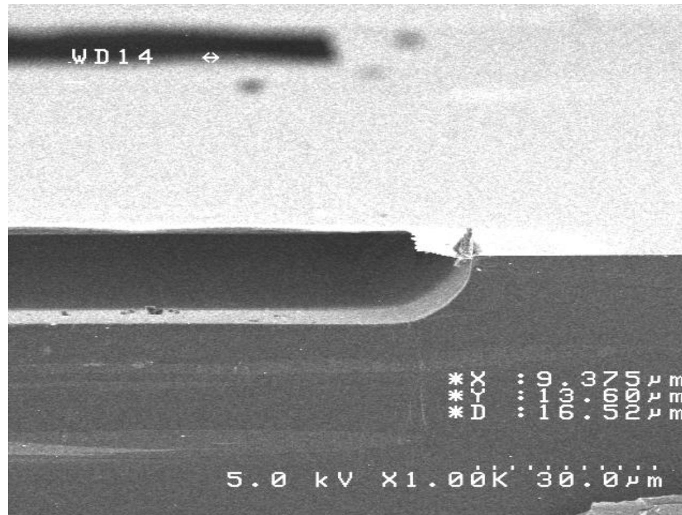


Figure 5.23: SEM image of silicon etch after 5 minutes using HNA, with details of the hard mask

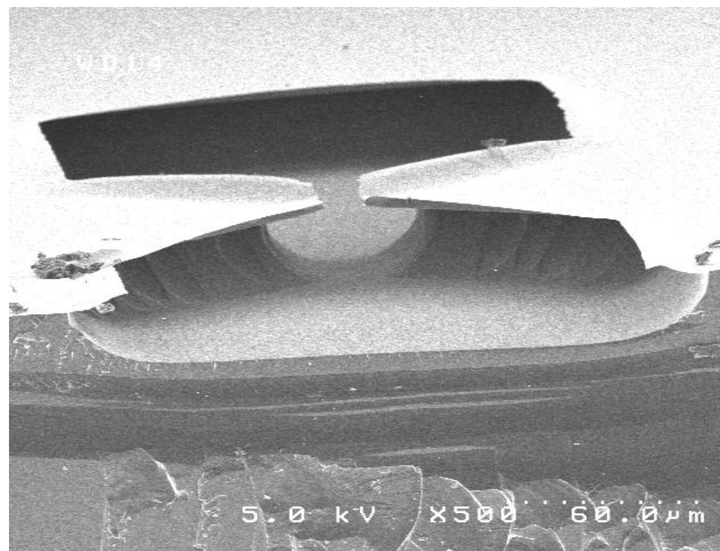


Figure 5.24: SEM image of silicon etch after 10 minutes using HNA, showing effect of undercut on narrow feature

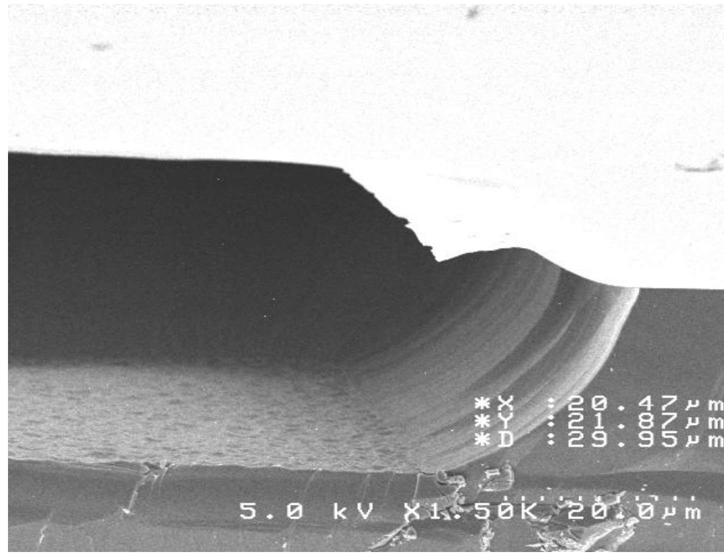


Figure 5.25: SEM image of silicon etch after 10 minutes using HNA, with high magnification showing detail of the hard mask

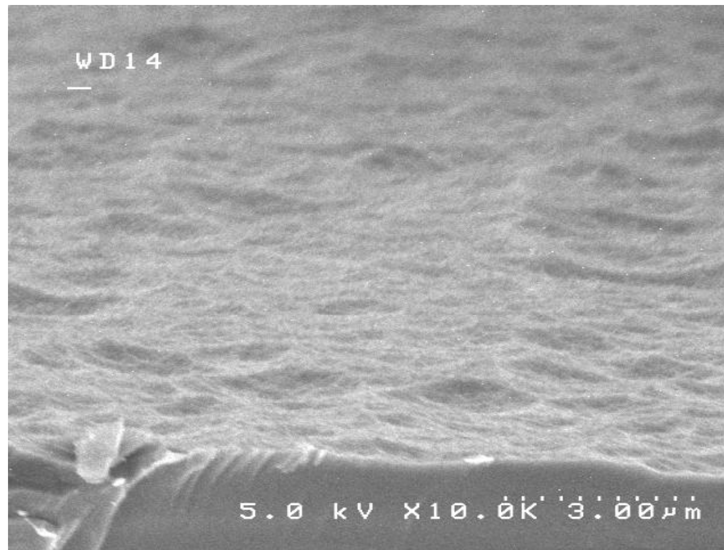


Figure 5.26: SEM image of silicon surface after HNA etch, resulting in high roughness of resulting surface

As can be seen from pictures above, freshly-mixed HNA solution has an etch rate in bulk silicon of 2.72 μm/min, and after 2 hours, drops down to 2.19 μm/min.

5.11 Combined etching

After developing a good sequence of etching steps for Bragg stack and bulk silicon, I have performed a combined test, where Bragg stack etch(3 min BOE, 5 min hydrogen peroxide, 3 min BOE, 5 min hydrogen peroxide) is followed by HNA etch (1 min)). The results are shown in Fig. 5.27 and Fig. 5.28:

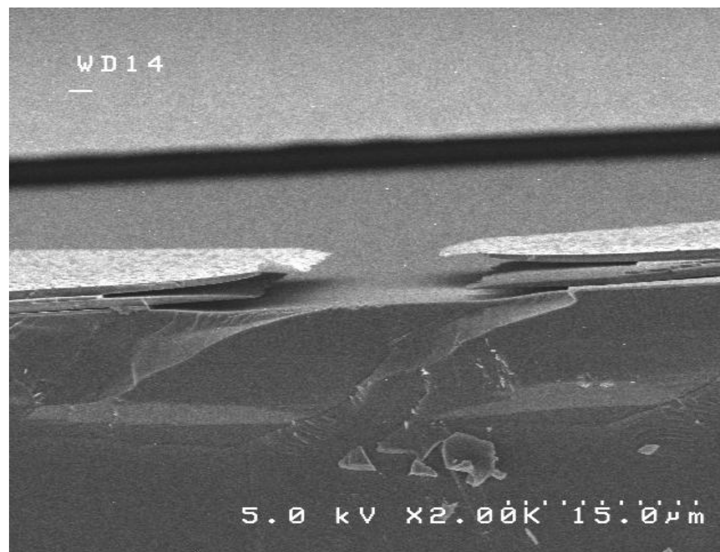


Figure 5.27: SEM image of result of combined Bragg stack and silicon etching

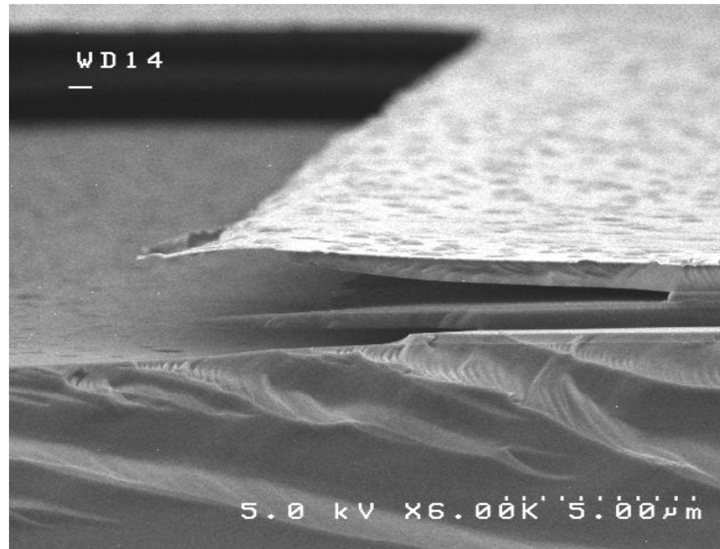


Figure 5.28: SEM image of result of combined Bragg stack and silicon etching, with magnified section showing undercut in different layers

This test demonstrated success of successive etching, but the most interesting result was that HNA etched all the layers of the Bragg stack (silicon oxide is naturally etched by HF, and nitride has the same effect on germanium as on silicon – rapid oxidation).

This gave me an idea that all the etching sequence can be combined into one single HNA step. A wafer with double Bragg stack and patterned gold/chromium mask was submerged into HNA for 4 minutes, with resulting SEM in Fig. 5.29:

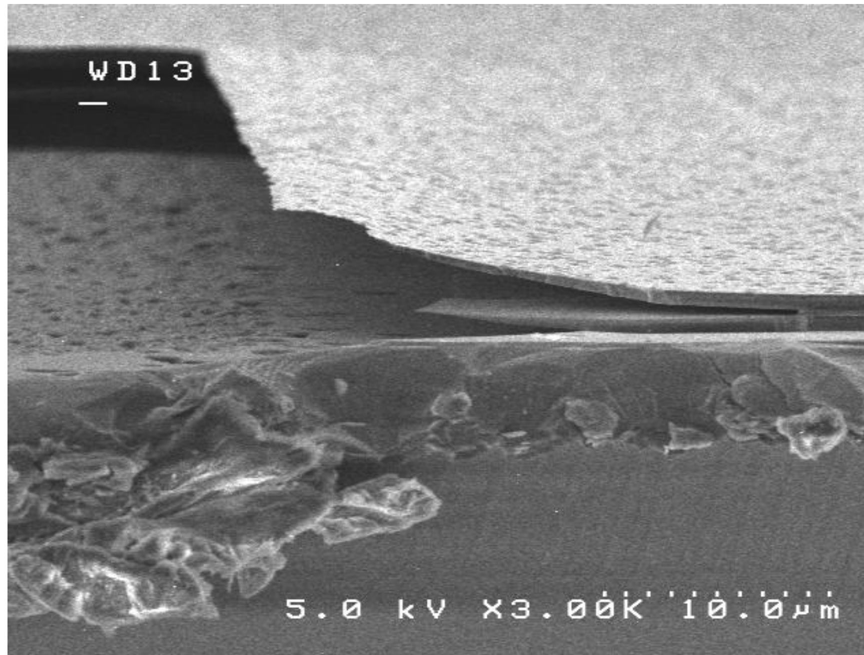


Figure 5.29: SEM image of result of combined Bragg stack and silicon etching

This demonstrates that if undercutting is of not great concern, all the steps for X-beam release can be combined into one 5 minute HNA etch.

5.12 Backside etching

Etching of windows, although not as useful unless done on SOI wafers, was performed to familiarize myself with the process and make at least some preliminary decisions.

The most common etchant for such through-wafer etching is KOH at 80 degrees, which etches anisotropically, with sidewalls of 54.7 degrees [63]. Masking material for the etch is usually thick nitride/oxide sandwich, with nitride being main

protection, and oxide compensating for pinholes. After etching, these materials are removed.

Using thick dielectric hard masks was not favorable for the process. The main reason is the added complexity, as these layers have to be deposited, etched and removed at the end of the KOH process. As the Bragg stack is composed of same materials, removal of these stacks has high chance of damaging optical surfaces.

I have performed a series of tests on standard one-side polished test wafers, using metal masks, gold, chromium and combination of the two. The results have been disastrous, as any concentration of KOH very quickly underetched the mask layers, and lifted them off after at most one hour of etch (through-wafer etch is at least a seven-hour process). Adding a nitride layer had the same effect.

Heating 20% KOH to 90 degrees resulted in 2 hour through-wafer etch, but was so rough that it thinned the wafer to tens of microns and ripped through all the masks on the protected side.

Second option was using TMAH, another anisotropic etchant of silicon [64]. It is used at higher temperature of 95 degrees, and is more selective than KOH. Initial trials have shown much better results than KOH. The etch is much more finicky, as it works best in 95 to 100 degree window, and is so selective to silicon oxide that it requires HF dip of the wafer to be done several seconds before process, to remove any miniscule native oxide.

As I was using only one-side polished wafers, roughness on the unpolished side (rms of 33nm) always guaranteed lifting of the mask and etching of the rough side.

Continued trials of KOH/TMAH etching were performed using several combinations of masks.

As stated above, the initial masking material was a chromium/gold sandwich, 20 nm Cr and 50 nm Au. This mask was ineffective and was peeled off in the first hour of etching in either KOH or TMAH.

Second attempt has been to use 100 nm of silicon oxide coated with Cr/Au mask. KOH has lifted the mask within first hour of etching, and TMAH within three hours. Replacing silicon oxide with 100 nm of silicon nitride had the same effect.

The protective layer combination that finally worked was: silicon nitride (300 nm) followed by 300 nm of silicon oxide, and 20 nm Cr/ 50 nm Au final layer. This mask protected both the backside and frontside of the wafer. Such a combination introduced several extra steps into the process, as both silicon oxide and silicon nitride had to be patterned on the side where windows are desired. Especially dangerous was the silicon nitride etch, which uses 85% phosphoric acid heated to 160 degrees.

Also, the edges of the wafer came out extremely ragged, with wafer diameter reduced by 2 mm. Flakes of metal mask were floating in the container afterwards, and complicated the clean-up. Another way has to be found for processing at a commercial foundry. Figs. 5.30-5.31 demonstrate alignment marks after TMAH etching, with characteristic undercuts.

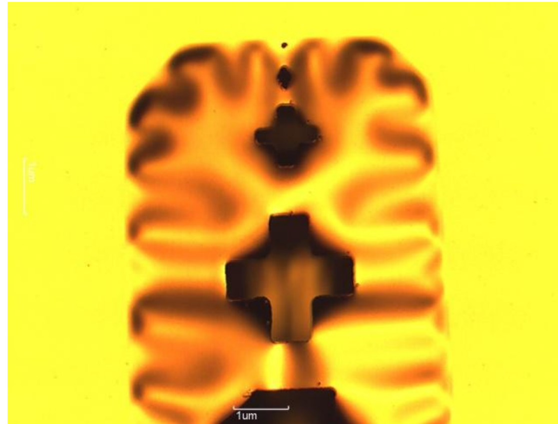


Figure 5.30: Gold mask over etched silicon, showing the degree of undercutting the hard mask

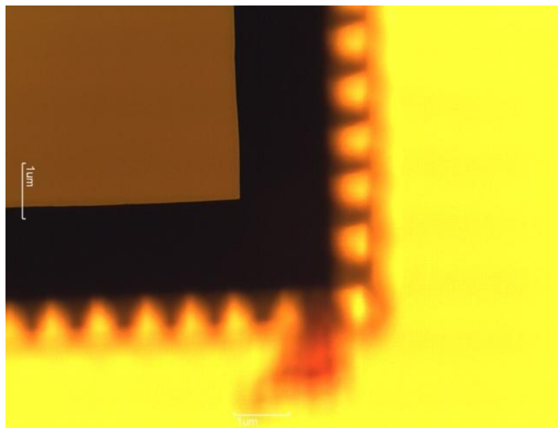


Figure 5.31: Gold mask over etched silicon, showing rough mask edges resulting from undercutting and smooth edge of window underneath

5.13 Bonding development

Although bonding in future devices will be done with either metal bumps or with fusion bonding, for the initial devices we developed bonding with photoresist. Although SU-8 polymer would be better suited for its permanence, processing of SU-8 requires special processing labware and de-contamination steps. So, standard

photoresist used for thick coatings was used, SRP-220. This photoresist has a well-developed process for thicknesses from 3 μm to 10 μm.

Development of the bonding process required some trials with spinning speeds and thicknesses, as well as baking times, temperatures, exposure and development times. After spinning on a wafer previously treated with PDMA, and baking for 60 s at 90 degrees, the wafer was exposed for 10 s and developed for 1 min, following 2-min bake at 90 degrees. Placing another (clean) wafer on top and baking at 120 degrees for 20 min, with 2 kg weight on top, resulted in a mechanically strong bond. The wafers could not be pried apart with tweezers, and withstood 1 min of soak in warm acetone. Only following 10 minutes of sonication in warm acetone bath did the wafers separate.

5.14 Substrates selection

After the development of the processing steps above, parameters for SOI wafers were determined. The requirements are as follows: device layer of 10 μm thickness, <100> orientation, low doping; buried oxide layer of 2-3 μm; handle wafer of <100> orientation, with backside polished. Several vendors were contacted for a quote, and Ultrasil Corp. of Hayward, CA was identified as the best vendor. Five wafers were purchased from their stock with the above specifications.

5.15 Final Processing

As stated above, five SOI wafers were purchased. These were designated as WE15-WE19. Time constraints were placed by the funding for this first fabrication run. After running short-loop tests to determine separate steps, time to produce devices for testing was very limited, especially with Bragg stack deposition taking up most of the remaining time. Fig. 5.32- 5.37 below represent step-by-step cross-sections of each significant step in the process. Photolithography steps are not shown, and layer thicknesses are not to scale.

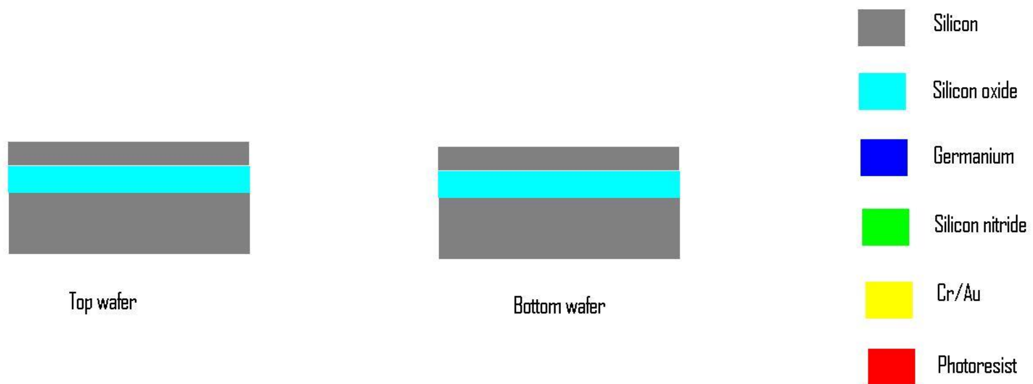


Figure 5.32: Fabrication flow: step 1: substrate

Following standard clean (RCA) processes on all the wafers, WE16, 17,18, 19 were coated with Bragg stacks, WE16 and WE17 with double, WE18 and WE19 with triple. WE15 was left as test wafer, for optical testing of single silicon layer.

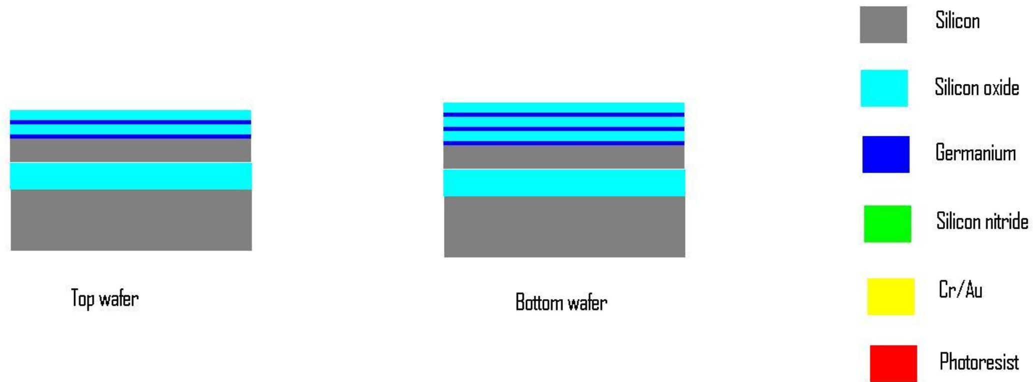


Figure 5.33: Fabrication flow: step 2: Bragg stack deposition

Protective coatings were deposited on all the wafers, with the following thicknesses: first, 320 nm of silicon nitride on front and back; 400 nm of silicon oxide on front, and 200 nm on back.

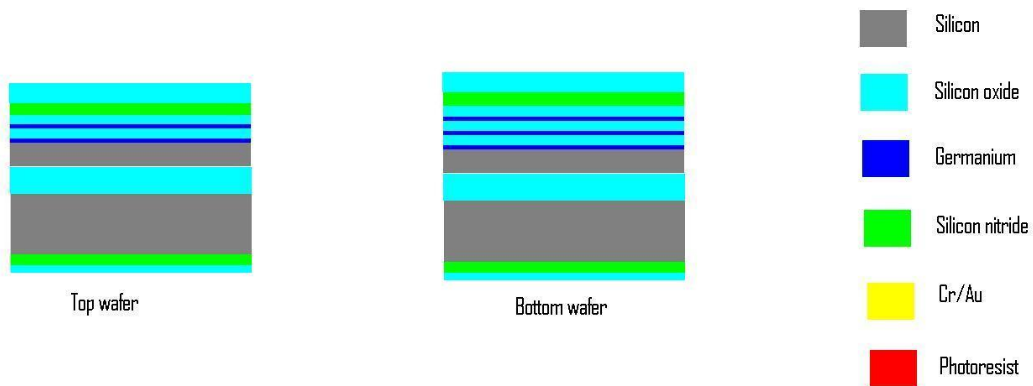


Figure 5.34: Fabrication flow: step 3: silicon nitride deposition

In order to ensure even further protection, silicon oxide on the back side, which previously been etched using Cr/Au as hard mask, was etched on the backside using the “Backside etch” mask. This reduced the front layer of silicon oxide to 200

microns. 25 nm chromium / 100 nm gold were deposited on both sides, and backside was etched with the "Backside etch" mask, aligned to previous oxide etch.

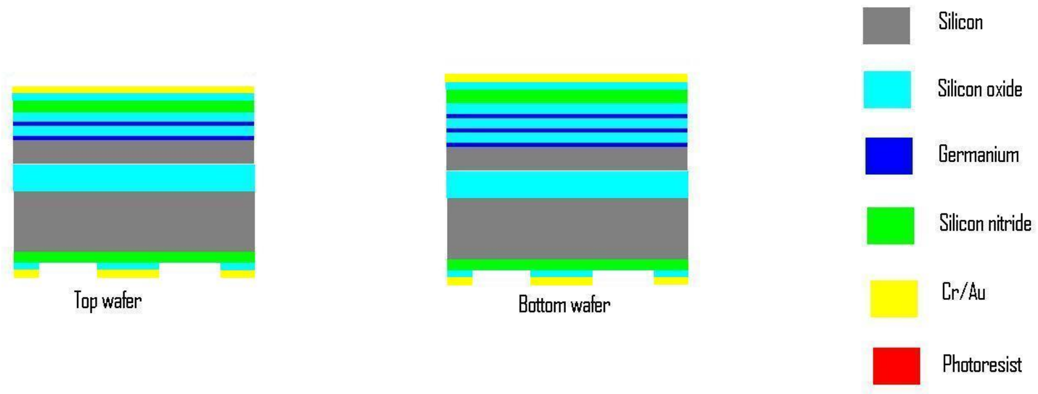


Figure 5.35: Fabrication flow: step 4: backside etch mask patterning

Following openings in the metal mask, wafers were dipped in 6:1 BOE for 30 s to remove any oxide in exposed areas, and silicon nitride was etched in hot phosphoric acid.

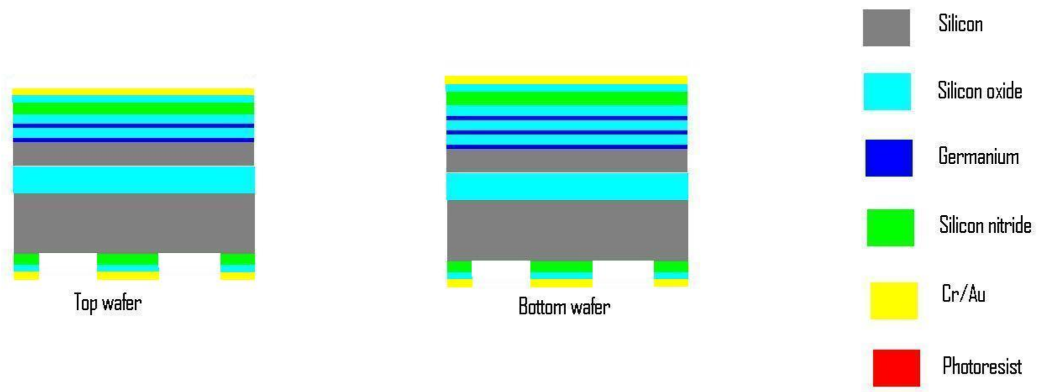


Figure 5.36: Fabrication flow: step 5: backside etch mask removal

Previous TMAH etch rates were deemed too low (0.5 μm/min) due to time limitations, and after the consulting literature [64], TMAH etch was performed at 96

degrees in 8% solution (lower concentration of TMAH increases etch rates, but is more aggressive toward the masks, so 8% was the compromise). The etch took 10 hours in a constant-temperature bath, and resulted in etching of windows on the backside, exposing the buried oxide layer.

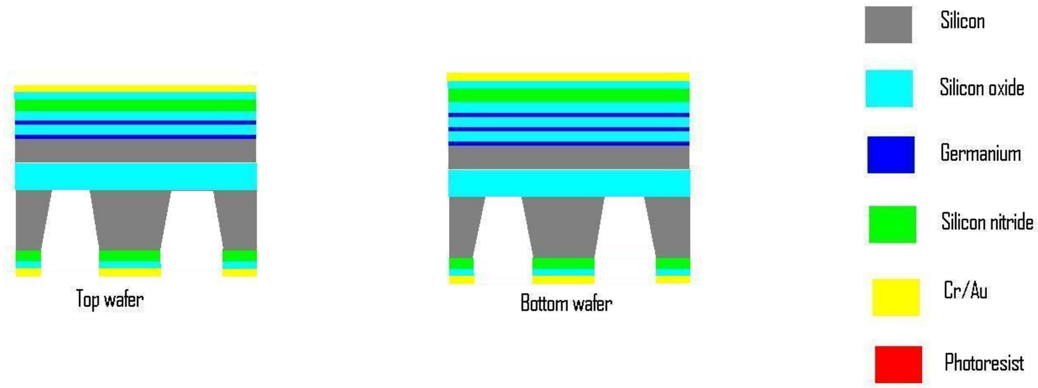


Figure 5.37: Fabrication flow: step 6: backside etch

As expected, the wafers were extremely rough on the edges, and had square holes in places of scratches and small pinholes. Front side of wafers did not get etched. After removing WE15 from the bath, and cleaning it with water and blow-drying, several of the membranes popped. This showed that the wafers were extremely fragile, and might not survive the following processing. Extreme care was used in removing and cleaning the remaining wafers. Upon visual inspection, on all the wafers, there were “hills” visible on front side where backside etching was done. This warping of the membranes happened due to high stress of layers deposited on one side.

As wafers WE17 and WE19 are to be used as bottom parts, they required no further processing apart from removing protective layers.

Wafers WE16 and WE18 were to have front sides patterned with an X-beam mask, and etched. These two wafers, along with WE15, were treated with PDMA, and 1.6 μm of SPR-3612 photoresist spun on them. During exposure, several membranes popped in the aligner, when placed in contact with the mask.

Apart from membranes popping, another problem was discovered: alignment of the frontside mask to the features etched in the backside. Usually, an IR camera is used for this purpose, but it could not penetrate all the protective layers. This resulted in severe misalignment of the frontside to the backside features.

After exposure and development, the X-beam patterns were etched in the metal layer on front side.

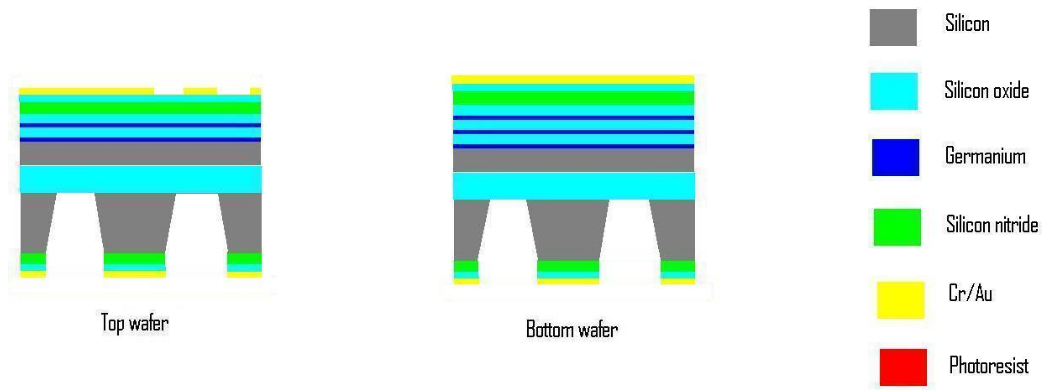


Figure 5.38: Fabrication flow: step 7: X-beam mask patterning

Dicing of wafers into chips was the next step. Due to the destructive nature of wafer dicing, all the protective layers were left on the wafers. This presented another problem, as it was difficult to see chip alignment marks, resulting in imperfect dicing.

Dicing was performed on blue sticky tape, as vacuum suction would not work due to large openings in the backsides of wafers. The removal of the sticky tape from such delicate structures required a piranha etch for 30 minutes and it resulted in popping of almost 80% of the membranes on WE17.

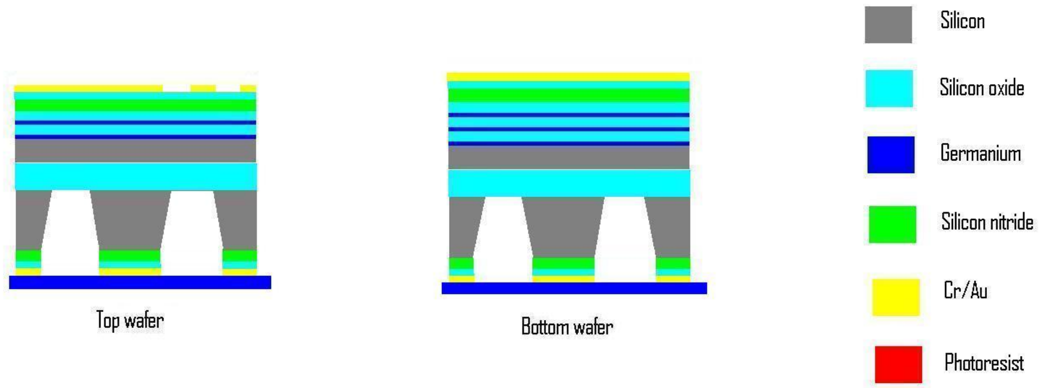


Figure 5.39: Fabrication flow: step 8: attachment to handle wafer

After blue tape and all adhesive residues were removed, the chips from wafers WE17 and WE19 underwent removal of all protective layers.

WE16 and WE18 had the X-beam patterns etched into them using 6 minutes in HNA.

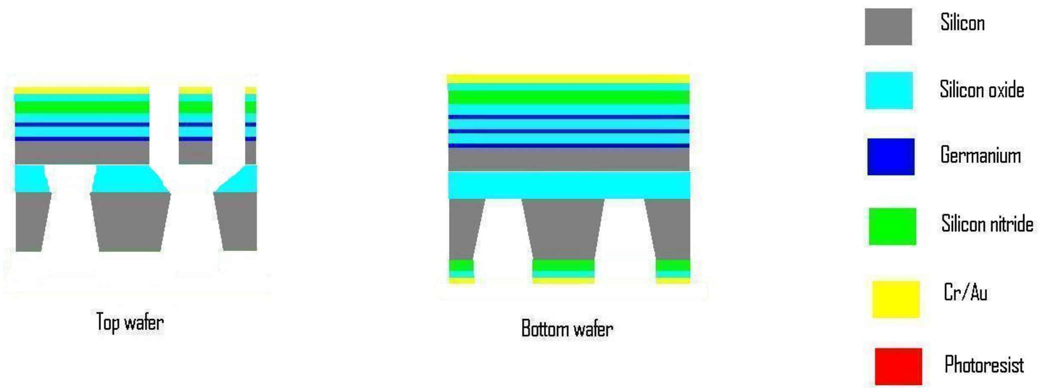


Figure 5.40: Fabrication flow: step 9: X-beam etch and release

From visual inspection, all the X-beam structures were released, but were misaligned to backside windows.

The protective layers were removed from the WE16 and WE18 chips. After removing the protective layers, the “hills” above backside windows were reduced in size.

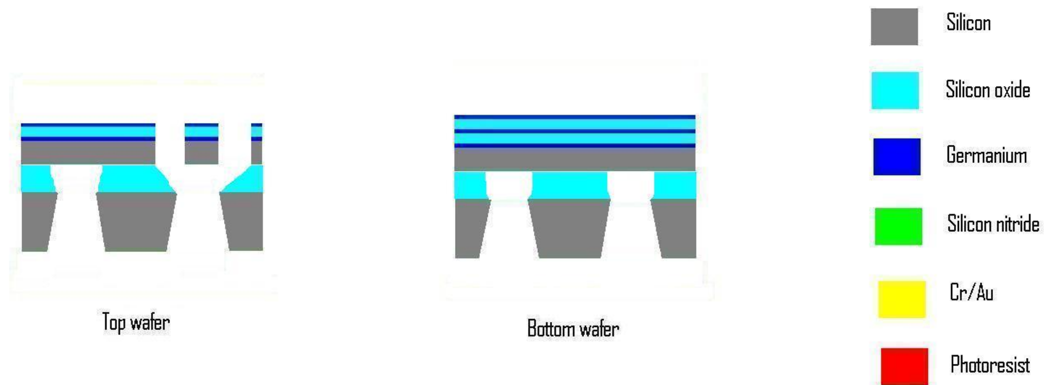


Figure 5.41: Fabrication flow: step 10: protective layer removal

At this point, time in the SNF lab almost ran out, and we needed to have at least some testable devices, so 7 μm of photoresist was spun on several chips from WE19 and WE17, and these chips were bonded to the best-looking chips from WE16, WE18 and WE15.

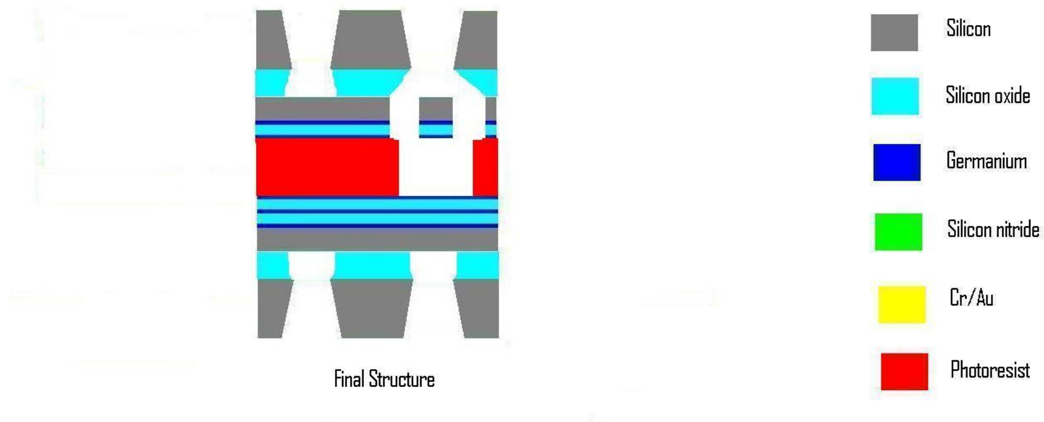


Figure 5.42: Fabrication flow: step 11: bonding

5.16 Resulting chips

Below are the summary results for each wafer:

WE15 – used primarily as a test wafer, left with just a device layer and X-beam released. Yield rate: out of 20 chips, 6 chips have membranes in both windows intact, and X-beam released. Out of the remaining chips: 8 chips have one window intact, can be used for testing. 6 chips have both windows destroyed and are unusable.

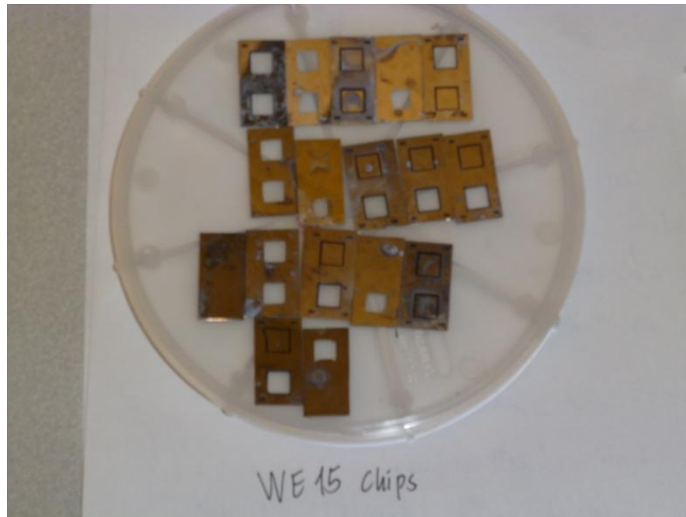


Figure 5.43: Photograph of WE 15 chips. See-though membranes were destroyed during processing.

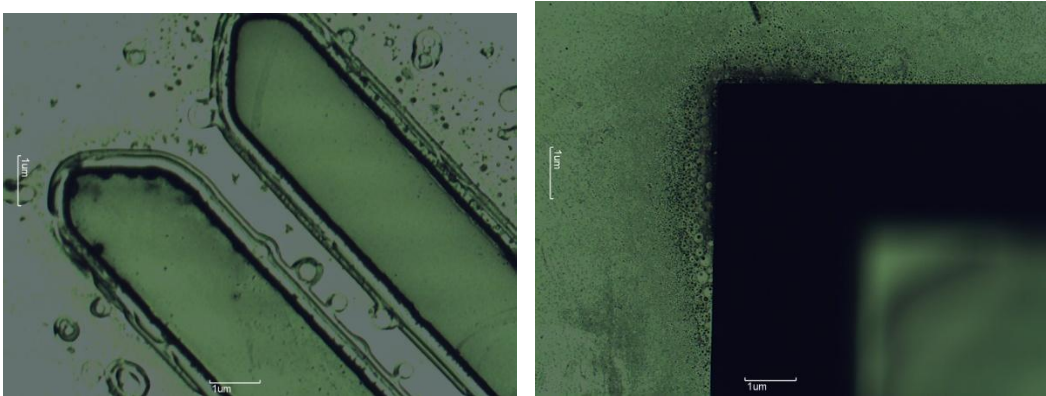


Figure 5.44: Details of WE 15 chips, showing etching of the X-beam springs and corner of backside window.

WE16 – had a double Bragg stack deposited had X-beam etched and released. Yield rate: 7 chips in good condition (both windows intact, and X-beam released). All the chips had misalignment of the X-beam in relation to backside etch. 8 of the chips had one window intact. 7 chips were destroyed during this process.

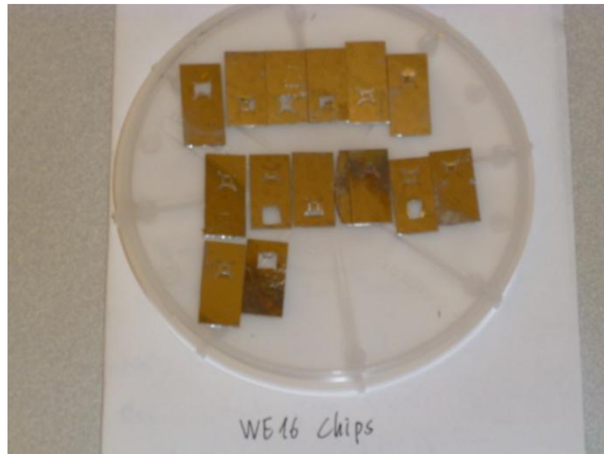


Figure 5.45: Photograph of WE16 chips. Good chips are chips 1, 2, 3, 5 (from right) in row 1, 1 and 6 in row 2, and 2 in row 3.

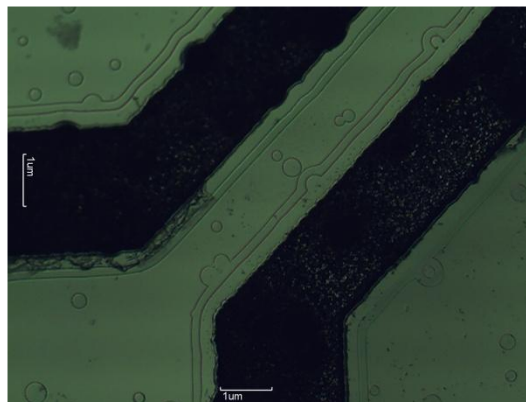


Figure 5.46: Detail of WE16 chips, showing uneven etch of the spring

WE17 – had double Bragg stacks, no X-beam. The lowest yield wafer (membranes popped during dicing/blue tape removal). Seven chips with both windows intact, two chips with one window intact. 11 chips were destroyed.

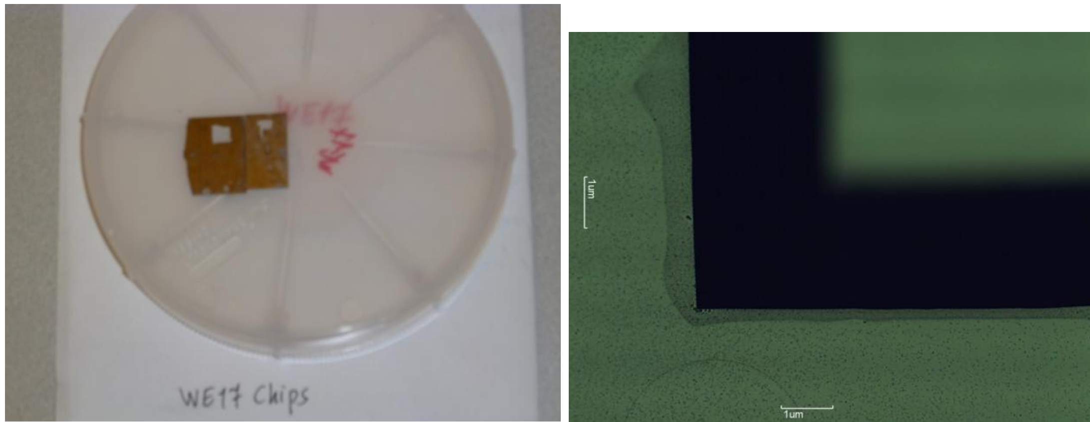


Figure 5.47: Photograph of WE17 chips with detail of backside window

WE18 – has triple Bragg stack, X-beam etched. This batch has 12 chips with intact windows and etched and released X-beams. Due to the triple thickness of the Bragg stack, the top and bottom mask were misaligned. X-beam etching was non-uniform across the wafer. 3 chips had only one window intact. 5 chips were destroyed.

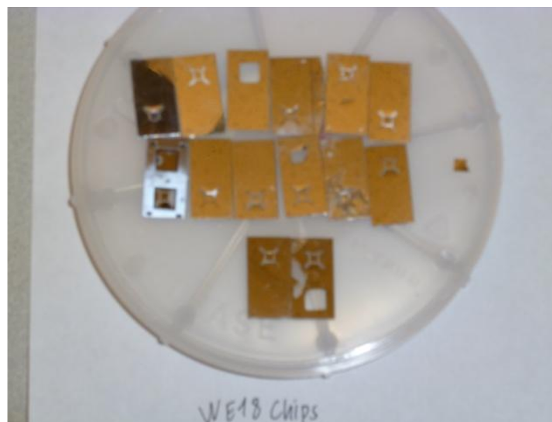


Figure 5.48: Photograph of WE18 chips, showing defect chips (chip 4 in row 1, chip 3 in row 2, and chip 1 in row 3)

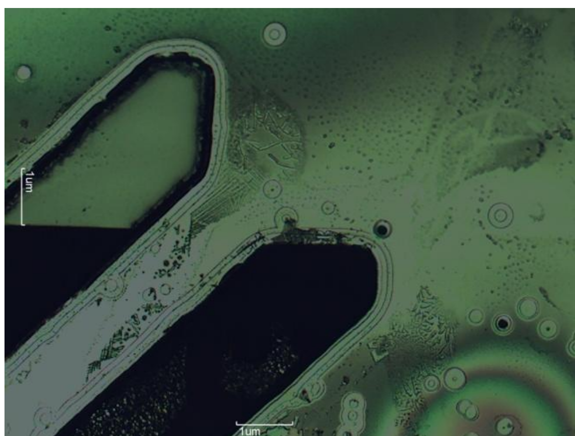


Figure 5.49:WE18 chip details show misalignment of X-beam to backside etching

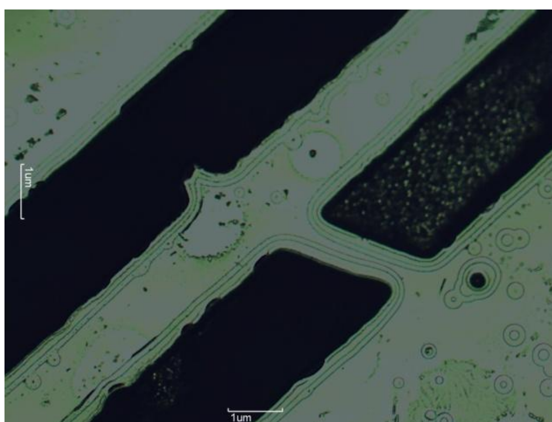


Figure 5.50: WE18 chip details show incomplete etch of the spring

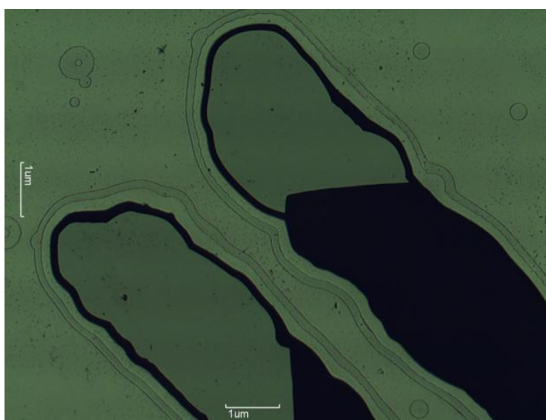


Figure 5.51: WE18 chip details show uneven etch of the spring

WE19 – triple Bragg stack, no X-beam. This batch of chips has 13 chips with both windows intact and 4 chips with only one window intact. 3 chips were destroyed.

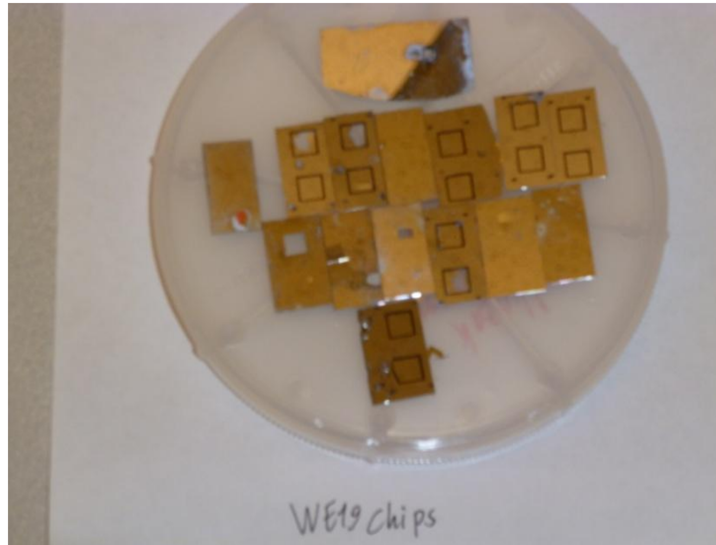


Figure 5.52: Photograph of WE19 chips. Chips 1-4 and 7 in row 1, chip 2 in row 2, and chip in row 3 have both membranes intact.

5.17 Bonded chips

From the chips obtained in this round of fabrication, several pairs of chips have been bonded for testing. There were five combinations, with two of each, as follows: WE19-WE15, WE19-WE16, WE19-WE18, WE17-WE16, WE17-WE18. This gives a good range of devices for optical testing of the Bragg stacks and optical effect of the silicon device layer.

5.18 Surface analysis

As stated previously, we obtained several bonded chips, with varied Bragg stacks combinations. Before performing mechanical testing, we checked their electrical conductivity, and found that all the chips were shorting to each other, making it impossible to perform mechanical testing.

To explain this, we performed white-light interferometry on all the chips, to determine their profiles. If you recall, chips from WE15, WE16 and WE18 had an X-beam and a membrane, and chips from WE17 and WE19 had two membranes.

WE15 chips: no Bragg stacks

In these chips, the X-beam is bowed by 0.76 µm, and the membranes are bowed by 0.44 µm, at the peak. Images are below:

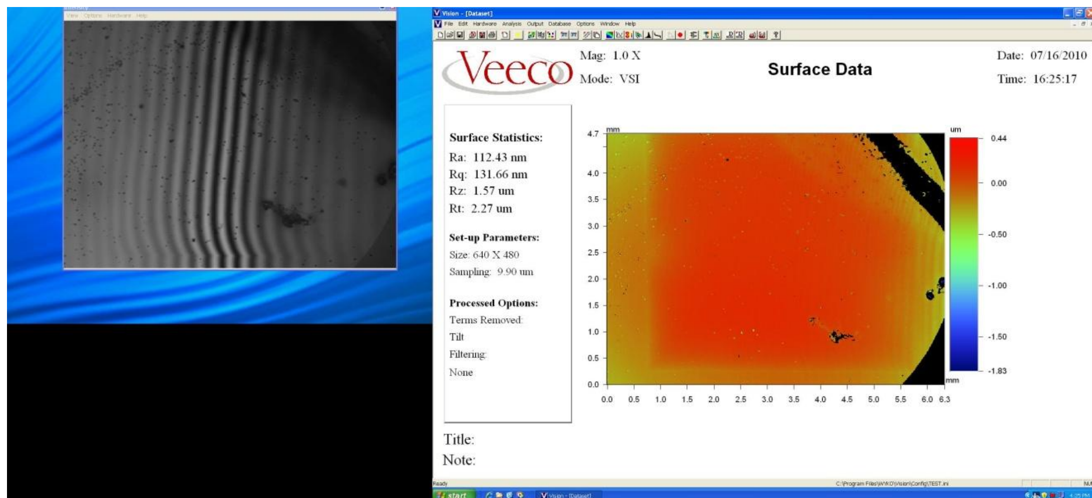


Figure 5.53: Surface of WE15 chip membrane

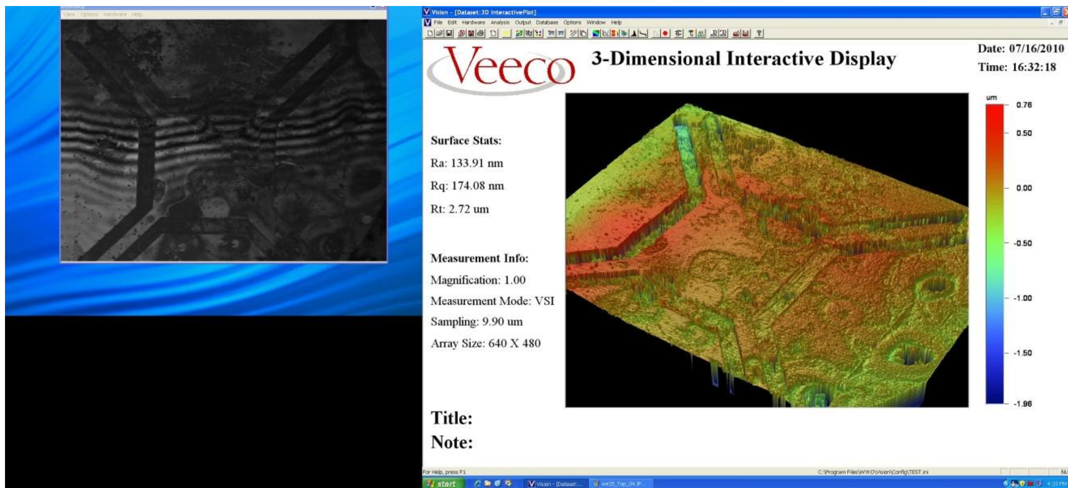


Figure 5.54: Surface of WE15 chip X-beam

The intact membranes of WE15 chips can be used for optical testing to measure transmission through silicon layers. As can be seen from the images above, small pinholes would allow some light through, introducing some error into the data. The X-beam parts do not look to be released, and the resulting non-uniformity of the thickness makes them unusable for optical testing.

5.18.1 WE16&WE17: double Bragg stacks

In these chips, the X-beam has a bow (spherical defect) of 14.2 µm, and the membranes were bowed by 2.38 µm. Multiple pinholes and deformations seen in both membrane and X-beam chips make them unusable for optical testing. Images are below:

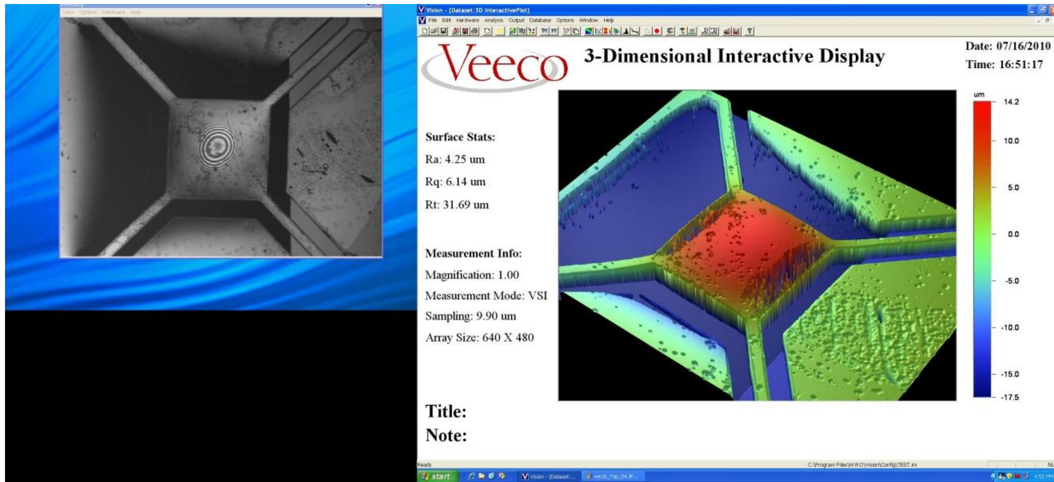


Figure 5.55: Surface scan of WE17 X-beam

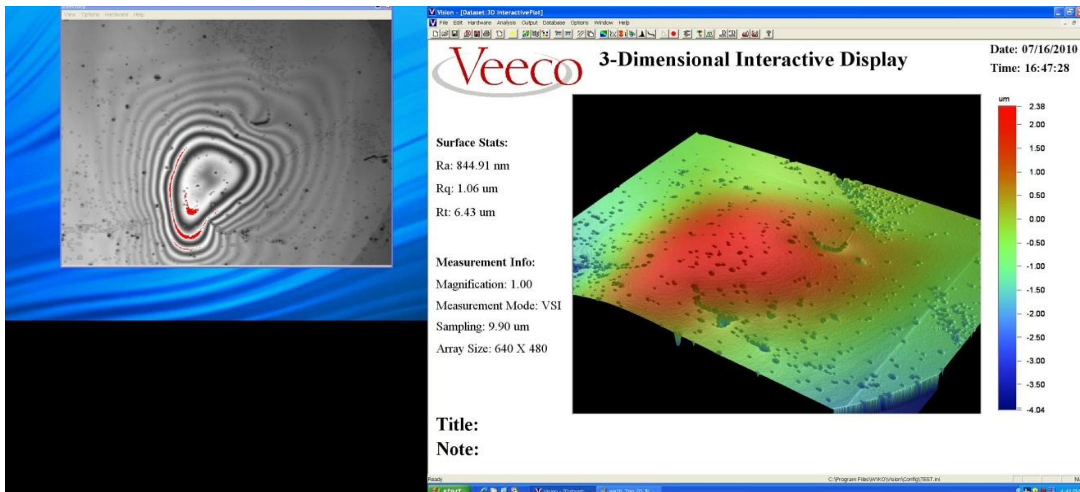


Figure 5.56: Surface scan of WE17 membrane

5.18.2 WE18&WE19: triple Bragg stacks

In these chips, the X-beam was bowed by 15.3 μm, and the membranes were bowed by 2.17 μm. Again, the large areas affected by pinholes and uneven surfaces make

them unacceptable for optical testing and even less so as working devices. Images are below:

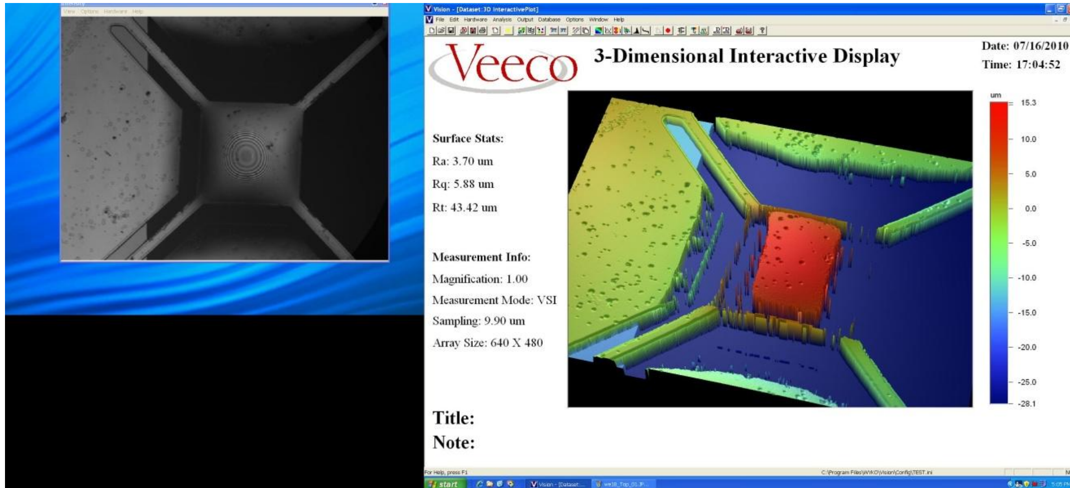


Figure 5.57: Surface scan of WE18 X-beam

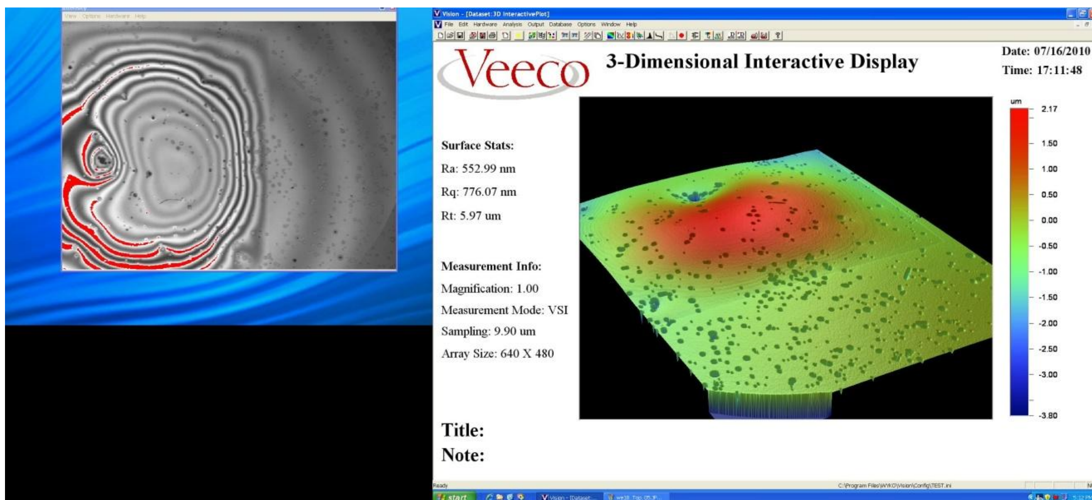


Figure 5.58: Surface scan of WE18 membrane

5.19 Optical Testing

The tool used to analyze the experimental results is the ThermoScientific Nicolet 6700, with custom HgCdTe detector instead of the factory-supplied one.

The tool has two modes, reflection mode and transmission mode. The basic schematics of these two modes are shown in Fig.5.59.

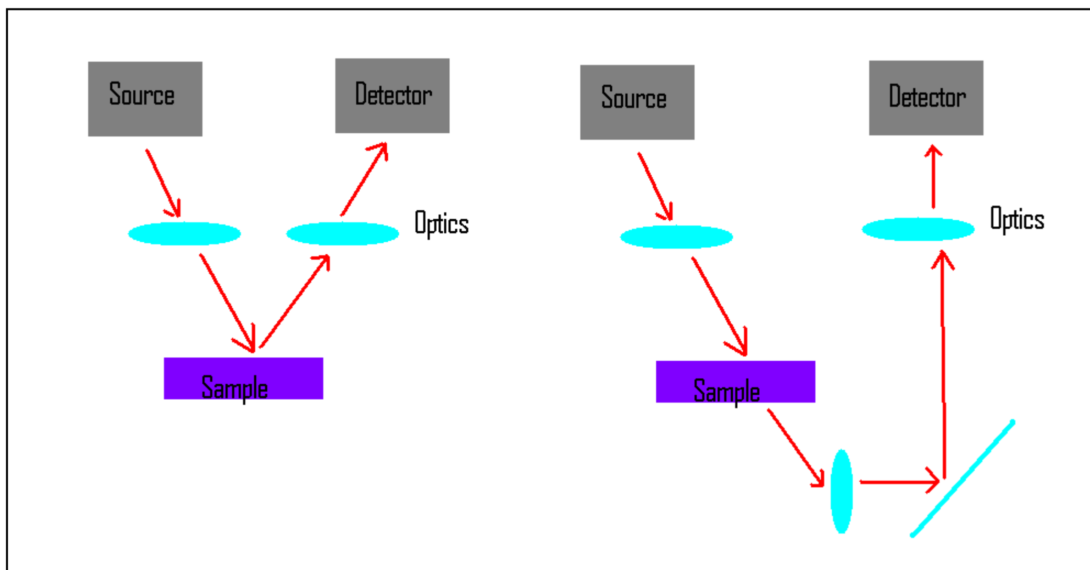


Figure 5.59: Basic schematic of optical testing setup, reflection and transmission

In the reflection mode, the source sends out a signal, $I_s(Y)$, which undergoes transmission through optics and atmosphere, is incident upon the sample, and signal $I_r(Y)$ is reflected back, though more optics and atmosphere, and the signal is received by the detector, $I_d(Y)$. In the transmission mode, the transmitted signal $I_t(Y)$ is again routed to detector after being transmitted though the sample.

The data output of the instrument is the ratio, T(Y) or R(Y), depending on the mode of operation, of the source signal to the detected signal, $I_d(Y)/I_s(Y)$. This gives the reflectance or transmittance of the sample.

Neither the source nor detector are perfectly linear devices, and $I_s(Y)$ and $I_d(Y)$ are wavelength-dependent. Also, both optics of the instrument and the atmosphere have their own wavelength-dependent absorbance functions. Therefore, looking at the pure data, as given by the instrument, is almost useless. It would be extremely complicated and unnecessary to analyze and collect data to separate each component of the total absorbance function. Contributions of all of these elements multiply, and therefore can be combined as a single term, $A_s(Y)$ (total system absorbance, including source, optics, atmosphere, and detector).

To correct for the above-mentioned wavelength-dependent aberrations, it is helpful to get a sample signal. For the reflectance mode, that would be a reflector that is as close to perfect as possible – in this case, we used a gold mirror. In the transmittance mode, simply recording the signal without any sample gives a base-line combination of the system aberrations.

5.20 Bragg reflectors optical testing results and comparison to simulations

Optical reflectivity testing has been done using a Fourier-transform infrared spectrometer in the MWIR-LWIR on the single, double and triple Bragg stacks that were fabricated at SNF. Initial reflectivity was taken from gold-coated wafer, and this was used as reference for the reflectivity of all the samples. After conversion

from wavenumber to wavelength and cropping the data to the 2.5µm-7 µm range (design range of the Bragg stacks), the following graph was obtained:

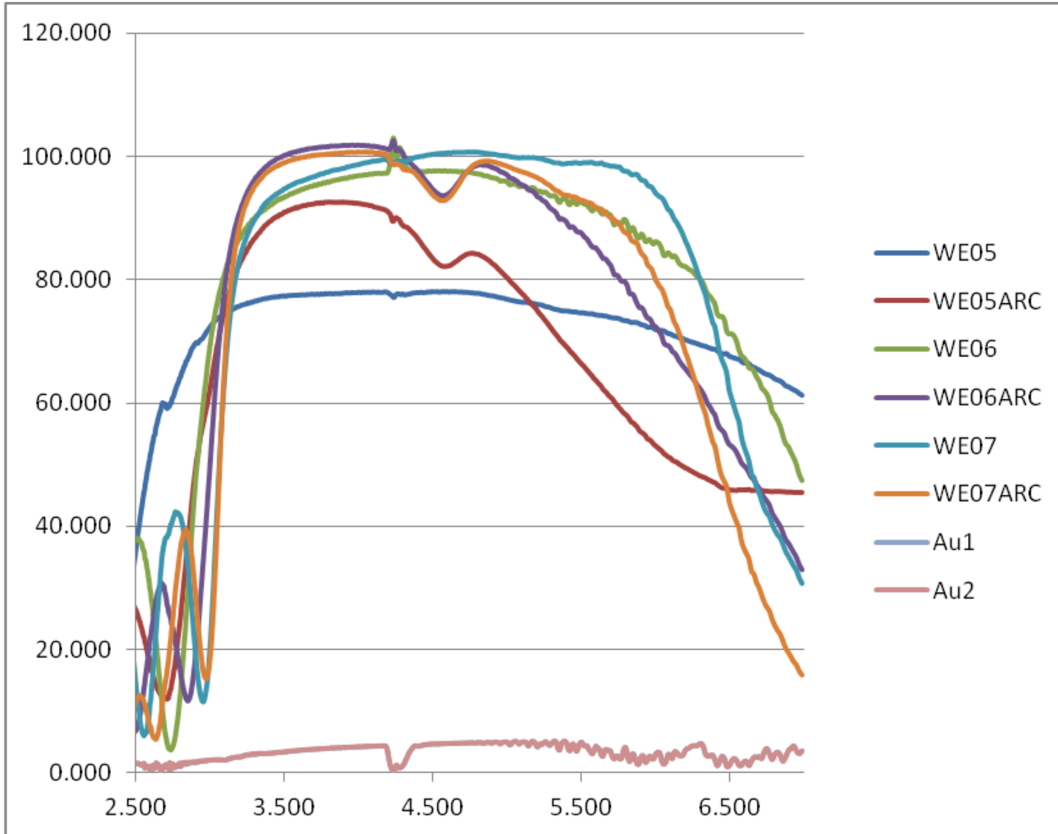


Figure 5.60: Transmission and reflection from fabricated chips (intensity (relative) vs. wavelength in microns)

In Fig. 5.60 above, WE05 is a single Bragg stack, WE06 is double Bragg stack, WE07 is triple Bragg stack, and WEXXARC are the stacks with silicon nitride anti-reflective layers. Just as a reminder, Bragg stacks consist of alternating germanium (250 nm thick) and silicon oxide (720 nm thick) layers, and the anti-reflective coating (ARC) is silicon nitride (500 nm thick).

Below is a discussion of the comparison of experimental data to a MATLAB simulation described in Chapter 2 and with code shown in Appendix A.

The single stack results are shown in the figure 5.61 below, experimental reflectivity data is plotted along with simulation data, for single Bragg stack, with and without ARC.

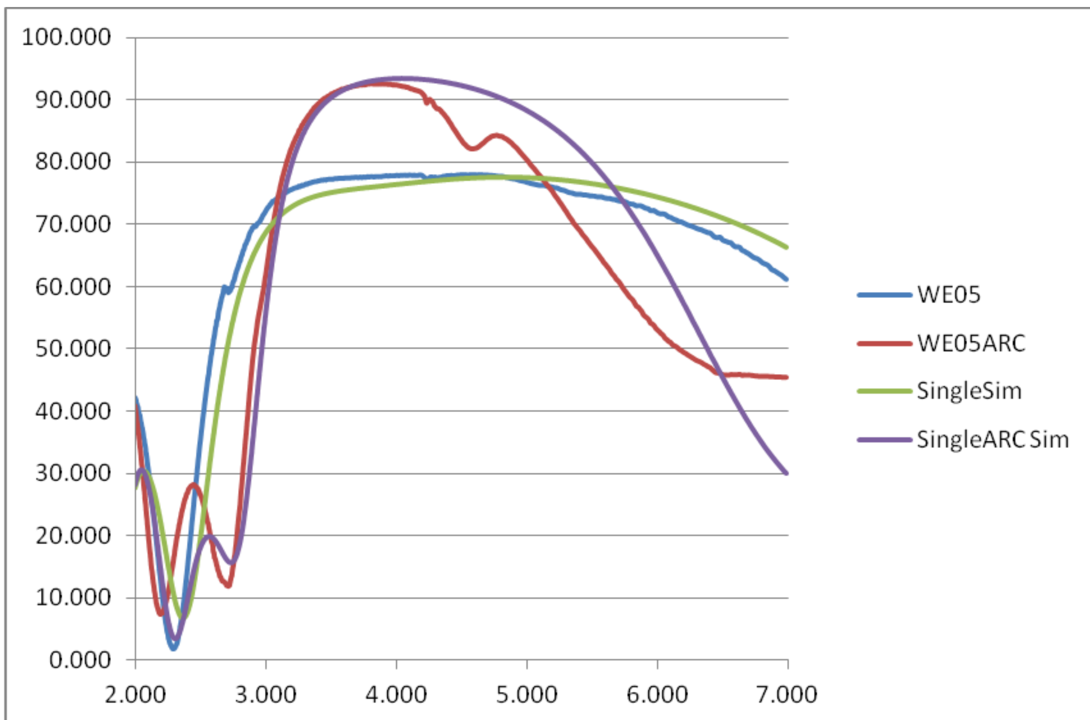


Figure 5.61: Simulation and test of reflection from fabricated chips, single stack (intensity (relative) vs. wavelength in microns)

The double stack data in Figure 5.62 below shows experimental reflectivity data plotted along with simulation data, for double Bragg stack, with and without ARC.

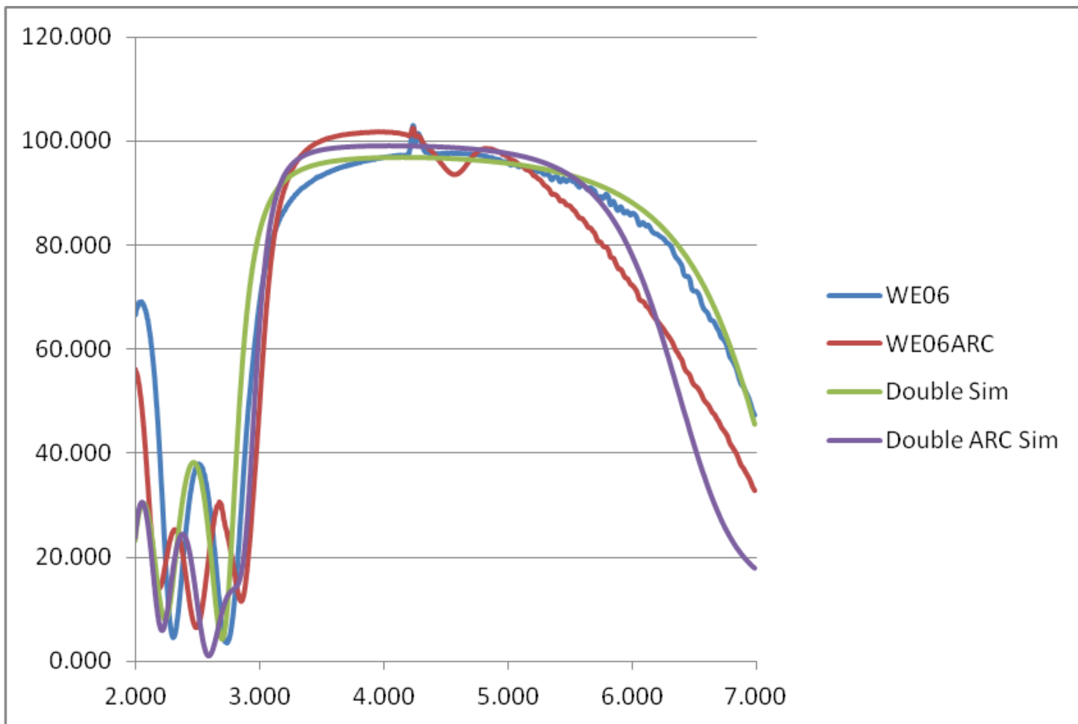


Figure 5.62: Simulation and test of reflection from fabricated chips, double stack (intensity (relative) vs. wavelength in microns)

The triple stack data in Figure 5.63 below shows experimental reflectivity results plotted along with simulation data, for a triple Bragg stack, with and without ARC.

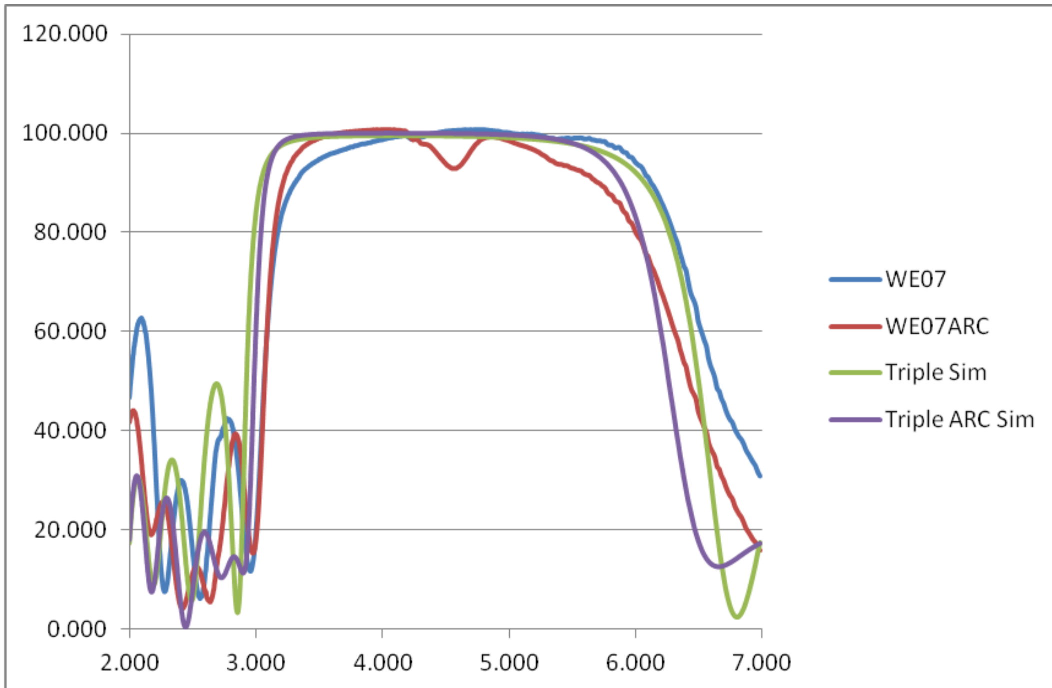


Figure 5.63: Simulation and test of reflection from fabricated chips, triple stack (intensity (relative) vs. wavelength in microns)

As can be seen, the correlation between experimental data and simulations are very good. This validation proves that simulation code is accurate, and the fabricated Bragg stack layers provide good optical reflection layers, with minimum defects affecting optical performance.

The major discrepancy is seen in layers with ARC, at a wavelength around 4.5 µm. All samples with ARC have a noticeable dip there, not seen in any other layers. My opinion is that it is caused by mild absorption by the silicon nitride layer. With proper analysis, this should not affect the behavior of the filter.

5.21 Bonded pair optical testing

The first series of tests performed was to test reflection and transmission of the single silicon membrane, silicon membrane with double Bragg stack, and silicon membrane with triple Bragg stack. The results are in Fig. 5.64 below.

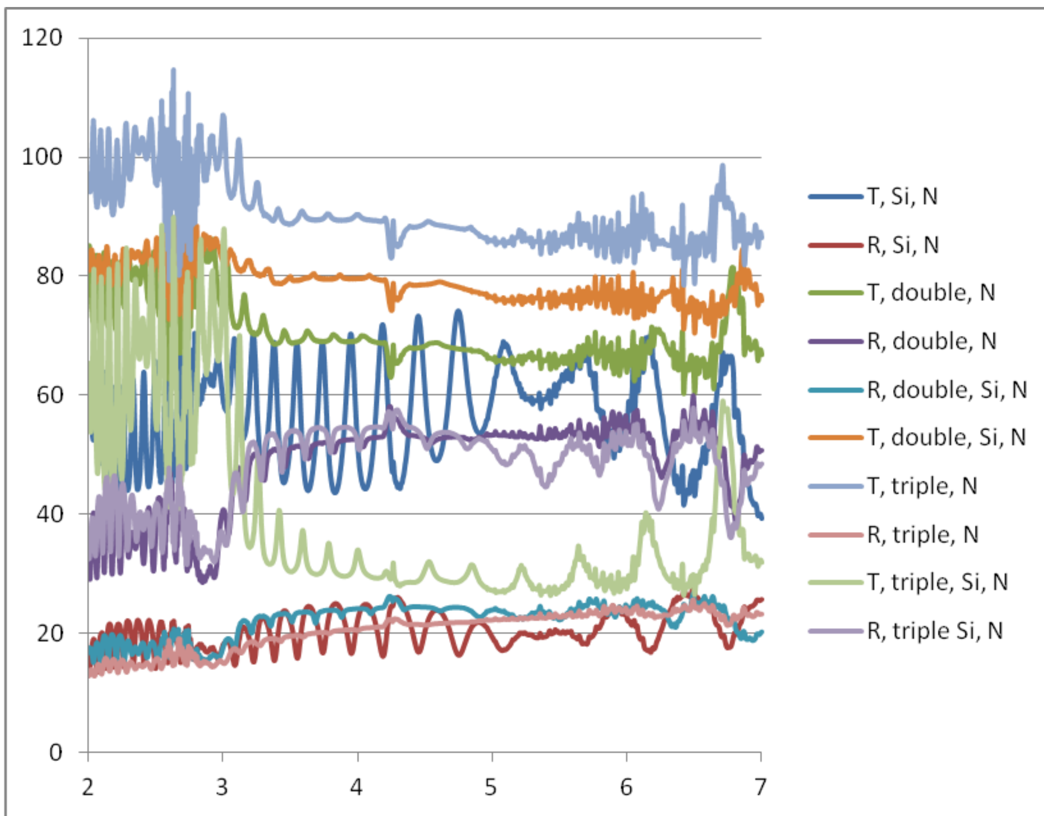


Figure 5.64: Experimental optical results for silicon, double and triple chips, (intensity (relative) vs. wavelength in microns)

None of the pairs of devices tested have produced significant filtering effects. In fact, most of the optical data from bonded pairs looks remarkably similar to reflection and transmission behavior predicted for single chips. This means that the surface defects

such as pinholes, roughness and curvature completely overwhelm the filtering done by Fabry-Perot effect.

Using the data from surface analysis, and assuming that the surfaces of the chips still maintain the reflectivity of 98%, the following can be concluded. The reflective finesse term is 155, and the defect finesse terms are as follows: finesse due to bowing is 0.044; finesse due to surface roughness is 1.89; effective finesse is dominated by the bowing term and is equal to 0.044. This results in FWHM= 90 μm at λ=4 μm.

5.22 Conclusion

In the first round of fabrication, key processes such as layer deposition and patterning have been explored. Several methods of depositing Bragg stack films have been done and analysis of the stress and optical quality. Reflectance data was obtained from single, double and triple Bragg stacks and was found to be in excellent correlation to optical simulations developed in previous chapters. Four SOI wafers have been put through complete processing steps with low yield and bad final surface quality. Bonded pairs were not of sufficient quality for use as a Fabry-Perot interferometer.

Chapter 6 : Second fabrication run

6.1 Introduction

This section is the analysis of the first fabrication run and identifies the mistakes, shortcomings of the first fabrication run and methods to improve them in the next run. To this end, we have done process analysis, inspection of the fabricated parts, and simulations that lead to better devices. After receiving optical data on the Bragg stacks, the MATLAB simulations were re-run for each case, and were compared to the experimental data, to make some conclusions about the optical component of the device. Mechanical part of the device was analyzed by simulations, especially focusing on stress compensation due to real stress data

6.2 Process analysis and modifications

As was observed in first fabrication run, there have been several problems in the process. They are re-hashed below:

The problem of rough edges of the wafer after TMAH etching is as follows: This resulted in edges of the wafers not being protected, and extremely rough sides (hacksaw) prevented wafers from being processed in standard equipment.

One of the possible solutions is to use a CVD furnace to deposit nitride, as it will be more conformal and cover edges. Sending the backside etching step to the back of processing might also mitigate this.

The problem with this method is that the windows are fragile; this turned out to be the most chip-killing problem. The fragility of the windows was unforeseen, and resulted in wafers not being able to go through such easy steps as blow-drying and photolithography.

The fragility was caused by too much released area and too thin a membrane. The backside etch windows don't have to be so large (5.6 mm across), and will have to be reduced. Size that can work for optical purposes is 3 mm across, thus reducing the area of the windows by a factor of 3.48, making them less fragile. If optical considerations allow, we might increase device layer thickness to 20 μm or above.

Another problem is the misalignment of the X-Beam mask to backside etch mask. This was caused by mask aligner not being able to see through the Bragg stack in IR mode, and find alignment marks on the other side. Neither did the global alignment marks, when etched through the wafer, provide accurate alignment.

Reversing the order of the process would solve the problem of misalignment. Define X-beam on the device layer first, using dry etching Bosh process. Pattern backside layer and align it to the top layer alignment marks without Bragg stack to impede IR vision. Move the backside window etching to the end of the process.

By performing the X-beam etching as the first step of the process, followed by deposition and etching of the Bragg stacks, with backside etching moved to the end of the process. Backside etching would be done in a specially designed holder that protects front of the wafer and the sides, eliminating the edge roughness and deposition/removal of many protective layers on the front. Dicing of the wafers

might have to be done by a laser process (outside vendor). The suggested process flow is in the diagram below (old process on the left, modified on the right):

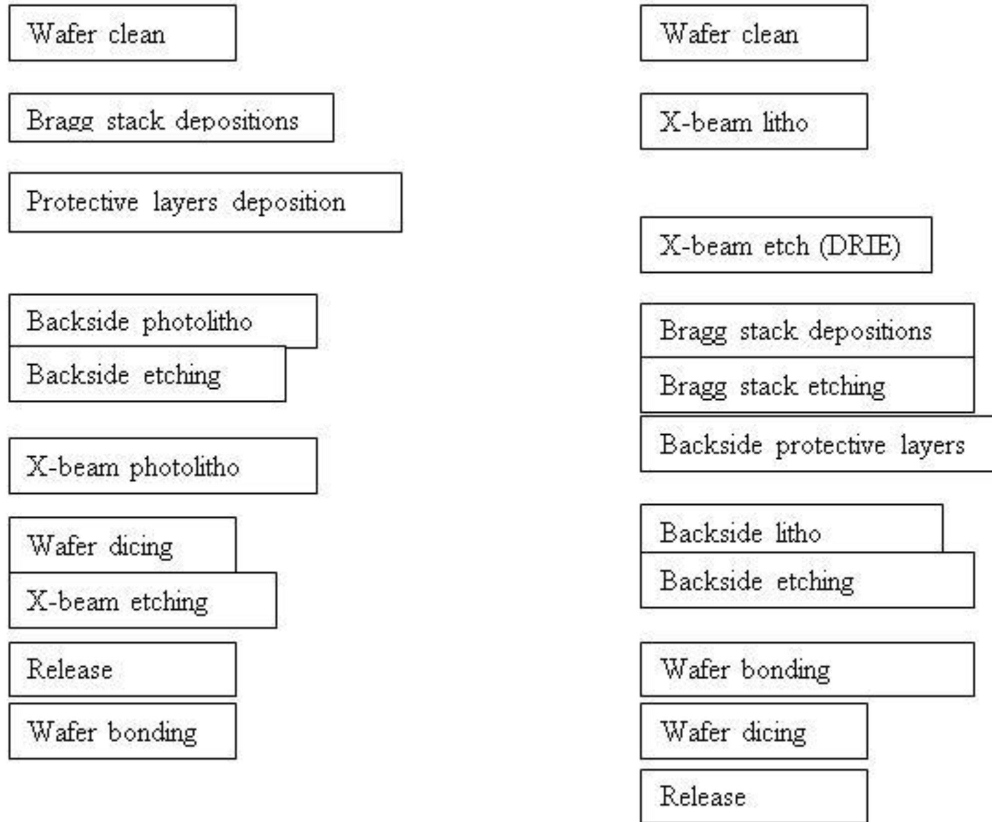


Figure 6.1 Comparison of fabrication flow

6.3 Stress simulations with input from fab

The original X-beam structure, as simulated previously, was modified by the addition of the Bragg stacks with real stresses measured during fabrication. The stress in the Bragg stack materials alone would not have caused as much deformation as was seen in the fabricated parts. Another large cause of stress in the structures was the stress in the device layer of the starting SOI wafer. As no test structures were included to

quantify this stress, simulation was performed in IntelliSuite [65] to get the value of this stress. This simulation was done by modeling the un-deformed shape of the X-Beam and the membranes, adding the Bragg stacks, and modeling deformation with the stress in the Bragg stack materials known from fabrication. Then, the stress in the device layer was increased, until the resulting deformation matched the fabricated one (Fig. 6.1).

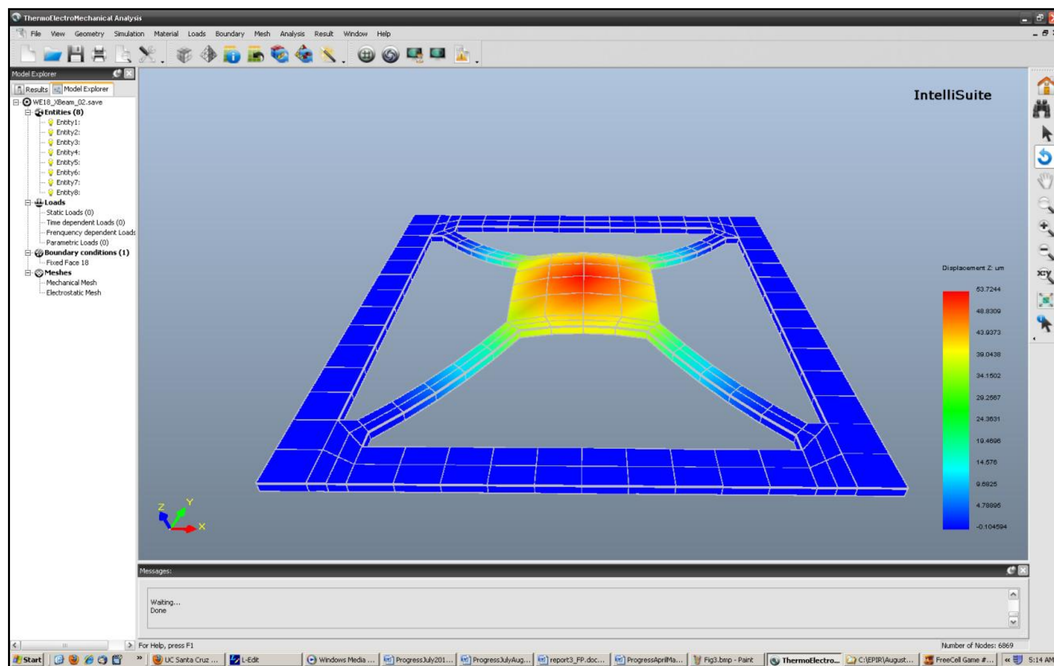


Figure 6.2 Simulation of the deformed X-Beam shape

The resulting stress in the silicon was calculated to be 100 MPa of compressive stress, much less than the 400 MPa stress in the SOI MUMPS wafers. This can be explained by the method used to fabricate SOI wafers: both handle and device wafers were diced from pre-fabricated boules of pre-doped high-quality silicon, bonded, and the

device wafer ground down to desired size. While this did introduce inevitable stress (grinding and polishing), it avoided the huge stress gradients from doping, present in SOI MUMPS wafers.

As was discussed in the first fab run, the bow in the X-beam and membranes can be compensated by deposition of silicon nitride layer, which acts as both stress compensator and anti-reflective coating. From our simulations, this layer would have to be of high compressive stress, 200 MPa. This can be easily achieved based on our development of stress vs. high/low frequency mix curve during fabrication.
After input of realistic stresses and bow compensation using silicon nitride layer, we have run several mechanical simulations to determine the behavior of the X-beam actuator (Fig. 6.3). Originally, the geometry of the X-beam (arm length and width) were developed to minimize the bow in the square section during actuation, with travel range from 4 μm to 1.6 μm, and actuation voltages of 0V-6V.
Addition of Bragg stacks and silicon nitride layer have completely modified the actuator behavior. With the same travel range, the actuation (prior to pull-in instability) happens only in the small 3V-3.5V range. This occurs due to stiff high-stress layers added, as well as Bragg stacks acting as multiple capacitors in parallel.

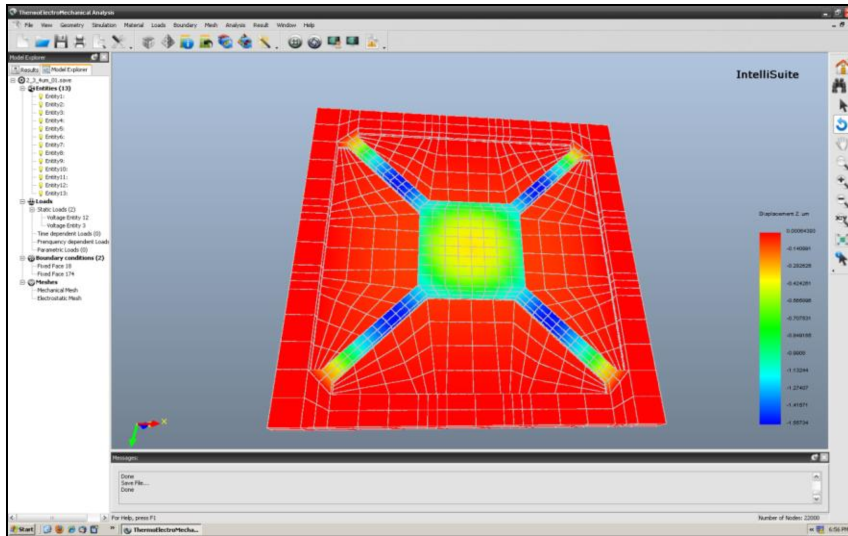


Figure 6.3 Simulation of the deformed X-Beam shape with silicon nitride compensating layer

6.4 Modifications to Layout

The first round of fabrication was successful in deposition of optical layers and investigation into individual steps of the process. The shortfalls of the original process flow and the layout was that optically active areas were designed to be 2 mm on the side, and this requirement has led to large size of the X-beams and membranes. Thin membranes with large surface area have resulted in large deformations due to stress, and very low yield during processing, as these membranes could not withstand small pressures that are inevitable during processing.

In order to increase yield and reduce the deformation of membranes and X-beams, it was necessary to reduce the area of released features. After consulting requirements of the detectors, it was decided that the maximum area needed for initial devices would be squares of 1 mm on the side, with possible reduction in the future. This

reduction has led to re-design of the chip, with active area 1 mm by 1mm, X-beam arms of 50 μm thickness and 700 μm length (Fig. 6.4), resulting in membranes of 1920 μm by 1920 μm, as compared to 7000 μm by 7000 μm in the previous design.

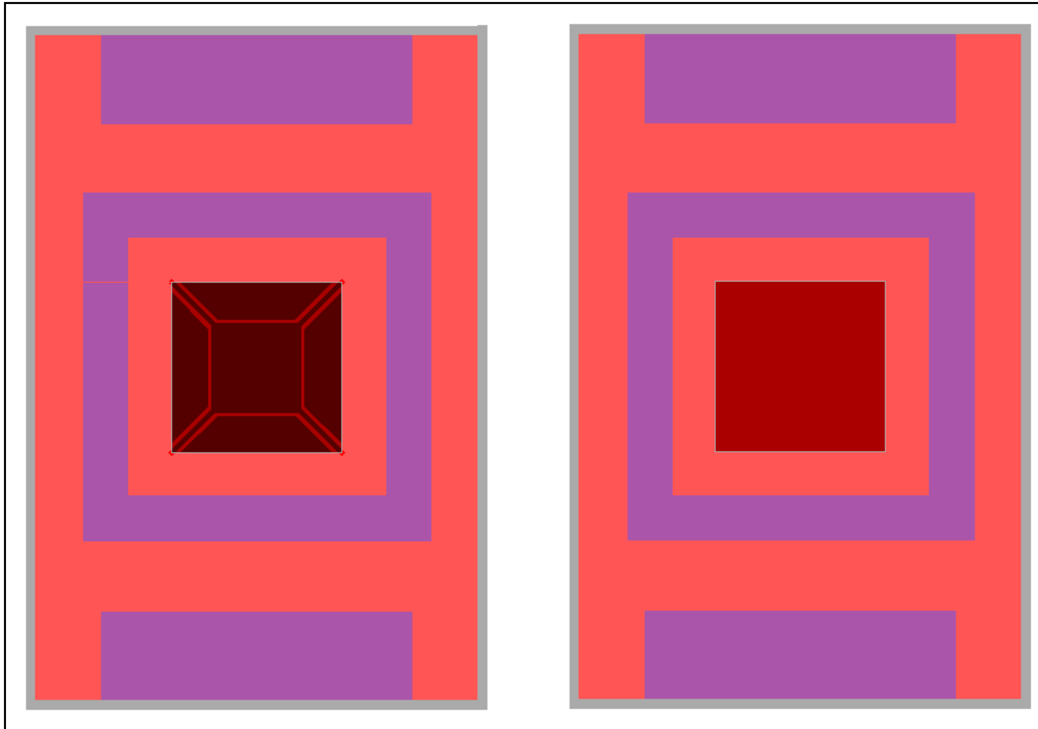


Figure 6.4: Layout for new round of fabrication

The size of the chips is decreased overall, and each chip would have only one membrane or X-beam. As compared to the previous design in Chapter 5, the chips would be placed across each other, as indicated in Fig. 6.5. The bonding of the chips would be done with metal-to-metal bonding, with 3 μm layer of gold and indium on each half. The metal layer is indicated in purple in the figures.

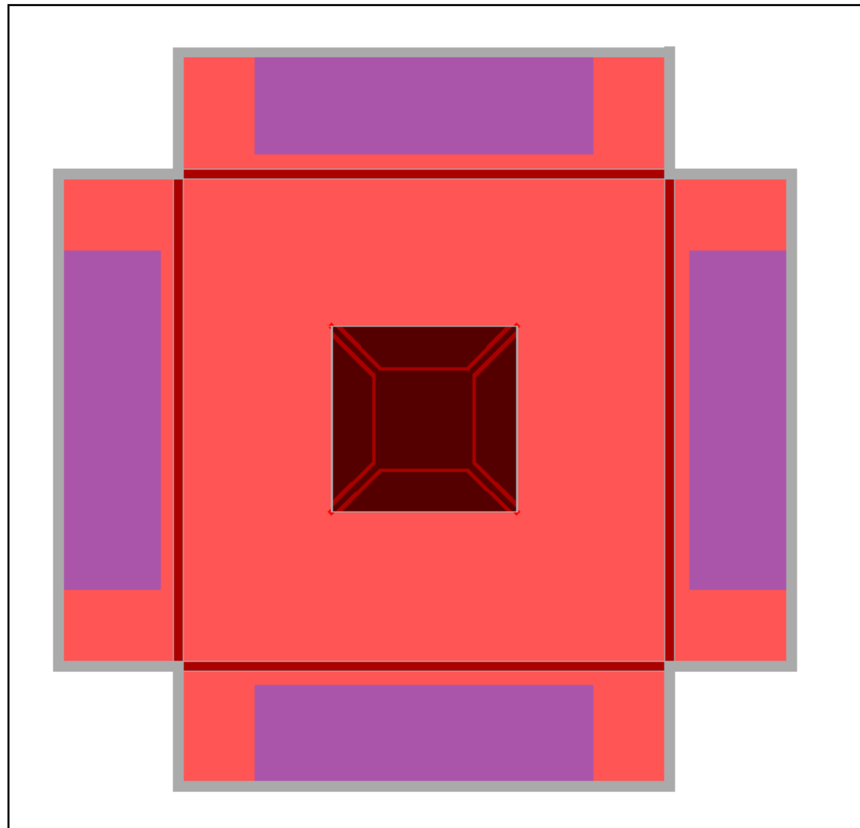


Figure 6.4: Schematic overlay and bonding

6.5 Modifications to the Process

6.5.1 SOI Wafer

As implied from the analysis above, the largest setback to the fabrication of the working device is the stress deformations in the mechanical parts. While the stress in

the Bragg stack layers could not be improved, the additional 100 MPa of stress in the device layer of the SOI wafer can be reduced.

In order to identify a SOI wafer combination (device layer thickness, BOX thickness, fabrication method) that would reduce the stress, the following points are considered: thicker device layer would provide stiffer mechanical base, and would not deform as much; thinner BOX would provide less stress. From the optical testing performed on the silicon membranes, the level of optical absorption is small, and therefore doubling the thickness of the silicon device layer should not adversely affect the optical performance. After reviewing the inventory of the supplier of the SOI wafers we use, Ultrasil Co. of Hayward, CA, we identified a stock of wafers with 20 μm device layer and 1 μm BOX layer.

As the stress is such an important issue in these devices, the first step of fabrication in the next cycle would be to try to verify the reduction of stress in SOI, before committing to further processing. To do this, I have added multiple stress testing structures to the layout. These structures would be etched in the device layer and released. By measuring the difference in gratings before release and after release, the stress in the silicon layer can be calculated.

6.5.2 Different Silicon Etch

As was mentioned in the section on the interferometry of the resulting devices, defects in the layers have caused further asymmetrical deformation of the devices and membranes. This resulted from etching steps and defects in the masking materials, and removal of the masking materials. While wet etching of the backside of the

wafer has been developed, the numerous protective layers it requires, and added complexity of the process, might be the cause of the added defects. Therefore, it makes sense to try a different process for the etching of the handle wafer. Deep reactive ion etching (DRIE), Bosch process, is available at SNF, and is a possible substitute for the wet backside etching.

6.5.3 Silicon Nitride Compensation

While there was no time in the first process run to add silicon nitride compensating layer to the backside of the chips, it is possible in the second run. After simulations described above and extraction of the stress needed to balance stress of the Bragg stack, tests will be performed to determine if the 200 MPa compressive silicon nitride would indeed compensate the bow in the X-beams and membranes.

6.6 Process flow for second run

The etching steps in the first fabricated run have resulted in extreme high degree of defects and very poor surface quality of the chips.

In the second run, the following process flow was used, for the reasons described above:

Step 1: The wafers were cleaned using standard RCA cleaning process, which removes organics, metals and native oxide on silicon layers.

Step 2: Device silicon layer was etched using DRIE process, with thick photoresist mask baked for 12 hours.

Step 3: Bragg stacks were deposited on the wafer using PECVD for silicon oxide and e-beam evaporation for germanium.

Step 4: Bragg stacks were etched using hard mask consisting of chrome and gold, using two-step wet etching process, HF for etching oxide film and hydrogen peroxide for etching germanium.

Step 5: Gold contact pads were deposited on the chips and defined using wet process.

Step 6: The backside window was etched using DRIE process, using thin layer of silicon oxide as hard mask.

Step 7: The chips were diced using wafer saw.

Step 8: The buried oxide was removed by dipping the chips in HF for 5 minutes. For this step, the Bragg stacks were protected using photoresist layer.

Step 9: The photoresist layer was removed and chips cleaned by soaking in acetone, methanol, and ethanol with consecutive bake at 100 ^{0} C for 1 hour.

6.7 Analysis of fabricated chips

After analyzing the chips produced by the process described above, it was determined that surface defects were down to minimum, with no visible pinholes and surface roughness reduced to 60 nm. The yield of the process was greatly increased to 80%.

The main problem remaining in the deformation of the X-beam and membrane surfaces was due to stress in the Bragg stacks. The bow of the X-beam was 2.7 μm in the X-beam component (Fig. 6.6), and 200 nm in the membrane.

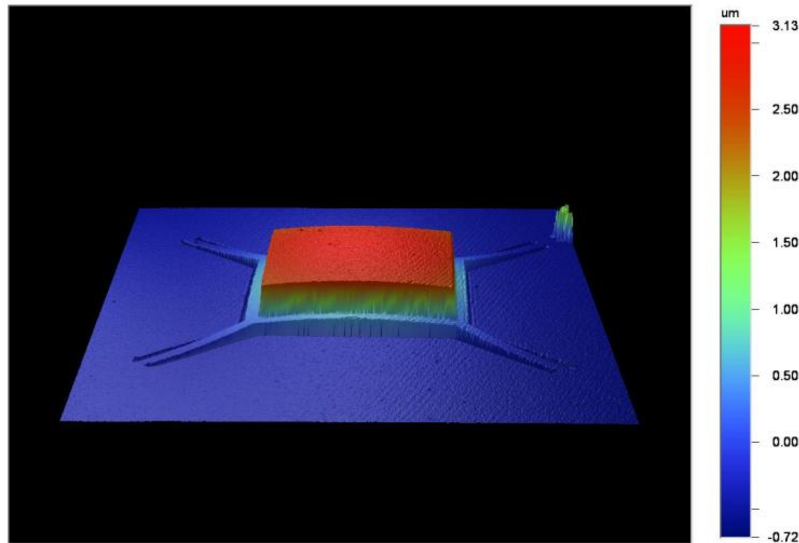


Figure 6.5: Bow in the X-beam component

The resulting bow in one of the two mirrors (ie. the fixed membrane component and the X-beam component) would cause drastic problems in the optical performance of the filter. In the first fabrication run, the change in height in the optically active area (the Bragg stack on the X-beam) was more than 15 μm from center to edge. Since the optical cavity is only modulated between 2.5 μm to 1.5 μm when filtering irradiant light, such a variation in membrane height would have a very significant change on cavity length and would result in a widening of the filter's FWHM to the point of complete loss of filtering ability.

6.8 Analysis of stress

There are two sources of the bow in the X-beam, the asymmetrical stress in the SOI wafer caused by the buried oxide (BOX) layer (Fig. 6.7), and the stress in the Bragg stack layer (Fig. 6.8).

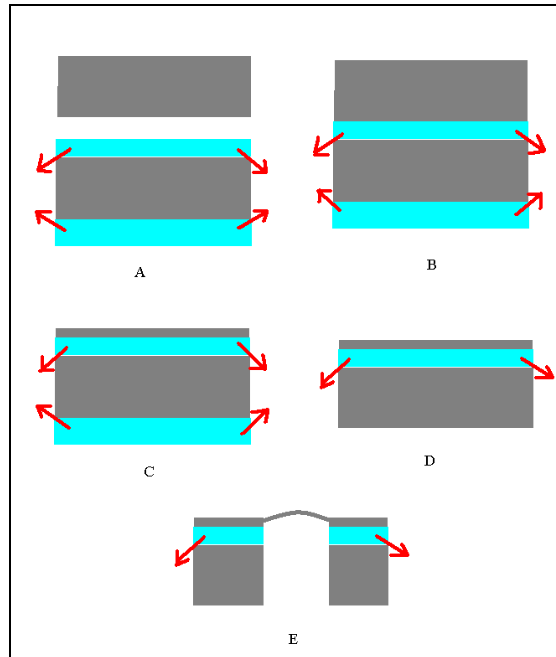


Figure 6.6: SOI fabrication process with resulting stress

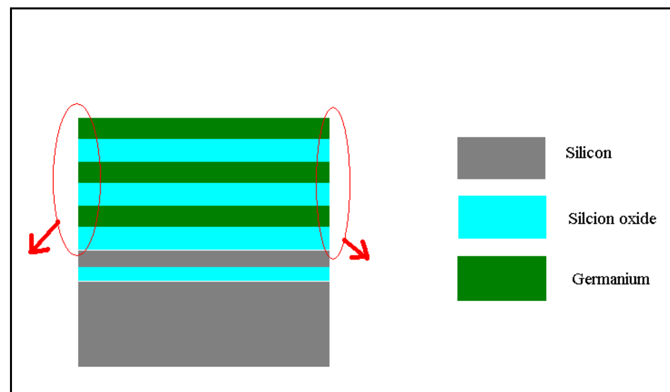


Figure 6.7: Wafer-scale stress caused by the Bragg stack

6.9 Attempts to reduce the bow

There are several ways to reduce the deformation caused by the internal stresses. Two of the ways that were attempted here were thermal annealing and deposition of compensating stress layer on the back of the chips.

6.9.1 Thermal annealing

Thermal annealing involves heating up the wafers or chips to high temperatures. This is usually used when the stress is caused by thermal mismatch after deposition, for example, silicon oxide film deposited at 350 degrees matches the underlying germanium layer, but after cooling to room temperature, the difference in coefficients of thermal expansion causes stress. The idea behind the thermal annealing is to heat up the final devices beyond the highest temperatures of deposition, and allow the films to re-form to lower energy point, when they are matched.

A series of tests were performed using an oven with slow ramp up and ramp down cycles, performed in the ambient. Table 6.1 shows the steps performed and the final bowing in the X-beam chips fabricated during second fab run.

Table 6.1: Effect of high temperature on bowing

Trial #	Highest temperature	Time held at highest temperature	Final bowing
0 –as fabricated			2.7 µm
1	100	12 hours	2.7 µm
2	300	12 hours	2.73 µm
3	400	12 hours	2.75 µm
4	500	12 hours	2.65 µm
5	600	12 hours	2.63 µm

As can be seen from the results, the reduction in the bowing was not significant. Visually, the Bragg reflectors changed color after the 500 degree anneal. When reflectivity of these annealed chips was measured, it was found that the reflectivity dropped from 98%, as deposited, to less than 10%.

The drastic decrease in the reflectivity can be explained by the rapid oxidation of the germanium layers in the Bragg reflectors. When these layers undergo deposition, it is done under vacuum conditions. Triple Bragg reflectors have germanium layers between silicon oxide, which is very rich in oxygen atoms. When the chips are heated to beyond 400 degrees, the mobility of these oxygen atoms is increased, resulting in their leakage into germanium layers and producing germanium oxide. As

the reflectivity of the Bragg reflectors is highly dependent on the index of refraction matched to the layer thickness, layers of germanium oxide sandwiched between silicon oxide do not act as reflectors in the MWIR.

6.9.2 Compensating layer depositions

As was described in the beginning of this chapter, finite element modeling showed that depositing compensating layer on the back of the X-beams, to match in stress the Bragg stacks, would reduce the deformation.

Silicon nitride, 500 nm thick, was deposited on the back of the chips using frequency combination that produced stress of 200 MPa compressive.

The chips were scanned, and it was determined that the bowing was increased from 2.7 μm to 2.95 μm. Deposition of zero-stress silicon nitride layer did not produce any change in the bow, and deposition of 300 MPa tensile layer has reduced the bow to 2.57 μm.

The difference in the bow reduction from the finite element analysis shows that the complexity of the system cannot be accurately predicted by the model. As the deposition of Bragg stacks happen before release of the components, and deposition of the compensating layers happens after, and is not limited only to the back of the X-beam, but covers the entire back of the chip, the model assumption that all the layers are deposited at once and are released is inaccurate.

6.9.3 Using silicon nitride in the Bragg stacks

The stress in the silicon oxide cannot be reduced below 190 MPa compressive, but the stress in the silicon nitride layers can be controlled by the frequency of the plasma during deposition. Refractive index of silicon nitride is not that far from the index of silicon oxide, and can be well used to produce highly reflective Bragg stacks.

After optical analysis, a test was performed to determine if the layers of silicon oxide could be replaced by layers of silicon nitride. A triple Bragg stack composed of germanium and zero-stress silicon nitride on a standard wafer was deposited. Unfortunately, the resulting stack was extremely unstable. The layers started to de-laminate almost immediately after final deposition, and delaminated completely during the photolithography steps.

6.10 Optical terms

From the information obtained from the surface analysis and the bowing, prediction of filtering behavior can be continued. The reflective finesse term is 155, and the defect finesse terms are as follows: finesse due to bowing is 0.490; finesse due to surface roughness is 17; effective finesse is dominated by the bowing term and is equal to 0.49. This results in a FWHM= 8.56 μm at λ=4 μm. Compared to the results of the first fabrication run, this is an improvement of effective finesse by an order of magnitude, and also decrease in the FWHM by an order of magnitude.

6.11 Conclusion

In the second fabrication run, a process flow that is greatly reduced in its complexity was developed. The resulting devices showed low surface roughness and zero defects. The bowing in the X-beam and membrane still remains a major issue. Several steps have been taken to reduce the bowing, without any significant results.

Chapter 7 : Third fabrication run

7.1 Introduction

This chapter will describe third and final fabrication run. Significant changes to the fabrication process were made, including the substrate and layout. This process produced very high yield and minimized defects, as well as reduce the bowing in X-beams. Results on surface morphology are presented.

7.2 Modifications to the previous Fabrication Process

The fabrication flow established in the previous fabrication cycles was intended to decrease the number of defects and provide a robust and simple process that could be extended from the fabrication of single-pixel devices to the fabrication of arrays. The key steps of the process were:

1) Selecting an appropriate SOI wafer for the substrate
2) Patterning the device layer of the SOI through deep reactive ion etching (DRIE)
3) Depositing the Bragg stack by using PECVD and e-beam evaporation for silicon dioxide and germanium respectively
4) Wet etching the Bragg stack by subsequent immersion in 6:1 BOE and in hot hydrogen peroxide for removal of the silicon dioxide and germanium layers respectively
5) DRIE etching of the backside of the wafer to open the optical window

It has been shown that this process can be applied to different device geometries and different SOI wafer configurations without significant changes except for adjusting the timing of some steps.

In the third run, to compensate for the asymmetrical BOX layer in the SOI, an additional silicon dioxide layer was deposited on the back of the wafer. The stress in the 0.33 μm BOX layer was matched with a 0.56 μm layer deposited by PECVD (Fig. 7.1). The difference in thickness was caused by a lower stress in the PECVD oxide layer; therefore a thicker layer was necessary.

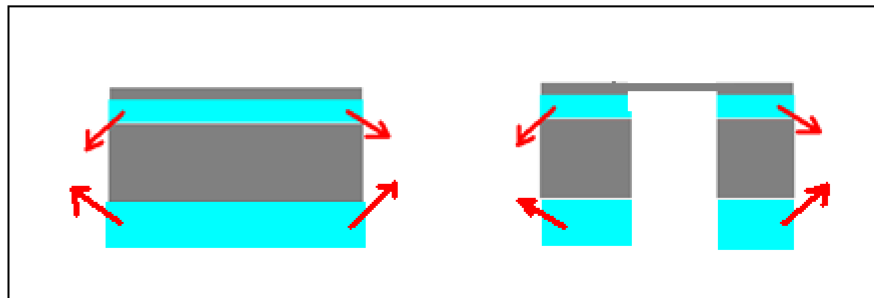


Figure 7.1: BOX compensation

7.3 Layout modifications

The area of the Bragg stack was reduced to that of only the active optical area, in the center of the X-beam component and the fixed membrane component (Fig. 7.2).

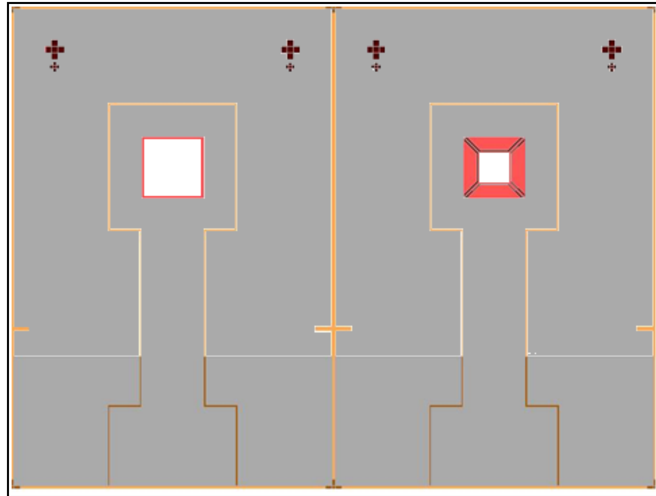


Figure 7.2: Modified layout of the chips with Bragg stack in white areas

The modification of this mask was potentially problematic, since previous modifications to the area of the Bragg stack caused complete de-lamination of the materials during the etching process (implemented in the second fabrication cycle with the silicon nitride – germanium stack). Therefore, it was thought initially that the change in geometry was one of the causes of de-lamination. In order to verify this, a test wafer was produced with the newly modified geometry and a silicon dioxide-germanium stack. The test wafer was then subjected to the Bragg etching process using subsequent etching in liquid bath of 6:1 BOE and hot hydrogen peroxide. The process did not cause de-lamination, and it was therefore concluded that the de-lamination in the second cycle was instead caused by the low silicon nitride-germanium adhesion.

The end goal of this project is the fabrication of large-scale arrays; therefore, several chips were incorporated into each wafer in order to test the viability of the inclusion

of arrays with smaller optical areas. The layouts of these two arrays are shown in Figure 7.3 and Figure 7.4.

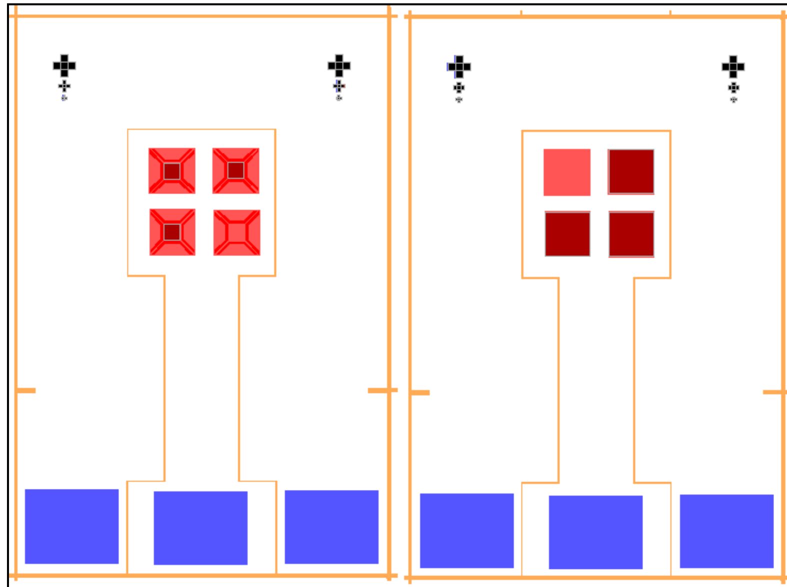


Figure 7.3: Array of 500 µm by 500 µm devices (4-array)

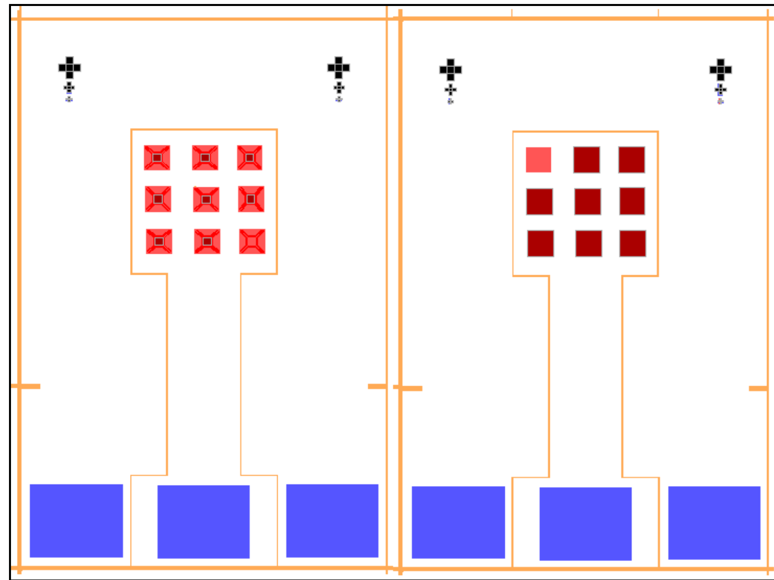


Figure 7.4: Array of 250 µm by 250 µm devices (9-array)

The four masks used for this fabrication process are shown overlaid with each other in Figure 7.5.

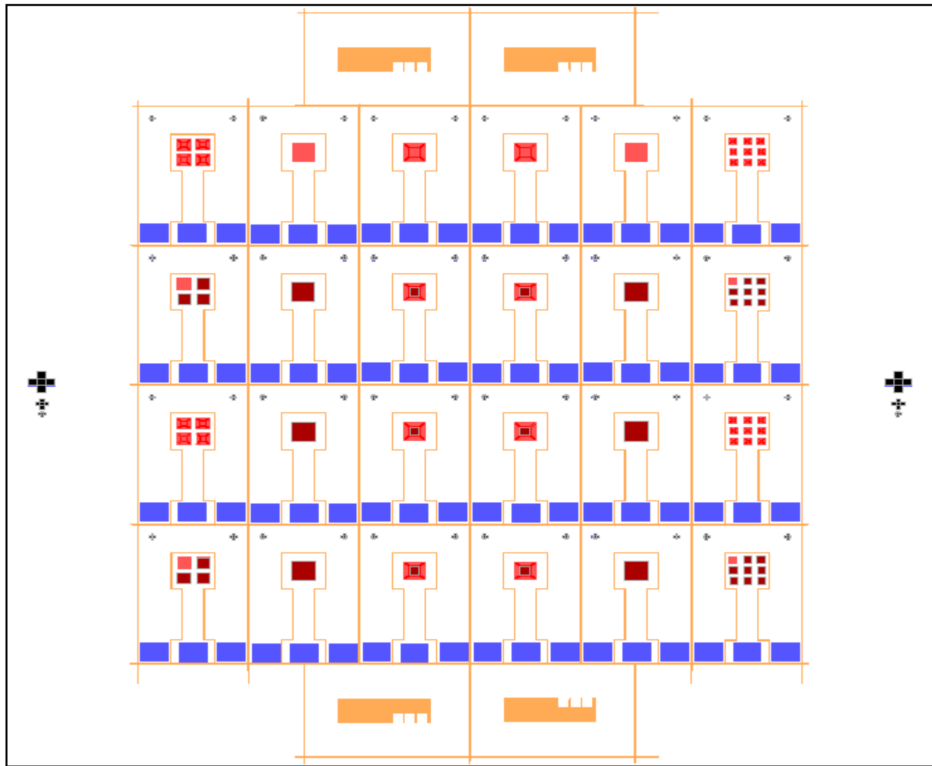


Figure 7.5: Four masks used for the fabrication

In the figure 7.5, the following colors correspond to the following masks:

a) **Orange**: Used for the first DRIE step which defines the device layer

b) **Black**: Used for defining the Bragg stack

c) **Red:** Used to etch the backside window

d) **Blue:** Used to define the gold electrodes

As can be seen in figure 7.5, each wafer consisted of:

- 6 X-beam chips with a Bragg stack
- 6 membrane chips with a Bragg stack
- 2 X-beam chips without a Bragg stack

- 2 two membrane chips without Bragg stack
- 2 sets of 4-arrays
- 2 sets of 9-arrays

7.4 Substrate modification

Finally, three new SOI wafers were used in this fabrication cycle. Table 7.1 shows the various SOI wafers used in all the fabrication cycles to date. The main modifications in this cycle consisted of increased device and handle layers with a reduced BOX layer.

Table 7.1: SOI wafers used in several fabrication cycles

Cycle (Dates)	Device Thickness (µm)	BOX Thickness (µm)	Handle Thickness (µm)
July 2010	5	2	300
October 2010	10	0.5	300
February 2011	25	0.5	300
July 2011 (WE52)	50	0.3	200
July 2011 (WE53)	75	0.3	300
July 2011 (WE54)	100	0.3	550

7.5 Stress Test Structures

One of the biggest problems in the first round of fabrication was the stress in the SOI wafer. As mentioned above, a new SOI configuration was chosen, and the wafer with a 0.3 μm BOX and 25 μm device layer was purchased.

In order to test the stress in the device layer that comes only from the SOI wafer, a set of test structures was designed. These structures are commonly known as V-beams, and are used for determination of either compressive or tensile stress in thin films [66]. A layout of one of the structures used is shown in Fig. 7.6.

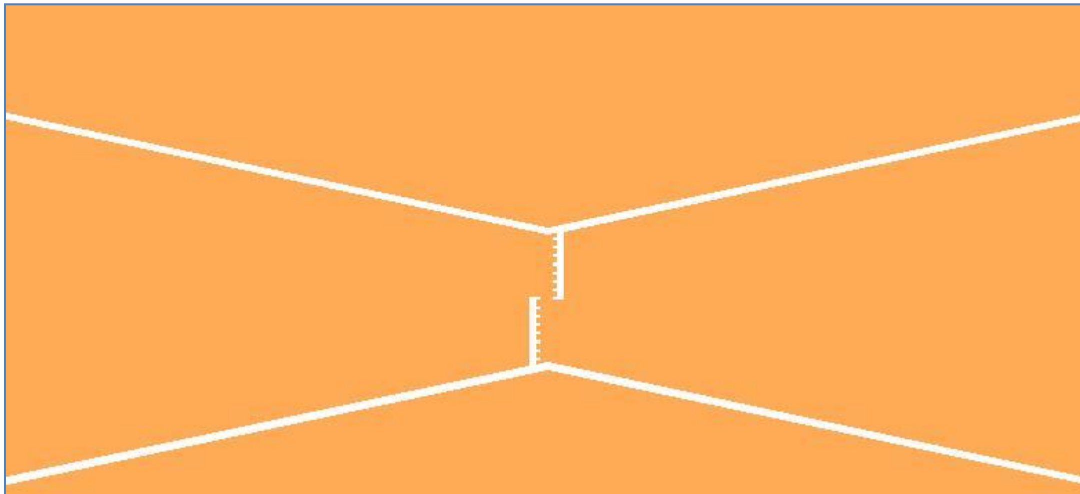


Figure 7.6: Layout of Bow Tie stress test structures

These structures transfer either compressive or tensile stress that is most pronounced along the direction of the longest dimension of the beam (y-direction, in the figure) and transfer the deflection caused by the stress into movement of calibrated bars in the direction normal (y-direction in the figure). By determining the deflection of the beams by measuring the relative position of the bars before and after release, and

doing some calculations, the stress level in the film is determined, along with sign (compressive or tensile).

For this fabrication cycle, a chip with nine V-beams was designed. The V-beams differed in thickness of the beams and angle of curvature (Fig. 7.7).

After measurements on several chips before and after etch and release, it was determined that the stress in the SOI wafer was on the order of 10 MPa compressive. As compared to the stress in SOI wafers used in first and second fabrication runs, this is an improvement by an order of magnitude and will result in lower stress-induced deformations.

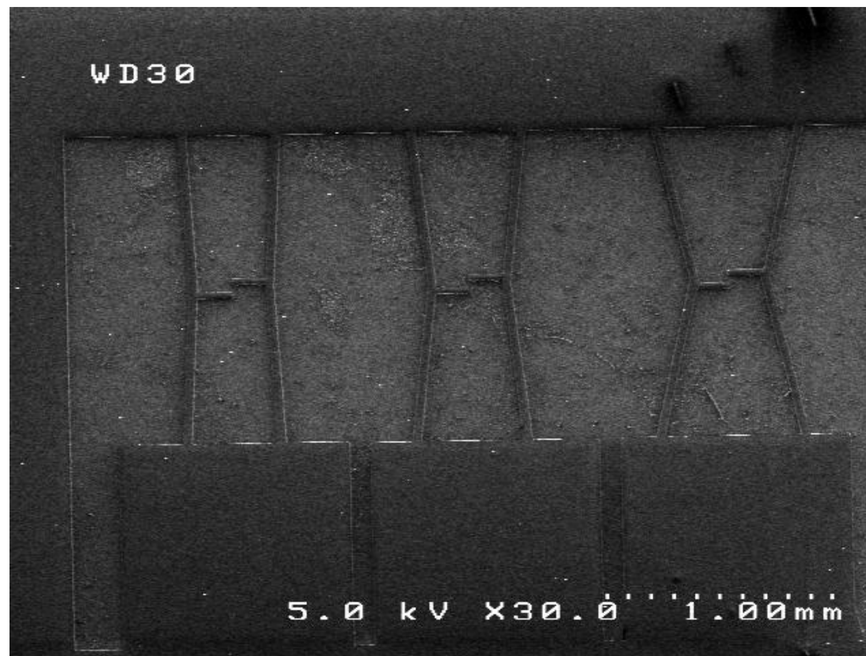


Figure 7.7: SEM image of V-beam test structures

7.6 Fabrication Process

Except for the changes in geometry and substrate, there have been no major modifications to the fabrication flow from second run. All the etching of silicon was done using dry etching, DRIE process. The etching of the Bragg stacks was done by subsequent wet etching process with hard masks composed of chromium/gold layers, buffered oxide etch for the silicon dioxide layer and hot hydrogen peroxide for the germanium etch.

7.7 Fabrication Cycle Results

Four device wafers and six control wafers were processed in this fabrication cycle. The device wafers were SOI wafers consisting of the layers shown in Table 7.1, plus one other wafer recovered from February fabrication cycle. The control wafers were standard 100 mm diameter C-Prime wafers of 350 μm thickness. The following naming convention was used during this fabrication cycle:

- The 25 μm device wafer: WE41
- The 50 μm device wafer was called WE52
- The 75 μm device wafer was called WE53
- The 100 μm device wafer was called WE54

Chips without a Bragg stack were also included in order to measure the deformation of the device layer resulting from purely internal SOI stresses. All the wafers were

subjected to the entire process flow while maintaining 100% yield (all the x-beam and membrane chips survived the processing).

7.8 Fabrication Issues

There were two key issues encountered during this fabrication cycle that were previously unseen; these included the non-uniformity of the photoresist coverage during photolithography steps, and also the incomplete release of device components. Both of these issues resulted from the much thicker device and handle layers in the new SOI wafers.

The non-uniformity of the photoresist coverage resulted from trenches etched in the device layer that were much deeper (50, 75 and 100 μm) than on previous 25 μm layers. This resulted in streaks of photoresist in a radial pattern originating at the center of the wafer. The most noticeable results were an incomplete removal of the Bragg stacks in some regions and the incomplete removal of the final metallization layer. The most problematic of these is that some metal remained on top of the Bragg stacks in the X-beam components (red regions in figure 7.8).

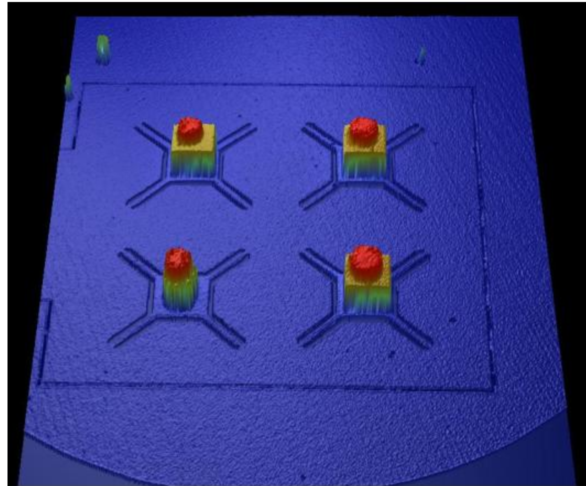


Figure 7.8: Metallization Remaining on WE54 wafers, 4-array chips

This issue was least noticeable in the thinnest wafer and most noticeable in the thickest wafer; however, an immediate work-around was achieved by hand-dipping the chips in gold etchant to remove the remaining metal. A long-term solution would be to increase the exposure and development times during photolithography steps which would reduce the thicker streaks of the photoresist.

The second issue was encountered during the release of the chips. The release step involves the submersion of the wafer (with etched optical windows down to the BOX layer) into a wet bath of 6:1 BOE, in order to remove silicon dioxide that remains on the backside of the X-beams and the membranes. However, this was complicated by the presence of trapped air bubbles in the optical windows. The much thicker handle wafers used in this cycle created a geometry that trapped air and prevented liquid etchant from reaching the BOX layer. Once this complication was noticed, air

bubbles were removed using needle-tipped tweezers from each window. A long-term solution would be to add ultrasonic agitation during the bath.

7.9 **Bow Reduction Results**

The results of this fabrication cycle demonstrate that the issue regarding the X-beam bowing has been successfully resolved. A large number of chips were produced in this fabrication cycle, resulting in a vast amount of data which highlight the effects of the three methods used to reduce the X-beam bow. The fixed membranes on all wafers exhibited practically zero bowing (Figure 7.9); therefore, the following discussion will be focused primarily on the X-beam components.

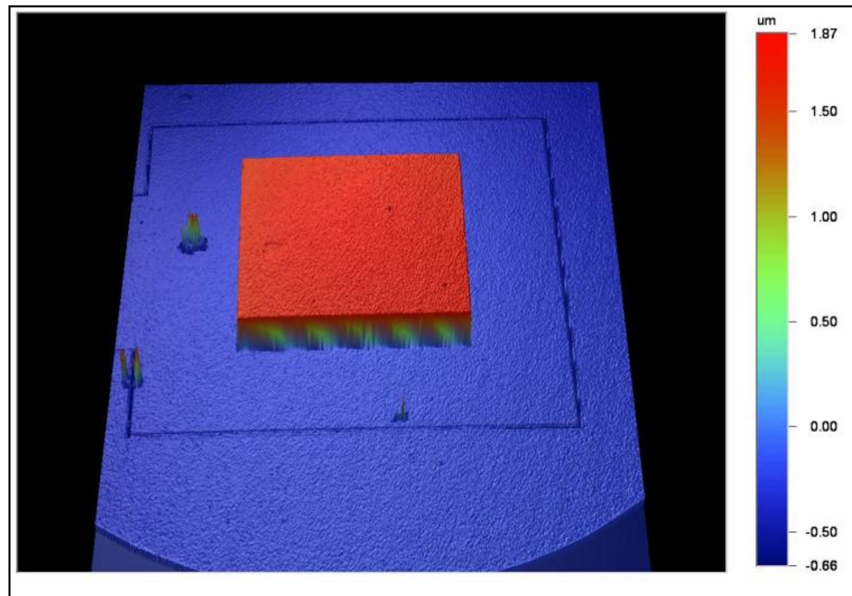


Figure 7.9: Membrane with Bragg stack, from wafer WE52

Before discussing the bowing reduction in the X-beam components, several terms should be defined in order to clarify the data. The bowing is evaluated using white-light interferometry. The following key parameters are considered:

- **Floor-to-X-beam (F2X)**: This parameter is the distance between the surface of the wafer and the top of the device layer of the SOI (figure 7.10 A).
- **Curvature of the Bragg stack (CBS)**: This parameter is the difference in height from the edge of the Bragg stack to the center of the Bragg stack. This is effectively the curvature of the mirror (figure 7.10 B).
- **Floor-to-top (F2T):** This parameter is the distance from the lowest level of the chip to the top of the Bragg stack. It is important in determining the thickness of the bonding layer to produce the optical cavity (figure 7.10 C).

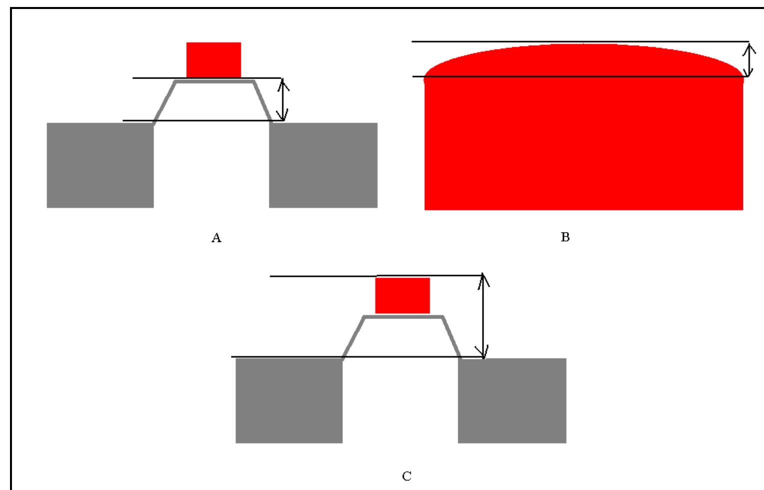


Figure 7.10: Parameters in the bow discussion

Tables 7.2, 7.3 and 7.4 show the aforementioned parameters for the three device wafers, WE52, WE53, WE54 respectively. Figures 7.11, 7.12, and 7.13 show representative scans from several chips.

Table 7.2: WE52 component measurements

Component	Bragg height (μm)	F2X (μm)	CBS (μm)	F2T (μm)
X-beam, No Bragg	--	0.178	0.06	2.184
Membrane, No Bragg	--	--	0.024	0.024
X-beam, Bragg	2.0	1.03	0.47	3.53
Membrane, Bragg	2.0	--	0.2	2.2
4-Array, X-beam, No Bragg	--	0.0	0.0	0.0
4-Array, Membrane, No Bragg	--	--	0.0	0.0
4-Array, X-beam, Bragg	2.0	0.20	0.036	2.23
4-Array, Membrane, Bragg	2.0	--	0.095	2.095
9-Array, X-beam, No Bragg	--	0.0	0.0	0.0
9-Array, Membrane, No Bragg	--	--	0.0	0.0
9-Array, X-beam, Bragg	2.0	0.126	0.01	2.126
9-Array, Membrane, Bragg	2.0	--	0.079	2.079

Table 7.3: WE53 component measurements

Component	Bragg height (µm)	F2X (µm)	CBS (µm)	F2T (µm)
X-beam, Bragg	2.0	0.54	0.18	2.76
Membrane, Bragg	2.0	--	0.056	2.056
4-Array, X-beam, No Bragg	--	0.0	0.0	0.0
4-Array, Membrane, No Bragg	--	--	0.0	0.0
4-Array, X-beam, Bragg	2.0	0.18	0.026	2.23
4-Array, Membrane, Bragg	2.0	--	0.057	2.057
9-Array, X-beam, No Bragg	--	0.0	0.0	0.0
9-Array, Membrane, No Bragg	--	--	0.0	0.0
9-Array, X-beam, Bragg	2.0	0.041	0.0031	2.046
9-Array, Membrane, Bragg	2.0	--	0.008	2.008

Table 7.4:WE54 component measurements

Component	Bragg height (µm)	F2X (µm)	CBS (µm)	F2T (µm)
X-beam, No Bragg	--	0.0045	0.023	2.03
Membrane, No Bragg	--	--	0.024	0.024
X-beam, Bragg	2.0	0.25	0.095	2.36
X-beam, Bragg	2.0	0.15	0.095	2.35
Membrane, Bragg	2.0	--	0.026	2.026
4-Array, X-beam, No Bragg	--	0.0	0.0	0.0
4-Array, Membrane, No Bragg	--	--	0.0	0.0
4-Array, X-beam, Bragg	2.0	0.045	0.00	2.045
4-Array, Membrane, Bragg	2.0	--	0.011	2.011
9-Array, X-beam, No Bragg	--	0.0	0.0	0.0
9-Array, Membrane, No Bragg	--	--	0.0	0.0
9-Array, X-beam, Bragg	2.0	0.01	0.0063	2.01
9-Array, Membrane, Bragg	2.0	--	0.011	2.011

The data in the tables above represents the performance across many component structures. Table 7.5 below consists only of the large X-beam components with the Bragg stack for three wafers, and demonstrates how modifications in device and handle layer thicknesses affect the bowing.

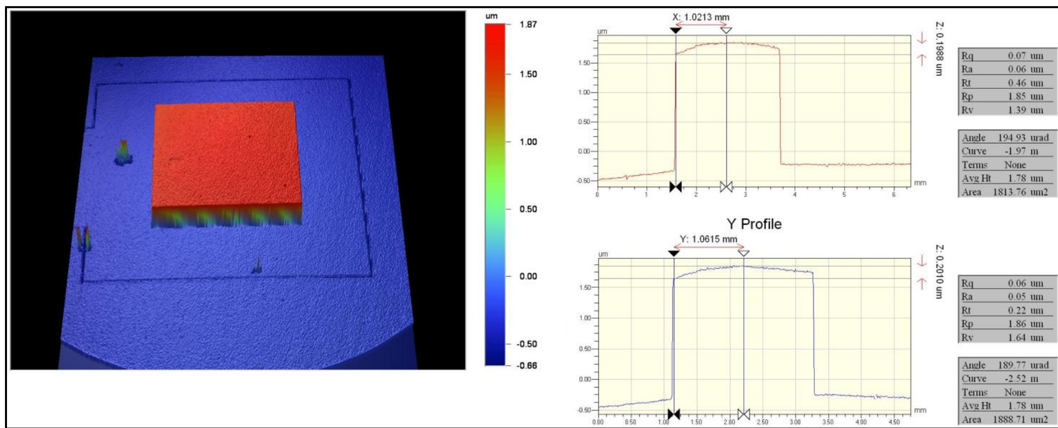


Figure 7.11: 3-D and 2-D scan of membrane with Bragg stack, single pixel chip, WE52

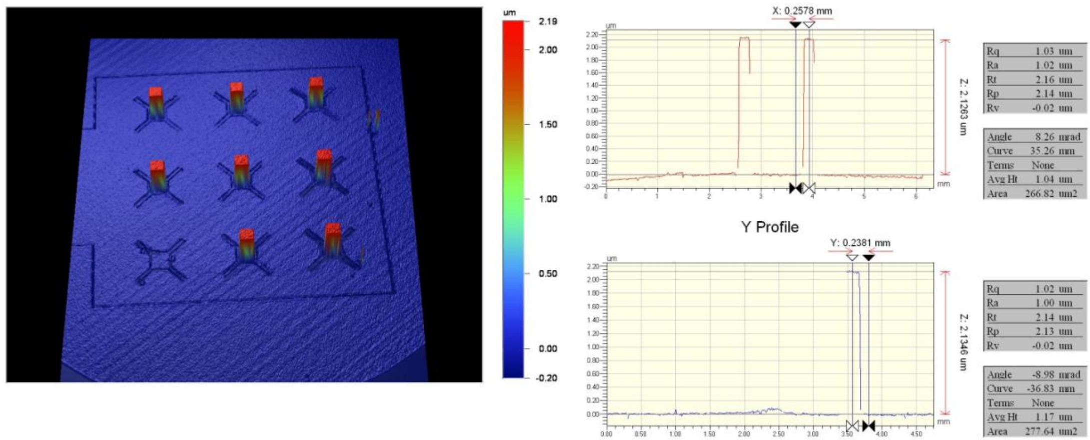


Figure 7.12: 3-D and 2-D scan of 9-array X-beams, WE53

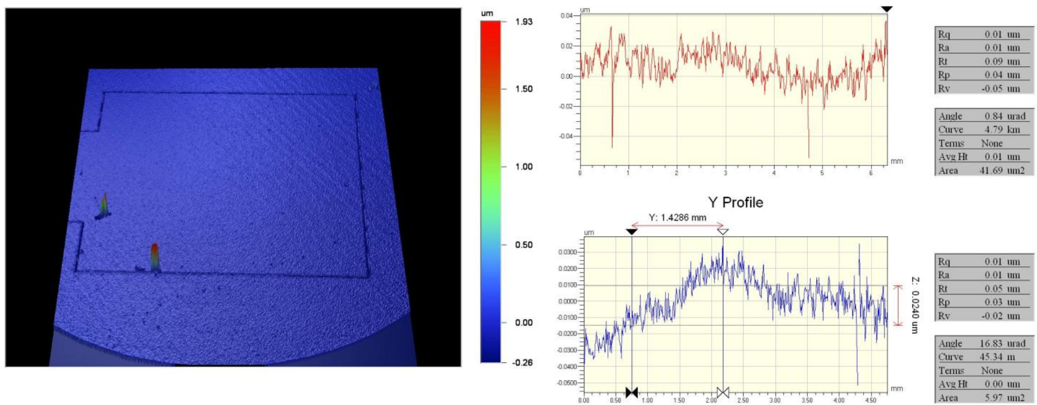


Figure 7.13: 3-D and 2-D scan of membrane without Bragg stack, single-pixel chip, WE53

Table 7.5: X-beam with Bragg

Component	Bragg height (µm)	F2X (µm)	CBS (µm)	F2T (µm)
WE52, X-beam, Bragg	2.0	1.03	0.47	3.53
WE53, X-beam, Bragg	2.0	0.54	0.18	2.76
WE54, X-beam, Bragg	2.0	0.25	0.095	2.36

It is evident that the bow is reduced with increased layer thickness. The best results were achieved on WE54; however, the improvement is most apparent between wafers WE52 and WE53. The bow in WE53 is sufficiently reduced such that it can be used for optical tests with minimal degradation of optical performance. The F2X parameter achieved under previous process conditions was as high as 5.46 µm; therefore, the new processing methods used to reduce the bow were extremely successful.

After the components were analyzed, the following tests were performed to ascertain the individual effect of each of the bow-reducing steps: the BOX compensation layer was removed from some X-beam components (indicated as -B), and the top silicon dioxide layer was removed to reduce the total stress in the Bragg stack (indicated as -F). The results are summarized in table 7.6 below.

Table 7.6: X-beam with Bragg, with post-processing

Component	Bragg height (µm)	F2X (µm)	CBS (µm)	F2T (µm)
WE52, X-beam, Bragg	2.0	1.03	0.47	3.53
WE52, X-beam, Bragg, -F	2.0	0.33	0.143	2.07
WE52, X-beam, Bragg, -B	2.0	1.03	0.388	3.47
WE53, X-beam, Bragg	2.0	0.54	0.18	2.76
WE53, X-beam, Bragg, -B	2.0	0.454	0.085	2.63
WE53, X-beam, Bragg, -F	2.0	0.134	0.034	2.36
WE54, X-beam, Bragg	2.0	0.25	0.095	2.36
WE54, X-beam, Bragg, -F	2.0	0.075	0.04	2.23
WE54, X-beam, Bragg, -B	2.0	0.235	0.11	2.27

As seen in table 7.7, removing the BOX compensation layer has almost no effect on the bow. This can be attributed to the much thicker device and handle layers than previously used, therefore the BOX stress is almost insignificant. Removing the top

silicon dioxide layer from the Bragg stack appears to reduce the bow slightly; however, the improved optical performance gained by having a 3 silicon dioxide layers (higher reflectivity) would have to be sacrificed to achieve the flatter mirror surface. The array devices exhibited almost insignificant bow. This may be attributed to the smaller membrane and X-beam areas, and also to the smaller Bragg stack areas in relation to larger device layer thicknesses.

7.10 Optical terms

Using the data from the surface analysis, and assuming the surfaces of the chips still maintain the reflectivity of 98%, the following can be concluded. The reflective finesse term is 155, and the defect finesse terms are as follows: finesse due to bowing is 6.99; finesse due to surface roughness is 42.5; effective finesse is dominated by the bowing term and is equal to 6.84. This results in FWHM= 0.58 μm at λ=4 μm. Again, as compared to the results from the second fabrication run, the finesse was improved by more than an order of magnitude, and the FWHM was reduced by more than an order of magnitude.

7.11 Chip Bonding

After chip analysis post-processing, bonding was performed with three pairs of components from each wafer. As mentioned in the previous report, chip bonding under prior conditions was problematic, because the excessive X-beam bowing (≈

6μm) necessitated extremely thick bonding layers to be used, so bonding materials were at least 12μm in some cases. This resulted in multiple layers of thick photoresist, with incomplete baking and re-flows after the bonding.

The new components exhibited minimal bowing, which permitted the use of single coats of photoresist of 7 μm and 10 μm thicknesses. Therefore the standard process was used:

1) the membrane component was spin-coated with 10μm of SPR 220-7 photoresist,

2) the chip was baked,

3) exposed to the mask,

4) developed, and

5) bonded with the X-beam component.

One issue encountered in this bonding cycle was the over-baking of the photoresist, since the process was developed for much thicker films; therefore, the bake used was too long, resulting in loss of adhesion. At least half of all bonded chips separated due to vibrations on the way to the mechanical testing lab.

Chapter 8 : Mechanical Actuation

8.1 Introduction

This chapter will describe the two methods of mechanical actuation for the Fabry-Perot interferometer made up of components fabricated in the third fabrication run. Two methods of actuation are described: electrostatic and magnetic.

Attempts at electrostatic actuation and the reasons why it failed will be described.

Alternative magnetic actuation is described, with the modifications needed to be done. The set-up for actuating the interferometer with a solenoid coil will be described, and data provided for actuation of MUMPS fabricated X-beam as well as SNF fabricated X-beam. The actuation results for both X-beams are compared to analytical model and finite-element model.

8.2 Electrostatic Actuation

As described in Chapter 4, in order to create a dynamically tunable Fabry-Perot interferometer, one of the reflecting plates has to be moved in relation to the other plate, and electrostatic actuation was chosen as the initial method. Two chips, an X-beam and a membrane chip fabricated during the third run at SNF, were bonded using photoresist, providing a parallel, isolating bond. In order to provide electrical connection to the components, wires were bonded to the gold contact pads of the X-beam chip using silver epoxy and baked at 60 ^{o}C, to cure the epoxy. Conductivity tests showed that the resistance from the wire to the device layer silicon was 147.7

Ohms, and showed perfect isolation to the bulk silicon. There is perfect isolation between the two bonded chips, satisfying the conditions for electrostatic actuation.

During the testing, a micro probe, connected to the positive voltage port of the power supply, was in contact with the gold pad of the membrane chip, and the ground wire was connected to the wire on the X-beam chip.

The test was performed under the white-light interferometer. The initial shape of the X-beam was recorded with 0 V applied, and subsequent scans were made with voltage increments of 10 V all the way up to the maximum voltage of 500 V.

The change in the deflection of the X-beam was negligible over the voltage range of 0-500 volts.

8.3 Analysis of electrostatic actuation

In order to understand the failure of the X-beam to actuate even for applied voltages as high as 500 V, mechanical analysis was re-done to account for the change in shapes of the X-beam, use of thicker device silicon layer, and changed separation of the two components.

Table 8.1 lists the mechanical spring constants for the X-beam components, starting with the MUMPS fabricated X-beam and ending with the X-beam fabricated on the 100 μm device silicon layer.

Table 8.1: The mechanical spring constants for the X-beam components

Run	Thickness, μm	Width, μm	Length, μm	k	k total	Vpi, V
MUMPS	25	250	2156	65.5	262	12.5
1st run	5	250	2156	0.523	2.1	3.3
2nd run	20	50	660	233.7	935	1469
3rd run, a	50	50	660	3652	14609	22957
3rd run, b	75	50	660	12326	49305	77479
3rd run, c	100	50	660	29217	116871	183654

According to the scaling law of the beams, the spring constant increases as cube of the increase in thickness. Therefore, increasing the silicon thickness from 5 μm to 50 μm, the mechanical constant increased by a factor of 1000, and for 100 μm silicon layer, by a factor of 4000. Also, the decrease in the length of the X-beam springs increased the spring constant.

The original actuation voltage was calculated for the 1-st order Fabry-Perot interferometer, with the starting distance between the plates as 2.5 μm. After scanning the bonded pair of the chips, it was determined that the separation between them was 158 μm. This increase in gap, according to equation 3.1, also increases the actuation voltage by a factor of 63.

The conclusion is that even with the chips bonded with the minimal distance, the voltage required to actuate the devices was prohibitively high. Such high voltage would cause the breakdown of the devices and would put too much charge on the optical layers.

Changes to the design done during the three iterations of fabrication were aimed at increasing the optical quality of the mirrors. The needed changes, such as increasing the thickness of layers, decreasing the area of the plates, and shortening the springs, negatively affected the mechanical properties of the devices, requiring actuation forces much higher than those afforded by electrostatic actuation.

8.4 Magnetic Actuation

Modifications done to the devices to improve their optical characteristics made electrostatic actuation impossible due to the low forces provided by that type of actuation. Another method of actuation had to be found that provides high actuation forces and does not require significant modifications to the fabricated chips. Magnetic actuation, another method used in MEMS, is a good alternative: it provides significantly higher force than electrostatic actuation, does not have a pull-in limit, and does not require electrical separation between two parts of the FPI. The disadvantages include high power for actuation and the need for two discrete elements, the permanent magnet on the X-beam and a solenoid coil. The chips already fabricated can be used for either electrostatic or magnetic actuation.

Magnetic actuation is a widely used method in MEMS devices, but there has not been a single use of magnetic actuation for Fabry-Perot interferometers in the MWIR range.

In order to perform the magnetic actuation, either a solenoid coil or a permanent magnet had to be attached to the X-beam component, on the side without the Bragg reflector coatings. Due to the small area of the X-beam, it would be extremely difficult to attach a solenoid coil. However, there are various sizes of permanent magnets on the market. The magnet had to be significantly smaller than the area of the X-beam, so as not to cover the optical area entirely.

Three sets of permanent magnets were purchased from two vendors. One set of magnets, D1, were disks of 1.5 mm diameter and 0.5 mm in height. Second set were ring magnets, R1, with magnetization though the thickness, 1 mm in outside diameter, 0.5 mm inside diameter, and 1.5 mm tall. Third set, R2, were ring magnets with 1 mm outside diameter, 0.5 inside diameter, and 0.5 mm tall.

Table 8.2 shows the magnetic field at the surface of each set.

Table 8.2: Magnetic field on the surface of three magnets

Magnet	D1	R1	R2
Magnetic field, Gauss	27	7.5	4.3

To attach the magnets, a drop of super glue was used. In order to decrease spreading of glue that might get in between the springs and hinder actuation, the drop size was reduced by dipping a thin wire in a drop of glue, touching it twice to a glass slide, and

finally touching it on the back surface of the X-beam. The magnets were positioned on the drop of glue and were cured for 24 hours at room temperature to solidify the bond.

During the placement of the magnets, low precision afforded by hand-placement has resulted in several magnets being stuck off the X-beam, or, in some cases, the glue was pushed between the spring and substrate, making the X-beam unusable. The yield rate of this process was less than 20%. Two of the successful X-beams, one fabricated in MUMPS process and one from WE42 wafer, are shown in figures below. The magnet on the MUMPS X-beam is from the R2 set, and magnet on the SNF X-beam is of the R1 set.

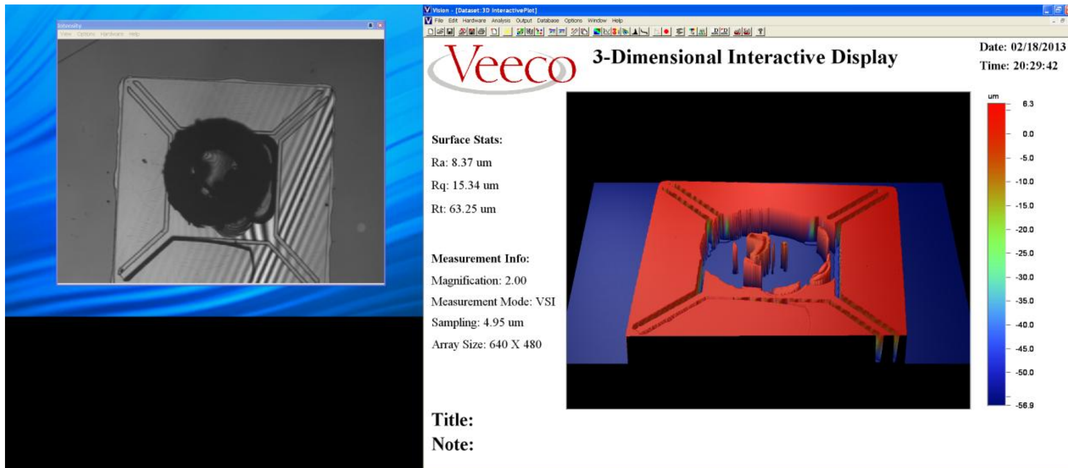


Figure 8.1: Surface scan of WE42 X-beam with R2 magnet and glue residue

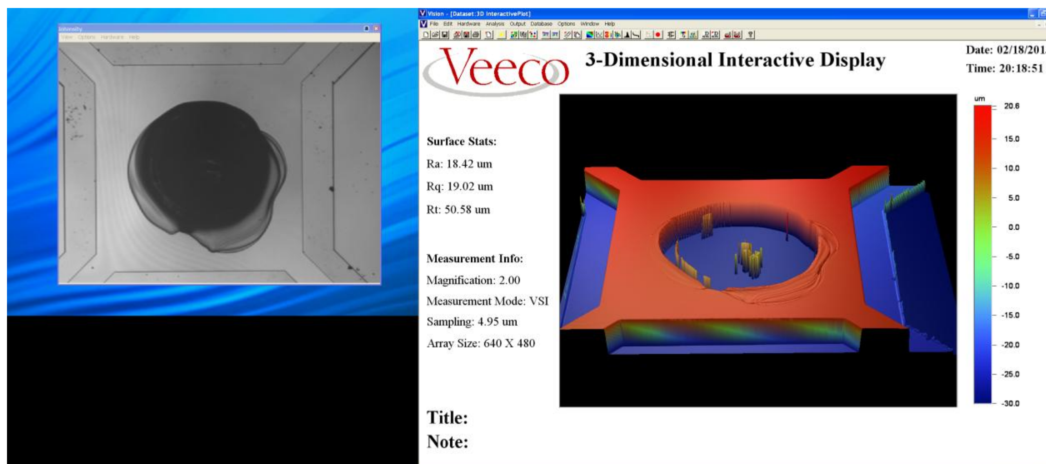


Figure 8.2: Surface scan of MUMPS X-beam with R1 magnet and glue residue

To make the initial solenoid coil, enamel-coated magnet wire, 30 gauge, was tightly wound on a plastic sewing spool. After testing, it was found that the wire generates enough heat to soften the spool and cause deformation. Materials traditionally used for making the solenoid coil shaft, such as weakly magnetic materials, could not be used for this set-up. In order to perform mechanical and optical testing, the X-beam with permanent magnet had to be placed in the center of the coil. The strength of permanent magnet attraction to the material of the shaft is very high compared to the strength of X-beam springs, so the coil had to be made of non-magnetic material. The final solenoid coil was made of Teflon, which is relatively heat-resistant and does not provide attraction for the permanent magnet.

With the coil of 400 turns and 2 cm high, the coil was characterized by placing the magnetic probe immediately on the shaft and measuring the magnetic field as a

function of current. This data, shown in figure 8.3, is the electromagnetic characterization of the solenoid coil used for experiments.

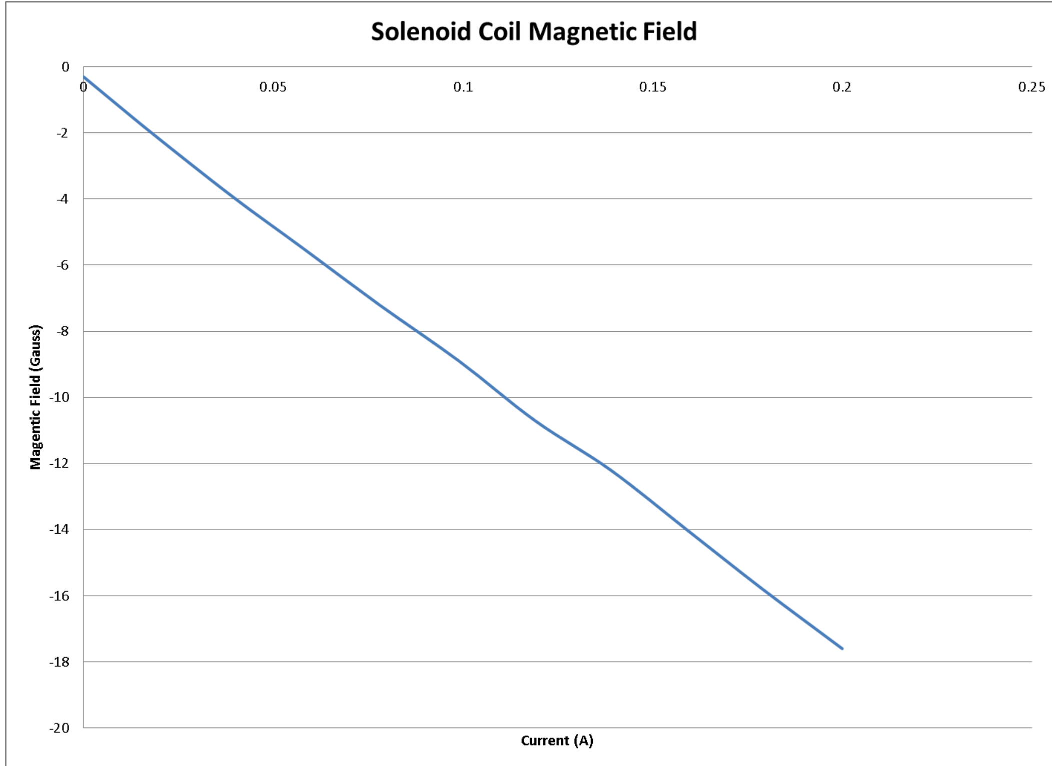


Figure 8.3: Magnetic Field of Solenoid Coil. The negative sign of the field indicates that with the polarity of the wires at the time of testing, the field direction is into the solenoid.

8.5 Magnetic actuation results

Knowing the exact deflection of the X-beam actuated by the solenoid provides data on the dynamic behavior of the Fabry-Perot interferometer. Using the solenoid coil connected to a power supply, mechanical testing was performed on MUMS X-beam with a disk magnet (D1) glued to the back. Testing was performed under the white-light interferometer, and the deflection of the center of the X-beam was recorded for

each step in current. The experimental data for the deflection, with deflection of the chip with no current taken as 0 μm, is shown in figure 8.4.

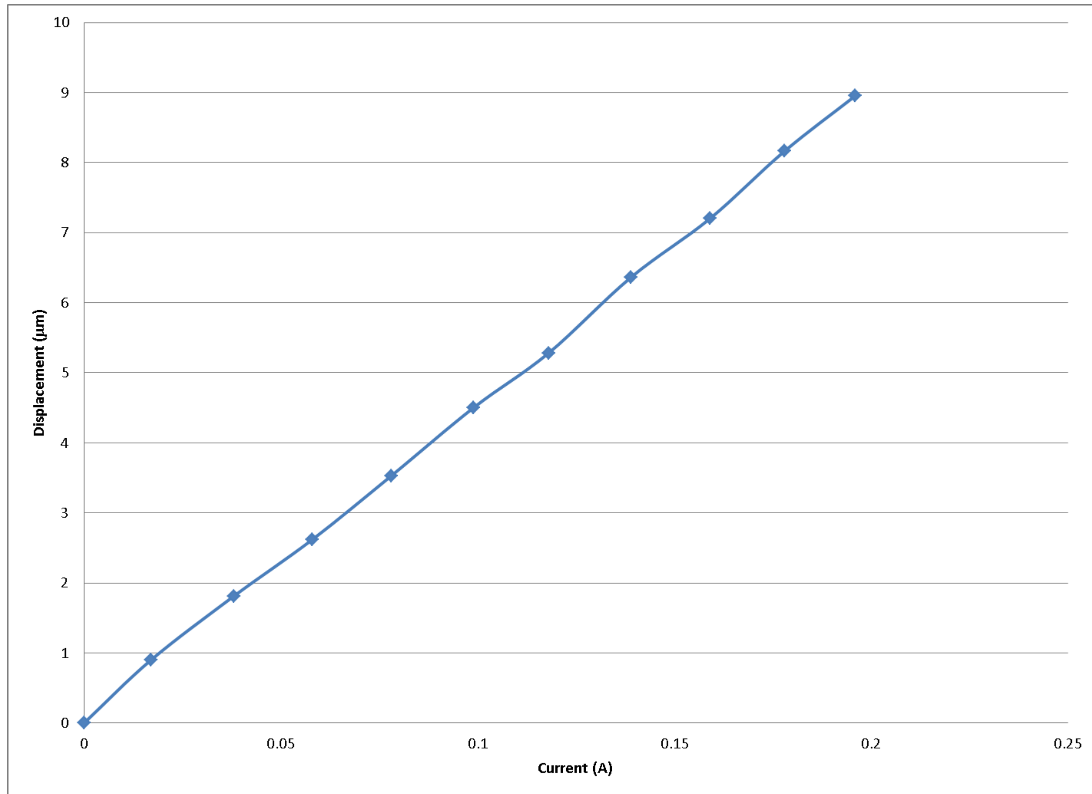


Figure 8.4: Deflection of MUMPS X-beam with D1 magnet

The deflection is linear, as expected from the Gilbert model and Hooke's law. As the disk magnet covered too much of the optical area, another chip, MUMPS X-beam with R1 magnet attached to it, was made. The deflection of this chip using the solenoid coil, and comparison to the analytical Gilbert model and finite element simulations, is shown in Fig. 8.5.

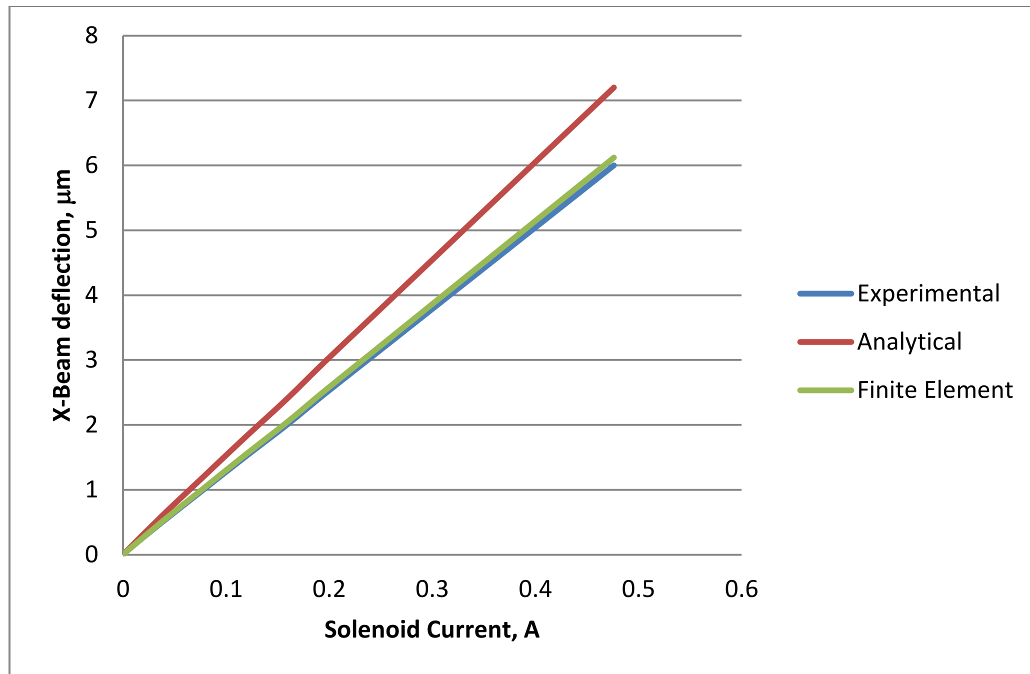


Figure 8.5: Deflection of MUMPS X-beam with R1 magnet

The experimental data is in good agreement with the finite element analysis performed using IntelliSuite software with magnetic force input from analytical calculations, but the analytical model predicts higher deflection for given solenoid current.

The MUMPS X-beam is a good mechanical prototype, but in order to do optical testing and get optical behavior that is close to the ideal Fabry-Perot interferometer with highly reflective surfaces, an X-beam with Bragg stack was used. Several samples were prepared, and the best sample was from the WE42 wafer, with 50 µm silicon device layer. This chip had a D2 magnet attached to it. Using the coil, it was actuated under the interferometer and the change in height at the center of the chip was used as measure of the deflection. Experimental data are shown Fig. 8.6. The

three dots on the graph show the deformation using the permanent magnets, discussed in Section 8.7.

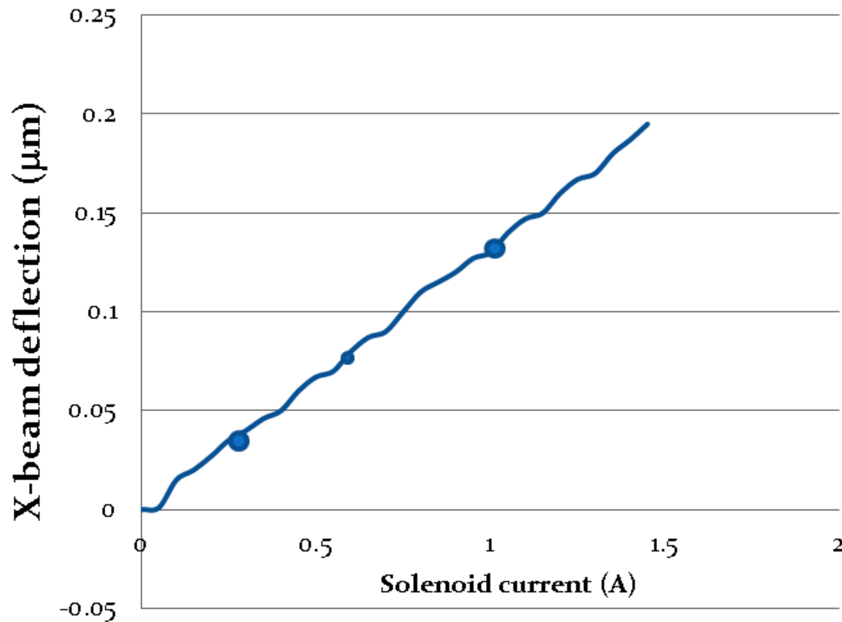


Figure 8.6: Deflection of WE42 X-beam with R2 magnet

Due to stiffness of the springs, the maximum deflection was 0.2 µm, much less than the 1 mm deflection required to scan the 3-5 mm range. Nonetheless, this range of actuation is sufficient to verify the change in optical filtering of the device. With the Bragg reflectors designed for 3-5 µm range, this change in deflection should provide tuning over 0.4 µm range.

8.6 Modifications to devices needed for magnetic actuation

Mechanical characterization of the devices had to be consistent for future optical testing. The placement of the chips and actuation results had to be precise over

several trials. While performing magnetic actuation trials, the polarity of the coil had to be correct in order to pull the X-beam down towards the solenoid coil. If the polarity was reversed, the data was not consistent. This happed due to the low mass of the chip compared to the force generated by the magnet actuation. The chip would rather lift up than bend the springs. This seemed very inconvenient, and for further testing, the following modification was made: a large aluminum washer, with inside diameter large enough to accommodate the movement of the X-beam and the light passing though, was placed on top of the chip. Therefore, the chip was stable between the solenoid coil and the aluminum washer.

8.7 Using permanent ring magnets

Since the solenoid actuation was too weak, a selection of permanent magnets were used to demonstrate the device. These parts will be used for optical testing, and the set-up at Naval Post-Graduate School, where the optical testing was conducted, did not allow for high-power currents to actuate the solenoid coil. In order to make the apparatus effective, instead of the solenoid coil five permanent magnet rings were used to quantify the actuation instead of a solenoid magnet. The strength of each magnet and combinations of two and three magnets were tested to correlate the magnetic field to the current used in solenoid coil.

For the single magnet used, the magnetic field was 26 Gauss, for two magnets, it was 52 Gauss, and for three, it was 88.6 Gauss. These magnetic fields and their correspondence to coil currents are listed in Table 8.3.

Table 8.3: Permanent Ring Magnets B-Field and corresponding solenoid current

Permanent magnets	B-field (Gauss)	Corresponding current (A)
1M	26	0.30
2M	52	0.595
3M	88.6	1.033

Deflections in the WE42 X-beam component using the permanent magnets are shown in Fig. 8.6. The data shows good agreement between analytical model and experimental results.

Chapter 9 : Optical Testing

9.1 Introduction

This chapter will describe the optical testing of devices fabricated in previous chapters. The optical set-up and calibration will be described, followed by comparison to computer simulations of experimental data obtained from several components as well as two types of Fabry-Perot interferometers.

The optical testing of these devices was performed at the Naval Postgraduate School, Monterey, CA. The MEMS lab at NPS is equipped with a Fourier transform infrared spectrometer (FTIR), ThermoScientific Nicolet 6700, and optics needed for performing these tests.

9.2 Optical setup

The key components of the optical set-up shown in Figure 9.1 are, in order of importance, the FTIR spectrometer, the hot plate with the black body source, and the aluminum plate. Typically, the spectroscopy using FTIR is done on small and flat samples. The FTIR is equipped with internal source and robotic stage that allows loading and unloading of samples. As the complexity of the optical set-up needed to test the magnetically actuated devices requires at least 5 cm of clearance between the source and the sample, it was not possible to use the internal source of the FTIR with the robotic stage. This means that the increased signal to noise obtained by the phase-lock capability of the internal source was lost, but tests could be done with an external body source. The set-up finally used was originally developed by the NPS MEMS

group for optical testing in the THz regime. The experimental set-up at NPS is shown in Fig. 9.1.

Figure 9.1: NPS FTIR

In order to test the optical properties of the FPI devices and elements, we need the following key components: a black body source to provide wide-spectrum radiation, an aluminum plate, and a parabolic mirror. Details of these components, previously shown as part of the complete system in Figure 9.1, are shown in Figure 9.2. the required radiation source was obtained by heating a piece of silicon wafer or a microscope glass slide, blackened over a candle to produce a thick and continuous film of carbon soot on the surface, to 250 degrees C. To minimize the emissions from the hot plate and the sample, an aluminum plate, 2.5 mm thick, with an aperture of 1 cm in diameter, was placed above the black body. The aluminum plate was chilled to

-5 degrees C for 30 minutes prior to each sample collection. In order to collect and focus the transmitted radiation from the sample onto the external port of the FTIR, a gold-coated parabolic mirror was used.

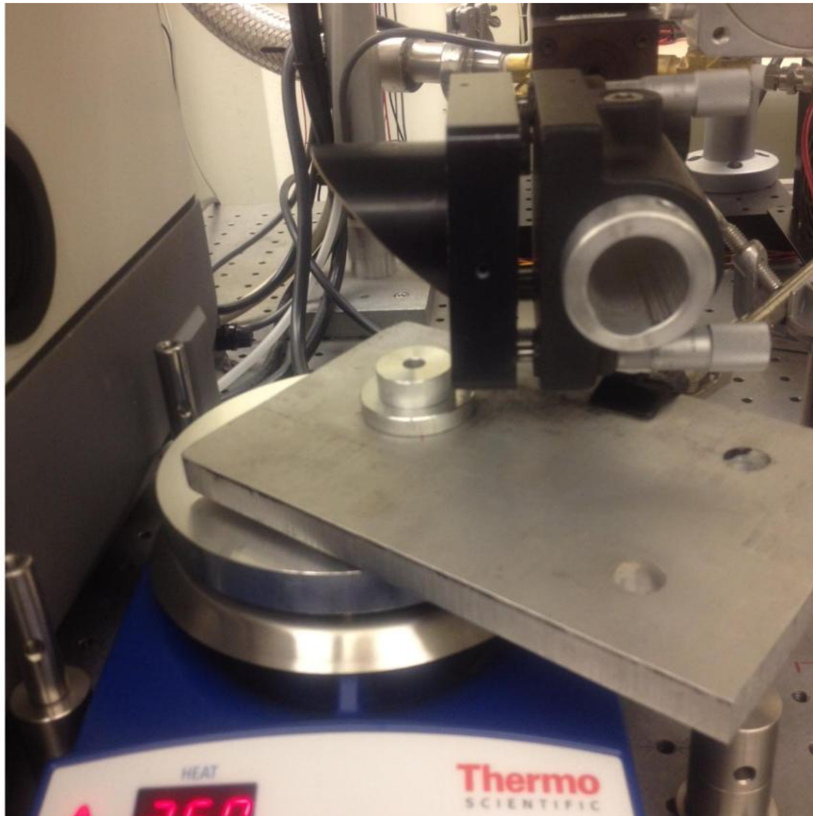


Figure 9.2: NPS FTIR: hot plate and mirror

9.3 Calibration of the FTIR optical set-up

In order to analyze optical test data from the FTIR, the optical set-up needs to be calibrated to account for radiation absorption by the environment and the instrument optics. This calibration is done by collecting background, or the absolute reading of the detector when scanned across the entire spectrum (2.5 μm -25 μm). This

information contains all the optical errors of the system, as well as noise. The background radiation collected using the chilled aluminum plate is shown in Fig. 9.3.

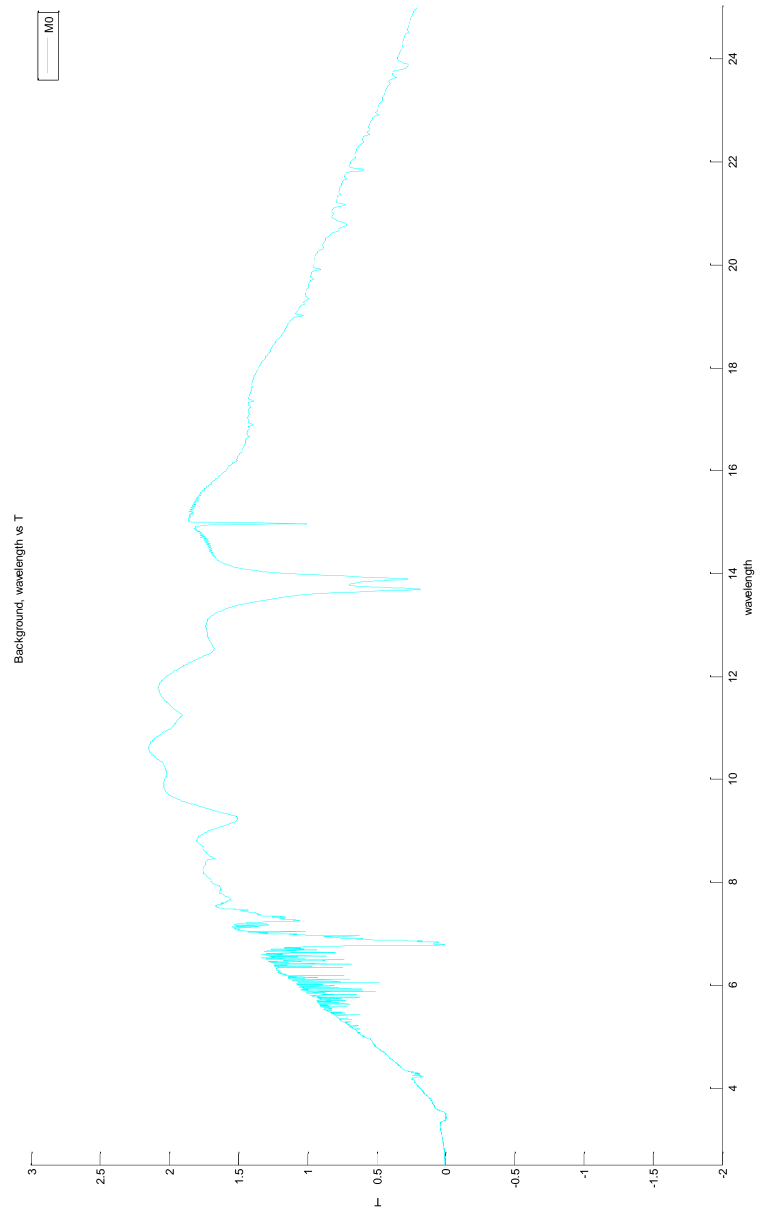


Figure 9.3: Background radiation for FTIR

As can be seen from the graph above, the background has several dips in the region of absorption of the optics and the atmosphere. To characterize the transmission signal through samples, each reading of the absolute value given by detector has to be divided by the background signal to get the percent of radiation transmission, I_t.

As an initial check, it is useful to record the transmission signal without any sample in the aperture. This is essentially a second recording of the background signal, and should be taken immediately after the first background reading. From this data, we need to determine the wavelength range for which the aperture transmission is unity. The data of aperture calibration is shown in figure 9.4.

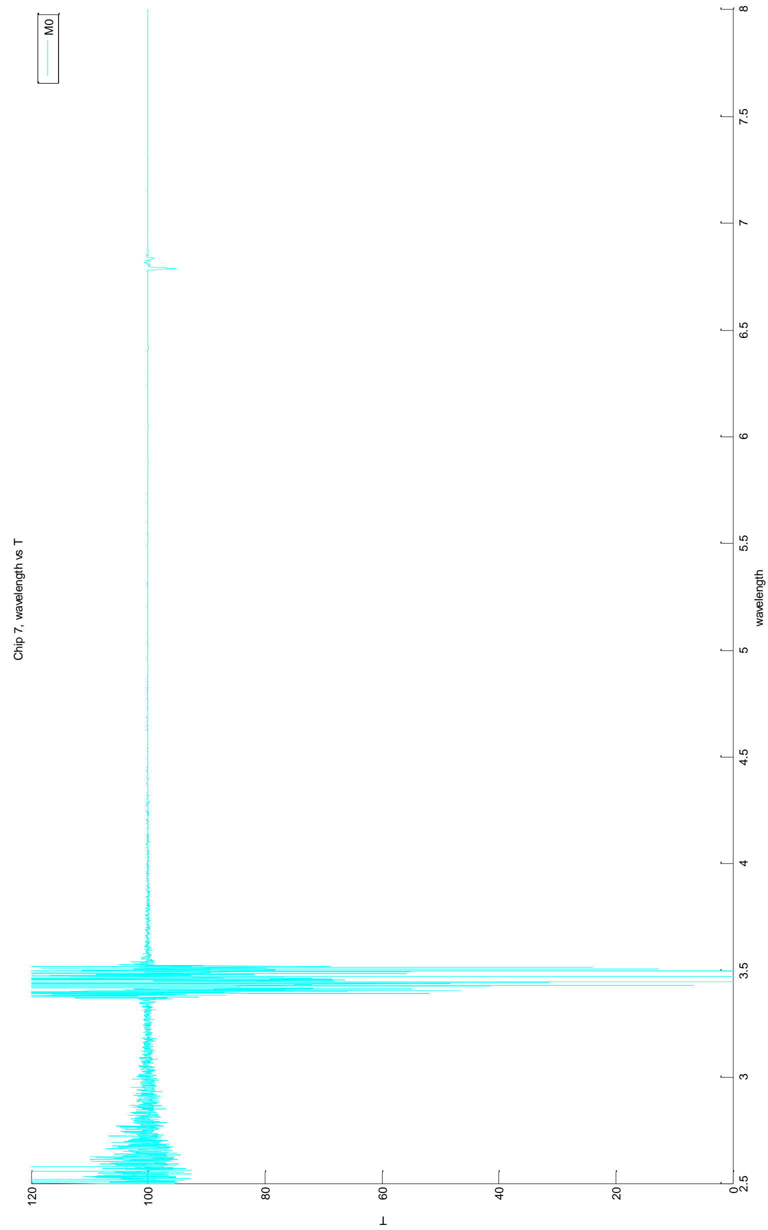


Figure 9.4: Aperture transmission calibration

As can be seen from Figure 9.4, the noise floor between 3.6 to 6.6 μm wavelength is averaged to zero, with maximum value of 0.5 percent transmission. The data in the region below 3.6 μm shows a high level of noise, as does the region between 6.6 and 6.8 μm. The noise in these regions is attributed to atmospheric absorption by water vapor and carbon dioxide. These regions will be discarded from the optical data.

9.4 Optical testing results for MUMPS X-beam (MX)

As a test of the set-up and consequently the optical simulator, transmission experiments through the MUMPS X-beam (see Chapter 8) with a magnet on it were done. The results, with data and simulation, are shown in Fig. 9.5.

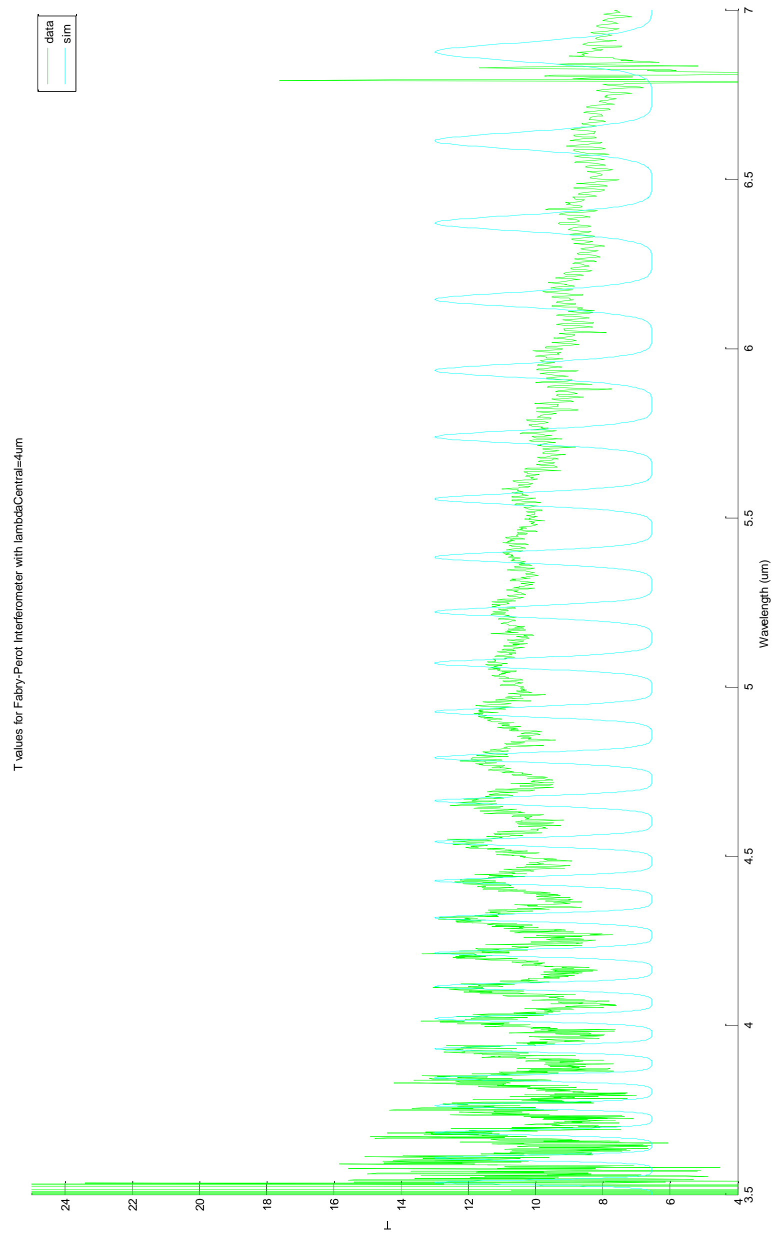


Figure 9.5: Transmission through MUMPS X-beam with magnet

In the region where noise level is low, it can be seen that the simulation accurately predicts the spacing of the peaks of transmission. It should be noted that the highest transmission value in the region of interest between 3.6 and 6.6 μm is 14%, owing to absorption of the material and greatly reduced area through which the light can pass through (compared to 1 cm diameter aperture taken as 100% transmission). For testing of Fabry-Perot interferometers made up of two such chips the maximum transmission peaks are expected to be even lower.

Two samples were tested with magnetic actuation: the first consisted of the MUMPS Xbeam, of 25 μm thickness, placed against a membrane with a Bragg coating; the second sample was of SNF Xbeam with Bragg reflector, from wafer WE42, placed against membrane with Bragg coating, also from WE42 wafer.

Through several attempts to achieve the closest and most consistent placement of the two parts, as was mentioned in the mechanical testing section, it was determined that the smallest gap and the most uniform distance was achieved by placing the X-beam chip on an aluminum washer with magnet centered in the hole, placing the membrane chip on top to align the optical windows, and placing the second aluminum washer on top, also optically aligned. As was mentioned in the mechanical testing section, the separation for the first sample was consistently 18.7 μm between the optical surfaces, and 4.8 μm for the second sample.

The high current required to actuate the X-beam made it impossible to use the solenoid coil for the optical testing. Instead, the five permanent ring magnets were used, as described in the mechanical actuation section.

9.5 Optical Testing Results for Static FPI

The previous section showed experimental optical testing results and correlation to the computer simulation for the simple element consisting of a single silicon membrane. To further correlate the optical model to the experimental optical results, a complete Fabry-Perot interferometer was tested. This device was made up of two membranes with Bragg reflectors fabricated during the third fabrication run. The membranes were held together between the two aluminum washers. No magnets were attached to either membrane, thus the optical area was greater than that for dynamic devices discussed later. The optical results for transmission measurements of this device are shown in Fig. 9.6.

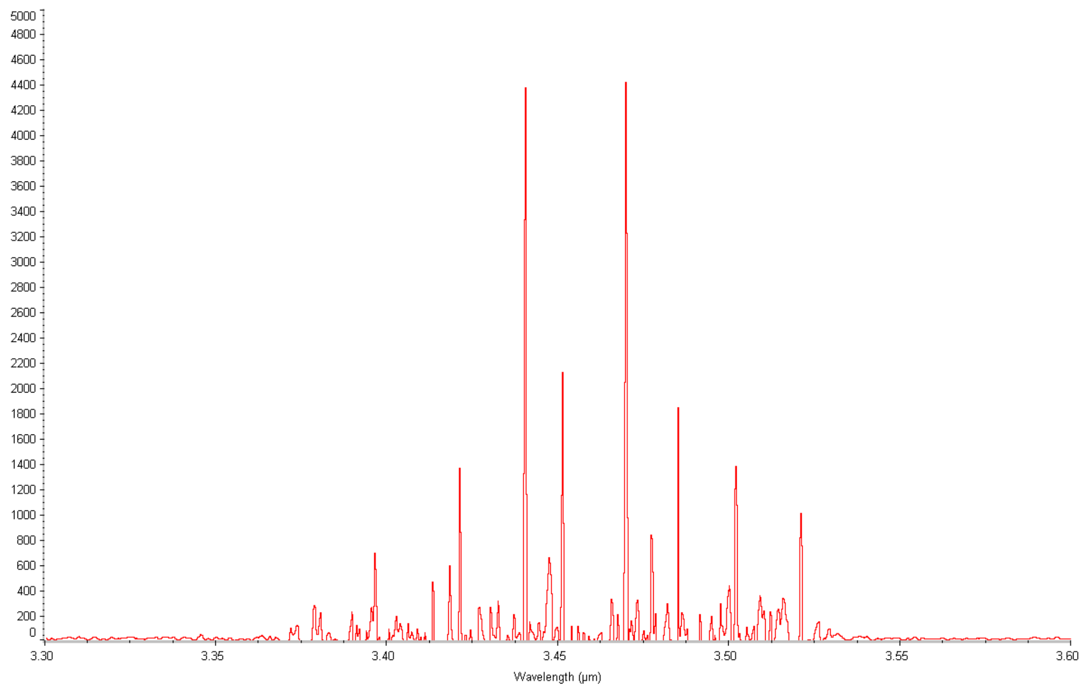


Figure 9.6 Transmission through static FPI over a 300 nm range centered on 3.45 µm

The experimental transmission result shows a typical Fabry-Perot transmission shape, with sharp spikes creating an envelope of transmission. The experimental bandwidth of this device is 168 nm. From theory and optical simulations developed in Chapter 2, the theoretical bandwidth of a perfect device should be 50 nm. The bandwidth of the device is broadened according to the defect theory described in Chapter 2. Considering the surface roughness and bowing of the membrane, shown in Chapter 7, calculations for the defect finesse terms are possible. Although the bowing term still dominates the finesse, the effective finesse is calculated as 24.6, giving FWHM as 162 nm. This experiment shows very good correlation of the bandwidth predicted by theory to the experimental data of Fig. 9.6.

9.6 Optical Testing Results for Asymmetrical FPI

In order to further confirm the optical model of the Fabry-Perot interferometer the asymmetrical device was tested. We note that this exercise is a test only – this device Iis not usable as a filter due to low finesse. The asymmetrical Fabry-Perot interferometer is made by placing together MUMPS X-beam and a Bragg coated membrane (MX-B device). To actuate the device, it was tested with no magnets (Fig. 9.7), one magnet (Fig. 9.8), two magnets (Fig. 9.9), and three magnets (Fig. 9.10). Figure 9.11 shows combined simulations, and figure 9.12 shows combined experimental data.

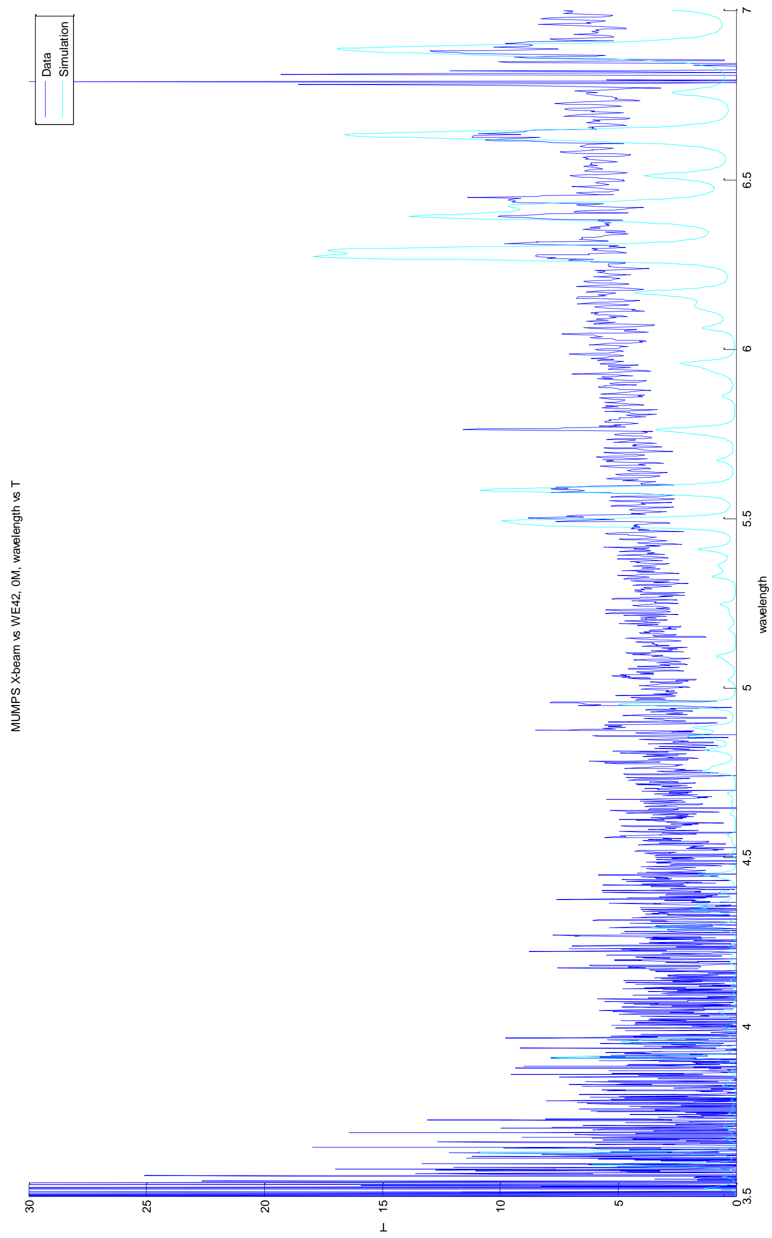


Figure 9.7: Transmission, MX-B device with no magnets

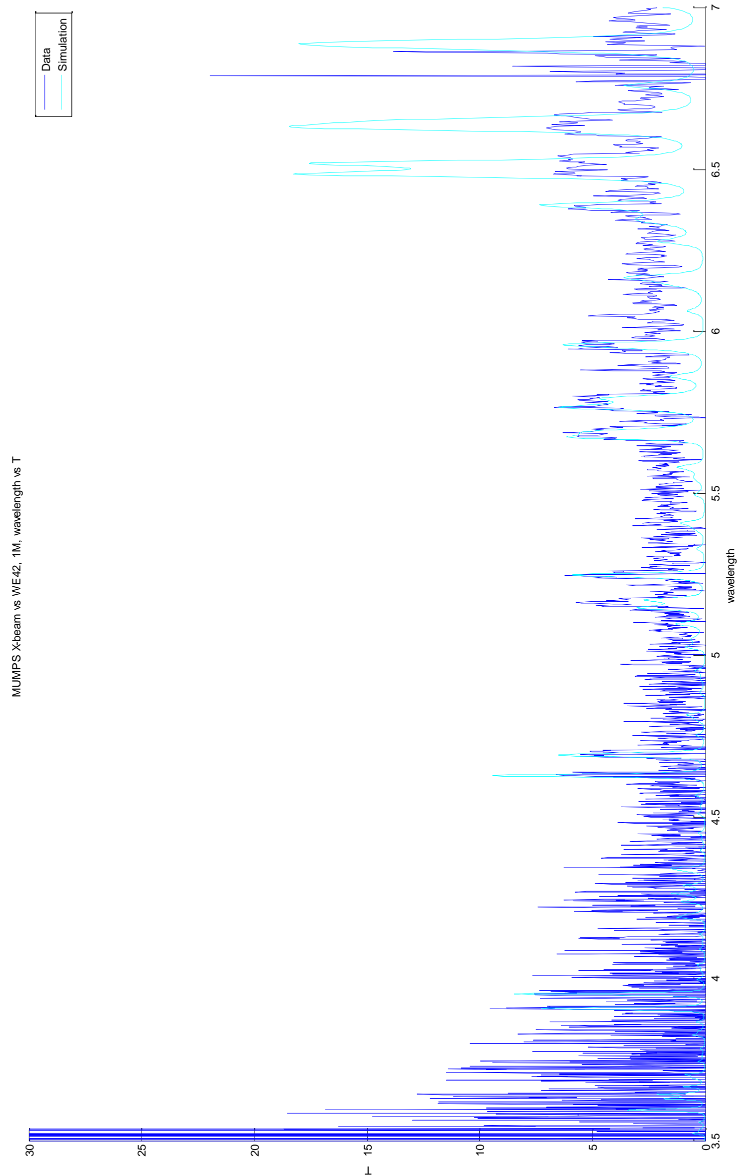


Figure 9.8: Transmission, MX-B device with one magnet (26 Gauss)

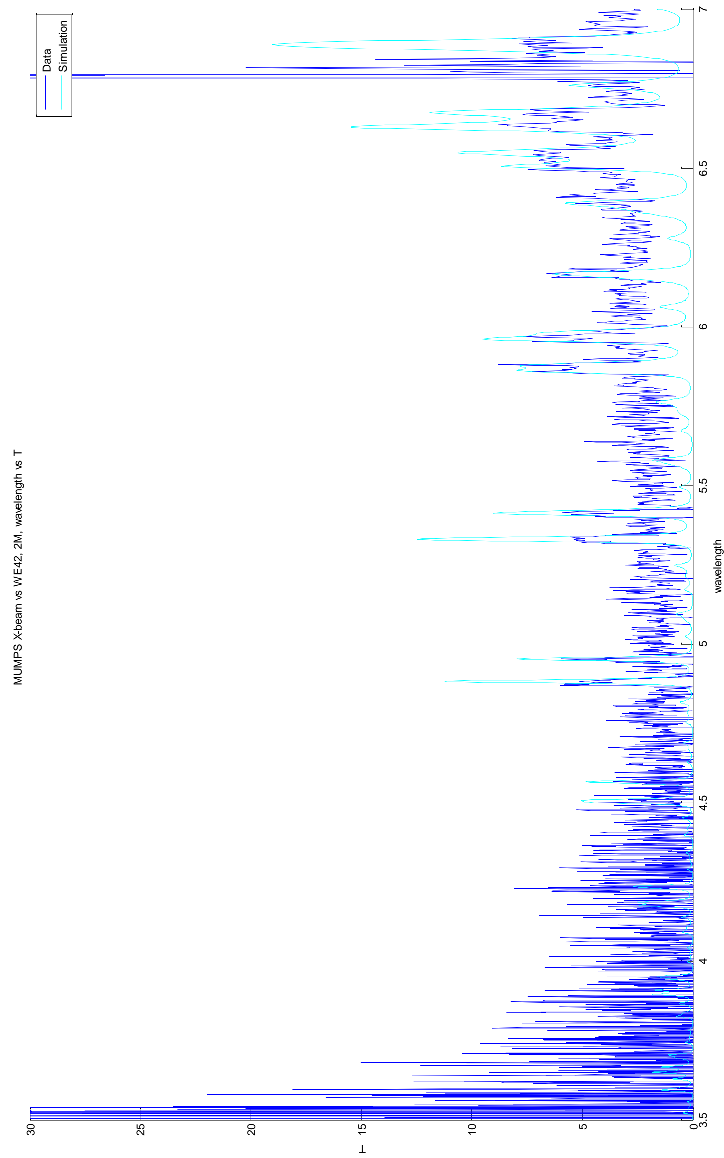


Figure 9.9: Transmission, MX-B device with 2 magnets (52 Gauss)

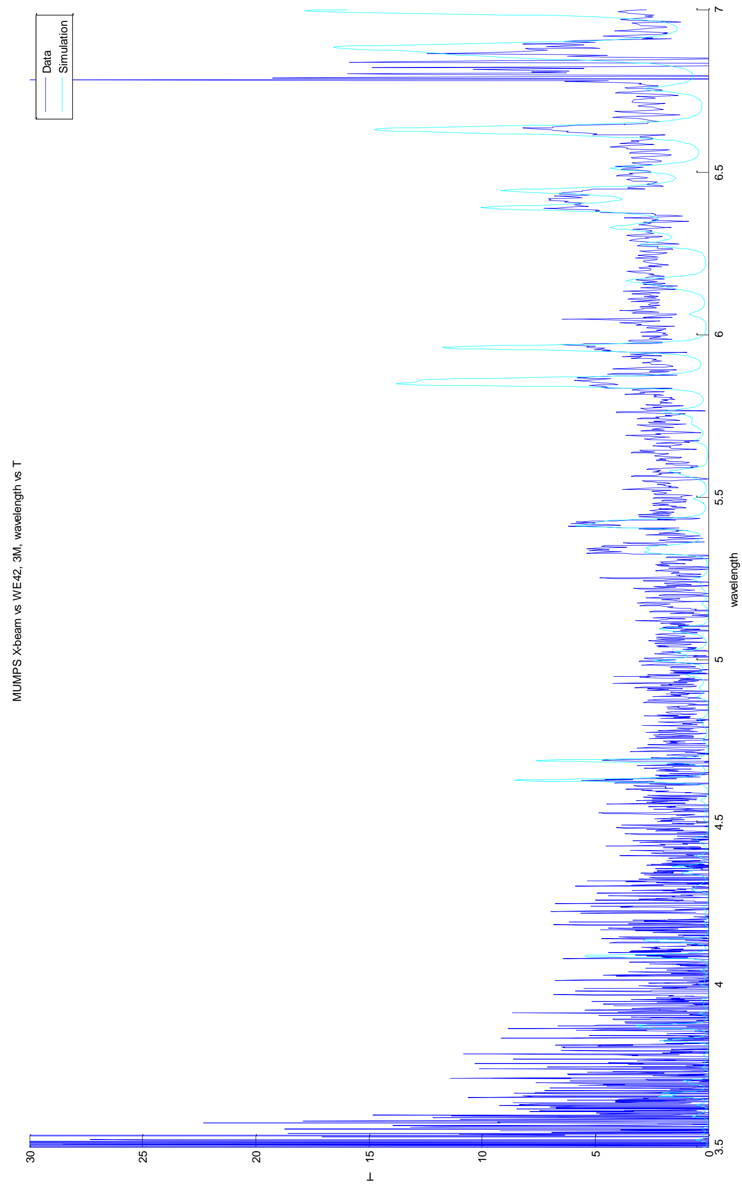


Figure 9.10: Transmission, MX-B device, 3 magnets (88.6 Gauss)

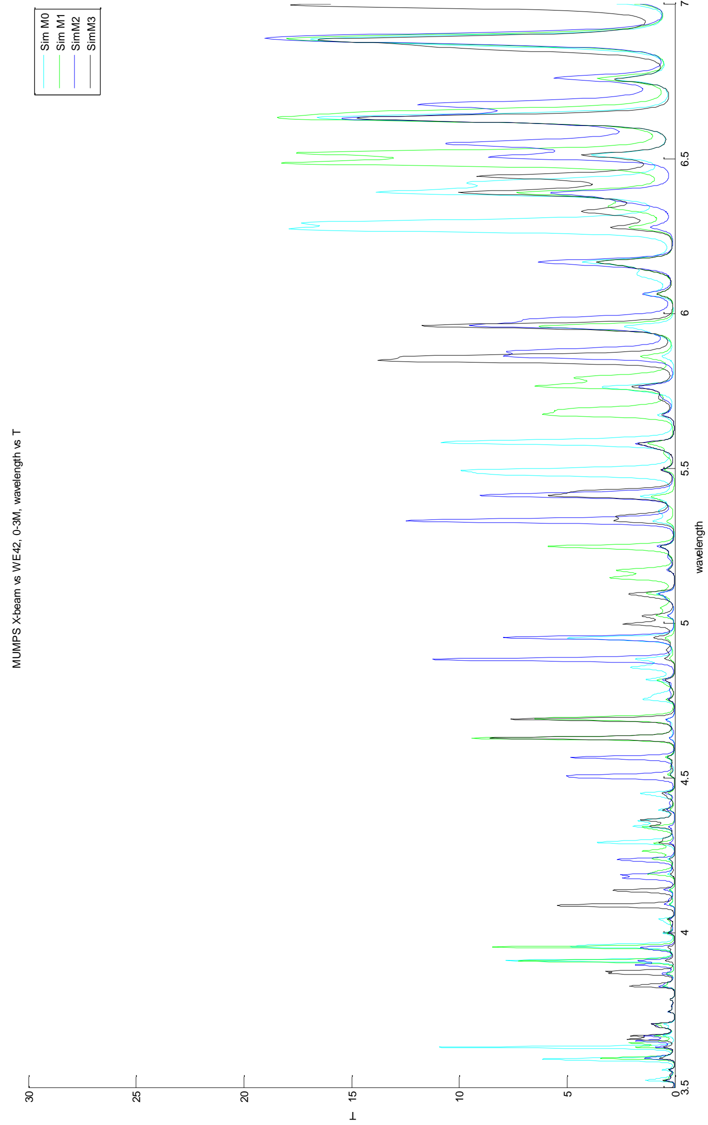


Figure 9.11: Transmission simulation, MX-B device, for 0, 1, 2 and 3 magnets, showing tuning of device

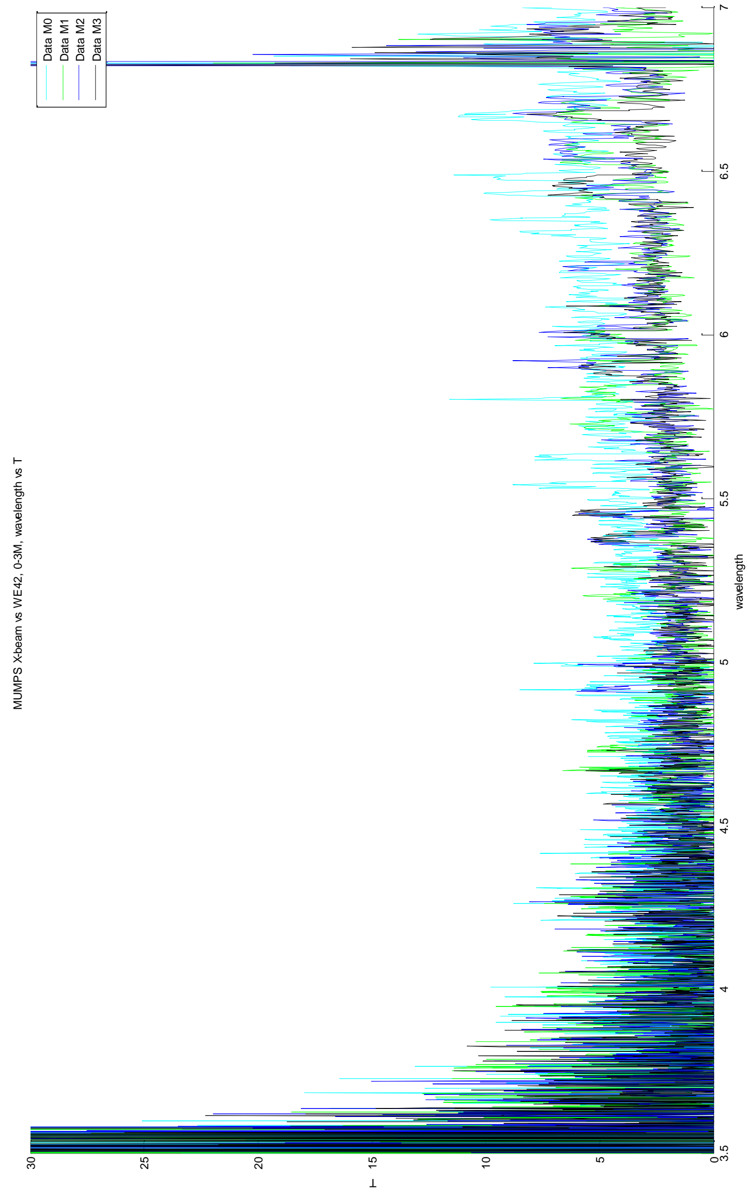


Figure 9.12: Transmission, MX-B device, experimental data for 0, 1, 2, and 3 magnets

As can be seen from the comparison of the data to computer simulations, the majority of the peaks correspond to the simulation results. The deformation of the X-beam was sufficient to show changes in the filtering behavior of the asymmetrical device. The finesse of the asymmetrical FPI is calculated to be 0.18, corresponding to FWHM of 22 μm. The finesse term is dominated by the bowing term in the X-beam component, and makes the device unusable as a filter.

9.7 Optical Results for SNF-fabricated chips (SX-B)

The results in Chapter 7 show that the Fabry-Perot interferometer made up of the pair of chips fabricated during the third fabrication run would serve as a good optical filter. The finesse calculations show that the bandwidth of this filter would be 0.5 μm. Chapter 8 details the experimental results for the dynamic deflections of the SNF fabricated X-beam. To confirm the optical filtering that changes with the mechanical deflection of the X-beam, a series of tests were performed using the optical set-up described above and that utilizes the same permanent magnets as in the asymmetrical device described above. Figure 9.13 shows experimental optical results for transmission through the SNF fabricated X-beam placed opposite SNF fabricated membrane (no magnets), and compares it to computer simulations. Figure 9.14 shows the transmission through the same device actuated with one magnet, and Figures 9.15 and 9.16 shows transmission data though the device actuated with two and three magnets, respectively. Figure 9.17 shows the change in the transmission that is predicted by combining the optical simulations with the experimental

mechanical actuation data described in Chapter 8, and Figure 9.18 shows the combined experimental optical data for the four positions of the device. In considering Figs. 9.13-9.18, note how the change in the magnetic field (due to number of permanent magnets, Table 8.3) changes the spectral response such that the peak response is at longer wavelength at higher magnetic field intensity (larger magnetic actuation) – thus, demonstrating the optical tuning of the spectrometer.

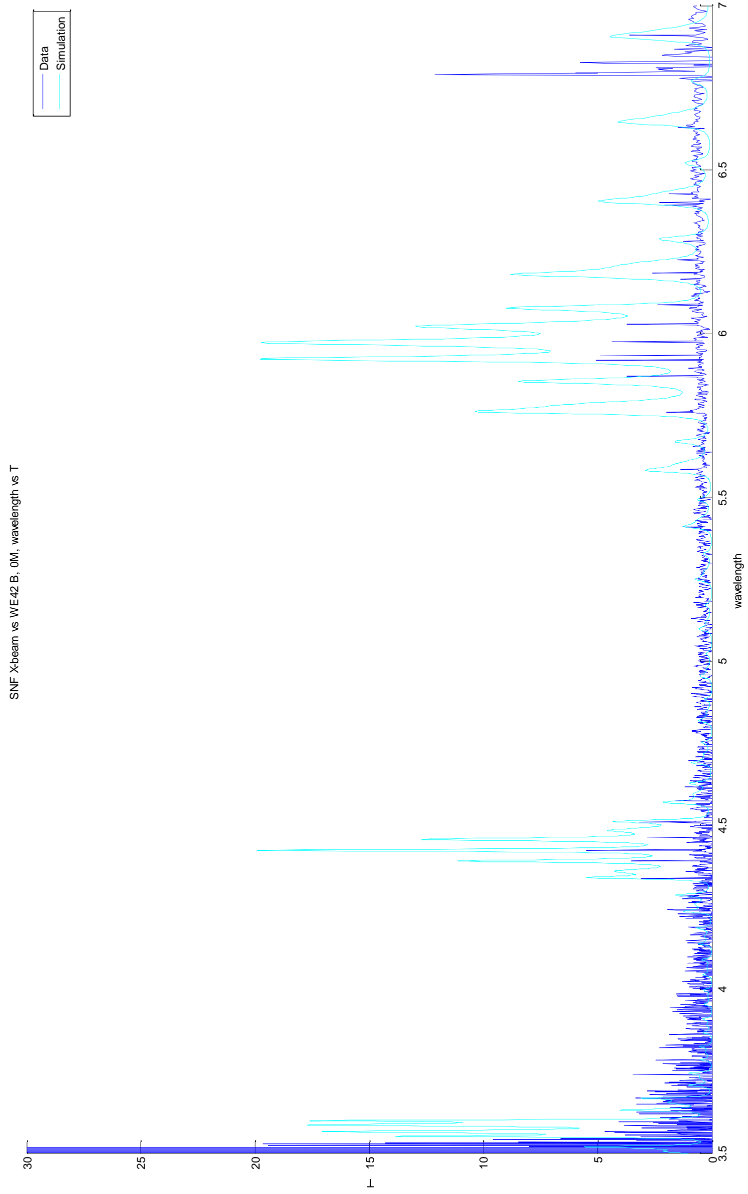


Figure 9.13: Transmission, SX-B device with no magnets

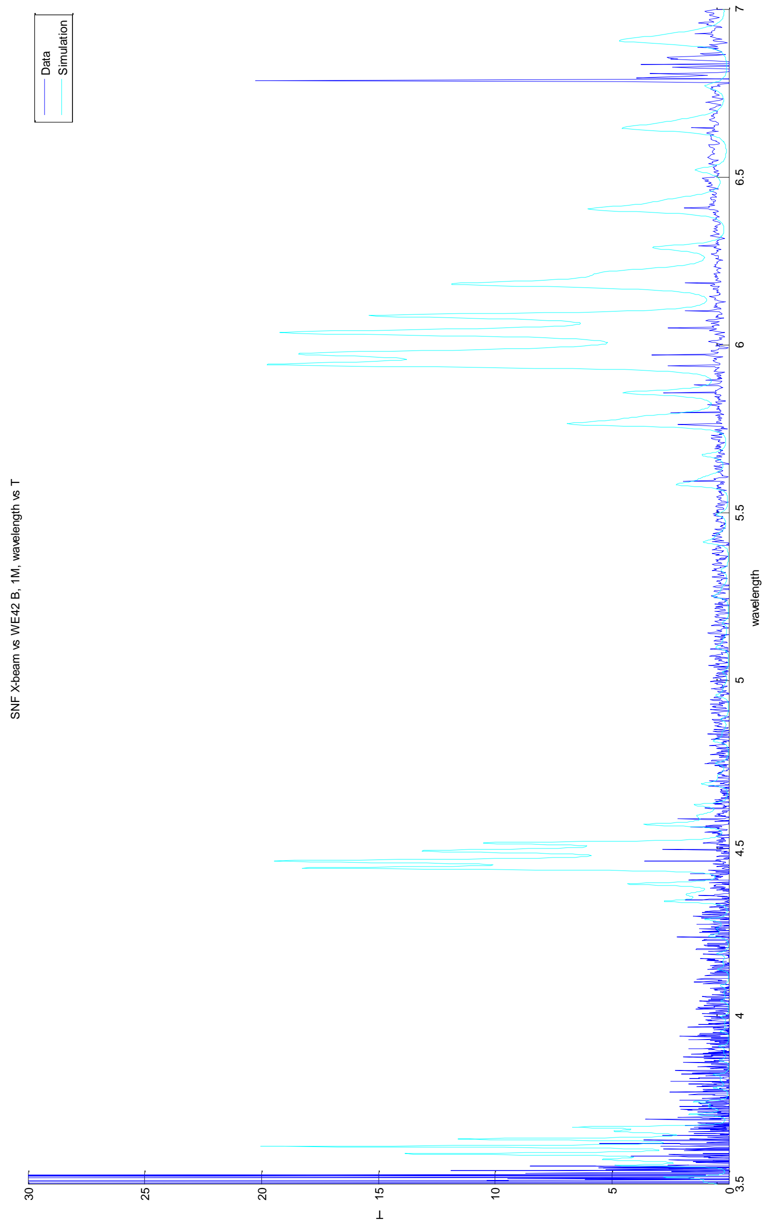


Figure 9.14:Transmission, SX-B device with one magnet (26 Gauss)

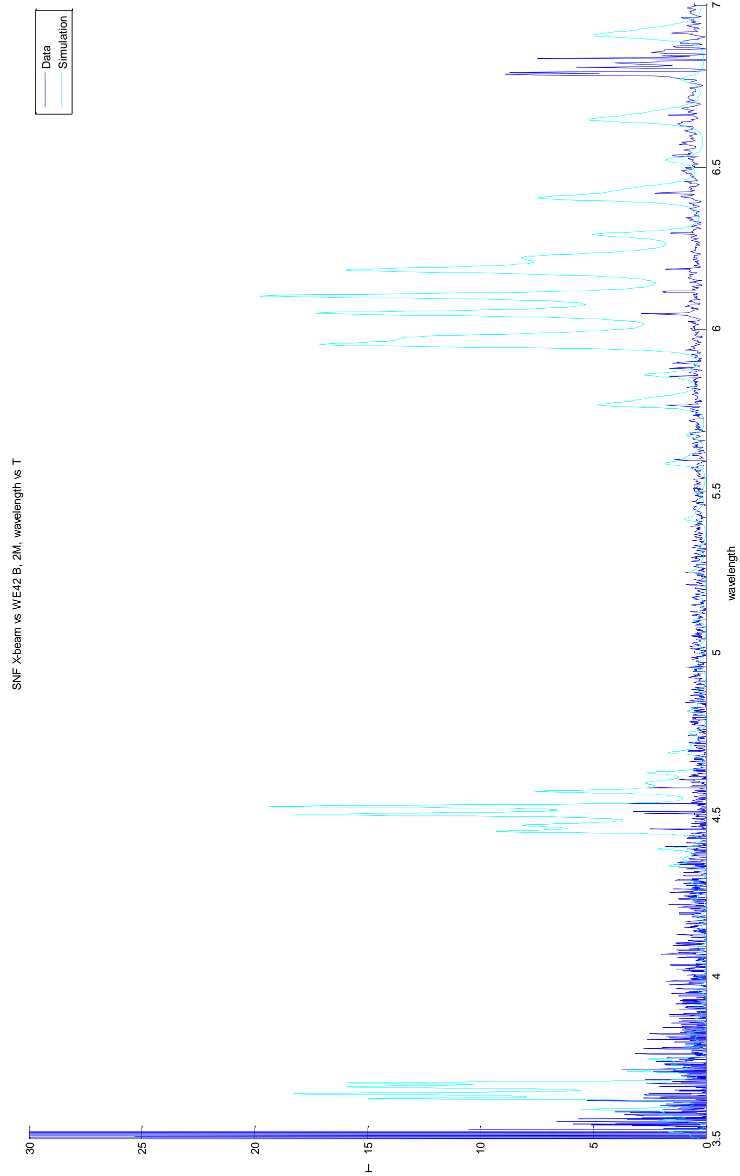


Figure 9.15: Transmission, SX-B device with two magnets (52 Gauss)

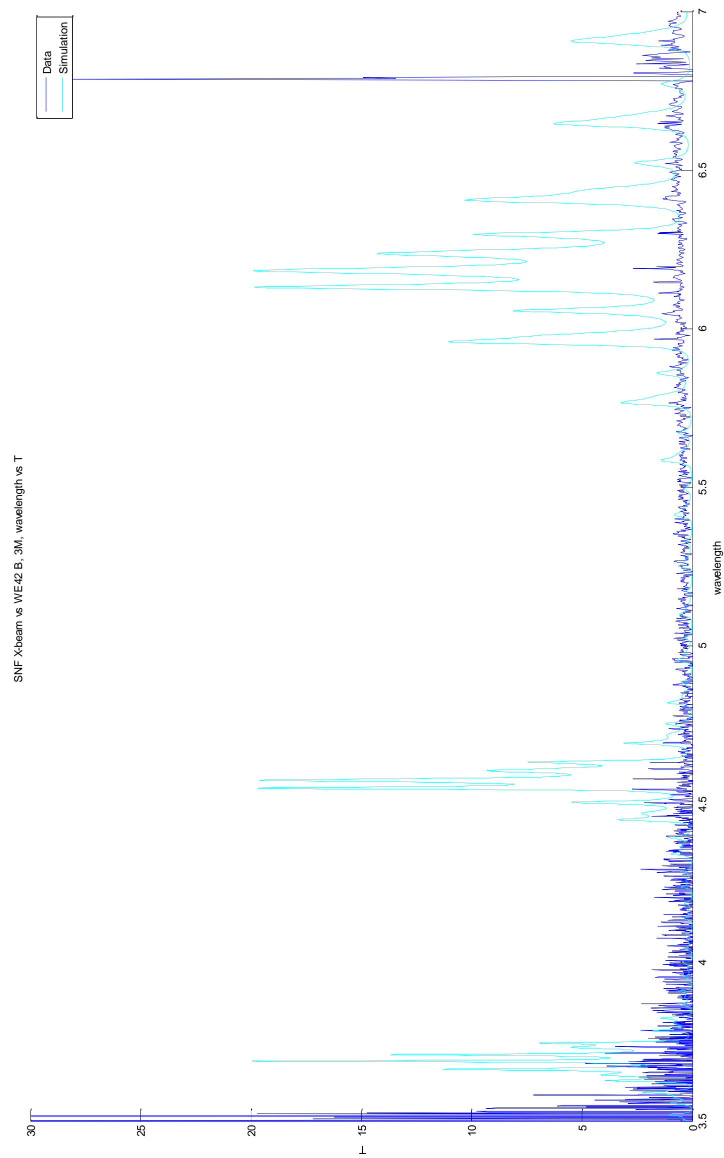


Figure 9.16:Transmission, SX-B device with three magnets (88.6 Gauss)

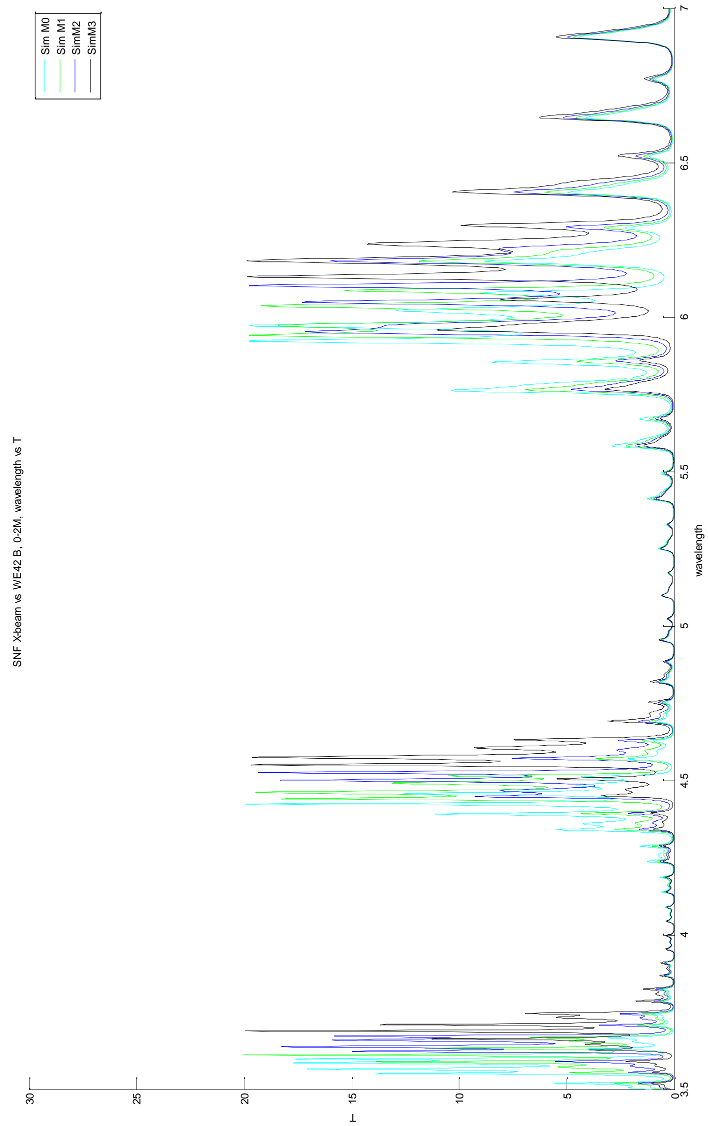


Figure 9.17:Transmission simulations, SX-B device with 0, 1, 2, and 3 magnets. Note change in peak position with number of magnets.

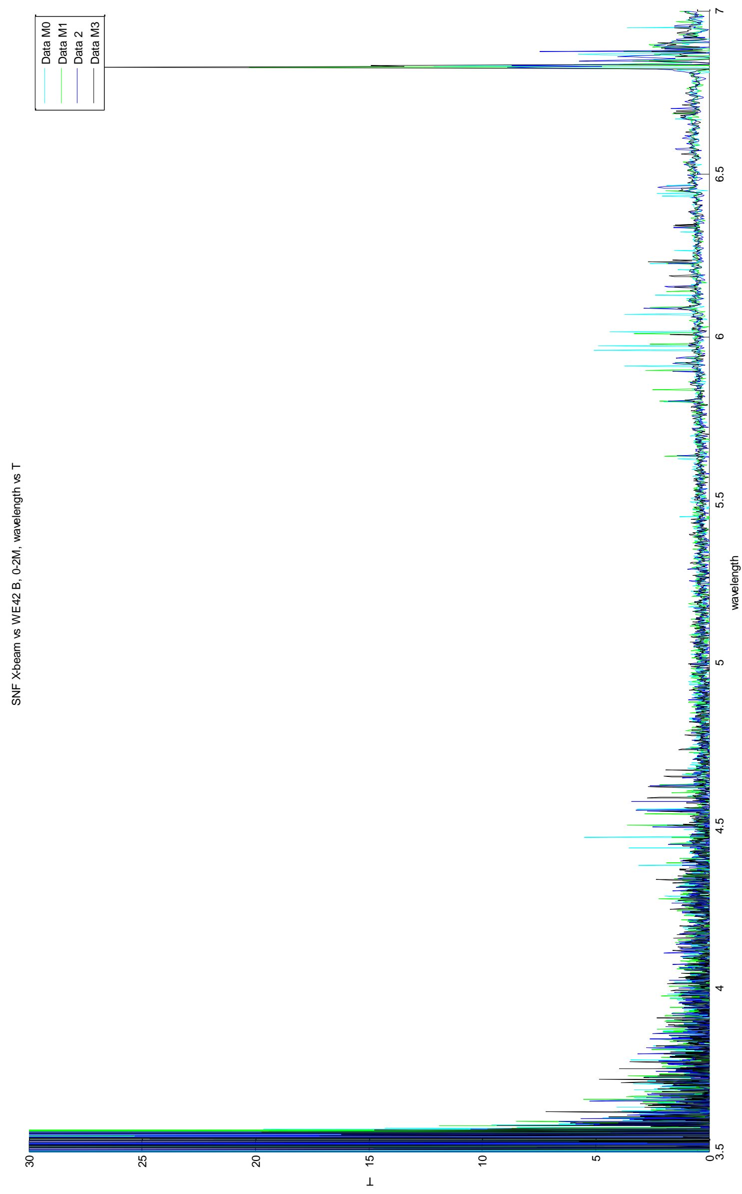


Figure 9.18:Transmission, SX-B device with combined data for 0, 1, 2, and 3 magnets

As can be seen from Figure 9.17, the mechanical actuation of the device is sufficient to produce a series of distinct optical peaks that would confirm the change in the filtering behavior of the device upon actuation. Matching the experimental curves in figures 9.13-9.17 to optical simulation results confirms the mechanical actuation behavior described in Chapter 8.

The 3-5 μm wavelength range is of main interest for this project. Detail of the transmission curve from Fig. 9.13, shown in Fig. 9.19, magnifies the region of interest from 4.0 to 4.9 μm. The experimental optical results show very good correlation of major peaks with the major peaks predicted by the simulation. The differences between the experiments and the simulation are due to the non-uniformities and other defects in the fabrication process. Reduction in the amplitude of transmission is explained by the greatly reduced optical area of the device and loss of emission from the source due to small apertures of the aluminum plate and aluminum washers. The simulation does not take into account any of these signal reduction effects. The current device shows a good compromise between optical, mechanical and fabrication considerations. This demonstrates that the device is a working prototype that, with improvements, could lead to a very competitive commercial device.

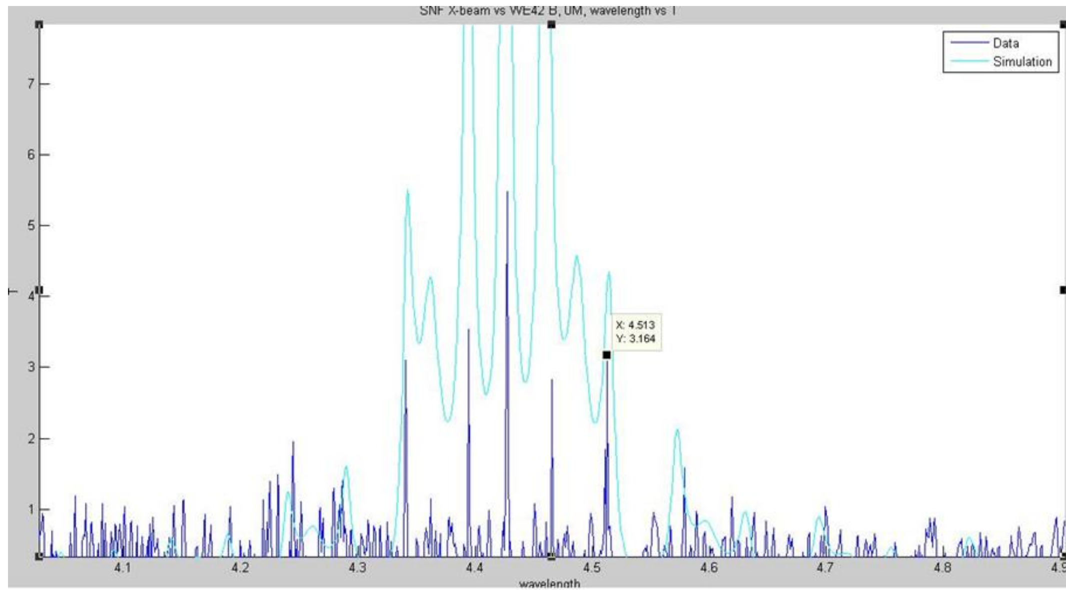


Figure 9.19 Detail of SX-B, 0M transmission

9.8 Summary of results

The optical experiments described in this chapter were performed to correlate the optical model and the mechanical model of the devices developed in earlier chapters. The optical model and the simulation software results are confirmed by the experimental data from the simplest device, MUMPS X-beam, shown in Fig. 9.5, and for static etalon, shown in Fig. 9.6. The dynamic optical behavior of the asymmetrical device correlates to the optical model, as shown in Figs. 9.7-9.12, but the widening of the bandwidth due to bowing prevents the device from being usable. Results for the interferometer made up of SNF fabricated chips shows correlation with the optical and mechanical models (Figs. 9.13-9.18), but the experimental signal level is extremely low. The low signal level is explained by the greatly reduced transmission area of the X-beam with magnet, approximately 10% of the original area, and further reduction of the signal by reduction of aperture due to two aluminum

washers, and de-focusing of the gold mirror with the samples being elevated by the magnets.

Chapter 10 : Summary and Conclusion

The goal of this project was to develop an optical filter for use in the 3-5 μm range. The development of the filter, from initial concept to process development to mechanical and optical testing, was completed and has been described in chapters 1-9.

Significant work was done on the optical design of the device, starting from the theory of Fabry-Perot interferometers, selection of materials for the reflectors, optical simulations of reflectors and ideal devices (chapters 2 and 3).

Mechanical design was performed to minimize the deformation of the optical areas upon actuation, while trying to keep actuation voltages low (chapter 4).

The fabrication process for optical filters was developed from layer deposition, stress analysis, layer patterning, resulting in a complete process (chapters 5-7). The final process (run 3) produced a yield of 100% with minimal defects and minimal surface roughness. The fabrication process and substrate selection were optimized to improve the optical behavior by more than two orders of magnitude from the first fabrication run.

The original method of actuation, electrostatic actuation, had to be changed to magnetic actuation with introduction of discrete permanent magnets attached to the optical area of the device (chapter 8). This modification resulted in very precise actuation, but has significantly decreased the optical area of the filters. From fabricated devices, optical measurements were taken that were in good agreement with computer simulations (chapter 9, Fig. 9.6).

In the course of this thesis, the first magnetically actuated MEMS Fabry-Perot interferometer was designed, fabricated and tested for MWIR range. Future development of this project, made possible by the development of analytic tools and a robust fabrication process described here, makes it possible to fabricate a commercially viable device to be used in either single pixel or arrays for applications in chemistry, biology and astronomy.

Future work by others on this device could involve mechanical re-design to take advantage of the magnetic actuation and make the device more compact. As several details of the design described here were developed for electrostatic actuation, such as contact pads and isolation channels, these features would not be needed, and this would simplify the fabrication process, i.e. tailor the fabrication process to magnetic rather than electrostatic actuation.

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Appendix A.

MATLAB code used in the optical simulations of the Fabry-Perot interferometer and the Bragg reflectors.

File: BestDeviceCavitySweep.m

```
% This program:
%  takes the best device -- here,
%  Si-SiN-SiO2-Ge-SiO2-Ge-Cavity-Ge-SiO2-Ge-SiO2-Ge-SiO2-Diaphragm
%  Device designed with central wavelenght of 4 um
%  Performs sweeps with cavity spacing from (3/2)=1.5 um to (6/2)=3
um,
%  delta=0.25 um,
%   records T
%  calculates FWHM for each

clear;
clc;
clf;



%Here, enter central wavelength:
lambC=4;
```

```
%Here, enter cavity distance:
%dCav=(1.5:0.25:3);

%Here, enter Si diaphragm thickness:
dSiD1=25;
dSiD2=50;

% This calculates optimal Bragg stack parameters:
dOx=(lambC/4)/nSiO2(lambC)
dGe=(lambC/4)/nGe(lambC)
dSiN=(lambC/4)/nSiN(lambC)

lamb=(1: 0.001: 8);
length(lamb)
%hold on;
axis([3 5 0 0.8])

%dCav=1.25;
%for  k=1:length(lamb)
%[r(k), R(k), t(k), T(k)] = FBAssymSubPostNit(lamb(k), dSiD, dSiN,
dOx, dGe, dCav, 0);
%k=k+1;
%end
%plot(lamb,abs(T), 'r');
```

```
dCav=109;

for  k=1:length(lamb)

[r(k), R(k), t(k), T(k)] = FBAssymSiBragg(lamb(k), dSiD1, dSiD2,

dOx, dGe, dCav, 0);

k=k+1;

end

plot(lamb,abs(T), 'c');


hold on;


dCav=101;

for  k=1:length(lamb)

[r(k), R(k), t(k), T(k)] = FBAssymBraggSi(lamb(k), dSiD1, dSiD2,

dOx, dGe, dCav, 0);

k=k+1;

end

plot(lamb,abs(T), 'r');



%legend( 'dCav=1.50', 'dCav=1.75', 'dCav=2.00','dCav=2.25',

'dCav=2.50');

title('T values for Fabry-Perot Interferometer with

lambdaCentral=4um')

xlabel(' Wavelength (um) ');

ylabel(' T  ');
```

```
hold off;


%FWHM:
%absT=abs(T);
%maxVal=max(absT)
%halfMax=maxVal/2
%find(absT>=halfMax)
```

File: FBAssymBraggSi

```
function [r, R, t, T] = FBAssymBraggSi(lambda, dSi1, dSi2, diSiO2,
diGe, dCav, angleIncident)
% This code: incident level => currently air
%             Si diaphragm
%             SiN
%             SiO2
%             Ge
%             SiO2
%             Ge
%             air (cavity)
%             SiO2
%             Ge
%             SiO2
%             Ge
%             SiO2
%             Ge
%             Si diaphragm
%             air
%

% Constants
epsilon=8.854e-12;
mu=1.26e-6;
```

```
% Initial Conditions
lamb=lambda ;
ango=angleIncident ;

%Layer thicknesses
di1=diSiO2 ;
di2=diGe;
di3=dSi1;
di4=dCav;
di5=dSi2;

% Index of refraction
no=1;
ns=1;
%SiO2
ni1=nSiO2(lamb);
%Ge
ni2=nGe(lamb);
% x-beam Si
ni3=nSi(lamb);
% Cavity (air)
ni4=1;
% Silicon diaphragm
ni5=nSi(lamb);

angs=asin((no/ns)*sin(ango));
```

```
angi1=asin((no/ni1)*sin(ango));
angi2=asin((no/ni2)*sin(ango));
angi3=asin((no/ni3)*sin(ango));
angi4=asin((no/ni4)*sin(ango));
angi5=asin((no/ni5)*sin(ango));

cosango=cosd(ango);
cosangs=cosd(angs);
cosangi1=cosd(angi1);
cosangi2=cosd(angi2);
cosangi3=cosd(angi3);
cosangi4=cosd(angi4);
cosangi5=cosd(angi5);

%parameters
kohi1=(2*pi()/lamb)*(ni1*di1*cosangi1);
kohi2=(2*pi()/lamb)*(ni2*di2*cosangi2);
kohi3=(2*pi()/lamb)*(ni3*di3*cosangi3);
kohi4=(2*pi()/lamb)*(ni4*di4*cosangi4);
kohi5=(2*pi()/lamb)*(ni5*di5*cosangi5);

coskohi1=cosd(kohi1);
sinkohi1=sind(kohi1);
coskohi2=cosd(kohi2);
sinkohi2=sind(kohi2);
coskohi3=cosd(kohi3);
```

```
sinkohi3=sind(kohi3);

coskohi4=cosd(kohi4);

sinkohi4=sind(kohi4);

coskohi5=cosd(kohi5);

sinkohi5=sind(kohi5);


sqso=sqrt(epsilon/mu)*no*cosango;

sqss=sqrt(epsilon/mu)*ns*cosangs;

sqss=sqrt(epsilon/mu)*ns*cosangs;

sqsi1=sqrt(epsilon/mu)*ni1*cosangi1;

sqsi2=sqrt(epsilon/mu)*ni2*cosangi2;

sqsi3=sqrt(epsilon/mu)*ni3*cosangi3;

sqsi4=sqrt(epsilon/mu)*ni4*cosangi4;

sqsi5=sqrt(epsilon/mu)*ni5*cosangi5;


% M parts calculation

m11i1=coskohi1;

m12i1=(i()/sqsi1)*sinkohi1;

m21i1=i()*sqsi1*sinkohi1;

m22i1=coskohi1;


m11i2=coskohi2;

m12i2=(i()/sqsi2)*sinkohi2;

m21i2=i()*sqsi2*sinkohi2;

m22i2=coskohi2;
```

```
m11i3=coskohi3;
m12i3=(i()/sqsi3)*sinkohi3;
m21i3=i()*sqsi3*sinkohi3;
m22i3=coskohi3;

m11i4=coskohi4;
m12i4=(i()/sqsi4)*sinkohi4;
m21i4=i()*sqsi4*sinkohi4;
m22i4=coskohi4;

m11i5=coskohi5;
m12i5=(i()/sqsi5)*sinkohi5;
m21i5=i()*sqsi5*sinkohi5;
m22i5=coskohi5;

matr1=[m11i1 m12i1; m21i1 m22i1];
matr2=[m11i2 m12i2; m21i2 m22i2];
matr3=[m11i3 m12i3; m21i3 m22i3];
matr4=[m11i4 m12i4; m21i4 m22i4];
matr5=[m11i5 m12i5; m21i5 m22i5];

matrf=matr5*matr1*matr2*matr1*matr2*matr1*matr2*matr4*matr3;

m11=matrf(1,1);
m12=matrf(1,2);
m21=matrf(2,1);
```

```
m22=matrf(2,2);


%r and R
r=(sqso*m11+sqso*sqss*m12-m21-
sqss*m22)/(sqso*m11+sqso*sqss*m12+m21+sqss*m22);
R=r*r;
%plot(lamb, abs(R));
%figure(2);
%plot(lamb, angle(R));




%t and T
t=(2*sqso)/(sqso*m11+sqso*sqss*m12+m21+sqss*m22);
T=(ns*cosangs)/(no*cosango)*(t*t);
%figure(3);
%plot(lamb, abs(T));
%figure(4);
%plot(lamb, angle(T));
```

File: NSi.m

```
function nSili = nSi(lambda)

C1Si = 10.6684293;
C2Si = 0.301516485;
C3Si = 0.003043475;
C4Si = 1.13475115;
C5Si = 1.54133408;
C6Si = 1104.0;
nSili = sqrt(1+ C1Si*lambda^2/(lambda^2-C2Si^2) +
C3Si*lambda^2/(lambda^2-C4Si^2) + C5Si*lambda^2./(lambda^2-C6Si^2));
%iSili = 4E-11*exp(1.654*lambda);
%nSili=rSili+i()*iSili;
```

File: nSiO2.m

```
function nOx = nSiO2(lambda)

A1Ox=0.6961663;
L1Ox=0.0684043;
A2Ox=0.4079426;
L2Ox=0.1162414;
```

```
A3Ox=0.8974794;
L3Ox=9.896161;
sqnOx=1+A1Ox*lambda^2/(lambda^2-L1Ox^2)+A2Ox*lambda^2/(lambda^2-
L2Ox^2)+A3Ox*lambda^2/(lambda^2-L3Ox^2);
nOx=sqrt(sqnOx);
```

File: nGe.m

```
function nGerm = nGe(lambda)

C1Ge = 9.28156;
C2Ge = 6.72880;
C3Ge = 0.44105;
C4Ge = 0.21307;
C5Ge = 3870.1;
nGerm=sqrt( C1Ge + C2Ge*lambda^2/(lambda^2-C3Ge) +
C4Ge*lambda^2/(lambda^2-C5Ge));
```

File: cosd.m

```
function cosdef = cosd(angle)
cosdef=(round(1e4*cos(angle)))/1e4;
```

File: sind.m

```
function sindef = sind(angle)
sindef=(round(1e4*sin(angle)))/1e4;
```