UC San Diego
UC San Diego Electronic Theses and Dissertations

Title
Multi-band high efficiency power amplifier

Permalink
https://escholarship.org/uc/item/6gb284v2

Author
Besprozvanny, Randy-Alexander Randolph

Publication Date
2011

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA, SAN DIEGO

Multi-Band High Efficiency Power Amplifier

A Thesis submitted in partial satisfaction of the requirements
for the degree of Master of Science

in

Electrical Engineering (Electronic Circuits and Systems)

by

Randy-Alexander Randolph Besprozvanny

Committee in charge:

      Professor James Buckwalter, Chair
      Professor Gabriel Rebeiz
      Professor Daniel Sievenpiper

2011

The Thesis of Randy-Alexander Randolph Besprozvanny is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

_____

_____

_____

_____
Chair

University of California, San Diego

2011

DEDICATION

I would like to first dedicate this work to my mother, Penny Besprozvanny, for without her, I would not be here.

Secondly, I would like to dedicate this work to Todd Thornton, a mentor and a friend that has not wavered in his commitment, guidance and friendship throughout the years.

TABLE OF CONTENTS

LIST OF SYMBOLS

[μ]   Scaling Factor of 1×10^{-6}

[∫]   Integral

[∑]   Summation

[ω]   Angular Frequency

[ϕ]   Conduction Angle

[π]   Pi

[θ]   Phase Variable

[ζ]   Phase Variable

[φ]   Phase Variable

[λ]   Wavelength

[δ]   Partial Derivative

[√]   Square Root

[Ω]   Ohms

[ε]   Dielectric Constant

LIST OF FIGURES

LIST OF FIGURES

LIST OF FIGURES

LIST OF TABLES

ABSTRACT OF THE THESIS

Multi-Band High Efficiency Power Amplifier

by

Randy-Alexander Randolph Besprozvanny

Master of Science in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2011

Professor James Buckwalter, Chair

Achieving high efficiency power amplification over multi-octave RF bandwidths pose many design challenges. Conventional design techniques do not support high efficiency operation since use of distributed matching circuits and/or multiplexing several power amplifiers incur non-optimal matching environments or high output losses. A new design approach is discussed whereby using the latest Gallium Nitride transistor technology and leveraging a Class E circuit environment, multiple electronically switched output networks are provided to the RF transistor providing high efficiency operation over multi-octave RF bandwidths. Two electronic switching elements are considered including PIN diodes and RF transistors. Using commercially available

components, measurements are conducted on a physical prototype using PIN diode switch elements demonstrating typical efficiencies of 50% over two octaves bandwidth and at frequencies up to 2.4GHz.

CHAPTER 1

1.   Introduction

As wireless communication evolves in the highly competitive technology market, the need for high efficiency power amplifiers is more critical than ever. The latest commercially available RF transistor technologies are able to offer power amplifier systems with high efficiency, high power densities and high frequency capabilities. To achieve enhanced efficiency operation, specialized tuning techniques are necessary that minimize the dissipated power and control the harmonic content from the device. These design techniques define specific high efficiency operating classes, but offer very narrow RF bandwidths.

Extended bandwidths can be offered in conjunction with these high efficiency design techniques by multiplexing multiple narrow-band power amplifiers together yielding a larger composite RF bandwidth. This method is not ideal since its implementation can be very large, expensive and incur high output losses. Another design approach is to use a distributed matching circuit environment. This method is also not ideal because high transformation ratios are required when matching to high power transistors. As a result, a non-optimal matching environment is provided without the ability to effectively control the dissipated power or harmonics from the device.

A new design approach shall be discussed by which multiple narrow-band, high efficiency circuits shall be electronically switched into the RF transistor matching network. This method shall provide enhanced efficiency operation over a demonstrated composite bandwidth in excess of two octaves. Utilizing Microwave Integrated Circuit (MIC) manufacturing processes, a prototype shall be constructed to demonstrate up to three bands with output power levels of 30W using commercially available components.

CHAPTER 2

2. Amplifier Operating Class

A power amplifier design requires a matching circuit on the input and output of an RF transistor in order for the device to provide signal amplification. These matching circuits are tailored for specific operating classes and are defined by the circuit environment and bias condition at the device. Conventional designs include Class A, Class AB and Class B operating conditions, while high efficiency designs include Class E, Class F and harmonically tuned circuits. Each presents inherent trade-offs in bandwidth, linearity and efficiency.

A Class A design is implemented by biasing the RF transistor such that the quiescent DC current draw is half of the maximum channel current capability, denoted as "I_{dss}". The bias current defines the conduction angle of the device. When the device is excited with a sufficiently large sinusoidal input signal, the peak to peak output current waveform conducts between "I_{dss}" and 0 Amps. The circuit implementation provides wide bandwidth capabilities by matching to the device load-line impedance and providing a conjugate match to the device reactance. The output circuit impedance allows the device to operate between its maximum current and voltage limitations, whereby achieving maximum output power capability and efficiency.

Efficiency is degraded by an intrinsic parasitic property of the transistor defined as the device knee voltage "V_{min}". At this operating point, the transistor transitions between the saturation and triode operating points and results in current collapse for any further decrease in drain voltage. Effectively, efficiency is reduced since the transistor is unable to produce RF power at drain voltages below "V_{min}" while DC supply power is dissipated within this region between common potential and the knee voltage.

With the exception of the current magnitudes near "I_{dss}" and 0, the device yields minimal distortion of which is predominantly controlled by the current saturation and non-linear device transconductance near threshold voltages. Therefore, Class A provides one of the most linear operating classes. Consequently, since the bias point operates the device at half "I_{dss}", Class A operation is one of the least efficient designs. Assuming an ideal RF transistor, the maximum efficiency of a Class A design is 50%. The corresponding operating characteristics are described by Colantonio [1] as:

$$P_{out} = 1/4 \, [I_{dss} * (V_{ds} - V_{min})]$$

$$R_L = 2(V_{ds} - V_{min}) / I_{dss}$$

$$N_d = ½ \, (1 - V_{min} / V_{ds})$$

A Class AB or Class B design is implemented by biasing the RF transistor such that the quiescent DC current draw is reduced from half "I_{dss}" to 0 Amps. When the device is excited with a sufficiently large sinusoidal input signal, the peak to peak output current waveform conducts between "I_{dss}" and 0 Amps as in the Class A case. Since part of the input voltage waveform operates the transistor below threshold voltage, part of the output current waveform is effectively clipped below 0 Amps, requiring more input drive power to achieve "I_{dss}", thereby reducing gain.

Since part of the current waveform is clipped, a non-sinusoidal signal is created as governed by the device conduction angle. This non-sinusoidal waveform adds distortion to the output power signal and can be represented by the Fourier series of the current waveform. Consequently, higher efficiency is achieved since the static DC power requirements are reduced without a peak power reduction from the transistor. When considering an ideal device, the maximum efficiency of a Class AB or Class B design ranges from 50% to 78.5% depending on the conduction angle. The corresponding design equations are detailed by Colantonio [1] as:

Conduction Angle:

$$\phi = \cos^{-1}(I_{dc}/I_{dss})$$

Fourier Series Waveforms:

$$i_D(t) = I_D + \sum I_n \cos(n\omega t + \zeta_n)$$

$$v_{DS}(t) = V_{dc} - \sum I_n |Z_n| \cos(n\omega t + \varphi_n)$$

Fourier Series Coefficients:

$$I_0 = (I_{dss}/2\pi) * [(2\sin(\phi/2) - (\phi*\cos(\phi/2)] / [1 - \cos(\phi/2)]$$

$$I_1 = (I_{dss}/2\pi) * [\phi - \sin(\phi)] / [1 - \cos(\phi/2)]$$

$$I_n = (2I_{dss}/\pi) * [\sin(n * \phi/2)\cos(\phi/2) - n*\sin(\phi/2)\cos(n * \phi/2)] / [n*(n^2 -1)*(1-\cos(\phi/2))]$$

Operating Characteristics:

$$P_{out} = [I_{dss} * (V_{ds} - V_{min})] * [\phi - \sin(\phi)] / [4\pi (1 - \cos(\phi/2)]$$

$$R_L = [2\pi (V_{ds} - V_{min}) (1 - \cos(\phi/2)] / I_{dss} (\phi - \sin(\phi))$$

$$N_d = [(\phi - \sin(\phi)) * (V_{max} - V_{min})] / [(2\sin(\phi/2) - \phi\cos(\phi/2)) * (V_{max} + V_{min})]$$

The Class AB and Class B power amplifier circuit design can achieve yet higher efficiencies by providing a harmonically tuned output impedance environment to the RF transistor. This harmonically tuned circuit design presents specific impedances to the device at the fundamental and harmonic frequencies, whereby minimizing the dissipated power within the transistor and reducing harmonic power delivered to the load. These are defined as the power balance conditions as discussed by Colantonio [1] and require the following relationships be satisfied simultaneously in order to achieve maximum efficiency:

Harmonic Power:

$$P_{dissipated} + \sum_{n=2}^{\infty} P_{out,n} = 0$$

Dissipated Power:

$$P_{dissipated} = 1/T \int_0^T v_{DS}(t) * i_D(t) \, dt = 0$$

A Class F design is a type of harmonically tuned amplifier which presents high odd-order harmonic impedances and low even-order harmonic impedances to the RF transistor drain. This harmonically tuned approach presents a square drain voltage to the device whereby the overlap between drain current and drain voltage is minimized. Reducing the time-domain overlap of the two drain signals ideally results in no dissipated power within the device satisfying part of the power balance condition and ideally resulting in up to 100% efficiency. Limited bandwidth in excess of 20% is achieved by controlling each of the harmonic impedances in this operating class.

A Class E design is another high efficiency operating class by which dissipated power and harmonic content delivered to the load are simultaneously reduced. These conditions are satisfied by ideally operating the device as a switch and ensuring that when the transistor is enabled, the drain voltage is zero. Simultaneously, it is necessary to ensure that any change in voltage across the transistors parasitic drain capacitance is zero so that no switching losses occur in the device. As discussed by Colantonio [1], these two conditions are defined as the Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS) and thus satisfy part of the power balance condition.

The circuit design requires a purely sinusoidal load current setup, an inductive load impedance with a phase angle of 32.5 degrees to the transistor and a specific amount of shunt capacitance on the output network as detailed by Asbeck [3]. The sinusoidal load current is facilitated by implementing a series resonator in-line with the load. As such, no power is lost to harmonics satisfying the remaining part of the power balance condition to ideally achieve 100% efficiency. The resonator is mis-tuned from the fundamental frequency by increasing the series inductance providing the required load phase angle. This results in limited bandwidth due to the reactive load variation over frequency.

For the time period that the transistor is enabled, a sinusoidal load current is constrained by the series resonator. During the period that the transistor is disabled, the remaining part of the sinusoidal load current is sustained through the output networks shunt capacitance. The required capacitance is determined by the operating frequency and can ideally absorb the device drain capacitance.

Increased RF bandwidths can be achieved by implementing reactance compensation on the output impedance network as discussed by Grebennikov [4] by which a consistent load phase angle is provided over much wider frequency ranges. It has been demonstrated that high efficiency operation can be provided for bandwidths in excess of 40% as discussed by Asbeck [3].

This circuit design approach is implemented by including a shunt resonator in conjunction with the series resonator on the output impedance network. The series resonator is tuned at the fundamental operating frequency while the shunt resonator is mis-tuned to present an inductive load phase angle of 34.244 degrees. The combination of the two resonators allows the shunt resonant circuit to compensate the frequency sensitive reactance variation of the series resonant circuit as is illustrated in FIGURE 2-1.

By offering extended bandwidth potential and higher frequency capabilities over the other operating class discussed, the reactance compensation Class E design is the best suited circuit configuration for the Multi-Band High Efficiency Power Amplifier and will serve as the baseline circuit design approach.
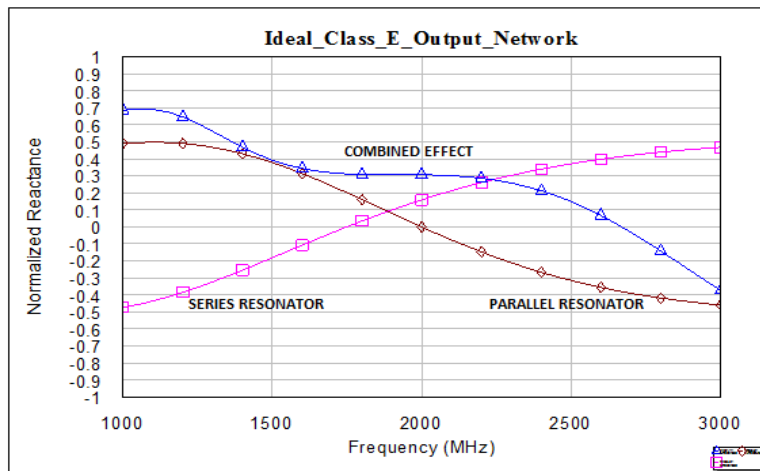
FIGURE 2-1: Reactance-Compensated Class E Output Network Reactance

CHAPTER 3

3. Power Transistor Technologies

There are four commercially available transistor technologies that can be considered for the Multi-Band High Efficiency Power Amplifier. These technologies include Gallium Arsenide (GaAs), Gallium Nitride (GaN), Silicon Carbide (SiC) and Silicon (Si) Laterally Diffused Metal Oxide Semiconductor (LDMOS) devices. Selection of the appropriate device is determined by the circuit requirements and can be evaluated based on the device properties detailed by Colantonio [1] and subsequently shown for the key parameters in TABLE 3-1.

Achieving high system efficiency not only requires a high efficiency circuit design, but selection of a transistor that can provide high power gain. Since a power amplifier achieves its highest efficiency when operated in saturation, high power gain reduces the input drive requirements to achieve saturation thereby resulting in high power added efficiency (PAE).

A particular transistors transit frequency "F_t" and maximum power gain frequency "F_{max}" limits are metrics used to determine the associated power gain. The transit frequency is the point where the device current gain goes to unity while the maximum power gain frequency is the point where the output power of a device is equivalent to the input power. Each frequency limit decays at a rate of 20dB per decade whereby the maximum expected device gain can be extrapolated based on the desired operating frequency. The corresponding maximum operating frequency should be selected in order to achieve a minimum 10dB. The relationship for the two frequency limits are detailed by Asbeck [3] as:

$$F_t = g_m \, / \, 2\pi \, (C_{gs} + C_{gd})$$

$$F_{max} = F_t \, / \, \sqrt{[2(R_g/R_o) + (8\pi \, F_t R_g C_{gd})]}$$

TABLE 3-1: Various Semiconductor Properties Contrasted

PROPERTY	UNITS	TRANSISTOR TECHNOLOGY			
		Si	GaAs	GaN	4H-SiC
Electron Mobility	cm^2/V*S	1500	8500	1000	900
Hole Mobility	cm^2/V*S	450	400	350	120
Bandgap	eV	1.12	1.42	3.2	3.23
Avalanche Field	10^5 V/cm	3.8	4.2	50	35
Saturated Drift Velocity	10^7 cm/s	0.7	2	1.8	0.8
Saturation Field	10^3 V/cm	8	3	15	25
Thermal Conductivity at 25C	W/cm*C	1.4	0.45	1.7	4.9
Dielectric Constant	-	11.9	12.9	14	10
Substrate Resistance	Ω*cm	-	>1000	>1000	1-20

High "F_t" and "F_{max}" frequencies are dependent on high device transconductance "g_m." There are many factors involved in achieving high transconductances from an RF transistor including transistor design, but the primary mechanism is attributed to high device electron mobility. GaAs transistors exhibit the highest electron mobility and consequently yield the highest power gain of the considered technologies. Among the wide bandgap devices considered, GaN yields the highest transconductance and associated power gain capabilities.

Another device characteristic needed to further enhance efficiency capability from an RF transistor are associated with the intrinsic parasitic elements. For the device technologies considered, various commercially available devices with a representative output power of 30W were evaluated as shown in TABLE 3-2.

Selection of a high efficiency device should include a low knee voltage "V_{min}" since it sets the upper limit on the device efficiency. For a particular current conduction capability, a low "V_{min}" is associated with a low on-state resistance "R_{on}" which is described as the ratio of "V_{min}" and "I_{dss}". By comparing the commercially available transistor technologies, GaAs transistors offer the lowest on-state resistance, while GaN offers the lowest among the wide bandgap devices.

TABLE 3-2: Commercially Available RF Power Transistor Properties

Manufacturer	Part Number	Technology	Rated Power	Voltage	Breakdown Votlage	Drain Capacitance	On-State Resistance	Trans-conductance	Ref.
			W	V	V	pF	Ω	mS	
Eudyna	FLL300IL-3	GaAs	30	10	15	-	0.1	6000	[14]
NXP	BLF3G21-30	LDMOS	30	28	65	48	0.3	3000	[15]
Cree	CRF24060	SiC	60	48	120	5	-	800	[16]
Cree	CGH60030	GaN	30	28	100	1.3	1.1	1800	[5]

Lastly, by operating an RF transistor in a Class E circuit environment, a device that can withstand high breakdown voltages is required. As detailed by Cripps [2], the Class E output circuit can present drain voltages in excess of 3.6 times the nominal DC bias voltage. Evaluating the key device properties show that only GaN presents the highest breakdown voltage margin relative to the nominal bias voltage. This is attributed to avalanche field strengths an order of magnitude higher than all other considered technologies.

3.1   *Power Transistor Selection*

Since the Multi-Band High Efficiency Power Amplifier is to be based on a Class E circuit design, high design voltages require wide bandgap devices to be considered exclusively. GaN transistors are able to offer the best balance of intrinsic properties and operational characteristics, making them the best technology choice.

Most commercially available GaN transistors are available in a packaged configuration. However, achieving maximum efficiency and frequency potential requires specific control of the impedances at the transistor drain, making it difficult to compensating package parasitic contributions. Therefore, device selection must consider an un-packaged transistor in "DIE" form. Consideration of the various commercially available devices has been restricted to transistors that can deliver output power levels of approximately 30W. Use of higher power device is possible depending on manufacturer product offerings. The various un-packaged, commercially available GaN transistors and their associated properties are summarized in TABLE 3-3.

TABLE 3-3: Commercially Available GaN DIE Transistors

Manufacturer	Part Number	Process	Rated Power	Vds	Vds,max	Cds	Fmax	Reference
		um	W	V	V	pF	GHz	
RFMD	RF3931D	0.5	30	50	150	12	0.08	[17]
Triquint	TGF2023-05	0.25	25	28	40	1.2	2.07	[12]
Cree	CGH60030D	0.4	30	28	100	1.3	2.35	[5]

Selection of the best commercially available DIE GaN transistor is predicated on the device maximum frequency capability when used in the reactance compensation Class E amplifier design. This limit is set by the device drain capacitance since the desired value becomes progressively small as the operating frequency increases. Operation beyond this limit is possible, however reduced efficiency will occur since the ZVDS operating constraint can no longer be satisfied. This upper frequency limit for Class E operation is described by Grebennikov [4] as:

$$F_{max,Class-E} = 0.0798 * [P_{out} * (C_{ds} * V_{dc}^2)^{-1}]$$

Use of larger power devices is possible without ideally influencing the frequency limit capabilities of the device in Class E operation. This is a result of the inverse proportionality between output power and drain capacitance. Thus, the limit can only be influenced by the DC bias voltage for a particular device.

By comparing the commercially available GaN device properties shown in TABLE 3-3, the best transistor choice is the Cree CGH60030D which offers the highest output power capabilities and frequency limit capabilities.

CHAPTER 4

4.   Power Transistor Device Model

The power amplifier design requires a non-linear transistor model that is representative of the physical device when operated under large signal conditions. When supplemented with external circuit elements, the model can reveal the fundament and harmonic behavior of the circuit by which a high efficiency, high frequency power amplifier design can be characterized and optimized. Evaluation of the transistor active and passive characteristics is necessary in the design of the external circuit elements.

A non-linear model is available from Cree Inc. for the CGH60030D transistor and is used in the Applied Wave Research (AWR) Microwave Office harmonic balance simulator. After consulting with Cree Inc., the transistor model is based on a modified Kondoh model [10] with inputs from Fager-Statz [19]. By using Cree Inc. proprietary modifications and additions, the non-linear model was constructed.

4.1   Transistor Active Characteristics

The active "on-state" characteristics of the CGH60030D can be evaluated by simulating the transistor drain voltage and current "I-V" characteristics. Since the selected transistor is a depletion mode device, the I-V characteristics can be evaluated by stepping the gate voltage between [-5.0V to +2.0V] and measuring the associated drain current as the drain voltage is swept between [0.0V to +50.0V]. The corresponding I-V characteristics are shown in FIGURE 4-1.
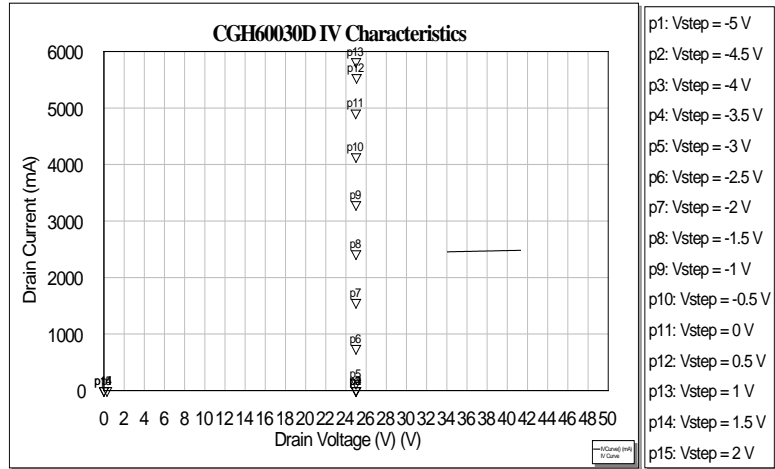
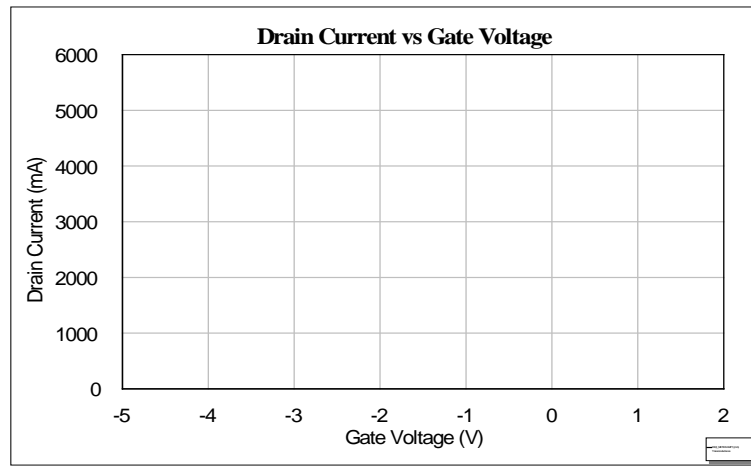FIGURE 4-1: I-V Characteristics for the CGH60030D

FIGURE 4-2: Drain Current vs. Gate Voltage Characteristics for the CGH60030D

TABLE 4-1: Active Characteristics for the CGH60030D

Description	Symbol	Units	Value	Equation
Minimum Voltage	V_{min}	V	5.75	Figure
Threshold Voltage	V_t	V	-3.4	Ids = 1mA
Saturation Voltage	$V_{gs,sat}$	V	0.8	Ids = 5.8A
Saturated Current	I_{dss}	A	5.8	Figure
Transconductance	g_m	S	1.8	Figure : $\delta I_D / \delta V_{gs}$
On-State Resistance	R_{on}	Ω	1	V_{min} / I_{dss}
Channel Modulation	λ	$1/\Omega$	0.00027	Figure 2: $\delta I_{ds,sat} / \delta V_{ds,sat}$

Additional active device characteristics can be obtained by evaluating the transistor "$I_{ds} - V_{gs}$" characteristics. With the drain biased at +28V, the transistor gate voltage was swept between [-5.0V to +2.0V] and the associated drain current recorded. The corresponding $I_{ds} - V_{gs}$ characteristics are shown in FIGURE 4-2. The device active characteristics are summarized in TABLE 4-1.

4.2 *Transistor Passive Characteristics*

The device model provided by Cree Inc. is a locked circuit element with four ports and does not permit visibility of any internal device characteristics. The only accessible attributes are the transistor gate, drain, source device terminals along with a port to monitor the device junction temperature.

Since the intrinsic properties of the transistor are critical to the design of the Class E output network, a representative model is constructed based on the equivalent transistor model detailed by Kondoh [10]. The corresponding equivalent transistor model is shown in FIGURE 4-3. Leveraging the model design considerations outlined by Pengelly [18], the model shall be representative of the transistors passive components. The current generator shall be ignored in the equivalent model and it shall be compared to the CGH60030D with ideal bias components, +28V drain bias and operated at pinch-off [$V_{gs} = -6V$].
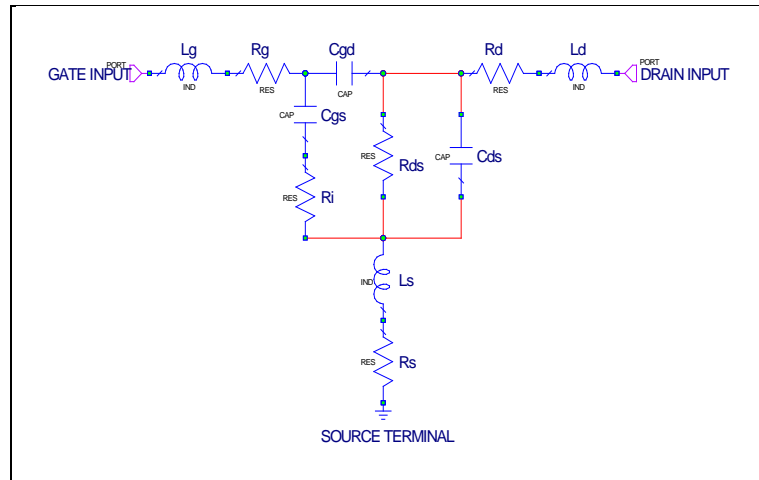
FIGURE 4-3: Equivalent RF Transistor Model

Baseline component values shall be leveraged from published values for a similar GaN DIE transistor, the Triquint TGF2023-05. Within the product datasheet [12], Triquint lists the device component for their 1.25mm GaN unit cell which is representative of the 6W transistor transistor. Since the CGH60030D is a 30W device, the device is approximated as five 1.25mm unit cells arranged in parallel, except for the parasitic elements "C_{gs}", "C_{ds}" and "C_{gd}" which are published in the Cree product datasheet [5]. The corresponding initial values are detailed in TABLE 4-2. The "R_{ds}" value was selected based on the leakage current through the drain terminal of the locked model. The corresponding leakage current was simulated as 13.9 µA and was approximated in the equivalent linear model as a 2MΩ resistance.

Since the Triquint GaN transistor is based on the 0.25 µm fabrication process and the Cree GaN transistor is based on the 0.40 µm fabrication process, a small error between the two models were observed. To bring the corresponding impedance environment in closer agreement, each component was iteratively tuned. The corresponding final values were then determined as shown in TABLE 4-2 for the CGH60030D device.

TABLE 4-2: Transistor Small Signal Equivalent Model Parameters

PARAMETER	UNITS	DEVICE	
		TGF2023-05	CGH60030D
Cgs	pF	8.95	8.6
Cgd	pF	0.32	0.86
Cds	pF	1.54	1.3
Lg	nH	-0.0026	-0.023
Ld	nH	0.0036	0.04
Ls	nH	0.00116	0.00116
Rg	Ω	0.156	0.26
Rd	Ω	0.256	0
Rs	Ω	0.026	0.026
Ri	Ω	0.052	0.052
Rds	Ω	24.72	2000000

After fine tuning the equivalent transistor model, the equivalent impedance environment was evaluated with respect to the gate and drain terminals while the source was terminated to ground. The corresponding impedance environment was then compared to the locked CGH60030D transistor model.

The corresponding input impedance and output impedance for both models are simultaneously detailed in FIGURE 4-4 and FIGURE 4-5, respectively. Correlating the two models together yields a typical error of less than 1Ω in magnitude. This close correlation validates the equivalent transistor model behavior of the CGH60030D. Under idealized circumstances, only "C_{ds}", "C_{gs}" and "C_{gd}" present the most significant parasitic loading effects in the off-state as these parameters are the largest for the selected device, however the contribution of the additional parasitic elements becomes more pronounced at higher operating frequencies.
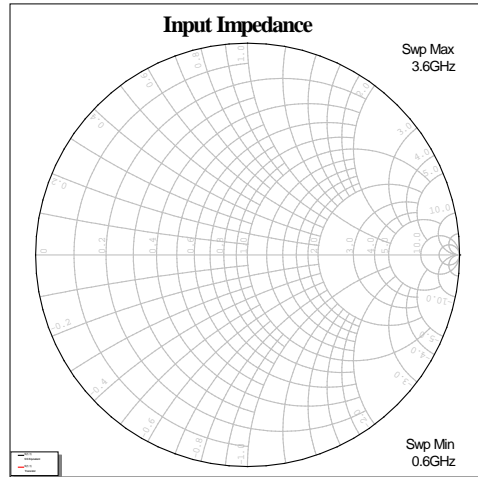
FIGURE 4-4: Transistor Input Impedance
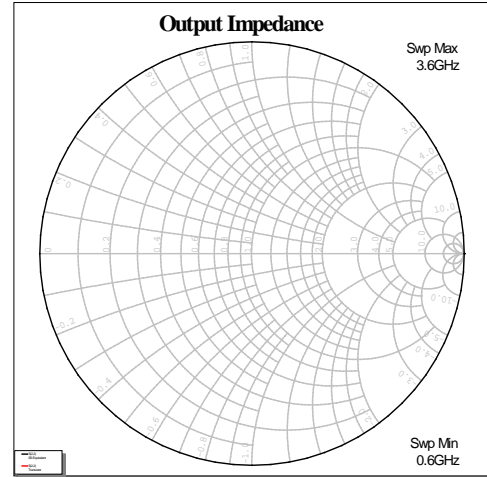
FIGURE 4-5: Transistor Output Impedance

CHAPTER 5

5.   Microwave Integrated Circuit Manufacturing Process

Physical realization of the power amplifier will require Microwave Integrated Circuit manufacturing processes. MIC assemblies provide integration of DIE RF transistors, substrates, associated passive components and specific metal features needed to fully realize a power amplifier design on a common assembly.

The substrate to be used for MIC assembly is Asfired Alumina Oxide (Al_2O_3). This substrate presents a dielectric constant "ε_r" of 9.8 while exhibiting excellent thermal conductivities in excess of 18 W/m*K. The thickness and dielectric constant influence the characteristic impedance of the transmission line and is arbitrarily selected as 20 mils. The conductor metallization will provide a solid ground plane on one surface while the other side shall have features facilitating the power amplifier design. The conductor material composition shall consist of 0.15 mils Gold (Au) over 0.006 mils Palladium (Pd) over 0.003 mils Tin-Tungsten (TiW).

The entire assembly shall be constructed on a Copper-Molyblyum-Copper (CuMoCu) base material. The assembly begins by applying Gold-Germanium (AuGe) pre-forms between the CuMoCu carrier, the substrate and under a transistor shim. The transistor shim is made of gold plated Molyblyum (Mo) and is used to account for the height differences between the transistor thickness and the substrate height so that the final assembly sets the top of the transistor at the same level as the substrate. The assembly is heated to 400C at which point the AuGe reflows and joins the substrates and shim to the CuMoCu.

After the substrates and shim are soldered in place with the pre-forms, Gold-Tin (AuSn) solder is placed between the RF transistor and the transistor shim. The assembly is heated up to 300C at which point the AuSn reflows and bonds the transistor to the assembly.

The RF transistor is connected to the substrates using three mil thick silver ribbons. Each ribbon is gap welded to the gate or drain land pad using DIE attach manufacturing processes.

Inductors shall be hand wound AWG-30 silver wire and shall be gap-welded to the substrates where appropriate. All tuning capacitors shall be the DiCAP series single layer capacitors from DiLABS with values and voltage breakdown limits required by the design. Each capacitor shall be installed on the substrates or CuMoCu carrier using conductive epoxy.

CHAPTER 6

6. High Efficiency Power Amplifier Design

The Multi-Band High Efficiency Power Amplifier design process shall implement an input matching circuit, an output matching circuit, bias networks and switch elements. The input matching circuit is responsible for matching the transistor input impedance to the system characteristic impedance, thereby maximizing the device gain and optimizing PAE. The output impedance network shall facilitate a high efficiency circuit environment. The bias networks shall provide DC voltage to the gate, drain and switch elements as necessary. The switch elements shall facilitate multi-band functionality of the output matching circuit. The general circuit schematic is shown in FIGURE 6-1.

6.1   Bias Circuit

Each bias circuit shall provide a high impedance RF path to the DC supply providing the appropriate DC bias voltage. The circuit implementation is achieved using an inductor between the supply and the RF path. After the inductor, a capacitor is used to provide a low impedance path to ground whereby increasing isolation between the two points.

The inductor shall be implemented by gap welding a silver AWG-30 wire to the substrates. Each wire shall by hand wound around a 60-mil diameter core with a total of 8-turns. The total inductor length shall be 120-mils yielding a net inductance of 48nH. The substrates shall provide a 25-mil square land pad attachment point which will be connected to the main RF path through 5-mil wide feed lines.
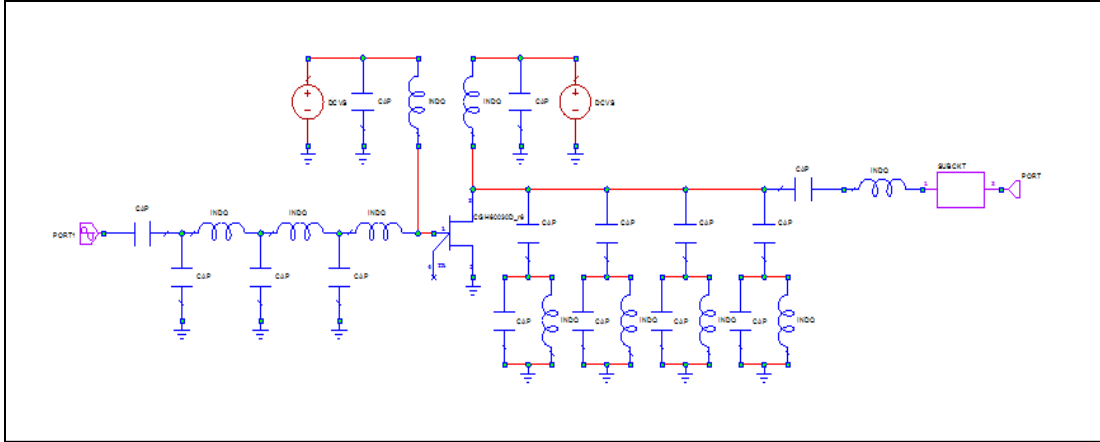
FIGURE 6-1: Multi-Band Class E Design Schematic

The bias network is completed by placing DC bypass capacitors after the inductor on the supply side. The DC bypass capacitor selected is the D20BU101F1EX, 100pF single layer capacitor from DLI Dielectric Laboratories. Isolation is further increased by placing the D20BU101F1EX adjacent to the American Technical Ceramics ATC200A102KCA100X, 1000pF gold terminated capacitor. Each capacitor is connected to the inductor using silver ribbons which are attached using thermosonic ribbon bonding.

To ensure that the bias network is properly isolating the DC supply from the RF path, the bias network discussed was modeled. The corresponding pass-band performance was evaluated for the bias networks connected in the center of two 100-mil long, 50Ω lengths of line. The isolation through the bias network was also modeled by placing an RF port after the inductor and recording the insertion loss between the main path and the third port. The results are detailed for the input bias network and output bias network in FIGURE 6-2 and FIGURE 6-3, respectively. The results show good isolation characteristics of at-least -30dB and insertion losses up to -0.08dB demonstrating the physical design provides a high impedance path between the DC supply and the RF network.
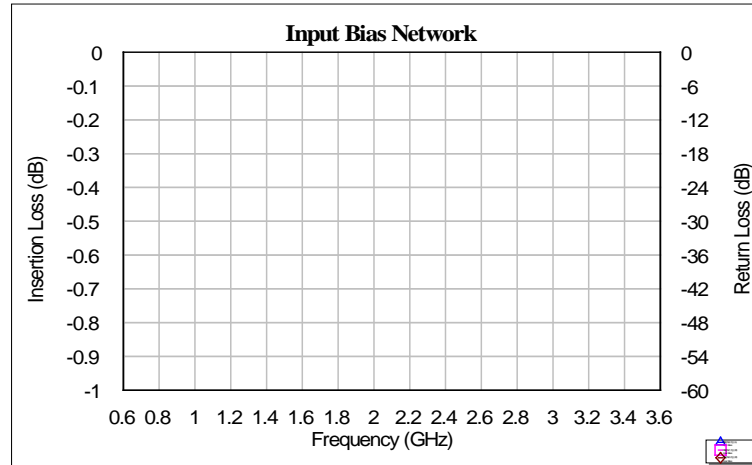
Input Bias Network

FIGURE 6-2: Input Bias Network

Output Bias Network
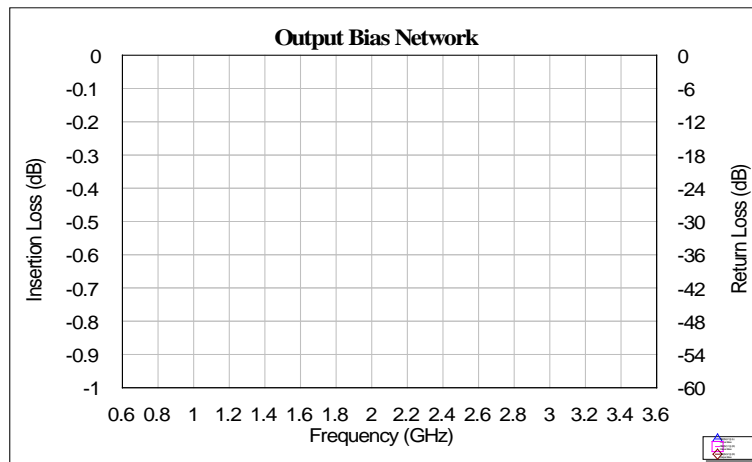
FIGURE 6-3: Output Bias Network

6.2   *Input Matching Circuit*

Implementing the ideal Class E amplifier design requires that the transistor is operated as a switch whereby the device is either enabled by conducting current, or disabled. Since the RF transistor is effectively a voltage controlled current source, this switch functionality can be provided by presenting a square voltage waveform to the device input. This input voltage characteristic can be provided by cascading a Class F driver amplifier with the Class E amplifier. Unfortunately, such a harmonically tuned amplifier design does not yield multi-octave RF

bandwidth capabilities necessary for the design. Therefore, a distributed input match is necessary to provide the wide bandwidth capabilities.

The input match design begins by determining the input impedance of the transistor when properly biased and terminated to the system impedance on both input and output. The bias condition was arbitrarily selected at $[I_{ds} = 0.25A]$ which corresponds to a gate voltage of $[V_{gs} = -2.7V]$ for the CGH60030D. The corresponding active input impedance is shown in FIGURE 6-4 and shows the device input impedance at center band $[F_c = 2.1GHz]$ is $[1.2 – j2.2]\Omega$.

To establish a broadband match, a low quality factor transformation ratio is necessary. This is achieved by cascading multiple transformer sections together yielding intermediate impedances between the transistor and the system characteristic impedance. The transformer used shall be a low-pass filter configuration consisting of a series inductor followed by a shunt capacitor. The actual component values are dependant on the operating frequency and the impedance step. The corresponding transformation ratio and component values are detailed by Asbeck [3] as:

$$Q_{trans} = \sqrt{R_{Load}/R_{source}} - 1$$

$$L_{inductor} = Q_{trans} * R_{source} / \omega$$

$$C_{capacitor} = Q_{trans} / R_{Load} * \omega$$

To achieve a low transformation ratio, the upper limit was arbitrarily set at a factor of about 1.5 which can be realized in the form of a 6 element low-pass filter. This reduces the transformation ratio from a high value of 6.3 which would be necessary if realized by a single low-pass section. The resulting tuning values are determined and shown in TABLE 6-1 with the matched input impedance shown in FIGURE 6-5.

TABLE 6-1: Initial Input Impedance Values

DESCRIPTION	SYMBOL	UNITS	INITIAL VALUE (Lumped Element)	FINAL VALUE (Lumped Element)	FINAL VALUE (Micro-Strip)
SECTION 1	L_1	nH	0.32	0.3	-
		mils	-	-	43
	C_1	pF	27.3	17.8	3.3
SECTION 2	L_2	nH	0.6	0.7	-
		mils	-	-	117
	C_2	pF	7.6	8.0	2.2
SECTION 3	L_3	nH	1.8	1.6	-
		mils	-	-	167
	C_3	pF	2.2	2.3	1.0

The matching conditions outlined thus far have provided a conjugate match at one discrete frequency. To extend the frequency capabilities, each input matching component is iteratively tuned until a more even impedance distribution is provided over the entire frequency range. The corresponding final lumped element component values are also detailed in TABLE 6-1 with the matched input impedance shown in FIGURE 6-6.

With the transistor output impedance terminated to 50Ω, the corresponding input impedance and associated small signal gain is modeled as shown FIGURE 6-8. Results show typical return losses of -6dB above 1.7GHz and small signal gain of 17dB across the evaluated frequency range. Due to bandwidth limitations, it proved extremely difficult to improve the return loss match at frequencies below 1.7GHz without significantly degrading the response above 3.5GHz.

The last step in the final input match design is to implement the lumped element components in a physical circuit environment. The final input match will consist of the matching components, bias networks and micro-strip to RF transistor transitions.
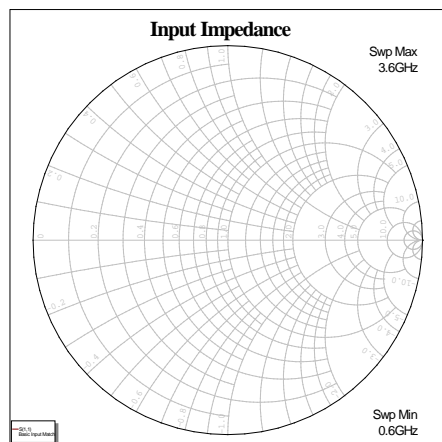
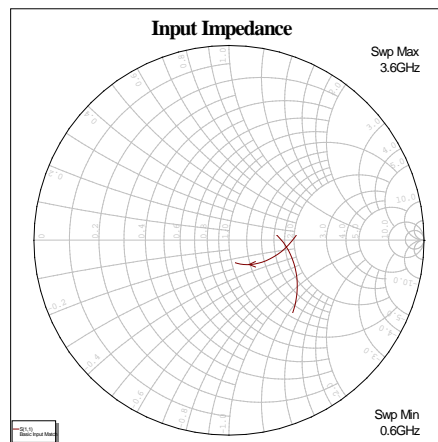FIGURE 6-4: Input Impedance (Un-Matched)   FIGURE 6-5: Input Impedance (Matched)
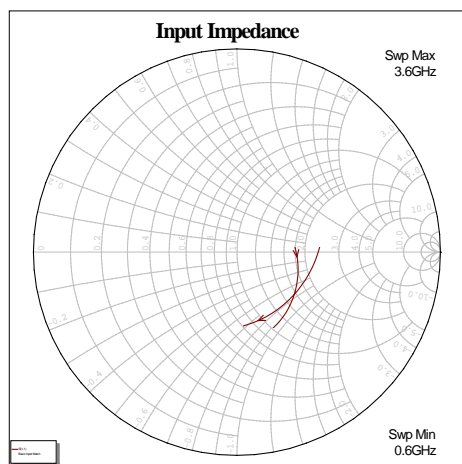

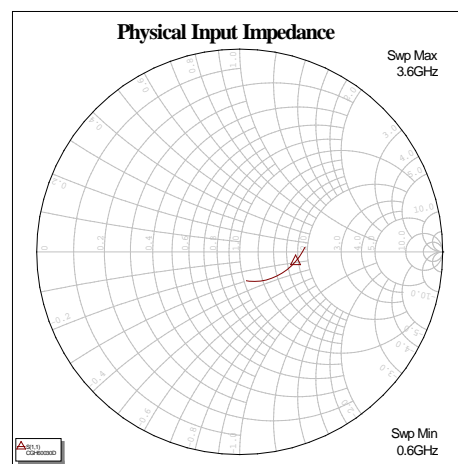FIGURE 6-6: Input Impedance (Optimized)   FIGURE 6-7: Input Impedance (Micro-Strip)
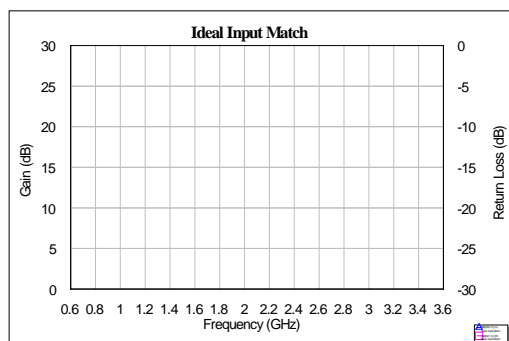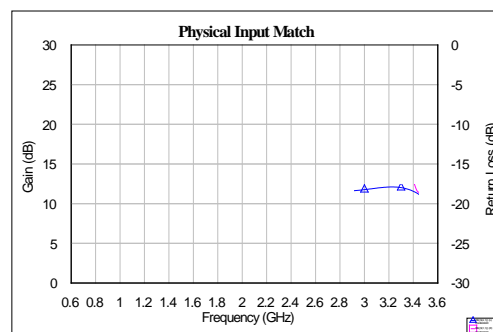

FIGURE 6-8: Small Signal (Lumped Tuning)   FIGURE 6-9: Small Signal (Micro-strip Tuning)

The input matching network inductors are to be approximated by micro-strip transmission lines with a particular line length printed on the substrates. Realizing the inductors on the substrates is preferred to implementing wire inductors to increase component quality factors and reduce manufacturing variation control. The shunt capacitors can be realized using single layer capacitors from DLI Dielectric Laboratories. Since the final design shall be used for demonstration of a physical prototype, the inductors will be realized by 50Ω micro-strip lines of specific length between shunt capacitors with the final tuning values summarized in TABLE 6-1 yielding modeled input impedances shown in FIGURE 6-7 and performances shown in FIGURE 6-9. The corresponding input impedance and associated small signal gain shows typical return losses of -2.2dB above 1.5GHz and typical small signal gain of 14dB.

6.3 Output Matching Circuit

The output impedance network shall be designed to support a reactance compensated Class E amplifier as outlined by Grebennikov [4] and [13] with the equations summarized in TABLE 6-2 and TABLE 6-3. Leveraging the peak output power capability from the transistor as indicated by the active component parameters summarized in TABLE 4-1, the output impedance network circuit component values are determined based on the formulas shown in TABLE 6-3.

With the operating characteristics determined, the circuit component values are derived based on the desired center-band operating frequency. The intended frequency range for the design shall extend between 600MHz through 2400MHz. Since the reactance compensation Class E design can support bandwidths in excess of 40%, a total of three individual bands will be necessary. A fourth band shall be considered in the analysis where possible to show the expected performance beyond which the ZVDS condition can be satisfied. The corresponding bands are divided as follows:

Band 1: [0.6 to 0.9] GHz→F_{center} = 0.75GHz

Band 2: [1.0 to 1.5] GHz→F_{center} = 1.25GHz

TABLE 6-2: Design Operating Conditions for Reactance Compensation Class E

DESCRIPTION	SYMBOL	UNITS	VALUE	FORMULA
Maximum Power	P_{out}	W	32	$1/4\ [I_{dss} * (V_{ds} - V_{min})]$
Load Impedance	R_L	Ω	33	$1.365 * (V^2_{dc} / P_{out})$
Peak Voltage	V_{pk}	V	102	$3.647 * V_{dc}$
Peak Current	I_{pk}	A	-	$2.647 * I_{dc}$
Frequency Limit	F_{max}	GHz	2.5	$0.0798 * [P_{out} * (C_{ds} * V_{dc}^2)^{-1}]$

TABLE 6-3: Ideal Component Values for Reactance Compensation Class E Operation

DESCRIPTION	SYMBOL	UNITS	BAND 1	BAND 2	BAND 3	BAND 4	FORMULA
Series Inductor	L_s	nH	7.2	4.3	2.7	1.8	$1.026 * (RL / \omega)$
Series Capacitor	C_s	pF	6.3	3.8	2.4	1.6	$(\omega^2 L_s)^{-1}$
Shunt Inductor	L_p	nH	5.1	3.1	1.9	1.3	$0.732 * (R_L / \omega)$
Shunt Capacitor	C_p	pF	4.4	1.8	0.4	0.0	$0.685 * (\omega R_L)^{-1}$

Band 3: [1.6 to 2.4] GHz➔F_{center} = 2.00GHz

Band 4: [2.5 to 3.6] GHz➔F_{center} = 3.00GHz

Utilizing each the center frequency of each band, the corresponding output network component values are determined and summarized in TABLE 6-3. The parallel resonant circuit capacitance "C_p" is compensated to absorb the transistor drain capacitance after reactive loading.

6.4 *Ideal Amplifier Performance*

The idealized Class E power amplifier design for the CGH60030D transistor was evaluated with the input and output impedance network circuits. For the output impedance network, each of the series and shunt resonator circuit elements were exclusively applied into the network for the evaluated frequency band. The output network is highly idealized because no transmission lines are implemented, selected components have infinite quality factors and the load impedance is purely resistive over all frequencies. The model serves as a baseline by which the maximum achievable efficiency can be established for the implemented Class E design.
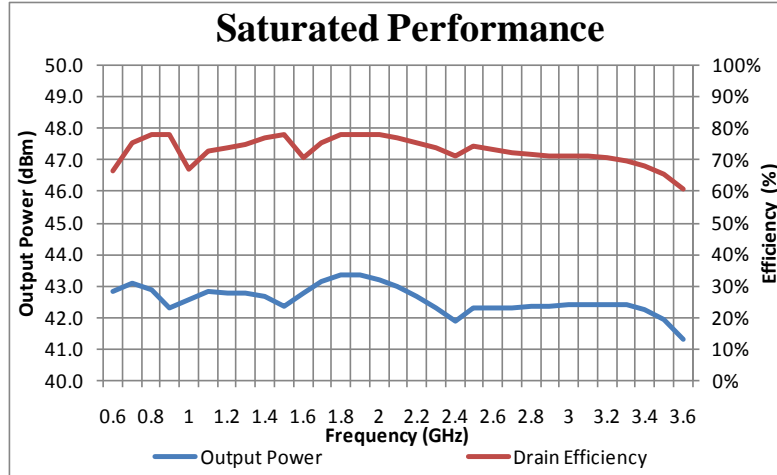
FIGURE 6-10: Multi-Band Class E Amplifier Performance

The corresponding simulation results show a composite performance response from all four bands in FIGURE 6-10. The average efficiency from the power amplifier is 75% over the target bandwidth with an average output power of +42.8dBm (19W). The corresponding power gain and power added efficiency is illustrated in FIGURE 6-11 with an average gain of 13.5dB and an average power added efficiency of 71%.

FIGURE 6-11: Multi-Band Class E Amplifier Power Gain and PAE

Based on the ideal Class E amplifier, the impedance environment presented to the RF transistor from the output impedance network was evaluated and summarized in TABLE 6-4. The output impedance environment up to the fourth harmonic was considered with the equivalent transistor model detailed in FIGURE 4-3 to show the impedances seen at the transistor drain. The transistor is presented an inductive load impedance which is sustained through each bands frequency range. Additionally, the transistor is presented capacitive impedances at harmonic frequencies which help facilitate a harmonically tuned impedance environment and meeting the design objectives for a reactively compensated Class E amplifier.
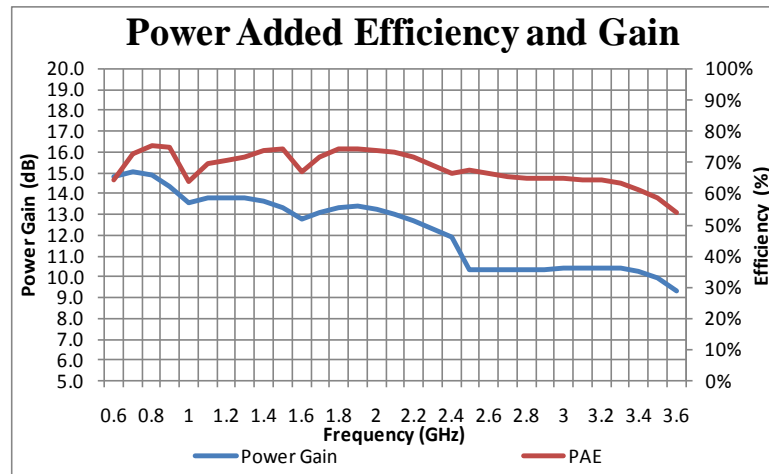
TABLE 6-4: Multi-Band Class E Output Network Characteristics

FREQUENCY		HARMONIC IMPEDANCE							
		FUNDAMENTAL		SECOND		THIRD		FOURTH	
	GHz	Re{Zin}	Im{Zin}	Re{Zin}	Im{Zin}	Re{Zin}	Im{Zin}	Re{Zin}	Im{Zin}
BAND 1	0.6	28	18	52	-27	3	-22	0.6	-13
	0.7	29	12	20	-38	1	-16	0.3	-10
	0.8	30	10	7	-29	1	-13	0.1	-9
	0.9	34	10	3	-22	0.3	-11	0.1	-7
BAND 2	1.0	29	18	50	-27	3	-22	0.5	-13
	1.125	29	12	26	-39	1	-17	0.3	-11
	1.25	29	10	11	-33	1	-14	0.2	-9
	1.375	31	10	5	-26	0.5	-12	0.1	-8
	1.5	35	10	3	-22	0.3	-11	0.1	-7
BAND 3	1.6	28	18	46	-30	2	-19	0.4	-11
	1.8	29	12	21	-37	1	-15	0.2	-9
	2	29	11	9	-30	1	-12	0.1	-7
	2.2	31	10	4	-24	0.4	-10	0.1	-6
	2.4	35	10	2	-19	0.2	-9	0.1	-5
BAND 4	2.6	34	6	9	-24	1	-10	0.0	-1
	2.8	33	3	5	-21	0.4	-8	0.1	-4
	3	33	1	3	-18	0.2	-7	0.1	-3
	3.2	34	-1	2	-15	0.2	-6	0.1	-3
	3.4	35	-3	1	-13	0.1	-5	0.0	-2
	3.6	37	-7	1	-12	0.1	-5	0.0	-2
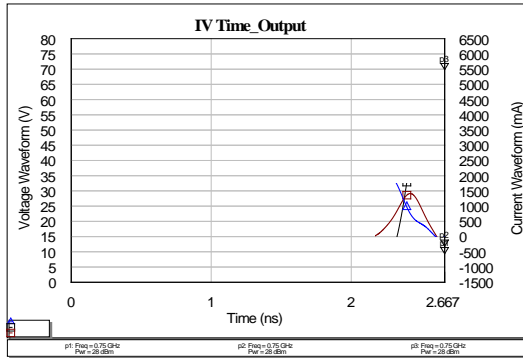
FIGURE 6-12: Voltage and Currents (Band 1) FIGURE 6-13: Voltage and Currents (Band 2)
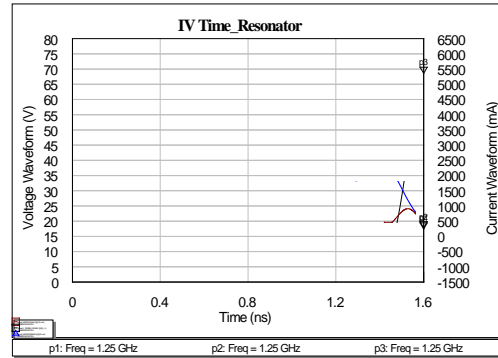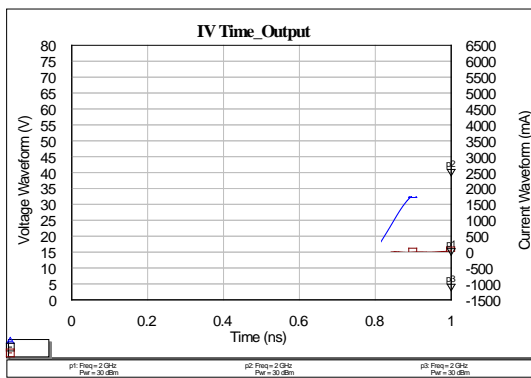
FIGURE 6-14: Voltage and Currents (Band 3) FIGURE 6-15: Voltage and Currents (Band 4)
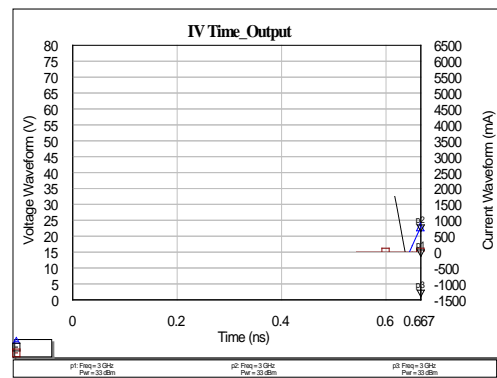
Lastly, to ensure the CGH60030D is operated as a Class E amplifier, the time domain drain voltage and current waveforms are evaluated and shown in FIGURE 6-12 through FIGURE 6-15 for the center of each band. The voltage and current waveforms closely resemble the desired Class E responses. Additionally, the load current is sustained through the parallel resonator capacitor as the transistor current drops below zero. An interesting observation is that the transistors drain currents drops below zero for a certain time period by which the parallel resonator capacitor begins to source current. This is caused by the transistor "C_{ds}" which could not be evaluated outside of the locked transistor model.

6.5   Output Impedance Transformer

The Class E amplifier circuit design is predicated on presenting a 33Ω load impedance to the output impedance network. To physically realize the design requirement, it will be necessary to transform the desired load impedance to the system characteristic impedance of 50Ω over the operating frequency range. Realizing the impedance transformation over multi-octave RF bandwidths requires a multi-section transformer as was implemented in the input matching circuit. Each section can be physically implemented using a lumped element low-pass filter approach, or by utilizing quarter-wave micro-strip transformers.

A distributed lumped element approach has the benefit of very small space requirements, however low component quality factors and large manufacturing tolerances result in high losses making it impractical in maintaining high efficiency. Alternatively, quarter-wave micro-strip transformers require larger form factors, but exhibit low loss mechanisms and can be made with higher manufacturing tolerance control. This design implementation provides the best approach for the multi-band high efficiency power amplifier.

The transformer is realized by achieving a low quality factor transformation ratio between each section. The simplest impedance steps are determined using the Binomial multi-section matching transformer as outlined by Pozar [6]. This approach realizes a maximally flat pass-band response and a gradual reactance variation across the pass-band frequency. The disadvantage of using a Binomial transformer is that the relative bandwidth capability is smaller than alternative designs including a Chebychev transformer approach.

The design processes involved in realizing the appropriate impedance steps are also outlined in Pozar [6]. This includes determining each impedance steps reflection coefficient $[\Gamma_n]$ and the total reflection coefficient $[\Gamma_N]$. Utilizing $[\Gamma_n]$, the overall reflection coefficient $[\Gamma(\theta)]$ can be determined based on the Binomial coefficient $[C^N_n]$ which is determined by the designs number of sections [N]. Subsitition back into the impedance steps reflection coefficient $[\Gamma_n]$,

provides the impedance of each section exclusively. The corresponding equations are detailed by

Pozar [6] as:

$$\Gamma_n = (Z_{n+1} - Z_n) / (Z_{n+1} + Z_n)$$

$$\Gamma_N = (Z_L - Z_N) / (Z_L + Z_N)$$

$$\Gamma(\theta) = \Gamma_0 + \Gamma_1 e^{-j2\theta} + \ldots + \Gamma_N e^{-j2N\theta}$$

$$= A(1 + e^{-j2\theta})^N$$

$$= A * \sum_{n=0}^{N} C_n^N e^{-j2n\theta}$$

$$|\Gamma(\theta)| = 2^N |A| \, |\cos(\theta)|^N$$

$$\theta = (2\pi/\lambda_g) * L_g$$

$$C_n^N = N! / (N - n)! * n!$$

$$A = 2^{-N} * \Gamma(0)$$

$$\Gamma(0) = (Z_L - Z_0) / (Z_L + Z_0)$$

The number of sections needed to realize the intended bandwidth can be derived by

setting an upper limit on the maximum desired pass band reflection coefficient [Γ_m], or

alternatively the return loss. Since the target is to achieve a near uniform response over the

intended frequency range, return loss limits were arbitrarily selected to be -15dB [$\Gamma_m = 0.177$].

Therefore, the minimum transformer order can be derived in Pozar [6] using the simplified

expression given as:

$$\Gamma_m = |A| * [2*\cos(-\pi/4*[(\text{Bandwidth} / F_{center}) - 2])]^N$$

$$N_{min} \rightarrow 4$$

Using the following initial conditions in conjunction with the design equations and

objectives detailed above, the corresponding Binomial impedance transformer parameters [C_n^N]

and [Γ_n] can be determined using the solved initial conditions [$\Gamma(0) = 0.205$] and [A= 0.013]. The

results can be used to find the desired impedance step [Z_n] yielding the characteristic impedance

of the quarter wave line [Z_{TL}]. Each section is to have an electrical length of ninety degrees

(quarter-wave) in the Alumina Oxide substrate [$\lambda_g/4$] at the center band frequency in order to accommodate a purely resistive transformation. Using the following initial conditions, the micro-strip transmission line design parameters were obtained by using the Rogers Corporation transmission line calculator [22] with the results summarized in TABLE 6-5.

The quarter-wave transformer pass-band performance was modeled and shown in FIGURE 6-16. The model provided an input impedance of 33Ω and an output impedance of 50Ω. It can be seen that the design yields the target return loss of -15dB with good symmetry around the center frequency while presenting a maximally flat pass-band response. Consequently, the typical insertion loss is 0.15dB is associated with the dielectric and conductor losses which reduce the output power by 3.4%.

Using the impedance transformer in-line with the transistor output impedance network and the system impedance, the power amplifier performance was re-evaluated as shown in FIGURE 6-17. Comparing the amplifier performance with the output transformer shows a typical power reduction of 0.13dB and a efficiency reduction of 2%. The pass-band response is sustained showing that the transformer is maintaining the desired impedance of 33Ω to the output network with negligible performance reduction.

TABLE 6-5: Binomial Transformer Design Parameters

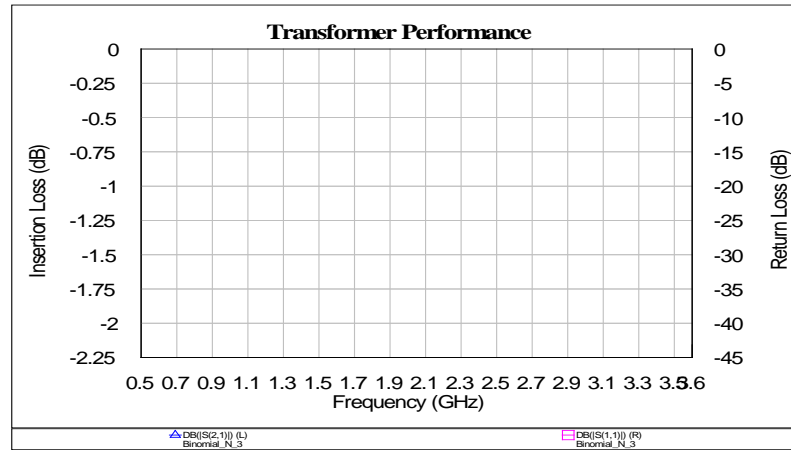| DESCRIPTION	SYMBOL	UNITS	SECTION 1	SECTION 2	SECTION 3	SECTION 4	FORMULA
Binomial Coefficient	C_n^N	nH	1	4	6	4	$N! / (N-n)! * n!$
Reflection Coefficient	$\Gamma(\theta)$	pF	0.01	0.05	0.08	0.05	$A * \sum_{n=0}^{N} C_n^N e^{-j2n\theta}$
Line Impedance	$Z_{n,TL}$	Ω	33.8	37.5	43.8	48.5	$(Z_{n+1} - Z_n) / (Z_{n+1} + Z_n)$
Line Width	W	mils	39.6	33.3	25.2	20.6	MWI - TX Line Calc
Line Length	L	mils	582	582	582	582	MWI - TX Line Calc

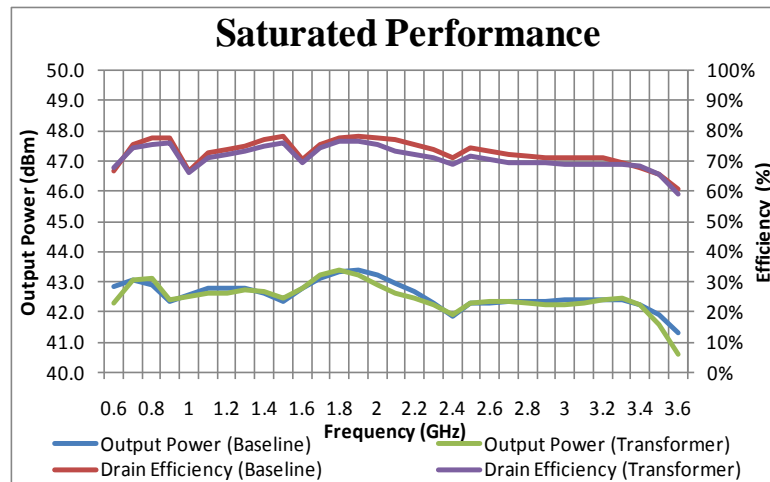FIGURE 6-16: Micro-strip Transformer Performance Characteristics

FIGURE 6-17: Multi-Band Class E Amplifier Performance with Output Transformer

CHAPTER 7

7. Multi-Band Series Switching Networks

Sustaining Class E operation requires a series resonator to be placed on the output network so that a purely sinusoidal current is delivered to the load. A sinusoidal load current is required so that when the transistor is off, the sinusoidal load currents are sustained by the output networks shunt capacitance. To support the multi-band output network approach, the design must provide a physically realizable, switchable series resonator network. This poses significant challenges due to the high frequency and high power levels associated with the design objective.

There are two switching options that can be used in series with the system load network. One option is to use Silicon PIN diode switches capable of supporting 30W of RF power over the intended frequency range. The second switch network can be achieved by utilizing transistor based RF switches. Evaluating RF transistor based switches from Peregrine Semiconductor [20] and Hittite Microwave Corporation [21] show that devices are commercially available that can handle the designs output power. However, neither RF switch proves as a good candidate due to high insertion losses in excess of 0.7dB above 2.4GHz and the need for external matching components.

RF switches are available from Aeroflex Metelics that can support high RF power levels in excess of 100W over the intended frequency range. There are two solutions available in the form of a single position dual throw (SPDT) or a single position three throw (SP3T) switch. To properly implement the switch on the output network, it is necessary to place a switch on both sides of the series resonator. Using two cascaded Aeroflex MSW2031-203 [23] SPDT switches on each side of the series resonator will support all four operating bands, however referencing the manufacturer datasheet shows that the combined insertion loss can be as high as 1.6dB (0.4dB

each) whereby adding 31% additional output losses and resulting in an average amplifier drain efficiency reduction of 24%. Alternatively, only one Aeroflex MSW3201-320 [24] SP3T switch can be used on each side of the series resonator to support the target frequency range. The net insertion loss can be as high as 1.0dB over the target frequency range whereby adding 20% additional output losses resulting in an average amplifier drain efficiency reduction of 15%.

The considered RF switches from Aeroflex Metelics are internally matched, series-shunt PIN diode switches yielding return losses better than -15dB. Unfortunately, Aeroflex does not publish any S-parameters, thereby the previous analysis assumes no impedance interaction from the switches to the output impedance network. This idealization cannot be supported with physical devices, therefore greater amplifier efficiency degradation would be expected due to impedance loading upon the series resonator.

To better approximate the impedance loading effects, a discrete solution PIN diode model was constructed based on the series-shunt circuit configuration as shown in FIGURE 7-1. This circuit configuration yields the best isolation at the expense of insertion loss as detailed by Radmanesh [7]:

Insertion Loss $= 20 \log_{10} | 0.5 + (Z_0 + Z_r) (Z_0 + Z_f) / 2Z_0Z_r |$

Isolation $= 20 \log_{10} | 0.5 + (Z_0 + Z_f) (Z_0 + Z_r) / 2Z_0Z_f |$

Z_0 $= $ Load characteristic impedance

Z_r $= R_r + j[\omega L_{int} - (1/\omega C_j)]$ (Diodes reverse bias impedance)

Z_f $= R_f + j\omega L_{int}$ (Diodes forward bias impedance)

The model shall use published S-parameters on a commercially available PIN diode, the M/A-COM MADP-030025-1314. This diode is in chip form, will support MIC manufacturing processes and has the following published properties within the product datasheet [8]:
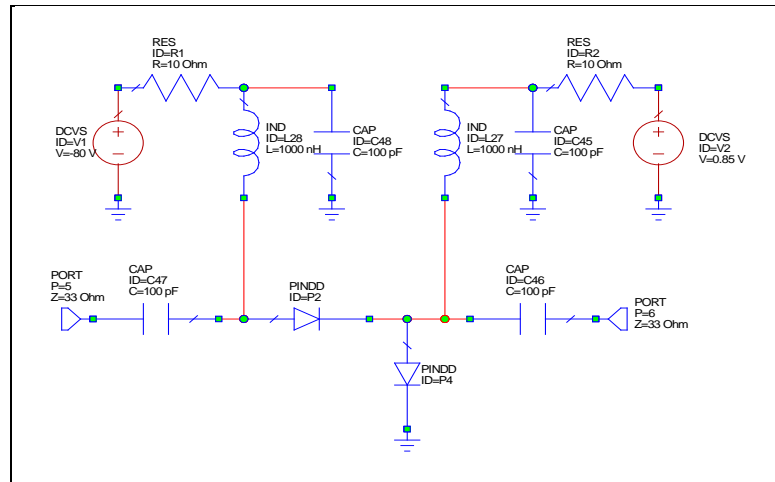
FIGURE 7-1: Series-Shunt Switch Network

Reverse Breakdown:	135V
Forward Current:	0.5A
Forward Power (CW):	+47dBm
R_{th}:	13 C/W
$C_j + C_{par}$:	0.5pF
R_f:	0.45 ohms

A PIN diode is similar to the conventional PN junction diode since applying a positive voltage across the device allows current to flow presenting an effective series resistance defining the on-state. Likewise, when a negative voltage is presented across the device, it becomes reverse biased presenting an effective capacitance defining the off-state. The basic circuit elements associated with a PIN diode includes the following parameters are discussed by Radmanesh [7]:

C_j → Junction Capacitance

R_r →Reverse Biased Resistance

R_f → Forward Biased Resistance

L_{int} → Series Inductor
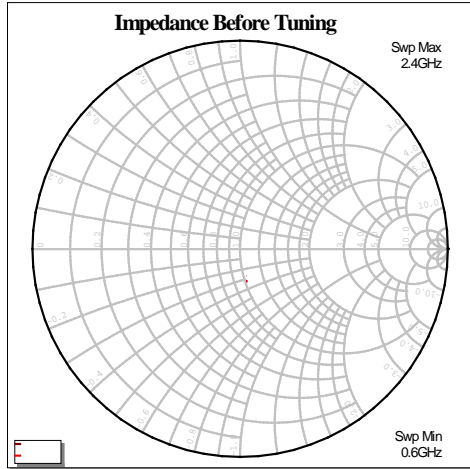
FIGURE 7-2: Diode Switch Impedance
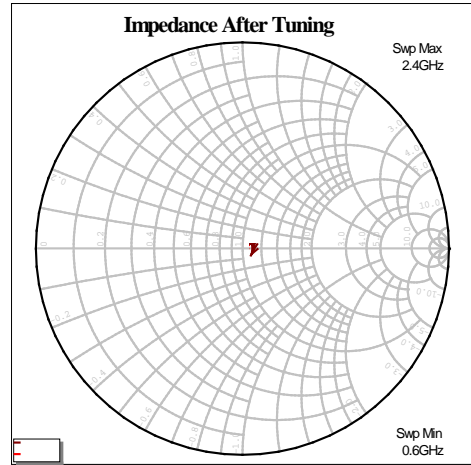
FIGURE 7-3: Diode Switch Impedance (Tuned)

A single series-shunt switch section input and output impedance was evaluated with the ports terminated to 33Ω. The input and output impedance is detailed in FIGURE 7-2 for the enabled switch configuration. Due to the diode parasitic capacitance $[C_j + C_{par}]$, tuning is required to present the desired characteristic impedance on both sides of the switch circuit. This is accomplished by placing a 1nH inductor prior to both ports and results in the tuned impedance environment as shown in FIGURE 7-3.

FIGURE 7-4: SP3T Schematic

FIGURE 7-5: Diode Switch Impedance   FIGURE 7-6: Diode Switch Impedance (Tuned)

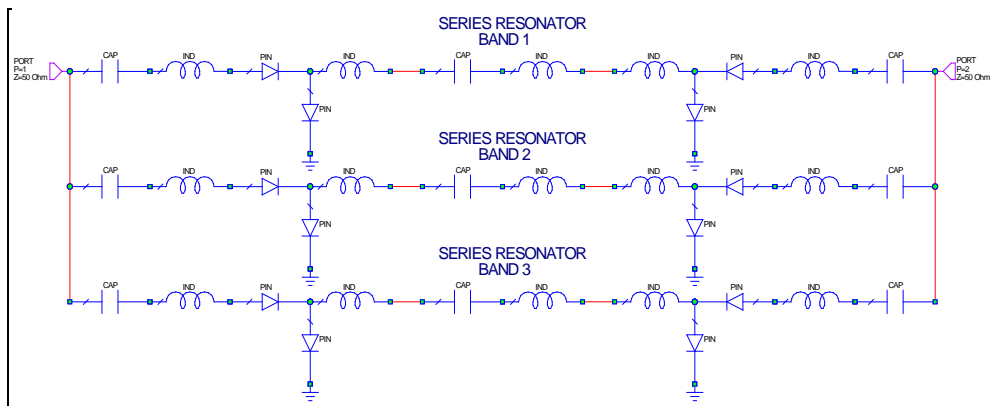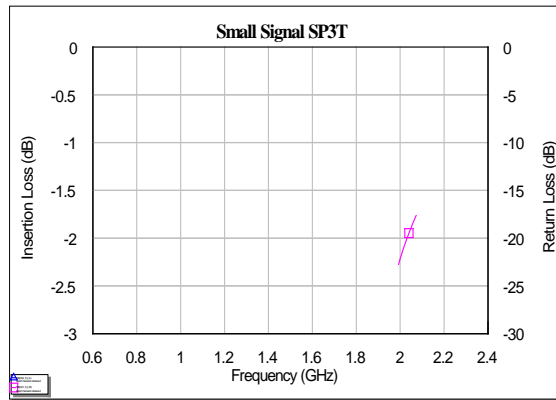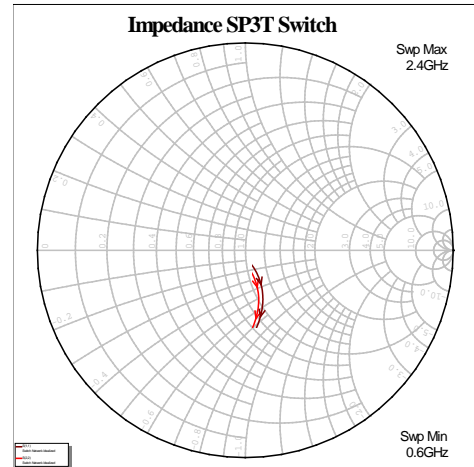The tuned switch was then cascaded into three branches with a common input and output port as shown in FIGURE 7-4. The corresponding small signal performance is detailed in FIGURE 7-5 and the impedances detailed in FIGURE 7-6. As can be seen, the interaction of the adjacent resonators mis-matches the desired band impedance characteristics. As a result, a degraded return loss and corresponding insertion loss is incurred.

With the series switch network discussed, the power amplifier performance was evaluated as shown in FIGURE 7-7. There are two effects present which are significantly reducing the efficiency of the power amplifier. The primary mechanism is the introduced insertion loss while the secondary mechanism is associated with the impedance loading effects on each series resonator. This is illustrated in the output impedance environment shown in FIGURE 7-8 through FIGURE 7-10 for Bands 1 through Band 3 respectively.
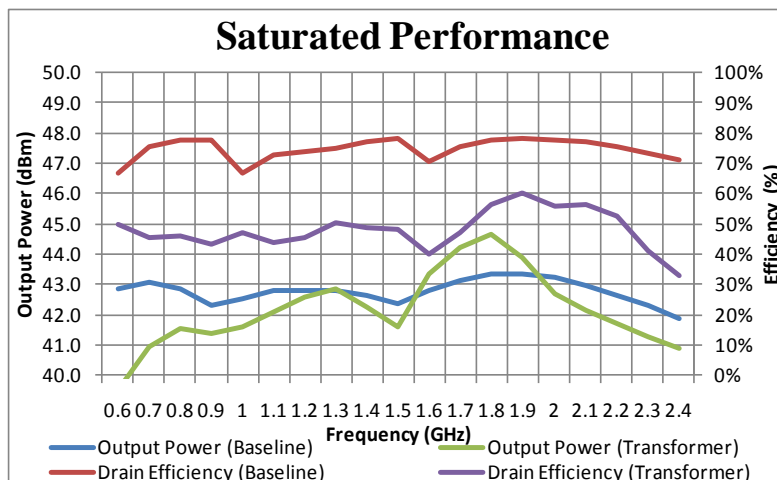
FIGURE 7-7: Class E Amplifier Performance with Switched Series Resonator

Implementing diode switches in the output network does not present a viable solution to switch in various series resonators. Compounded by the insertion loss attributed to each resonator, impedance matching cannot be sufficiently provided with minimal reactive loading to keep from degrading the efficiency and output power from the amplifier.
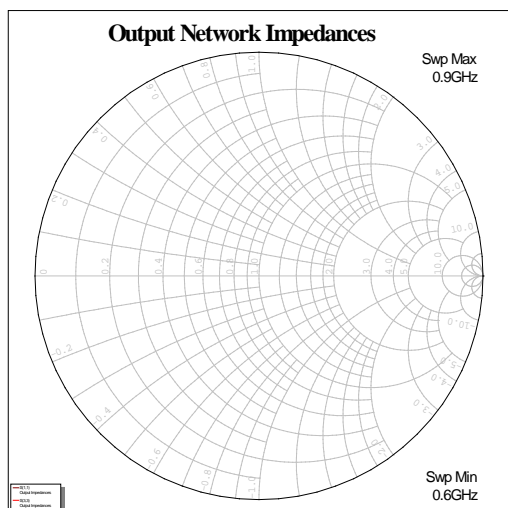
FIGURE 7-8: Output Impedance (Band 1)
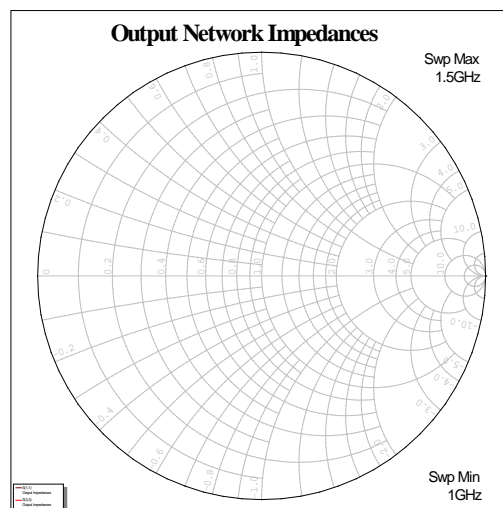
FIGURE 7-9: Output Impedance (Band 2)
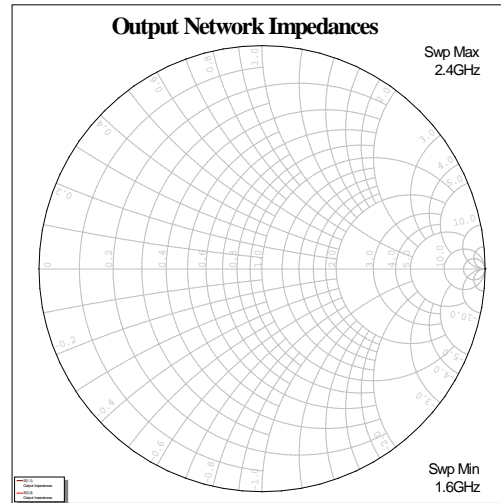
FIGURE 7-10: Output Impedance (Band 3)

Due to the challenges posed by including a switched series resonator on the output path of the power amplifier, the design performance was evaluated without any series resonator. Such a design implementation becomes a harmonically tuned power amplifier because ideally the shunt resonator network provides a harmonic short at all frequencies except at the fundamental operating frequency. The corresponding power amplifier saturated performance is shown in FIGURE 7-11 and the power gain and power added efficiency is shown in FIGURE 7-12. The results show that the average drain efficiency is 66% over the target frequency range exhibiting a degradation of 9% from the Class E design configuration. Output power and associated power gain is consistent between both configurations. Since performance can be maintained without the series resonator, the design moving forward will not include the network in any further analysis.

FIGURE 7-11: Multi-Band Power Amplifier Output Power and Drain Efficiency

FIGURE 7-12: Multi-Band Power Amplifier Power Gain and PAE

CHAPTER 8

8.   Multi-Band Shunt Switching Networks

The previous design processes were based on the Class E amplifier design proposed by Grebennikov [4] including series and shunt resonators. Due to the high output power levels associated with the design, a series resonator could not be implemented. Only the shunt switching network can be used for band selection whe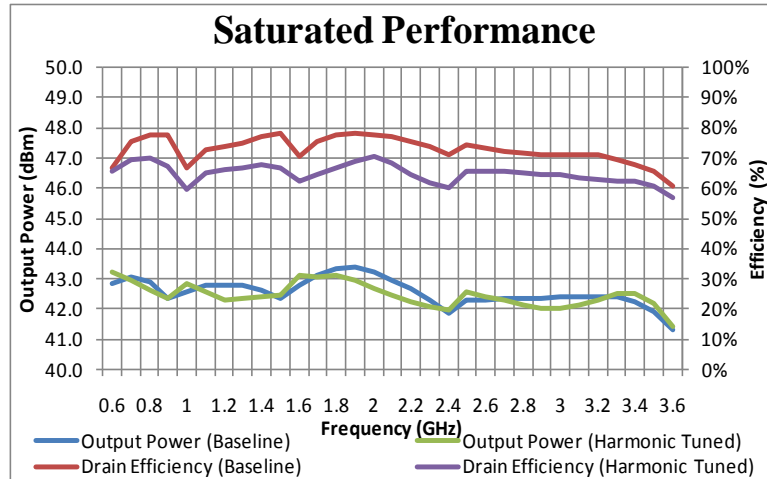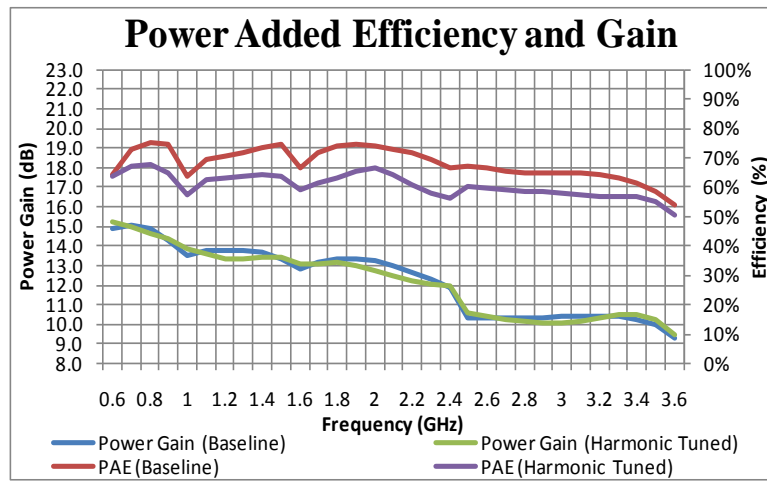reby high efficiency is provided by a harmonically tuned output network at the RF transistor. Amplifier performance can provide typical drain efficiencies of 66% over two RF bandwidth octaves.

To complete the design, electronic switching elements will be considered for the shunt parallel networks exclusively. It is necessary to provide a physically realizable element with low parasitic properties that can withstand the high power levels and high frequency objectives of the design. PIN diodes and RF transistor switch elements are considered the best technology choices for the switch element.

8.1   PIN Diode Switching

The PIN diode switch would be placed in-line with each parallel resonator and ground. When the diode is enabled, the resonator will be presented a ground reference. Likewise, when the diode is disabled, the diode will ideally present an open circuit between ground and the resonator. These design objectives require that the switch element parasitic resistance and capacitance should be very low to provide high off-state isolation and low on-state resistance.

Selection of the diode is ultimately predicated on the devices operating limitations. Therefore, selection of a diode that can support the peak voltage and current requirements for each resonator is necessary. To determine the operating requirements, the time domain characteristics are evaluated and subsequently shown in FIGURE 8-1 through FIGURE 8-4 for

the center of each band respectively. Under active conditions, it is determined that a peak voltage of +46V is present across the disabled resonators while the enabled resonator conducts peak currents of 1.4A. The peak voltage is effectively the peak drain voltage seen at the RF transistor, however due to the series decoupling capacitor placed on each resonator, the resonator voltage is offset by the drain voltage.

The peak current requirements through the shunt resonator require more current capability than can be provided by the M/A-COM MADP-030025-1314 diode considered for the series resonator. Therefore, a new silicon PIN diode from Aeroflex Metelics is selected for use as the shunt switch element. The diode is a custom part and comes as a Mesa PIN diode to facilitate MIC manufacturing processes. The diode has the following device properties as provided by the manufacturer [9]:

Reverse Breakdown: 250V

Forward Current: 2500A

C_j: 0.5pF

R_f: 0.3 ohms

To enable the diode for the appropriate resonator, a DC bias must be presented across the diode such that a specific current can be conducted across the device. Generally, the more current the device is allowed to conduct, the lower the on-state resistance becomes. Selection of the bias current can be determined based on the PIN diode resistance curve published in the manufacturer datasheet [9] and shown in FIGURE 8-5. From the curves, the optimal bias condition is 100mA which results in an on-state resistance of 0.2 ohms.
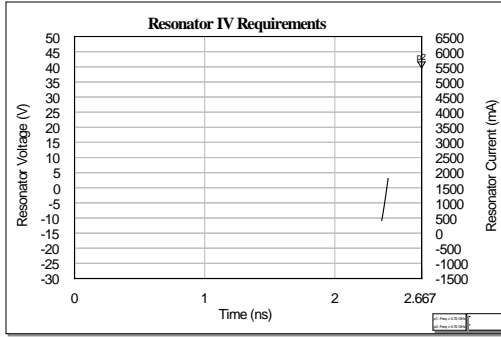
FIGURE 8-1: Voltage and Currents (Band 1)
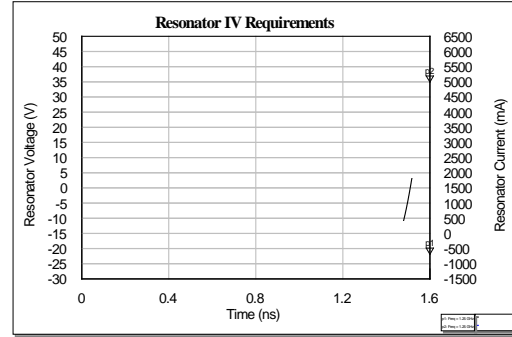
FIGURE 8-2: Voltage and Currents (Band 2)
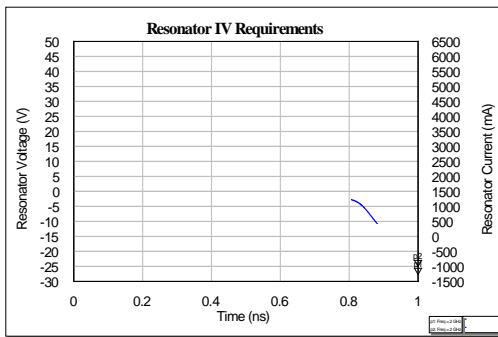
FIGURE 8-3: Voltage and Currents (Band 3)
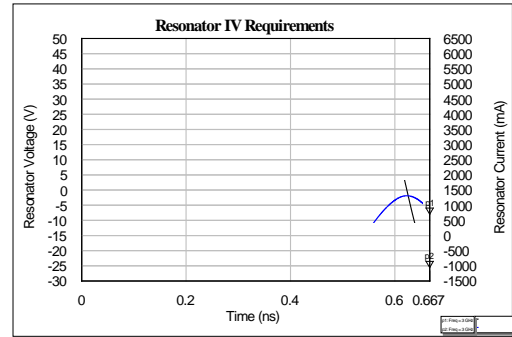
FIGURE 8-4: Voltage and Currents (Band 4)

The same bias network topology illustrated in FIGURE 7-1 is used for the shunt resonator diodes. When the device is enabled, current control is established across the bias network resistor with respect to the 0.85V forward voltage drop across the diode and the supply voltage. When the device is disabled, the diode will require a DC bias of at-least -47V to prevent forward biasing the device during operation. Current in the disabled state is governed by the reverse bias leakage.
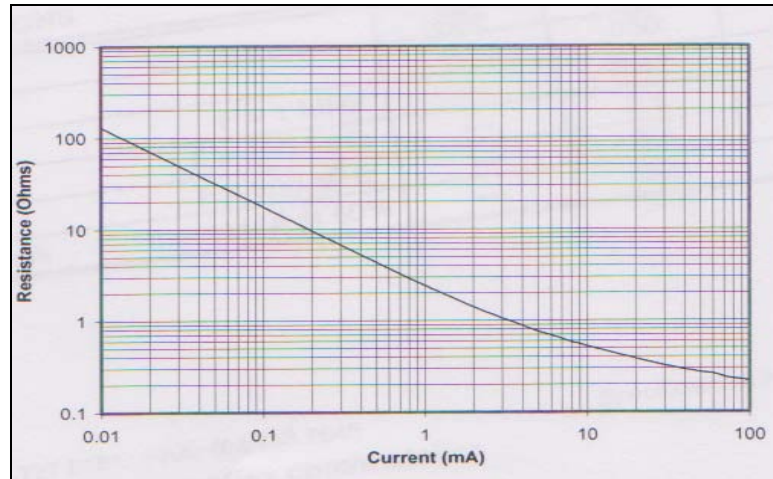
FIGURE 8-5: Aeroflex Metelics PIN Diode Resistance Bias Curve [9]

Ultimately, the bias condition will require additional power consumption through the system, however only one resonator is to be operated at any given time minimizing net power consumption. Considering that the forward voltage of the PIN diode is 0.85V, the minimum system voltage provided across the bias resistor should be 1.0V, thereby reducing the DC power requirement to 0.1W and thus contributing to a typical efficiency reduction less than 1%. Higher resistance values are ultimately desired to increase isolation between the RF network and the bias network under physical operating conditions.

S-parameter datasets for a representative PIN diode were obtained based on the appropriate bias state. One S-parameter dataset defined the on-state of the device with a forward current of 100mA and the second defined the off-state of the device with a reverse bias voltage of -40V. Both S-parameters were evaluated over a frequency range between 0.1GHz through 26GHz, thereby allowing consideration of the fundamental and harmonic impedance effects presented by the diode on the impedance network. The corresponding diode series impedance for both bias conditions is illustrated in FIGURE 8-6 and FIGURE 8-7, respectively.
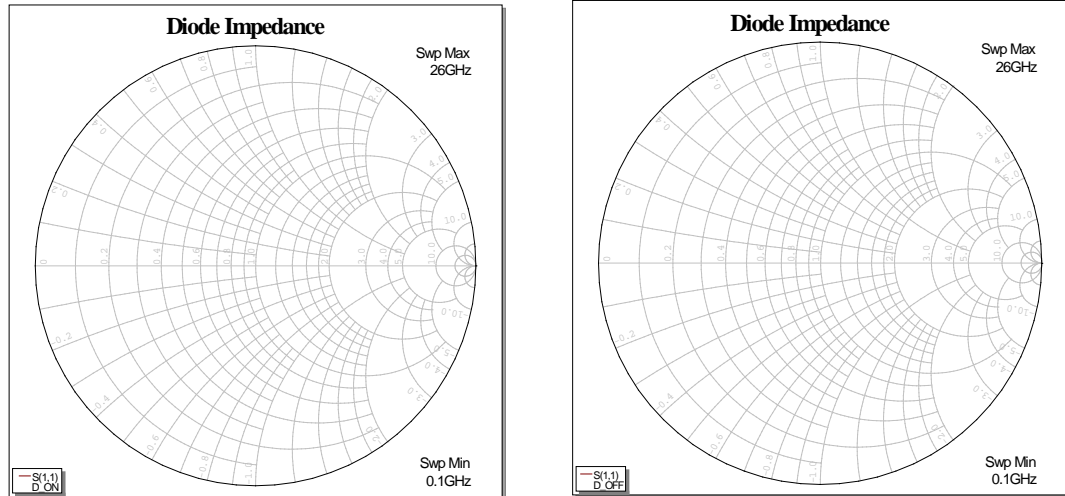
FIGURE 8-6: PIN Diode Impedance (100mA)   FIGURE 8-7: PIN Diode Impedance (-40V)

Within the harmonically tuned power amplifier model, each bands shunt resonator network was applied to the output impedance network with both S-parameter files placed as the element bridging the resonator to ground. When the performance for a specific band was evaluated, that bands on-state S-parameter file was enabled while each adjacent resonator had the off-state S-parameter file enabled. This provides the on-state characteristics to the resonator band evaluated and also includes the parasitic effects of the adjacent disabled resonators. The corresponding composite power amplifier performance is shown in FIGURE 8-8.

The performance from the power amplifier shows significant degradation in output power and efficiency. In all evaluated cases, the peak drain efficiency was shifted down frequency with respect to the appropriate bands frequency range. Furthermore, there are series resonances observed in Band 3 and Band 4 resulting in a power and efficiency reduction. Series resonances are the most detrimental type of resonance for this type of impedance network since it effectively presents a short circuit to the output impedance network at the resonant frequency. Evaluation of the output impedances seen at the transistor device shows that the Band 2 shunt resonator is presenting a series resonance at 1.75GHz resulting in an impedance of [2.7-j0.01] Ω. Likewise,

the Band 3 shunt resonator is presenting a series resonance at 3.19GHz resulting in an impedance of [1.7-j0.3] Ω.

Though the PIN diode presents significantly lower low parasitic characteristics than other switching element choices, it is still sufficiently high to degrade the performance of the amplifier. To recover the desired pass-band response, each parallel resonator will need to absorb the diodes parasitic contributions and present the same impedance environment used to evaluate the amplifier performance in FIGURE 7-11 and FIGURE 7-12. Therefore, a baseline impedance map is generated from the output network without the series resonator and is detailed in TABLE 8-1. The impedance map includes the equivalent transistor model to represent the impedance seen at the device drain.
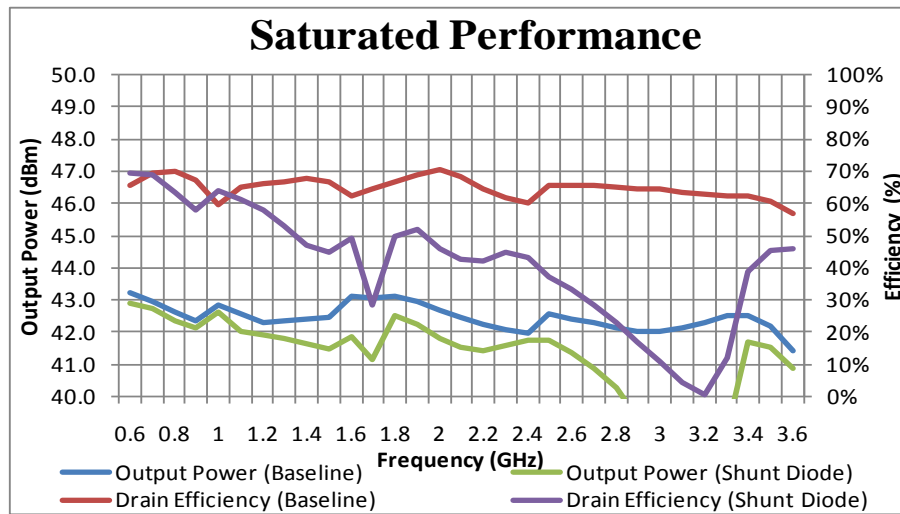

FIGURE 8-8: Power Amplifier Performance with Shunt Diode Switching

TABLE 8-1: Output Network Impedances

FREQUENCY		HARMONIC IMPEDANCE							
		FUNDAMENTAL		SECOND		THIRD		FOURTH	
	GHz	Re{Zin}	Im{Zin}	Re{Zin}	Im{Zin}	Re{Zin}	Im{Zin}	Re{Zin}	Im{Zin}
BAND 1	0.6	21	13	20	-16	8	-14	4	-10
	0.7	26	9	14	-16	5	-12	3	-9
	0.8	29	4	10	-15	4	-10	2	-8
	0.9	31	-2	8	-14	3	-9	2	-7
BAND 2	1.0	18	16	21	-17	7	-14	3	-11
	1.125	25	14	14	-16	6	-12	2	-8
	1.3	30	9	12	-15	4	-12	2	-8
	1.375	32	2	10	-15	2	-10	2	-7
	1.5	30	-3	7	-14	2	-8	1	-7
BAND 3	1.6	18	15	19	-15	6	-12	3	-9
	1.8	23	15	18	-16	4	-11	2	-8
	2.0	30	11	9	-19	3	-10	1	-7
	2.2	34	2	6	-14	3	-9	1	-6
	2.4	31	-5	6	-12	2	-8	1	-5
BAND 4	2.6	26	10	8	-14	2	-9	1	-5
	2.8	30	8	7	-13	1	-7	1	-4
	3.0	33	1	5	-12	1	-6	0.3	-3
	3.2	30	-4	4	-11	1	-6	0.3	-3
	3.4	28	-6	4	-10	1	-5	0.2	-2
	3.6	31	-8	3	-9	1	-4	0.1	-2

To absorb the diode parasitic capacitance contribution "C_D" in each disabled band, each resonator circuit inductor "L_x" and capacitor "C_x" will need to be re-tuned so that it ideally matches the impedance map shown in TABLE 8-1. This process begins by adding the series impedance from the diode [$Z_D = 1/j\omega C_D$] to the effective series resistance of the parallel resonator "$Z_{Cx||Lx}$". This yields the effective impedance from each resonator to the output network. The combined contribution can be determined by calculating the parallel impedance of two adjacent resonators. Subsequent resonators can then be calculated iteratively as the parallel contribution to the previously calculated resonator. The corresponding calculations are as follows:

$$Z_{Cx\|Lx} = j\omega L_x / (1 - \omega^2 C_x L_x)$$

$$Z_{res} = Z_D + Z_{Cx\|Lx}$$

$$= 1/j\omega C_D + j\omega L_x / (1 - \omega^2 C_x L_x)$$

$$= + j [(\omega^2 L_x(C_x+C_D) - 1) / (\omega C_D * (1-\omega^2 C_x L_x))]$$

$$Z_{res1\|res2} = (X_1 + jY_1) \| (X_2 + jY_2)$$

$$= (X_1 + jY_1) * (X_2 + jY_2) / (X_1 + jY_1) + (X_2 + jY_2)$$

Breaking down the real and imaginary impedance components of the equivalent resonator impedance is determined as:

$$Re\{Z_{res1\|res2}\} = [(X_1+X_2)(X_1X_2-Y_1Y_2)+(Y_1+Y_2)(X_1Y_2+X_2Y_1)] / [(X_1+X_2)^2+(Y_1+Y_2)^2]$$

$$Im\{Z_{res1\|res2}\} = [(X_1Y_2+X_2Y_1)(X_1+X_2)-(Y_1+Y_2)(X_1X_2-Y_1Y_2)] / [(X_1+X_2)^2+(Y_1+Y_2)^2]$$

Using the equivalent resonator impedance, each active band was re-tuned until the impedances were representative of output network without the diodes. The new parallel resonant circuit component values are thus determined and summarized in TABLE 8-2. With the optimized component values, the power amplifier saturated performance and power gain characteristics were re-evaluated as shown in FIGURE 8-9 and FIGURE 8-10, respectively.

TABLE 8-2: Tuned Parallel Resonator Components

DESCRIPTION	SYMBOL	UNITS	BAND 1	BAND 2	BAND 3
Initial Inductor	L_p	nH	5.1	3.1	1.9
Initial Capacitor	C_p	pF	4.4	1.8	0.4
Final Inductor	L_p	nH	4.6	2.2	1.1
Final Capacitor	C_p	pF	4.4	1.8	0.4
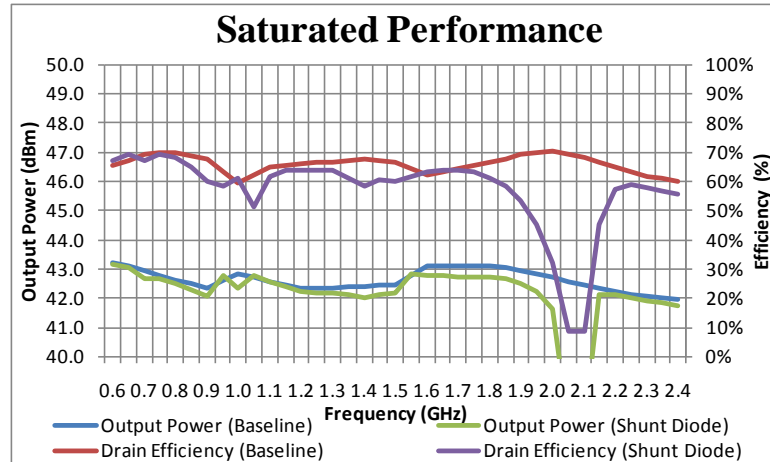
FIGURE 8-9: Power Amplifier Performance with Shunt Diode Switching (Optimized)

Using the optimized tuning component values, each bands performance is consistent with the initial baseline results showing a proper impedance environment with the diode switches included in the output network. The average power amplifier efficiency is 57% over the target frequency range exhibiting a degradation of 9% as evaluated without the switches. Output power and associated power gain is consistent between both configurations which is expected since the impedance environment has been appropriately compensated.
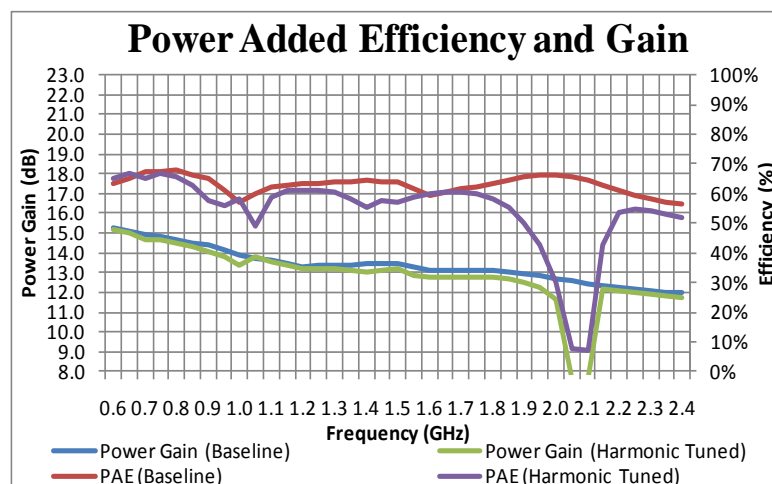

FIGURE 8-10: Power Amplifier Performance with Shunt Diode Switching (Optimized)

Unfortunately, the series resonances are still present from the shunt resonators resulting in additional performance degradation. Evaluation of the output impedances seen at the transistor device shows that the Band 1 shunt resonator is presenting a series resonance at 1.023GHz resulting in an impedance of [3.6+j0.5] Ω. Likewise, the Band 2 shunt resonator is presenting a series resonance at 2.076GHz resulting in an impedance of [2.4-j0.0] Ω.

8.2   *Transistor Switching*

RF transistors can be used as shunt switching elements for each parallel resonator since they permit high current control where the operational state can be defined by a voltage. These switching elements offer high frequency capabilities and low control power requirements.

Selection of the RF transistor is ultimately predicated on the devices operating limitations and associated parasitic attributes. Therefore, an RF transistor that can support the peak voltage and current requirements for each resonator is necessary. To determine the operating requirements, the time domain characteristics for each resonator are evaluated and subsequently shown in FIGURE 8-1 through FIGURE 8-4 for the center of each band respectively. Under active conditions, it is determined that a peak voltage of +46V is present across the disabled resonators while the enabled resonator conducts peak currents of 1.4A. The peak voltage is effectively the peak drain voltage seen at the RF transistor, however due to the series decoupling capacitor placed on each resonator, the resonator voltage is offset by the RF transistor drain bias.

Evaluating the operational limitations and parasitic attributes of the various transistor technologies summarized in TABLE 3-2, GaN again provides the best transistor technology solution for the switch element. This device technology is able to offer the lowest drain capacitance of any of the considered transistor technology that can withstand the peak resonator voltages associated with the design. A drawback of GaN transistors is that the devices tend to exhibit high on-state resistances which are attributed to higher potentials needed to allow electrons to conduct between the valence and conduction bands within the semiconductor. As

such, higher drain voltages are associated with higher currents and thus resulting in higher on-state resistances.

Selection of the RF transistor size is determined by the resonator current requirements. There is a natural trade-off in device selection where a smaller device is preferred to minimize the parasitic capacitance contribution. Alternatively, a larger device size is preferred to minimize the effective on-state resistance contribution from the part relative to the resonator current requirements. Consideration of the best transistor showed the CGH60015D provides the best trade-off for the design. The device presents an effective on-state resistance of 1.5Ω when conducting 1.4A of current as detailed in the device I-V curve shown in FIGURE 8-11.

Since a FET transistor is effectively a voltage controlled current source where the operating state is defined by the voltage presented to the gate, proper control of the RF transistor requires the device is sufficiently biased to permit strong inversion when enabled or deep sub-threshold when disabled as discussed in Kelly [11].
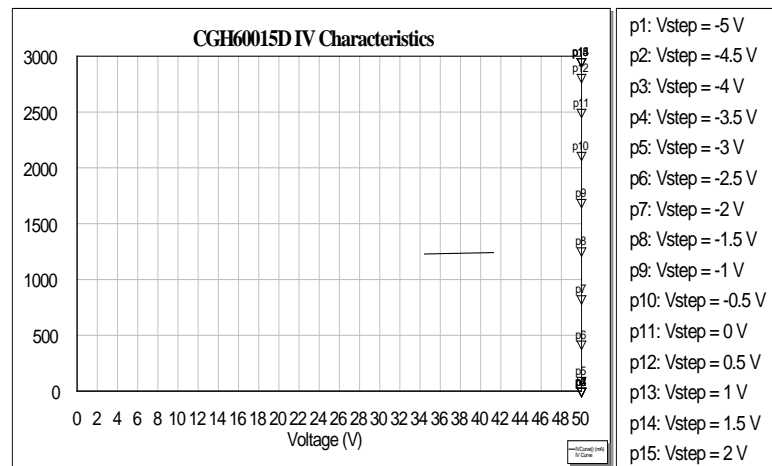

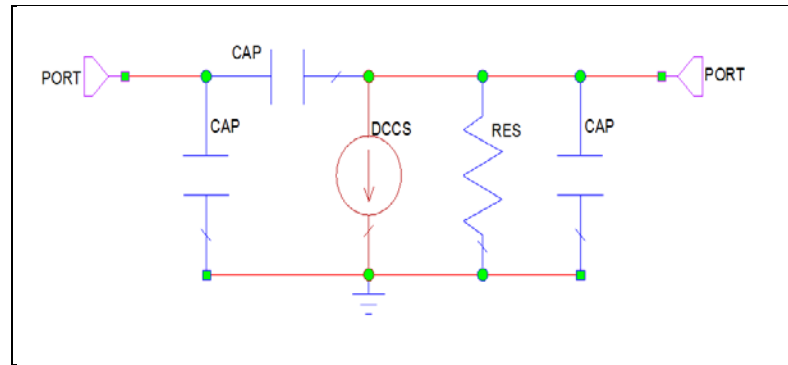FIGURE 8-11: CGH60015D I-V Characteristics

FIGURE 8-12: Simplified FET Model

These requirements are particularly critical in the disabled band resonators since the RF voltage signal present at the drain can enable the transistor if not properly biased. Evaluating the long channel equation of a FET operated in the "Triode" operating region [$I_d = k(V_{gs} - V_t - V_{ds}/2)$] shows that the device can be enabled if the relationship between the gate and drain voltages exceed [$V_d = 2(V_g - V_t)$]. Additionally, when considering the simplified FET model as shown in FIGURE 8-12, an AC voltage divider is present through "C_{gd}" and "C_{gs}" such that the AC voltage at the gate is represented as a function of the drain voltage by:

$$V_g = V_d * [C_{gd} / (C_{gd} + C_{gs})]$$

It can be assumed that each parasitic capacitor contribution from the CGH60015D is approximately half of the values indicated in TABLE 4-2 for the CGH60030D since the device output power capability is reduced proportionately. Therefore, as a result of the AC voltage divider created by "C_{gd}" and "C_{gs}", the drain induced gate voltage can be as high as +4.2V. Since the transistor pinch-off voltage was measured at -3.4V, the DC supply voltage must be -7.6V to guarantee the device will not begin to conduct current. This bias voltage provides a -2.4V margin from gate-drain breakdown.
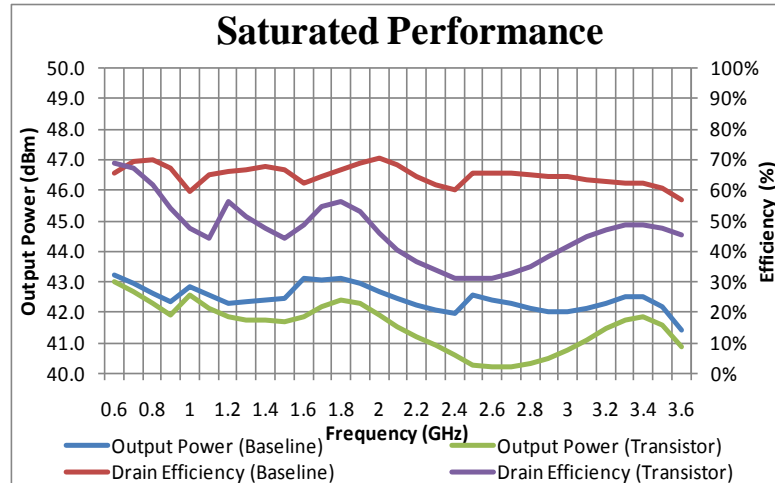
FIGURE 8-13: Power Amplifier Performance with Shunt Transistor Switching

Since each resonator is DC decoupled from the main RF path, the voltage across the resonator will reach up to -28V as illustrated in FIGURE 8-1 through FIGURE 8-4. Presenting a negative voltage across the transistor drain will cause forward conduction of the drain-source diode and cause the device to rectify the AC signal. This rectification causes current to conduct through the disabled resonator, enabling the undesired resonator and potentially resulting in transistor burn-out. Therefore, an AC coupled +28V supply needs to be presented to each disabled resonator transistor drain, while the +28V supply will need to be disabled for the enabled resonator. This additional circuit requirement adds complexity to the design as a separate drain voltage switch is needed for each transistor used.

Within the harmonically tuned power amplifier model, each bands shunt resonator network was applied to the output impedance network with the RF transistor model and bias networks implemented as the element bridging the resonator to ground. For each enabled resonator, the transistor gate was presented a bias of +1.0V to facilitate strong inversion. For each adjacent disabled resonator, the gate was presented a bias of -7.6V. The corresponding composite power amplifier performance is shown in FIGURE 8-13.

The performance from the power amplifier shows significant degradation in output power and efficiency. In all evaluated cases, the peak drain efficiency was shifted down frequency with respect to the appropriate bands frequency range. Furthermore, there are series resonances observed in Band 3 and Band 4 resulting in a power and efficiency reduction. Series resonances are the most detrimental type of resonance for this type of impedance network since it effectively presents a short circuit to the output impedance network at the resonant frequency. Evaluation of the output impedances seen at the transistor device shows that the Band 2 shunt resonator is presenting a series resonance at 1.69GHz resulting in an impedance of [0.6-j0.6] Ω. Likewise, the Band 3 shunt resonator is presenting a series resonance at 3.00GHz resulting in an impedance of [5.1+j0.06] Ω.

The primary amplifier performance degradation mechanism is associated with the disabled transistors parasitic capacitance. To recover the desired pass-band response, each parallel resonator will need to absorb the transistors parasitic contributions and present the same impedance environment used to evaluate the amplifier performance in FIGURE 7-11 and FIGURE 7-12. Therefore, a baseline impedance map is generated from the output network without the series resonator and is detailed in TABLE 8-1. The impedance map includes the equivalent transistor model to represent the impedance seen at the device drain.

To absorb the transistors parasitic capacitance contribution "Z_T" in each disabled band, each resonator circuit inductor "L_x" and capacitor "C_x" will need to be re-tuned so that it ideally matches the impedance map shown in TABLE 8-1. Approximating the contribution from the transistor begins by assuming that the equivalent series impedance from the transistor is governed by transistor capacitances and resistances "C_{gd}", "C_{gs}", "C_{ds}", "R_d", "R_s". The gate resistance is ignored since it is terminated through the RF choke which ideally presents high impedance to the transistor. The transistor equivalent capacitance and impedance can then be expressed as:

C_T $= Cds \parallel (Cgd + Cgs)$

         $= Cgd * Cgs / (Cgd + Cgs)$

         $= 1.0pF$

Z_T $= (R_d + R_s) + 1/j\omega C_T$

Determining the effective impedance of the resonator and transistor involves summing the resonator impedance "$Z_{Cx\parallel Lx}$" with the transistor impedance "Z_T". The combined contribution can be determined by calculating the parallel impedance of two adjacent resonators "$Z_{res1\parallel res2}$". Subsequent resonators can then be calculated iteratively as the parallel contribution to the previously calculated resonator. The corresponding calculations are as follows:

$Z_{Cx\parallel Lx}$ $= j\omega L_x / (1 - \omega^2 C_x L_x)$

Z_{res} $= Z_T + Z_{Cx\parallel Lx}$

         $= (R_d + R_s) + 1/j\omega C_T + j\omega L_x / (1 - \omega^2 C_x L_x)$

         $= (R_d + R_s) + j \, [(\omega^2 L_x(C_x + C_T) - 1) / (\omega C_T * (1 - \omega^2 C_x L_x))]$

$Z_{res1\parallel res2} = (X_1 + jY_1) \parallel (X_2 + jY_2)$

         $= (X_1 + jY_1) * (X_2 + jY_2) / (X_1 + jY_1) + (X_2 + jY_2)$

Breaking down the real and imaginary impedance components of the equivalent resonator impedance is determined as:

$Re\{Z_{res1\parallel res2}\}$ $= [(X_1+X_2)(X_1X_2-Y_1Y_2)+(Y_1+Y_2)(X_1Y_2+X_2Y_1)] / [(X_1+X_2)^2+(Y_1+Y_2)^2]$

$Im\{Z_{res1\parallel res2}\}$ $= [(X_1Y_2+X_2Y_1)(X_1+X_2)-(Y_1+Y_2)(X_1X_2-Y_1Y_2)] / [(X_1+X_2)^2+(Y_1+Y_2)^2]$

TABLE 8-3: Tuned Parallel Resonator Components

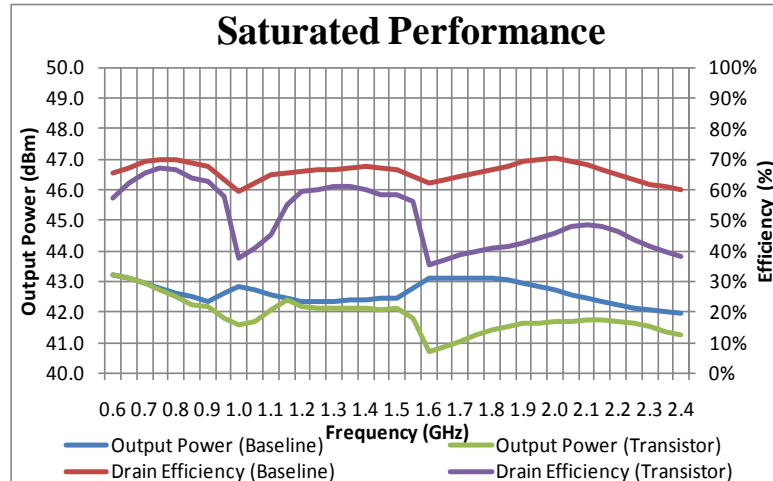| DESCRIPTION	SYMBOL	UNITS	BAND 1	BAND 2	BAND 3
Initial Inductor	L_p	nH	5.1	3.1	1.9
Initial Capacitor	C_p	pF	4.4	1.8	0.4
Final Inductor	L_p	nH	4.0	2.2	1.8
Final Capacitor	C_p	pF	4.4	1.8	0.4

FIGURE 8-14: Power Amplifier Performance with Shunt Diode Switching (Optimized)

Using the equivalent resonator impedance, each active band was re-tuned until the impedances were representative of output network without the transistors. The new parallel resonant circuit component values are thus determined and summarized in TABLE 8-3. With the optimized component values, the power amplifier saturated performance and power gain characteristics were re-evaluated as shown in FIGURE 8-14 and FIGURE 8-15, respectively.
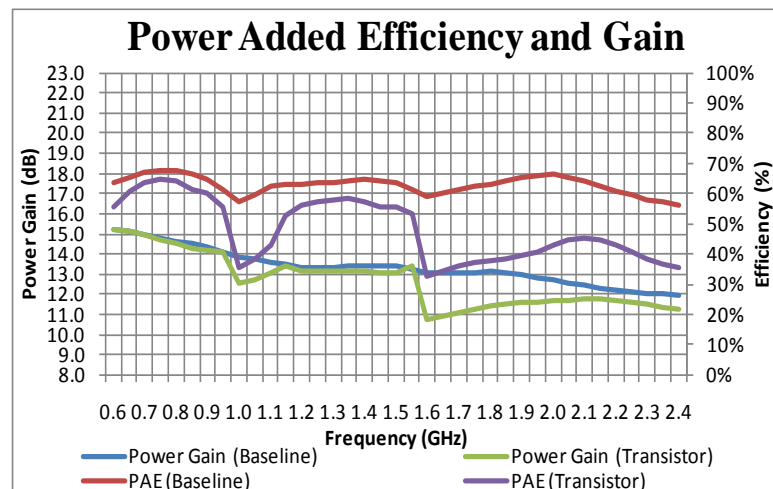

FIGURE 8-15: Power Amplifier Performance with Shunt Diode Switching (Optimized)

Using the optimized tuning component values, Band 1 and Band 2 performance is consistent with the initial baseline results showing a proper impedance environment with the diode switches included in the output network. Band 3 performance shows significant degradation. The average power amplifier efficiency is 51% over the target frequency range exhibiting a degradation of 15% as evaluated without the switches.

Unfortunately, the series resonances are still present from the shunt resonators resulting in additional performance degradation. Evaluation of the output impedances seen at the transistor device shows that the Band 1 shunt resonator is presenting a series resonance at 1.093GHz resulting in an impedance of [0.6-j0.5] Ω. Likewise, the Band 2 shunt resonator is presenting a series resonance at 2.006GHz resulting in an impedance of [0.6-j0.2] Ω.

CHAPTER 9

9.   Measurements

Utilizing the design processes outlined for the Multi-Band High Efficiency Power

Amplifier without the series resonant circuit, a prototype fixture was developed. The prototype

fixture utilizes commercially available components and standard MIC manufacturing processes to

validate the simulation results. The prototype fixture is referenced to a system characteristic

impedance of 50Ω on both input and output ports using coaxial to micro-strip transition. The final

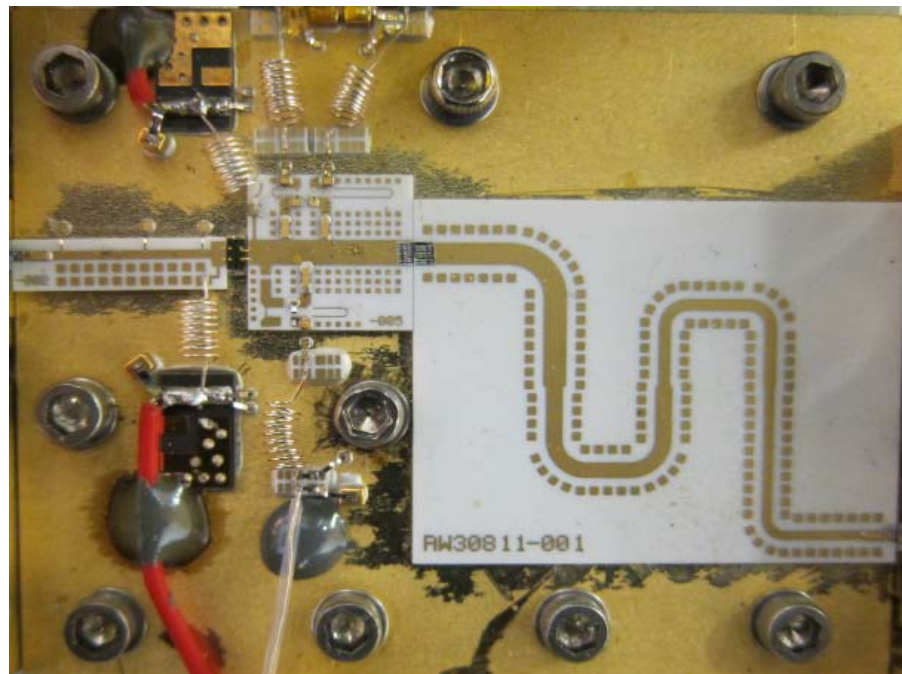prototype fixture is shown in FIGURE 9-1.

FIGURE 9-1: MIC Prototype Fixture

9.1 Test Environment

The prototype test fixture was evaluated for its small signal and large signal functionality. To conduct the tests, appropriate power supplies, driver amplifiers and test equipment were used as outlined within FIGURE 9-2.

The transistor gate bias was provided from a single power supply which presented a potential of [V_{gs} = -2.668V] resulting in an [I_{dq} = 0.25A] from the CGH60030D device. Drain bias was provided by a single power supply capable of sourcing 2.5A of current with a potential of [V_{ds} = +28V].
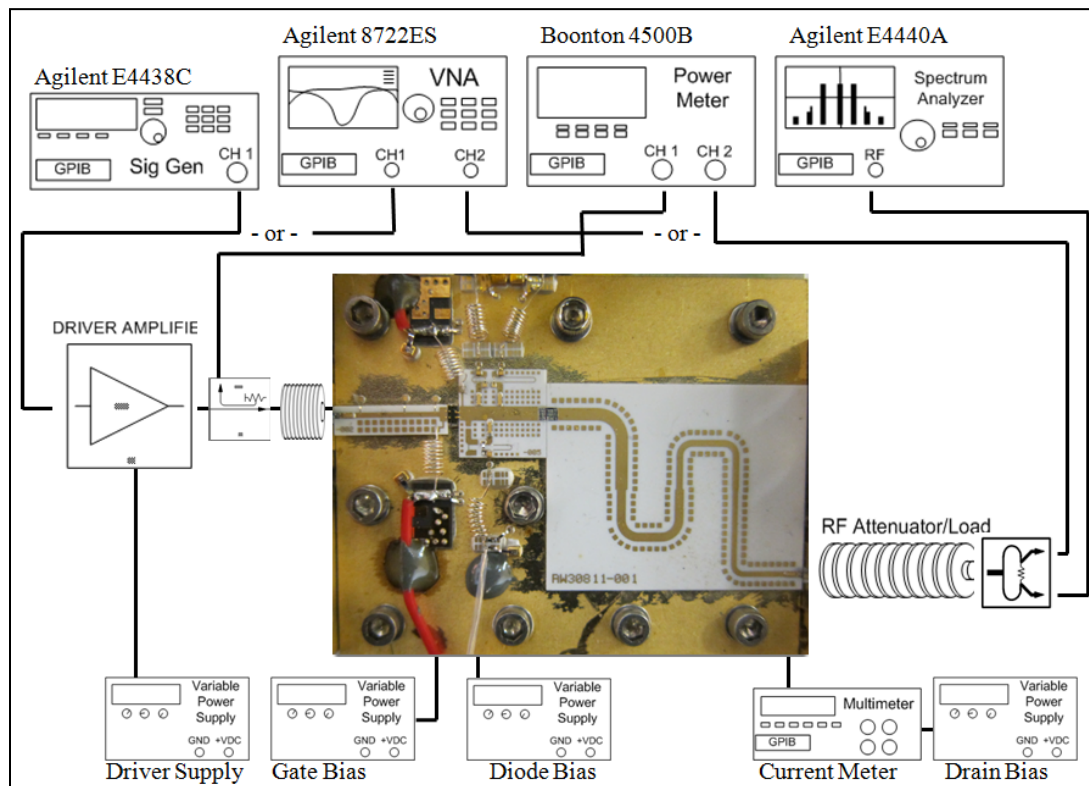

FIGURE 9-2: Prototype Test Setup

Each enabled diode was provided a [V_d = +5.0V] power source through a 42Ω bias resistor. The bias resistors allowed 0.1A of supply current to forward conduct the diode. Each disabled diode was provided a [V_d = -81.0V] power source from a common power supply across the 42Ω resistor.

Small signal measurements including port impedances were conducted using the Agilent 8722ES Vector Network Analyzer (VNA). Each measurement was conducted directly at the input and output port of the prototype test fixture. Power measurements were conducted using the Agilent E4438C signal generator, Boonton 4500B dual power meter, Agilent E4440A spectrum analyzer, driver amplifier, directional coupler, attenuators and power dividers. The signal began at the signal generator which provided a CW signal to a driver amplifier.

The output of the driver amplifier passed to a 40dB directional coupler which passed the signal to a buffer 6dB attenuator while providing a sample of the driver output power to the power meter. The buffer attenuator padded the output impedance of the driver amplifier and the input impedance of the prototype fixture to reduce VSWR interaction. The prototype fixture then amplified the signal based on the desired operational band. The output signal was then passed to a 40dB attenuator which fed a resistive power divider. The resistive power divider was connected to the power meter and the spectrum analyzer for simultaneous measurements of output power and harmonic content. Device current was measured using a current meter in-line with the prototype fixture and the drain power supply.

Two different driver amplifiers were used in the test depending on the tested frequency. The first driver amplifier was a GaAs based unit capable of providing +43dBm (20W) across the frequency range extending between 0.6GHz to 2.0GHz. The second driver amplifier was a GaN based unit capable of providing +47dBm (50W) across the frequency range extending between 2.0GHz to 2.4GHz.

9.2   *Physical Model*

Using the development process outlined, a physical model was constructed for all discussed elements of the Multi-Band High Efficiency Power Amplifier. The final model consisted of over 200 circuit elements including the physical implementation of the bias networks, input impedance network, output impedance network and impedance transformer. The final model is detailed in FIGURE 9-3.

DC blocking capacitors used shall be the DiLABS GapCap part number G15BV680K5MX10. This series of capacitors permits component attachment between two circuit points requiring DC isolation without the need for bond wires or ribbons. The component is electrically equivalent to two series capacitors and provides a net capacitance of 68pF with a voltage breakdown limit in excess of 50V.
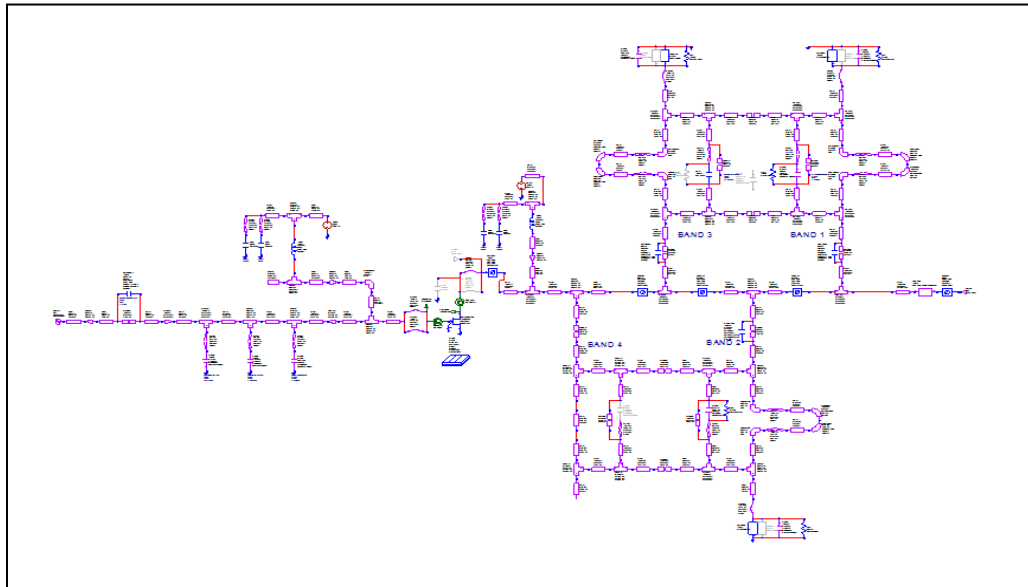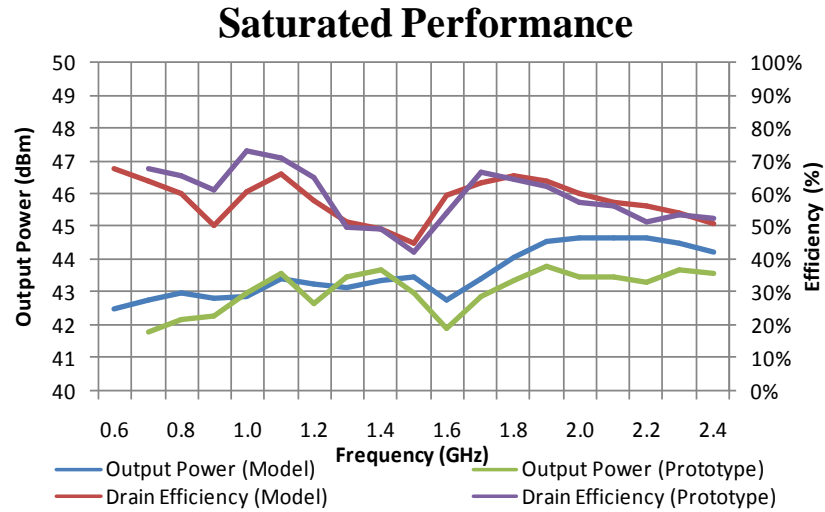

FIGURE 9-3: Physical Model

Saturated Performance

FIGURE 9-4: Prototype Saturated Performance

9.3   *Prototype Results*

The objective of the prototype is to demonstrate the power amplifier performance over three operating bands covering the target frequency range between 0.6 to 2.4GHz. Performance results are correlated to the physical model results and model deviations identified. Inherent to the physical model and idealized model detailed in subsequent sections, an expected shift in performance is expected. Prototype results are thus validated to the physical model exclusively to identify model attributes which were not explicitly identified to bring the two measurements into closer agreement.

The prototype efforts have been conducted in piecewise approach where initial efforts evaluated the prototype performance without diode switches, second prototype efforts evaluated a separate prototype fixture representative of the output impedance network exclusively and the third prototype effort evaluated the prototype performance with diode switches.
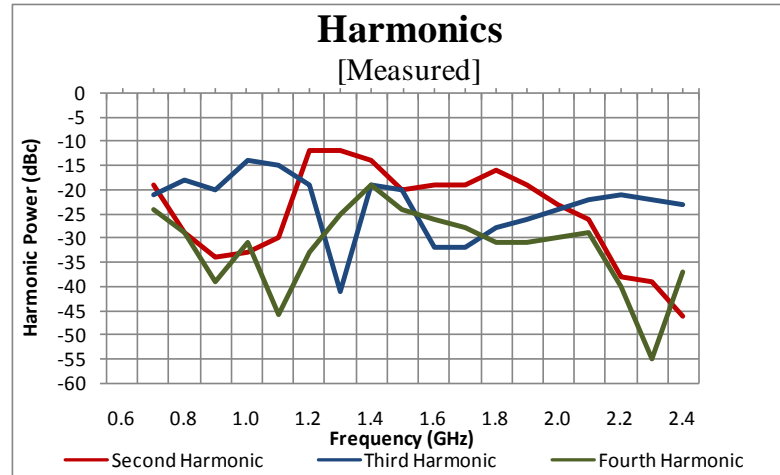
FIGURE 9-5: Prototype Harmonic Performance

The first prototype data-set was constructed facilitating ideal switching functionality. This is achieved by gap-welding a 10-mil wide silver ribbon in place of the diode. When the corresponding band was enabled, the silver ribbon was attached to the adjacent CuMoCu carrier providing the ground reference potential for the appropriate band. The silver ribbons on all other adjacent resonators were left un-connected. The measured performance results were then correlated to the modeled results. The corresponding saturated performance results are shown in FIGURE 9-4 while the corresponding measured harmonics are shown in FIGURE 9-5.

The saturated performance data shows output power and efficiency in excess of +42.7dBm (18W) and 59%, respectively. In all measured cases, the pass-band performance seems to be shifted down in frequency which is representative of a mis-tuned resonator network as shown in previous analysis prior to resonator optimization. There is a somewhat close correlation between measurements and model results where major deviation is shown in output power across the entire band and efficiency in Band 1.

The second prototype data-set was constructed by measuring the small signal s-parameter performance characteristics of the output impedance network exclusively. A separate prototype

fixture was constructed using the same shunt resonator networks, diodes and impedance transformer except the interface for the transistor to the output network was replaced with a 50Ω line length and terminated to an output port for measurement. In this test case, each diode was installed with the appropriate bias networks and potential applied for the desired operating band. The measured performance results were then correlated to the modeled results of the output network exclusively.
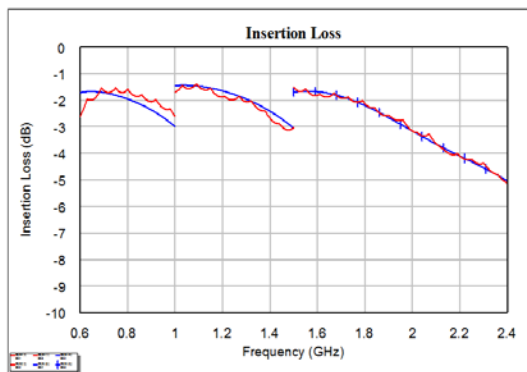
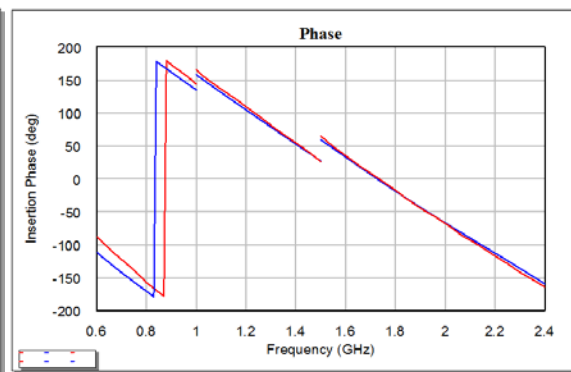

FIGURE 9-6: Insertion Loss

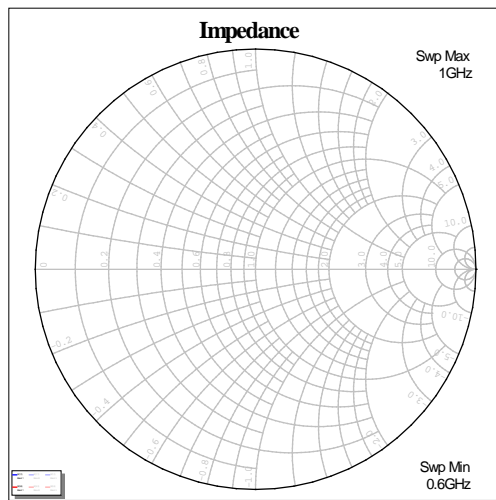

FIGURE 9-7: Insertion Phase
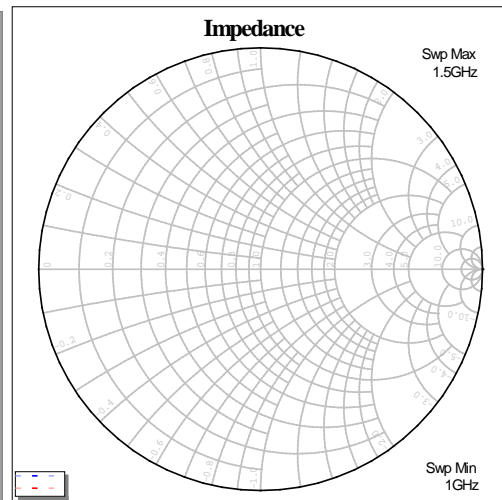

FIGURE 9-8: Impedance (Band 1)
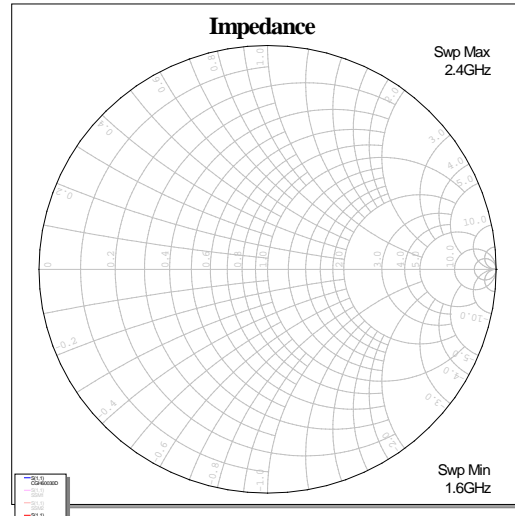

FIGURE 9-9: Impedance (Band 2)

FIGURE 9-10: Impedance (Band 3)

The correlation efforts involved aligning the magnitude and phase of the measured s-parameters with the output impedance network. The ports and 50Ω line lengths used in the output impedance network were de-embedded from the measured s-parameters. After fine tuning each bands resonator network, the model was better approximated to the actual prototype fixture measurements. The corresponding insertion loss and insertion phase measurements for the modeled network (blue) was compared to the measured results (red) as shown in FIGURE 9-6 and FIGURE 9-7, respectively. Likewise, the corresponding impedances as seen by the transistor are compared for Band 1, Band 2 and Band 3 as shown in FIGURE 9-8, FIGURE 9-9 and FIGURE 9-10, respectively.

The mechanisms associated with the model deviation were attributed to manufacturing and component variations. The key deviation from the initial model included the bond-wire inductance connecting each resonator capacitor, capacitor tolerance variation and additional package capacitance across the diode. To better approximate the physical prototype, the corresponding bond wire lengths were increased by an average of 5-mils, capacitor values were reduced by 10%, a shunt 0.2pF capacitor was placed across each shunt diode, a shunt 1000Ω

 resistor was placed across each shunt diode to account for the leakage current, a 1000Ω resistor was placed across each resonators capacitor and a phase element of about 4 degrees was inserted between each resonator element.

   The final prototype data-set was constructed facilitating real diode switching functionality in the output impedance network. When the corresponding band was enabled, the appropriate diode was forward biased with 0.1A while each adjacent bands diodes were reverse biased with -80V. The measured performance results were then correlated to the optimized output impedance network model. The corresponding saturated performance results are shown in FIGURE 9-11, the power gain and associated power added efficiency is shown in FIGURE 9-12, while the corresponding measured harmonics are shown in FIGURE 9-13.

   The saturated performance data shows output power and efficiency in excess of +42.9dBm (19W) and 50%, respectively. Correlating the modeled results show very close agreement on the drain efficiency demonstrating that the model is accounting for the physical model closely. Measured power gain is above 10dB above the majority of each band yielding typical PAE's of 47%.
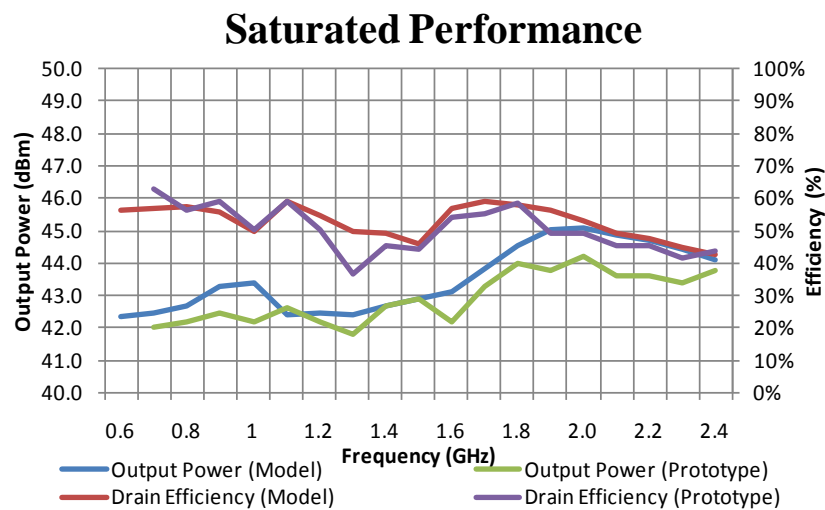

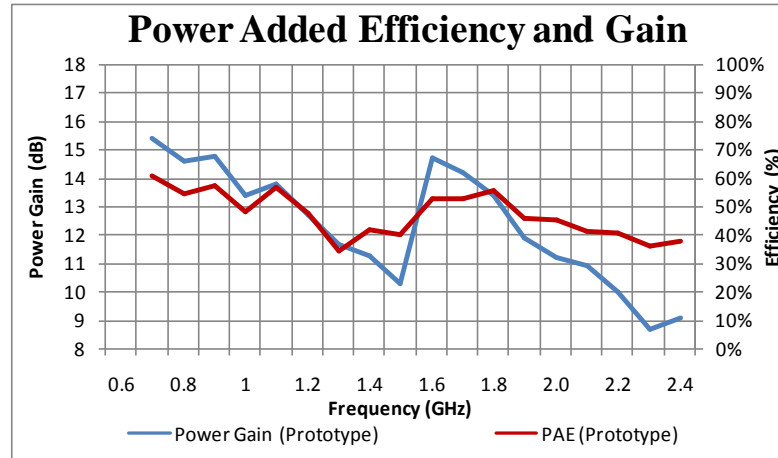FIGURE 9-11: Prototype Saturated Performance
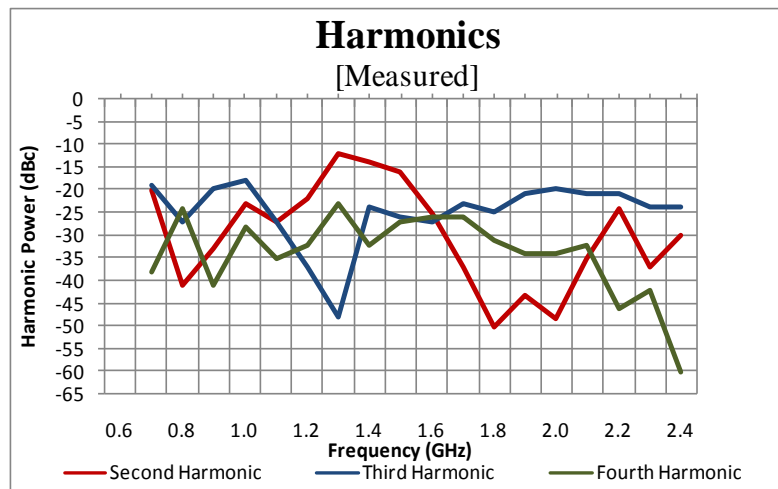
FIGURE 9-12: Prototype Power Gain and PAE

FIGURE 9-13: Prototype Harmonic Performance

CHAPTER 10

10. Conclusion

Achieving high efficiency power amplification requires specialized operating classes by which harmonic power and transistor dissipated power are controlled. The reactance compensated Class E circuit design proposed by Grebennikov [4] provides the best opportunity to achieve high efficiency operation over extended bandwidths, though limited to 40%. This design technique includes both a series and shunt resonator circuit in the output impedance network.

Electronically selecting multiple Class E output impedance networks proved to be impractical for the design while maintaining high efficiency operation. This was a result of the high insertion losses and impedance loading effects of the switch elements on the series resonator. Therefore, Class E operation could not be sustained with multiple switch networks.

Instead, high efficiency operation can be sustained by the shunt resonator network by providing a harmonically tuned output impedance environment with average efficiencies in excess of 66%. Multiple shunt resonators can be electronically switched into the output network providing wideband operation over two octaves ranging between 600MHz through 2400MHz. Diode switch elements provide the best device technology for high power applications due to their circuit simplicity and extremely low parasitic properties.

Operating a device in a harmonically tuned circuit environment requires a device that can sustain high breakdown voltages and low parasitic attributes. The Cree GaN DIE transistor provides the best commercially available device technology for high frequency and high efficiency applications.

Utilizing a broadband input impedance match and an output impedance transformer, a prototype fixture was developed to demonstrate the switching functionality using commercially

available diodes from Aeroflex Metelics [9]. The circuit prototype showed average efficiencies of 50% over the designed frequency range demonstrating that an electronically controlled, harmonically tuned power amplifier can be achieved.

References

[1]   P. Colantonio, F. Giannini, E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*, The Atrium, Southern Gate, Chichester, West Sussex, PO19 8SQ, United Kingdom, John Wiley & Sons Ltd, 2009

[2]   S. Cripps, *RF Power Amplifiers for Wireless Communications*, Norwood, MA, Artech House, 2006

[3]   P. Asbeck, "Power Amplifiers Course Notes," San Diego, CA, UCSD AS Soft Reserves, ECE287A RN01, Fall 2007

[4]   N. Kumar, C. Prakash, A. Grebennikov, A. Mediano, "High-Efficiency Broadband Parallel-Circuit Class E RF Power Amplifier With Reactance-Compensation Technique", IEEE Trans. On Microwave Theory and Techniques, Vol 56, No 3, March 2008, pp. 604-612

[5]   Product Datasheet, "Preliminary Cree CGH60030D 30 W, 6.0 GHz, GaN HEMT Die," Durham, NC, Cree Inc., Rev 1.3, September 2007

[6]   D. Pozar, *Microwave Engineering*, John Wiley & Sons Inc., Second Edition, 1998

[7]   M. Radmanesh, *RF Frequency and Microwave Electronics Illustrated*, Upper Saddle River, NJ, Prentice Hall PTR, 2001

[8]   Product Datasheet, "MADP-017025-1314 MADP-030025-1314 SURMOUNT 25 μm PIN Diodes RoHS Compliant," Lowell, MA, M/A-COM Technology Solutions Inc., Rev V5

[9]   Product Datasheet, "TBA Silicon PIN Diode," Sunnyvale, CA, Aeroflex Metelics, Rev -, October 2009

[10]   H. Kondoh, "An Accurate FET Modelling from Measured S-Parameters," Hewlett Packard Microwave Technology Division, IEEE MTT-S Digest, June 1986, pp. 377-380

[11]   D. Kelly, C. Brindle, C. Kemerling, M. Stuber, "The State-of-the-Art of Silicon-on-Sapphire CMOS RF Switches," San Diego, CA, Peregrine Semiconductor Corporation, CSIC 2005 Digest, 2005, pp. 200-203

[12]   Product Datasheet, "TGF2023-05 25 Watt Discrete Power GaN on SiC HEMT," Hillsboro, OR, TriQuint Semiconductor Inc., Rev D, April 2011

[13]   A. Grebennikov, "Simple Design Equations for Broadband Class E Power Amplifiers with Reactance Compensation", Loughmahon Technology Park, Skehard Road, Blackrock, Cork, Ireland, M/A-COM Eurotec Operations, Microwave Symposium Digest, IEEE MTT-S International, Vol 3, May 2001, pp. 2143-2146

[14]   Product Datasheet, "FLL300IL-1, FLL300IL-2, FLL300IL-3 L-Band Medium & High Power GaAs FET," San Jose, CA, Eudyna, Edition 1.2, July 1999

[15]   Product Datasheet, "BLF3G21-30 UHF power LDMOS transistor," Eindhoven, The Netherlands, NXP Semiconductors, Rev 01, February 2007

[16]   Product Datasheet, "CRF24060 60 W, SiC RF Power MESFET," Durham, NC, Cree Inc., Rev 2.0, April 2010

[17]   Product Datasheet, "RF3931D 30W GAN on SIC Power Amplifier DIE," Greensboro, NC, RF Micro Devices, Prelim DS110216, 2006

[18]   R. Pengelly, B. Millon, D. Farrel, B. Pribble, S. Wood, "Application of Non-Linear Models in a range of challenging GaN HEMT Power Amplifier Designs," Research Triangle Park, NC, Cree Inc., IEEE MTT-S, IMS, 2008

[19]   H. Statz, P. Newman, I. Smith, R. Pucel, H. Haus, "GaAs FET device and circuit simulation in SPICE," IEEE Trans. On Electron Devices, Vol. 34, No 2, February 1987, pp. 160

[20]   Product Datasheet, "PE42510A SPDT High Power UltraCMOS Reflective RF Switch 30 – 2000MHz," San Diego, CA, Peregrine Semiconductor Corporation, Document No. 70-0266-02, 2010

[21]   Product Datasheet, "HMC646LP2/646LP2E GaAs MMIC 40W Failsafe Switch, 0.1-2.1GHz," Chelmsford, MA, Hittite Microwave Corporation, v02.1009

[22]   Product Design Tool, "Microwave Impedance Calculator," Rogers, CT, Rogers Corporation, MWI-2010, Rev 2.2

[23]   Product Datasheet, "Surface Mount PIN Diode SP2T Switches MSW2030-203, MSW2031-203 & MSW2032-203 Series Datasheet," Sunnyvale, CA, Aeroflex Metelics, DS 13162, Rev C, April 2011

[24]   Product Datasheet, "Surface Mount PIN Diode SP3T Switches MSW3200-320, MSW3201-320 Series Datasheet," Sunnyvale, CA, Aeroflex Metelics, DS 13167, Rev B, April 2011