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Compensation for Lithography Induced Process Variations during Physical Design

by

Eric Yiow-Bing Chin

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Andrew Neureuther, Chair
Professor Kameshwar Poolla
Professor John Wawrzynek
Professor Fiona Doyle

Spring 2011

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Eric Yiow-Bing Chin

Abstract

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Doctor of Philosophy in Engineering - Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Andrew Neureuther, Chair

This dissertation addresses the challenge of designing robust integrated circuits in the deep sub micron regime in the presence of lithography process variability. By extending and combining existing process and circuit analysis techniques, flexible software frameworks are developed to provide detailed studies of circuit performance in the presence of lithography variations such as focus and exposure. Applications of these software frameworks to select circuits demonstrate the electrical impact of these variations and provide insight into variability aware compact models that capture the process dependent circuit behavior. These variability aware timing models abstract lithography variability from the process level to the circuit level and are used to estimate path level circuit performance with high accuracy with very little overhead in runtime.

The Interconnect Variability Characterization (IVC) framework maps lithography induced geometrical variations at the interconnect level to electrical delay variations. This framework is applied to one dimensional repeater circuits patterned with both 90nm single patterning and 32nm double patterning technologies, under the presence of focus, exposure, and overlay variability. Studies indicate that single and double patterning layouts generally exhibit small variations in delay (between 1-3%) due to self compensating RC effects associated with dense layouts and overlay errors for layouts without self-compensating RC effects. The delay response of each double patterned interconnect structure is fit with a second order polynomial model with focus, exposure, and misalignment parameters with 12 coefficients and residuals of less than 0.1ps. The IVC framework is also applied to a repeater circuit with cascaded interconnect structures to emulate more complex layout scenarios, and it is observed that the variations on each segment average out to reduce the overall delay variation.

The Standard Cell Variability Characterization (SCVC) framework advances existing layout-level lithography aware circuit analysis by extending it to cell-level applications utilizing a physically accurate approach that integrates process simulation, compact transistor models, and circuit simulation to characterize electrical cell behavior. This framework is applied to combinational and sequential cells in the Nangate 45nm Open Cell Library, and the timing response of these cells to lithography focus and exposure variations demonstrate Bossung like behavior. This behavior permits the process parameter dependent response to be captured in a nine term variability aware compact model based on Bossung fitting equations. For a two

input NAND gate, the variability aware compact model captures the simulated response to an accuracy of 0.3%. The SCVC framework is also applied to investigate advanced process effects including misalignment and layout proximity.

The abstraction of process variability from the layout level to the cell level opens up an entire new realm of circuit analysis and optimization and provides a foundation for path level variability analysis without the computationally expensive costs associated with joint process and circuit simulation. The SCVC framework is used with slight modification to illustrate the speedup and accuracy tradeoffs of using compact models. With variability aware compact models, the process dependent performance of a three stage logic circuit can be estimated to an accuracy of 0.7% with a speedup of over 50,000. Path level variability analysis also provides an accurate estimate (within 1%) of ring oscillator period in well under a second.

Another significant advantage of variability aware compact models is that they can be easily incorporated into existing design methodologies for design optimization. This is demonstrated by applying cell swapping on a logic circuit to reduce the overall delay variability along a circuit path. By including these variability aware compact models in cell characterization libraries, design metrics such as circuit timing, power, area, and delay variability can be quickly assessed to optimize for the correct balance of all design metrics, including delay variability.

Deterministic lithography variations can be easily captured using the variability aware compact models described in this dissertation. However, another prominent source of variability is random dopant fluctuations, which affect transistor threshold voltage and in turn circuit performance. The SCVC framework is utilized to investigate the interactions between deterministic lithography variations and random dopant fluctuations. Monte Carlo studies show that the output delay distribution in the presence of random dopant fluctuations is dependent on lithography focus and exposure conditions, with a 3.6 ps change in standard deviation across the focus exposure process window. This indicates that the electrical impact of random variations is dependent on systematic lithography variations, and this dependency should be included for precise analysis.

To Mom and Dad, with everlasting love

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Chapter 1

Introduction

1.1 Motivation

Semiconductors are ubiquitous in modern society. Computing devices, mobile phones, cameras, digital memories, automobile sensors, and traffic light controllers are a small subset of components that incorporate semiconductor devices known as transistors. These transistors are carefully designed and arranged to form integrated circuits that process and transmit electronic signals within a semiconductor chip. In 1965, Gordon Moore made an astute observation that the transistor density in a chip doubles every two years, and theorized that this trend would continue [26]. This theory was later known as Moore's Law, and has been a strong driver of semiconductor technology scaling to date. The doubling of transistor density every two years has traditionally provided improvements in transistor performance and reductions in manufacturing costs.

Today, there are thousands of steps needed to develop a semiconductor chip for use in an end product. Circuit designers carefully design robust integrated circuits that meet performance targets and are ideally immune to manufacturing nonidealities. These designs are handed off to a manufacturing facility for fabrication. After fabrication, each chip is electrically tested to ensure acceptable circuit performance. Then the wafer is diced up to separate all the individual chips, and each chip is packaged so it can be incorporated into a bigger electronic system. For certain specialized chips, software interfaces are also developed to access the hardware capabilities of the chip. Post-packaging hardware and software testing might reveal certain flaws or bugs in the circuit performance that require a revision in integrated circuit design, process technology or a software workaround.

The successful development of a semiconductor chip requires close interaction between all the stakeholders in this complex process. Circuit designers must be aware of the potential manufacturing issues that affect design performance. Process technologists working in the fabrication facilities must understand how their optimizations affect design performance. Both circuit designers and process technologists must work with the testing teams to root cause any issues identified from post-fabrication testing. Should there be any bugs or flaws in functionality, all parties, including software and testing teams, need to come together to determine the appropriate fix.

Aggressive technology scaling in accordance with Moore's Law leads to additional challenges in this semiconductor development ecosystem. Process technologies no longer scale as easily as before, but innovative engineering solutions permit extending the lifetimes of existing process technologies. However, as device sizes become smaller and smaller, nanometer scale process non-idealities begin to affect circuit performance. Consequently, traditional design methodologies no longer accurately capture circuit performance. These process non-idealities must be understood, captured, and incorporated in circuit analysis, requiring tight collaboration between circuit designers and process technologists. The existing rate of technology scaling cannot be sustained with existing design and process paradigms, requiring new innovative methods to handle the complexities of semiconductor development in the deep sub micron regime.

1.2 Dissertation Organization

Developing solutions that address manufacturing complexities requires a broad understanding into key areas of semiconductor development. Gone are the days where expertise in a single area is sufficient. Even so, gaining expertise in multiple areas is difficult due to the enormous depth that can be developed in any single area. For this reason, there are many novel research solutions that address design and manufacturing complexity, but few are transferred to production semiconductor development due to their narrow scopes and limited applicability.

This dissertation addresses future-generation challenges in semiconductor development by developing solutions that incorporate lithography variability in design methodologies. It is extremely challenging to develop solutions that transcend design and process boundaries, as there has historically been limited information sharing between the two. In light of this, background in both of these areas is provided in Chapter 2. Starting with a process perspective, key physical causes of lithography variability are described. A brief overview of physical design methodologies is provided, leading to exploration of traditional corner based design methods that ensure design robustness to process variability. The chapter continues with a survey on recently introduced strategies that address lithography variability, followed by a discussion of the opportunity to incorporate lithography variability analysis at higher stages of design implementation, through the use of compact modeling techniques. These techniques compress lithography variability data into compact models that contain a limited number of process dependent parameters and can be quickly assessed with little time, taking fractions of a second to assess for any combination of input parameters.

Chapter 3 centers around the approach taken to create lithography variability aware compact models appropriate for use in physical design modules. The speed, compactness, and compatability of these models with existing design techniques allow designers to make appropriate tradeoffs between lithography variability and other performance metrics. Developing these models requires new analytical techniques that combine different existing design automation tools to transform lithography variability into electrical circuit variability. Still, integrating these tools is far from trivial due to proprietary data formats and different input/output requirements for each tools. Therefore, it is essential to develop integrated frameworks to per-

form lithography aware circuit analysis for the purpose of creating the desired compact models. The three frameworks developed for such analysis are detailed in this chapter.

The Interconnect Variability Characterization (IVC) framework is used to investigate interconnect level lithography variations in Chapter 4. Instead of utilizing an official process design kit (PDK) that restricts publication of data derived from PDK access, custom generated PDKs are utilized to perform studies and obtain results that can be openly published. The IVC framework is applied to a one dimensional repeater circuit with differing layout topologies under varying focus and exposure conditions at the 90nm node. Similar analysis is performed at the 32nm node, where double patterning is assumed and misalignment variability is introduced. For both technologies, the delay responses can be visualized on a three dimensional plot and are shown to be easily modeled using a 12 term second order polynomial equation. Designers can use these models to obtain insight into the degree of delay variability associated with specific circuit topologies and interconnect routing scenarios.

Chapter 5 explores lithography variability at the cell level using the Standard Cell Variability Characterization (SCVC) framework, the FreePDK45 design kit, and the Nangate 45nm Open Cell Library. One approach to create variability aware timing models utilizes geometrical biasing, which upsizes or downsizes the ideal transistor dimensions within a cell. Using this method, delay sensitivity tables are created to complement existing delay tables in standard cell libraries. The second approach utilizes lithography contour analysis to more precisely account for typical non-uniform transistor dimensions caused by lithography variations. With this approach, the timing performance in the presence of focus and exposure variations can be visualized in an electrical process window fit with a Bossung like compact model with a fraction of a picosecond accuracy. Chapter 6 illustrates that the SCVC framework is extensible for the more advanced topics of misalignment and layout proximity effects. Further studies on multi-stage combinational cells and sequential cells illustrate that the same compact model can be used to model advanced timing and power performance in the presence of lithographic variability.

Chapter 7 ties the cell level compact models developed in Chapters 5 and 6 into physical design methodologies through path level variability analysis. The first circuit path explored is an 11-stage ring oscillator. With pre-characterized compact models for an inverter cell, the ring oscillator period can be estimated for 27 different focus and exposure combinations to an accuracy of 1% in approximately 1/5 of a second. For a three stage combinational circuit path, an estimate of circuit path delay can be obtained across the same process window to an accuracy of 0.7%, with a speedup of over 50,000 compared to post-layout lithography aware circuit analysis. These immense speedups are achieved by moving computationally intensive lithography aware circuit analysis into cell level pre-characterized libraries.

While the ability to perform fast variability aware path level performance estimation is useful, the true power of these compact models lies in enabling design methodologies to compensate for lithography variations. This is demonstrated through manual analysis of a three stage combinational circuit path, where one of the cells is swapped out for another cell with less performance sensitivity to lithography variability at the expense of additional power. With additional automation, tradeoffs between lithography variability and other design metrics can be quickly assessed in physical design methodologies, allowing for lithography variability to be

included in circuit optimization.

1.3 Unique Dissertation Contributions

This dissertation results from multiple years of research dedicated towards developing solutions that address the complexity of designing digital circuits in the presence of variability. Most of the frameworks, studies, and results detailed in this dissertation, unless mentioned otherwise, are my own original works, developed under the mentorship of Professor Andrew Neureuther. Many thanks to Cooper Levy who, under my direct guidance, utilized my SCVC framework to perform lithography aware variability analysis on sequential cell timing performance and combinational cell power consumption. Cooper was also instrumental in running Monte Carlo simulations to model random dopant fluctuations, which led to the discovery that the distribution of cell performance is a function of lithography process parameters.

There are several original contributions in this dissertation that I feel are worth highlighting. I am proud of developing the IVC and SCVC frameworks, which integrate existing analysis techniques in a novel fashion to investigate the electrical impact of lithography process variations. I improved upon an existing contour based device analysis technique, boosting the accuracy of such analysis by replacing coarse transistor performance approximations with a more accurate table based lookup method that is detailed in Section 5.4.3. Recognizing that the cell level behavior in response to lithography focus and exposure variations follows a well behaved and very recognizable pattern, I captured the cell level electrical behavior in a compact model with little loss in accuracy. Later, I demonstrated that these cell level compact models, when combined with a specific circuit topology and generic timing calculations, permit path level variability aware circuit analysis at fast speeds with a slight tradeoff in simulation accuracy.

Chapter 2

Background

2.1 Lithography Variability

Fabricating a modern integrated circuit involves a myriad of wafer processing steps, including oxidation, ion implantation, diffusion, etching, lithography, chemical-mechanical polishing, annealing, and electroplating. As with any manufacturing system, there is some amount of uncontrollable process variability in each of these steps. One of the largest sources of variability is optical lithography, which is used to transfer patterns pre-defined on a mask to individual dies on the wafer. This mask transfer process is performed multiple times before fabrication is complete, to define front end layers and back end layers. Front end layers define device performance, and include well implant, active, polysilicon, and threshold implant layers. Back end layers affect interconnect performance, and include up to eleven metal and eleven via layers.

In 2010, state of the art process technologies utilize 193nm deep ultraviolet (DUV) optical projection lithography to define features on a silicon wafer. To meet the demands of shrinking feature sizes, process technology engineers create unique engineering solutions to extend the lifetime of 193nm DUV lithography. Since the incorporation of 193nm DUV lithography technology in semiconductor manufacturing, the standard lithography process has been refined by increasing the numerical aperture, changing the illumination source, moving to immersion lithography, using phase shift masks, and optical proximity correction (OPC) [39]. Each of these steps adds additional complexity to the process, with the benefit of extending the lifetime of 193nm DUV lithography.

As process engineers strive to push 193nm DUV lithography to its limits, controlling lithography variability is becoming a top priority. State of the art process technologies utilize step and scan lithography systems where the slit and the wafer stage are continuously moving. These moving parts create position dependent focus and exposure variations on all processed wafers. To characterize the focus exposure process window, a focus exposure matrix is commonly used [27]. This is achieved by exposing the different dies on a wafer in a systematically varying fashion, with different focus and exposure conditions for each die. Dimensional measurements of a one dimensional test structure are taken at the same location for each die to create a Bossung plot which depicts how the measured critical dimension changes under different focus and exposure conditions [6]. An example Bossung plot obtained through lithography simulation is

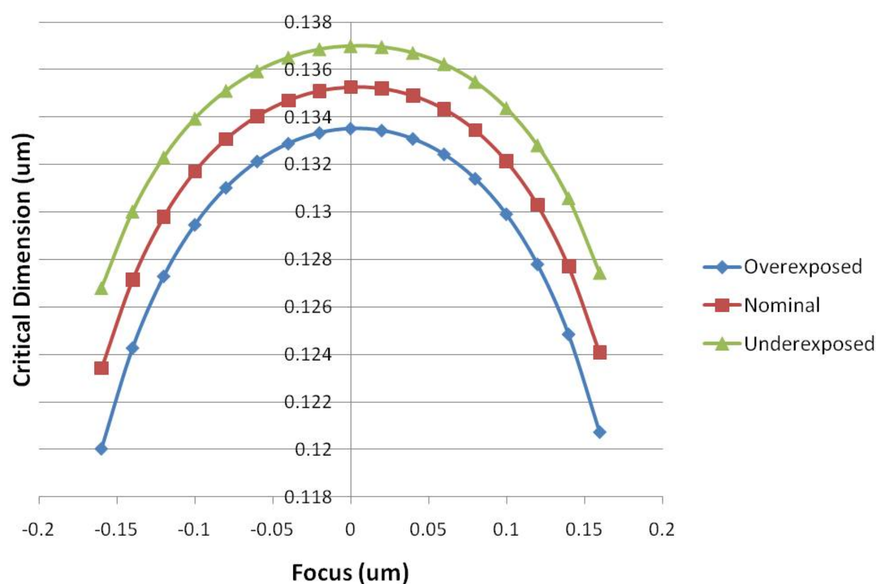


Figure 2.1: Sample Bossung Plot

shown in Figure 2.1.

These focus and exposure variations, along with other lithography variations, distort the contours transferred from the mask patterns and ultimately alter the performance characteristics at the device, interconnect, circuit, and system levels. The behavior of the Bossung plot indicates that the identical layout feature resolves on wafer differently under different process conditions. In addition, the nature of patterns in the local proximity of the feature will affect its printability. Experimental data collected from a 90nm test wafer indicates that the presence of a neighboring dummy feature on the polysilicon layer affects ring oscillator performance, shifting the ring oscillator frequency by over 10% percent [30].

Lithography at the 32nm and 22nm nodes becomes even more complex, as select critical layers can no longer be patterned with a single mask due to small feature sizes and tight pitches. Instead, multiple patterning steps will be used to pattern a single layer, thus increasing process complexity. This opens up another source of variability, as neighboring features may be defined with separate masks each with different process conditions and misalignment.

One of the most highly anticipated replacements for 193nm DUV lithography is 13.5nm extreme ultraviolet (EUV) lithography, currently under development. It is expected that EUV lithography will be used at the 16nm node and below. Even so, EUV lithography will quickly enter the regime of sub-wavelength lithography, and the complexity of the process technology combined with continually shrinking feature sizes indicates that similar process non-idealities for EUV lithography will be observed as with 193nm DUV lithography.

2.2 Physical Design Methodologies

While process technologists strive to minimize lithography induced variability through process engineering and optimization, circuit designers strive to create robust designs that function across typically expected ranges of such variability. However, making changes in the design is not as simple as changing a design parameter and then resimulating the design to validate that it meets all the specifications. The latest computer chips today contain over one billion transistors, and many complex design methodologies are utilized to achieve the final design.

These design methodologies include custom design, analog and mixed signal (AMS) design, and physical design. The first two design methodologies are used to create design blocks with a limited number of transistors, and each transistor is tuned to achieve the final design. Due to the small number of transistors, simulation tools that model each transistor's behavior are used to characterize the circuit performance. In contrast, physical design methodologies integrate cells to achieve the circuit design performance. The number of cells in any one block can be in the order of hundreds of thousands of cells, and each cell generally contains multiple transistors.

To realize such large designs, physical design methodologies must handle the intricate process of cell level integration to meet block level cell specifications. This is achieved through abstraction of transistor level performance into cell level models, which are developed through the same transistor level circuit simulation methods used for custom design and AMS design. These cell level performance models can then be combined with behavioral and layout models for analysis in each step of physical design.

A high level overview of physical design methodologies is shown in Figure 2.2. First, a netlist or circuit schematic is generated from the desired circuit functionality. Then, a floorplan is created to define the physical layout area in which cells are allowed to be placed. Placement tools interpret the netlist and place cells in locations that are legalized, as defined during the previous stage. Clock tree synthesis is then used to route interconnect wires that distribute the clock signal evenly across the chip. Routing tools then connect the pins of each cell using interconnect wires that minimize wirelength and reduce delay. Interconnect extraction is used to determine the parasitic resistance and capacitance values along the chip. Finally, static timing analysis is performed to ensure the delays for all paths meet design specifications.

Though these modules each seem to be very self contained, there are many customizations in each module, and a single change can cause profound effects that ripple through other stages in the design. For example, an attempt might be made to minimize power in a block. One solution is to change the transistor threshold voltages of all cells in non-critical paths. However, some of these non-critical paths might turn into critical paths with timing violations, and so to address this one might increase the driving strength of problematic cells by swapping them with similar cells with larger transistor widths. The new cell might be bigger than the old cell, and thus the placement and routing of all other cells in the design might be modified. Ultimately, the designer must developed a customized design methodology specific to each block to meet all performance specifications. This is a very iterative process that involves many steps and customizations to achieve design closure.

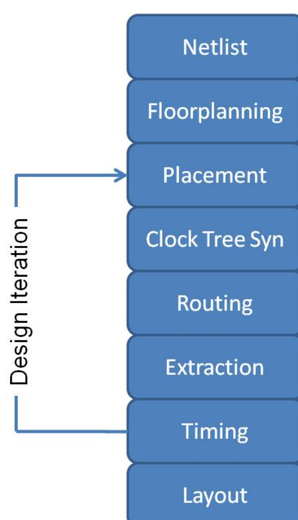


Figure 2.2: High Level Overview of Physical Design Methodologies

2.3 Modeling Variability in Design

No matter which design methodology is used to realize a design, all the circuits within a design are simulated under different conditions to ensure design robustness. This provides a design guardband against expected values of process variability. The types of conditions that are chosen for circuit simulation depend on the level of analysis. Traditionally, these conditions are chosen at the corners of the process window and between three and nine different corners are used for simulation analysis.

In the case of transistor level circuit simulation, transistor models are provided for a range of process characteristics. Usually two transistor models are used for circuit analysis, one for NMOS transistors and the other for PMOS transistors [15]. Each model contains three different options to denote the transistor performance: slow, typical, and fast. A two letter combination is used to denote one corner case simulation condition. The first letter corresponds to the NMOS compact model and the second letter corresponds to the PMOS compact model. For example, a SF corner case simulation indicates a simulation performed using slow NMOS and fast PMOS transistors. With a two transistor models per simulation, there are nine possible corner cases: SS, ST, SF, TS, TT, TF, FS, FT, FF.

The corners for the cell level circuit simulation associated with physical design are different in nature. Instead of choosing corners corresponding to transistor performance, the corners are based on three factors: process, voltage, and temperature (PVT) [16]. The process conditions are identical to those used for transistor level circuit simulation; typically only SS, TT, and FF are used. There are three corner voltages used; for a design at a nominal 1.1V technology, 0.95V and 1.25V are the other two corners. There are also three corner temperatures: 0°C, 25°C, and 125°C. Using these corner values for process, voltage, and temperature, three datasets are created corresponding to the slowest, typical, and fastest PVT corners. For example, the slow PVT corner combines the SS process, 125°C temperature, and 0.95V voltage. Physical design methodologies utilize all three datasets to achieve a design robust to circuit and process vari-

ability.

The PVT corners for physical design involve analysis at the cell level, which model effects at the active, poly and contact layers. Proper circuit path analysis requires accounting for layout induced parasitic resistances and capacitances for all metal interconnect layers. Since the performance of a circuit is also dependent on the RC load of the interconnect wires, it is not surprising that corners are also used for interconnect analysis. There are usually at least five corners that are used in analysis: nominal, worst case capacitance, worst case delay, best case capacitance, and best case delay [17]. Each of these corners consist of some combination of best and worst case scenarios for resistance and capacitance for all metal layers.

For complete analysis of a silicon chip, some combination of corner case design analysis at all levels of abstraction must be performed. Analog blocks are simulated using slow and fast transistor models. Cell based blocks are simulated at different PVT corners. And for proper interconnect analysis, parasitic extraction is performed at different RC corners. For older technologies, it used to be the case that corner based analysis was sufficient to ensure a robust design. However, the physical phenomena associated with shrinking today's transistor sizes even smaller are becoming more significant. It continues to be an ongoing debate whether corner based design sufficiently accounts for process variability. Though it is possible to design circuits that pass all corner based analysis checks, certain unique combinations of process variations can still cause a real circuit failure that is undetected by corner case analysis.

2.4 Coping with Lithography Variability

The increasing challenges of semiconductor manufacturing at shrinking technology nodes have increased complexity in both process and design engineering, leading to closer design and process technology collaboration. In response to these challenges, new design strategies have been developed to model, mitigate, and control the impact of lithography variability.

2.4.1 Strategy #1: Avoid Poor Layouts

The conventional interface between semiconductor manufacturing and design is the design rule manual. The design rule manual is created through collaboration between manufacturing and design teams. Once the design rule manual is finalized, it serves as a contract that process technology will fabricate functional chips provided that the design meets all rules in the manual. Most of these rules are geometrical rules. Some rule examples include minimum distance between contacts and transistor gates, acceptable ranges of poly pitch, and metal-contact overlap distances.

Scaling at the same 193nm wavelength used in DUV lithography has made it increasingly difficult to print layouts permitted at earlier technology nodes. One strategy to combat this is to add additional rules to the design rule manual to restrict poor layouts from being incorporated into design. However, many poorly printing layouts are two dimensional in nature, and in recent years, attempts to restrict these specific layouts have led to a drastic increase in the number of design rules in the manual. To complement standard design rule checking tools, new algorithms have been developed to identify and classify problematic layout patterns using

pattern matching techniques [18, 20, 41]. These algorithms are part of a class of tools called physical verification tools that are run on layouts to ensure that they meet design rules and match the circuit intent.

2.4.2 Strategy #2: Layouts Regularization

Another technique being used to improve printability is to restrict the possible layout patterns even further. In older technologies, poly features are allowed to run in both horizontal and vertical dimensions. However, at the 32nm technology node and beyond, most design kits only allow unidirectional poly running in a single direction. This reduces the amount of geometrical variation induced by lithography process variations, as well as allows unique off axis illumination sources to be used for poly printing.

There has also been effort at the cell level to co-optimize circuit performance and manufacturability. Starting off with printability friendly cell layouts increases the likelihood that the entire design will have reduced sensitivity to variability. One such approach derives cell layouts from a set of printability friendly patterns[22]. These cell layouts are known as regular fabrics, and a new set of physical implementation tools is created to leverage the regularity of the layouts. For a sample 65nm processor design, the usage of regular fabrics comes at a 6.7% area penalty with an estimated 6.8% increase in the number of good dies per wafer.

2.4.3 Strategy #3: Statistical Design Analysis

An increasing number of process variability sources each significantly impacting circuit performance has led to an increase in the number of corners used in design analysis. However, analysis at these corners may not be totally comprehensive and may even be overly conservative. An alternative to corner based analysis is the use of statistical design analysis. The most prominent example of statistical analysis in physical design is in assessing performance of critical timing paths through Statistical Timing Analysis (SSTA).

Instead of calculating absolute delays for every process corner, SSTA propagates a distribution of signal arrival times at each node in the circuit path. Advanced SSTA algorithms can accurately predict bounds for statistical timing procedures with linear run time complexity[8, 3]. These bounds are calculated using provided confidence intervals, and the accuracy of these results is dependent on accurate models for process variations. A reputable commercial implementation of SSTA utilizes distributions in transistor channel length to model inter and intra die process variations. Obtaining accurate models for SSTA algorithms is an expensive process, requiring experimental characterization that create models which may no longer represent the often changing process technology.

2.4.4 Strategy #4: Contour Based Compact Transistor Modeling

At smaller technology nodes, wafer level contour profiles no longer produce rectangular transistors with uniform channel widths and lengths [21, 28]. Both active and poly corner rounding begin to encroach upon the transistor gate region, defined as the intersection of poly

geometries and active geometries. Additionally, lithography induced line edge roughness creates non-uniform channel lengths across the width of each device.

These non-uniform transistors are typically modeled by spatially subdividing each transistor contour into fine segments, each with its own effective gate width and gate length [33, 40, 7, 37]. These transistor segments are then simulated to determine the new performance of the transistor. Each original transistor in the circuit simulation is then replaced with a set of transistors in parallel that represent the new transistor performance. These models are validated against rigorous device simulation results.

2.4.5 Strategy #5: Lithography Simulation Speedups

Lithography simulation is inherently a time consuming process. However, some methods have been developed that speed up this analysis with only a slight degradation in accuracy. A Pattern Matching engine was developed to allow quick assessment of lateral electrical field spillover effects based on a convolution kernel and full chip layout [19]. Using physics based kernel convolution models, the intensity deviation from focus and coma lens aberrations can be modeled accurately with a R^2 value of greater than 0.98 [25]. This intensity deviation can be translated to edge movement with a lithography simulation at the nominal process condition. Thus the geometrical impact of lithographic aberrations can be captured through fast kernel convolutions and one nominal lithography simulation.

2.5 Summary

The complexity of process and design engineering increases with smaller features sizes at every new technology node. Process engineers dedicate their efforts to tune and optimize the process to achieve performance targets and limit variability, while design engineers synthesize circuits that are robust to an acceptable range of process variability. New nanometer level effects arise from patterning smaller features using the same 193nm wavelength DUV technology. To mitigate these nanometer level effects, solutions have been developed that restrict problematic layouts with high variability and provide new design analysis techniques to account for process variability.

While these solutions have enabled continued scaling to the 45nm node and beyond, there are still areas for improvement in process and design co-optimization. Existing lithography aware analysis techniques, including those described in Section 2.4.4, require a layout to combine lithography variability with circuit performance. This may be permissible for designs with tens or hundreds of transistors due to small layout sizes, but is too rigorous for large scale layouts associated with physical design.

In the case of physical design, the design engineer is tasked with running the whole suite of tools illustrated in Figure 2.2 and must artfully tweak settings for each step to achieve desired performance targets. Existing lithography aware analysis techniques can only be run at the layout level when the design is mostly complete, and the results provide very limited insight to the designer about modifications needed to reduce variability in the circuit. Therefore analysis at the layout level is computationally expensive with very little benefit.

Clearly there is much opportunity to abstract lithography variability upstream into earlier stages of the design flow such as placement and routing. By making quantitative data about lithography variability available at higher levels of abstraction, proper tradeoffs between lithography variability and other design metrics can be achieved at earlier stages in the design, allowing for a more robust design. The abstraction of lithography variability is achieved by building upon existing design and lithography analysis techniques, and the details of this approach are detailed in Chapter 3.

Chapter 3

Tools for Circuit Variability Analysis

3.1 Introduction

This chapter presents an approach to enable variability aware circuit analysis that transcends the boundaries between process technology and circuit design. Software requirements and functionality for tools in each of these areas are quite different in nature. For example, the speed, flexibility, and accuracy of a tool used in process simulation may be completely different from what is needed in design implementation and analysis. In this chapter, we review existing coverage of electronic design automation (EDA) tools and highlight challenges in incorporating these tools in a lithography aware analysis flow. From these assessments, we identify opportunities to create specialized tools that abstract the impact of lithography process variability into physical design methodologies, and detail three key frameworks that are developed to support this purpose.

3.2 Existing Electronic Design Automation (EDA) Tools

The electronic design automation industry provides a spectrum of software tools to aid in the design and manufacturing of electronic systems. These tools can be categorized into different areas based on the desired application. In considering the impact of process variability on circuit analysis, the core areas of interest are technology computer aided design (TCAD) simulation tools, mask data preparation (MDP) tools, circuit simulation tools, and physical implementation tools.

3.2.1 TCAD Simulation Tools

Of all the EDA tools covered in this chapter, TCAD simulation tools are by far the most rigorous in terms of accuracy and physics based modeling. The purpose of such tools is precise modeling of physical effects, often times at the atomistic level. Thus developers often prioritize accurate modeling over simulation speed, resulting in tools that are appropriate for the development of process technology. These TCAD tools can be sub-divided into two distinct areas: process modeling and device modeling. Process modeling tools simulate topological profiles

for specific processing steps that occur in semiconductor fabrication. Examples include optical imaging simulation, photoresist modeling, etch profile edge simulation, CMP thickness modeling, and optical waveguide modeling. Device modeling simulates the electrical characteristics of devices created through a sequence of process steps, modeling advanced device characteristics including carrier transport, electron tunneling, and strain.

3.2.2 Mask Data Preparation Tools

After the design of a chip is complete, the entire design layout is sent to a tapeout team that post-processes the layout to meet manufacturability criteria. This tapeout process includes layout scaling, fracturing, metal fill, manufacturability checking, and optical proximity correction (OPC). By far the most complex step is OPC, where the mask layout is modified by perturbing polygon edges to obtain the desired silicon contour on the wafer. This involves an iterative process with a lithography simulation after each step of layout perturbation. Since running a TCAD level optical imaging simulation tool on full-chip layouts would be far too time intensive, the lithography simulation used in OPC relies on a faster algorithm that incorporates a set of convolution kernels as an approximation to rigorous lithography simulation. Even with this approximation, performing OPC on a full chip microprocessor design may take on the order of days to run, with multiple machines and computer processors.

3.2.3 Circuit Simulation Tools

Circuit simulation tools allow the designer to study the DC, AC, and transient behavior of circuits. The industry standard tool for circuit simulation is the Simulation Program with Integrated Circuit Emphasis (SPICE), which incorporates equation formulation, solutions to linear and nonlinear equations, and numerical integration [29]. Compact device models are used in conjunction with SPICE to model advanced device behavior. One prominent example of such models is the Berkeley Short-Chanel IGFET Model (BSIM), which contains hundreds of parameters to model device behavior [35]. These compact models are calibrated with both TCAD simulations and measured data, and are considered extremely accurate with modeling of advanced physical effects including short channel effects, temperature, layout dependent parasitics, and strain.

3.2.4 Physical Implementation Tools

Physical implementation tools are utilized to realize very large scale designs. Instead of striving to achieve optimal circuit performance through the tuning of each transistor, the designer is tasked with achieving area, power, and performance targets through the selection, placement, and routing of pre-designed cells within a large block. The basic building blocks of these designs are the individual cells, which contain up to 20 transistors. Abstract timing and power models for each cell are developed using standard cell characterization tools. Placement algorithms allow cells to be placed in rows of standard cells and optimized for small area and routability. Routing algorithms connect the pins of each cell to other cells or the ports of the

design. These tools are utilized to create designs with millions of transistors, without having to simulate each circuit path with standard circuit simulation tools, which would otherwise be infeasible due to time constraints.

3.3 Lithography Aware Circuit Analysis

To model the circuit level impact of lithography variations, process variability must be transformed to circuit performance. The conventional approach begins with a layout level lithography simulation, performed on the layers of interest. The resulting lithography contours are mapped to new device characteristics or parasitics through compact transistor models, such as those described in Section 2.4.4. The lithography aware circuit performance can be obtained through a subsequent circuit simulation performed using the updated device or parasitic characteristics.

There are two disadvantages to this approach. First, this analysis can only be performed after the layout is complete. Any subsequent layout change caused by a new placement or routing will modify the circuit topology and thus negate the results of lithography aware analysis. Secondly, this analysis is extremely costly to perform. To perform analysis at one lithography process condition, a very time consuming process and circuit simulation must be done. In the time it takes to do perform this analysis, another iteration of placement and routing could have been performed. Furthermore, this type of analysis should be performed at not only one process condition but multiple process points to provide feedback to the designer about circuit variability.

3.4 Creating Variability Aware Analysis Models

Conventional post-layout lithography analysis does not scale. For large designs with over 100,000 cells, this analysis is prohibitively time intensive. Moreover, this analysis yields information about the variability in performance of certain critical paths, but provides no feedback or tradeoffs that can be used to balance lithography induced variability with other design metrics such as area, timing, power, nose, electromigration, and IR drop. Therefore, the goal of this dissertation was to create compact models of lithography variability that are compatible with existing cell based design flows and fast enough to be used in parallel with the physical implementation modules. The speed, compactness, and compatibility of these models allow designers and EDA tools to make the appropriate tradeoffs between lithography variability and other design metrics.

The primary challenge in the creation of these models is that there is no existing framework to study the impact of lithography variations on circuit performance. Industry grade EDA tools focus on core areas including TCAD simulation, mask data preparation, circuit simulation, and physical implementation. Each of these tools has proprietary formats and operates with different inputs and outputs, often times at different levels of abstraction. To address this challenge, a set of unique process and design information frameworks have been developed that allows for the transformation of process level effects to circuit level impact.

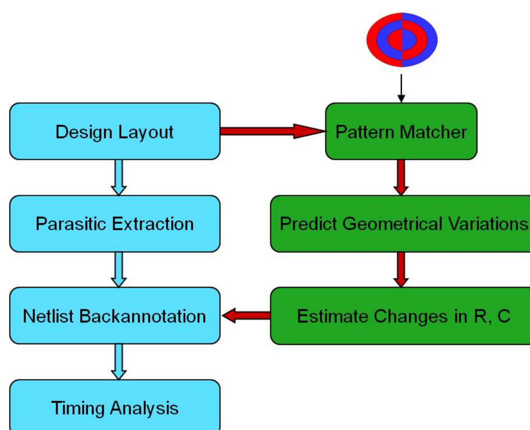


Figure 3.1: Process Variation Net Scanning Methodology

There are multiple considerations for the creation of compact variability models that we wish to create. These considerations change based on the actual application of these models. In general, a good model should be both fast and first-cut accurate, achieving the right balance of accuracy and runtime. Models should encapsulate variability with a flexible model that allows library size to scale efficiently, and should be easily incorporated into existing design methodologies.

3.5 Developed Methodologies

Three key frameworks have been developed that allow for the study of interaction between lithography variability and circuit performance. These frameworks integrate a wide range of tools across the EDA spectrum, including process simulators, device simulators, compact transistor models, circuit simulators, parasitic extraction tools, static timing analysis tools, and cell characterization tools.

3.5.1 Process Variation Net Scanning

Process Variation Net Scanning leverages the fast speed of pattern matching in conjunction with kernel convolution methods to obtain an accurate estimate of through focus lithography contours without simulations at multiple process points. The flow, as applied to interconnect level analysis, is demonstrated in Figure 3.1.

First, models similar to Kernel Convolution with Pattern Matching (KCPM) are applied to an existing layout to estimate changes in intensity at every point along the contour. Combined with a nominal lithography simulation which provides information about the image slope along the contour, the estimated change in contour can be predicted. From there, edge movements can be translated to geometrical variations in interconnect, and therefore estimated changes in parasitic resistance and capacitance. These estimated changes are backannoted in the design netlist and are used to perform a new SPICE level timing analysis.

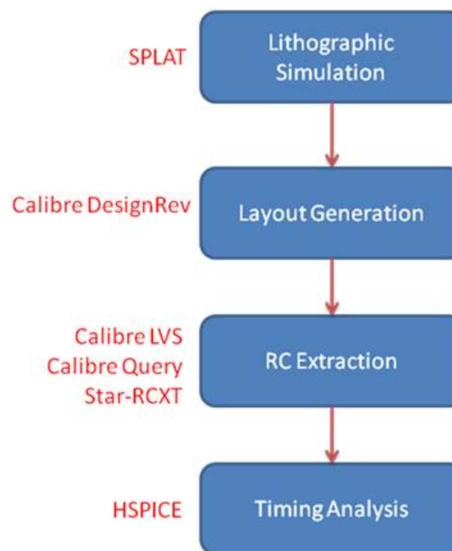


Figure 3.2: Interconnect Variability Characterization Methodology

This framework was applied to a 90nm digital design containing over 325,000 nets with an area of $3.61mm^2$, to study the impact of lithography coma variations in Metal 3 and defocus variations on Metal 4 [9]. KCPM results were obtained at every micron along straight interconnect wires, and those results are used to derive a new netlist with modified parasitics. A rerun of static timing analysis on the new netlist showed that the topmost critical paths have changed with new timing results. Runtime analysis of this methodology indicated that the speed of this KCPM approach can be made at least twice as fast as a comparable extraction run without the need for rigorous lithography simulation.

3.5.2 Interconnect Variability Characterization

Interconnect Variability Characterization combines process simulation, parasitic RC extraction, and SPICE level timing analysis to develop compact parameter interconnect timing models. Figure 3.2 depicts the methodology used to transform lithographic variations to delay variations.

First, lithographic simulation of a target pattern is performed across the process window. The response of critical dimensions across the process window is modeled, and a new rectangular layout with modified wire and space sizes is automatically generated. To model misalignment during double patterning, these wires are also shifted by an overlay factor. Then transistor level parasitic extraction is run to generate a netlist with extracted R and C parasitics. Finally, transient SPICE simulations are run for delay characterization.

This framework is applied to one-dimensional repeater circuits to characterize the timing response to focus and exposure variations using single patterning and double patterning process technologies [11]. The delay responses of each homogenous interconnect structure are fit using an algebraic compact model containing 12 coefficients. The effects of advanced lithography structures are explored through the use of cascaded interconnect structures with the same

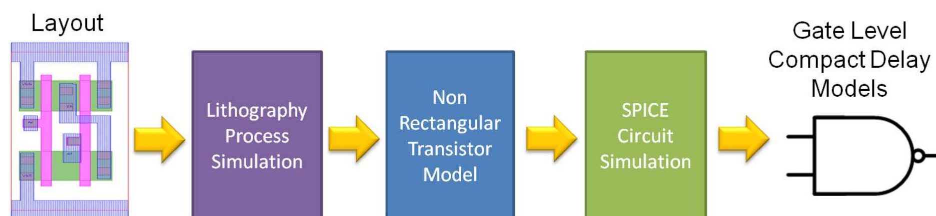


Figure 3.3: Standard Cell Variability Characterization Methodology

repeater circuit topology, and it is observed that the variations on each segment average out to reduce the overall delay variations. A through explanation of these studies is provided in Chapter 4.

3.5.3 Standard Cell Variability Characterization

Standard Cell Variability Characterization combines existing non-rectangular transistor models and timing libraries to create a variability aware timing model. Figure 3.3 illustrates the methodology.

To begin, a layout context is generated for the cell under study. Then rigorous process simulation, including OPC and lithography simulation, is performed on the layout at multiple points within the process window. For each specific process condition, the contour of each transistor is extracted to generate a new device model that can be used for circuit simulation. Circuit simulation is performed using the new device models to obtain the delay response. Finally the delays are aggregated and used to fit cell level compact timing models that can be integrated in existing design flows.

This framework was applied to standard cells in the Nangate 45nm Open Cell Library to characterize cell level electrical performance in the presence of lithography variations, including focus and exposure [10]. Electrical data obtained through this framework showed that the timing response in the presence of focus and exposure variations can be fit with a nine term compact model that can be stored in existing standard cell timing libraries. Details on the basic development of this compact model are provided in Chapter 5, and the advanced exploration into complex cells and additional sources of lithographic variation is covered in Chapter 6. This framework is also used with a few modifications to explore lithography aware path level circuit analysis and tradeoffs in Chapter 7.

3.6 Summary

Conventional methods of analyzing the circuit level impact of lithography variations are not likely to be used in design-time analysis due to the burden of computational power and runtime. A more compact and abstract level of lithography aware circuit analysis is needed to provide relevant information to designers and design tools so that the appropriate tradeoffs between lithography variability and other circuit metrics can be performed. To accomplish this goal, models and tools across the EDA spectrum are leveraged to create unique process and

design information frameworks that facilitate the transformation of process data into circuit performance. Consequently, three key frameworks are developed that allow for fast analysis of lithography variability in the context of circuit performance.

Chapter 4

Interconnect Variability Modeling

4.1 Introduction

Modern semiconductor chips contain as many as twelve layers of metal interconnect, each patterned with a separate mask and exposure step. Lithography induced process variations occur for each of these patterning layers. Traditional design methodologies guardband for these variations through corner case design and analysis. Design analysis of systematic lithography focus and exposure variations is not traditionally performed due to the extensive permutations of possible lithography variations for each level of interconnect, causing an explosion in the computational power needed for such analysis. Nonetheless, systematic lithography focus exposure variations will affect the dimension of wafer level features, ultimately affecting the circuit performance through changes in parasitic resistances and capacitances. In this chapter, we detail our studies of the circuit level impact of systematic lithography variability using the Interconnect Variability Characterization (IVC) framework, and discuss key observations of interconnect variability at the 90nm and 32nm technology nodes using a repeater circuit topology. For each of our studies, the circuit level response is then fit into a compact delay model that can be used to estimate the circuit level impact of process variations without the need for time consuming circuit simulations. Finally, we describe our efforts to extend the IVC framework that allows analysis of more complex interconnect scenarios.

4.2 Interconnect Delay

The total delay in a digital datapath can be decomposed into two components: the gate delay and the interconnect delay. These two quantities are not independent since the delay through the device is dependent on the load that it is driving. Thus when analyzing variations in physical interconnect layers, the effects of the source driver and load capacitance must be included for accurate analysis. Figure 4.1 shows the equivalent RC network for an inverter driving a load capacitance through an interconnect wire. The interconnect wire is modeled as a distributed RC network, and the resistance and capacitance of the driver, as well as the load capacitance, is included for accurate delay calculation.

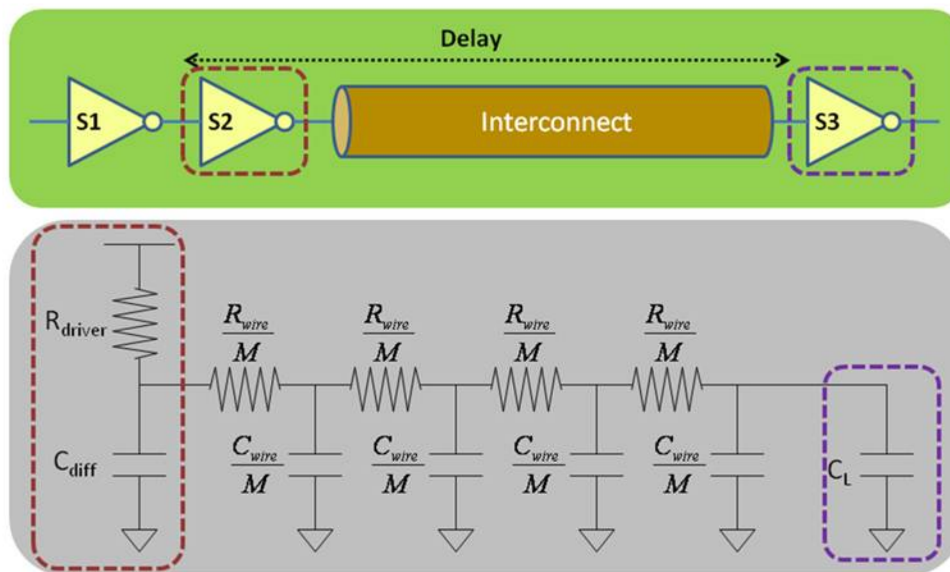


Figure 4.1: Interconnect equivalent RC delay model

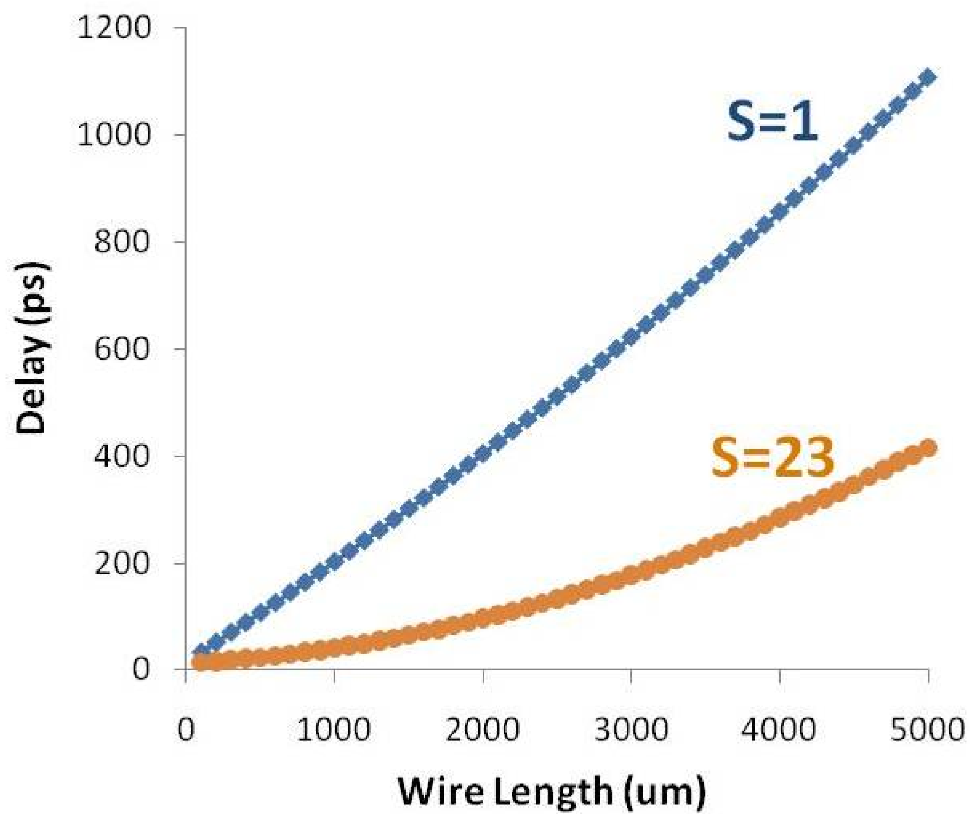


Figure 4.2: Delay as a function of length for driver size S

Figure 4.2 shows the characteristic response of the total delay as a function of length for two different driver sizes. There are two curves; one is linear and the other is quadratic with respect to length. The linear curve corresponds to the minimum sized device, which has a driver resistance of 20kΩ. The quadratic curve corresponds to a device of size 33, which has a driver resistance of 0.25kΩ. When the resistance of the driver is bigger than that of the wire, propagation delay increases linearly with the wire length [4]. In this mode of operation, the delay is dominated by delay through the device due to the limited amount of current provided by the driver. Increasing the size of the driver reduces driving resistance relative to the wire, resulting in a delay that is quadratic with respect to wire length. Modern high speed designs operate in this regime. Therefore the interconnect topologies studied in this work assume a large driver so that the overall delay is dominated by the interconnect delay.

To investigate the impact of lithography process variability at the interconnect levels, the Interconnect Variability Characterization framework, described in Section 3.5.2 and illustrated in Figure 3.2 is used. This framework leverages rigorous TCAD process tools to perform lithography characterization of small layout clips. These characterization results are generalized and used to create larger sized 1D interconnect layouts representative of post-lithography contours. The contours are then combined with parasitic extraction design analysis tools to determine the circuit level impact of lithography variability.

4.3 90nm and 32nm Process Technology Characterization

Integrated circuit manufacturers limit access to their official process design kits (PDK), which contain proprietary information about the process technology, device performance, and manufacturability targets. At the university level, access to these PDKs is difficult to achieve. PDK access is only made available through a non disclosure agreement which restricts any derived information can be used in publications, such as this dissertation. Thus, custom generated PDKs using assumptions from publicly available sources were used for this study.

Separate PDKs were generated for 90nm and 32nm technology nodes. The 90nm technology assumes a single lithography exposure and patterning step for each interconnect layer. In contrast, the 32nm technology assumes a double exposure and double patterning procedure. Device models for 90nm and 32nm high performance CMOS technology were provided by the NIMU group at Arizona State University [2, 42]. For each technology, a corresponding interconnect stack was derived using predictions from the ITRS roadmap[1]. The minimum intermediate metal pitch at the 90nm and 32nm nodes is 280nm and 90nm, respectively. Optimization methods from repeater insertion are applied to each technology to derive the optimal interconnect length L and driver sizing S [34]. The optimal values for 90nm technology are S=23 and L=921um. For 32nm, they are S=33 and L=58um.

Process technology assumptions are also derived from the ITRS roadmap [1]. Table 4.1 lists the parameters of the imaging system for both technologies. Lithography simulations are performed using SPLAT v6.0 for each technology, and the critical dimension (CD) for both technologies is measured using a 30% aerial intensity threshold for nominal exposure. The lithography focus-exposure (FE) process window, obtained empirically through simulation results, corresponds to a 10% change in CD. For 90 nm technology, this FE window ranges from

Table 4.1: Lithographic Simulation Settings

Technology Node	90nm	32nm
Lambda	193nm	193nm
Numerical Aperture	0.85	0.95
Illumination	Annular	Dipole
Sigma In	0.5	0.5
Sigma Out	0.9	0.9
Mask	Binary	EPSM
Patterning Steps	Single	Double
Nominal Aerial Image Threshold	0.3	0.3
Underexposed Aerial Image Threshold	0.306	0.306
Overexposed Aerial Image Intensity Threshold	0.294	0.294

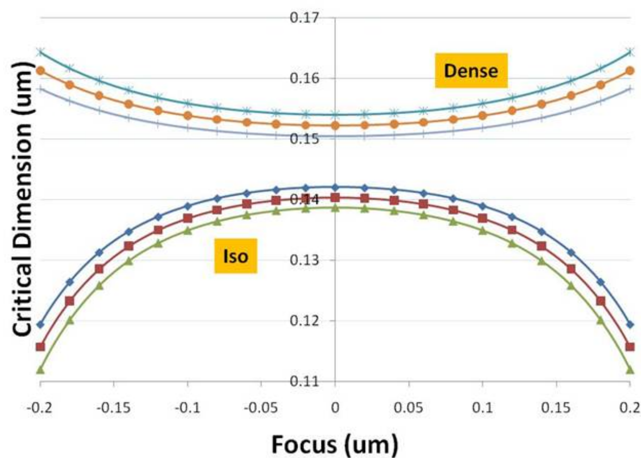
± 0.16um defocus and ± 2% exposure, and is shown in Figure 4.3a. The corresponding process window for 32nm technology is ± 0.10um defocus, ± 2% exposure, and ± 10% overlay error, and is shown in Figure 4.3b.

4.4 One Dimensional Interconnect Studies

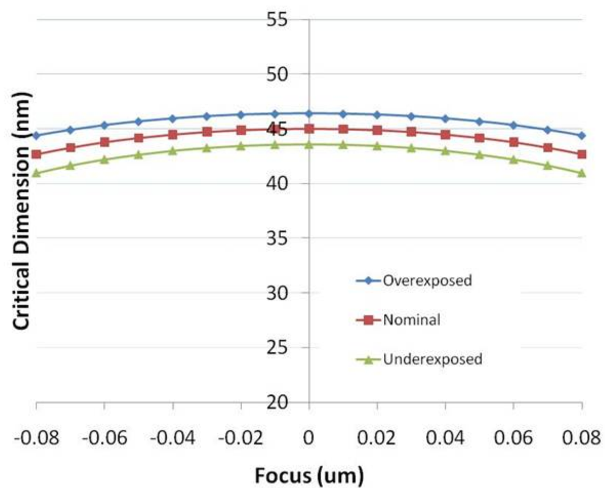
The general circuit topology used to characterize delay variations is shown in Figure 4.4. Three inverters, of size S1, S2, and S3, are connected sequentially in an inverter chain. S1 and S2 are placed in close proximity to minimize interconnect delay between the two. S2 drives S3 through the long interconnect wire of interest. A square wave with a 50% duty cycle is applied to the input of S1, and the average propagation delay is measured between the input of S2 and input of S3. This circuit topology is representative of repeater circuits, which propagate a signal from one area to a chip to another. The interconnect wires for each repeater segment tend to be lengthy and one dimensional in nature, thus making repeater circuit topologies an excellent vehicle for exploration of process variability using the Interconnect Variability Characterization framework.

4.4.1 90nm Single Patterning Results

Three interconnect scenarios are analyzed using 90nm technology characteristics. The first interconnect topology of interest is an isolated metal 4 minimum sized wire with no other features in the design as depicted in Figure 4.5a. The sizing of all the drivers and interconnect wire length was carefully chosen to be similar to the optimal values for buffer insertion in this technology. Figure 4.5b shows the response of delay across the process window. The worst case change in delay across the focus exposure (FE) window is 2.61ps (5.9%). The change in delay can be explained through an examination of lumped resistance, lumped capacitance, and lumped RC product at the nominal 30% aerial image intensity threshold (Figure 4.5c). The change in lumped capacitance is almost negligible, so the change in delay tracks the change



(a) 90nm Dense and Isolated Features



(b) 32nm Dense Features

Figure 4.3: 90nm and 32nm Bossung Curves

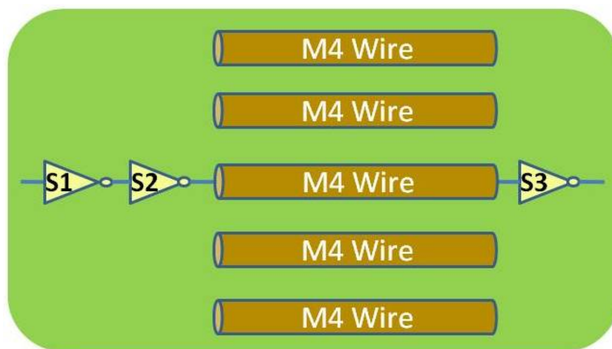
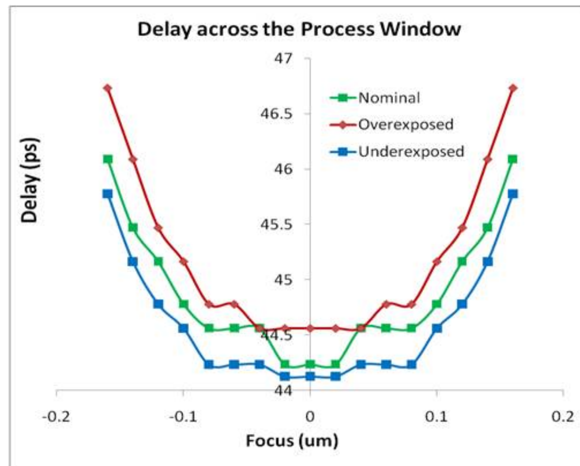
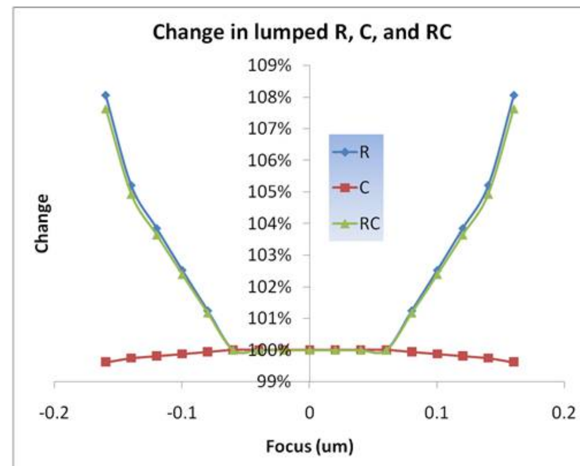


Figure 4.4: General Interconnect Topology

(a) Circuit Topology



(b) Delay Across the Process Window



(c) Change in Lumped Parasitics

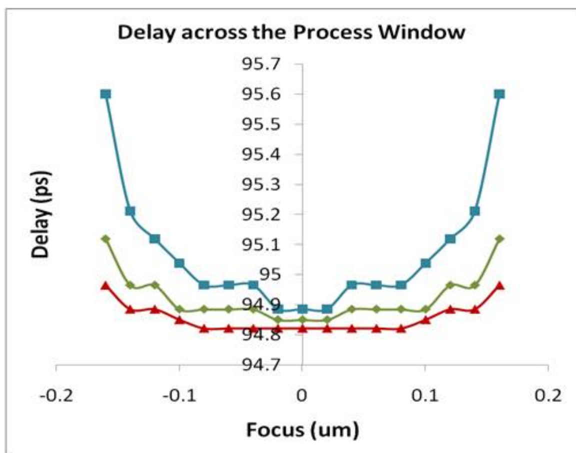
Figure 4.5: 90nm Interconnect Structure #1 (Isolated Wire)

in wire resistance very closely. While the CD of the isolated line is quadratic with focus, both Figures 4.5b and 4.5c exhibit bumpy curves which are an artifact of the layout discretization by the extraction tool. This tool snaps wafer level lithography contours to a nanometer grid, which is too coarse considering that the range of lithography induced geometrical variability is 10% of the nominal linewidth, or 14nm.

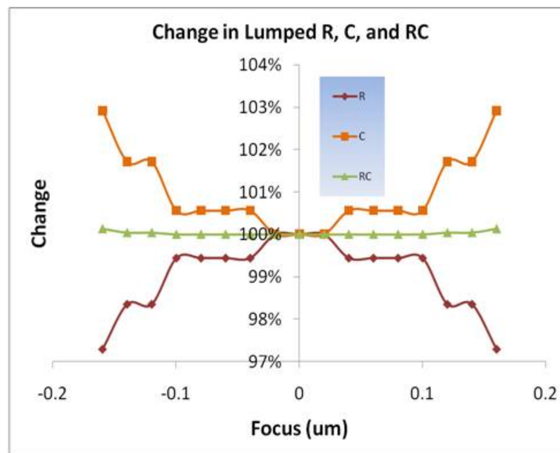
The second interconnect topology is shown in Figure 4.6a. The second inverter in the chain now drives the center metal 4 wire of a five line array. To model modern designs which contain features in every metal layer, the metal layers directly above and below contain features that run perpendicular to the wire at a 25% density. This interconnect layout has a well behaved response to FE variations, leading to only a 3.6% change in CD versus 10% for the isolated case. Figures 4.6b and 4.6c show the response of delay and lumped parasitics across the same process window. A worst case change in delay of 0.78ps (0.82%) is observed. Closer inspection of Figure 4.6c shows the lumped parasitic resistance and capacitance changing in opposite directions. This self compensating effect of resistance and capacitance minimizes the overall change in delay.

The third interconnect topology is shown in Figure 4.7a. Instead of driving the center wire of the five line array, the wire being driven is at the end of the array. This feature of interest is semi-isolated; it appears dense on one side and isolated on the other side. Again, features in the layers directly above and below run perpendicular to the wire at a 25% density. Plots of the delay and lumped parasitic are shown in Figures 4.7b and 4.7c. The worst case change in delay across the process window is 0.79ps (0.94%), and the self compensating effect is no

(a) Circuit Topology

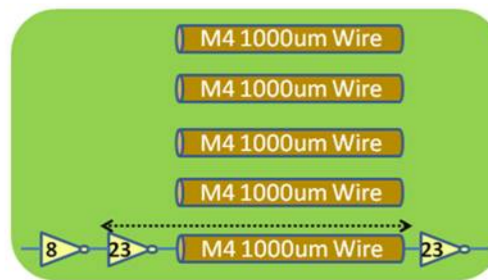


(b) Delay Across the Process Window

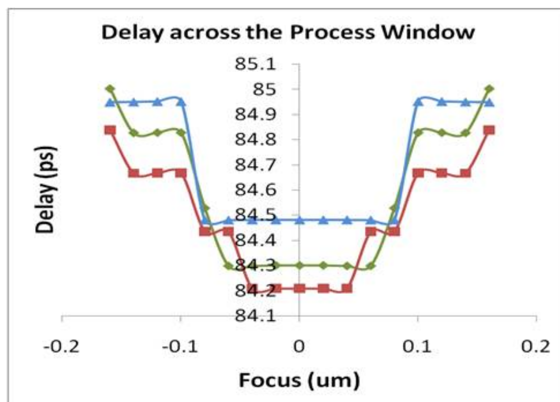


(c) Change in Lumped Parasitics

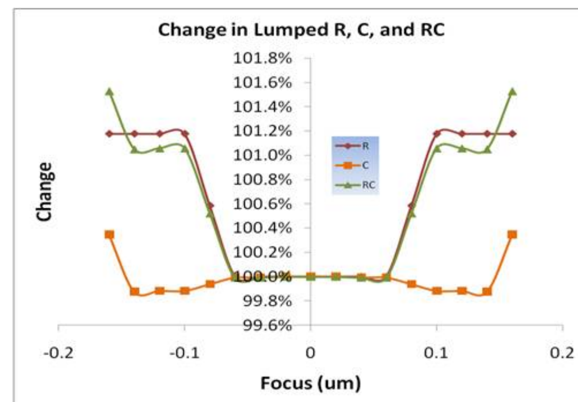
Figure 4.6: 90nm Interconnect Structure #2 (Center of Array)



(a) Circuit Topology



(b) Delay Across the Process Window



(c) Change in Lumped Parasitics

Figure 4.7: 90nm Interconnect Structure #3 (End of Array)

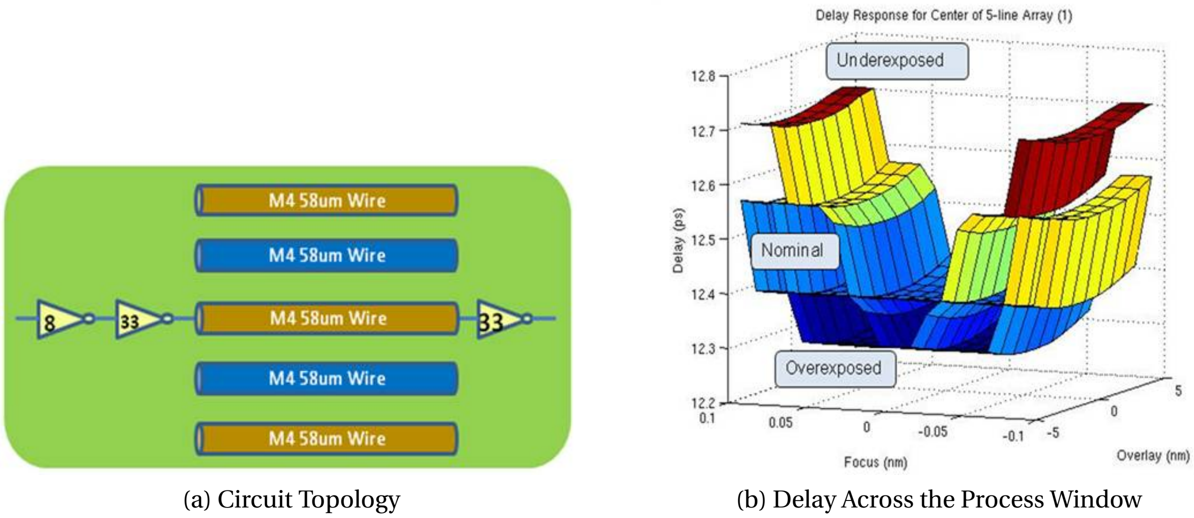
longer exhibited.

4.4.2 32nm Double Patterning Results

At smaller technology nodes, interconnect layers may be defined with multiple patterning steps. Thus, we proceed with interconnect variability analysis using 32nm technology, under the assumption that intermediate interconnect layers are defined using two separate exposure and patterning steps. Thus, proper variability analysis will also include modeling double patterning misalignment. Again, three different interconnect scenarios are investigated.

The first interconnect scenario is a five line array as depicted in Figure 4.8a. Again, the sizing of all the drivers and the interconnect wire length was carefully chosen to be similar to the optimal values for buffer insertion in this technology. The separate patterning steps are indicated by the color of the wires. Blue wires are at the nominal 45nm CD, while brown wires are affected by focus, exposure, and overlay variations. Figure 4.8b shows the response of delay across the process window. These delay surface curves exhibit granularity due to layout snapping by the extraction tool to the nearest 1nm grid. However, the delay exhibits a quadratic response with response to focus and overlay. For this topology, the worst case change in delay across the FE window is 0.42ps (3.4%).

The second interconnect example is shown in Figure 4.9a. Relative to our previous scenario, the blue and brown wires have been switched. In the previous case, the signal wire would



(a) Circuit Topology (b) Delay Across the Process Window

Figure 4.8: 32nm Interconnect Structure #1 (Center Array)

experience process variations. Now the signal wire stays at the nominal CD, while its direct neighbors experience process variations from the other patterning step. Figure 4.9b shows the delay response across the same process window. The worst case delay change is 0.22ps (1.7%).

The third interconnect example is shown in Figure 4.10a. Instead of driving the center wire of the five line array, the signal wire is the last wire in a 5 line array. As before, the blue wires are fixed at the nominal 45nm CD, while the brown wires undergo process variations. The worst case delay change across the process window is 0.323ps (2.69%) as observed in Figure 4.10b.

4.5 Compact Delay Modeling

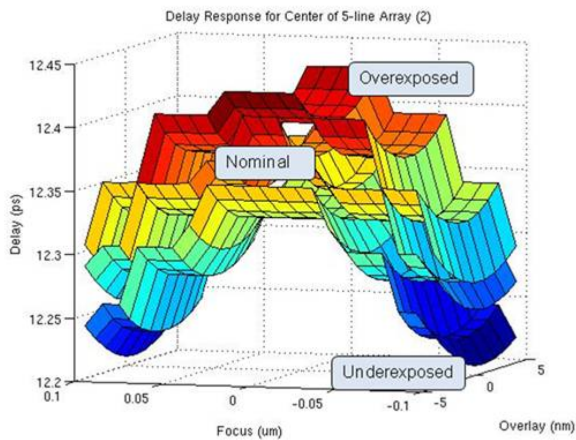
For one dimensional interconnect structures, the geometrical response with respect to focus and exposure is well behaved and easily modeled using a second order polynomial. Due to the one dimensional nature of this interconnect, the delay can be calculated using the RC product, which is a known function of silicon geometries. Since the mapping from process parameters to interconnect geometries and the mapping from geometries to timing are known, the delay response to focus and overlay is modeled using equation 4.1, where $A_1 - A_6$ are model fitting coefficients found using linear regression, focus is in units of um, and overlay is in units of nm.

$$\tau = A_1 focus^2 + A_2 focus + A_3 overlay^2 + A_4 overlay + A_5 focus \times overlay + A_6 \qquad (4.1)$$

The results of model fitting for the three interconnect scenarios analyzed with 32nm process technology (see Section 4.4.2) are listed in Table 4.2. The squared 2-norm of residuals is also included, and indicates the quality of the model fit.

There are some trends of interest that can be noted by looking at the coefficients for these model fits. Starting with the first term, the A_1 ($focus^2$) coefficient is positive in the first interconnect structure, and turns negative in the second interconnect structure. Therefore, the

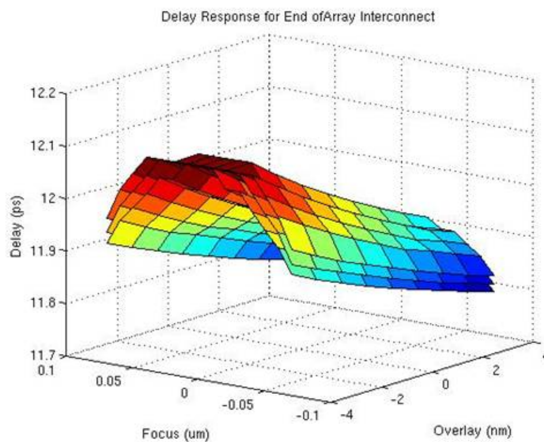
(a) Circuit Topology



(b) Delay Across the Process Window

Figure 4.9: 32nm Interconnect Structure #2 (Center Array)

(a) Circuit Topology



(b) Delay Across the Process Window

Figure 4.10: 32nm Interconnect Structure #3 (End of Array)

Table 4.2: Model Fitting Coefficients (Equation 4.1, includes focus and overlay)

Structure	Exposure	A_1	A_2	A_3	A_4	A_5	A_6	Residuals
#1	-2%	34.385	0.0000	0.0017	0.0014	0.0000	12.399	0.3429
	Nominal	24.900	0.0000	0.0018	0.0017	0.0000	12.318	0.2417
	+2%	20.932	0.0000	0.0019	0.0020	0.0000	12.261	0.2276
#2	-2%	-11.958	0.0000	0.0016	-0.0016	0.0000	12.320	0.0178
	Nominal	-10.817	0.0000	0.0018	-0.0016	0.0000	12.356	0.0264
	+2%	-11.543	0.0000	0.0019	-0.0014	0.0000	12.395	0.0253
#3	-2%	-26.094	0.0000	0.0009	-0.0235	0.0000	11.972	0.0142
	Nominal	-25.527	0.0000	0.0009	-0.0249	0.0000	11.991	0.0161
	+2%	-24.106	0.0000	0.0007	-0.0258	0.0000	12.009	0.0154

presence of variations in neighboring wires caused by a separate patterning step can alter the delay response of the circuit.

Looking at the other terms in the model, both A_2 $(focus)$ and A_5 $(focus \times overlay)$ coefficients are zero, indicating symmetric response through focus. In general, this may not be the case if the Bossung curves are tilted, which occurs in practice due to resist effects, lens aberrations, and electromagnetic mask edge effects.

Also, overlay variations for the third interconnect structure are much larger than for any of the other structures, exhibiting a delay response mostly linear to the degree of overlay. The coefficients for overlay are still smaller than those of focus, indicating that the defocus variability is a larger concern in this process technology.

Most of the coefficients show a trend to exposure level, suggesting that this model can be improved to account for exposure variations as well. Thus the model above was changed to account for exposure variations, resulting in a new model that handles focus, dose, overlay, shown in Equation 4.2.

$$\begin{aligned}\tau = {} & B_1 focus^2 + B_2 focus^2 \times dose + B_3 focus + B_4 focus \times dose + B_5 overlay^2 \\ & + B_6 overlay^2 \times dose + B_7 overlay + B_8 overlay \times dose + B_9 focus \times overlay \\ & + B_{10} focus \times overlay \times dose + B_{11} dose + B_{12} \end{aligned} \tag{4.2}$$

Additional terms were used to linearly model the change in coefficients with dose, in units of percentage variability. Since dose has primarily an inverse linear effect on linewidth, no second order dose term is included.

Table 4.3 shows the results of model fitting. Again, there are some trends of interest. The B_3 $(focus)$, B_4 $(focus \times dose)$, and B_{10} $(focus \times overlay \times dose)$ coefficients are zero, indicating minimal linear focus effects. As explained earlier, this may be attributed to the simulation environment which assumed largely ideal lithography conditions. For the lithography process window used in this study, the impact of dose variability is largely captured through B_2 $(focus^2 \times dose)$ and B_{11} $(dose)$ terms.

Table 4.3: Model Fitting Coefficients (Equation 4.2, includes focus, overlay, and dose)

Structure	B_1	B_2	B_3	B_4	B_5	B_6	
#1	26.7389	3.3633	0.0000	0.0000	0.0018	-0.0001	
#2	-11.4392	-0.1038	0.0000	0.0000	0.0018	-0.0001	
#3	-25.4520	-0.4969	0.0000	0.0000	0.0008	0.0001	
	B_7	B_8	B_9	B_{10}	B_{11}	B_{12}	Residuals
#1	0.0017	-0.0001	0.0000	0.0000	0.0344	12.3260	0.0855
#2	-0.0015	-0.0001	0.0000	0.0000	0.0188	12.3566	0.0712
#3	-0.0247	0.0006	0.0000	0.0000	-0.0093	11.9909	0.0459

4.6 Cascaded Interconnect Scenarios

The one dimensional scenarios studied in Section 4.4 provide insight into the nature of process induced interconnect variations and their effects on circuit performance. However, in most designs, a one dimensional assumption of interconnect routing is overly simplistic. The interconnection between two different devices on a chip will likely traverse multiple layers, and due to routing blockages and optimizations, the routing will include two dimensional features. The Interconnect Variability Characterization framework only supports analysis of one dimensional interconnect; however, to emulate more sophisticated interconnect scenarios, the framework was extended to allow analysis of cascaded interconnect segments.

The first scenario combines all three 32nm interconnect scenarios described in Section 4.4.2, and is shown in Figure 4.11. Instead of a single 58um segment of metal 4 interconnect, the new structure is composed of three equal-length segments of 19um. For the first segment, the signal traverses through the end wire of a five line metal 4 array. Then the signal traverses the center wire of a five line metal 5 array. The last segment, closest to the load, is the center wire of a metal 4 array that experiences opposite focus and exposure variations. Blue and red colors denote wires at the nominal 45nm CD, while black and brown colors indicate wires that undergo focus and exposure variations. During simulation, all subsections are assumed to go through the same identical process variation (i.e. a focus simulation of -0.5um results in defocus being applied to all segments).

The second three-segment structure is shown in Figure 4.12. It is very similar to the first structure, with the exception that the first and last segments are switched. This structure was selected so that there would be more resistive changes in the first segment and more capacitive changes near the end of the wire. According to the Elmore delay model [34], such a structure would have larger delay variability across the process window.

Surface plots of the delay response are shown in Figures 4.13 and 4.14. For the first three segment interconnect, the worst case change in delay is 0.1250ps (1.06%). The second case has a worst case delay of 0.191ps (1.62%). In both of these structures, the amount of variability seen is smaller than the weighted average of delays of the one dimensional models in the previous section. Additionally, the delay responses for each exposure cross. This suggests that the effects of these variations on each segment add and subtract, thus averaging out.

Figure 4.11: Three Segment Interconnect Structure #1

Figure 4.12: Three Segment Interconnect Structure #2

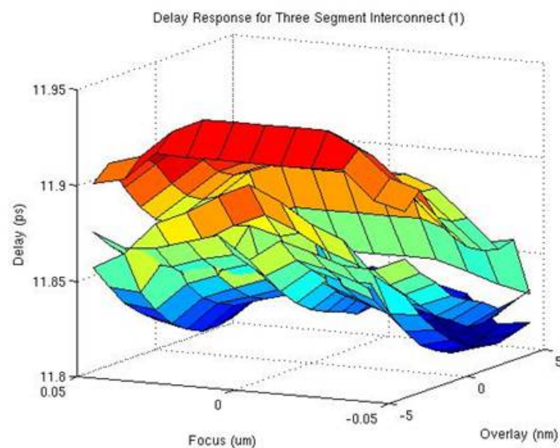


Figure 4.13: Delay Response for Three Segment Interconnect Structure #1

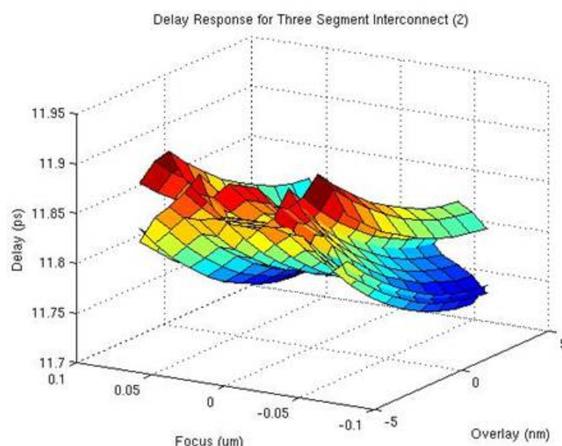


Figure 4.14: Delay Response for Three Segment Interconnect Structure #2

4.7 Summary

Performing design analysis of interconnect variations can prove to be challenging with multiple sources of variability for each of the interconnect layers in the chip. The Interconnect Variability Characterization (IVC) framework is utilized to examine the impact of lithography focus and exposure variations on one dimensional interconnect layouts patterned by single and double patterning, using a repeater circuit topology for analysis. For single patterned interconnect, dense interconnect features exhibit smaller variability in delay (less than 1%) due to self compensating resistance and capacitance and better CD control. Delay variability still is minimal (less than 3%) for double patterned interconnect, even for a signal wire that experiences no self compensating RC effect.

The delay response of each double patterned interconnect structure is fit using a second order polynomial model with focus, exposure, and misalignment input parameters, with 12 coefficients and a squared 2-norm of residuals of less than 0.1ps. These compact models provide designers insight into the degree of delay variability that specific circuit topologies and interconnect routing scenarios create. Though only a limited number of interconnect scenarios were studied using this framework, the compact modeling of interconnect variability can be extended to study other circuit topologies and interconnect scenarios.

To study the response of circuit timing for more advanced interconnect layouts, the IVC framework is extended to permit analysis of cascaded interconnect structures using the same repeater circuit topology. Using a combination of three different double patterned structures, two different types of multi-segment interconnect are created to explore the behavior of delay variations in multiple layout environments. It is observed that the variations on each segment average out to reduce the overall delay variations. This indicates that in the realm of double patterned interconnect, one possible solution to reduce circuit variability is to cross couple signal wires, at the expense of additional vias and routing length.

Chapter 5

Basic Standard Cell Variability Modeling

5.1 Introduction

As with interconnect level design analysis, transistor and cell level design analysis are also performed using corner case scenarios that do not model the impact of systematic lithography process variability. This chapter expands upon the study of process variability presented in the previous chapter, focusing now on lithography variability on front end of line active and poly layers, in the context of standard cell based designs. These process effects produce changes in each transistor that in-turn affect the timing characterization of the cell. The goal of this chapter is to develop compact models that encapsulate the process variability dependent behavior of cell timing performance. To achieve these models, two unique approaches are presented. The first utilizes an approach that applies geometrical biasing to transistor dimensions. The second utilizes lithography contour based analysis to map wafer level contours to device and ultimately circuit level performance. Each of these approaches produces a unique timing model that can be used to provide quick path estimates of level circuit variability. A comparison of the speed, compatibility, and required dataset size for each model is presented.

5.2 Standard Cell Delay Characterization

A digital signal propagates through a standard cell via a timing arc or timing path within the cell. The output waveform is a function of the input waveform, the timing arc, and the load capacitance. Figure 5.1 shows the signal propagation from input A of the NAND2 cell to output ZN.

The propagation delay associated with a timing arc is the time difference between transitions at the input and the output. Standard cell libraries contain timing models for each cell that contain pre-characterized propagation delays for selected combinations of timing arc, input signal transition time, and load capacitance [5]. Static timing analysis tools utilize these timing models to perform analysis of circuit timing paths, thereby eliminating the need for circuit level simulation which can be very time intensive. An example timing model is shown in Table 5.1.

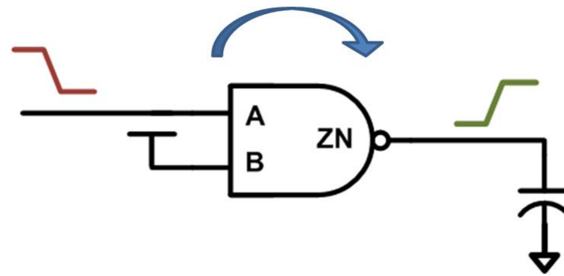


Figure 5.1: Signal Propagation of a 2 Input NAND Gate from Input A to Output ZN

Table 5.1: Sample Propagation Delay Table (ps)

Load Capacitance / Input Transition Time	0.4 fF	0.8 fF	1.6fF	3.2fF
15 ps	38.6	48.5	67.9	106.4
30 ps	42.1	52.0	71.5	110.1
60 ps	49.5	59.3	78.8	117.5
120 ps	65.3	74.8	94.0	132.5

5.3 Geometrical Biasing of Rectangular Transistors

A simple and fast approach to creating variability aware timing models is to apply geometrical biasing on rectangular transistors. To illustrate this point, a minimum sized inverter is taken from the Nangate 45nm Open Cell Library [14]. Both PMOS and NMOS transistor lengths (L) are systemically varied such that all transistors experience the same gate length change, and the propagation delay is measured after SPICE circuit simulation. Figure 5.2 shows that propagation delay behaves linearly for two different output transitions: output fall and output rise.

This linear behavior allows modeling of the propagation delay response with a single number that represents the delay sensitivity to L in units of ps/nm. This delay sensitivity is extracted by taking the slope of each line in Figure 2b. These values can be extracted for each combination of input transition time, timing arc, and load capacitance to create delay sensitivity tables that complement existing standard cell timing libraries. Delay sensitivity tables combined with a presumed distribution of variability in L for each cell in a synthesized design enable static timing analysis techniques to assess critical path process induced delay variability. An example delay sensitivity model is shown in Table 5.2.

The delay response to systemic changes in transistor width (W) also behaves linearly and thus a similar delay sensitivity table for W can similarly be created to complement existing standard cell timing libraries.

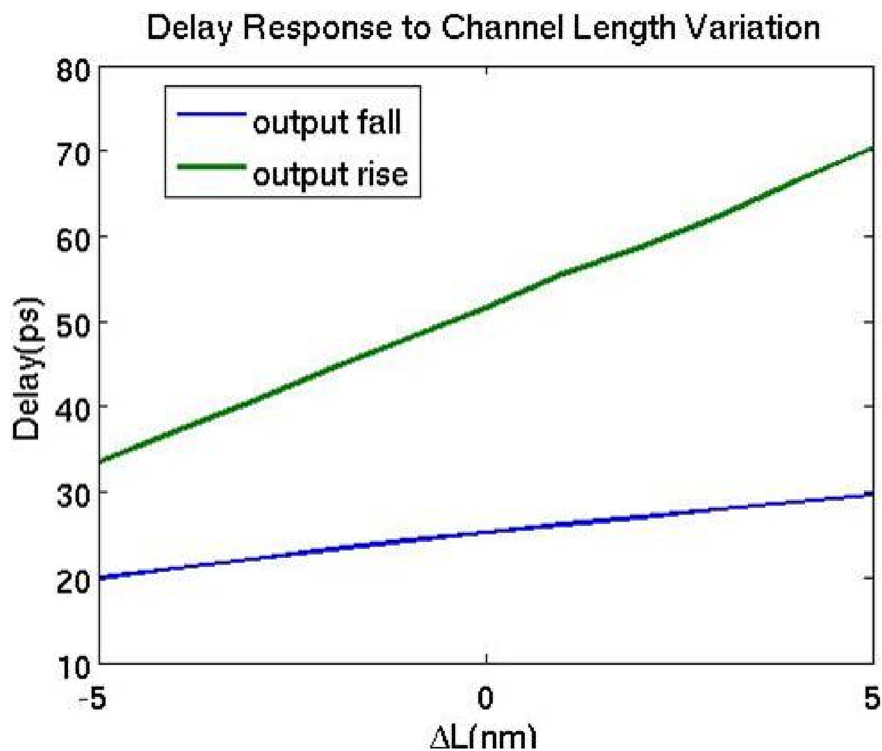


Figure 5.2: Delay Response of a Minimum Sized Inverter to Systemic Changes in Channel Length L

Table 5.2: Delay Sensitivity to Systemic L Variations for a NAND4 Timing Path

Load Capacitance / Input Transition Time	0.4 fF	0.8 fF	1.6fF	3.2fF
15 ps	2.77	3.50	4.91	7.78
30 ps	2.84	3.55	5.02	7.85
60 ps	2.97	3.72	5.18	8.05
120 ps	3.20	3.98	5.49	8.40

5.4 Contour Based Timing Characterization

5.4.1 High Level Overview

A more detailed and rigorous approach to characterizing standard cells with different variability sources involves the analysis of wafer level contours and the modeling of non-idealities in device performance. This differs from the approach of geometrical biasing discussed in the Section 5.3 as it goes much further to transform process level effects into cell level performance, requiring complex integration of process, device, and circuit level simulation. The Standard Cell Variability Characterization framework detailed in Section 3.5.3 is used to perform such characterization, and utilizes the five step approach shown in Figure 3.3. First a layout context is generated. Secondly, rigorous process simulation is performed on the layout at multiple points within the process window. It is assumed that all transistors within a cell experience identical process variations. For each specific process condition, the contour of each transistor is extracted to generate a new device model that can be used for circuit simulation. Circuit simulation is performed using the new device models to obtain the delay response. Finally the delays are aggregated and used to fit a gate level compact delay model. This analysis is performed using the Nangate 45nm Open Cell Library in conjunction with the FreePDK45 design kit [38].

5.4.2 Lithography Models and Simulation

Optical and resist models corresponding to a 193nm immersion lithography process are developed specifically for use in process simulations. Detailed lithography settings are listed in Table 5.3. The range of focus and exposure variations is carefully chosen to target a 45nm feature size with 10% overall critical dimension variation. This translates to 0.6 Rayleigh Units of focus variability and 3% exposure-induced intensity variability. These lithography settings are also used in performing optical proximity correction (OPC) on drawn layouts and subsequent lithographic simulation on post-OPC layouts. Thus the results obtained using OPC simulation include reduced sensitivity after pre-compensation for lithography effects.

5.4.3 Contour Based Device Analysis

Each lithography contour is subsequently extracted to model changes in device performance due to geometrical non-idealities. The transistor region is sliced into multiple segments using an algorithm that accounts for both poly and active contours. A sample slicing result in shown in Figure 5.3.

Each slice represents a transistor with a unique W, L, and Vth. The current contribution from each slice is summed to obtain the current for the extracted transistor at multiple operating points. This methodology has been shown to match 3D TCAD device current simulations results with an average accuracy of 2.7%, with errors as large as 7% for certain devices [7]. Though these errors may be considered substantial from a device current standpoint, in the context of CMOS cell transitions, there will be an imbalance of current going through the

Table 5.3: Lithography Simulation Settings

Lithography Optical & Resist Model Parameters	
Wavelength	193nm
Numerical Aperture	1.2
Illumination	Quasar
Illumination Angle	30 degrees
Sigma Inner	0.72
Sigma Outer	0.95
Nominal Aerial Image Intensity Threshold	0.3
Underexposed Aerial Image Intensity Threshold	0.309
Overexposed Aerial Image Intensity Threshold	0.291
Resist	n=1.7; k=0
Resist Thickness	100nm

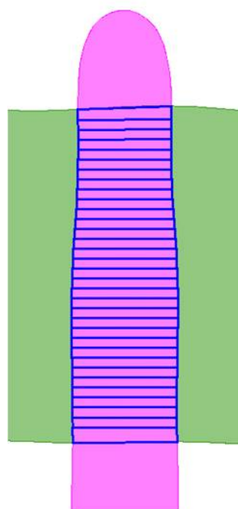


Figure 5.3: Transistor Slicing Example

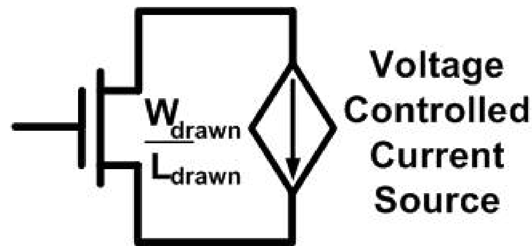


Figure 5.4: Accurate Table Lookup Based Device Model

PMOS transistors relative to the NMOS transistors. This imbalance means that deviations in device current map to smaller errors in timing performance.

After slicing the transistor and summing currents at multiple operating points, the contour extracted device behavior must be represented in a form compatible with circuit simulation. Several works model the new extracted device performance by fitting a new transistor or multiple transistors in parallel with effective transistor parameters (L, W, Vth, etc) at select operating points [33, 40, 7, 37], which may include I_{off}, I_{on}, and I_{lin}. However, such fits do not guarantee drain current equivalence at operating points other than those used for the fit.

Delay characterization requires a more accurate means of modeling transistor performance because circuit simulators iterate through multiple operating points for each transistor as signal waveforms transition. In this work, a table lookup method similar to the approach of Shi [36] is used to model the altered device performance. This is accomplished by placing a voltage controlled current source (VCCS) in parallel with the original transistor used for circuit simulation, as shown in Figure 5.4. The current supplied by the VCCS is the difference in currents between that of the drawn transistor and that of the contour extracted transistor. For this work, each transistor is characterized for multiple values of drain and source voltages in increments of 50mV and gate voltages in increments of 25mV. The only source of current mismatch occurs from interpolating currents at transistor operating points that have not been characterized. This interpolation error can be reduced by increasing the voltage step sizes at the cost of increased runtime.

5.5 NAND2 Cell Timing Analysis

5.5.1 Cell Schematic and Layout

The contour based timing characterization methodology is applied to a two input NAND cell placed in an isolated layout context. The circuit schematic and layout are shown in Figure 5.5. The following analysis examines the propagation delay response from a falling input A to a rising output ZN with fixed input transition time and load capacitance.

5.5.2 Poly Layer Focus Exposure Variations

First the delay response to focus and exposure (FE) variations on the poly layer is characterized. The process window used in this study is defined by the focus and exposure range that

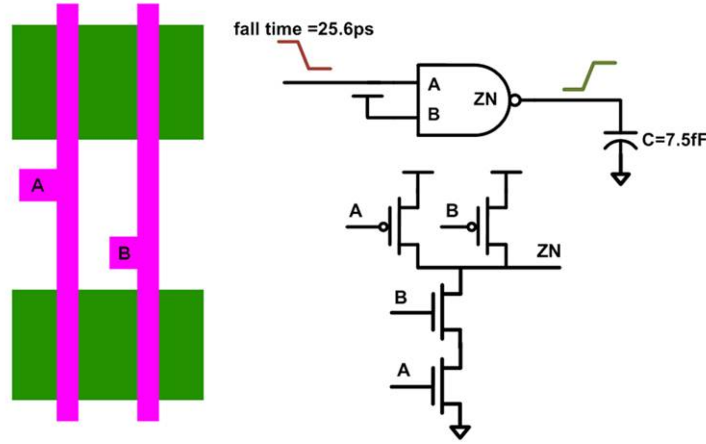


Figure 5.5: NAND2 Layout and Circuit Schematic

causes a 10% variation in poly transistor linewidth. This delay response appears similar to a Bossung plot of critical dimension. Thus the data points are fit using the equation 5.1 commonly used to fit standard Bossung plots as a function of focus F and exposure E [31]. A plot of the data points and model fit is shown in Figure 5.6. This nine term model fits delay data points with a RMS error of 0.19ps (0.3%). Several coefficients in the nine term model do not significantly contribute to the model fit. Eliminating these terms still yields in a good fit, with an elevated RMS error of 0.32ps (0.5%). The resultant five term model is shown in 5.2.

$$\tau = a_0 + a_1 F + a_2 E + a_3 FE + a_4 F^2 + a_5 E^2 + a_6 F^2 E + a_7 FE^2 + a_8 F^2 E^2 \tag{5.1}$$

$$\tau = b_0 + b_1 F + b_2 E + b_3 F^2 + b_4 F^2 E \tag{5.2}$$

5.5.3 Active Layer Focus Exposure Variations

A similar analysis is performed to characterize active layer FE variations. Again, a similar Bossung like delay response is observed across the process window. Poly and active delay responses to FE variations are shown in Figure 5.7. FE variations on the poly layer have a 38% impact on delay, while the same variations on the active layer have a 2% impact on delay.

5.5.4 Comparison of Two Different Layout Contexts

To investigate the impact of layout proximity effects, the results of poly FE variation for the isolated layout context are compared to a new layout context. The new layout context is shown in Figure 5.8 and consists of an array of identical NAND2 cells. The cell selected for analysis is the cell in the center of the array. Contour based timing characterization is applied to this target cell. Close examination of the PV-bands for the same cell under two different layout contexts show that the PV-bands only vary slightly, by 0.1nm. As a result, the difference in delay response to poly FE variations is minimal. The two delay responses are plotted in Figure

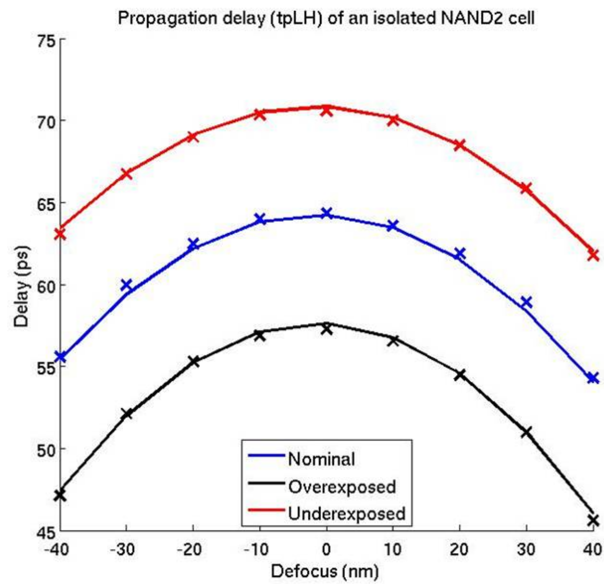


Figure 5.6: Propagation Delay Response to Poly Focus Exposure (FE) Variations with 9 Term Bossung Model Fit

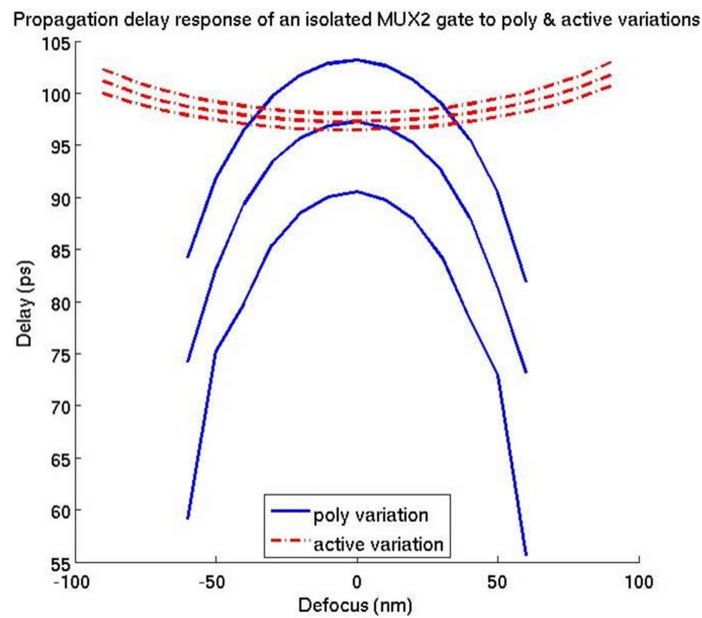


Figure 5.7: Propagation Delay Response to Poly and Active FE Variations

Figure 5.8: Second Layout Context for NAND2 Timing Characterization.

5.9, and the maximum observed delay difference across all selected process points is 0.27%. While the layout proximity effect studied in this specific scenario is small, there may be other layout configurations that induce a larger timing deviation. A more detailed investigation into layout proximity effects using a different cell is provided in Section 6.2.4.

5.6 Compatibility of Contour Based Compact Timing Models

Timing analysis for the NAND2 cell using contour based timing characterization shows that the delay response to focus and exposure variations exhibits Bossung-like behavior. Thus it is appropriate to use equation 5.1 for fitting Bossung plots as a basis for contour based compact timing models that complement standard cell timing libraries. However, if higher accuracy is desired, then the delay FE data points can be left in tabular form in standard cell timing libraries. As is the case with typical standard cell delay characterization, variability aware standard cell delay characterization should be performed for various combinations of input transition time, timing arc, and load capacitance.

The analyses presented in Section 5.5 are specific to a fixed timing arc, a fixed input transition time, and a fixed load capacitance. However, the same approach can be easily extended to develop variability aware delay models for each combination of timing arc, input transition time, and load capacitance. The Non-Linear Delay Model database provided in conjunction with the Nangate Open Cell Library contains timing data for each timing arc, for 48 different combinations of input transition time and load capacitance. In order to include information about lithography variability, this database needs to store information about the compact delay model. Since there are nine different coefficients required in the compact delay model, the existing database, currently consuming 3.5MB of space, would increase by a factor of 9X, to 31.5MB. This increased dataset size can still be reasonably used in conjunction with downstream design analysis tools, including static timing analysis.

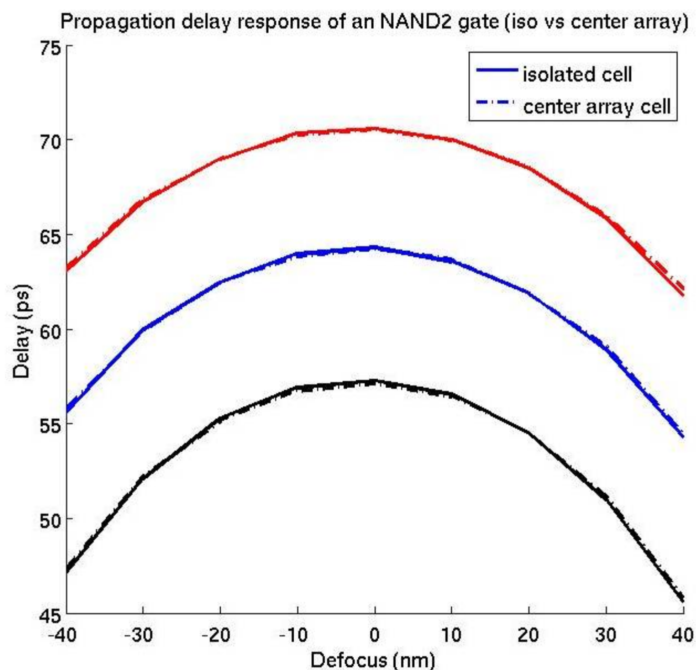


Figure 5.9: NAND2 Propagation Delay Response to Poly FE Variations for 2 Layout Contexts

5.7 Comparison of Variability Aware Timing Models

Two distinct variability aware timing models have been discussed in this chapter. The first model consists of calculated delay sensitivity based on the first order timing response to geometrically biased transistor dimensions. The second timing model consists of a nine term Bossung equation based on the timing response to lithography focus and exposure variations. Whereas as delay sensitivity models assume uniform transistor dimensions, contour based compact timing models more precisely model non-uniform transistor dimensions that can be caused by corner rounding and illumination effects. What both models have in common is that they are compatible with existing design methodologies because they complement existing standard cell timing libraries.

One of the significant differences between these two models is that their intended usage is different because each requires a different input parameter. Path level circuit analysis using delay sensitivity tables requires a distribution of geometrical variations, while the same analysis using contour based compact timing models requires a distribution of process parameters. Thus the usage of delay sensitivity models would be appropriate with knowledge or assumptions about across chip linewidth variation. Likewise the usage of contour based timing models would be appropriate to model focus variations across the lithography slit. While the examples provided are of specific position dependent effects, position dependent effects across different length scales (within-die, within-wafer, and within-lot) can be modeled using both of these methodologies.

Another difference is the storage space needed to include these models in existing standard

cell libraries. As explained in Section 5.6, contour based compact timing models increase the existing database size by a factor of 9X. In contrast, delay sensitivity models require storing one additional datapoint for each dimension of geometrical variation. To account for geometrical variations on both poly and active layers, the existing database size would increase by a factor of 2X. Even the larger 9X database increase should be acceptable for use with existing tools, as alternative dataset formats for the Nangate 45nm Open Cell Library are approximately this size as well (see Section 7.3 for additional detail).

The most significant difference between these two models is the computational effort required for cell level characterization. It takes a couple of seconds of SPICE circuit simulation to obtain delay sensitivity for one combination of timing arc, input transition time, and load capacitance using the NAND2 cell shown in Figure 5.5. In contrast, the simulation required for contour based analysis is much more intensive and takes 12 CPU hours on the same machine. This long runtime occurs primarily due to the contour based device analysis detailed in Section 5.4.3, which uses transistor contour segmentation and circuit simulation to derive new device characteristics in table lookup form. This runtime can be reduced by decreasing the frequency of transistor contour segmentation and reducing the number of transistor characterization operating points, at the cost of reduced accuracy. Finding the right balance between accuracy and speed is an interesting problem; however, runtime optimization is not addressed in this dissertation as effort is instead expended towards advanced cell characterization studies and path level applications.

5.8 Summary

Variability aware timing models that encapsulate lithography focus exposure variability are developed in this chapter. These timing models are compatible with existing cell based design methodologies and enable path level circuit analysis by moving time intensive lithography variability analysis into pre-design standard cell characterization. Two different approaches are used to develop these timing models, and it is assumed that all transistors within a cell experience identical process effects. The first approach utilizes geometrical biasing of transistor L and W in standard cells to create delay sensitivity tables. These delay sensitivity tables, combined with information about across chip, across die, and localized linewith variation, provides the designer insight into the impact of circuit path timing from these different sources of variability.

The second approach is more physically accurate and combines rigorous process simulation, compact transistor models, and circuit simulation to investigate the cell level electrical response of process variations. Using this approach, the delay responses for a 2 input NAND gate in the Nangate 45nm Open Cell Library are shown to exhibit Bossung like behavior, and are visualized in an electrical process window. The Bossung shaped delay responses are used to develop generic process parameter dependent delay variability models that are fit with an accuracy of under 1ps RMS error. With such a compact delay model for every cell in a standard cell library, designers can easy assess circuit level impact of different lithography process variability scenarios without the need for time consuming lithography simulation and contour analysis.

While the geometrical biasing approach is more approximate, it produces delay sensitivity tables that can be quickly derived and used in conjunction with typically collected across chip linewidth testchip characterization data. In contrast, the contour based approach is much more computationally expensive, but produces more precise contour based timing characterization models and captures some of the non-uniform geometrical effects along the edges of the transistor. This contour based approach will be applied to more complex gates and generalized for other applications in Chapter 6.

Chapter 6

Advanced Standard Cell Variability Modeling

6.1 Introduction

The contour based timing models presented in the previous chapter provide a starting point for the development of a comprehensive and complete variability aware standard cell library. Those models were derived upon analysis of a single stage logic gate with a very regular and uniform layout style. In this chapter, a more complex cell is selected for analysis to determine if the same compact models are still applicable. The selected cell, a 2:1 multiplexer, contains a more complex layout with multiple stages of logic and exhibits increased layout proximity effect due to two dimensional layout features. A delay characterization of this cell is performed using the contour based timing characterization methodology detailed in Section 5.4, for both active and poly focus exposure (FE) variations, misalignment variations, and different layout contexts. This same cell is then used to investigate how delays and layout proximity effects of a single logic stage combine to develop a multiple logic stage timing response. Finally, the feasibility of extending compact modeling to power analysis and sequential cell timing characterization is explored. The entire analysis of this chapter utilizes the FreePDK45nm toolkit, the Nangate 45nm Open Cell Library, and process technology parameters described in Section 5.4.

6.2 MUX2 Timing Analysis

6.2.1 Cell Schematic and Layout

The 2:1 multiplexer cell is placed in an isolated layout context and run through the contour based timing characterization methodology. This cell was specifically chosen due to its unique layout characteristics and multiple stages of logic. Unlike the NAND2 gate shown in Figure 5.5 which contains a very regular layout, this cell contains jogs in both active and poly layers, which increases the layout proximity effect from neighboring layout context. The cell schematic and

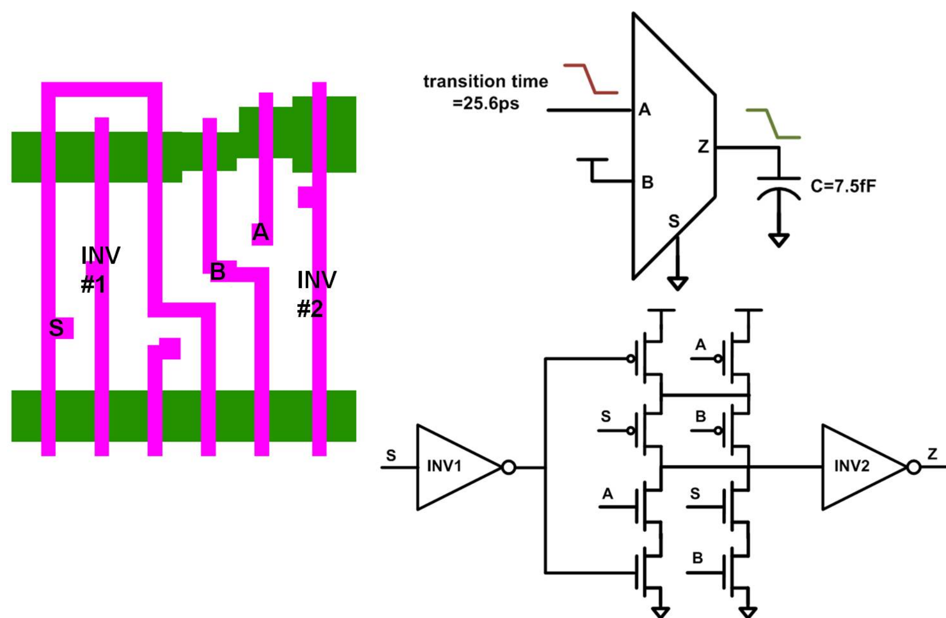


Figure 6.1: MUX2 Layout and Circuit Schematic

layout are shown in Figure 6.1. The following analysis examines the propagation delay response from a falling input A to a falling output Z with fixed input transition time and load capacitance.

6.2.2 Poly and Active Layer Variations

The delay response to poly and active layer focus exposure (FE) variations are compared in Figure 6.2. A wider process window is used to examine the impact of non-ideal geometries such as active corner rounding and poly line end tapering. The poly process window used in this study is defined as the FE range that causes approximately 15% variation in poly transistor linewidth. Poly FE variations have a 48.9% delay impact, while active FE variations have a 6.6% delay impact.

6.2.3 Poly and Active Misalignment Variations

The impact of misalignment variability is studied by selecting contours from the edges of this process window. The contours associated with these process corners exhibit corner rounding that creates non-ideal transistor geometries, as depicted in Figure 6.3a. The poly contour corresponds to an overexposure with -60nm defocus. The active contour corresponds to an overexposure with +100nm defocus.

To model misalignment, the poly layer is shifted in both X and Y directions by ±10nm in increments of 2nm. Figure 6.3b shows that the delay response to X and Y misalignment has a gradient from the upper left to bottom right, resulting in a 5.7% impact on delay.

The impact of active corner rounding can be studied by examining cases with zero y misalignment. In this scenario, the poly layer shifts left and right, causing a 3.7% change in delay.

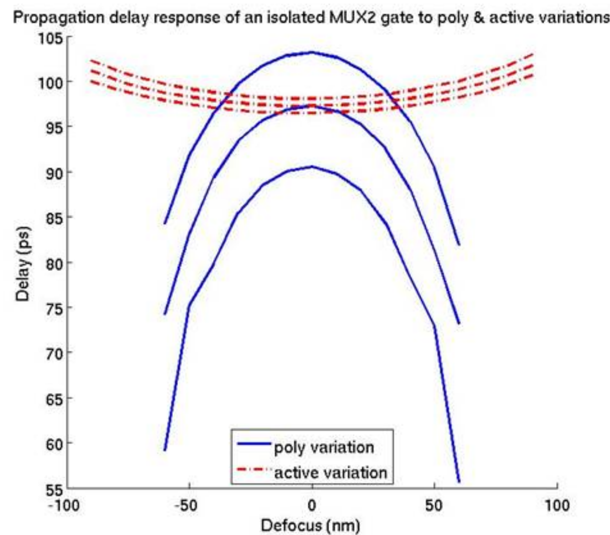


Figure 6.2: Propagation Delay Response to Poly and Active FE Variations

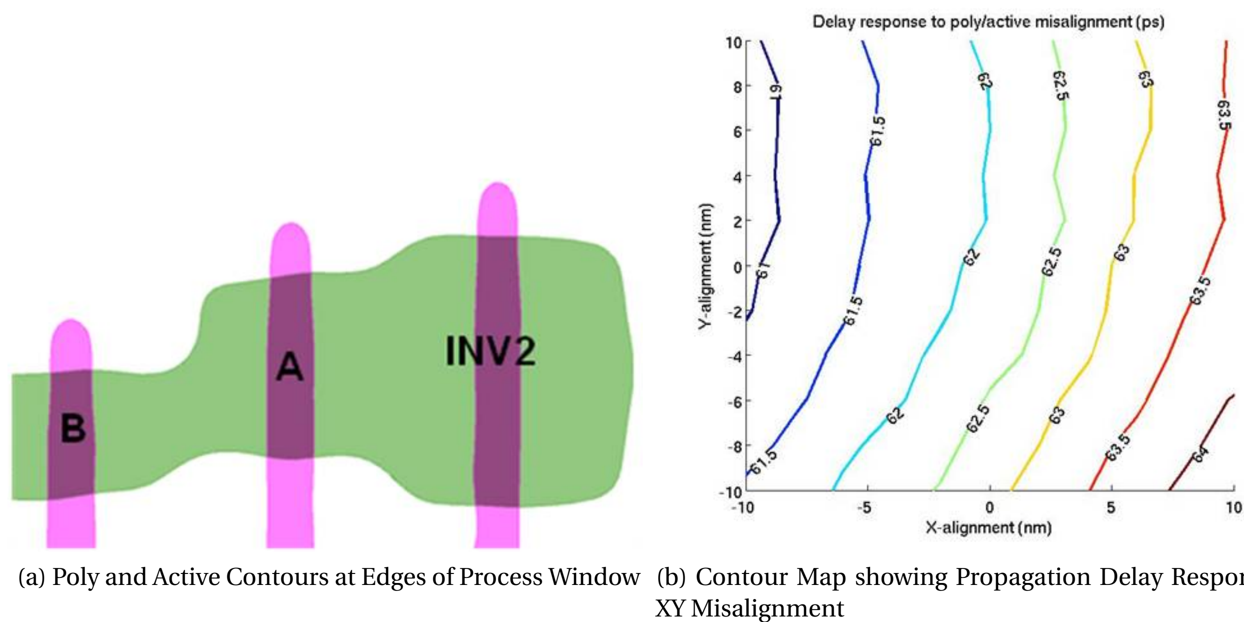
Similarly, the impact of poly line end tapering can be studied by examining cases with zero x misalignment, resulting in a 1.6% change in delay.

6.2.4 Comparison of Two Different Layout Contexts

A second layout context is generated to assess the impact of layout proximity effects. Two cells are placed adjacent to the MUX2 cell, one to the top and one to the right of the cell. The new layout context is shown in Figure 6.4a, and the MUX2 cell is highlighted in red. These cells are carefully selected to induce a large layout proximity effect on the PMOS transistors. This can be visualized through the XOR of the process variability bands for each layout context, shown in Figure 6.4b. The presence of color in the resulting XOR bands indicates a large layout proximity effect in that region of the cell.

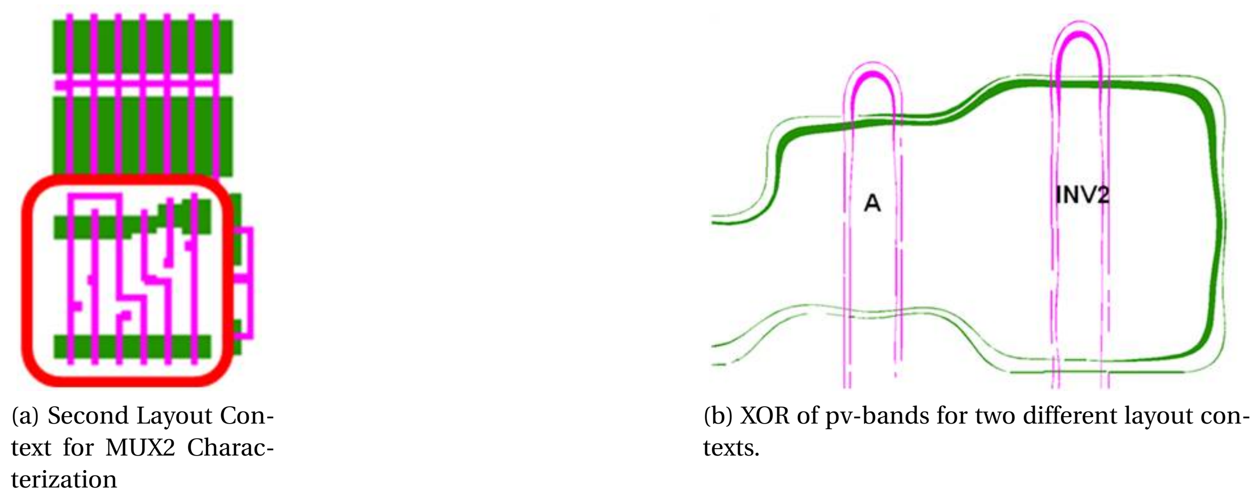
The largest differences in active FE variation due to layout proximity effect were observed to be associated with a rising transition at input A causing a rising transition at output Z. Using the timing arc, plots of active and poly FE variations for both layout contexts are shown in Figure 6.5a and Figure 6.5b. Differing layout proximity effects induce a 1.8% delay mismatch in the active FE window, and 5.4% delay mismatch in the poly FE window. These effects are most significant at the edges of the process window.

While this new layout context induces a large layout proximity effect leading to a large deviation in delay variability, there are many other layout configurations that can significantly alter device performance. The Nangate 45nm Open Cell Library contains 134 cells and is considered to be a small cell library. Even given a smaller library with 10 cells, there are a seemingly infinite number of layout contexts that can be explored, with permutations on the number, type, and exact placement of neighboring cells. However, this complexity may be reduced through the binning of layout proximity effects into categories based on density rules or distance to layouts in the adjacent cell.



(a) Poly and Active Contours at Edges of Process Window (b) Contour Map showing Propagation Delay Response to XY Misalignment

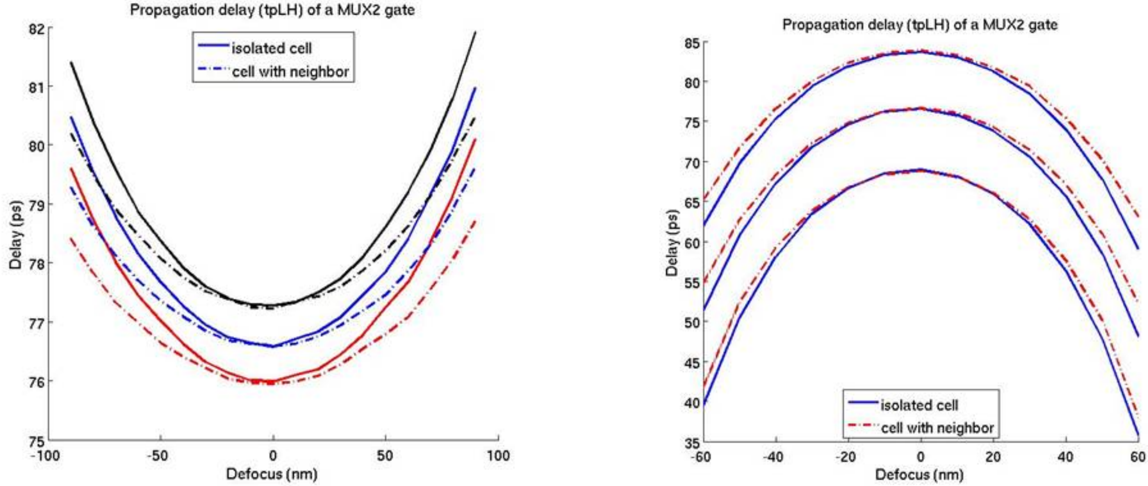
Figure 6.3: Poly and Active Misalignment Variations



(a) Second Layout Context for MUX2 Characterization

(b) XOR of pv-bands for two different layout contexts.

Figure 6.4: MUX2 Layout Context



(a) Second Layout Context for MUX2 Characterization (b) XOR of pv-bands for two different layout contexts.

Figure 6.5: MUX2 Layout Proximity Effect

6.3 Timing Components for Multiple Stage Logic Cells

The results in the previous section illustrate that the timing response for a two stage logic cell exhibits Bossung like behavior that can be captured by the compact timing model in equation 5.1. This is a general model that captures the overall timing response for both stages. This section delves deeper into the timing response and demonstrates that the overall timing response can be decomposed into components for each stage within the cell.

6.3.1 Core Delay Component

Along with the MUX2 cell, many other cells in the Nangate 45nm Open Cell Library contain multiple stages of logic. The nominal delay of timing paths equals the sum of the measured delays through each stage of logic. However, in the presence of process variations, the overall delay may not necessarily be equal to the sum of the delays of each stage due to slope effect and changes in signal waveforms at intermediate nodes.

To investigate whether the overall delay response across the FE process window can be predicted by summing up the delay contributions of each stage, the individual delays of each stage and total delay are shown in Figure 6.6. The sum of individual delays matches the total measured delay with a residual sum of square (RSS) of less than 10^{-5} ps. This small RSS confirms that the overall delay through this path can be accurately predicted by summing up delay components through each stage.

6.3.2 Layout Proximity Component

In Section 6.2.4, it was noted that the MUX2 cell layout context affects the delay response to FE variations. In effect, there is a layout proximity effect on both the overall timing path

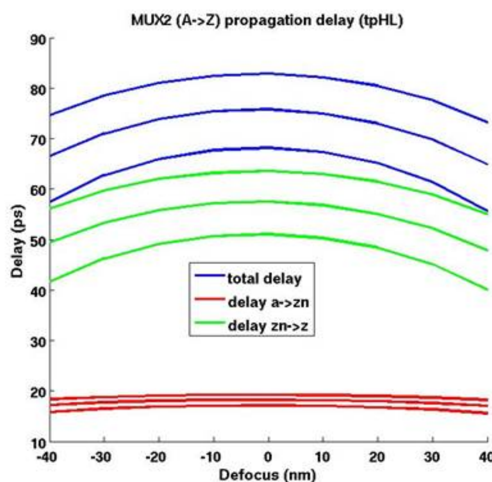


Figure 6.6: Delay Components of MUX2 Cell

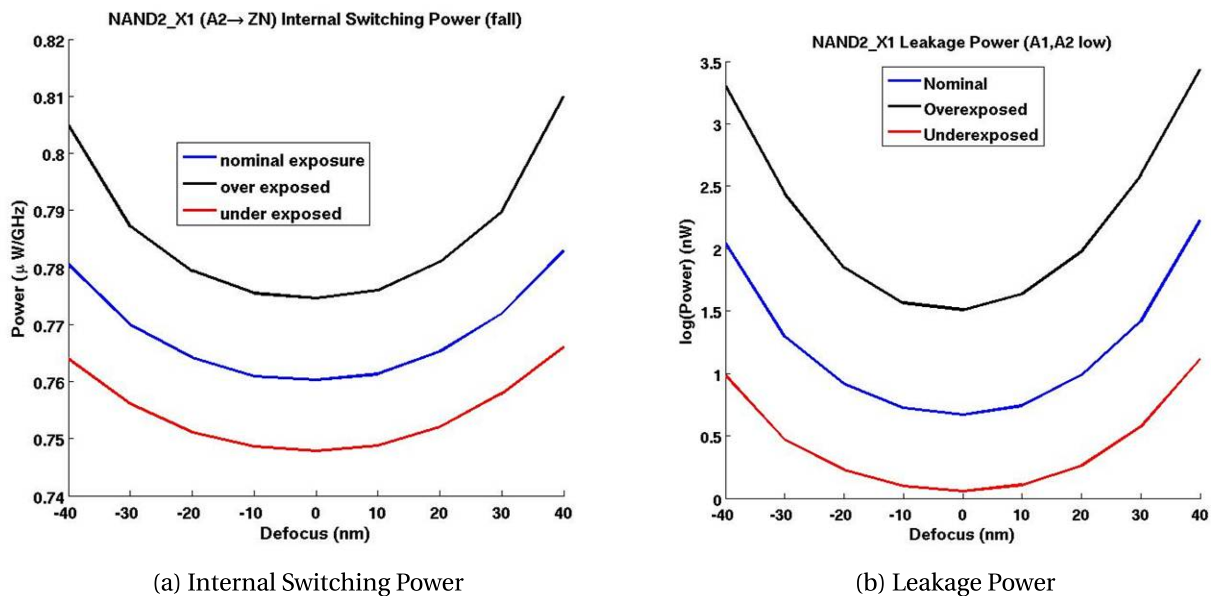
and individual delay stages. Of interest is whether the sum of the layout proximity effects of each delay stage is an accurate predictor of the overall layout proximity effect. Using the same simulation setup, the differences in delay for each stage are calculated and then summed to obtain an estimate of the layout proximity effect for the overall delay. It was found that this summation accurately matches the measured overall layout proximity effect seen in Figure 6.5b with a RSS of less than 10^{-4} ps.

6.4 Extension to Sequential Cell and Power Characterization

To this point, compact lithography variability timing models have been shown to be compatible with single and multiple stage combinational logic cells. In order to develop a complete variability aware standard cell library that can be used with downstream analysis tools, variability aware models need to be developed for both power and sequential cell characterization.

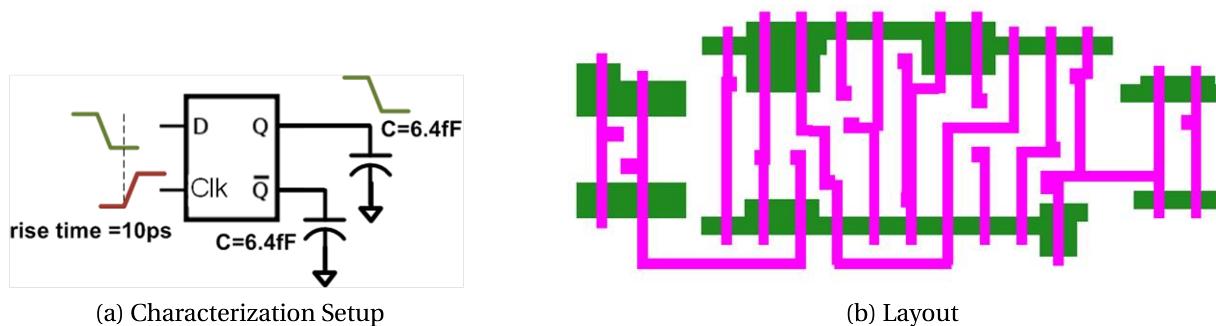
6.4.1 Power Characterization

The NAND2 gate shown in Figure5.5 is used for power characterization. To perform power characterization, the same contour based timing analysis methodology described in Section 5.4 is used. However, the circuit simulation setup needs to be slightly altered to add power measurement commands for analysis. Both the internal switching power and leakage power are characterized using the NAND2 gate, and results are shown in Figures 6.7a and 6.7b. Both plots illustrate that the power response due to lithography FE variations illustrate Bossung like behavior that can be captured via the same underlying compact model used in timing characterization, shown in Equation 5.1. These contour based power variability models can be developed in conjunction with timing characterization of the same cell, and enable power analysis to be included in path level variability analysis.



(a) Internal Switching Power (b) Leakage Power

Figure 6.7: NAND2 Power Characterization



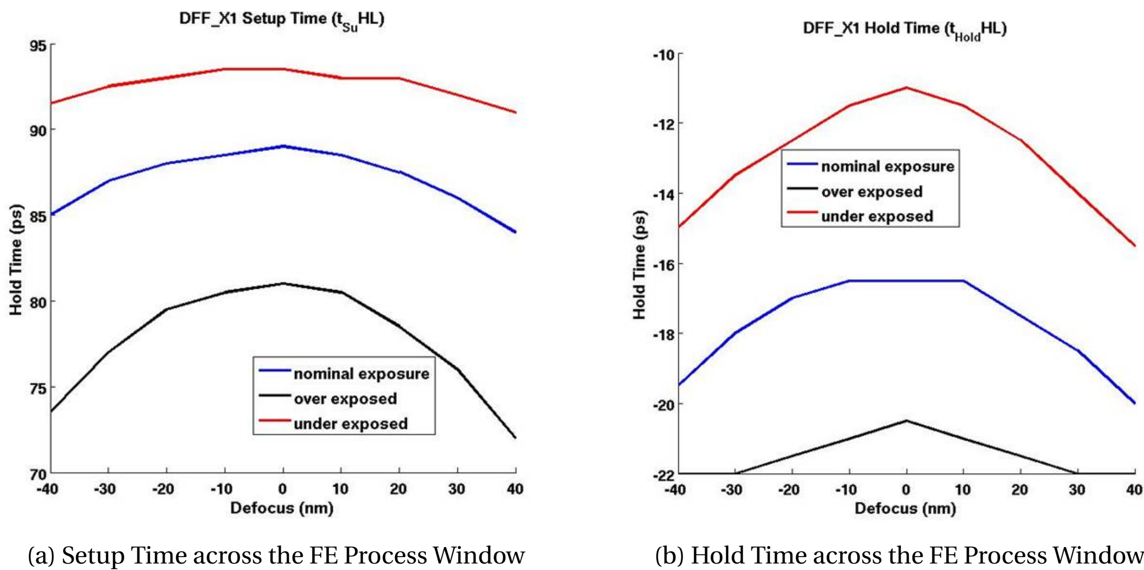
(a) Characterization Setup (b) Layout

Figure 6.8: D Flip Flop (DFF_X1) Cell

6.4.2 Sequential Cell Characterization

The D Flip Flop (DFF) cell from the Nangate Open Cell Library is used for sequential cell timing characterization. The characterization setup and cell layout are shown in Figures 6.8a and 6.8b.

As with the previous studies, the same contour based timing analysis methodology is applied. However, minor modifications need to be applied to the circuit simulation netlist to measure the clock to output (CLK to Q) delay for multiple arrival and departure times of the input switching signal. These CLK to Q delays are used to determine the setup and hold time for this sequential element. For this analysis, the setup and hold time is defined as 110% percent of the nominal CLK to Q delay. The nominal delay is defined as the CLK to Q delay for an input signal that arrives long before and departs long after CLK transitions. Figures 6.9a and 6.9b show that the setup and hold time responses also illustrate Bossung like behavior that can



(a) Setup Time across the FE Process Window

(b) Hold Time across the FE Process Window

Figure 6.9: D Flip Flop Sequential Cell Timing Characterization

be captured with the same underlying compact model used for combinational timing characterization.

6.5 Summary

Studies of complex circuit topologies illustrate that the contour based timing models presented in Chapter 5 hold up for advanced characterization studies. Here the delay response to a more complex cell with multiple stages of logic and increased layout proximity effect is characterized, and like the simple cell detailed in Section 5.5, exhibits Bossung like behavior. Additionally, the identical methodology is utilized to investigate other process effects, including horizontal and vertical misalignment, and layout proximity. The complex delay response for a cell with multiple logic stages is investigated, and it is observed that the overall delay response can be decomposed into two elements, a core delay element and a layout proximity effect element, that are additive in nature. Finally, with slight modifications to the contour based timing analysis flow, power characterization and sequential cell timing characterization is performed on select cells, and the results indicate that the contour based timing model in Equation 5.1 can be applied to power characterization and sequential cell timing characterization results. Thus, with proper contour based characterization, a complete set of variability models can be derived for every cell in the standard cell library, allowing for a comprehensive path level circuit variability analysis solution.

Chapter 7

Path Level Variability Analysis in Cell Based Design

7.1 Introduction

The variability aware compact models shown in Chapters 5 and 6 transform process variability into cell level electrical performance. This abstraction of lithography variability provides a foundation for path level variability analysis without process simulation or circuit simulation. This chapter demonstrates the path level applications of these compact models using example circuits including multiple stage logic datapaths and dynamically oscillating ring oscillators. To demonstrate that lithography variability can be used as an additional quantitative parameter in design tradeoffs and optimization, the use of cell swapping to reduce timing variability is examined. Finally, the interaction between systematic and random variations is explored using a combination of Monte Carlo simulation methods and the Standard Cell Variability Characterization framework. The entire analysis of this chapter utilizes the FreePDK45nm toolkit, the Nangate 45nm Open Cell Library, and process technology parameters described in Section 5.4.

7.2 Path Level Circuit Analysis

7.2.1 Ring Oscillator Period Estimation

One circuit commonly found in digital designs is the ring oscillator, which is an oscillating circuit composed of an odd number of inverters connected back to back. With dynamically oscillating capacitances and voltages, ring oscillators are usually simulated using transistor level circuit simulation tools like SPICE. However, with the appropriate variability aware compact timing models, it is possible to estimate ring oscillator performance at multiple process conditions without post-layout lithography aware circuit analysis or SPICE circuit simulation.

An 11 stage ring oscillator is created using an inverter cell from the Nangate 45nm Open Cell Library, and the circuit schematic is shown in Figure 7.1. SPICE circuit level simulations are used to determine the input capacitance of each inverter and the rise and fall times at each intermediate node in the circuit. These values are then used to create variability aware com-

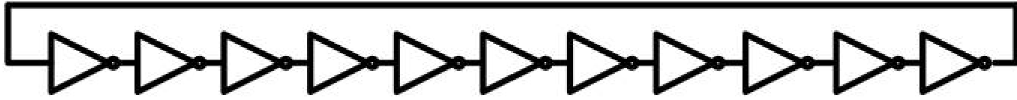
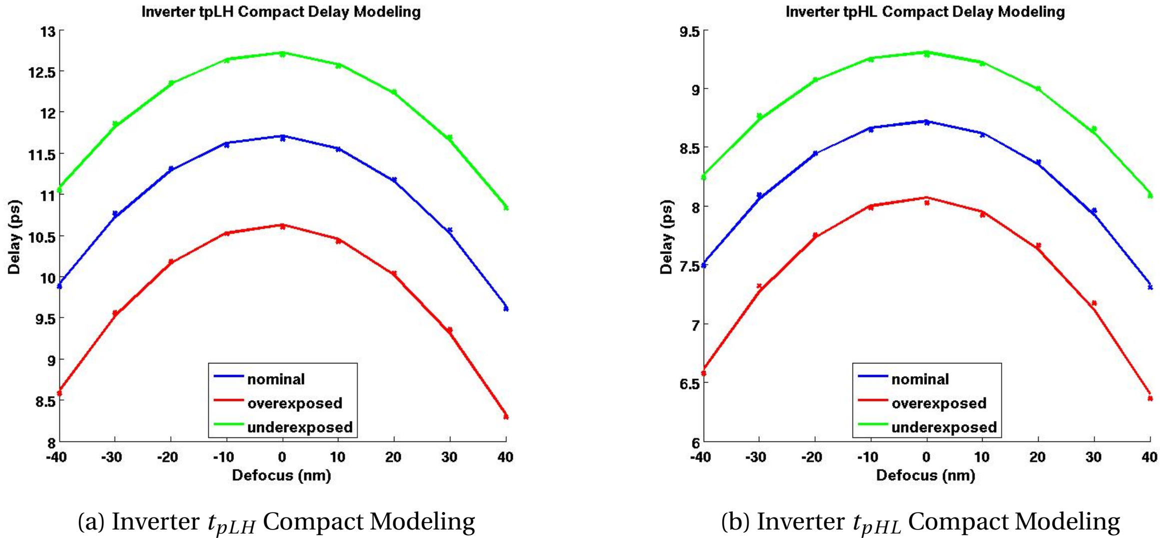


Figure 7.1: 11 Stage Ring Oscillator



(a) Inverter t_{pLH} Compact Modeling

(b) Inverter t_{pHL} Compact Modeling

Figure 7.2: Variability Aware Compact Modeling for Inverter Cell

pact models of the inverter cell using the Standard Cell Variability Characterization (SCVC) framework. Figure 7.2 shows the data points and model fit for propagation delays for both input transitions. The RMS error for each of the compact models is less than 0.4ps. By combining these compact models with the equation for the period of a ring oscillator, $N \times (t_{pLH} + t_{pHL})$, where N represents the number of stages and t_{pLH} and t_{pHL} represent propagation delays, the ring oscillator period can be estimated for various focus and exposure values.

Validation of the ring oscillator period estimations can be performed by applying the SCVC framework in a slightly different manner. The standard process of characterizing the through-focus and through-exposure behavior of the inverter cell in a fixed layout context is performed. However, a slight modification is made in the last step of SPICE circuit simulation. Instead of simulating one cell, the entire ring oscillator circuit is simulated using the newly derived device models for the inverter cell. This allows the process parameter dependent behavior of the ring oscillator to be characterized, under the assumption that the layout context impact of the inverter cell can be ignored.

A plot of the ring oscillator period estimations versus actual simulations is shown in Figure 7.3. The ring oscillator period estimations are shown as lines, while the actual simulation data points are plotted as X's. The RMS error of ring oscillator period predictions is approximately 2.23ps or 1% of the nominal delay. With existing 9-term variability aware compact models for the inverter cell, the period of the ring oscillator period for a fixed focus and exposure point can be estimated with one multiplication operation combined with a 9-term compact model×

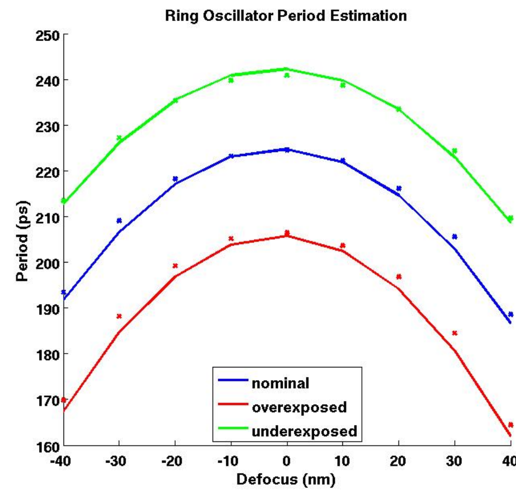


Figure 7.3: Ring Oscillator Period Estimation

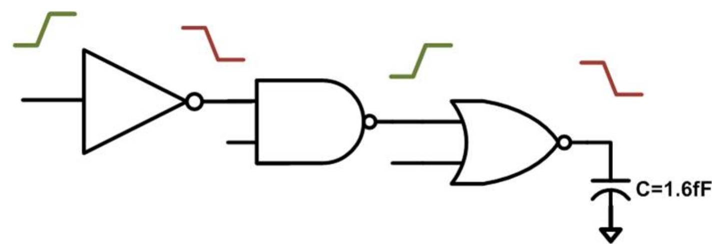


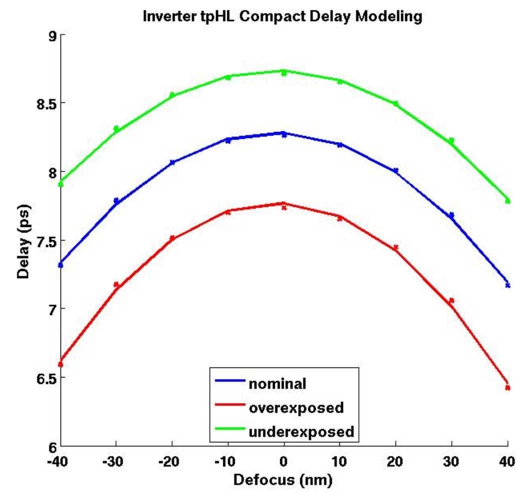
Figure 7.4: Three Logic Depth Circuit

2 compact model calculation. The time taken to obtain the ring oscillator period estimation for all 27 process points shown in Figure 7.3 is 0.26 seconds, which includes time for compact modeling of inverter delay behavior.

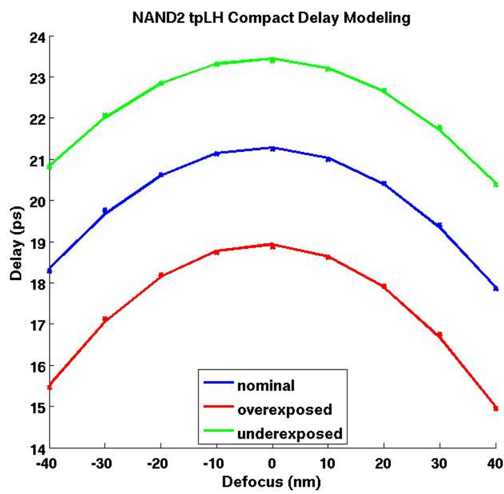
7.2.2 Circuit Path Delay Estimation

An estimation of the circuit path delay can also be derived using variability aware compact timing models. This is demonstrated using the three logic depth circuit shown in Figure 7.4, which incorporates an inverter, a NAND2 and a NOR2 gate. The SCVC framework is applied to all three gates to derive compact delay models for the nominal circuit operating points, and the data points and model fits are shown in Figure 7.5. The RMS error for each cell is less than 0.04ps. The circuit level path delay is estimated by summing up the delays of each individual stage, using the same methods as those incorporated in static timing analysis. In the context of our variability aware compact models, a summation of three 9-term compact models is used to estimate the behavior of the entire circuit path.

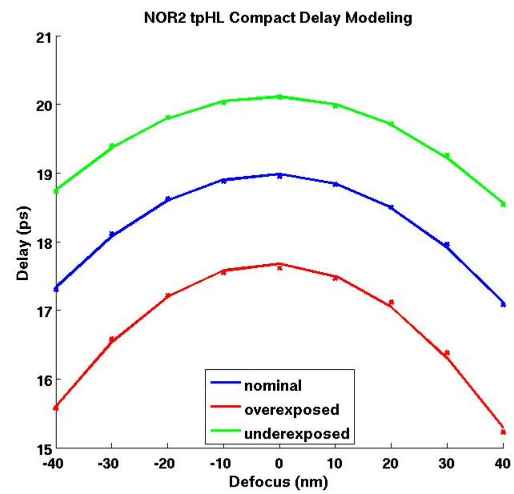
Similarly as with oscillator period estimation, the SCVC framework is also applied to simulate the entire circuit under a variety of process conditions. This allows the process dependent behavior of the circuit to be captured, under the assumption that the layout context impact of



(a) Inverter t_{pHL} Compact Modeling



(b) NAND2 t_{pLH} Compact Modeling



(c) NAND3 t_{pLH} Compact Modeling

Figure 7.5: Variability Aware Compact Modeling for Cells in Circuit Path

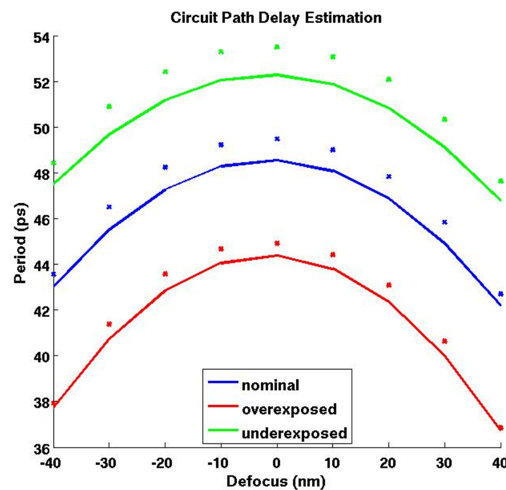


Figure 7.6: Circuit Path Delay Estimation

each cell can be ignored. Figure 7.6 illustrates the simulated circuit behavior across the focus exposure process window. The estimated path level circuit delay matches the simulated circuit behavior with a RMS error of 3.6ps (0.7%). The time taken to obtain the path level delay estimate is 0.85 seconds, which includes time taken for compact modeling of each of the three cells.

7.2.3 Speedup of Circuit Analysis with Compact Models

These cell level variability aware compact models speed up path level circuit analysis by shifting the post-layout lithography contour and device characterization upstream into pre-design characterization. To incorporate these compact models into existing standard cell libraries, the library dataset increases by an order of 9-fold since the compact models are based on Equation 5.1, a nine term compact model. For the Nangate 45nm Open Cell Library, the library dataset size is projected to increase from 3.5MB to 31.5MB. While this may seem like a large increase, alternative dataset formats (see Section 7.3) are approximately 30MB in size as well.

The primary benefit of storing these compact models in existing library datasets is that this information is made available to all physical implementation tools used to construct and analyze the design. With slight modifications to placement tools, electrical cell variability can be used as an additional consideration to determine exact cell placement. Similarly, with slight modification, static timing analysis tools can provide timing reports that include delay variability at multiple points in the circuit path.

The speedup in path level circuit analysis is enormous. Using conventional post-layout lithography aware circuit analysis, characterization time for 27 different focus and exposure conditions for the three stage circuit path shown in Figure 7.4 takes 12 CPU hours. With pre-characterized timing models, the through-focus and through-exposure behavior of this circuit can be estimated in well under a second, resulting in a speedup greater than 50,000. This num-

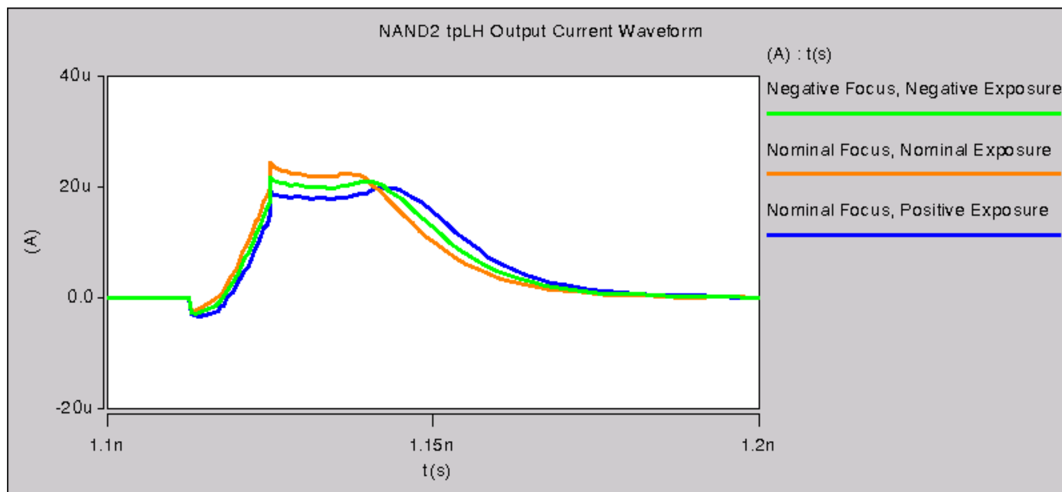


Figure 7.7: NAND2 tpLH Output Current Waveform

ber increases drastically with the logic depth of the circuit.

7.3 Composite Current Source Modeling

The variability aware compact models presented in previous chapters are based on non-linear delay models (NLDM), where the delay of a specific timing arc is characterized for different input slew and load capacitances. However, in recent years, alternative models have begun to emerge due to the limitations of NLDM to capture advanced effects in sub-100nm technologies. Details about these models are defined by the Open Source Liberty organization.

The Composite Current Source (CCS) format addresses some of these advanced effects. For path level delay calculation using NLDM models, the receiver at every stage is a fixed load capacitance. However, in reality, due to the Miller effect, the effective load capacitance changes as the output signal transitions. Delay calculation using the CCS format addresses the Miller effect by assuming the load capacitance changes as the output signal transitions. Studies show that migrating from NLDM to CCS formats increases static timing analysis accuracy with respect to SPICE simulation results from 10% to 2%.

The core difference between NLDM characterization and CCS characterization is the data format that is stored in the library dataset. NLDM models store the absolute delay between the input and output waveforms. CCS models store current waveforms for both input and output nodes, which can then be integrated to obtain the voltage waveforms and absolute delays.

To create variability aware delay models that are compatible with the CCS format, current waveforms instead of cell delays must now be stored in library datasets. The SCVC framework can still be used, with modifications to the final step of SPICE circuit simulation to capture current waveforms instead of measuring absolute delay. Figure 7.7 shows a suite of current output waveforms for the NAND2 gate shown in Figure 5.5, corresponding to different process points.

Though incorporating lithography awareness into CCS library datasets increases accuracy

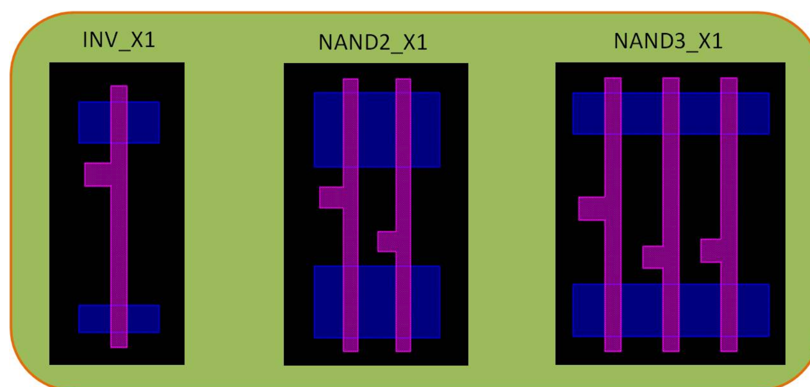


Figure 7.8: Cell Layouts

in variability aware analysis, this enhancement comes at a cost of library dataset size. CCS library datasets for the Nangate 45nm Open Cell Library are around 29MB in size. Adding 10 different process points into this library dataset will increase the library size by a factor of 10, to 290MB. This dataset size may be too large and unwieldy for path level circuit variability analysis.

7.4 Sensitivity Driven Circuit Optimization

Delay variability data automatically generated by the SCVC framework can be used in conjunction with other design metrics for library and circuit optimization. In parallel with standard NLDM models and variability aware compact timing models, delay sensitivity tables can be created for each timing arc, input slew, and load capacitance. Delay sensitivity, defined as the change in delay for a 3σ variation in process parameter divided by the nominal delay, provides a metric to compare the effects of different process effects within and across cells. A 3σ focus variation corresponds to 0.6 Rayleigh Units, while a 3σ exposure variation corresponds to a 3% intensity change at the wafer plane. Variations in threshold voltage are transistor geometry dependent, and can be calculated using Pelgrom's model, detailed in Section 7.5.2.

Table 7.1 shows delay sensitivities to 3σ variations in focus, exposure, and V_T for the NAND2 cell shown in Figure 5.5. Two observations are apparent from these tables. First, delay sensitivity from focus variations is nearly twice as large as that from exposure variations. Second, the impact of worst case V_T variations is much larger than focus and exposure variations. However, V_T variations are considered to be random instead of systematic in nature, and the path level delay variability will be largely reduced since the path level delay is a summation of independent variables, and the variance in delay decreases with the number of logic stages in the path.

Delay sensitivity can also be used to determine cell usage. Figure 7.8 shows the layout of three different types of cells: an inverter, a NAND2, and a NAND3 gate. When the SCVC framework is applied to these three cells, the delay sensitivity to focus and exposure for all three cells can be compared for a fixed input slew and load capacitance. Table 7.2 provides this comparison.

Table 7.1: NAND2 Delay Sensitivity Tables (from 3σ process variations)

(a) Focus Sensitivity (ps/3σ focus variation)

Load Capacitance / Input Transition Time	0.4 fF	0.8 fF
15 ps	0.0861	0.0859
30 ps	0.0950	0.0886

(b) Dose Sensitivity (ps/3σ dose variation)

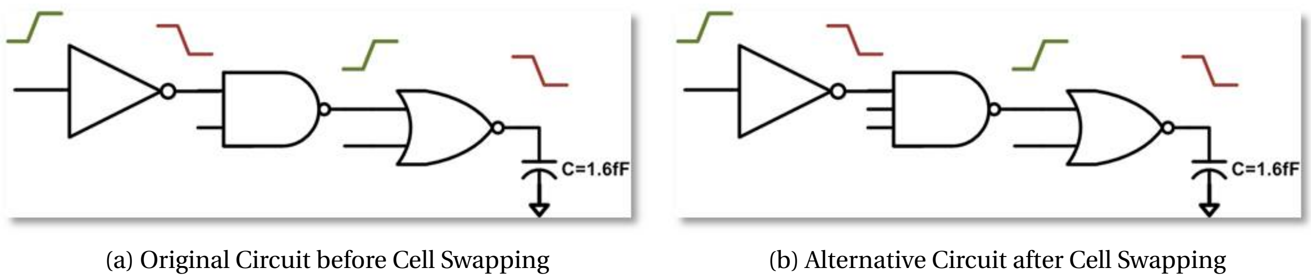
Load Capacitance / Input Transition Time	0.4 fF	0.8 fF
15 ps	0.0506	0.0501
30 ps	0.0492	0.0510

(c) V_T Sensitivity (ps/3σ V_T variation)

Load Capacitance / Input Transition Time	0.4 fF	0.8 fF
15 ps	0.2543	0.2549
30 ps	0.2512	0.2532

Table 7.2: Cell Delay Sensitivities for 3σ Focus and Dose Variations (ps/3σ variation)

Cell	Focus	Dose
INV	0.174	0.077
NAND2	0.170	0.118
NAND3	0.115	0.085



(a) Original Circuit before Cell Swapping (b) Alternative Circuit after Cell Swapping

Figure 7.9: Cell Swapping Circuit Scenarios

Table 7.3: Cell Swapping Circuit Tradeoffs for the 2 Circuit Scenarios of Figure 7.9

Circuit	Nominal Delay	Path FE Delay Variation	NAND Leakage Power	NAND Switching Power (uW/GHz)	NAND Area
Original	49.5 ps	16.2 ps	20.7 nW	1.83	1.33 um^2
Alternative	45.7 ps	13.7 ps	29.9 nW	4.91	1.862 um^2

The reduced process sensitivity for the NAND3 cell allows it to be a good substitute for the NAND2 gate, if delay variability is a high concern. To illustrate this concept, the circuit shown in Figure 7.9a is characterized under different focus and exposure conditions. It is composed of an inverter, followed by a NAND2 gate and a NOR2 gate. To reduce delay sensitivity of the overall timing path to focus and exposure variations, the NAND2 gate is replaced with a NAND3 gate, and the new circuit is illustrated in Figure 7.9b. This new circuit functions identically if the additional input of the NAND3 gate is tied to VDD. This new circuit is also characterized under different focus and exposure conditions, and a comparison of the two circuits is shown in Table 7.3.

This example illustrates an important point. By having delay variability models and delay sensitivity tables in standard cell library datasets, circuit level tradeoffs can be quickly and efficiently assessed. All the entries in Table 7.3 can be estimated in less than a second, as most of the entries are derived from table lookup and summation. In this scenario, the new circuit reduces path delay variability at the expense of higher power consumption and area. It is left up to the circuit designer to assess whether these tradeoffs are acceptable in the context of the entire design.

Finally, it is important to note that this is one of many possible improvements to this circuit, and the new circuit is by no means guaranteed to be the most optimal one. Other possible improvements include increasing drive strengths and reordering the logic structure. With appropriate enhancements and automation in physical implementation tools, these tradeoffs can be automatically calculated instead of the manual analysis that was used to create Table 7.3.

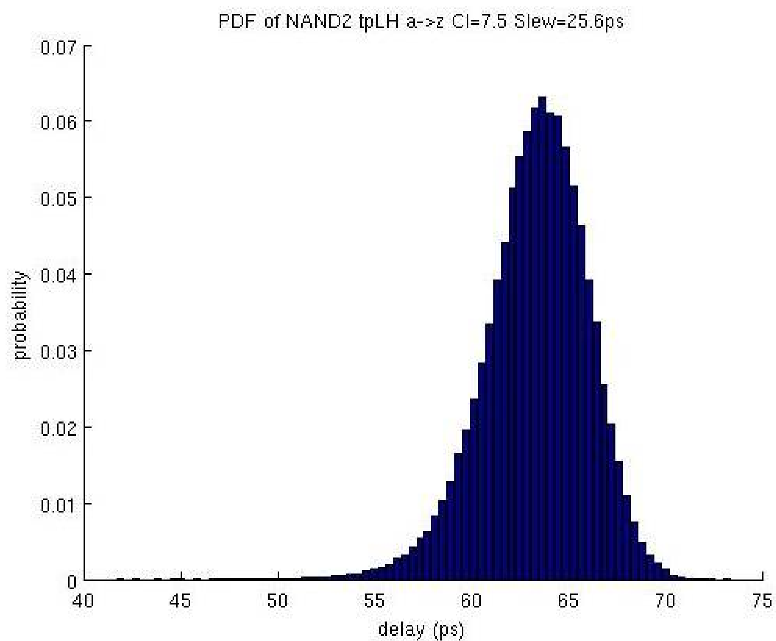


Figure 7.10: NAND2 Probability Distribution Function

7.5 Statistical Circuit Analysis

Conventional path level circuit analysis incorporates static timing analysis methods, which sum up absolute delays of each logic stage to obtain the overall path level delay. Another form of analysis which is being adopted is statistical timing analysis, which propagates probability distribution delay functions through each stage of a circuit path. Thus a probability distribution function is derived for the overall delay path, and a one sided confidence interval is utilized to determine if the simulated circuit performance meets desired specifications. In this section, we explore how the Standard Cell Variability Characterization framework and variability aware compact models can be applied to statistical circuit analysis techniques.

7.5.1 Statistical Timing Analysis Focus Exposure Models

The variability aware compact timing models developed in previous chapters are used to derive probability distribution functions (PDF) for use in statistical timing analysis. Monte Carlo methods are used to sample lithography focus and exposure process parameters, assumed to have normal distributions, to derive a PDF of the output delay distribution. Figure 7.10 shows the PDF corresponding to the NAND2 cell timing shown in Figure 5.6. The output distribution is skewed left, with a longer tail of slow delays. In the context of path level circuit analysis, the long tail highlights that operating at specific focus and exposure points may drastically speed up circuits, which may be problematic for circuit paths marginally meeting hold time specifications.

7.5.2 Systematic versus Random Variations

Process variations can be segmented into two categories: systematic and random variations. Systematic variations, like lithography focus and exposure variations, are deterministic in nature and can be modeled if their effects are characterized properly. In contrast, random variations cannot be accurately predicted for a specific instance because they are not deterministic. One common mechanism for random variations is random dopant fluctuation. Due to the nature of ion implantation to dope the channel, the number of dopant atoms fluctuates, inducing a change in threshold voltage. The effect is well characterized and follows Pelgrom's model, shown in Equation 7.1. Pelgrom's Model states that the standard deviation in threshold voltage scales inversely to the square root of the transistor gate area $W \times L$ [32]. Measured data indicates that the Pelgrom's coefficient, A_p, for a commercial 45nm technology is 2mV/um [13]. This coefficient is used in later sections for Monte Carlo simulations of cell performance.

$$\sigma_{V_T} = \frac{A_p}{\sqrt{W \times L}} \tag{7.1}$$

7.5.3 Analysis of Random Variability using Geometrical Biasing

Variability aware compact models account for systematic process variations. When performing statistical circuit analysis, it is important to understand the interactions between random variations and systematic variations. It is unclear how the cell level impact from random V_T variations is affected by lithography focus exposure conditions. To get a rough estimate of this impact, SPICE circuit simulations of the NAND2 cell shown in Figure 5.5 are performed. This cell is simulated with Monte Carlo methods that assign random threshold voltages for each transistor based on Pelgrom's model. Ten thousand cell level simulations are run, each with random threshold voltage variations assigned to each of the four transistors in the cell. The delay mean and standard deviation is plotted in Figure 7.11. The delay mean varies from 62ps to 118ps, and the standard deviation varies from 2.8 to 6.3 ps. These results show that the standard deviation of delay is a function of the geometrical dimensions of the transistor.

7.5.4 Analysis of Random Variability using Standard Cell Variability Characterization (SCVC)

Similarly, the cell level impact of random variability is studied using the SCVC framework. As in the previous section with geometrical biasing, Monte Carlo methods are used to assign random threshold voltages for each transistor based on Pelgrom's model. Three hundred samples are taken at each focus exposure process condition. Figures 7.12a and 7.12b show the mean and standard deviation of delay across the focus exposure window. As expected, the mean exhibits Bossung like behavior. In contrast, the standard deviation data is irregular because for the same number of samples, the estimate of the standard deviation is much noisier than the estimate of the mean. If the number of samples were increased, the confidence interval bounds on the standard deviation would decrease and the data would smoothen out to a Bossung like curve of Figure 7.12a. However, with three hundred samples, the characterization

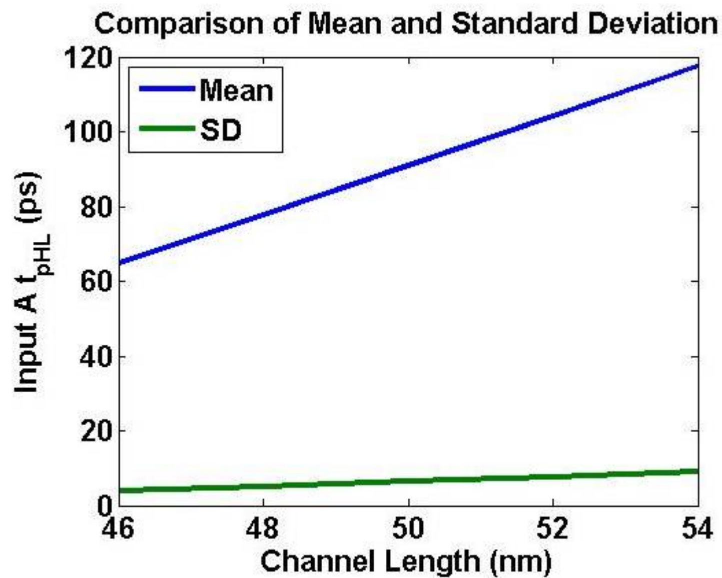


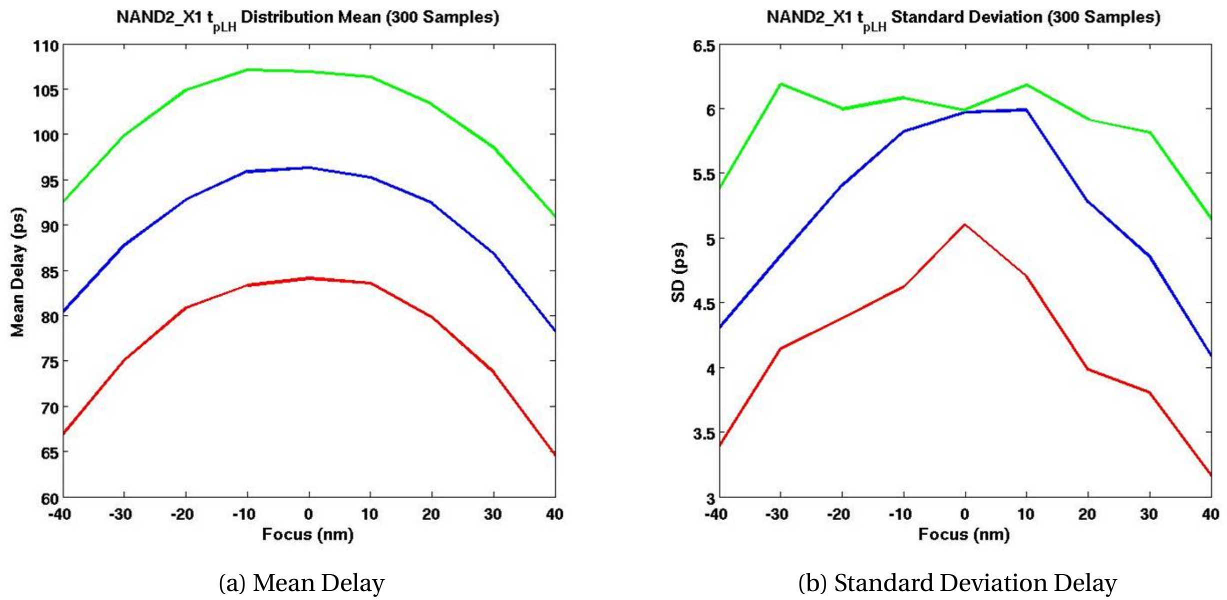
Figure 7.11: Mean and Standard Deviation of NAND2 Delay (Geometrical Biasing) with 10,000 Monte Carlo V_T simulations

consumes 150GB of data and nearly 300 CPU hours, and it is unrealistic to increase the number of samples. This extensive datasize and characterization time indicates that the geometrical biasing is a more efficient method to understand how cell level statistical delay distributions are affected by the process point.

7.6 Summary

The studies performed in this chapter illustrate the benefits of variability aware compact models obtained through the Standard Cell Variability Characterization framework. The abstraction of process variations from the post-layout level to cell level opens up an entire new realm of circuit analysis and optimization. Path level circuit analysis shows that the process dependent performance of a complex ring oscillator circuit with dynamically changing voltages and capacitances can be estimated to an accuracy of 1%. Similarly, the performance of a three stage logic circuit can be estimated to an accuracy of 0.7%, with a speedup of over 50,000. This accuracy and speedup tradeoff aligns with the goal of incorporating variability analysis in physical design.

With these compact models and slight modifications to existing physical implementation tools, electrical cell variability can used as another metric that is available to circuit designers and physical implementation tools. One such case is explored through sensitivity driven circuit optimization, where cell swapping is used to reduce the overall delay variability along a circuit path. Based on fast table lookup from the standard cell library dataset, design metrics such as circuit timing, power, area, and delay variability can be assessed in well under a second. This enables consideration of alternative circuit structures that meet design specifications while optimizing for the correct balance of all design metrics, including delay variability.



(a) Mean Delay

(b) Standard Deviation Delay

Figure 7.12: NAND2 Delay Results (SCVC) with 300 Monte Carlo V_T simulations

The variability aware compact models provide circuit level analysis of systematic process variations. However, a complete variability aware analysis must jointly account for both systematic and random variations. Monte Carlo sampling of the Bossung shaped timing response to systematic focus exposure variations results in a skewed delay distribution that increases the likelihood of hold time race violations. Further Monte Carlo investigations into random threshold voltage variations show that the output delay distribution is dependent on the lithography focus and exposure conditions, with a 3.6 ps variation in standard deviation across the focus exposure process window. The extreme computational and datasize cost of combining the SCVC framework with Monte Carlo threshold voltage sampling suggests that using selected cases of specific gate length biases and weighting them by their probability of occurrence is a better method to explore the complex process dependent effects of random variation.

Chapter 8

Conclusions

8.1 Dissertation Summary

The complexity of semiconductor development continues to increase with technology scaling. Challenges for every aspect of semiconductor development, including design and manufacturing, arise at smaller technology nodes. With an ever increasing impact of process variability on circuit performance, one important challenge is to ensure that integrated circuits function with the variability inherent in semiconductor fabrication.

This dissertation addresses this challenge by detailing existing solutions from both design and manufacturing perspectives, and identifying high-impact opportunities to achieve design robustness. Existing process and circuit analysis techniques are combined in a unique fashion to develop flexible software frameworks that transcend the traditional boundary between design and manufacturing. These frameworks are used to provide detailed studies of circuit performance in the presence of lithography variability, and the results of these studies provide physics based insight into the impact of significant sources of lithography variation such as focus and exposure. The trends associated with these results lead to the development of variability aware compact models that abstract lithography variability from the wafer level to a circuit level. Cell level compact models permit path level circuit performance to be estimated with high accuracy and very little overhead to standard analysis techniques. Both cell level compact models and variability aware path level circuit analysis techniques can be used to drive circuit optimization that balances all design metrics while additionally including the impact of lithography variability.

The first study of lithography variability presented in this dissertation involved analysis on metal interconnect layers using the Interconnect Variability Characterization (IVC) framework which maps lithography induced geometrical variations to electrical delay variations. The IVC framework is used to study one dimensional repeater circuits under 90nm single and 32nm double patterning lithography technologies in the presence of focus, exposure, and overlay variations. Studies indicate that single patterning and double patterning layouts generally exhibit small variations in delay (between 1-3%) due to self-compensating RC effects associated with dense layouts and overlay errors for layouts without self-compensating RC effects. The delay response of each double patterned interconnect structure is fit with a second order poly-

nomial model with focus, exposure, and misalignment parameters with 12 coefficients and residuals of less than 0.1ps. The IVC framework is also applied to investigate cascaded one dimensional interconnect structures that emulate the more advanced nature of interconnect found in designs. Simulation results for these cascaded interconnect structures show that the variations on each segment average out to reduce the overall delay variation.

Studies of lithography variability at the cell level begin with an approximate method that upsizes or downsizes transistor dimensions to simulate linewidth variations at different length scales. This method of geometrical biasing is applied to standard cells in the Nangate 45nm Open Cell Library to explore the linewidth dependent effects of cell level performance and create delay sensitivity tables which are easily incorporated into existing timing libraries. These delay sensitivity tables can then be utilized in a path level circuit analysis framework to analyze the impact of linewidth variability across different length scales.

To investigate advanced lithography variability which results in non-uniform transistor geometries, the Standard Cell Variability Characterization (SCVC) framework is developed. This framework advances existing layout-level lithography aware circuit analysis by extending it to cell-level applications, utilizing a physically accurate approach that integrates rigorous process simulation, compact transistor models, and circuit simulation to characterize electrical cell behavior. The timing response for a simple combinational cell illustrates Bossung shaped behavior to focus and exposure variations, allowing this response to be captured in a variability aware compact model, based on Bossung fitting equations, that captures simulation results to an accuracy of 0.3%. The SCVC framework is also applied to investigate advanced process effects including misalignment and layout proximity. The SCVC framework is also applied to advanced studies of multi-stage combinational and sequential logic cells, and the results confirm that the variability aware compact model can be applied to advanced cells that are typically found in standard cell libraries.

The abstraction of process variability from the layout level to the cell level opens up an entire new realm of circuit analysis and optimization and provides a foundation for path level variability analysis without the computationally expensive costs associated with process or circuit simulation. The SCVC framework is applied to demonstrate the advantages of path level circuit analysis using variability aware compact models. Path level circuit analysis shows that the process dependent performance of three stage logic circuit can be estimated to an accuracy of 0.7%, with a speedup of over 50,000. When applied to a complex 11-stage ring oscillator that typically requires transistor level circuit simulation, path level circuit analysis is able to estimate the through-focus and through-exposure performance of an 11 stage ring oscillator performance to an accuracy of 1% in well under a second.

The variability aware compact models are compatible with existing design methodologies because they can be included in standard cell characterization libraries that are utilized through all stages of physical design. With slight modifications to existing physical implementation tools, electrical cell variability can be used as another metric for circuit optimization and trade-off analysis. This is demonstrated by applying cell swapping on a logic circuit to reduce the overall delay variability along a circuit path. By including these variability aware compact models in characterization libraries, design metrics such as circuit timing, power, area, and delay variability can be quickly assessed without extensive simulation runtimes to optimize for the

correct balance of all design metrics, including delay variability.

Lithography variations are considered to be systematic variations that can be deterministically modeled. However, lithography variations at the cell level affect the transistor dimensions, which in turn affect the random threshold voltage fluctuations associated with random doping fluctuations. Monte Carlo investigations into the these random threshold voltage variations using 45nm technology show that the output delay distribution is dependent on the lithography focus and exposure conditions, with a 3.6 picosecond delay variation in standard deviation across the focus exposure process window, indicating that the electrical impact of random variations has a dependency on systematic lithography variations that affect device dimensions.

8.2 Future Work

The software frameworks presented in this dissertation have been utilized to study the circuit level electrical impact of lithography process variability. The studies in this dissertation are based on process design kits and assumptions developed at the university level, which provide a just but not entirely accurate representation of advanced process technologies. Lithography variability is only one of the major causes of circuit variability. Other advanced process effects that impact circuit performance, such as chemical mechanical polishing and transistor device strain, are not captured in these studies. However, many techniques associated with lithography variability analysis frameworks can be applied to study these advanced process non-idealities. Extension of the frameworks developed in this dissertation to consider these other effects will open up opportunities to create a comprehensive model that captures not only lithography variability but other process variability sources as well.

The IVC framework plays an important role in studying homogenous one-dimensional interconnect topologies, but its utility is limited for complex interconnect scenarios typically found in conventional semiconductor designs. The number of permutations of layers and layout topologies makes it impractical to utilize this framework to develop timing variability models that can be applied to a wide range of circuits found in a design. Instead, this framework can be utilized to study the circuit level variability associated with different interconnect layout topologies. From such a study, preferred interconnect routing scenarios can be identified and potentially incorporated into the cost function of an interconnect routing tool to enhance variability awareness during the routing step of a design.

The SCVC framework facilitates the creation of cell level compact models that enable lithography variability aware path level circuit analysis. Characterization time is still very lengthy, with 12 CPU hours required for variability aware characterization of a NAND2 combinational logic cell. Since the priority of cell level compact modeling was to obtain accurate results, very little was done to reduce the overall characterization runtime, though many possibilities are open for further exploration. Some potential optimizations include reducing the number of focus and exposure process simulation points and reducing the number of entries in the current based lookup table that represents transistor behavior derived from contour analysis. It is also worth investigating if the current based lookup table can be replaced with an alternative, more efficient representation of transistor behavior based on average transistor dimensions

measured during contour analysis. If so, this will reduce the file size associated with storing the current based lookup table and dramatically reduce runtime through a reduction in the number of memory accesses.

The abstraction of lithography variability from the layout level to the cell level provides a very powerful tool for circuit level analysis. While much of the focus of this dissertation centered on timing performance of circuit paths to create a more robust design, there are many other opportunities for analysis that have not been addressed. One such opportunity is to combine variability aware compact models with wafer characterization data of the lithography process to analyze the impact of lithography non-idealities at different length scales. These non-idealities might include systematic lens aberrations across the lithography slit, exposure variations between die, and defocus variations from tilt. By combining a process footprint with design data, both the designer and process technologist can quickly assess and quantify the impact of these process variations without the rigors of detailed analysis that previously made such analysis intractable.

8.3 Final Words

Looking ahead to the future, it is clear that the rapid pace of technology scaling will continue to increase the complexity of semiconductor development. As feature sizes continue to decrease, the impact of process non-idealities will become more prominent, and effort must be expended to model and control the impact of process variability. Solutions to address these challenges must integrate expertise from design methodologies as well as process technologies.

For intricate designs with hundreds of thousands of cells, standard variability aware analysis techniques cannot be applied due the rigors of process simulation and circuit analysis at the transistor level. Instead, these process effects must be abstracted to a higher level that can be easily incorporated with design methodologies and used in creating design level circuit tradeoffs. The flexible frameworks presented in this dissertation do exactly this by transforming layout level variability to cell level compact models that enable path level circuit variability analysis.

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