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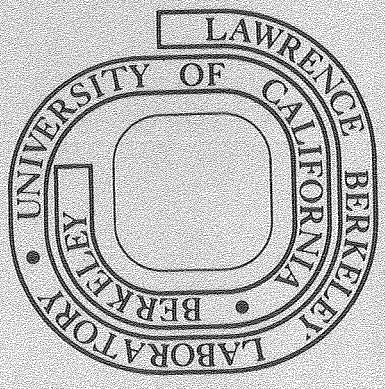

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A WIDE-BAND MEASURING SYSTEM FOR STUDYING CHARGE-COUPLED DEVICE CHARACTERISTICS

Branko Leskovar and C. C. Lo*

Abstract

A wide-band four-channel measuring system has been developed for studying charge-coupled devices and optimizing their characteristics. The system incorporates a high-to-low frequency processor capable of handling the 100-300 MHz high frequency clock CCD driver and generating the 0.5-10 MHz readout frequency, a microwave component based on a four-phase signal generator, a four-channel phase-matched RF power amplifier and a wide-band CCD test fixture. The phase error between the four low frequency channels is less than ± 5 degrees through the 1 to 10 MHz band, and less than ± 10 degrees in the 100 to 250 MHz range.

The measuring system is capable of delivering an output voltage of 10 V peak-to-peak up to frequencies of 280 MHz and 170 MHz into a capacitative load of 25 pF and 100 pF, respectively.

Introduction

The investigation and optimization of the characteristics of high-speed charge-coupled devices is becoming increasingly important in a multitude of applications, such as: signal processing systems, transient analog signal recording, electro-optical imaging, and radar systems.[1-4] Theoretical calculations,[5] and experiments using a uniphase clock[6] have projected operating data rates of the order of 1 GHz for peristaltic charge-coupled devices with charge transfer inefficiencies of about 10^{-4}. However, these operating speeds have not been experimentally achieved because of the present frequency limitations of input, output, and driving circuitry.

In most applications, charge-coupled devices require a complex array of peripheral circuitry to support their operation, such as: input gates, multiple phase clock signal generators, output gates, propagation gate drivers, reset gates, photogates and various d.c. biasing circuits. For example, for a 128 cell CCD analog shift register, the supporting circuitry contains an input sample and hold propagation gate driver, a multiphase phase generator, amplifiers and output strobe circuits. Such a shift register is used for both delaying and expanding the time base of quantized analog data with a 62.5 Msample/second input rate and a 100 Ksample/second output rate. The four-phase clock signals required can be generated by using a pair of D-type Flip Flops connected as shown in Fig. 1. When a clock signal with a pulse rate four times the shift rate is applied to the generator, the four outputs will produce the signals shown in Fig. 2. Each pulse is shifted 1/4 a cycle in phase. The logic family used for such an operation has to be consistent with frequency of operation. For example, for a shift rate of 62.5 MHz an input clock frequency of 250 MHz is required. The Emitter Coupled Logic (ECL) is the only logic family capable of operating at these frequencies. Some new D-Flip-Flop devices can be made to operate at frequencies up to 700 MHz, but with a very distorted waveshape of the output signals. With this method of four-phase generation, the clock frequency can vary, preserving at the same time the quadrature relationship between the generator output signals.

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The CCD development programs at the Lawrence Livermore Laboratory[7] have created a need for a versatile four-phase CCD testing instrument being capable of operating at clock frequencies of from 100 MHz to 250 MHz.[8] A new, special measuring system has been designed to meet the requirements for testing CCD's to be used for use in analog signal recorders for sampling and time expansion of transient signals. The testing instrument should have the capability of generating a high driver frequency and a lower CCD readout frequency. It should supply, at appropriate levels, the required signals for the input gate, the input diffusion clock, the input diffusion d.c. bias, and the reset gate. The low CCD readout frequency should vary from 500 kHz to 10 MHz. All signals necessary to operate CCD should have waveshapes that preserve phase integrity over a wide range of frequencies. Both the high and low readout frequency clock generators should supply four channel signals which are in quadrature. Furthermore, the switching from high-to-low frequency and from low-to-high frequency should be very smooth, that is without excessive ringing. This is especially important during the high-to-low clock frequency switch over period. Hence, electronic switches with very short on and off time should be used to insure fast switching actions and they must be well matched over a wide frequency range to insure smooth transitions.

Description of the Wide-Band Charge-Coupled Device Measuring System

A block diagram of the wide-band measuring system for charge-coupled devices is shown in Fig. 3. The system consists of the following components: a high-to-low frequency processor, a high and low frequency switch with input two-channel wide-band preamplifier, a two channel buffer wide-band amplifier, a four phase generator, a four channel radio frequency to ECL level translator, a four channel output amplifier unit, a charge-coupled device jig and a four channel d.c. power supply.

High-to-Low Frequency Processor and Two Channel Wide-Band Amplifier

The system requires for its operation an external high frequency clock signal generator capable of operating in a frequency region of 100 to 250 MHz and delivering an output of at least 1 V rms into a 50 ohm load. The first stage of the system is a high-to-low frequency processor capable of operating at frequencies up to 300 MHz. A thumb-wheel switch selects the following high-to-low frequency ratio: 20, 40, 60, 100...up to 500. Therefore, with a 200 MHz clock signal and a division ratio of 100, the low readout frequency clock signal is 2.0 MHz. The output from the frequency processor unit consists of a high frequency clock signal, which is at the same frequency as the input signal and a low readout CCD frequency clock signal whose frequency is determined by division ratio selected by the switch. Both the high frequency and low frequency signals are gated on and off by a dual radio-frequency high speed switch. The gating conditions depend entirely on the external logic signal which in turn is governed by the requirements of the CCDs under test. Only one channel is on at any given time. The output signals from the switch are amplified

by wide-band amplifiers with adjustable gain controls to approximately 0.25 W output power level. After amplifications, the high and low frequency clock signals are processed by the four-phase signal generator which provides a pair of four high and low frequency output signals which are 90 degrees out of phase with respect to each other.

Four-Phase Clock Signal Generator

Concerning the four-phase signal generation, the ECL logic family was considered initially for a possible application. Unfortunately, at frequencies above 80 MHz, output signals do not have a rectangular waveshape, but instead is a distorted trapezoidal waveshape which approaches a distorted sinusoidal wave as the frequency increases. Therefore, a completely new approach for the generation of four-phase signals over a wide range of frequency had to be taken using microwave technology components. Hybrid junctions and quadrature hybrids were specifically evaluated for this particular application.

A hybrid junction is a four-port network capable of splitting input signals into equal amplitude, isolated output which are either in phase or 180° out of phase. The network is recognized in the microwave technology under various names, such as magic tee, ring hybrids and hybrid tees. Their low frequency counterpart is the hybrid transformer. When a signal is applied to the H, or symmetrical port, it will split equally and in-phase between the collinear output ports (1 and 2), Fig. 4. When a signal is applied to the E, or antisymmetric port, it will split equally, but out-of-phase, between the ports 1 and 2. This in-phase and out-of-phase output relationship results in isolation between the E and H ports, the extent of which is an important measure of hybrid balance. The simultaneous application of signals of both H and E ports results in their vector addition at one collinear port and vector subtraction at the other. Typically, a 50-ohm hybrid junction designed for frequency range from 5 MHz to 1000 MHz has an insertion loss of approximately 4 dB, an isolation of 25 dB, a maximum value of the phase balance of 3 degrees, and the amplitude balance of 0.5 dB.

A quadrature hybrid is a four-port 3 dB coupler capable of splitting an input signal into isolated quadrature phased outputs. This type of device is commonly known in microwave technology field as a 3 dB stripline coupler or a "short slot" waveguide coupler. The device can also be made from lumped components permitting application to low frequencies. If a signal is applied to Port 1, as shown in Fig. 5, it splits equally between output Ports 2 and 3 with a 90° phase difference. If Ports 2 and 3 are properly terminated, the signal applied to Port 1 is absorbed in the loads. Therefore, Port 4 can be isolated and receive very little power from the incident signal. The extent of this isolation is an important measure of the coupler performance. Typically, a 50-ohm quadrature hybrid, designed for frequency range from 50 MHz to 500 MHz, has an insertion loss of 1 dB, isolation of 20 dB, an amplitude balance of 0.5 dB, and a maximum deviation from quadrature of 3 degrees. Generally, for low level signal application the device can handle input power levels of 1 W. The hybrid junction and quadrature hybrid specifications given above are typical of the available devices manufactured in this country as well as in Europe.

The four-phase clock signal generator was developed combining a number of hybrid junctions and quadrature hybrids. Because of the frequency bandwidth limitations of these devices, the four-phase generator was designed with two channels in an appropriate configuration. The channel for very high frequency signal generation uses components capable of operating in the frequency range of 50 MHz to 500 MHz. The channel for low CCD readout frequency generation uses components with operating characteristics from 2 MHz to 32 MHz. A combination of five hybrid junctions, used as broadband out-of-phase and in-phase power dividers, and two broadband 90° quadrature hybrids generates pairs of four-phase clock signals in the 50-500 MHz frequency range. A similar configuration generates pairs of the four-phase clock signals in the 2-32 MHz range. Finally, combining the outputs from the high-frequency and the low-frequency channels by means of eight in-phase linear power combiners, as shown in Fig. 6, four-phase clock signals are obtained in pairs over a frequency range from 2 to 500 MHz. As a self-contained unit, the four-phase generator is capable of operating at frequencies up to 1000 MHz.

Four Channel Wide-Band Output Amplifier and Radio Frequency to ECL Level Translator

One set of four-phase high and low frequency clock signals is further amplified by four separate wide-band RF power amplifiers having output power capabilities of 3 W each. Each amplifier channel has at its input a 1 dB step and a 0.1 dB step, wide-band, low-phase error attenuator. These attenuators have phase errors of less than ±3 degrees in the frequency band 1-250 MHz. The amplifiers used were phase matched so that the phase difference between any of the four amplifiers is less than ± 5 degrees in the 1-250 MHz frequency band. The nominal gain of each amplifier is 37 dB with a gain flatness of ± 1 dB over the same frequency range.

The second set of four-phase high and low frequency clock signals is applied to a four channel radio frequency to ECL level translator. The translator module supplies ECL level signals to other logic devices required for the CCD operation.

Charge-Coupled Device Testing Fixture

The output signals from the four-channel, wide-band, amplifier are applied to the test fixture where the CCD will be tested. The final driving signals are supplied to the CCD through four, low Q-factor, wide-band transformer circuits. A schematic diagram of the transformer driving stage is shown in Fig. 7. The primary-to-secondary turns ratio of each transformer is 4:1. The nominal 50 ohm output impedance of the output amplifier is transformed to approximately 3 ohm for the source impedance. With this impedance the charging and discharging time constant is 120 ps for a 40 pF capacitive load. The transformers are designed in such a way that their stray and leakage inductances do not resonate with the load capacitance at any frequency range of interest. Also, the transformer core material was selected to be lossy at high frequencies to make the Q-factor of the circuit low. At very high frequencies, additional loss is introduced by the eddy current loss of the enclosure walls. A small high-Q capacitor is connected in parallel across the primary of each transformer for final phase adjustment and tracking between channels. Each driving stage is enclosed in a separate chamber, which is properly ventilated. The CCD under test is mounted on a small printed circuit board which is situated between the two main transformer circuit enclosures, as shown in Fig. 8.

Measuring System Characteristics

The phase difference between the four low frequency channels (90 degrees out of phase with respect to each other) as a function of frequency is shown in Fig. 9. The measurement was made with a 10 V peak-to-peak signal across a 35 pF load. The phase difference was measured directly at the capacitive load with the 0 degree channel as a reference channel. The phase difference between the four high frequency channels as a function of frequency is shown in Fig. 10. The phase difference of high frequency channels is within ± 10 degrees through the 100-250 MHz frequency band. The available output voltage across a capacitive load, in volts peak-to-peak, as a function for frequency for the high frequency channels is shown in Fig. 11. With a 100 pF load, a voltage of 10 V peak-to-peak can be obtained up to 170 MHz. For a 25 pF load, voltage of 10 V, peak-to-peak can be obtained up to 280 MHz. The upper frequency limits are determined by the power available from each driver for the various capacitive loads. A very important characteristic of the tester is its performance when switching from high-to-low frequency and from low-to-high frequency. The waveform of the high-to-low frequency switching is shown in Fig. 12.

Conclusions

Design and characteristics of a wide-band four channel measuring system for studying and optimizing charge-coupled devices have been presented and discussed. A new high-to-low frequency processor, four phase clock signal generator and charge-coupled device testing fixture had to be developed to meet flexible requirements of CCD testing. The system was constructed in modular form and can be easily modified by increasing the power of the output amplifiers and changing the output transformer stages to accommodate larger capacitive loads. Furthermore, the size and cost of the system can be significantly reduced using high Q-factor output circuitry once the optimum operating parameters for the CCD's have been chosen.

Acknowledgments

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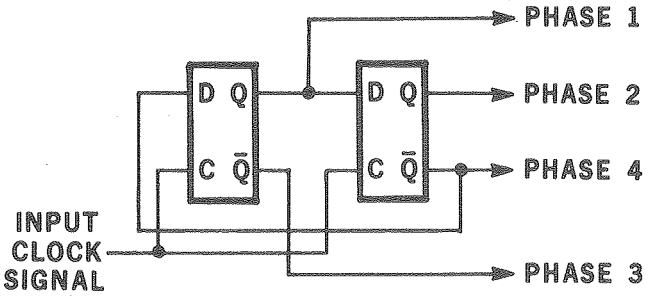

Fig. 1 Four-phase generator logic diagram.

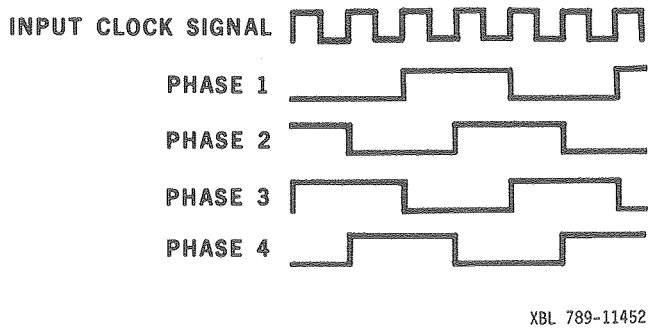

Fig. 2 Four-phase generator output timing diagram.

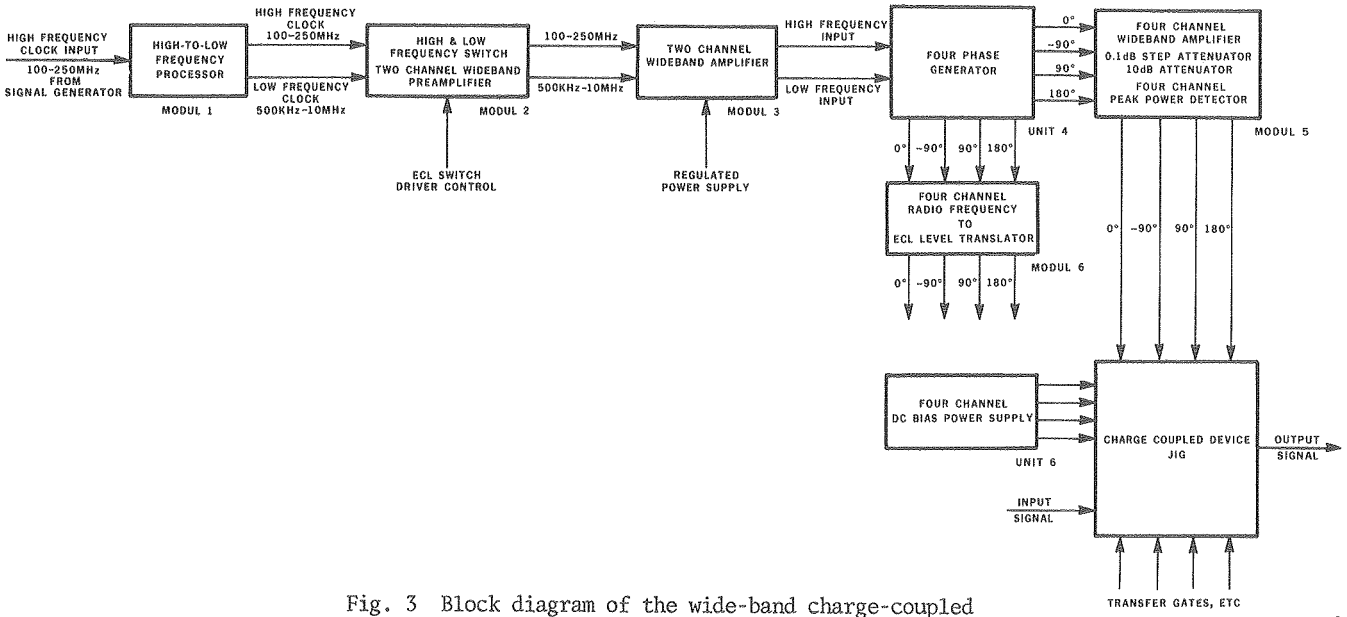

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Fig. 3 Block diagram of the wide-band charge-coupled device measuring system.

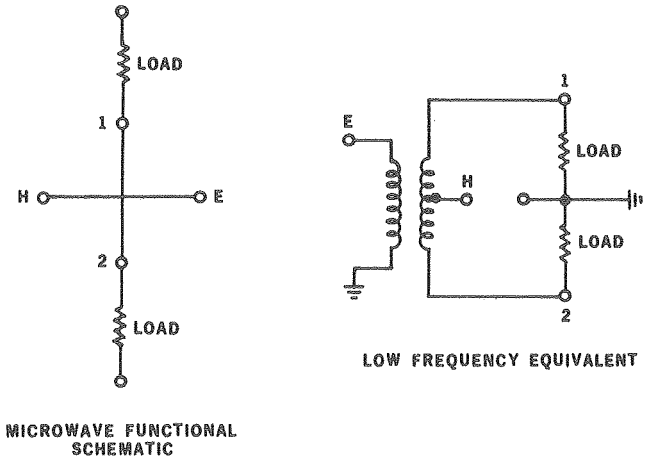

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Fig. 4 Functional schematic of a hybrid junction and its low-frequency equivalent.

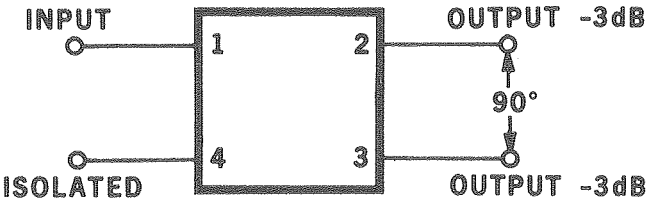

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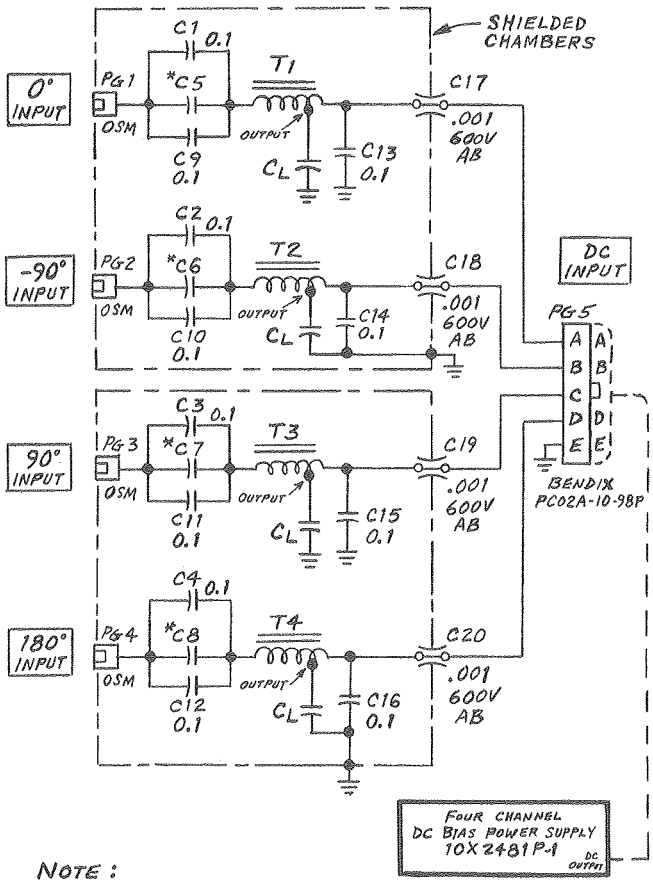
Fig. 5 Functional schematic of a quadrature hybrid.



NOTE:
1. CAPACITORS 0.1μF 50V CK05 CERAMIC.
*2. C5-C8 ARE 470pF CHIP CAPACITORS.
3. CAPACITIVE LOAD C_L

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Fig. 7 Schematic diagram of the transformer driving stage.

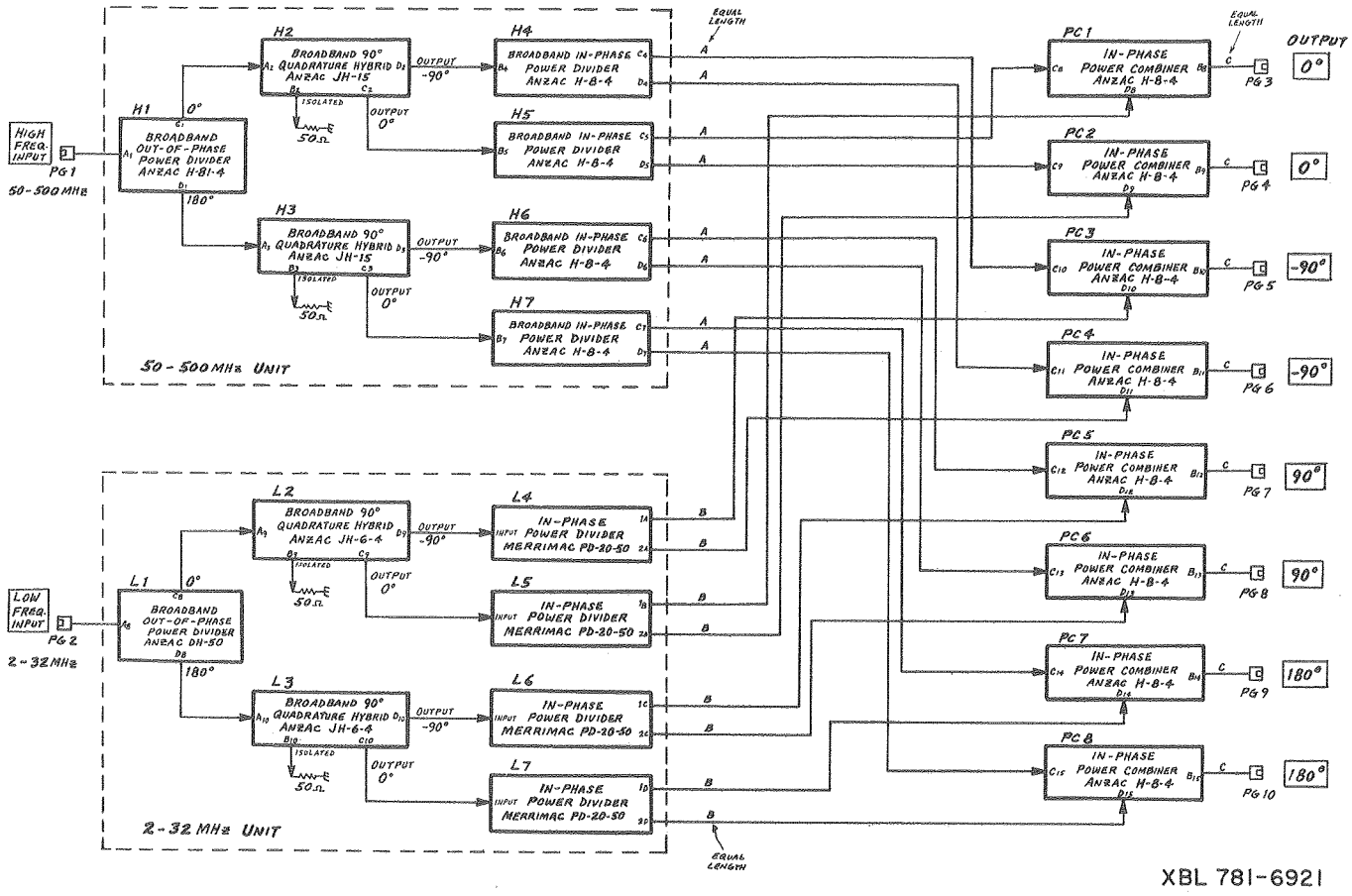

Fig. 6 Block diagram of the four-phase clock signal generator.

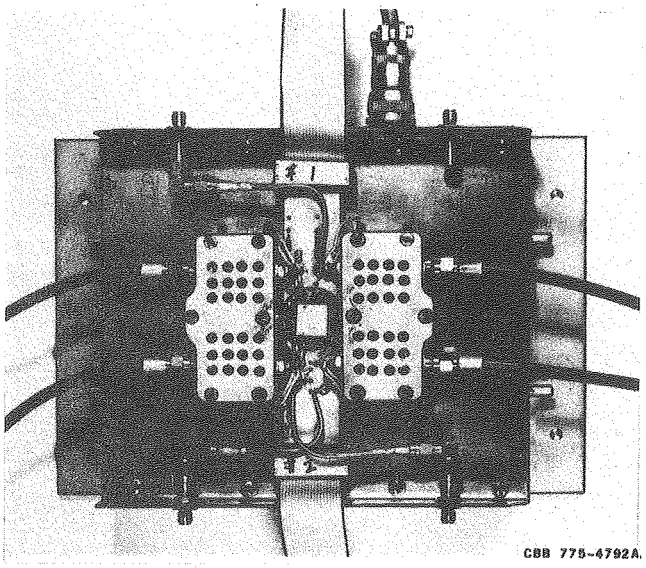

Fig. 8 Top view of the testing fixture.

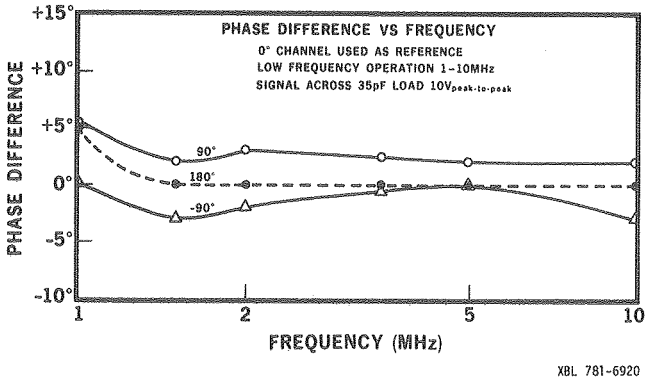

Fig. 9 The phase difference between the four low-frequency channels.

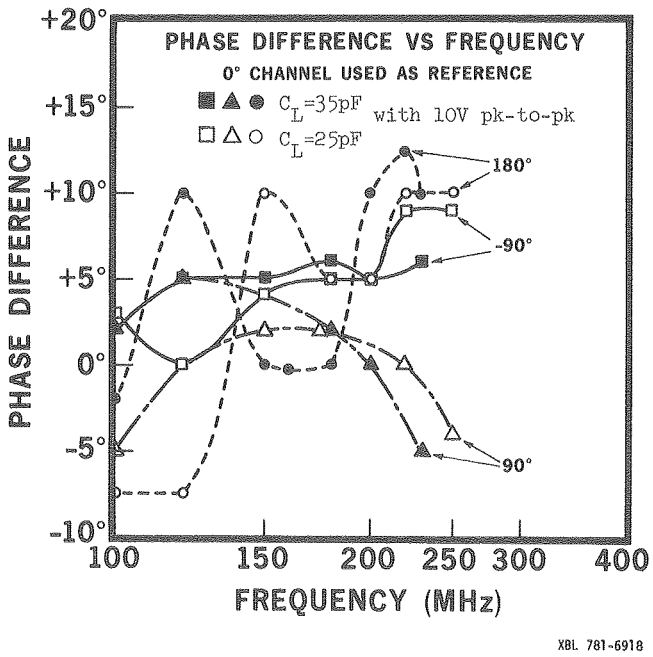

Fig. 10 The phase difference between the four high-frequency channels.

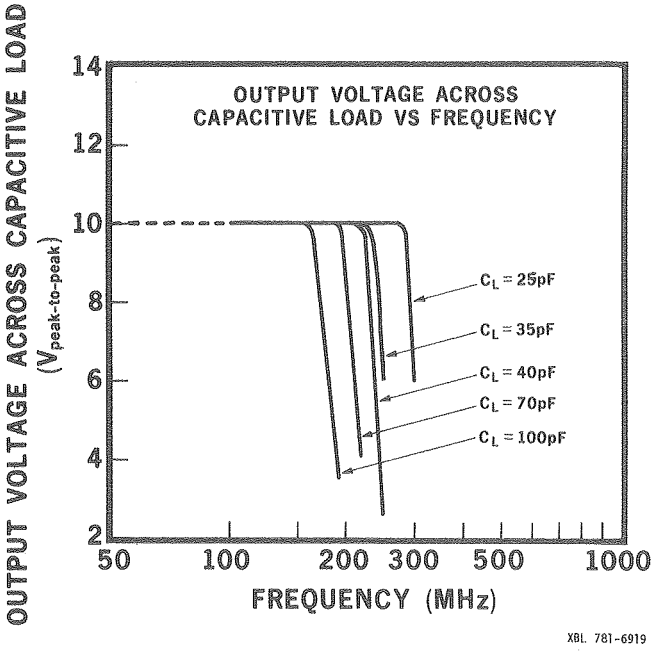

Fig. 11 Available output voltage as a function of frequency for the high-frequency channels.

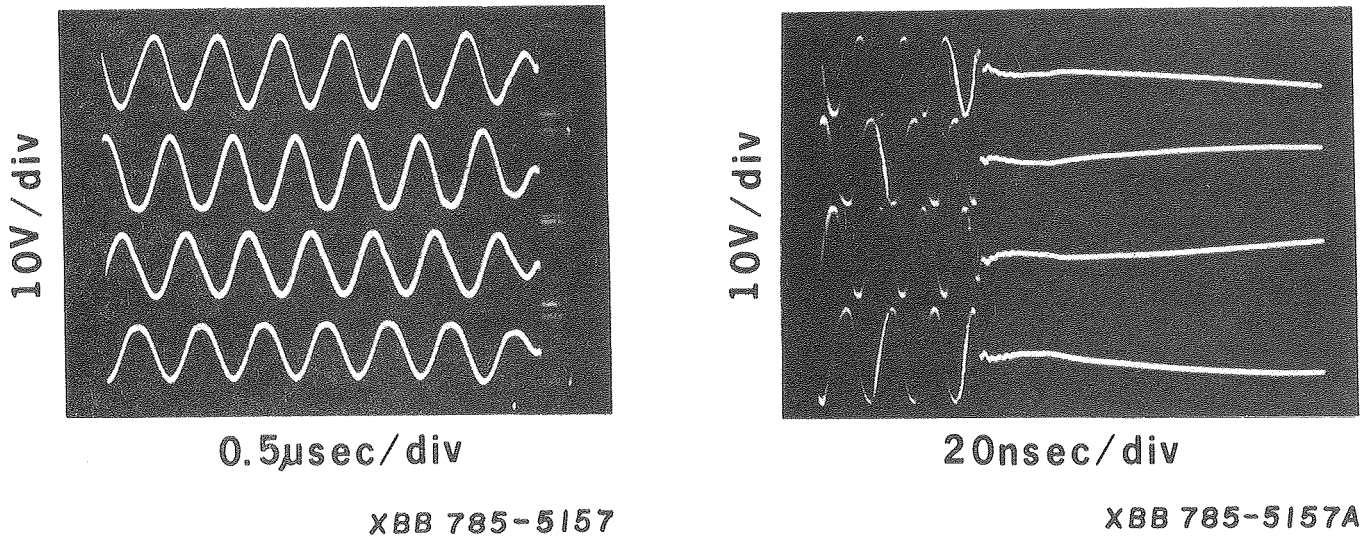

Fig. 12 The waveform of the high-to-low frequency clock switching.