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UNIVERSITY OF CALIFORNIA, SAN DIEGO

**High Efficiency Wideband Envelope Tracking Power Amplifier for
Next-Generation Wireless Communications**

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronics Circuits and Systems)

by

Myoungbo Kwak

Committee in charge:

Professor Lawrence E. Larson, Chair
Professor Peter M. Asbeck
Professor James F. Buckwalter
Professor Chung-Kuan Cheng
Professor William G. Griswold

2011

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The dissertation of Myoungbo Kwak is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

Chair

University of California, San Diego

2011

DEDICATION

*To my grandparents, parents, brother, sister,
and my wife Youngsun.*

EPIGRAPH

" Logic will get you from A to B. Imagination will take you everywhere."

— Albert Einstein (1879-1955)

TABLE OF CONTENTS

| | | |
|--|--|------|
| Signature Page | | iii |
| Dedication | | iv |
| Epigraph | | v |
| Table of Contents | | vi |
| List of Figures | | viii |
| List of Tables | | xii |
| Acknowledgements | | xiii |
| Vita | | xvii |
| Abstract of the Dissertation | | xix |
| Chapter 1 | Introduction | 1 |
| | 1.1 Modern Wireless Communications | 1 |
| | 1.2 Wireless Transceiver Systems and Power Amplifiers | 2 |
| | 1.3 Efficiency and Linearity Enhancement Techniques | 3 |
| | 1.3.1 Doherty Power Amplifier | 5 |
| | 1.3.2 LINC and Chireix Outphasing Power Amplifier | 7 |
| | 1.3.3 Envelope Elimination and Restoration (EER) and En- velope Tracking (ET) Power Amplifiers | 9 |
| | 1.3.4 Linearity Improvements with Pre-Distortion Tech- niques | 11 |
| | 1.4 Dissertation Objectives and Organization | 17 |
| Chapter 2 | Design of High Voltage Envelope Tracking Integrated Circuit for Micro-Base Station Power Amplifiers | 19 |
| | 2.1 Introduction | 19 |
| | 2.2 Envelope Tracking Amplifier Circuit Design and Implemen- tation | 21 |
| | 2.3 Measured Envelope Amplifier Results | 34 |
| | 2.4 Conclusion | 44 |
| | 2.5 Acknowledgment | 44 |

| | | |
|------------|---|-----|
| Chapter 3 | Wideband High Efficiency Envelope Tracking Power Amplifiers for Micro-Base Station Applications | 46 |
| | 3.1 Introduction | 46 |
| | 3.2 Envelope Tracking Amplifier System Design | 47 |
| | 3.2.1 High Voltage Envelope Amplifier Design Considerations | 49 |
| | 3.2.2 RF Power Amplifier Design Considerations | 52 |
| | 3.3 Measured Envelope Tracking Power Amplifier Results | 53 |
| | 3.4 Conclusion | 63 |
| | 3.5 Acknowledgment | 64 |
| Chapter 4 | High-Efficiency CMOS Envelope Amplifier with Direct Current Sensing for Handset RF Power Amplifiers | 65 |
| | 4.1 Introduction | 65 |
| | 4.2 High Efficiency Envelope Tracking Power Amplifier Design | 68 |
| | 4.3 Envelope Tracking Amplifier Circuit Design and Implementation | 69 |
| | 4.4 Measured Envelope Tracking Power Amplifier Result | 80 |
| | 4.5 Conclusion | 98 |
| | 4.6 Acknowledgment | 98 |
| Chapter 5 | Conclusion | 100 |
| References | | 103 |

LIST OF FIGURES

| | | |
|--------------|--|----|
| Figure 1.1: | Heterodyne wireless handset transmitter section, showing a complete upconversion path from baseband [1]. | 3 |
| Figure 1.2: | Trade-off between efficiency and linearity [2]. | 5 |
| Figure 1.3: | (a) Simplified block diagram of a Doherty PA, (b) power properties [2]. | 6 |
| Figure 1.4: | (a) Simplified block diagram of a LINC PA, (b) amplitude combining [2]. NLPA : Nonlinear Power Amplifier. | 8 |
| Figure 1.5: | Simplified block diagram of: (a) an Envelope Elimination and Restoration (EER) PA, (b) an Envelope Tracking (ET) PA [1, 3]. | 10 |
| Figure 1.6: | Illustration of predistortion, cascading of NLPA (Nonlinear Power Amplifier) together with circuit providing inverse nonlinear characteristics ($NL^{-1}PA$) [2]. | 12 |
| Figure 1.7: | Simplified schematic of digital pre-distortion (DPD) based on look-up table(LUT). | 13 |
| Figure 1.8: | Measured: (a) AM-AM, (b) AM-PM performance before pre-distortion after memory-effect mitigation pre-distortion. | 14 |
| Figure 1.9: | Measured: (a) AM-AM, (b) AM-PM performance after memoryless pre-distortion. | 15 |
| Figure 1.10: | Measured: (a) AM-AM, (b) AM-PM performance after memory-effect mitigation pre-distortion. | 16 |
| Figure 2.1: | Block diagram of wireless transmitter with envelope tracking system for improved efficiency. | 20 |
| Figure 2.2: | Proposed monolithic envelope amplifier schematic. | 22 |
| Figure 2.3: | Simplified schematic of the linear stage. All the devices are 0.35- μ m DMOS, and the $ V_{GS} $ was limited to 3.3 V in all cases. | 23 |
| Figure 2.4: | Switch voltages and currents in a buck-converting switcher [4]. | 24 |
| Figure 2.5: | Simulation of the conduction loss in the switch-FETs, as a function of device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$ | 26 |
| Figure 2.6: | Simulation of the crossover loss in the switch-FETs, as a function of device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$ | 27 |
| Figure 2.7: | Simulation of the dynamic power dissipation at the output node in the switch-FETs, as a function of device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$ | 28 |

| | | |
|--------------|---|----|
| Figure 2.8: | Simulation of the total power loss in the switch-FETs, as a function of device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$ | 29 |
| Figure 2.9: | Simulation of the total power loss in the switch-FETs as a function of the P-channel LDMOS switch-FET width. The width of the N-channel LDMOS switch-FET was set to 40 mm. An optimum P-channel FET width of 80 mm was used for this design. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$ | 30 |
| Figure 2.10: | Simulation of the power loss in the driver, as a function of switch-FET device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$ | 32 |
| Figure 2.11: | CMOS comparator with controllable offset. | 33 |
| Figure 2.12: | Chip micrograph of the BCD envelope amplifier. The chip occupies 5.85 mm ² die area including the pads. | 35 |
| Figure 2.13: | Test fixture setup of an envelope amplifier IC with resistive loads. | 35 |
| Figure 2.14: | Measured envelope amplifier input, output voltage, and switcher stage output voltage. The envelope input signal is a 7.7dB PAR 4MHz WCDMA signal. The closed-loop gain is 20 dB with 15 V supply voltage. (200 ns/div) | 37 |
| Figure 2.15: | Measured baseband envelope amplifier output spectrum for a 4 MHz WCDMA signal. The noise is - 132.6 dBc/Hz at a 180 MHz offset. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$ | 38 |
| Figure 2.16: | Comparison of measured and simulated envelope amplifier efficiency as function of signal bandwidth and output power. Sine wave input, $V_{DD} = 15$ V and $R_{load} = 7.7$ to 30 Ω | 39 |
| Figure 2.17: | Comparison of measured and simulated comparator offset voltage versus input bias current. | 40 |
| Figure 2.18: | Measured comparator positive input, negative input, differential input voltages, and output voltage with offset voltage of 120 mV. Differential input voltage is a symmetric triangle wave with period 1 ms and varying between -1 and 1 V. (200 us/div) | 41 |
| Figure 2.19: | Measured envelope amplifier efficiency with a 7.7dB PAR 4MHz WCDMA signal and a 10 Ω resistive load, as a function of the comparator offset voltage. | 42 |
| Figure 3.1: | BCD6 process cross section thru the fourth-layer metal [5]. | 48 |
| Figure 3.2: | Conventional linear-assisted hybrid envelope amplifier for envelope tracking applications [6]. | 50 |
| Figure 3.3: | Proposed monolithic envelope amplifier with improved operation at high V_{DD} | 51 |

| | | |
|--------------|--|----|
| Figure 3.4: | Test fixture setup with envelope amplifier IC and RF power amplifier for the envelope tracking system. | 53 |
| Figure 3.5: | Measured results on GaN HFET power amplifier with WCDMA input at 2.14 GHz (a) instantaneous drain efficiency versus drain voltage, (b) instantaneous gain versus drain voltage, (c) instantaneous envelope loadline (V_{env}/I_{env}) versus drain voltage, (d) instantaneous output power versus drain voltage. | 55 |
| Figure 3.5: | Measured results on GaN HFET power amplifier with WCDMA input at 2.14 GHz (a) instantaneous drain efficiency versus drain voltage, (b) instantaneous gain versus drain voltage, (c) instantaneous envelope loadline (V_{env}/I_{env}) versus drain voltage, (d) instantaneous output power versus drain voltage (continued). | 56 |
| Figure 3.6: | Measured drain efficiency of the RF stage along with a WCDMA signal probability density function. | 57 |
| Figure 3.7: | Normalized measured output power spectral density of single carrier WCDMA signal with 7.7-dB PAR before predistortion, after pre-distortion, and after memory-effect mitigation DPD. ($f_{CENTER} = 2.14$ GHz, $P_{OUT} = 2.5$ W) | 58 |
| Figure 3.8: | Measured: (a) AM-AM, (c) AM-PM performance before pre-distortion and (b) AM-AM, (d) AM-PM performance after memory-effect mitigation pre-distortion. | 60 |
| Figure 3.8: | Measured: (a) AM-AM, (c) AM-PM performance before pre-distortion and (b) AM-AM, (d) AM-PM performance after memory-effect mitigation pre-distortion (continued). | 61 |
| Figure 4.1: | Conventional PA with constant supply voltage. | 66 |
| Figure 4.2: | Envelope tracking PA with modulated supply voltage. | 67 |
| Figure 4.3: | Normalized power spectral density (PSD) of the envelope signal for 20 MHz LTE. | 70 |
| Figure 4.4: | Proposed CMOS envelope amplifier. | 72 |
| Figure 4.5: | Simplified schematic of the linear stage. | 73 |
| Figure 4.6: | Simplified simulation schematic for the efficiency of the envelope amplifier as a function of an additional delay in the switcher stage. $R_{load} = 5.7 \Omega$ and $C_{load} = 5$ pF. | 76 |
| Figure 4.7: | Simulated output load and switch current waveforms with an additional switcher stage time delay of 20 ns. | 77 |
| Figure 4.8: | Simulated linear stage main power loss comparison with an additional switcher stage time delay of 20 ns. | 78 |
| Figure 4.9: | Simulated efficiency of the envelope amplifier as a function of an additional delay in the switcher stage. | 79 |
| Figure 4.10: | Die-photograph of envelope amplifier. The chip occupies 1.5 mm ² die area including the pads. | 81 |

| | |
|--|----|
| Figure 4.11: Comparison of measured and simulated envelope amplifier efficiency as a function of signal bandwidth. Sine wave input, $V_{DD} = 5$ V and $R_{load} = 10 \Omega$ | 83 |
| Figure 4.12: Comparison of measured and simulated envelope amplifier efficiency as a function of supply voltage. 5 MHz sine wave input and $R_{load} = 10 \Omega$ | 84 |
| Figure 4.13: Measured envelope amplifier input, output voltage, and switcher stage output voltage. The envelope input signal is a 6.1dB PAR 20 MHz LTE signal. $V_{DD} = 5$ V and 50 ns/div. | 85 |
| Figure 4.14: Measured envelope amplifier output voltage with 1 MHz square waveform input. $V_{DD} = 5$ V, $R_{load} = 5.7 \Omega$. and 500 ns/div. | 86 |
| Figure 4.15: Comparison of measured and simulated envelope amplifier efficiency as a function of output power and LTE signal bandwidths. $V_{DD} = 5$ V. $R_{load} = 5.7 - 9.9 \Omega$ | 87 |
| Figure 4.16: Comparison of measured and simulated envelope amplifier efficiency with a 20 MHz LTE signal as a function of supply voltage. $V_{DD} = 5$ V. $R_{load} = 9.9 \Omega$ | 88 |
| Figure 4.17: Measurement test setup diagram of the complete ET PA. | 90 |
| Figure 4.18: Measured input RF signal and envelope signal under time-alignment condition. | 91 |
| Figure 4.19: Test fixture setup with envelope amplifier IC and RF power amplifier for the envelope tracking system. | 92 |
| Figure 4.20: Normalized measured output power spectral density of single carrier 5 MHz LTE signal with 6.1-dB PAR before predistortion, and after pre-distortion. ($f_{CENTER} = 2.535$ GHz, $P_{OUT} = 27.6$ dBm.) | 93 |
| Figure 4.21: Measured: (a) AM-AM performance before pre-distortion and (b) AM-AM performance after memoryless pre-distortion. | 96 |
| Figure 4.22: Measured: (a) AM-PM performance before pre-distortion and (b) AM-PM performance after memoryless pre-distortion. | 97 |

LIST OF TABLES

| | | |
|------------|--|----|
| Table 1.1: | Comparison of amplifier approaches [2]. | 4 |
| Table 2.1: | Envelope Amplifier Performance Summary in a WCDMA ET System | 43 |
| Table 3.1: | Comparison of Base Stations [7] | 47 |
| Table 3.2: | Performance Summary of Envelope Tracking Power Amplifier with WCDMA Signal | 59 |
| Table 3.3: | Comparison to Previous Monolithic Envelope Tracking Work and the Work Presented in This Paper | 62 |
| Table 4.1: | Performance Summary of the Measured Envelope Amplifier | 94 |
| Table 4.2: | Comparison to Previous Monolithic Envelope Tracking Work and the Work Presented in This Chapter | 95 |

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- M. Kwak, J. Jeong, M. Hassan, J. J. Yan, D. Kimball, P. M. Asbeck, and L. E. Larson, "High efficiency wideband envelope tracking power amplifier with direct current sensing for LTE applications," submitted to *IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, 2012.
- M. Kwak, D. Kimball, C. Presti, A. Scuderi, C. Santagati, J. Yan, P. M. Asbeck, and L. E. Larson, "Design of wideband high-voltage high-efficiency BiCMOS envelope amplifier for Micro-base station RF power amplifiers," submitted to *IEEE Transactions of Microwave Theory and Techniques*, 2011.
- M. Kwak, J. Jeong, M. Hassan, J. J. Yan, D. Kimball, P. M. Asbeck, and L. E. Larson, "Design of a high efficiency CMOS envelope amplifier with direct current sensing for handset RF power amplifiers," to be submitted to *IEEE Transactions of Microwave Theory and Techniques*, 2012.

The dissertation author was the primary researcher and the first author listed in

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M. Kwak, D. Kimball, C. Presti, A. Scuderi, C. Santagati, J. Yan, P. M. Asbeck, and L. E. Larson, "Wideband high efficiency envelope tracking integrated circuit for Micro-base station power amplifiers," *Proc. IEEE Radio Frequency Integrated Circuits Symp., RFIC*, 2011, pp. 145-148.

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M. Hassan, M. Kwak, V. W. Leung, C. Hsia, J. J. Yan, D. F. Kimball, L. E. Larson, and P. M. Asbeck, "High efficiency envelope tracking power amplifier with very low quiescent power for 20 MHz LTE," *Proc. IEEE Radio Frequency Integrated Circuits Symp., RFIC*, 2011, pp. 131-134.

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ABSTRACT OF THE DISSERTATION

**High Efficiency Wideband Envelope Tracking Power Amplifier for
Next-Generation Wireless Communications**

by

Myoungbo Kwak

Doctor of Philosophy in Electrical Engineering (Electronics Circuits and Systems)

University of California, San Diego, 2011

Professor Lawrence E. Larson, Chair

The latest generation of smart devices deployed in cellular networks has created explosive growth in network data traffic, and the increasing demand for broadband services with higher data rates, require higher peak to average power ratio (PAPR) with wider bandwidth. One of the challenges in the conventional power amplifiers (PAs) with fixed supply voltage, is the degraded efficiency and generated heats at a large back-off to meet tight linearity requirements. This dissertation presents high efficiency wideband envelope tracking power amplifiers for 2.1 GHz micro base-stations and 2.5 GHz wireless mobile applications. By superimposing the envelope signal at the drain such

that the RF amplifier operates consistently closer to saturation, the overall efficiency is improved and the generated heat is reduced dramatically.

In the first part of the dissertation, a high performance BiCMOS DMOS monolithic envelope amplifier for micro-base station power amplifiers is presented. Due to the low breakdown voltage of the CMOS transistors, the high voltage envelope amplifier has been implemented with discrete components with high voltage process. Compared to these discrete solutions, an integrated circuits implementation for the envelope amplifier brings many benefits. The design of monolithic envelope amplifiers for high voltage ($V_{DD} = 15$ V) envelope tracking applications, and the design techniques to solve the reliability issues with thin gate oxide is described. The overall envelope tracking system employing a GaN-HEMT RF transistor, and fully integrated high voltage envelope amplifier with a $0.35\mu\text{m}$ BiCMOS DMOS process, is demonstrated.

In the second part, a high-efficiency wideband envelope tracking power amplifier for mobile LTE applications will be presented. The CMOS envelope amplifier with hybrid linear and switcher is designed in a 150 nm CMOS process. The envelope amplifier employs direct sensing of the linear stage current to reduce the propagation delay in the switcher. The strategy is demonstrated to improve the efficiency of the complete envelope tracking power amplifier system. The resulting performance of envelope tracking system employing a GaAs HBT-based RF PA with a 5 MHz LTE signal input demonstrated state-of-the-art efficiency while meet the linearity requirement.

Chapter 1

Introduction

Albert Einstein, when asked to describe radio, replied:

"You see, wire telegraph is a kind of a very, very long cat. You pull his tail in New York and his head is meowing in Los Angeles. Do you understand this? And radio operates exactly the same way: you send signals here, they receive them there. The only difference is that there is no cat."

1.1 Modern Wireless Communications

The modern wireless communications has been developed with a long history and the key inventions such as radio, telephone, wireless devices, and integrated circuits, make big impacts on human life. The latest generation of smart devices deployed in cellular networks has created explosive growth in network data traffic, and the volume of data traffic has already exceeded that of voice traffic. Motivated by the increasing demand for mobile broadband services with higher data rates, the next-generation mobile standards, signals in 3G systems and beyond require higher peak to average power ratio (PAPR) and wide channel bandwidth. As a result, transmitters in the modern wire-

less communication system, require high efficiency wideband RF amplifiers to transmit complex modulation signals in order to provide good quality of wireless services.

In addition, the research on the extension of network coverage without increasing the density of traditional macro base stations, have motivated to cover the seamless support for the extensive mobile data usage such as mobile web browsing and video streaming contents. By installing smaller base stations, such as micro, pico and femto cells, to complement the conventional macro base stations, coverage can be significantly improved. The micro base station concept is ideal for operators needing a cost effective solution for high data rates to end users, without over-building the traditional macro base station network.

1.2 Wireless Transceiver Systems and Power Amplifiers

A modern wireless transceiver systems consists of a transmitter, a receiver and the airchannel, in general. The common transmitter system, as illustrated in Fig. 1.1, has three major functions of modulation, frequency conversion and power amplification. The power amplifier is the final interface from the baseband signal to the antenna systems, and the main function is the amplification of the input signal and delivery of the resulting power to the antenna [2]. The generation of high output power leads to a high DC power consumption, thus, the power consumption of transceivers is mainly determined by the transmitter rather than by the receiver, in active operation [1]. Thus, high efficiency RF power amplifier is critical in the modern transmitter design. This demand leads designers to explore cost-effective and high performance solutions, many architectures have emerged for the design of high efficiency power amplifiers. A brief review on basic amplifier topologies will be discussed in the next section.

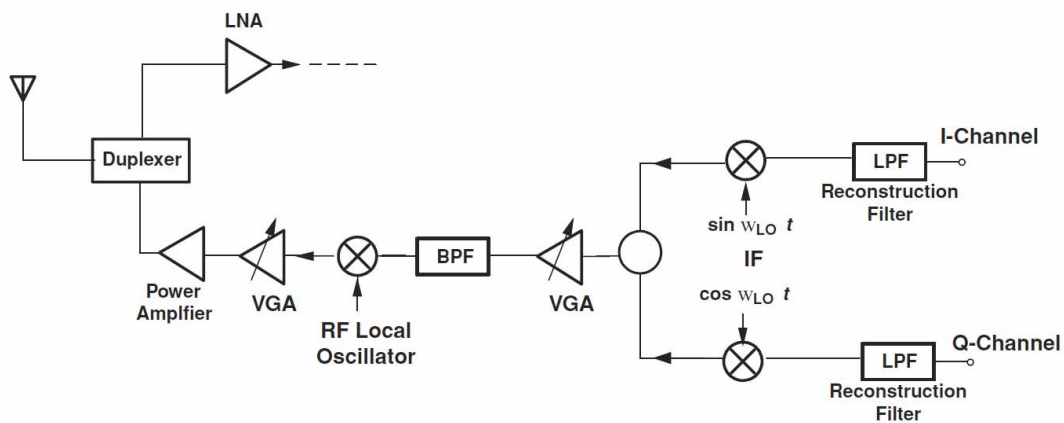


Figure 1.1: Heterodyne wireless handset transmitter section, showing a complete upconversion path from baseband [1].

1.3 Efficiency and Linearity Enhancement Techniques

In Table 1.1, comparison of the classical linear and switched power amplifiers are listed [2]. The selection of power amplifier type is generally depends on the key design parameters according to the applications. For example, the key characteristics of power amplifiers, efficiency and linearity, have trade-offs, as shown in Fig. 1.2. For the standard power amplifier topologies, such as classes A and AB, relatively high linearity can be obtained, but the efficiency is dramatically reduced at a output power back-off conditions. At 10 dB power backoff of class-A and class-B amplifiers, the efficiencies fall from 50% to 5% and from 78.5% to 25%, respectively [2]. In other words, amplifiers have to be driven close to their saturation region to have maximum output power and higher efficiency. Thus, various efficiency and linearity enhancement techniques are proposed to solve these problems, and a brief review on these topologies will be discussed in the following sections.

Table 1.1: Comparison of amplifier approaches [2].

| Type | Classical Current Source Amplifier | | | | | Switched Amplifiers | | |
|---------------------------|--|--------------------------------------|--|--|--|--|--|--|
| | Class-A | Class-AB | Class-B | Class-C | Class-D | Class-E | Class-F | |
| Sub-type | Class-A | Class-AB | Class-B | Class-C | Class-D | Class-E | Class-F | |
| Bias point | $I_{dc}=I_{max}/2$ $V_{dc}=V_{max}/2$ | Between A and B | $I_{dc}=I_{max}/\pi$ $V_{dc}=V_{max}/2$ | $I_{dc}<I_{max}/\pi$ $V_{dc}=V_{max}/2$ | $I_{dc}=I_{max}/\pi$ $V_{dc}=V_{max}/2$ | $I_{dc}=I_{max}/2.86$ $V_{dc}=V_{max}/3.56$ | $I_{dc}=I_{max}/\pi$ $V_{dc}=V_{max}/2$ | |
| Output waveform | Both polarities of sinusoidal | More than one polarity of sinusoidal | Positive part of sinusoidal | Peak wave | Both polarities of sinusoidal | Both polarities of sinusoidal | Both polarities of sinusoidal | |
| $p_n(= P_{fund}/P_{max})$ | 1/8 | Up to 0.1375 | 1/8 | < 1/8 | 1/π | 0.0981 | 1/2π | |
| η_{max} at P_{max} | ≤ 50% | 50%-78.5% | 78.5% | 78.5%-100% | 100% | 100% | 100% | |
| Heat power/ P_{dc} | ≥ 50% | 21.5%-50% | ≥ 21.5% | ≤ 21.5% | 0% | 0% | 0% | |
| Possible bandwidth | High | High | Moderate | Low | Depends on transformer bandwidth | Small, class-E resonance | Small due to filter bandwidth | |

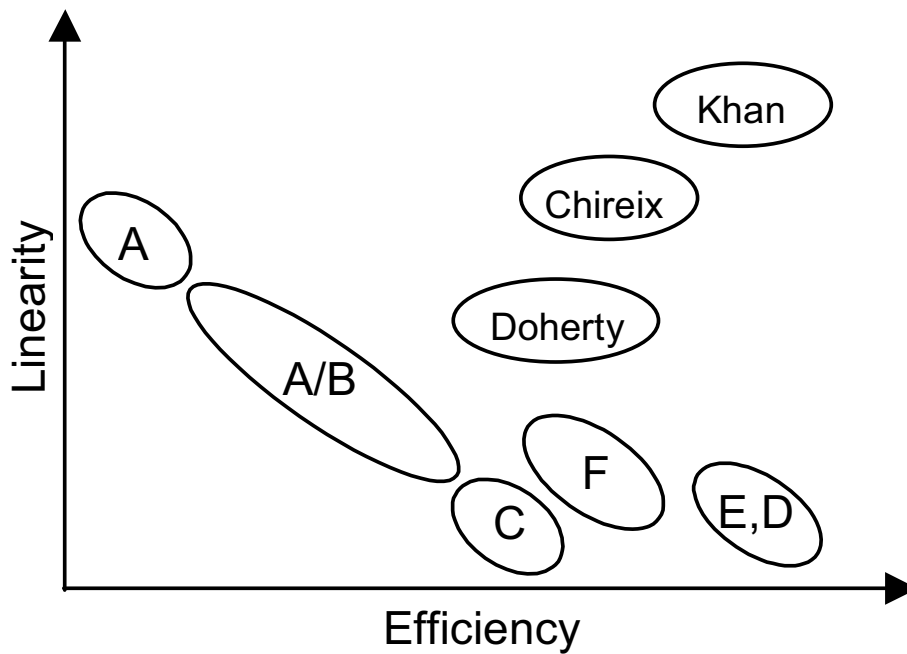
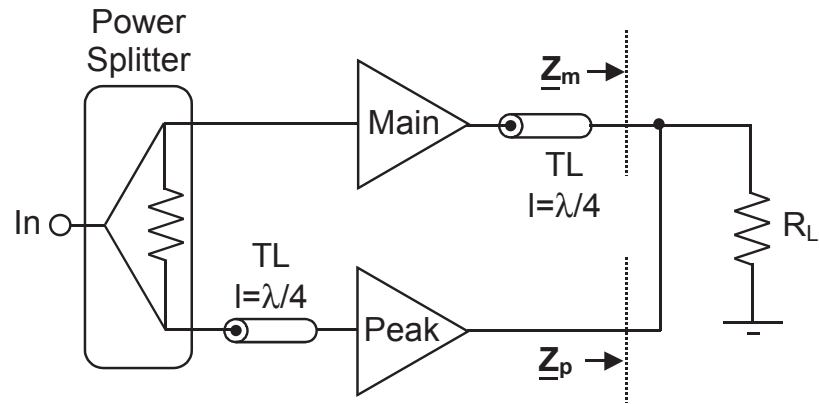


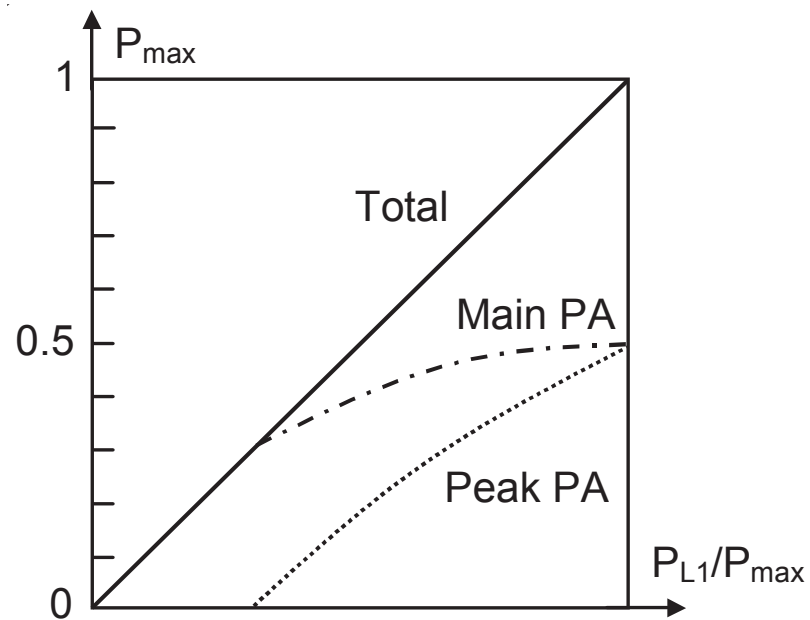
Figure 1.2: Trade-off between efficiency and linearity [2].

1.3.1 Doherty Power Amplifier

Doherty amplifier was proposed by William H. Doherty [8] in 1930s and was originally employed for high power AM radio transmitter using vacuum-tube amplifiers. The simplified configuration of a Doherty amplifier, which consists of two amplifiers, the main amplifier biased in Class AB, and the peak amplifier biased in Class C in general, is shown in Fig. 1.3(a). The main and peak amplifiers are connected in parallel with the outputs joined by a quarter-wave transmission line, which performs impedance transformation. At low powers, the main amplifier is operated with a relatively high load impedance, which allows it to achieve high efficiency. At the same time, the peak amplifier is usually off because it is biased in class C. At high powers, both amplifiers are turned on and the peak amplifier delivers current as the main amplifier saturates. This joint mechanism helps to achieve high efficiency without hard saturation of the



(a)



(b)

Figure 1.3: (a) Simplified block diagram of a Doherty PA, (b) power properties [2].

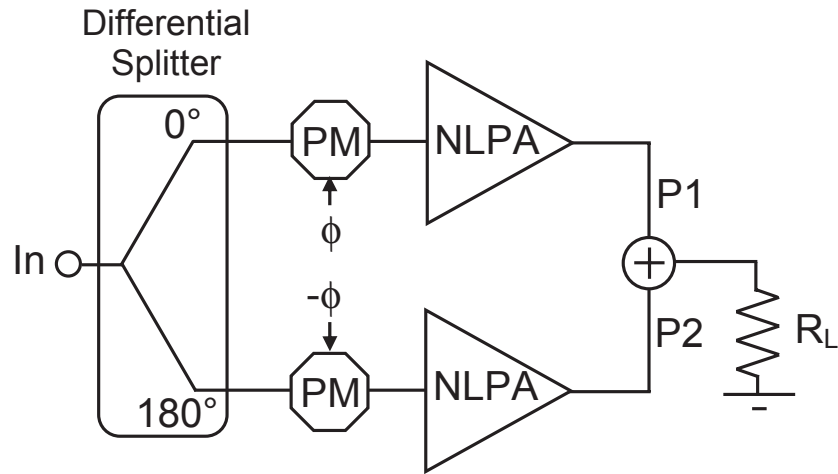
main amplifier.

In general, Doherty amplifiers shows better efficiency as compared with classic class-AB amplifier while the linearity performance is similar, as shown in Fig. 1.2. Thus, it could be a good candidate for the replacement of the low efficiency linear amplifiers [9–20]. However, there are drawbacks according to the applications: (1) the quarter-wave transmission line is fixed at the specific RF frequency, and this limits the use in multi-band applications, (2) the linearity is degraded by the action of the peak amplifier, whose phase behavior may be very different from that of the main amplifier [1], and (3) the maximum efficiency is dependent on the peak-to-average power ratio (PAPR), and optimum PAPR is fixed such as 6 dB.

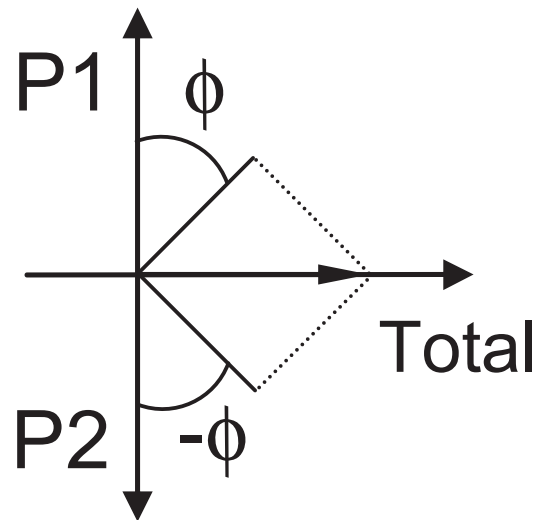
1.3.2 LINC and Chireix Outphasing Power Amplifier

Linear amplification with nonlinear components (LINC) is a method of vector summing two constant amplitude phase-modulated signals to achieve power amplification. Basic idea comes from that the switched amplifiers such as class-D can not be used for amplitude modulation, although the maximum efficiency can be 100% ideally. The theoretical efficiency of the LINC power amplifier has been reported as 100% since highly efficient nonlinear constant amplitude amplifiers can be used. However, the 100% efficiency performance is only possible at one or two loads along the power output curve. The Chireix outphasing amplifier, as shown in Fig. 1.4(a), is one example of an LINC approach. The differential input signal is split into two signal paths, which are modulated by $+\phi$ and $-\phi$, and then amplified by two identical nonlinear PAs(NLPAs). The combined output power can have wide range of amplitude modulation according to the proper phase(ϕ), as shown in Fig. 1.4(b).

Although its maximum achievable efficiency is very high, this architecture has



(a)



(b)

Figure 1.4: (a) Simplified block diagram of a LINC PA, (b) amplitude combining [2].
NLPA : Nonlinear Power Amplifier.

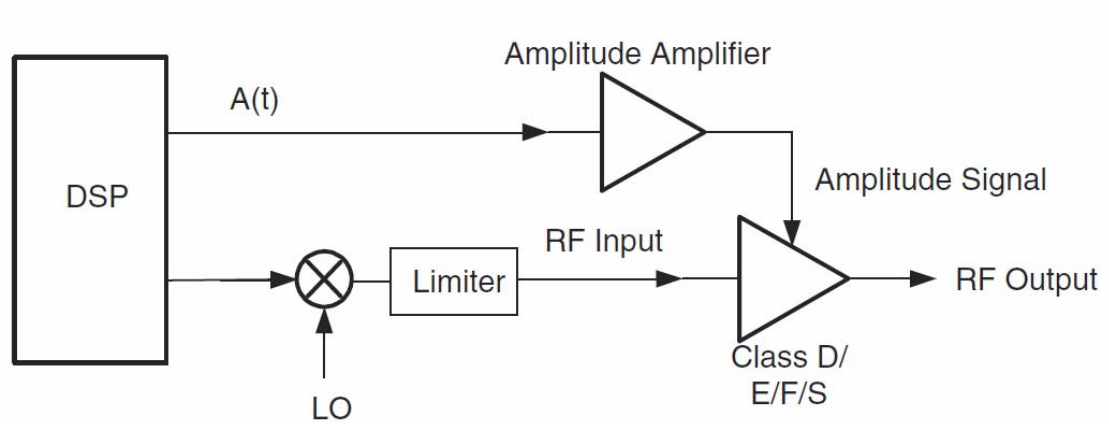
limitations. Several design approaches are proposed in [21–29] to overcome these limitations, LINC amplifiers are not widely adapted today as compared with other efficiency enhancement techniques. For example, the power combiner at the output has to have good isolation in addition to the low loss and sufficient bandwidth. In addition, two input phase should be equal, but the input phases vary with frequency.

1.3.3 Envelope Elimination and Restoration (EER) and Envelope Tracking (ET) Power Amplifiers

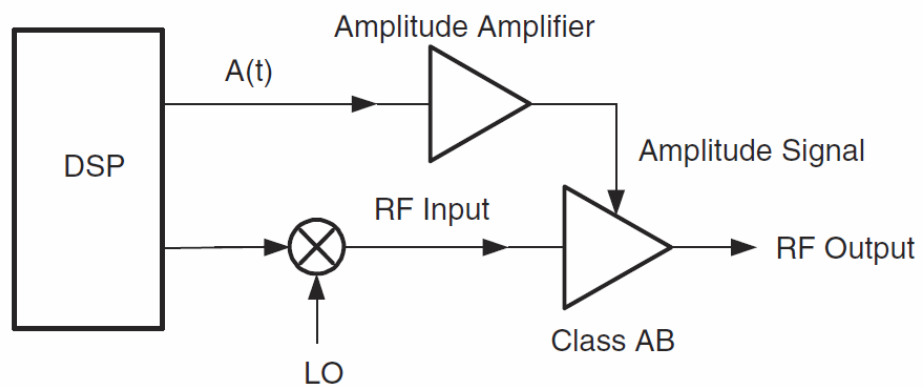
Envelope elimination and restoration (EER) was proposed by Leonard R. Kahn in 1950s [30]. As shown in Fig. 1.5(a), the phase modulation (PM) signal is fed into a limiter preserving the PM information, and the amplitude modulation (AM) signal modulating the drain (or collector) supply voltage of the PA. This architecture consists of a high-efficiency switch-mode amplifier, limiter and an envelope amplifier. Since the RF PA always operate at the saturation in this scheme, EER technique theoretically can achieve very high efficiency [31].

The resulting constant amplitude phase modulated carrier is then amplified by a switch-mode PA like Class E or Class F [3, 32–34]. However, it faces several implementation issues for base-station power amplifiers, such as 1) the linearity is stringently dependent on the time-alignment between RF input and dynamic envelope voltage [35], and 2) the envelope eliminated input signal will have extreme bandwidth such that a high power input driver is typically required, which lowers the system overall performance.

Envelope Tracking (ET) technique is similar with EER in the sense of dynamic power supply modulation. The main difference with EER is that ET utilize a linear PA and the modulated supply voltage tracks the long-term average of the output envelope



(a)



(b)

Figure 1.5: Simplified block diagram of: (a) an Envelope Elimination and Restoration (EER) PA, (b) an Envelope Tracking (ET) PA [1, 3].

signal, as shown in Fig. 1.5(b). This approach gives another benefits, as compared to the EER techniques, that the stringent time-mismatch is not required and free from the possible bandwidth limitation in the limiter. The efficiency attained in the envelope tracking amplifier is dramatically better than that obtained with constant supply voltage because 1) the RF amplifier operates closer to saturation at all times and 2) the transistor temperature is maintained at a lower value due to the reduced thermal dissipation as well as the thermal partitioning between the envelope amplifier and RF stage [6, 36]. Envelope tracking techniques have demonstrated excellent performance from mobile station to macro base-station applications [33, 37–48]. A more detailed description of the ET system including an envelope amplifier design will be described in the following chapters.

1.3.4 Linearity Improvements with Pre-Distortion Techniques

The poor efficiency of a power amplifier in real situations can be improved with the efficiency improvement techniques such as Doherty, LINC, EER, and ET. However these techniques also degrade the linearity of the power amplifier to achieve higher efficiency. To improve the linearity, a series inverse nonlinear characteristics can be added as shown in Fig. 1.6. This pre-distortion technique can be applied to fix AM-AM distortion and AM-PM distortion in a power amplifier, and conceptually the gain and phase nonlinearity could be canceled out.

However, the pre-distortion approach suffers from several practical drawbacks. For example, it is very difficult to track precisely the effects of temperature, process, and power supply variations on the characteristics of the power amplifier nonlinearity [1]. This practical limitation have motivated the research on the robust and complicated lin-

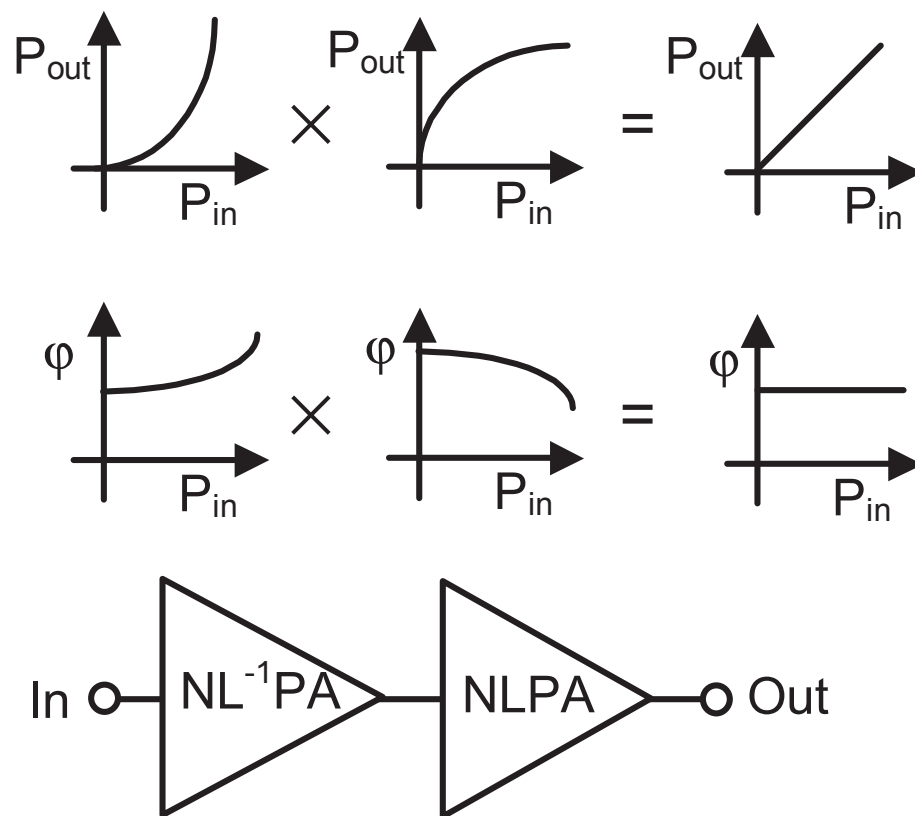


Figure 1.6: Illustration of predistortion, cascading of NLPA (Nonlinear Power Amplifier) together with circuit providing inverse nonlinear characteristics ($NL^{-1}PA$) [2].

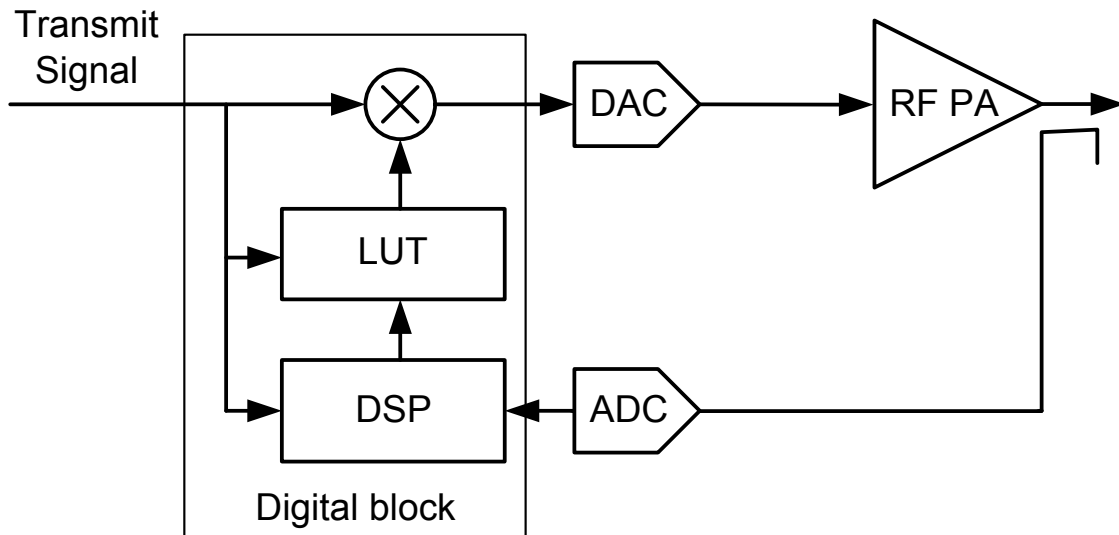
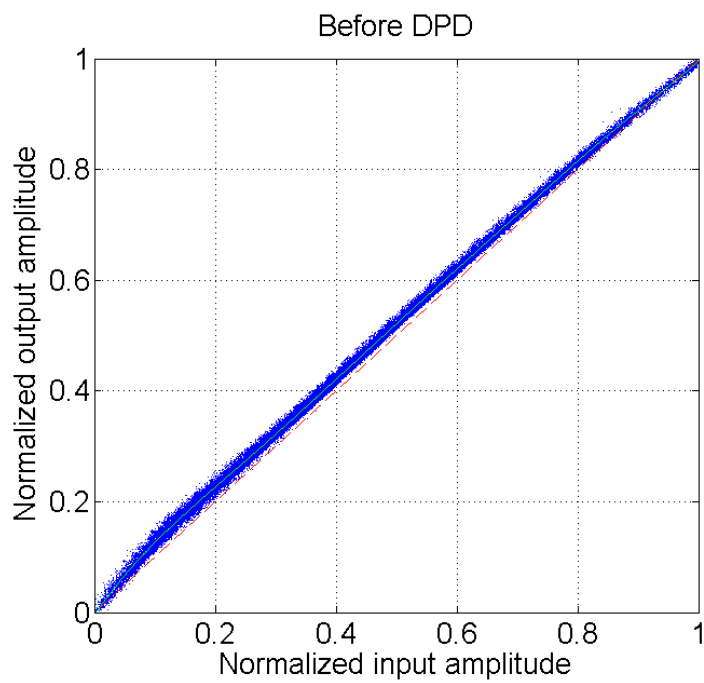


Figure 1.7: Simplified schematic of digital pre-distortion (DPD) based on look-up table(LUT).

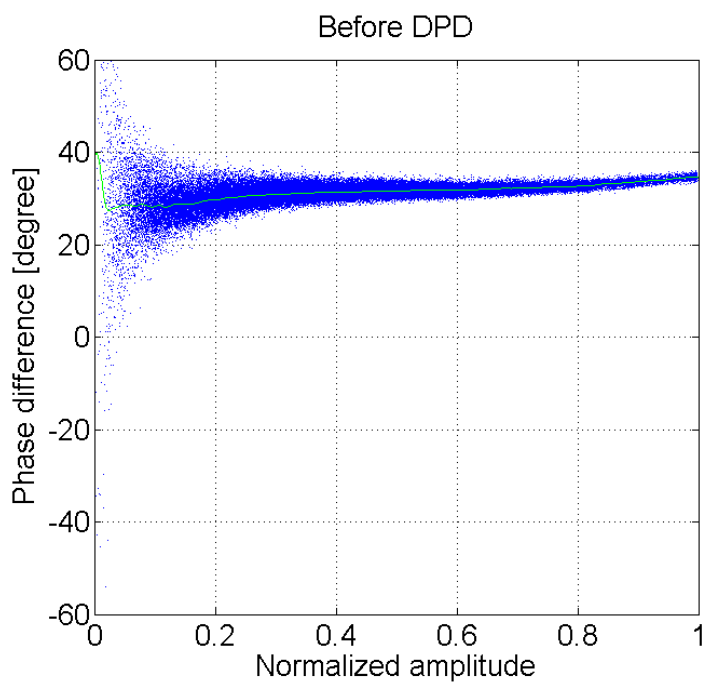
earity enhancement techniques.

To improve robustness in the pre-distortion, the pre-distortion can be performed using digital techniques at baseband frequencies, as shown in Fig. 1.7. For an effective pre-distortion technique, the amplified and distorted output signal should be measured first, and stored in a look-up table (LUT) in this scheme. After appropriate digital processing based on LUT, which contains the pre-distorted signal values, the compensated signal will be transmitted to the RF path to improve the linearity characteristics. An advantage of digital pre-distortion lies in its flexibility. If the behavior of the RF PA changes, a new set of pre-distorted signal values is calculated and updated in the LUT. Using this method, the AM-AM and AM-PM distortions can be corrected and the overall linearity will be improved.

In this digital pre-distortion (DPD) techniques, memory mitigated DPD can be also implemented to reduce the memory effects in a power amplifier [37, 49–52]. A

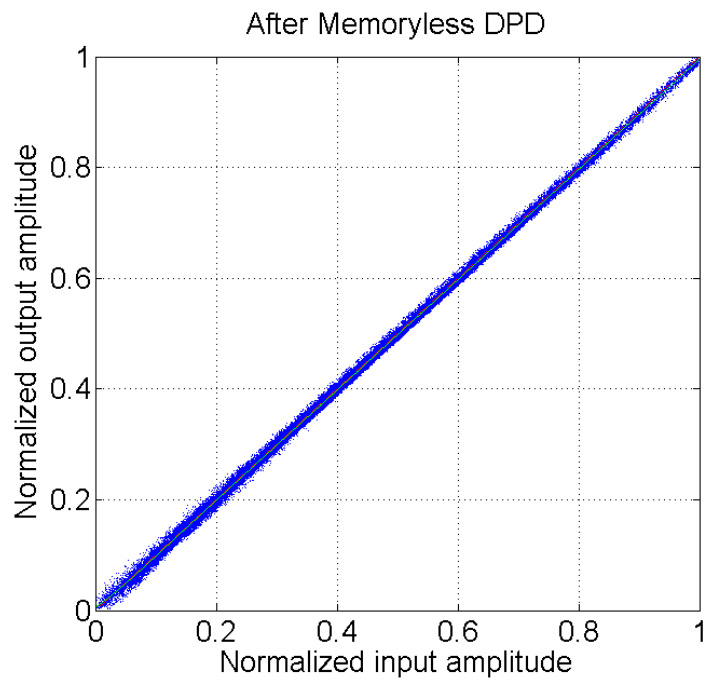


(a)

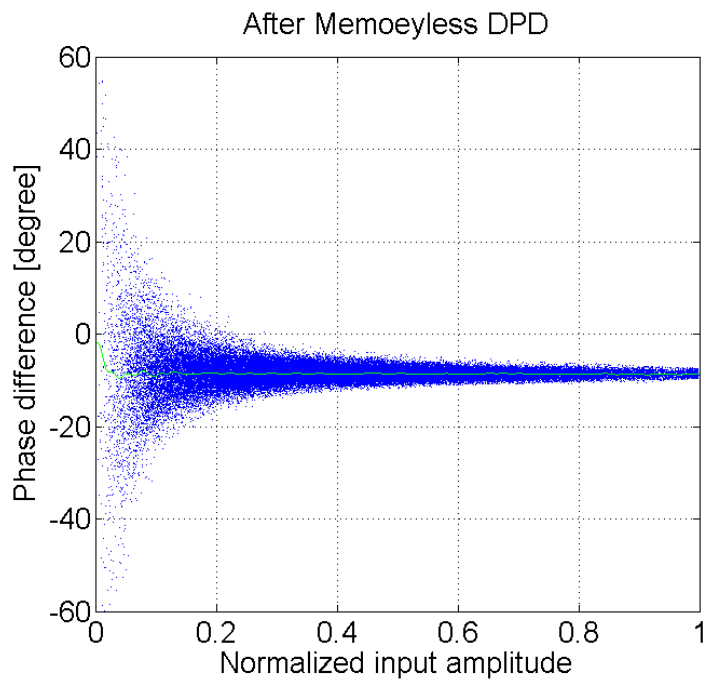


(b)

Figure 1.8: Measured: (a) AM-AM, (b) AM-PM performance before pre-distortion after memory-effect mitigation pre-distortion.

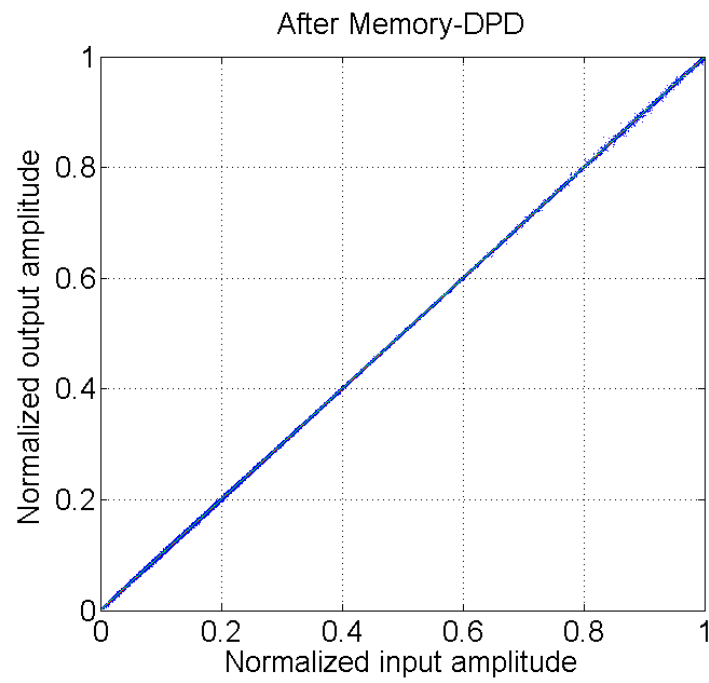


(a)

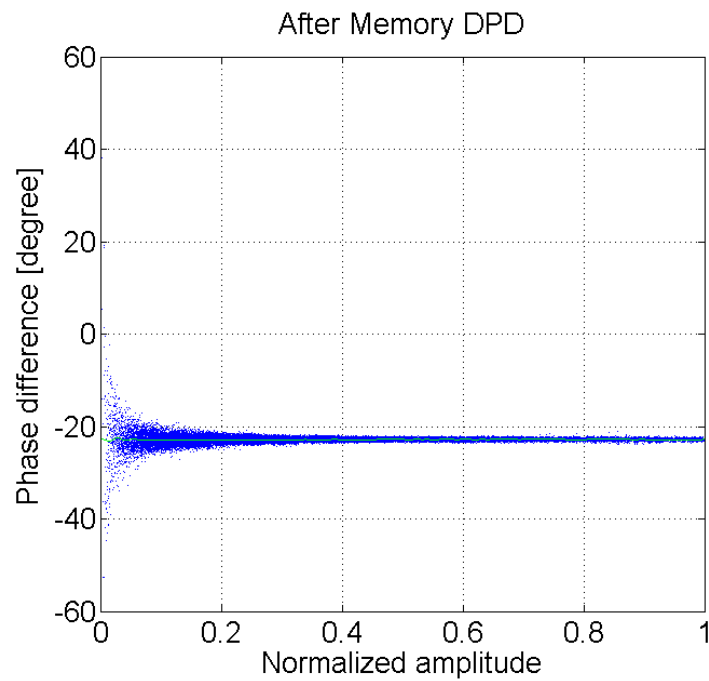


(b)

Figure 1.9: Measured: (a) AM-AM, (b) AM-PM performance after memoryless pre-distortion.



(a)



(b)

Figure 1.10: Measured: (a) AM-AM, (b) AM-PM performance after memory-effect mitigation pre-distortion.

typical example of a memory effect is the thermal behavior of the power amplifier. If the amplifier operates at a higher output power, the amplifier heats up due to the generated heats. Then if the output power is reduced, the higher temperature of the amplifier will change the distortion characteristics.

In Fig. 1.8, the measured AM-AM and AM-PM curves are shown for a digital pre-distortion example of an envelope tracking power amplifier. The scatter of the plotted data indicates a modest memory effect and nonlinearity. After memoryless digital pre-distortion, the distortions are improved, as shown in Fig. 1.9. Memory mitigation DPD results in a further improvement in the linearity characteristics as shown in Fig. 1.10. The AM-AM and AM-PM distortions are almost nonexistent after memory mitigated DPD. This implies that the efficiency improvements techniques along with DPD, the higher efficiency can be achieved while meeting the tight linearity requirements.

1.4 Dissertation Objectives and Organization

This dissertation is dedicated to exploring the design of the integrated envelope amplifiers used in the high efficiency wideband envelope tracking RF power amplifiers for modern wireless communication systems. To design a high efficiency wideband envelope amplifier circuit for high efficiency and good linearity performance, two major challenges are investigated and analyzed: (1) development of high-voltage envelope amplifier architecture to solve the reliability issue regarding thin-gate oxide in the BiCMOS DMOS process technology, (2) analysis and design of envelope amplifier for wide bandwidth with CMOS process technology.

The dissertation is organized as follows:

In chapter 2, a high performance BiCMOS DMOS monolithic envelope amplifier for micro-base station power amplifiers is presented. Due to the low breakdown

voltage of the CMOS transistors, the high voltage envelope amplifier has been implemented with discrete components with high voltage process. The design of monolithic envelope amplifiers for high voltage ($V_{DD} = 15$ V) envelope tracking applications, and the proposed design techniques to solve the reliability issues with thin gate oxide is described.

In chapter 3, the design of the envelope tracking power amplifier is reviewed to improve overall efficiency. The overall envelope tracking system employing a GaN-HEMT RF transistor, and fully integrated high voltage envelope amplifier with a $0.35\mu\text{m}$ BiCMOS DMOS process, is demonstrated.

In chapter 4, a high-efficiency wideband envelope tracking power amplifier for mobile LTE applications is presented. The CMOS envelope amplifier with hybrid linear and switcher is designed in a 150 nm CMOS process. The envelope amplifier employs direct sensing of the linear stage current to reduce the propagation delay in the switcher. This strategy is demonstrated to improve the efficiency of the complete envelope tracking power amplifier system.

Chapter 5 concludes the dissertation and possible future investigation areas are suggested.

Chapter 2

Design of High Voltage Envelope Tracking Integrated Circuit for Micro-Base Station Power Amplifiers

2.1 Introduction

In modern wireless communication transmitter systems, high power efficiency is an important objective in addition to high linearity. The envelope tracking (ET) system shown in Fig. 2.1 improves the efficiency of a power amplifier (PA) by superimposing the envelope signal at the drain, such that the RF amplifier operates consistently closer to saturation [35]. The RF transistor is biased in the Class AB region and the envelope signal provides the dynamic supply biasing to the RF PA. In much of the past work, envelope tracking techniques for macro base stations have demonstrated excellent performance, but the envelope amplifier was implemented using discrete components [6, 37, 53, 54]. Compared to these discrete solutions, an integrated circuit implementation for the envelope amplifier brings many benefits because 1) it can minimize

cost, 2) an integrated signal path provides better signal integrity, and 3) each transistor design parameter can be chosen for optimum size and power level for better performance. In [39, 45, 55–57], integrated envelope amplifiers for handset applications have been reported; however, the average output power was less than 1 W and the supply voltage was limited to 5 V due to the breakdown voltage of the CMOS transistors. For micro base-station applications, a higher supply voltage is required to generate the average output power of 2 to 4 W. Recently, high-voltage LDMOS devices have been integrated with CMOS devices in a single IC process [5].

In this chapter, we implement a high voltage envelope amplifier in a Bipolar-CMOS-DMOS (BCD) process technology for micro base-station applications. To our knowledge, this is the first high-voltage monolithic envelope amplifier for multi-watt wide bandwidth RF applications. This chapter is organized as follows. Section 2.2 describes the detailed design consideration and circuit level implementation of a proposed envelope amplifier. In Section 2.3, experimental results are shown for WCDMA signals and a conclusion is given in Section 2.4.

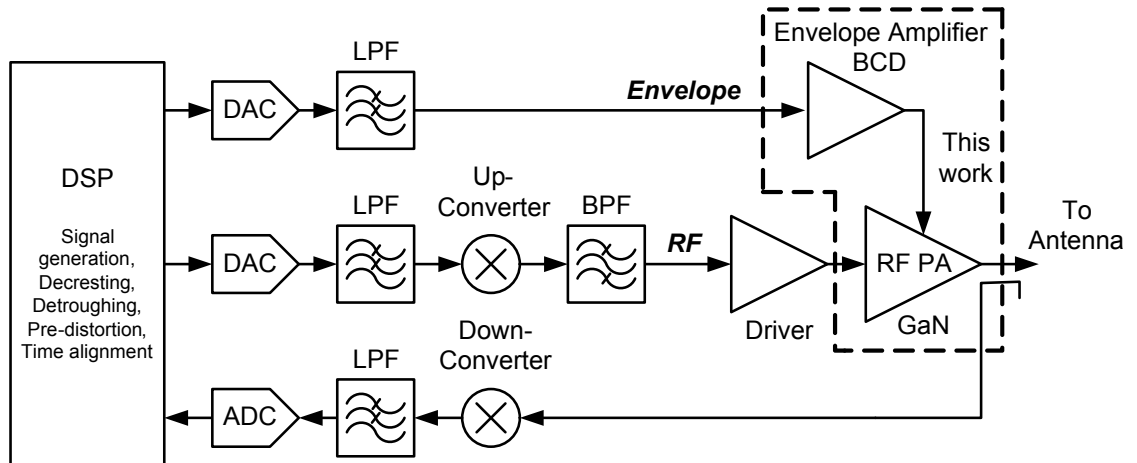


Figure 2.1: Block diagram of wireless transmitter with envelope tracking system for improved efficiency.

2.2 Envelope Tracking Amplifier Circuit Design and Implementation

High efficiency is one of the main goals in the envelope amplifier circuit design, while maintaining high linearity. The efficiency of the proposed envelope amplifier, as shown in Fig. 2.2, can be evaluated by considering the power loss mechanisms associated with each stage. The efficiency of the envelope amplifier, η_{env} , is given by

$$\eta_{env} = \frac{P_{out}}{P_{dc}} = \frac{P_{out}}{P_{out} + P_{loss}} \quad (2.1)$$

where $P_{loss} = P_{loss_lin} + P_{loss_sw}$, P_{out} is the output power of the envelope amplifier, P_{dc} is the dc power dissipated by the envelope amplifier, P_{loss} is the total power loss of the envelope amplifier, P_{loss_lin} is the loss of the linear stage, and P_{loss_sw} is the loss of the switcher stage, respectively.

In previous work [6], linear-stage efficiency was analyzed in the presence of an ideal switcher stage, and the loss of the linear stage is ideally zero at the average (or dc) level of the input signal, since all the average power is supplied by the ideal switcher stage. In a real circuit implementation, the power loss at this operating point is not zero due to the fact that the output stage quiescent current is not zero and there are static dc bias currents.

Figure 2.3 shows the schematic of the linear stage. The first stage is implemented with a folded-cascode type amplifier to achieve high gain, and the output transistors are connected in a common-source configuration for near rail-to-rail output voltages [58]. Class-B output stages have very low quiescent current, but introduce crossover distortion. To achieve a good compromise between distortion and quiescent dissipation,

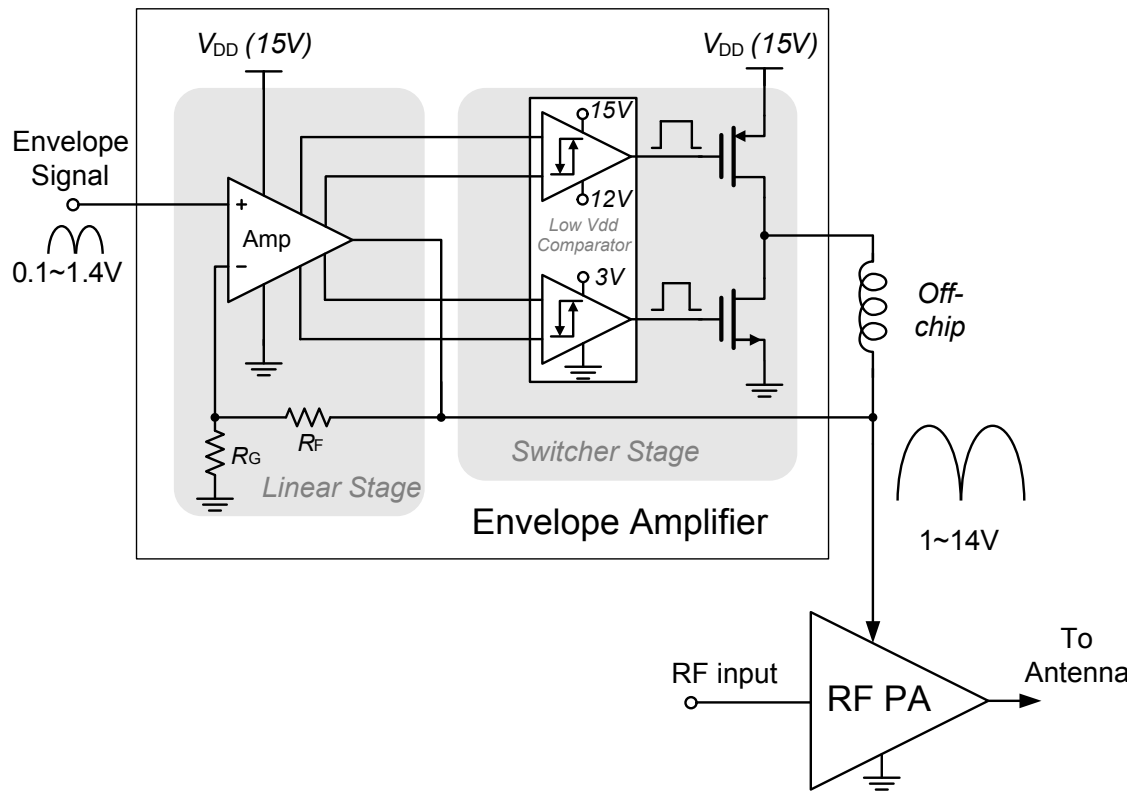


Figure 2.2: Proposed monolithic envelope amplifier schematic.

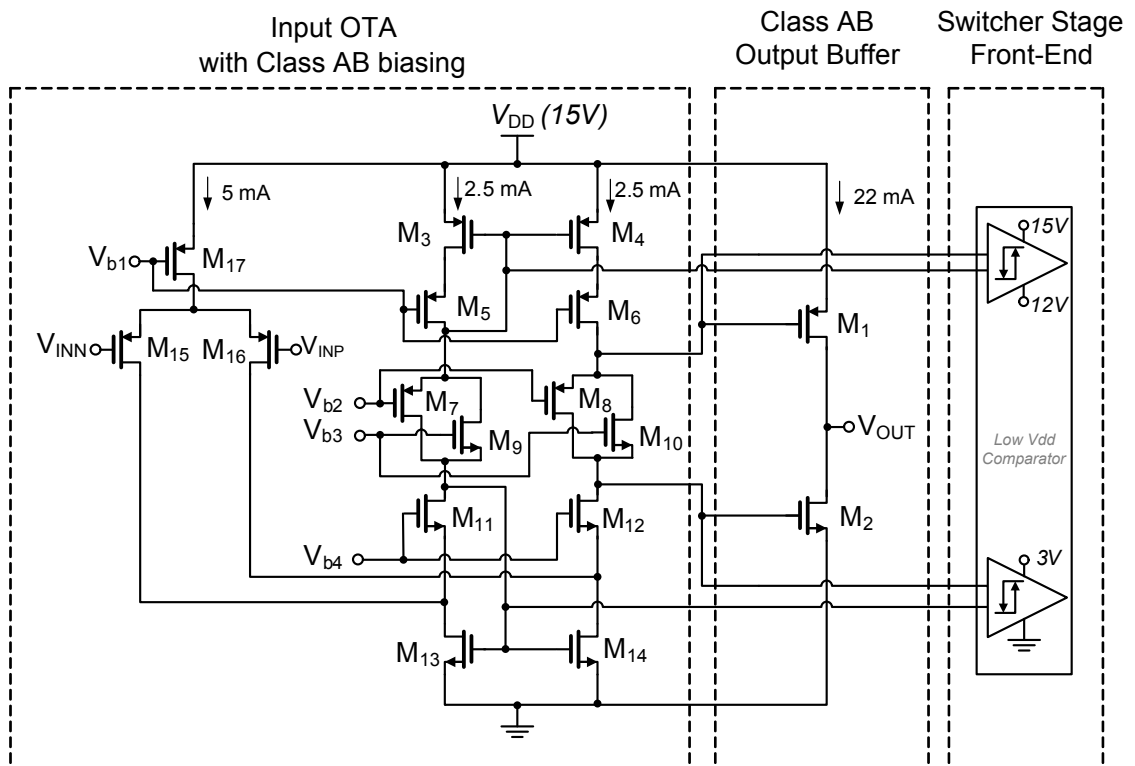


Figure 2.3: Simplified schematic of the linear stage. All the devices are $0.35\text{-}\mu\text{m}$ DMOS, and the $|V_{GS}|$ was limited to 3.3 V in all cases.

the output stage is biased in class-AB mode. In this case, the output transistors are biased at a small (3%) quiescent current compared to the maximum output current to prevent a turn-on delay of the non-active output transistor [58]. The class-AB biasing can be realized by keeping the voltage difference between the gates of the output transistors M_1 and M_2 at a constant value. In [39], class-AB biasing circuitry was implemented with a source follower and its biasing circuit, which were separated with the input OTA. In this design, the class-AB control is implemented by M_8 and M_{10} , as shown in Fig. 2.3 to save die area and reduce dc bias currents [58]. By eliminating the bias sources of the class-AB control, the static dc bias currents in the linear stage can be reduced.

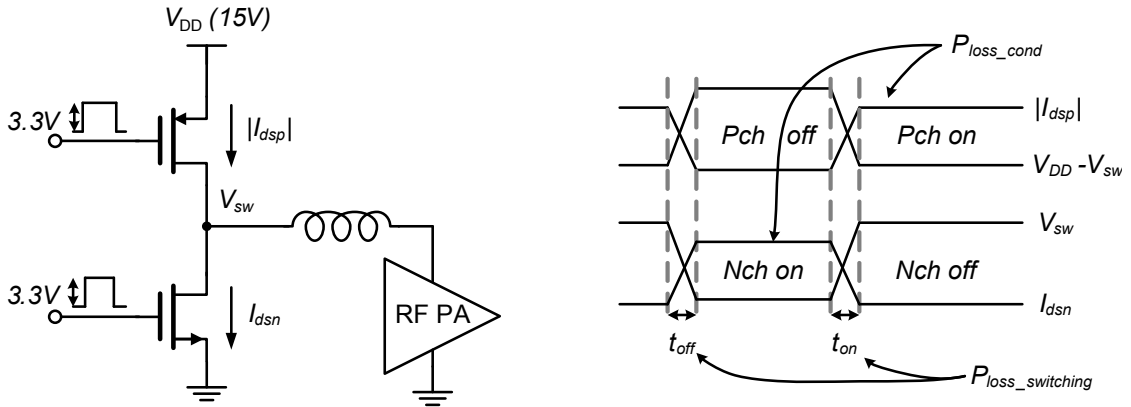


Figure 2.4: Switch voltages and currents in a buck-converting switcher [4].

The power loss in the buck switching converter comes from two sources: conduction loss, P_{loss_cond} and switching loss, $P_{loss_switching}$ as shown in Fig. 2.4. These two sources have different design parameters and it is important to minimize these power losses together in the switcher-stage circuit design. The power loss of the switching-FETs in the switcher stage is simulated as a function of the various device widths and the average switching frequencies, and the results are shown in Fig. 2.8.

As shown in Fig. 2.4, the conduction loss results from the loss that is generated when the P-channel (or N-channel) LDMOS switching FET is on, and is approximately

$$P_{loss_cond} \cong D \cdot I_{on}^2 \cdot R_{onp} + (1 - D) \cdot I_{on}^2 \cdot R_{onn} \quad (2.2)$$

where D is the average duty cycle ratio of the switching pulses, I_{on} is the drain current while the switching FET is on, R_{onp} is the *on* resistance of the P-channel LDMOS switching FET, and R_{onn} is the *on* resistance of the N-channel LDMOS switching FET, respectively. The conduction loss as shown in Fig. 2.5, is not dependent on the switching frequency and is inversely proportional to the device width. To minimize the conduction loss, the wider device width is preferred.

The switching loss, $P_{loss_switching}$, is the sum of the losses caused from simultaneous current and voltage during the turn-on and turn-off time, as well as the loss due to the output drain capacitance and the loss due to the input gate capacitance during switching. So, the switching loss can be expressed as the sum of three factors.

$$P_{loss_switching} = P_{loss_cross} + P_{loss_swout} + P_{loss_driver} \quad (2.3)$$

where P_{loss_cross} is the crossover loss when both p-channel and n-channel devices are on during the turn-on and turn-off periods, P_{loss_swout} is the dynamic dissipation at the switcher output node and P_{loss_driver} is the input driver power dissipation, respectively. In Fig. 2.4, the switching loss is generated during the switch turn-on and turn-off time period and dependent on the switching frequency.

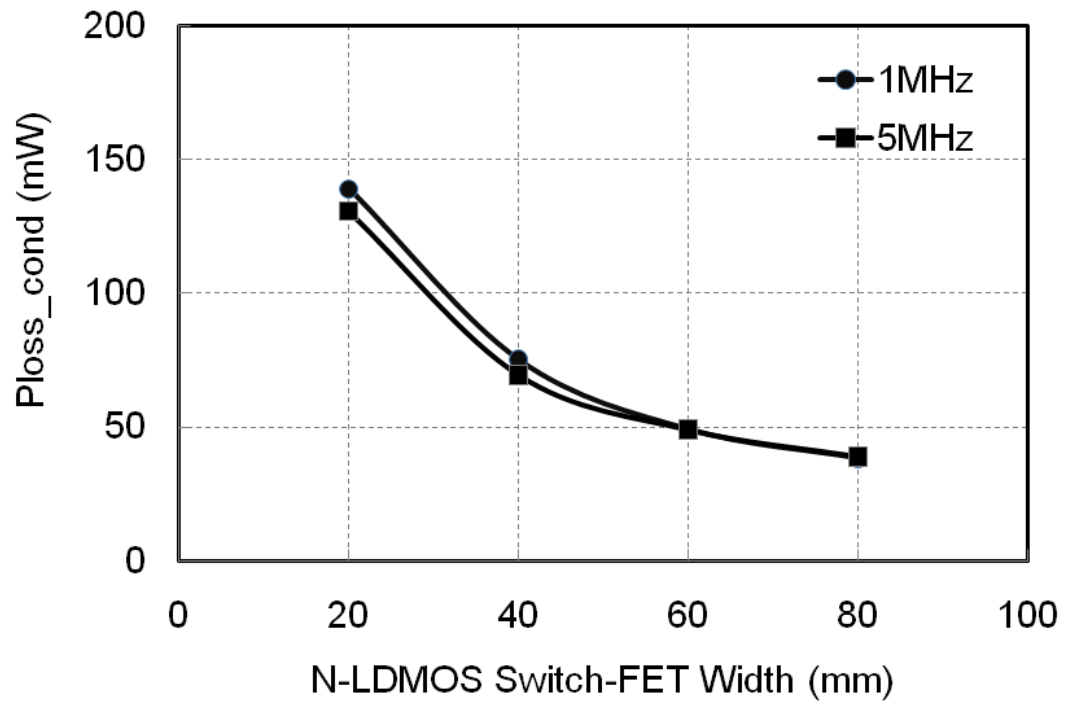


Figure 2.5: Simulation of the conduction loss in the switch-FETs, as a function of device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$.

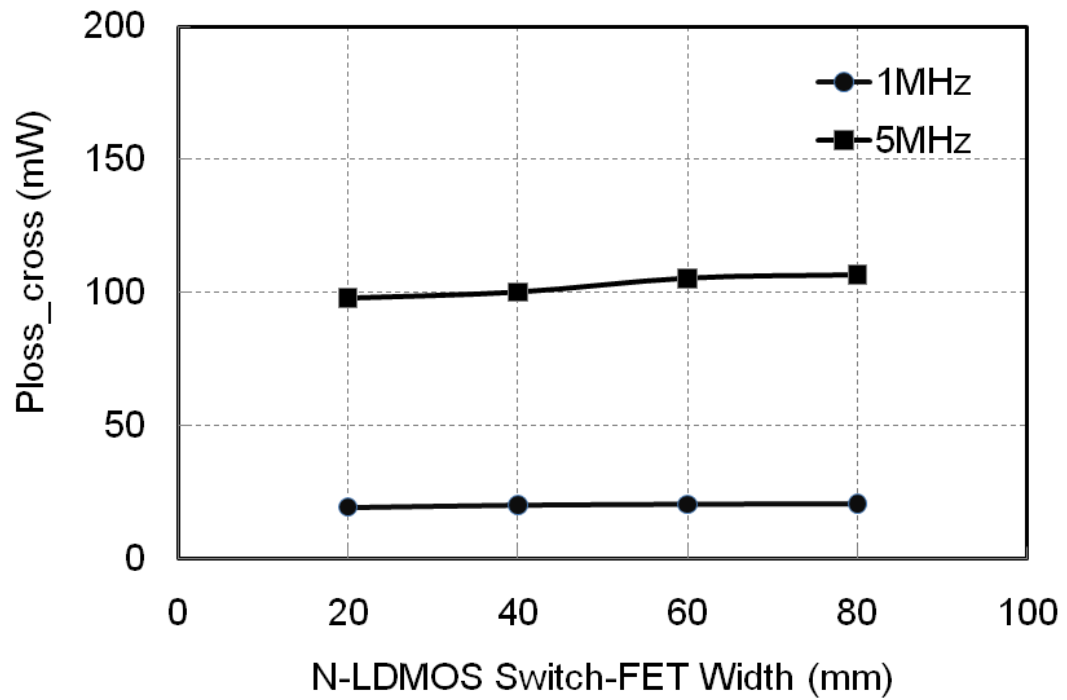


Figure 2.6: Simulation of the crossover loss in the switch-FETs, as a function of device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15 \text{ V}$ and $R_{load} = 10 \text{ } \Omega$.

The crossover loss is given by

$$P_{loss_cross} \cong V_{dmax} \cdot I_{on} \cdot t_{cross} \cdot f_{sw} / \alpha \quad (2.4)$$

where t_{cross} is the crossover time, which is the sum of the turn-on and turn-off time period, α is the commutation parameter (assuming $\alpha=2$ for a first approximation [4]), and f_{sw} is the average switching frequency, respectively. Note that the crossover loss is not dependent on the device width and is proportional to the switching frequency, as shown in Fig. 2.6.

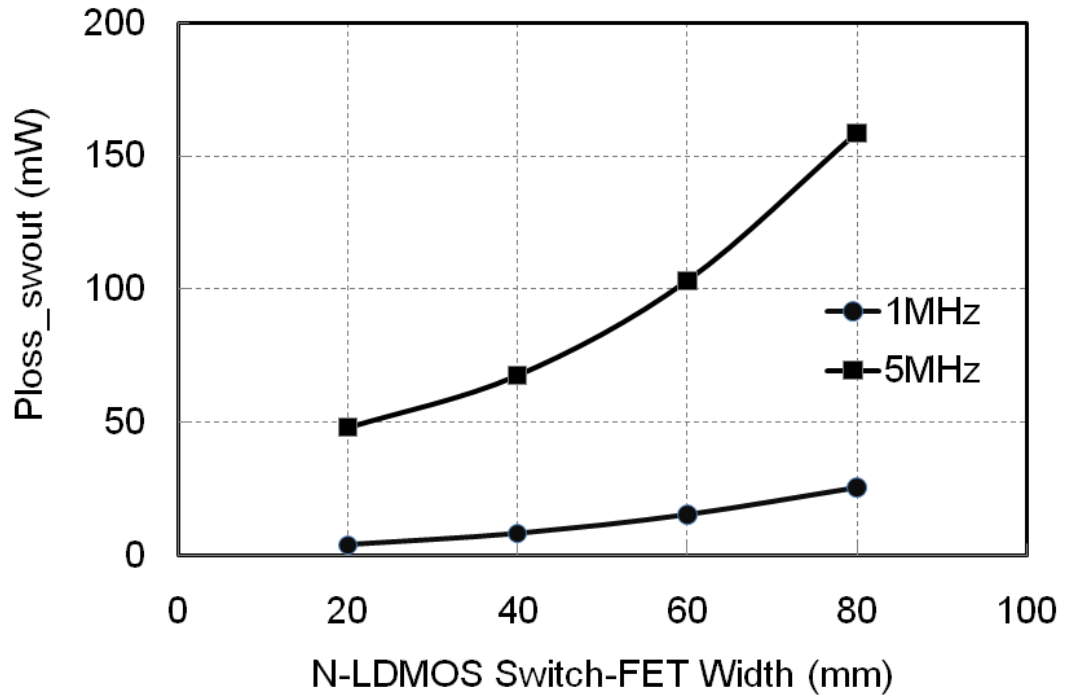


Figure 2.7: Simulation of the dynamic power dissipation at the output node in the switch-FETs, as a function of device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10$ Ω .

The dynamic power dissipation at the switcher output node is given by

$$P_{loss_swout} \cong C_d \cdot V_{dmax}^2 \cdot f_{sw} \quad (2.5)$$

where C_d is the total drain capacitance at the output node. This loss is dependent on the switching frequency and the device width as shown in Fig. 2.7. To minimize the switching power loss, the device is required to have a low input and output capacitance, but this causes a higher conduction loss.

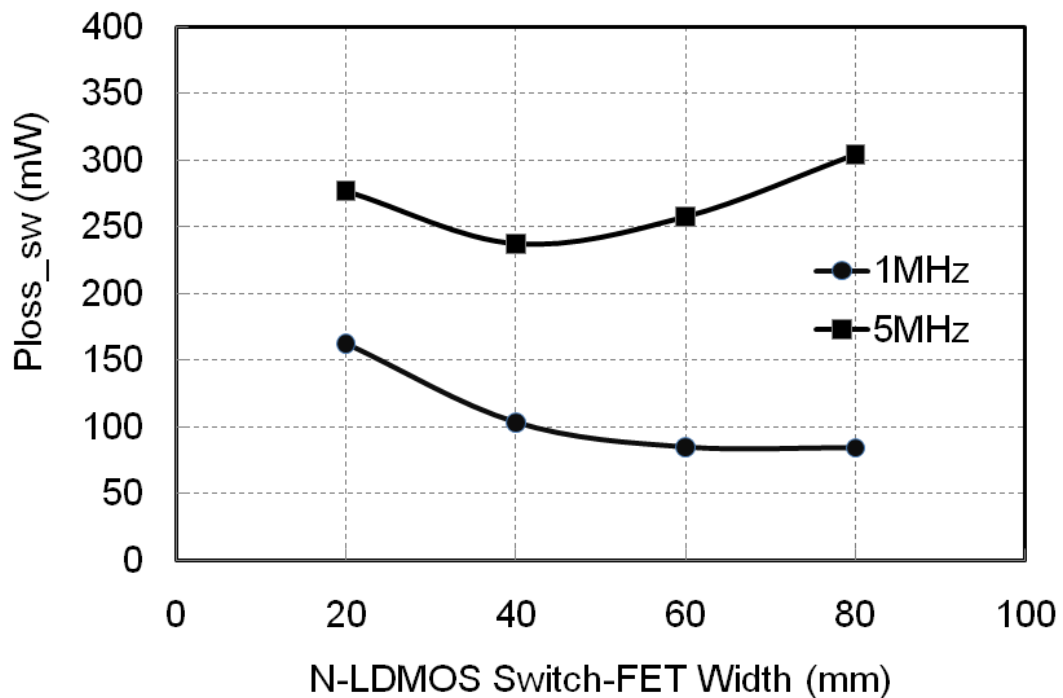


Figure 2.8: Simulation of the total power loss in the switch-FETs, as a function of device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$.

With a low switching frequency, such as 1 MHz, the conduction loss would

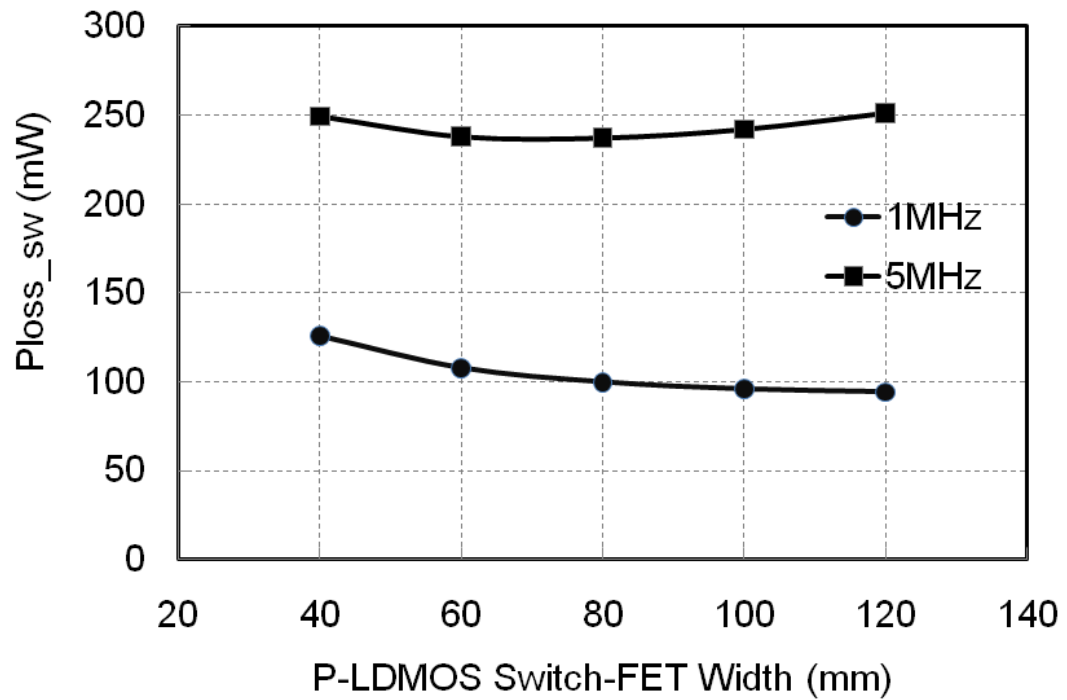


Figure 2.9: Simulation of the total power loss in the switch-FETs as a function of the P-channel LDMOS switch-FET width. The width of the N-channel LDMOS switch-FET was set to 40 mm. An optimum P-channel FET width of 80 mm was used for this design. $V_{DD} = 15 \text{ V}$ and $R_{load} = 10 \text{ } \Omega$.

be dominant because the switching loss is inversely proportional to the switching frequency. In this case, the circuit designer would prefer to increase the device width to reduce the conduction loss as shown in Fig. 2.8. However, a faster switching frequency is required to support a wideband signal and the optimum device width is found in the balance of the conduction loss and the switching loss to improve the overall efficiency. In this design, the width of the switching FET is set to 40 mm and 80 mm for the N-channel and P-channel respectively to minimize a total power loss in the switch-FETs as shown in Fig. 2.8. For a fixed N-channel switching FET width of 40 mm, the P-channel switching FET width is swept to check the power loss in the switch-FETs as shown in Fig. 2.9. The device width ratio between the N-channel and P-channel switching FET has an optimum value when the ratio is 1:2 in this simulation.

To minimize shoot-through currents in the switcher stage, which affects t_{cross} , an input offset voltage control feature is proposed. Without this feature, the gate control signal for N-channel and P-channel LDMOS FETs in the switcher stage are synchronized, and for a short time, both transistors are turned-on. These shoot-through currents cause additional undesirable power loss in the switcher stage. In past work [3], a dead-time control logic was implemented with digital logic gates, and a rail-to-rail voltage swing was required. This kind of circuit cannot be easily used with thin-gate LDMOS FETs for reliability reasons.

In the proposed architecture in Fig. 2.2, the comparator operating at a lower voltages (closer to ground) has a positive input offset voltage and the output signal is non-overlapping with the output signal of the high-side comparator, to minimize shoot-through currents. The comparator output voltage swing level is limited to 3.3 V in order to meet the maximum gate-to-source voltage requirements of the switcher stage. This

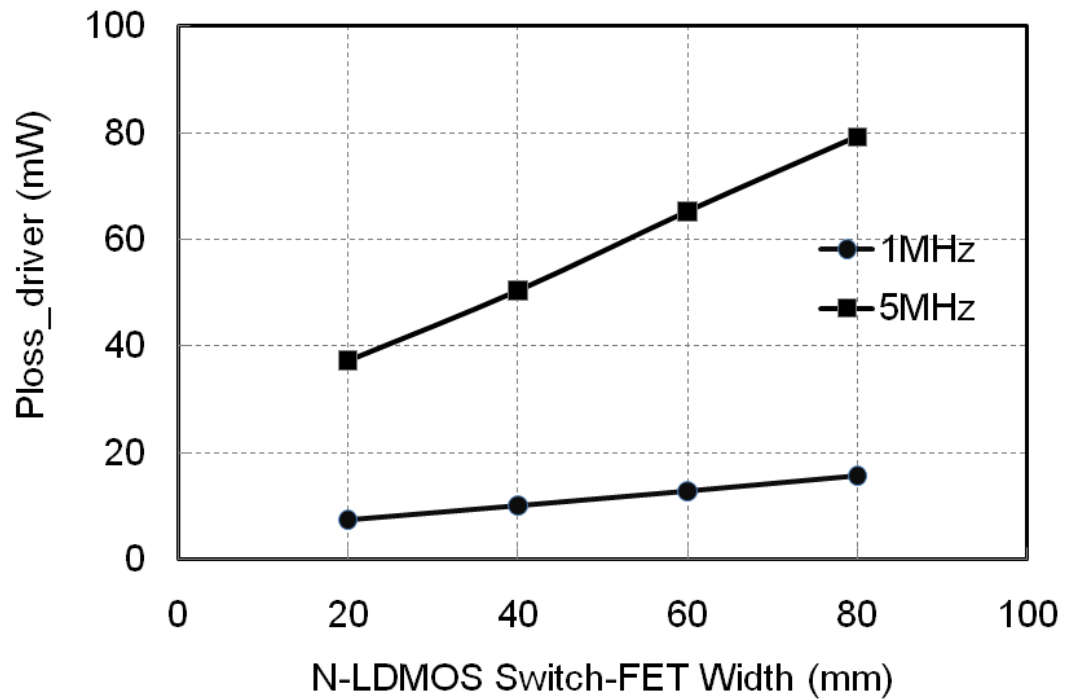


Figure 2.10: Simulation of the power loss in the driver, as a function of switch-FET device width and switching frequencies. The width of the P-channel LDMOS switch-FET was twice that of the N-channel LDMOS switch-FET. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$.

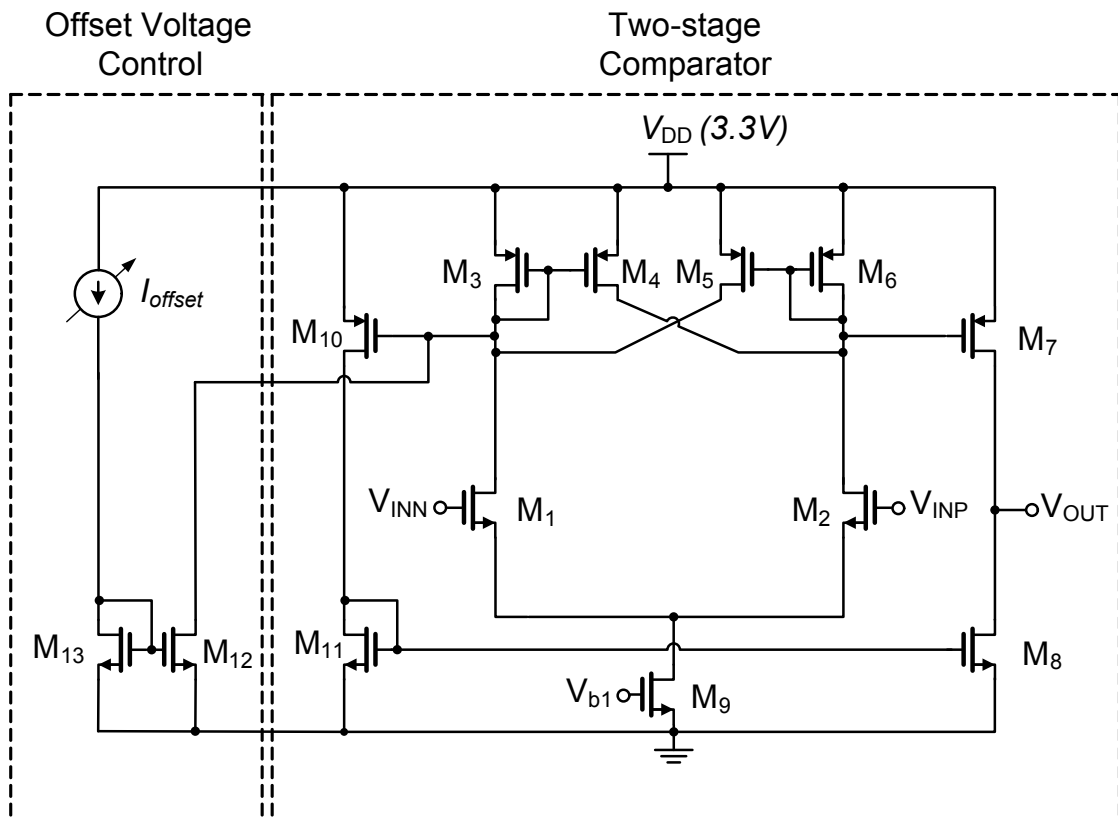


Figure 2.11: CMOS comparator with controllable offset.

topology also helps to reduce the power loss in the driver stage, given by

$$P_{loss_driver} \cong C_g \cdot V_{gs}^2 \cdot f_{sw} \quad (2.6)$$

where C_g is the total gate capacitance at the input node, and V_{gs} is the gate-to-source turn-on voltage, respectively [3]. With the help of the limited input voltage swing, the power loss in the driver stage is a relatively small portion (10 to 20%) compared with other power losses in the switch-FETs. Like the dynamic power dissipation in the switch-FETs in (2.5), the device width of the switch-FETs and the switching frequency affect the driver power loss as shown in Fig. 2.10. So a smaller device width in the switch-FETs is also required to minimize the driver loss, but the increase in the conduction loss should be considered at the same time.

Figure 2.11 shows the schematic of the comparator with the offset voltage controllable by bias current, I_{offset} . In addition, this comparator senses the current by monitoring the input voltage of the class-AB biased final stage of the linear stage. The input stage of the comparator has a differential architecture to increase the voltage swing and reduce common-mode noise effects.

2.3 Measured Envelope Amplifier Results

The proposed envelope amplifier is fabricated using a 0.35- μm BCD process with 4 metal layers [5]. A chip micrograph is shown in Fig. 2.12, and it measures 3.9 mm \times 1.5 mm. The performance of the envelope amplifier was measured with a single carrier WCDMA downlink signal at 2.14 GHz. The peak-to-average power ratio of the signal is 7.7 dB. Figure 2.13 shows the picture of the test fixture of an

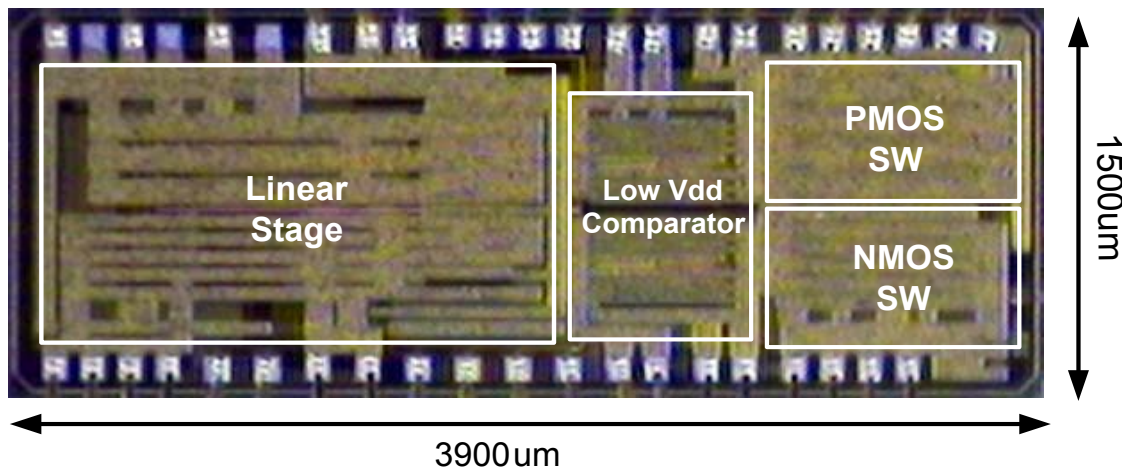


Figure 2.12: Chip micrograph of the BCD envelope amplifier. The chip occupies 5.85 mm² die area including the pads.

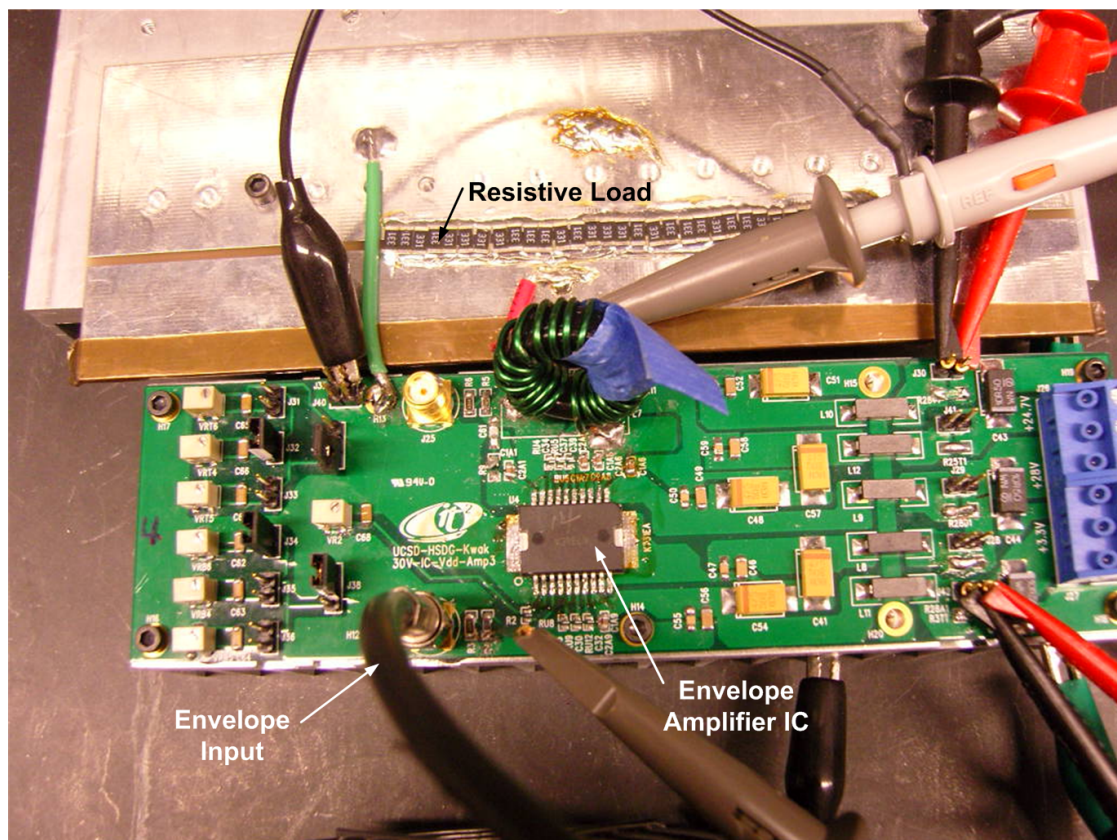


Figure 2.13: Test fixture setup of an envelope amplifier IC with resistive loads.

envelope amplifier IC with resistive loads. The envelope signal is detrouged, so that the minimum drain voltage is 1.4 V, to avoid gain collapse of the RF amplifier at low drain voltages, and amplified in the envelope amplifier. The closed-loop voltage gain of the envelope amplifier was set to 20 dB, with a 15 V supply voltage.

Figure 2.14 shows the measured time-domain input and output of the envelope amplifier in conjunction with the switcher stage output. The output voltage of the envelope amplifier is ten times the input voltage and the switching voltage is rail-to-rail. The average switching frequency was 2 MHz for a single carrier WCDMA signal (4 MHz bandwidth). To check the noise performance of the proposed envelope amplifier, the measured spectrum at the output voltage with a 10 Ω resistive load is shown in Fig. 2.15. The noise at the WCDMA receive band 180 MHz offset was measured to check the indirect effects of the receive band noise in a WCDMA system. With the envelope signal supplied by a 14 bit DAC, the noise floor at the output of the DAC at a 180 MHz offset was measured to be -136 dBc/Hz relative to the dc output. At the output of the envelope amplifier, there is an upward boost in the noise at a 180 MHz offset of 3.4 dB, which is caused by an envelope amplifier, and the measured noise at the 180 MHz offset is -132.6 dBc/Hz.

Figure 2.16 shows the measured efficiency of the envelope amplifier as a function of the signal bandwidth and output power. As the signal frequency of the input single-tone sine waveform is increased from 1 MHz to 5 MHz the overall efficiency drops because of the increased switching loss. The switching loss is proportional to the switching frequency, and the simulated total switcher loss in the switch-FETs at 5 MHz is 2.5 times higher than that of the 1 MHz case as shown in Fig. 2.8. If desired, the switcher stage efficiency can be improved at wider bandwidths by using a multi-switcher

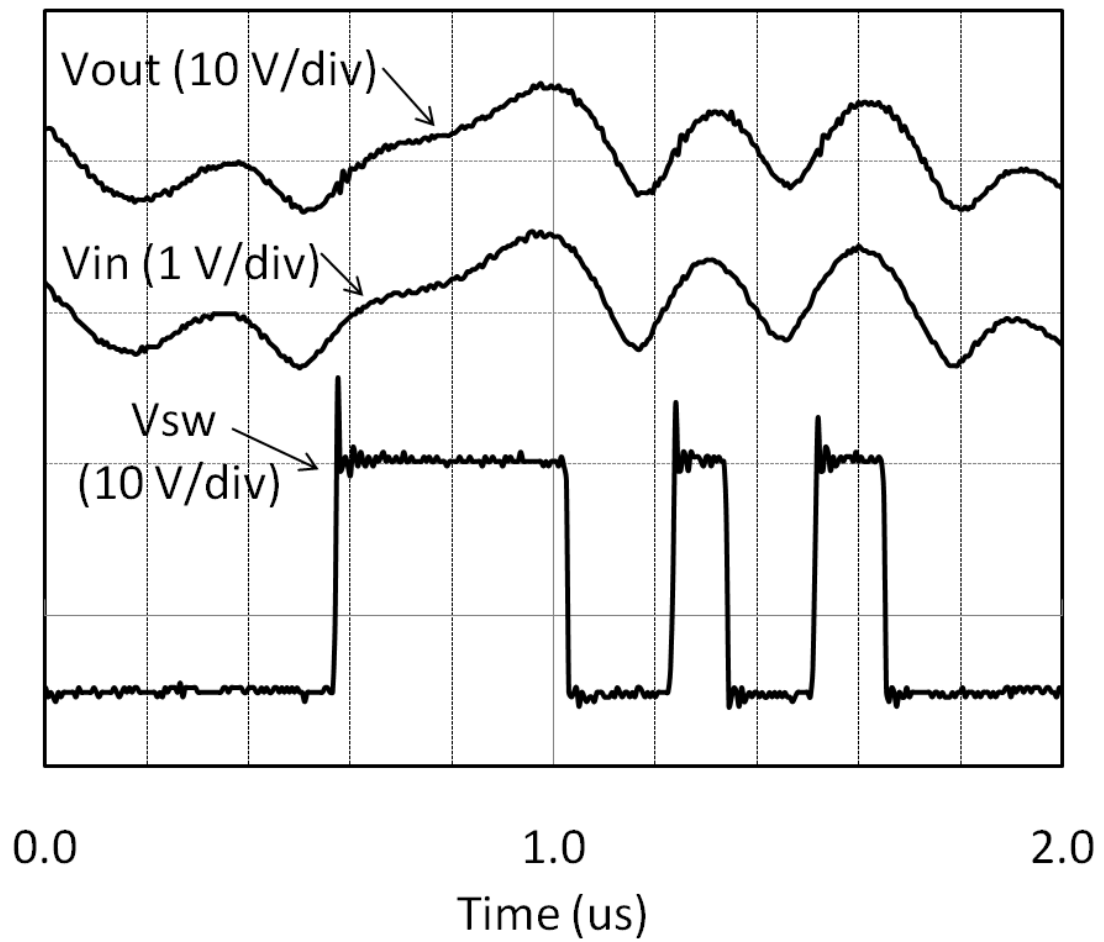


Figure 2.14: Measured envelope amplifier input, output voltage, and switcher stage output voltage. The envelope input signal is a 7.7dB PAR 4MHz WCDMA signal. The closed-loop gain is 20 dB with 15 V supply voltage. (200 ns/div)

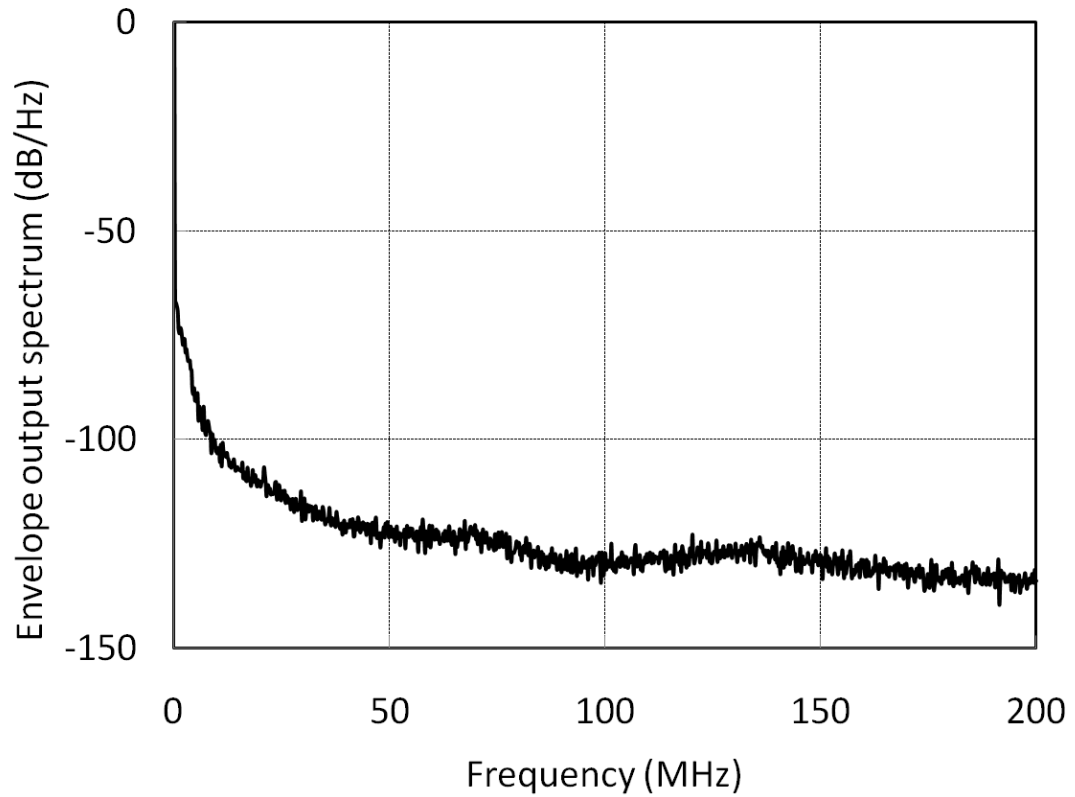


Figure 2.15: Measured baseband envelope amplifier output spectrum for a 4 MHz WCDMA signal. The noise is - 132.6 dBc/Hz at a 180 MHz offset. $V_{DD} = 15$ V and $R_{load} = 10 \Omega$.

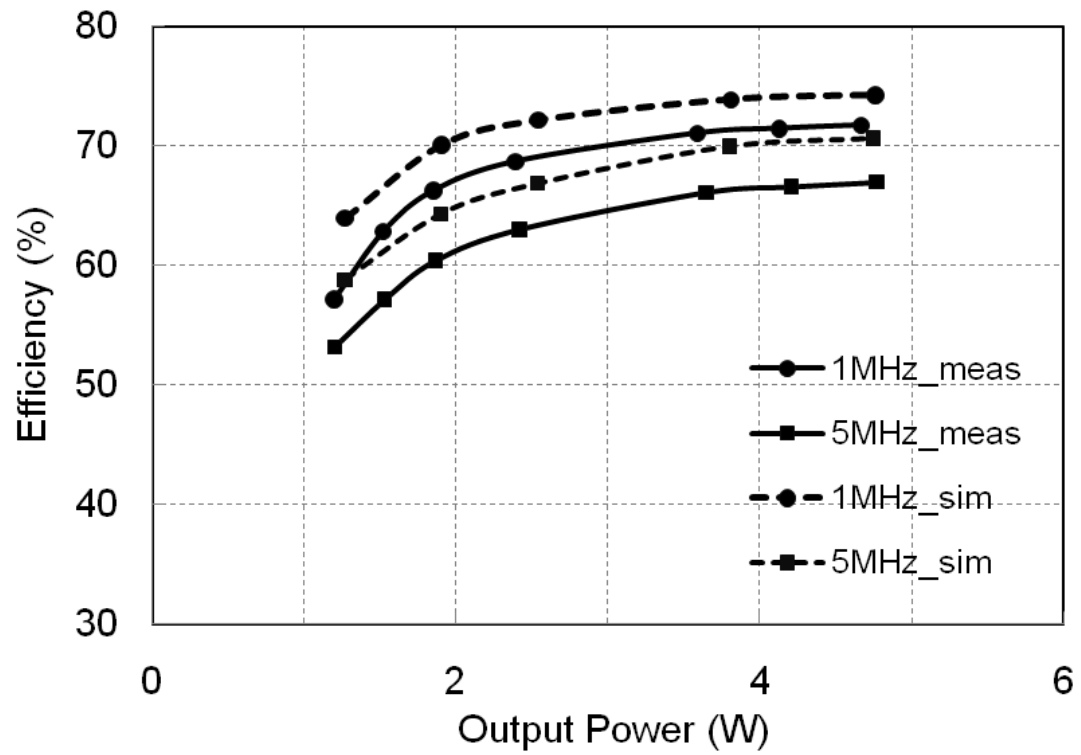


Figure 2.16: Comparison of measured and simulated envelope amplifier efficiency as function of signal bandwidth and output power. Sine wave input, $V_{DD} = 15$ V and $R_{load} = 7.7$ to 30Ω .

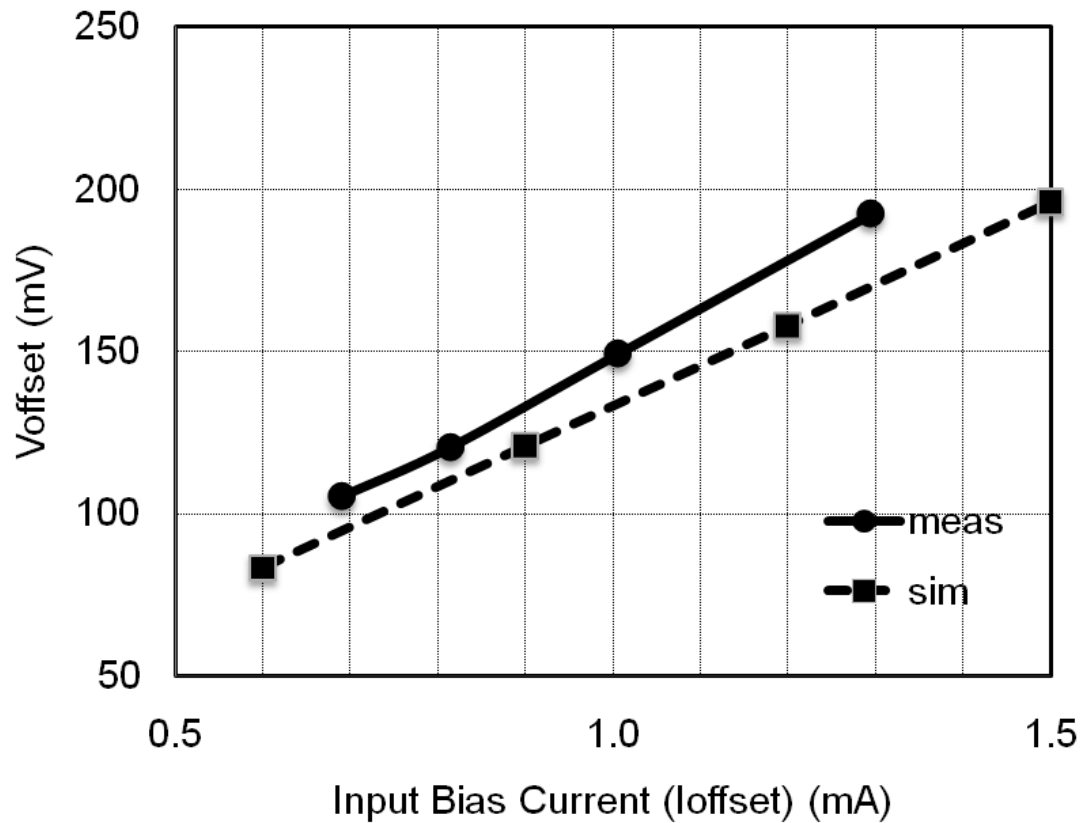


Figure 2.17: Comparison of measured and simulated comparator offset voltage versus input bias current.

architecture [54].

To minimize the shoot-through currents, a controllable offset voltage was applied to the low-side comparator operating at a lower voltage in Fig. 3.3. This offset voltage is controllable with an input bias current, I_{offset} as shown in Fig. 2.17 and linearly increased according to this bias current. Figure 2.18 plots the transient response of the low-side comparator with a positive input offset voltage of 120 mV. The value of the offset voltage determines the non-overlapping time between the output signal

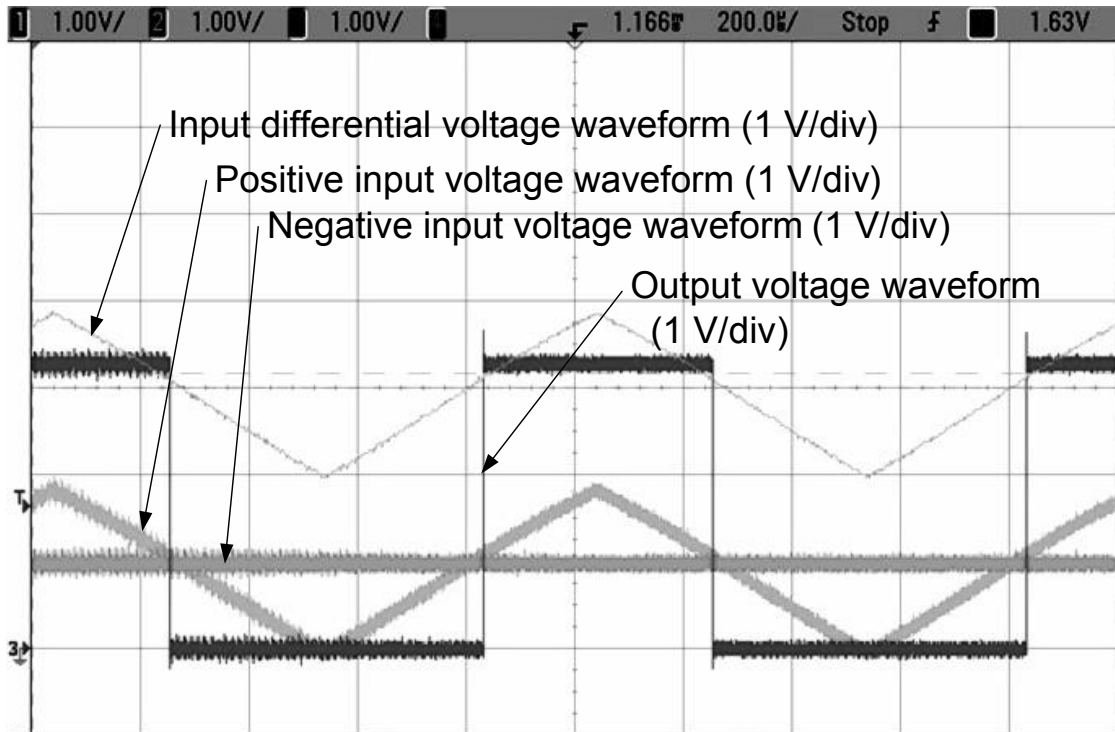


Figure 2.18: Measured comparator positive input, negative input, differential input voltages, and output voltage with offset voltage of 120 mV. Differential input voltage is a symmetric triangle wave with period 1 ms and varying between -1 and 1 V. (200 μs/div)

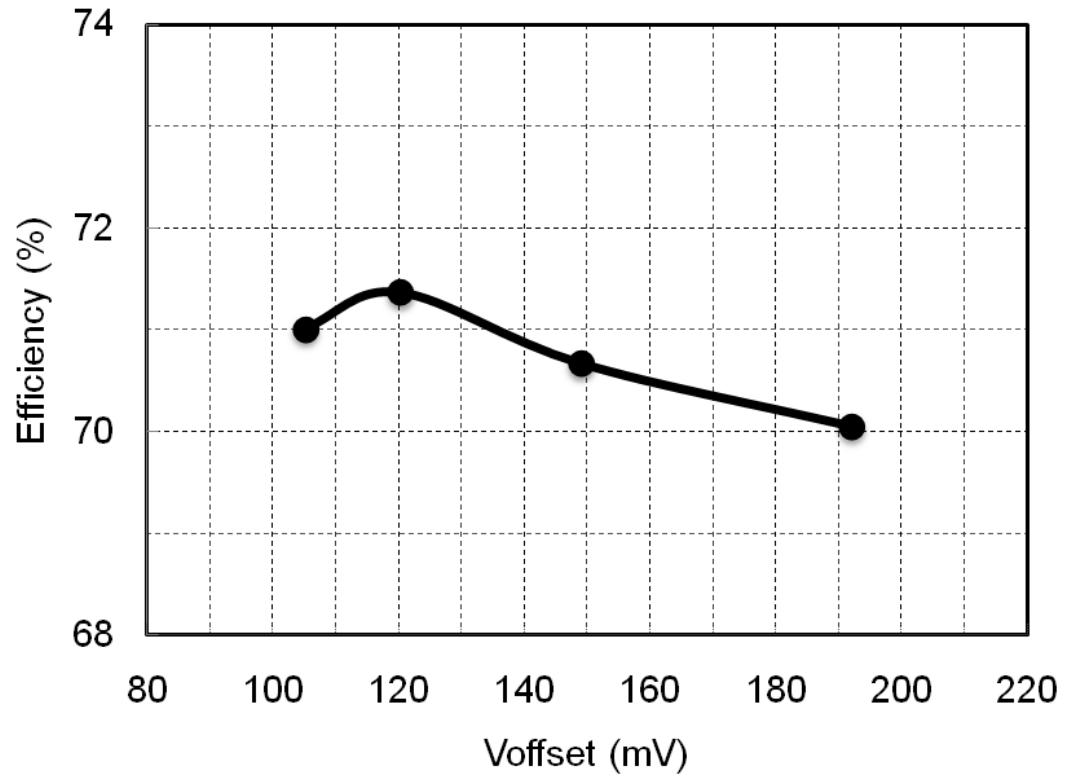


Figure 2.19: Measured envelope amplifier efficiency with a 7.7dB PAR 4MHz WCDMA signal and a 10 Ω resistive load, as a function of the comparator offset voltage.

Table 2.1: Envelope Amplifier Performance Summary in a WCDMA ET System

| Parameter | Values |
|-----------------------------|----------------------------|
| Supply Voltage | 15 V |
| Output Voltage | 1.4 V to 14 V |
| Output Current | 0.59 A (rms) 1.37 A (peak) |
| Bandwidth | 4 MHz |
| Output Power | 3.5 W (rms) 19.2 W (peak) |
| Total Amp Efficiency | 72% |
| Average Switching Frequency | 2 MHz |

of the low-side comparator and that of the high-side comparator. Without this non-overlapping time, there would be an unwanted power loss due to the shoot-through currents when both switch-FETs are turned-on for a short time. However, if there is excess non-overlapping time, both switch-FETs are turned-off simultaneously and the body diode of the N-channel switch-FET will contribute to an additional power loss by turning on and conducting current. The efficiency of the envelope amplifier with a 10 Ω resistive load was measured with a WCDMA signal to find an optimum offset voltage of the comparator as shown in Fig. 2.19. The optimum offset voltage was determined to be 120 mV so as to avoid the shoot-through currents in the switcher stage with margin.

Table 2.1 shows the performance summary of this envelope amplifier IC in a WCDMA ET system. The measured average efficiency of the high voltage envelope amplifier was 72% with 7.7 dB PAR 4 MHz WCDMA signal.

2.4 Conclusion

This Chapter presented a high-performance high-voltage BCD monolithic envelope amplifier design for micro base station power amplifiers. The proposed envelope amplifier is fabricated using a 0.35- μm BCD process with 4 metal layers. The measured average efficiency of the high voltage envelope amplifier was 72% with 7.7 dB PAR 4 MHz WCDMA signal. The results make this architecture an attractive candidate for monolithic integration of a high-voltage envelope amplifier for micro base station RF power amplifier applications. The complete envelope tracking power amplifier system design with this high voltage envelope amplifier, is presented in the next Chapter.

2.5 Acknowledgment

The author would like to thank Giuseppe Meola in STMicroelectronics for fabricating the chip, Sandro Lanfranco in Nokia Siemens Networks for supporting this work, and Cuong Vu's assistance on measurements at UCSD.

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- M. Kwak, D. Kimball, C. Presti, A. Scuderi, C. Santagati, J. Yan, P. M. Asbeck, and L. E. Larson, "Design of wideband high-voltage high-efficiency BiCMOS envelope amplifier for Micro-base station RF power amplifiers," submitted to *IEEE Transactions of Microwave Theory and Techniques*, 2011.

The contributions from the co-authors are appreciated. The dissertation author was the primary researcher and the first author listed in these publications.

Chapter 3

Wideband High Efficiency Envelope Tracking Power Amplifiers for Micro-Base Station Applications

3.1 Introduction

The recent increase of mobile data usage and the emergence of new applications, such as mobile web browsing and video streaming content, have motivated research on the extension of cellular network coverage without increasing the density of traditional macro base stations [59]. By installing smaller base stations, such as micro, pico and femto cells, to complement the conventional macro base stations, coverage can be significantly improved. Table 3.1 compares the categories of these new smaller base stations to the traditional macro base station [7]. The micro base station concept is ideal for operators needing a cost effective solution for high data rates to end users, without over-building the traditional macro base station network.

Table 3.1: Comparison of Base Stations [7]

| | Macro | Micro | Pico | Femto |
|-----------------|--------------|-----------------|--------|-----------------|
| Application | Outdoor cell | Medium coverage | Campus | Indoor resident |
| Range | Upto 5km | Upto 3km | 1km | 50m |
| RF output power | 45dBm | 36dBm | 30dBm | 15dBm |
| Mobility | High | High | High | None |
| Cost | High | Med High | Med | Low |

This chapter will describe the design considerations and implementation of a monolithic BCD wideband high efficiency envelope amplifier, and its application to an envelope tracking PA for micro base station applications. This chapter is organized as follows. Section 3.2 presents the envelope tracking system design consideration and the comparison with a conventional architecture. In Section 3.3, experimental results are shown for WCDMA signals and a conclusion is given in Section 3.4.

3.2 Envelope Tracking Amplifier System Design

The envelope tracking (ET) system shown in Fig. 2.1 improves the efficiency of a power amplifier (PA) by modulating the power supply to a nearly saturated RF PA stage. As compared with a constant DC supply voltage, the thermal dissipation is dramatically reduced and the transistor temperature is maintained at a low value. Another benefit of the envelope tracking technique, compared with other techniques such as the Doherty or LINC, is that the efficiency enhancement mechanism is totally decoupled from the RF matching [9]. The overall efficiency of the envelope tracking RF power amplifier is approximately

$$\eta_{ET} \cong \eta_{RF} \cdot \eta_{env} \quad (3.1)$$

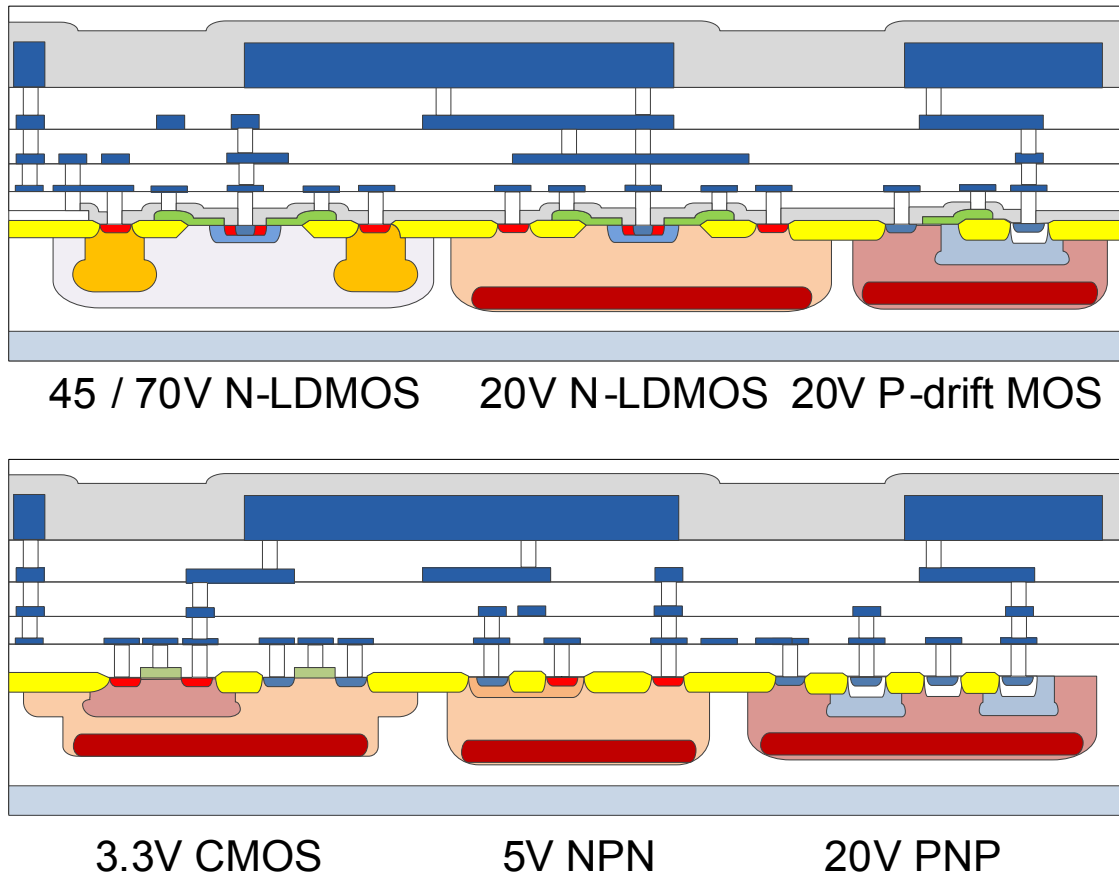


Figure 3.1: BCD6 process cross section thru the fourth-layer metal [5].

where η_{RF} and η_{env} are the efficiencies of the RF amplifier and the envelope amplifier, respectively. From (3.1), it is important to optimize the efficiencies of both the envelope amplifier and the RF amplifier to maximize the overall efficiency.

3.2.1 High Voltage Envelope Amplifier Design Considerations

The envelope amplifier was fabricated in STMicroelectronics' 0.35- μm BCD process, which allows mixing different structures such as CMOS for digital circuits and DMOS structures for power and high voltage applications [5]. Figure 3.1 shows a cross-section of the BCD6 process, and the DMOS transistors are fully compatible with the existing 0.35- μm CMOS process. The power MOS devices used in the design are 30 V N-channel and P-channel LDMOS FETs showing $R_{on} = 29 \text{ m}\Omega \times \text{mm}^2$ and $49 \text{ m}\Omega \times \text{mm}^2$ respectively at $|V_{GS}| = 3.3 \text{ V}$.

The conventional envelope amplifier shown in Fig. 3.2 comprises a linear stage to provide a wideband, but less efficient, voltage source in parallel with a switching stage, which provides a narrowband but efficient dynamic current source [6]. The current is supplied to the drain of the RF PA from both the linear stage and the switching stage through a current feedback network, which senses the current flowing from the linear stage and turns on and off the buck converting switcher. The linear stage provides the difference between the desired output current and the current provided by the switching stage, such that the overall difference current is minimized [6].

In Fig. 3.2, the current sensing circuitry needs to accommodate a rail-to-rail input voltage swing. For micro base-station applications, a high supply voltage, such as 15 V, is required to generate the average RF output power of 2 to 4 W. To meet this high supply voltage requirement, 0.35- μm 30 V N-channel and P-channel LDMOS FETs were used to implement the linear stage and switching FETs in the switcher stage. In addition,

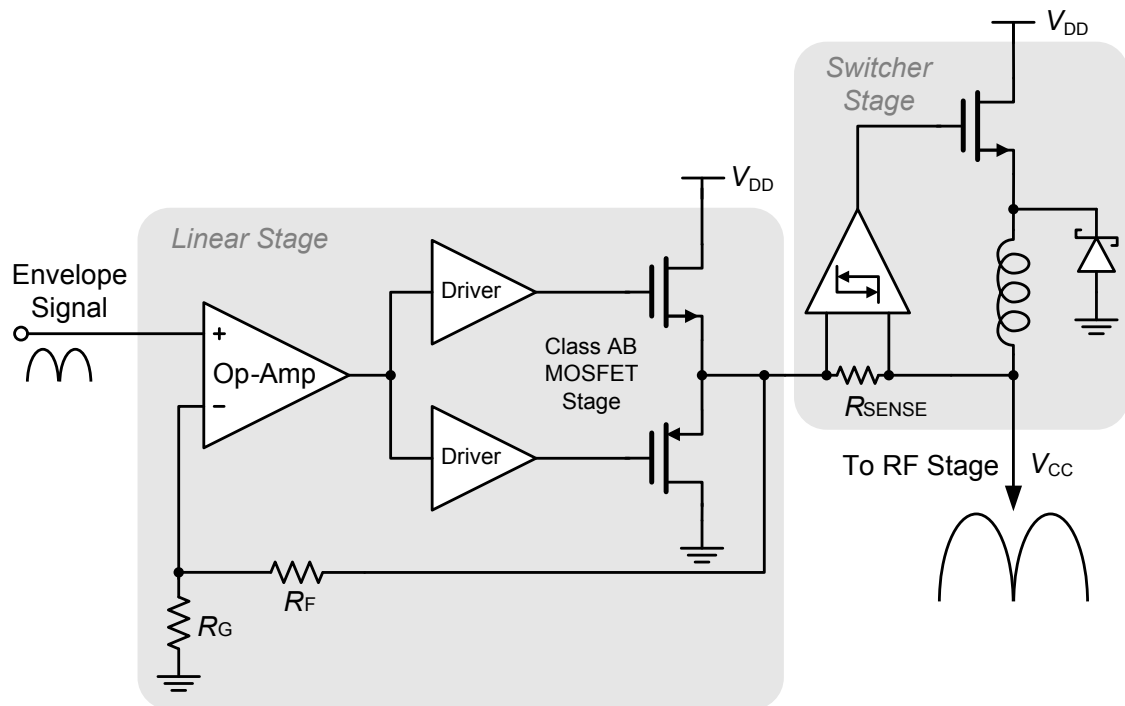


Figure 3.2: Conventional linear-assisted hybrid envelope amplifier for envelope tracking applications [6].

the maximum allowable magnitude of V_{GS} of these LDMOS devices is limited to 3.3 V to protect the gate oxide. Hence, the conventional current sensing circuitry, which is subject to rail-to-rail voltage swings, cannot be used with these LDMOS devices.

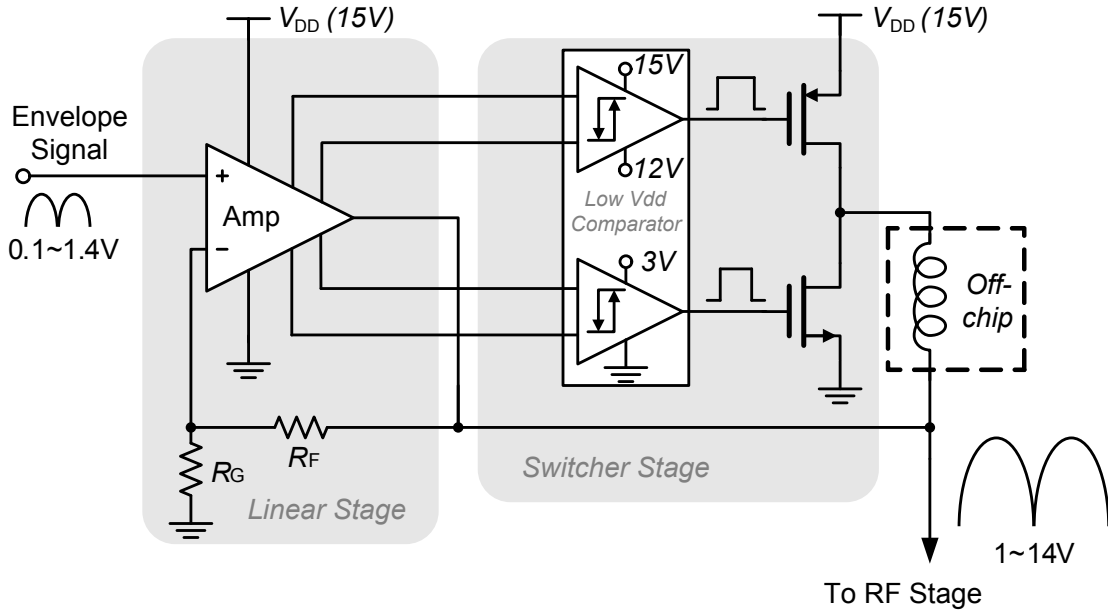


Figure 3.3: Proposed monolithic envelope amplifier with improved operation at high V_{DD} .

The proposed envelope amplifier block diagram, as shown in Fig. 3.3, employs dual current sensing comparators, which require limited voltage swings. This architecture has several advantages. First, the supply voltage and output voltage swing of each comparator is set to 3.3 V to maintain the reliability of the LDMOS devices. Second, dynamic power consumption in the low V_{DD} comparator is reduced because the dynamic power loss is proportional to the square of the supply voltage. Third, a current sensing resistor is not needed and the required input dynamic range in the comparator is not rail-to-rail. Finally, common-mode noise is reduced due to the differential input signal.

3.2.2 RF Power Amplifier Design Considerations

The RF transistors were fabricated using a separate GaN-on-silicon HFET process [60]. GaN HFETs offer efficiency, bandwidth, and power advantages compared to Si LDMOS FETs. The high charge density combined with the ability to operate HFETs at high voltages results in devices that have approximately ten times the power density of silicon and wider bandwidths due to the resulting higher input and output impedances [60]. However, the price gap between GaN HFETs and Si LDMOS power transistors is still significant because the majority of GaN HFETs are produced on silicon carbide substrates [60]. GaN HFETs grown on a silicon substrate, which were used in this design, potentially offer substantial cost savings by combining the high performance attributes of GaN HFETs with the economies of Si wafer substrates. In addition, devices with low values of R_{on} are preferred in the envelope tracking system for optimum efficiency [6]. GaN HFETs have intrinsic benefits of lower output capacitance and on-resistance compared to Si LDMOS FETs.

If a constant drain bias is used (e.g, $V_{DD} = 15$ V), the RF power-added efficiency rapidly degrades as the output power is backed-off. The maximum efficiency can be achieved at the peak output power and cannot be maintained over a wide range. In our design, the drain supply voltage is dynamically varied from 1 to 14 V with output power level, so as to maintain high efficiency at most times. In this approach, the envelope signal does not have to be very accurate and the drain supply voltage could be tracked for the envelope signal with several dB margin [9]. The GaN HFET was biased in class-AB mode.

3.3 Measured Envelope Tracking Power Amplifier Results

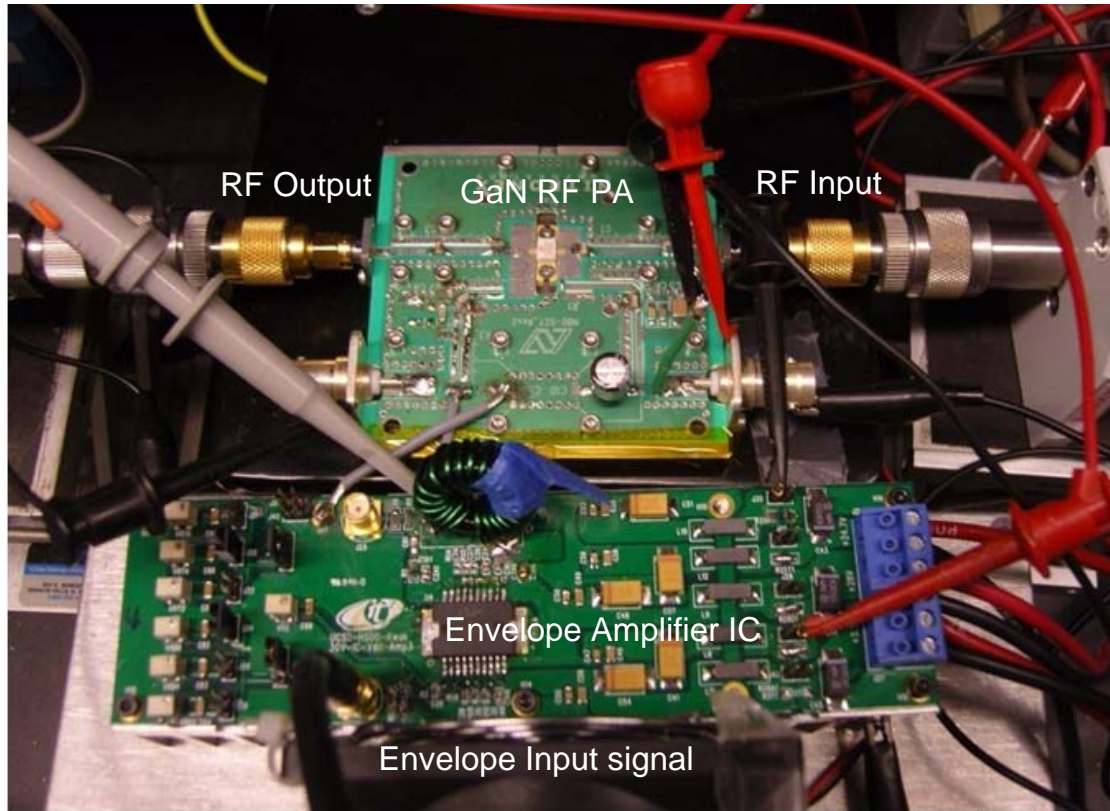
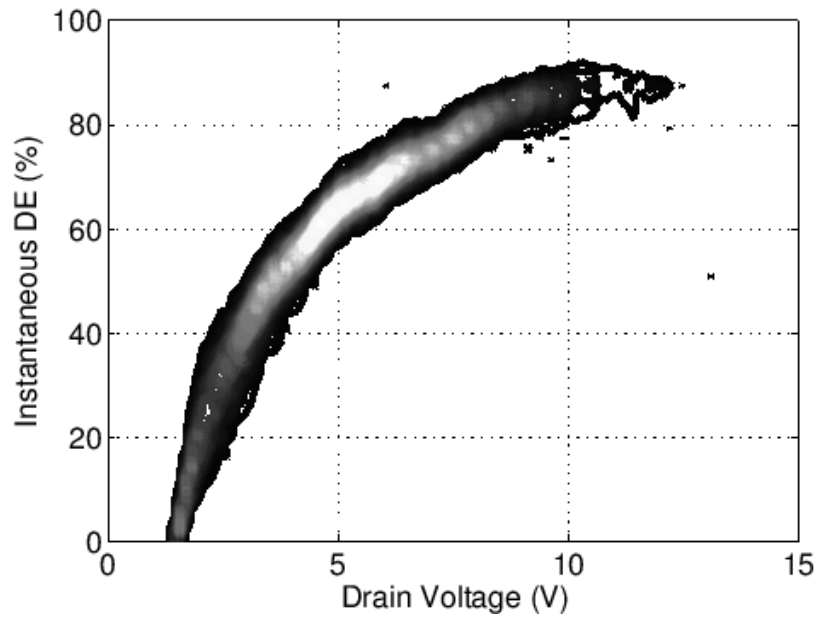


Figure 3.4: Test fixture setup with envelope amplifier IC and RF power amplifier for the envelope tracking system.

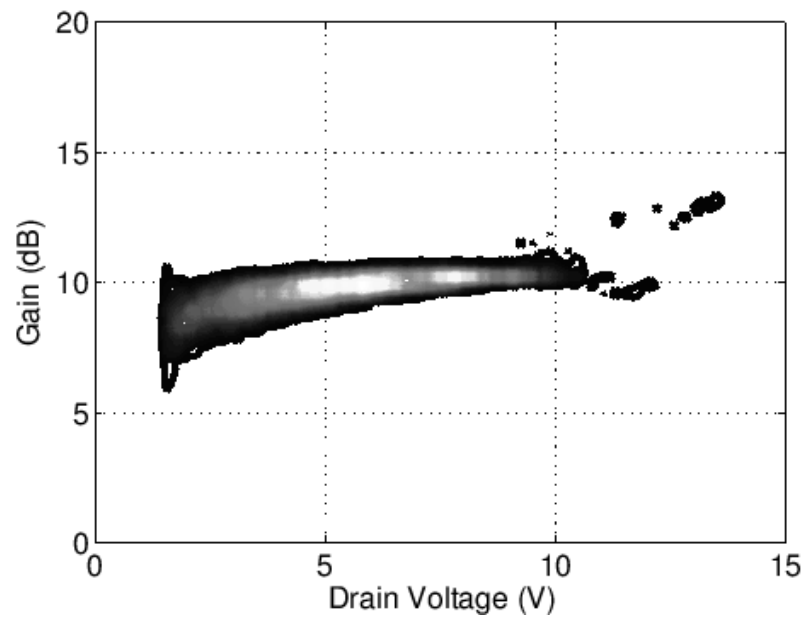
The performance of the envelope tracking power amplifier was measured with a single carrier WCDMA downlink signal at 2.14 GHz. The peak-to-average power ratio of the signal is 7.7 dB. Input signals such as the envelope and RF signals are generated in the digital domain and transformed to analog signals by the Digital-to-Analog Converters (DACs) as shown in Fig. 2.1. The envelope signal is detrouged, so that the minimum drain voltage is 1.4 V, to avoid gain collapse of the RF amplifier at low drain voltages, and amplified in the envelope amplifier. The time delay difference between the

envelope signal path and the RF signal path is adjusted to minimize the resulting distortion [3]. A GaN HFET-based RF PA was used with the high-voltage envelope amplifier for the complete envelope tracking PA. The gate of the GaN HFET was biased at -1.4 V and the drain supply voltage was modulated by the envelope amplifier from 1.4 V to 14.0 V. Figure 3.4 shows the picture of the test fixture with envelope amplifier and RF power amplifier.

The instantaneous values of $V_{drain}(t)$, $I_{drain}(t)$, $V_{in}(t)$, and $V_{out}(t)$ are measured utilizing a high-speed sampling oscilloscope to analyze the characteristics of the RF stage and the envelope amplifier respectively. Figure 3.5 shows experimental results of the drain efficiency, gain, envelope loadline and output power. The instantaneous RF PA drain efficiency is shown in Fig. 3.5(a), and reaches a maximum above 80% at the peak envelope voltage. Around the RMS voltage of the envelope signal (5.8 V) the drain efficiency of the RF stage was above 60% and the average drain efficiency of the RF stage was calculated to be 71%. The measured overall drain efficiency of the envelope tracking RF power amplifier is 51% under these signal conditions and the high voltage envelope amplifier shows an average efficiency of 72% by (3.1). The measured gain of the RF stage and the envelope load line is approximately 10 dB and 10 Ω as shown in Fig. 3.5(b) and Fig. 3.5(c), respectively. Figure 3.6 shows the measured drain efficiency of the RF stage with a WCDMA signal probability density function. With a constant supply voltage, the RF PA efficiency will drop dramatically as the output power is backed-off. However, in the envelope tracking RF power amplifier system, the optimal RF PA efficiency follows the envelope tracking trajectory and high efficiency above 60% can be maintained over a 10 dB range of output power as shown in Fig. 3.6.

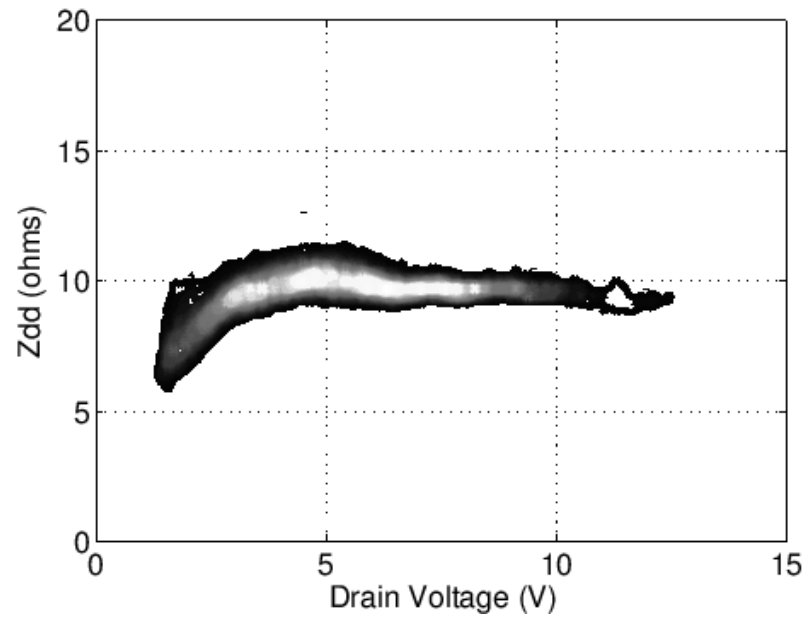


(a)

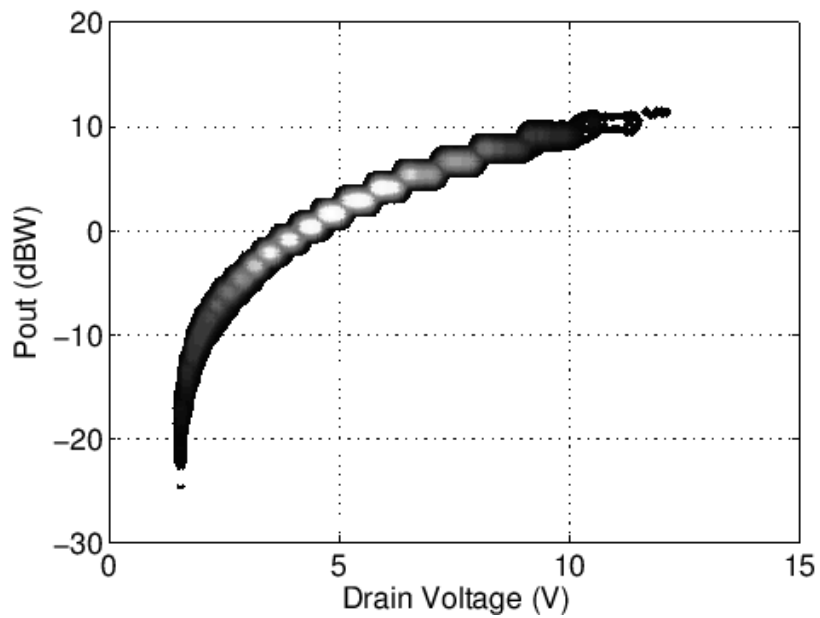


(b)

Figure 3.5: Measured results on GaN HFET power amplifier with WCDMA input at 2.14 GHz (a) instantaneous drain efficiency versus drain voltage, (b) instantaneous gain versus drain voltage, (c) instantaneous envelope loadline (V_{env}/I_{env}) versus drain voltage, (d) instantaneous output power versus drain voltage.



(c)



(d)

Figure 3.5: Measured results on GaN HFET power amplifier with WCDMA input at 2.14 GHz (a) instantaneous drain efficiency versus drain voltage, (b) instantaneous gain versus drain voltage, (c) instantaneous envelope loadline (V_{env}/I_{env}) versus drain voltage, (d) instantaneous output power versus drain voltage (continued).

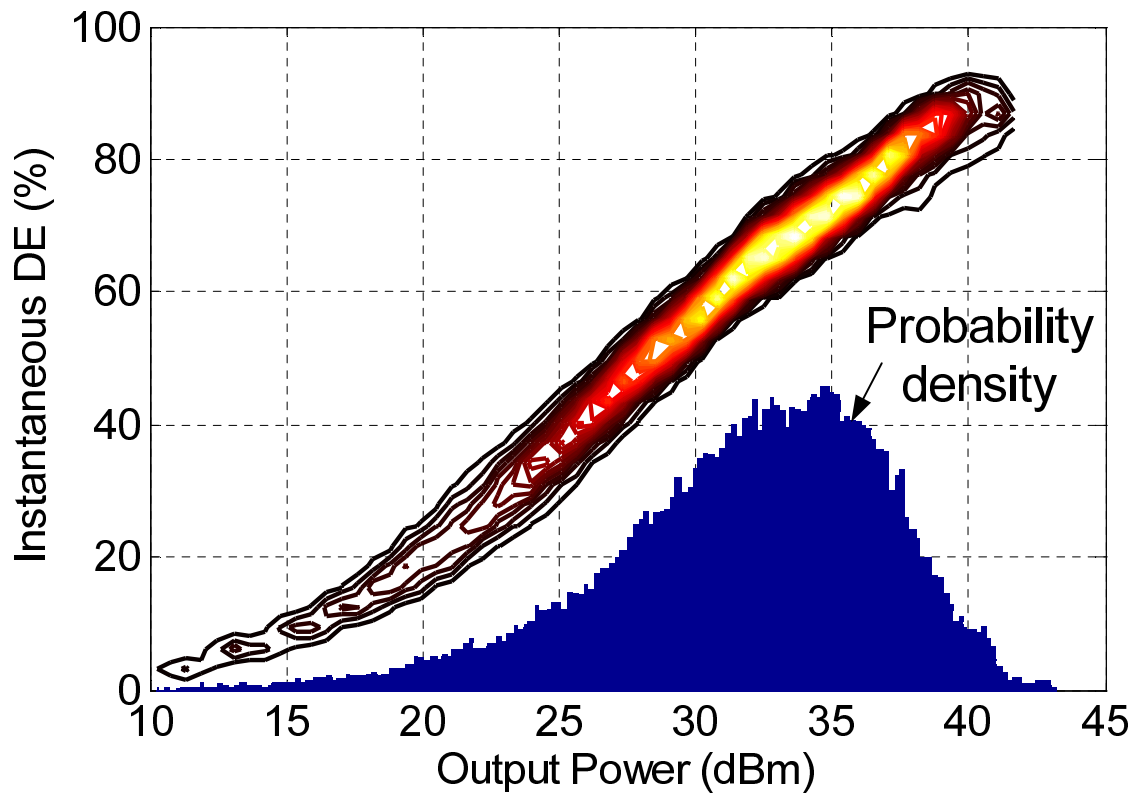


Figure 3.6: Measured drain efficiency of the RF stage along with a WCDMA signal probability density function.

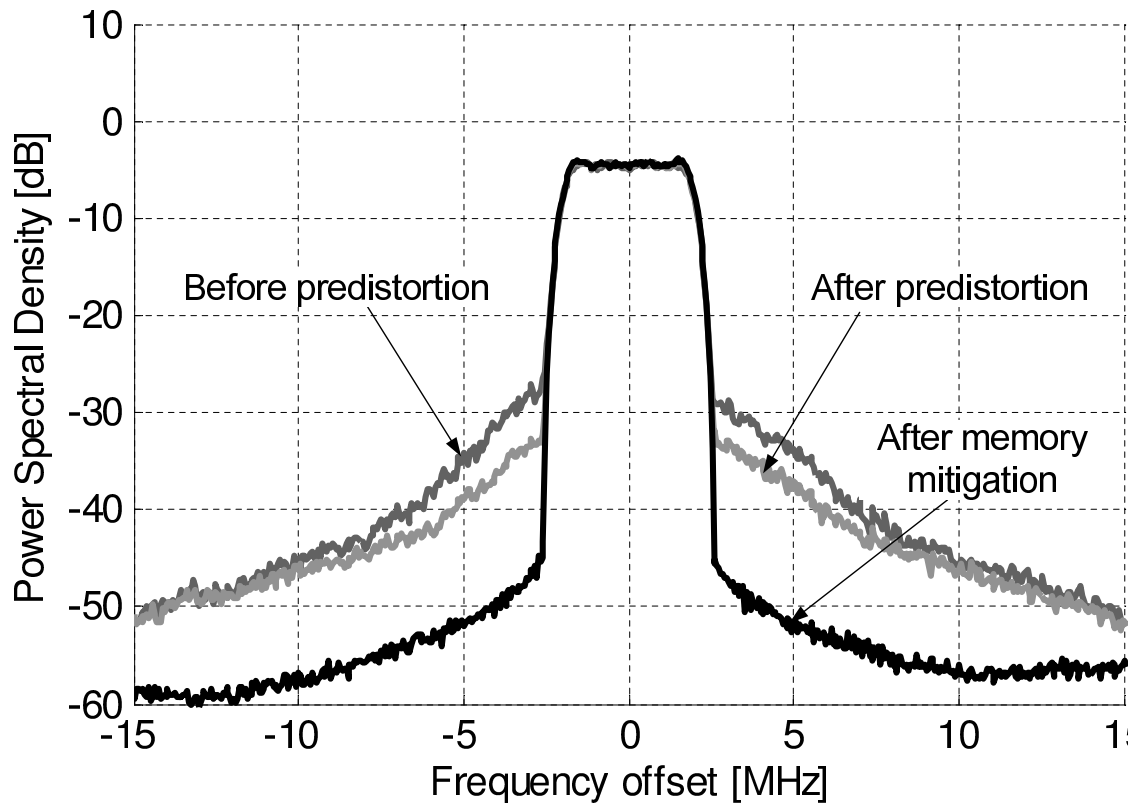


Figure 3.7: Normalized measured output power spectral density of single carrier WCDMA signal with 7.7-dB PAR before predistortion, after pre-distortion, and after memory-effect mitigation DPD. ($f_{CENTER} = 2.14$ GHz, $P_{OUT} = 2.5$ W)

Figure 3.7 shows a comparison of the normalized output signal spectrum before and after memory-effect mitigation digital pre-distortion (DPD). We applied a memory-effect mitigation algorithm [49] to improve the memory effects associated with this device. The ACLR performance is improved by 20 and 13 dB at the 5 and 10 MHz offset, respectively, and the specifications are met with margin through memory-effect mitigation DPD. The ACLR specifications for WCDMA radio base station output signals are -45 dBc at the 5 MHz offset and -50 dBc at the 10 MHz offset. Figure 3.8 shows the measured AM-AM and AM-PM characteristics before and after memory-effect mitigation DPD. The scatter of the plotted data indicates a perturbation to the instantaneous gain caused by deterministic memory effects [6] and these memory effects are compensated after memory-effect mitigation DPD.

Table 3.2: Performance Summary of Envelope Tracking Power Amplifier with WCDMA Signal

| | Gain | Po | DE | PAE | NRMSE | ACLR1 | ACLR2 |
|------------------|------|-----|-----|-----|-------|-------|-------|
| Unit | [dB] | [W] | [%] | [%] | [%] | [dBc] | [dBc] |
| Before DPD | 10.2 | 2.2 | 49 | 47 | 23.5 | -29 | -40 |
| After ML DPD | 10.2 | 2.3 | 51 | 49 | 9.4 | -32 | -41 |
| After Memory DPD | 10.2 | 2.5 | 51 | 49 | 1.2 | -49 | -53 |

DE : drain efficiency, ML DPD : Memoryless digital pre-distortion, WCDMA specifications : ACLR1 < -45 dBc, ACLR2 < -50 dBc, ACLR1 at 5 MHz offset, ACLR2 at 10 MHz offset for WCDMA.

The average measured drain efficiency of the power amplifier, including dissipation of the envelope amplifier, is 51% with an average output power of 2.5 W and

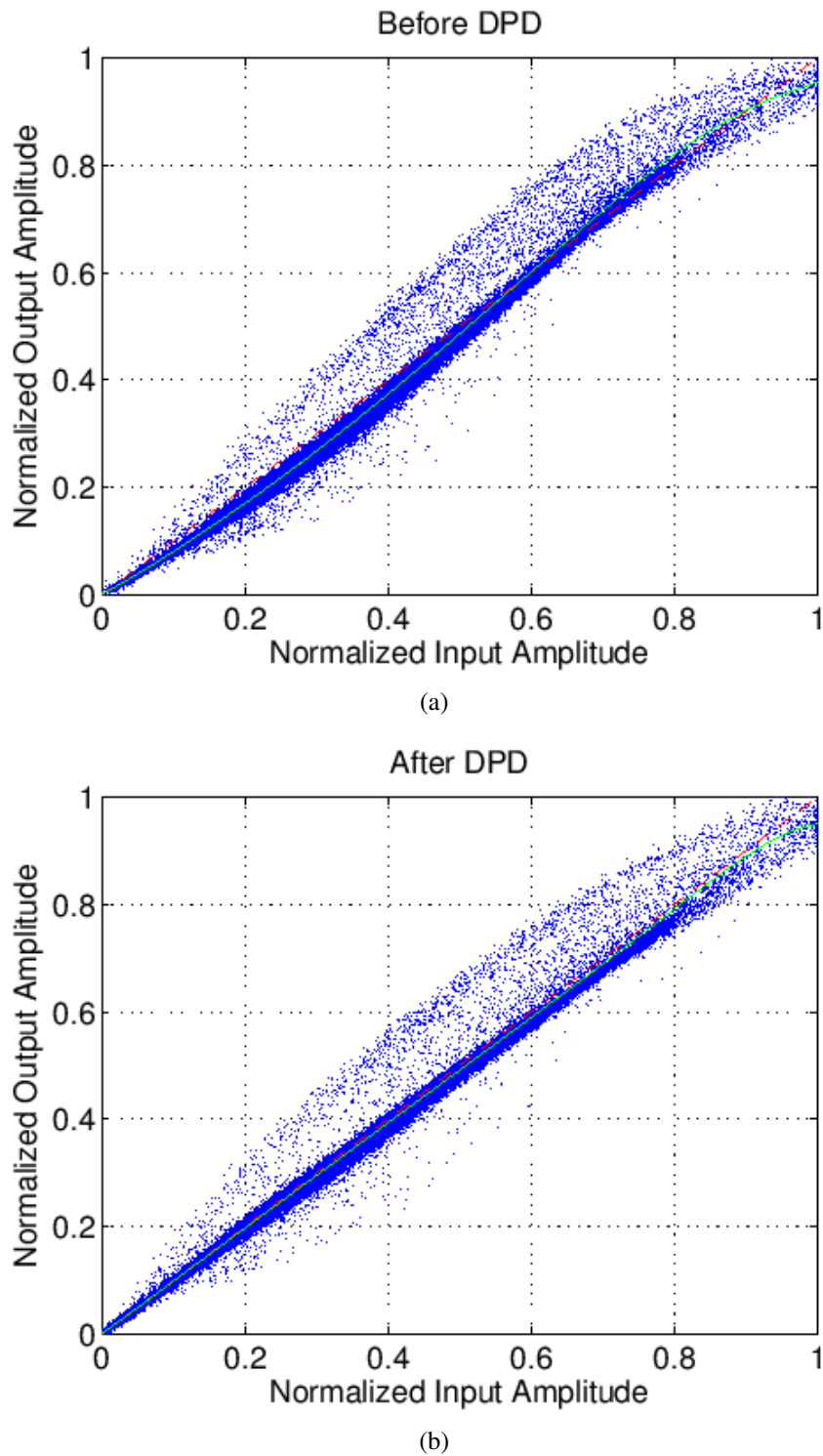
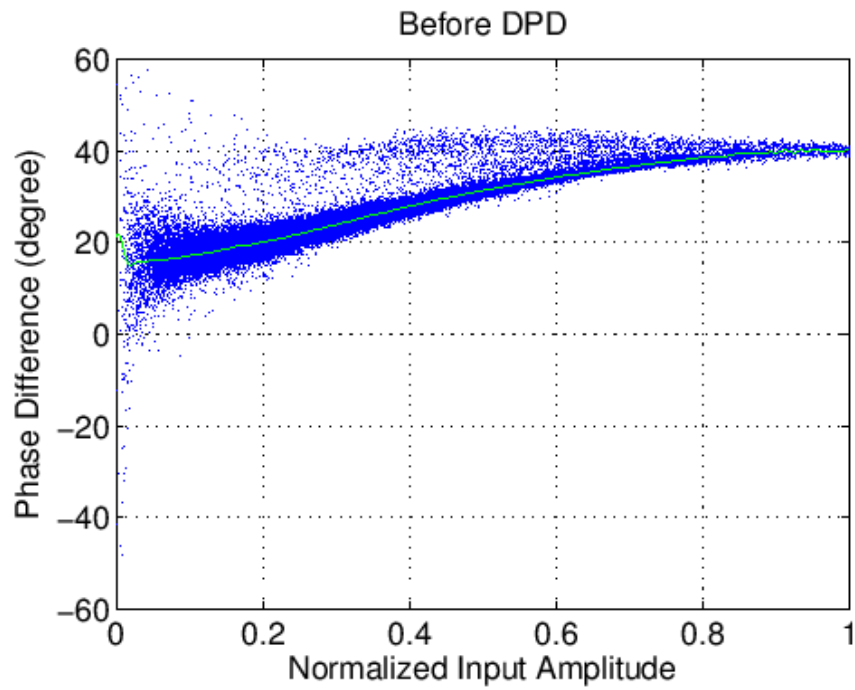
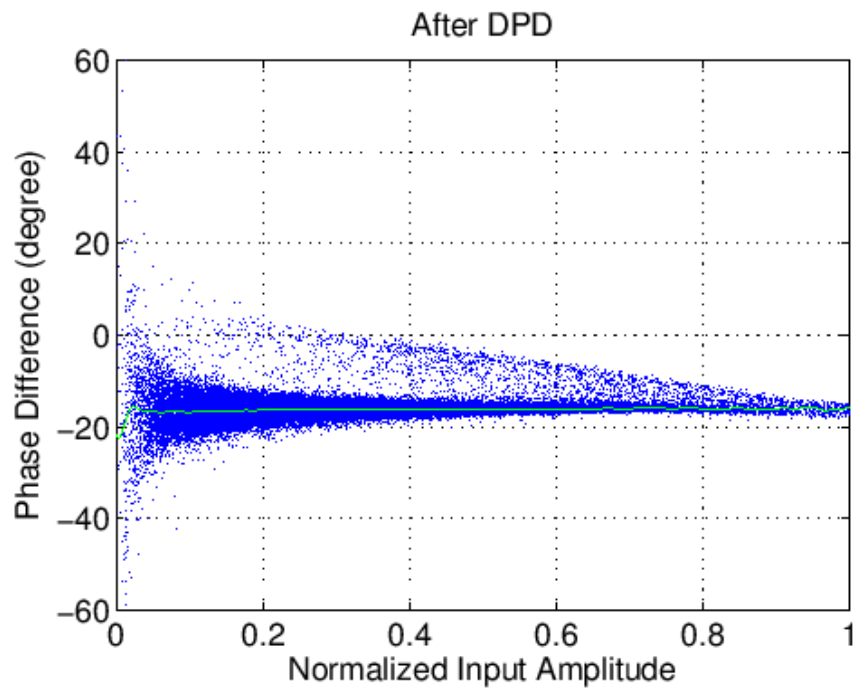


Figure 3.8: Measured: (a) AM-AM, (c) AM-PM performance before pre-distortion and (b) AM-AM, (d) AM-PM performance after memory-effect mitigation pre-distortion.



(c)



(d)

Figure 3.8: Measured: (a) AM-AM, (c) AM-PM performance before pre-distortion and (b) AM-AM, (d) AM-PM performance after memory-effect mitigation pre-distortion (continued).

Table 3.3: Comparison to Previous Monolithic Envelope Tracking Work and the Work Presented in This Paper

| Unit | Application | PAPR [dB] | Bandwidth [MHz] | Gain [dB] | Po [dBm] | PAE [%] | Technology | Efficiency (η_{em}) [%] |
|-----------|-------------|-----------|-----------------|-----------|----------|---------|----------------------------|--------------------------------|
| [39] | WLAN | 8 | 20 | 11 | 20 | 28 | 0.18- μ m BiCMOS | 65 |
| [56] | CDMA | 5 | 1.25 | - | - | - | 0.35- μ m CMOS | 82* |
| [45] | LTE | 7.42 | 20 | >26 | 26.1 | 34.1 | 65 nm CMOS/HBT | 71* |
| [61] | LTE | 6 | 20 | 29 | 30 | 45 | 150 nm CMOS/HBT | 68 |
| This work | WCDMA | 7.7 | 4 | 10 | 34 | 49 | 0.35- μ m BCD/GaN HFET | 72 |

* peak efficiency at the peak output power

a peak output power of 15 W. The gain and normalized power RMS error (NRMSE) are 10.2 dB and 1.2% after memory-effect mitigation DPD, respectively. At full output power, the peak envelope voltage was 14 V and the RMS voltage was 5.8 V. Table 3.2 summarizes the measured performance of the envelope tracking power amplifier with a single carrier WCDMA signal, and Table 3.3 summarizes a comparison of this work and the previously published envelope tracking power amplifiers with monolithic envelope amplifiers. In previous monolithic envelope tracking amplifiers (Table 3.3), the average output power of the integrated envelope amplifiers has been below 1 W and the supply voltage has been limited due to the low breakdown voltage of the CMOS transistors. For micro base-station applications, a higher supply voltage is required to generate the average output power of 2 to 4 W, and this high-voltage envelope amplifier shows the average output power more than 2 W and an average efficiency of 72%. To our knowledge, this is the first high-voltage monolithic envelope amplifier for multi-watt wide bandwidth RF applications, and the overall performance is demonstrated in the complete envelope tracking system is shown in Table 3.2.

3.4 Conclusion

This Chapter presented a high-efficiency envelope tracking power amplifiers with a high-voltage BCD monolithic envelope amplifier, to achieve high efficiency and linearity for wide bandwidth micro-base station applications. The overall drain efficiency of the ET system is 51% at 34 dBm output power with an average high voltage envelope amplifier efficiency of 72%, and the linearity requirements are met after memory-effect DPD for a WCDMA signal with a PAPR of 7.7 dB. This makes it possible for this high voltage monolithic envelope amplifier to be applied to wideband high efficiency micro-base station applications.

3.5 Acknowledgment

The author would like to thank Giuseppe Meola in STMicroelectronics for fabricating the chip, Sandro Lanfranco in Nokia Siemens Networks for supporting this work, Randy Cochran in Nitronex for providing the HFETs, and Cuong Vu's assistance on measurements at UCSD.

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The contributions from the co-authors are appreciated. The dissertation author was the primary researcher and the first author listed in these publications.

Chapter 4

High-Efficiency CMOS Envelope Amplifier with Direct Current Sensing for Handset RF Power Amplifiers

4.1 Introduction

High-efficiency is an important objective for RF power amplifiers (PAs), improving thermal characteristics and reliability. As the latest generation of smart devices deployed in cellular networks, explosive growth in network data traffic has been created, and the volume of data traffic has already exceeded that of voice traffic. This requires an energy-efficient device for long battery life with lower operating cost. At the same time, to meet the increasing demand for mobile broadband services with higher data rates, signals in 3G systems and beyond require higher peak to average power ratio (PAPR) and wide channel bandwidth. In case of a conventional linear power amplifier (PA) with fixed supply voltage, as shown in Fig. 4.1, higher PAPR signals cause the power amplifier to operate at a large back-off to meet tight linearity requirements. This impacts

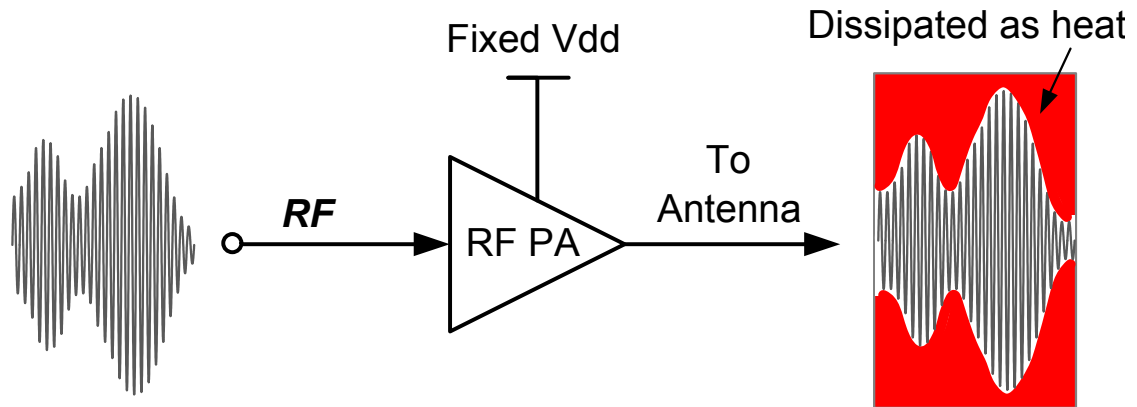


Figure 4.1: Conventional PA with constant supply voltage.

the efficiency and thermal characteristics due to the generated heat, as shown in Fig. 4.1. To solve these problems, many design techniques such as Doherty amplifier, out-phasing techniques, envelope elimination and restoration (EER), and envelope tracking (ET), have been proposed [9]. Among them, the envelope tracking (ET) system, shown in Fig. 4.2, improves the efficiency of a RF power amplifier (PA) by superimposing the envelope signal at the drain such that the RF power amplifier operates consistently closer to saturation. There are potential benefits in this technique, because the generated heat is reduced dramatically and this improves reliability.

It is important to optimize the efficiencies of both the envelope amplifier and the RF amplifier together to maximize the overall efficiency of the envelope tracking RF power amplifier. To improve the efficiency of the envelope amplifier, several architectures have been proposed [6, 45, 55–57, 62, 63]. In [62], a linear regulator is used for amplitude modulation, since it has wide bandwidth and low output ripple. However, its efficiency drops dramatically with a higher PAPR signal due to the low efficient regulator. In [57], a switched-mode power supply (SMPS) is used, since it has high efficiency. But high switching frequency (130 MHz) is required for a 4 MHz WCDMA signal and

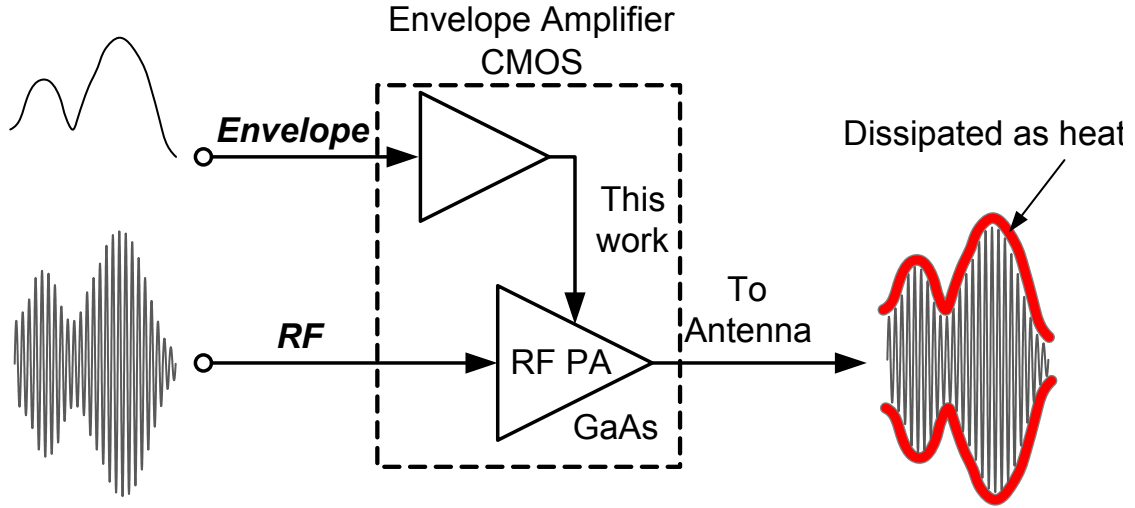


Figure 4.2: Envelope tracking PA with modulated supply voltage.

this limits the maximum operating signal bandwidth. For example, to be used with a wideband signal such as 20 MHz LTE, a higher switching frequency will be expected, and the efficiency will drop due to the high switching loss. In [6, 45, 55, 56, 63], a hybrid architecture combining both a linear stage and a switching stage is used to achieve the high efficiency and wide bandwidth together. However, the bandwidth in [55] is limited and an exceptionally large inductor was used to obtain the very-small output ripple in [56]. In [54, 64], a two-phase switching hybrid supply modulator is proposed to reduce output ripple, and improve the static efficiency by lowering the switching loss. However, two external inductors and additional die area are needed to implement a two-phase switching amplifier. To lower manufacturing cost in handset applications, the number of external components are limited.

This paper will describe the detailed design considerations and implementation of a monolithic CMOS wideband high efficiency envelope amplifier, and its application to an envelope tracking PA for LTE mobile-station applications. This paper is organized as follows. Section II presents the envelope tracking RF PA design consideration and the

comparison with a conventional architecture. Section III describes the detailed design consideration and circuit level implementation of a proposed CMOS envelope amplifier. In Section IV, experimental results are shown for LTE signals and a conclusion is given in Section V.

4.2 High Efficiency Envelope Tracking Power Amplifier Design

In envelope tracking techniques, the envelope amplifier drives the drain of the RF amplifier with an envelope signal proportional to the amplitude of the RF input signal, as shown in Fig. 4.2. As compared with a constant DC supply voltage, as shown in Fig. 4.1, the thermal dissipation is dramatically reduced and overall efficiency can be improved. However, dynamic supply modulation techniques can generate added nonlinearity, such as AM-AM and AM-PM distortion, from the limited bandwidth of the RF PA and the envelope amplifier [6]. In general, digital pre-distortion (DPD) techniques are employed in ET RF power amplifiers, to correct the nonlinearity of the dynamically biased amplifier, which is significantly different from that of an amplifier with constant bias voltage, and to achieve high efficiency while meeting the required linearity [49,52].

The overall efficiency of the envelope tracking RF power amplifier is given by

$$\eta_{ET} \cong \eta_{RF} \cdot \eta_{env} \quad (4.1)$$

where η_{RF} and η_{env} are the efficiencies of the RF amplifier and the envelope amplifier, respectively. From (4.1), it is important to optimize the efficiencies of both the envelope amplifier and the RF amplifier to increase the overall efficiency.

Since the RF device acts as a switch when highly saturated, low values of on-resistance becomes a critical characteristic of the device to achieve the optimal efficiency [36]. Silicon based technologies, such as SiGe HBT and CMOS, offer a low-cost solution for RF front-end block design. However, their low breakdown voltage is their main drawback for PA applications, and unique PA architectures need to be applied to resolve this issue [65, 66]. On the other hand, GaAs HBTs have high breakdown voltage, high gain, low on-resistance, and high efficiency due to high carrier mobility and bandgap engineering. RF transistors used in this work were fabricated using a single GaAs heterojunction bipolar field effect transistor (BiFET) process, which provides for all positive power supply voltage operation while maintaining high efficiency and good linearity [67]. As compared with a conventional GaAs HBT, this merged HBT-FET technologies (BiFET process) results in performance gains in low voltage biasing and reference voltage insensitivity, and the added versatility of having both bipolar and field-effect devices available for advanced applications [68].

4.3 Envelope Tracking Amplifier Circuit Design and Implementation

The power spectral density of the envelope of the 20 MHz LTE waveform is shown in Fig. 4.3. The envelope waveform has a high DC content due to full wave rectification during envelope extraction [56] and more than 85% of the envelope signal power lies below a few hundred kHz. The main key to achieving high efficiency with a wide bandwidth input signal comes from combining a switching stage, in order to provide a narrowband but efficient dynamic current source, and a linear stage to provide a wideband, but less efficient voltage source, as shown in Fig. 4.4. In a hybrid envelope

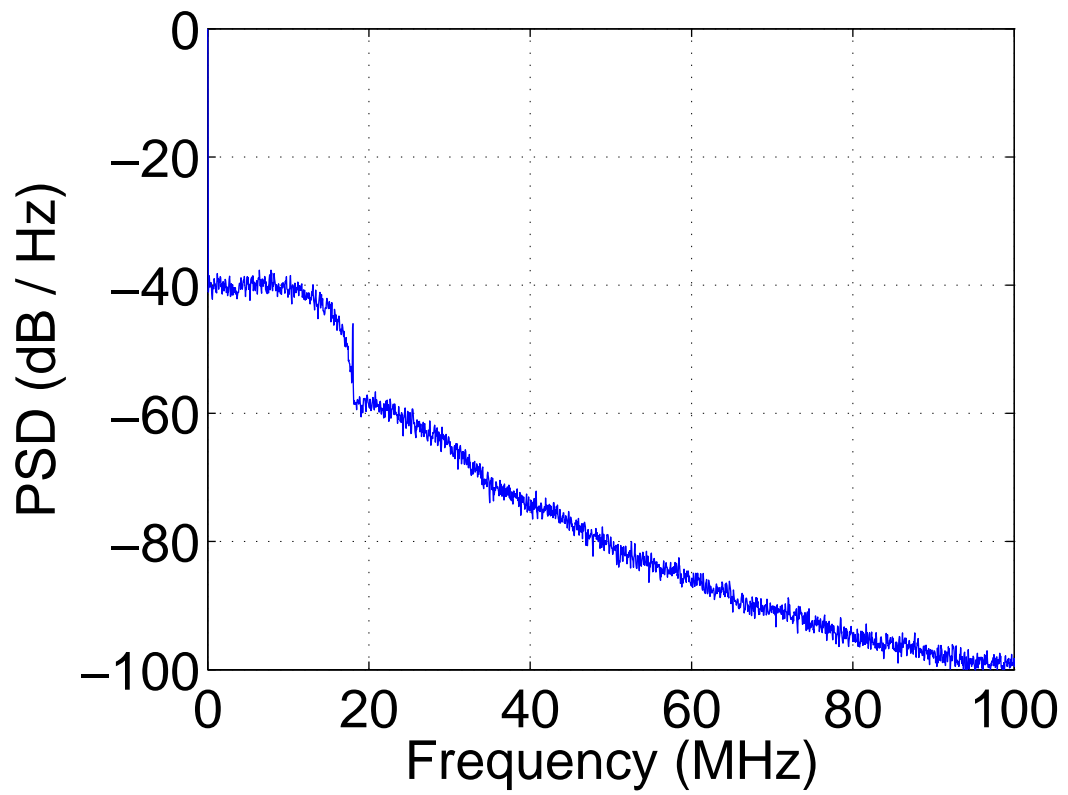


Figure 4.3: Normalized power spectral density (PSD) of the envelope signal for 20 MHz LTE.

amplifier, the current is supplied to the drain of the RF PA from both the linear stage and the switching stage through a current sensing network, which senses the current flowing out of the linear stages. The linear stage provides the difference between the desired output current and the current provided by the switching stage, such that the overall error is minimized [6]. Hence, the overall high efficiency is maintained when a highly efficient switching stage provides most of the load current by sensing the output current of the linear stage.

However, in the current sensing network, there is a non-zero delay between the output of the linear stage and the control input of the switching stage. This delay decreases the overall envelope amplifier efficiency, because it causes the less efficient linear stage to provide more power [6]. In [39], a current sense resistor is used to detect the current direction, but the input common-mode range of the hysteresis comparator needs to be rail-to-rail. This can result a large propagation delay variation according to the input common-mode voltage level. In [56], a current sensor and a trans-impedance amplifier (TIA) are used to sense the current and convert it to a voltage for the comparator. In [63], dual current sensing scheme with limited low-voltage output voltage swing, is used to generate the separate control signals for the switching stage. This scheme is proposed to solve the maximum allowable gate-to-source voltage limitation of LDMOS transistor and minimize the sensing delay time, however two sensing comparators and additional supply voltages are needed.

In the proposed envelope amplifier as shown in Fig. 4.4, single current sensing scheme is used to minimize die area and power consumption in the comparators. By applying the direct current sensing comparator, the delay between the output of the linear stage and the control input of the switching stage can be reduced because the

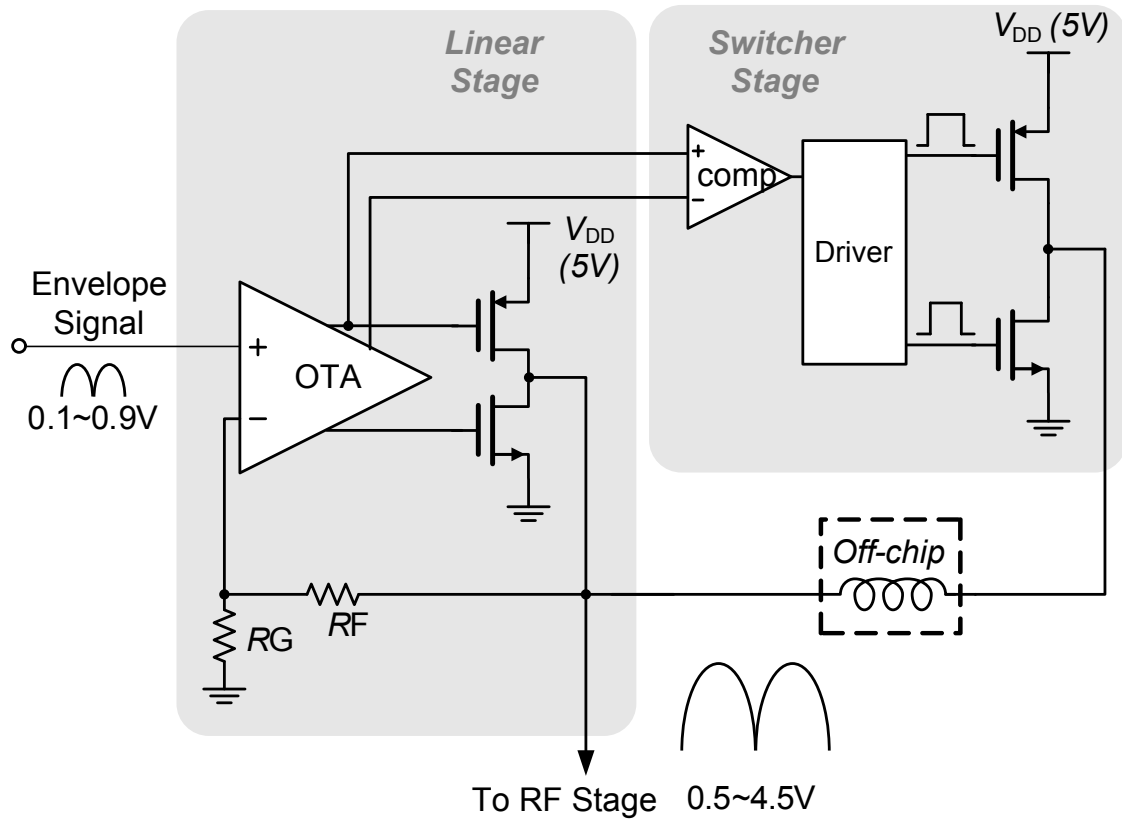


Figure 4.4: Proposed CMOS envelope amplifier.

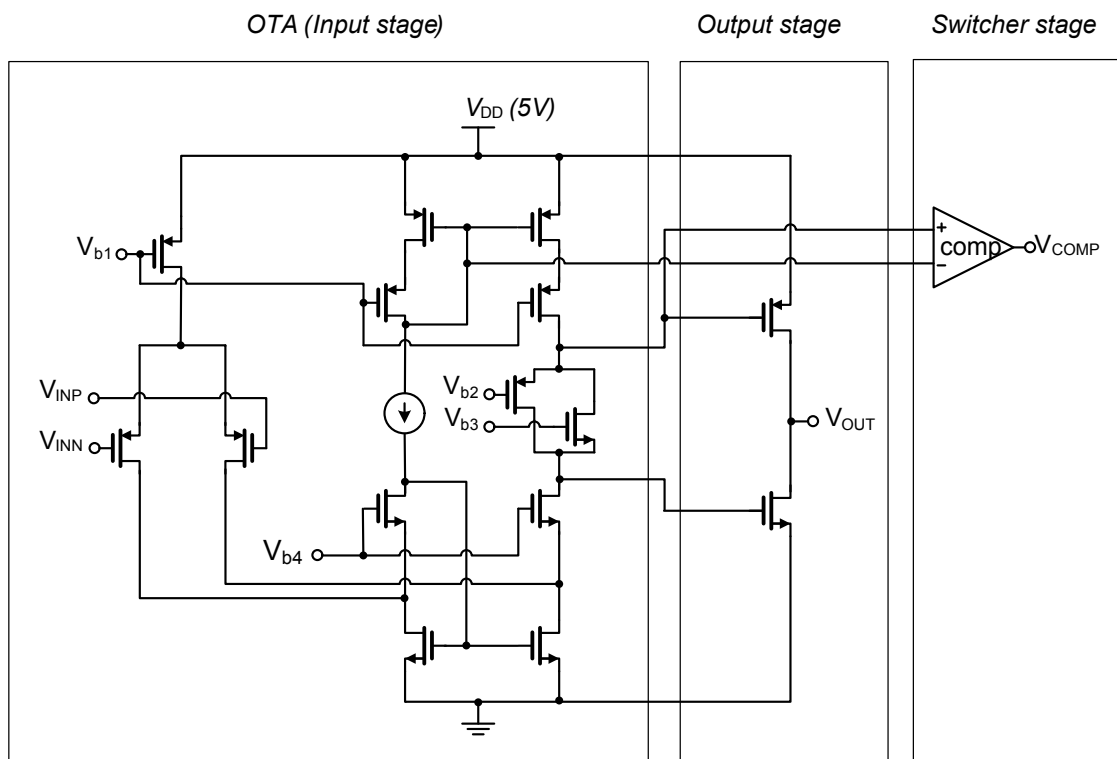


Figure 4.5: Simplified schematic of the linear stage.

comparator directly detects the control signals for the switching stage from the input of the push-pull amplifier in the linear stage. This brings many potential benefits because 1) additional circuit blocks such as the current sensing resistor and a trans-impedance amplifier (TIA), are not needed, 2) smaller area and lower power loss, and 3) the input common-mode of the comparator does not need to be rail-to-rail.

The low quiescent current is one of key factor to increase battery life and longer standby time in handset power amplifiers. In [61], a source cross-coupled linear amplifier is used as the first stage followed by a class-AB output stage to minimize the quiescent current. It has very low power dissipation of 83 mW with 6 V supply voltage in the quiescent condition. However, additional circuitry for a current sensing, such as a TIA and current mirrors contribute dc power consumption in the quiescent mode. Figure 4.5 shows the simplified schematic of the linear stage. The first stage is implemented with a folded-cascode type differential amplifier to achieve high gain and the output transistors are connected in a common-source configuration for rail-to-rail output voltages [58]. To achieve a good compromise between distortion and quiescent dissipation, the output stage is biased in class-AB mode. To minimize the unnecessary dc power consumption in the circuit, a traditional current biasing circuitry for the class-AB control is removed, and the class-AB control is biased by the cascodes of the summing circuits to save power consumption in the biasing circuit [58]. At the same time, a current mirror sensing the current from the linear stage and an op-amp based TIA converting the current into a voltage in [61, 64] can be eliminated by applying proposed direct current sensing scheme to minimize power loss. The simulated dc power consumption in the quiescent condition was measured to be 51 mW with 5 V supply voltage. The linear amplifier shows over 55 dB open-loop DC gain and over 170 MHz bandwidth.

The efficiency of the envelope amplifier in Fig. 4.4 can be evaluated by consider-

ing the power loss mechanisms associated with each stage. The power loss in the output stage of the linear stage, P_{loss_lin} , is a sum of the loss from NMOS transistor, P_{loss_MN} , and the loss from PMOS transistor, P_{loss_MP} . Each power loss is given by

$$P_{loss_MN}(t) \cong (I_{sw}(t) - I_{load}(t)) \cdot V_{out}(t) \quad (4.2)$$

$$P_{loss_MP}(t) \cong (I_{load}(t) - I_{sw}(t)) \cdot (V_{DD} - V_{out}(t)) \quad (4.3)$$

where I_{sw} is the switcher stage current, I_{load} is the output load current, V_{DD} is the supply voltage, and V_{out} is the output voltage at the load, respectively [3]. In [6], the switcher stage current, I_{sw} , is assumed to be constant, because I_{sw} has a slowly varying amplitude compared with the output voltage waveform with a large inductor. The delay effects in the switcher stage can be negligible, when the switcher current variation is small enough to be considered as constant. However, a smaller value of inductance is preferred in wideband applications such as 20 MHz LTE [61] to increase the bandwidth, so that a switcher stage can drive more currents. As a result, the switcher current has a fast varying amplitude, and should be considered as a time-varying signal for wideband applications.

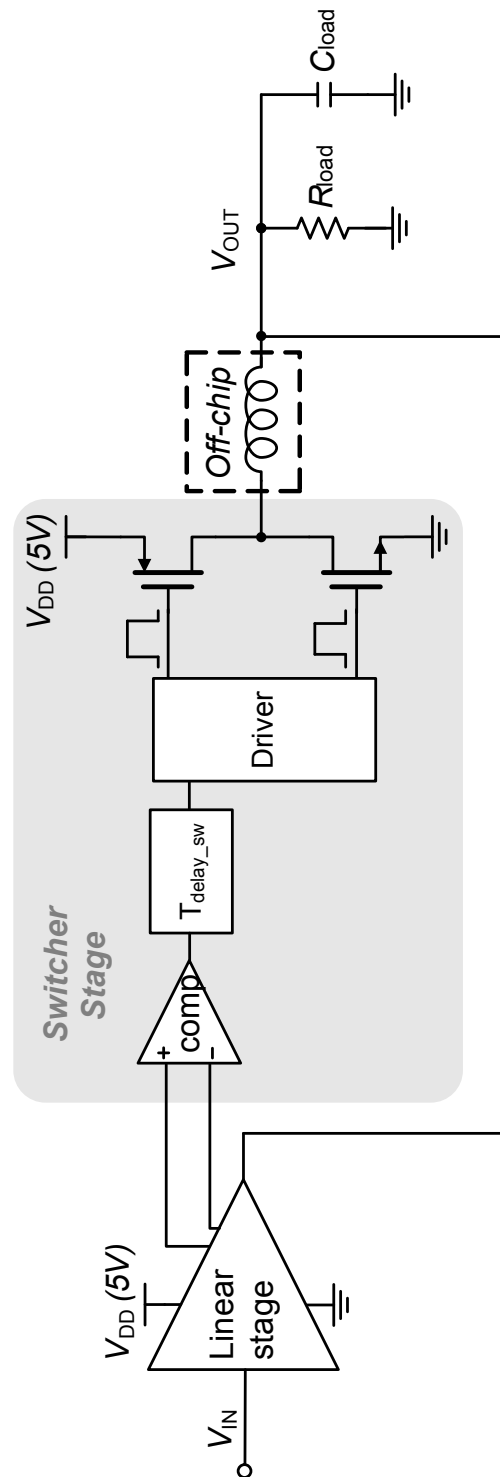


Figure 4.6: Simplified simulation schematic for the efficiency of the envelope amplifier as a function of an additional delay in the switcher stage. $R_{load} = 5.7 \Omega$ and $C_{load} = 5$ pF.

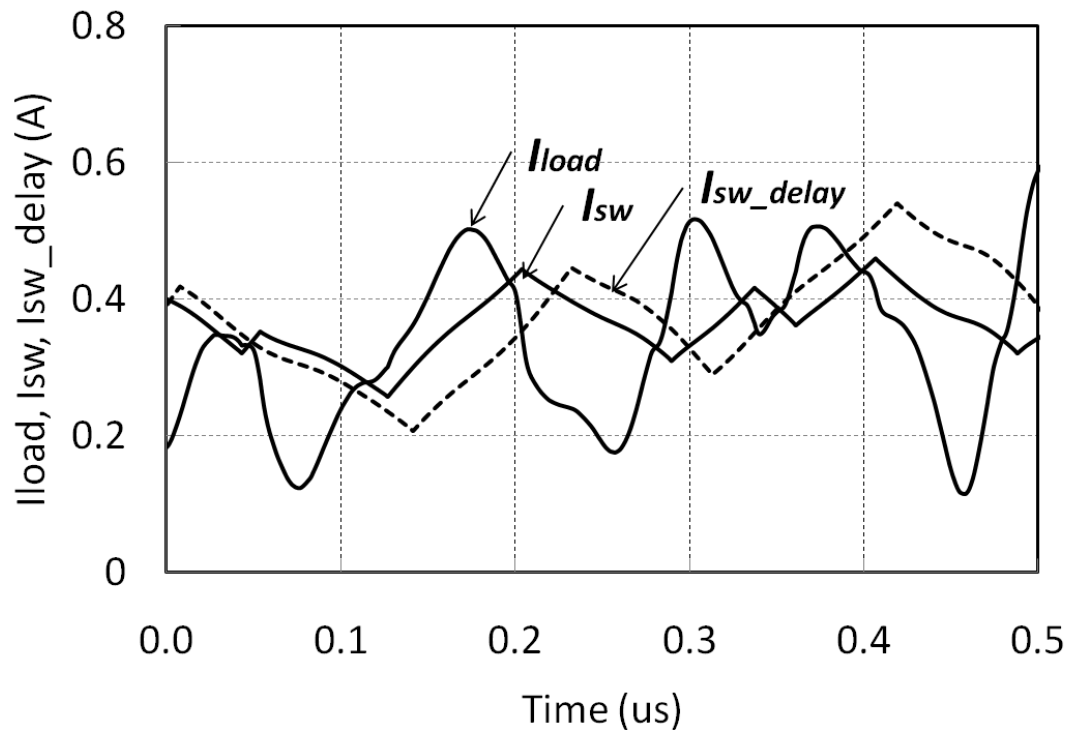


Figure 4.7: Simulated output load and switch current waveforms with an additional switcher stage time delay of 20 ns.

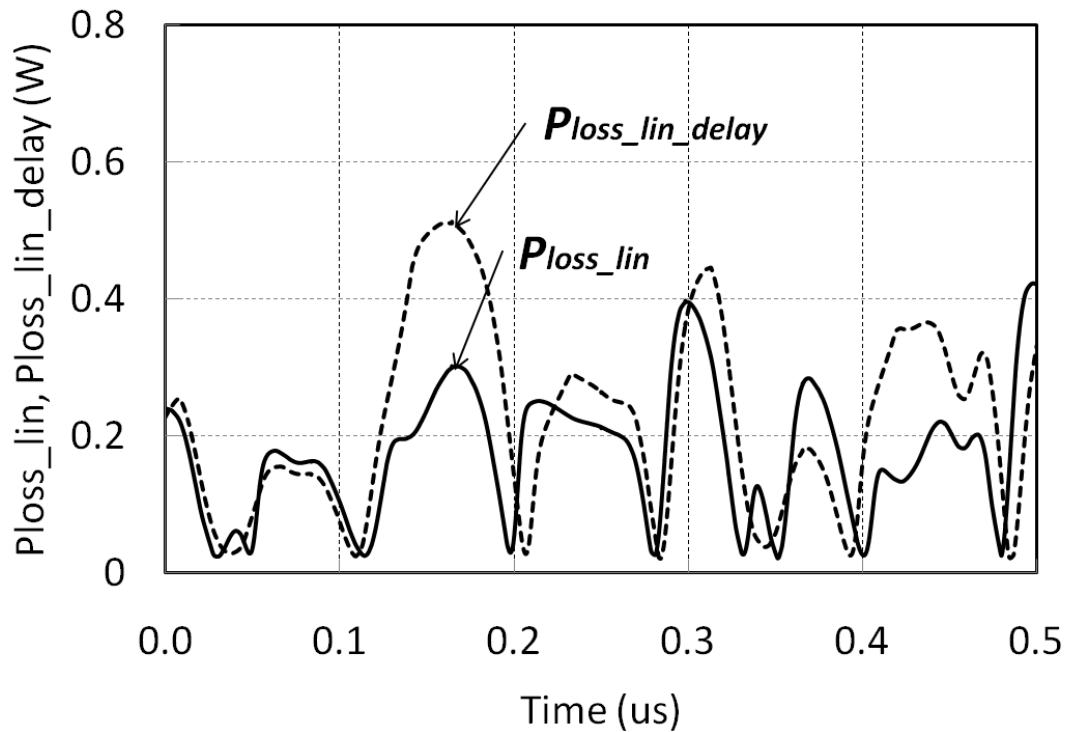


Figure 4.8: Simulated linear stage main power loss comparison with an additional switcher stage time delay of 20 ns.

To check the effects of the delay in the switcher stage on the overall efficiency of the envelope amplifier, an additional time delay (T_{delay_sw}) is added in the circuit simulation as shown in Fig. 4.6. By adding this time delay, the current from the switcher stage would be mis-aligned from the optimum condition as shown in Fig. 4.7. As the time delay is increased, the current from the low efficient linear stage would be increased. As a result, the power losses in 4.3 and 4.2 are also increased. Figure 4.8 shows the comparison of the total linear stage power loss, P_{loss_lin} , according to the delays. The overall envelope amplifier efficiency with a 5.7 ohm resistive load for a 6.1 dB PAR 20 MHz LTE signal drops as an additional delay increases as shown in Fig. 4.9. For example, the

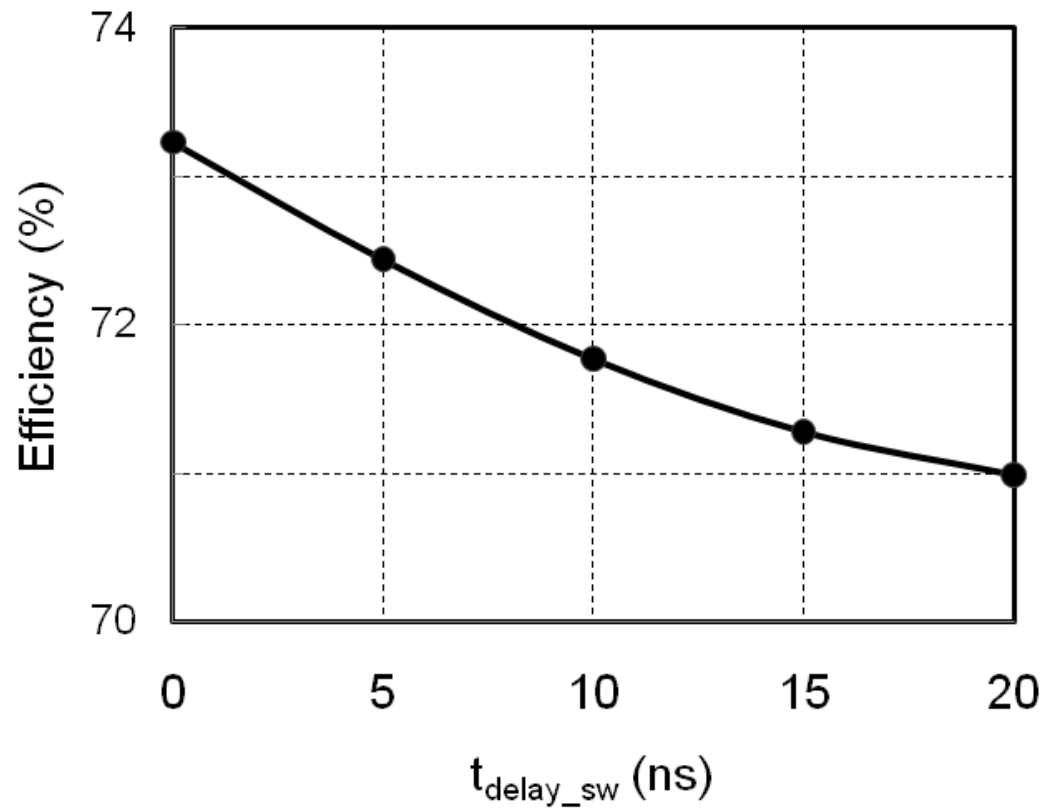


Figure 4.9: Simulated efficiency of the envelope amplifier as a function of an additional delay in the switcher stage.

overall efficiency drops more than 2% with an additional 20 ns delay and it is important to minimize the propagation delay in the switcher stage to improve the efficiency of the envelope amplifier in this architecture.

There are two main sources of power loss in the switching stage, conduction loss which mainly comes from on-resistance and switching loss which is dependent on the switching frequency and the parasitic capacitance [6]. To minimize the conduction loss, wider device width is needed, but at the same time the switching loss will be increased due to the large parasitic capacitance. As the high switching frequency due to wide bandwidth is required, this design trade-offs should be considered to improve the overall efficiency. In this design, the switching stage is sized to achieve minimum power loss and optimum gate drive together. The simulated efficiency of the switching stage including a driver, is greater than 94% up to a switching frequency of 10 MHz. The comparator is based on a standard CMOS design, as described in [69]. When the gate control signal for NMOS and PMOS transistors in the switcher stage are synchronized, both transistors are turned-on for a short time [39]. These shoot-through currents cause additional undesirable power loss in the switcher stage and a non-overlapping control signal generation circuit is implemented in the gate driver logic [70].

4.4 Measured Envelope Tracking Power Amplifier Result

The proposed envelope amplifier is fabricated using a 150 nm CMOS process with 6 metal layers [71]. To achieve a high voltage operation such as 5 V, thick gate oxide transistors are used. A chip micrograph is shown in Fig. 4.10, and its size is 1.5 mm × 1.0 mm including I/O pads. For a wideband applications, the switching

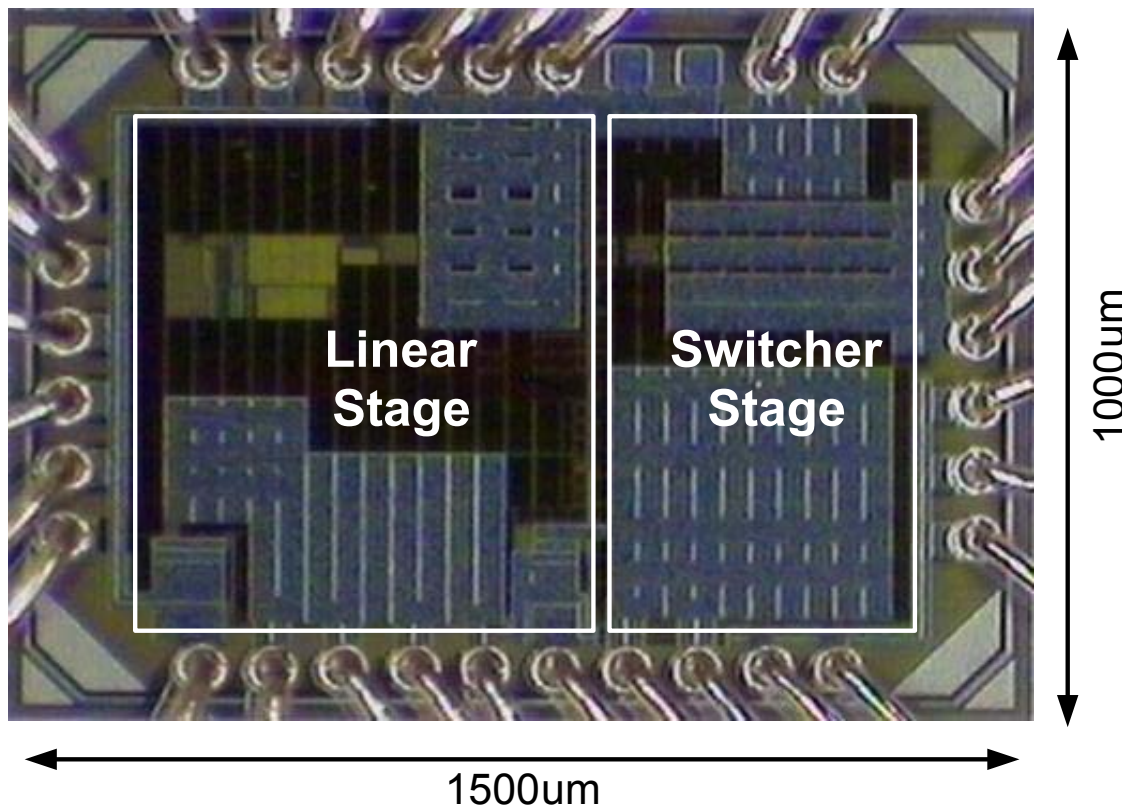


Figure 4.10: Die-photograph of envelope amplifier. The chip occupies 1.5 mm^2 die area including the pads.

frequency of the envelope amplifier has been increased to provide enough bandwidth [61]. In a monolithic envelope amplifier, the switching noise of the buck-converter can be modulated onto the envelope amplifier output waveform if the noise coupling between the linear amplifier and the switching buck-converter is large. To achieve good isolation between the linear amplifier and the switching buck-converter, special care is taken in the physical layout. By placing the two circuit blocks on separate ends of the die, with separate substrate contacts, the coupling of the switching noise to the envelope amplifier output signal was reduced. In addition, double guard-rings with dedicated substrate and n-well rings surrounded each circuit.

Figure 4.11 shows the comparison of measured and simulated efficiency of the envelope amplifier as a function of the signal bandwidth with a $10\ \Omega$ resistive load. As the signal frequency of the input single-tone sine waveform is increased from 1 MHz to 10 MHz, the overall efficiency drops because of the increased switching loss. To check the supply voltage dependence, the supply voltage of the envelope amplifier was swept from 4 V to 6 V with 1 V step and the efficiency with a 5 MHz sine input was shown in Fig. 4.12. The overall efficiency of the envelope amplifier has changed less than 1% over the wide range of supply voltage.

The measured performance of the amplifier with a resistive load is summarized in Table 4.1. A load resistor of 5.7 ohm corresponding to 30 dBm RF output power, was used to characterize the performance. The supply voltage for the envelope amplifier is 5 V and Fig. 4.13 shows the measured time-domain input and output of the envelope amplifier in conjunction with the switcher stage output. The output voltage of the envelope amplifier is five times the input voltage and the output voltage range is 0.5 to 4.5 V. The switching voltage is rail-to-rail ($V_{DD} = 5\ \text{V}$) and the average switching frequency

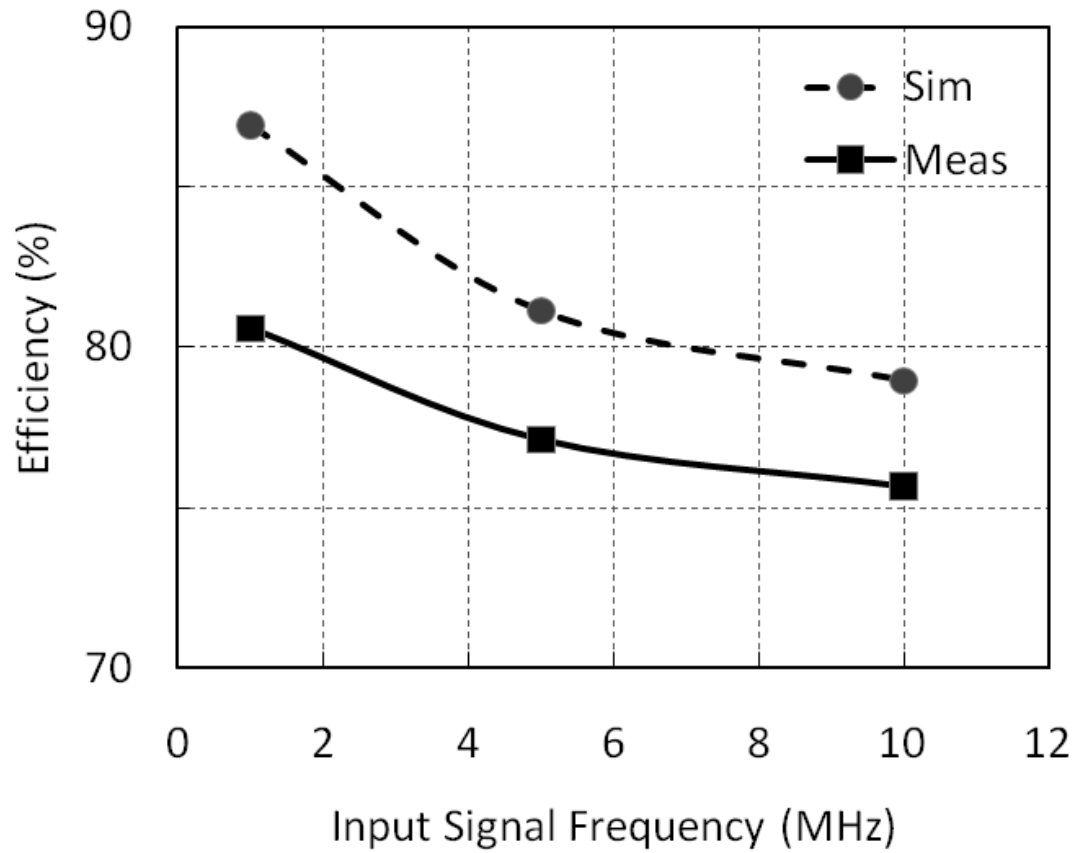


Figure 4.11: Comparison of measured and simulated envelope amplifier efficiency as a function of signal bandwidth. Sine wave input, $V_{DD} = 5 \text{ V}$ and $R_{load} = 10 \ \Omega$.

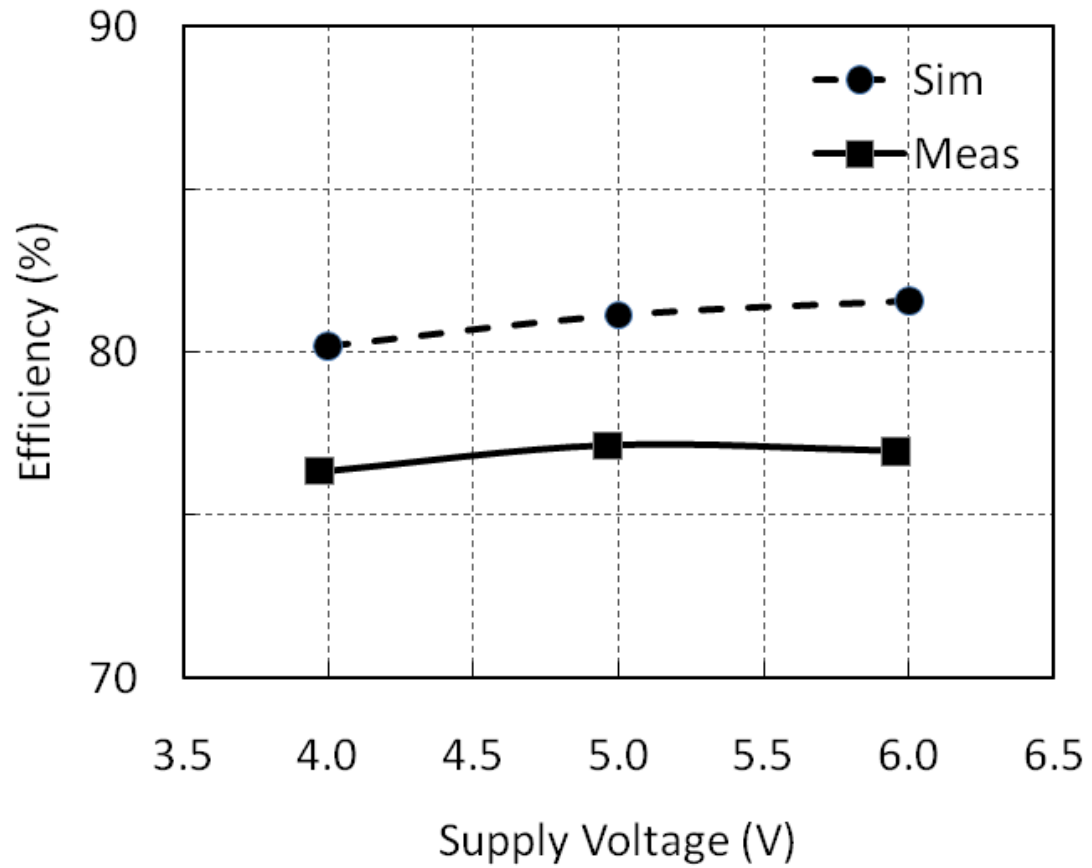


Figure 4.12: Comparison of measured and simulated envelope amplifier efficiency as a function of supply voltage. 5 MHz sine wave input and $R_{load} = 10 \Omega$.

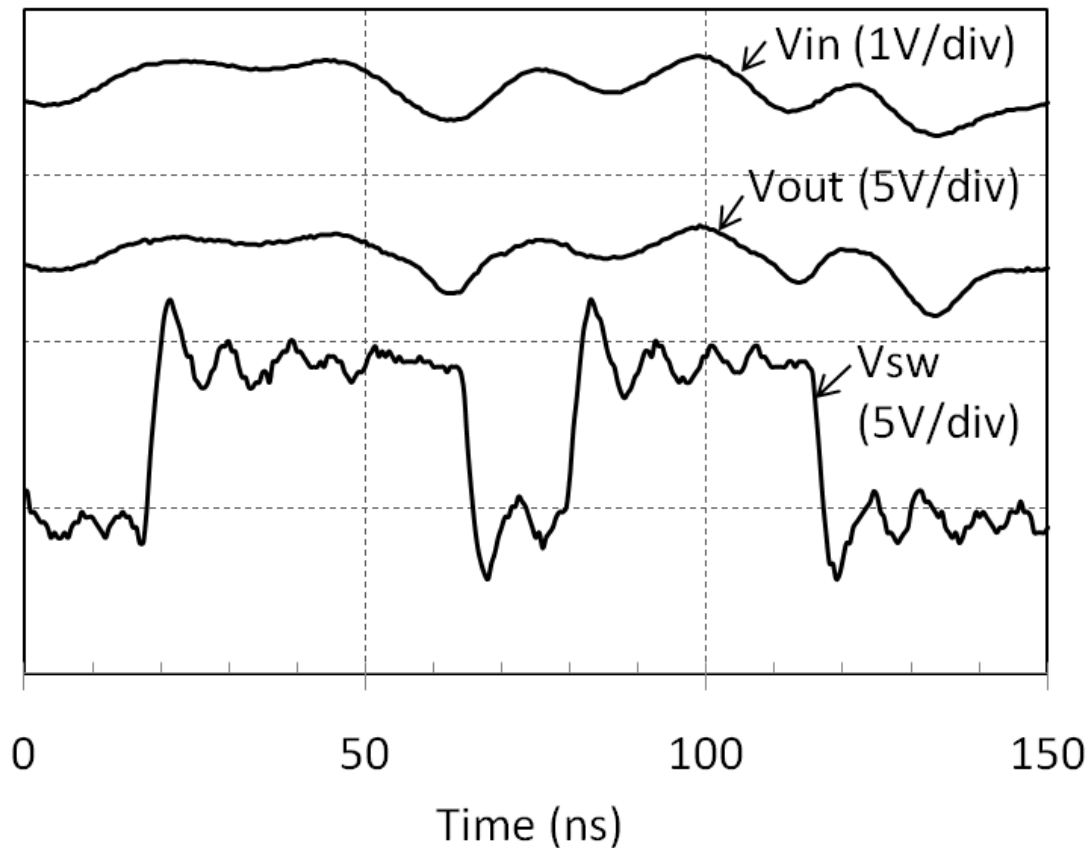


Figure 4.13: Measured envelope amplifier input, output voltage, and switcher stage output voltage. The envelope input signal is a 6.1dB PAR 20 MHz LTE signal. $V_{DD} = 5$ V and 50 ns/div.

of the switching voltage was 10 MHz for a single carrier 20 MHz LTE signal. Figure 4.14 shows the input and output transient response of a 1 MHz square waveform with a 5.7 ohm resistive load. For wideband signals, high slew rate is required, and it shows a slew-rate of 200 V/us.

To check the overall efficiency of the envelope amplifier with 5 and 20 MHz LTE signals, the efficiency was measured with resistive loads as shown in Fig. 4.15.

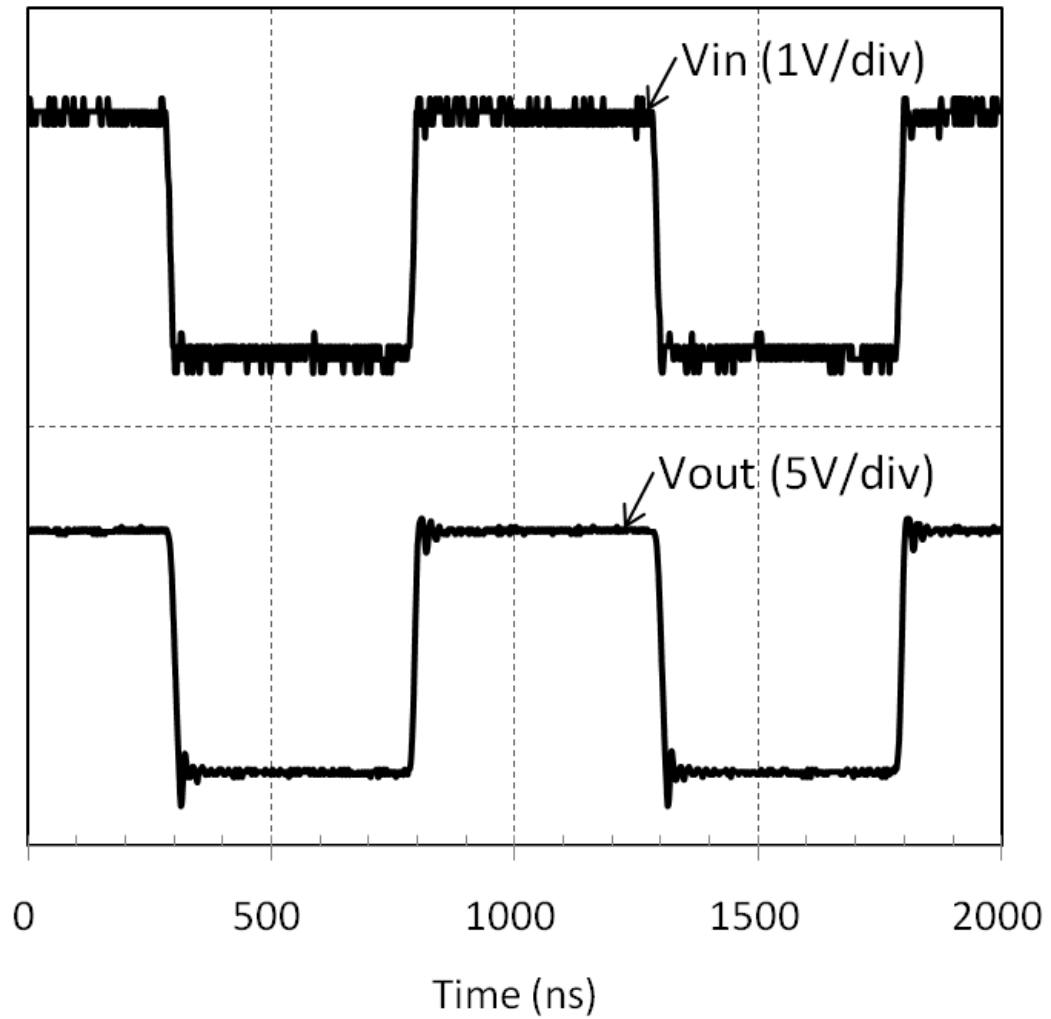


Figure 4.14: Measured envelope amplifier output voltage with 1 MHz square waveform input. $V_{DD} = 5\text{ V}$, $R_{load} = 5.7\ \Omega$. and 500 ns/div.

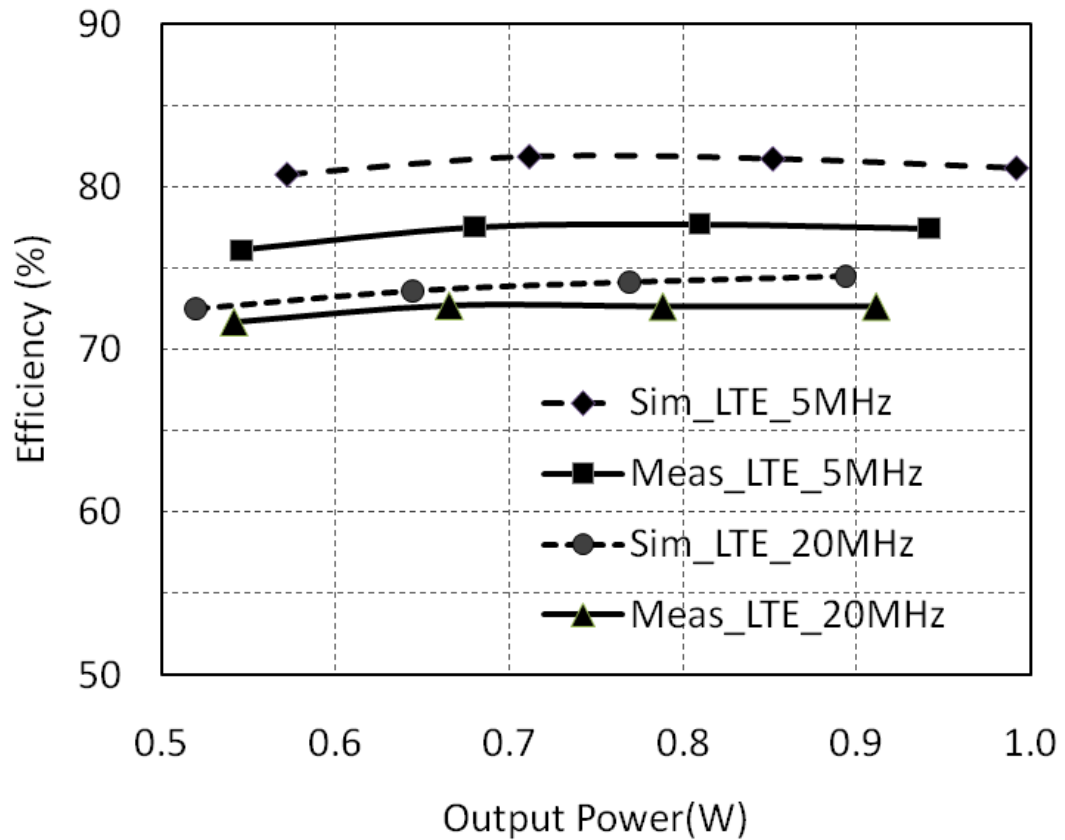


Figure 4.15: Comparison of measured and simulated envelope amplifier efficiency as a function of output power and LTE signal bandwidths. $V_{DD} = 5$ V. $R_{load} = 5.7 - 9.9 \Omega$.

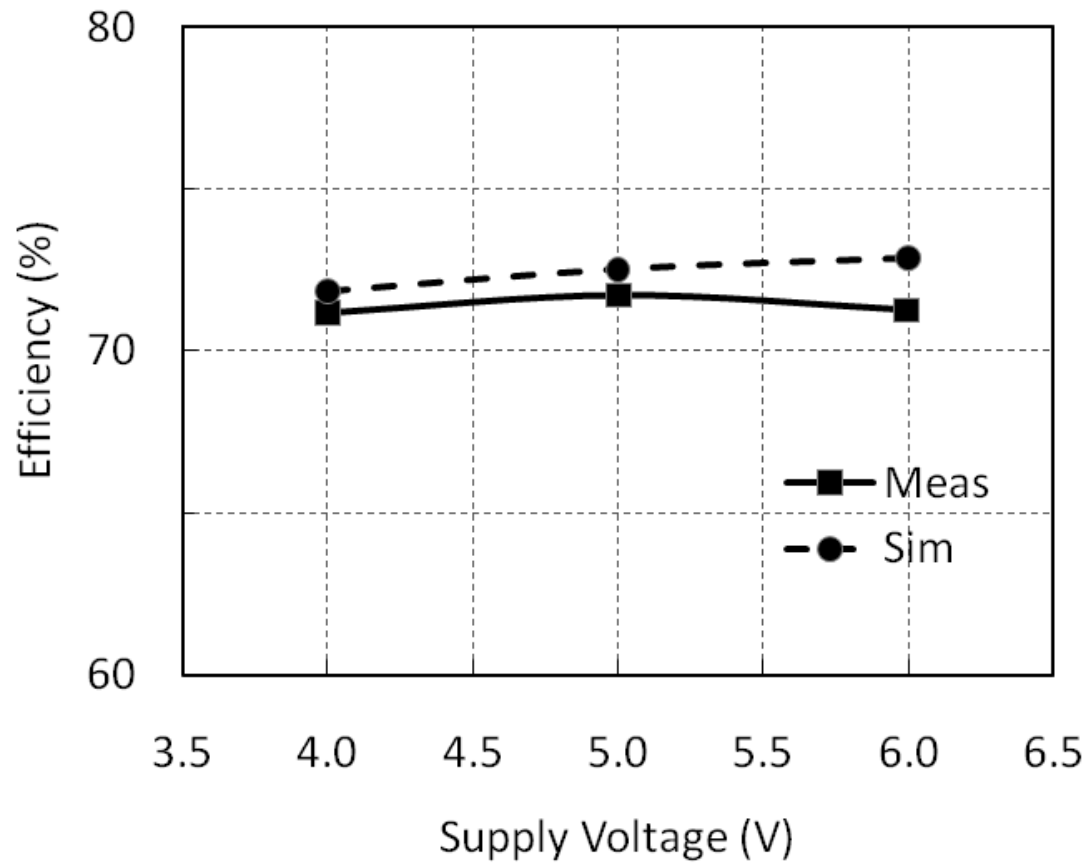


Figure 4.16: Comparison of measured and simulated envelope amplifier efficiency with a 20 MHz LTE signal as a function of supply voltage. $V_{DD} = 5$ V. $R_{load} = 9.9 \Omega$.

The value of the resistive load was increased from 5.7 ohm to 9.9 ohm, to check the effects of different load line of RF PAs and various output power level. The measured overall efficiency of the envelope amplifier is approximately 78% and 73% with 5 MHz and 20 MHz LTE signals respectively and shows stable performance over the wide range of the output power level. In Fig. 4.16, the efficiency of the envelope amplifier with a 20 MHz LTE signal shows low dependence on the supply voltage and the efficiency difference was less than 1%. When the supply voltage was increased from 4 V to 6 V, the maximum output envelope voltage was set to have 0.5 V voltage headroom for each case.

The performance of the envelope tracking amplifier utilizing the GaAs HBT-based RF PA was measured using a 5 MHz LTE signal at 2.535 GHz. The measurement setup for the complete ET amplifier is shown in Fig. 4.17. The envelope signal and baseband signal are generated in the digital domain. To optimize efficiency while meeting the linearity requirements, decreasing, an adjustment of the PAPR, digital pre-distortion is performed digitally on the baseband signal. After up-conversion, the resultant RF signal provides the input to the RF amplifier, and the supply voltage is modulated by the envelope signal which has been amplified by the wideband and high-efficiency CMOS envelope amplifier.

The output of the envelope amplifier has to be time-aligned to the output of the RF amplifier, so that extra distortion is not created by the resulting time mismatch between the RF path and envelope signal path [39]. Synchronization is performed in the digital domain by comparing the input signal and the down-converted output signal, to minimize distortion [35]. Figure 4.18 shows the measured time-domain output of the

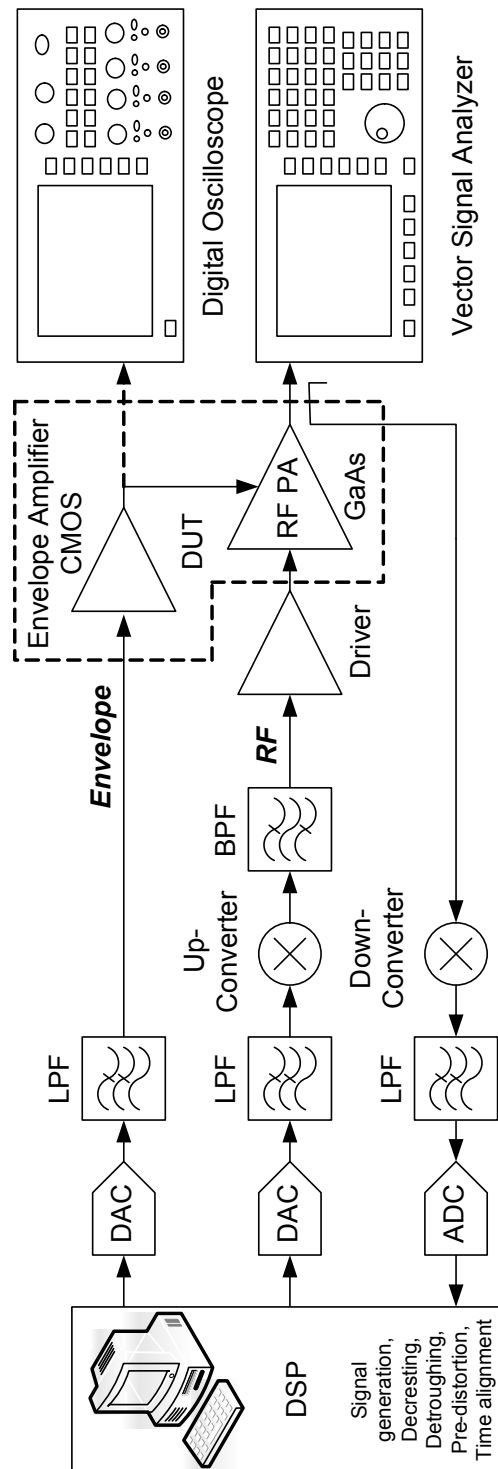


Figure 4.17: Measurement test setup diagram of the complete ET PA.

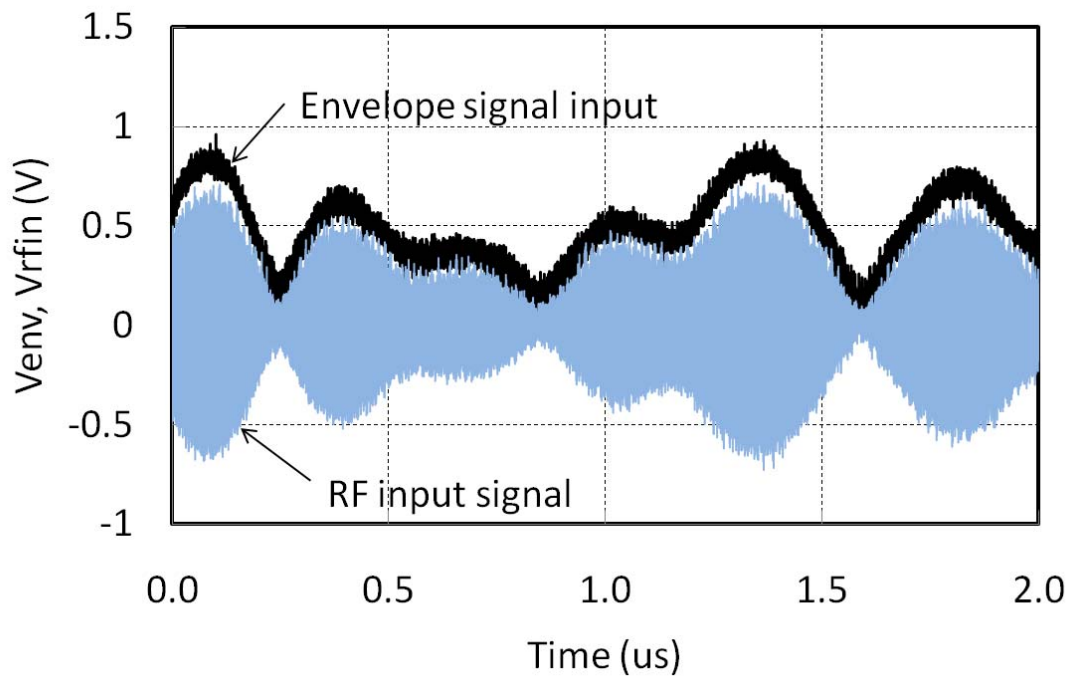


Figure 4.18: Measured input RF signal and envelope signal under time-alignment condition.

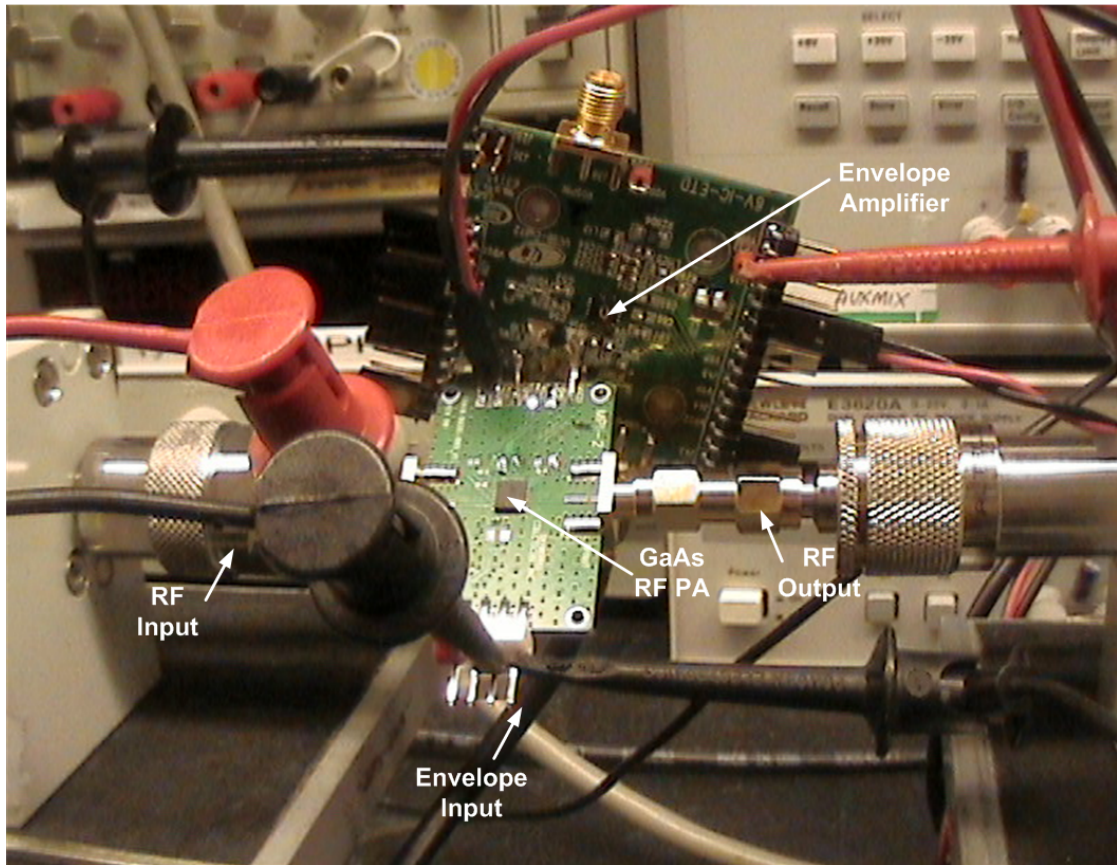


Figure 4.19: Test fixture setup with envelope amplifier IC and RF power amplifier for the envelope tracking system.

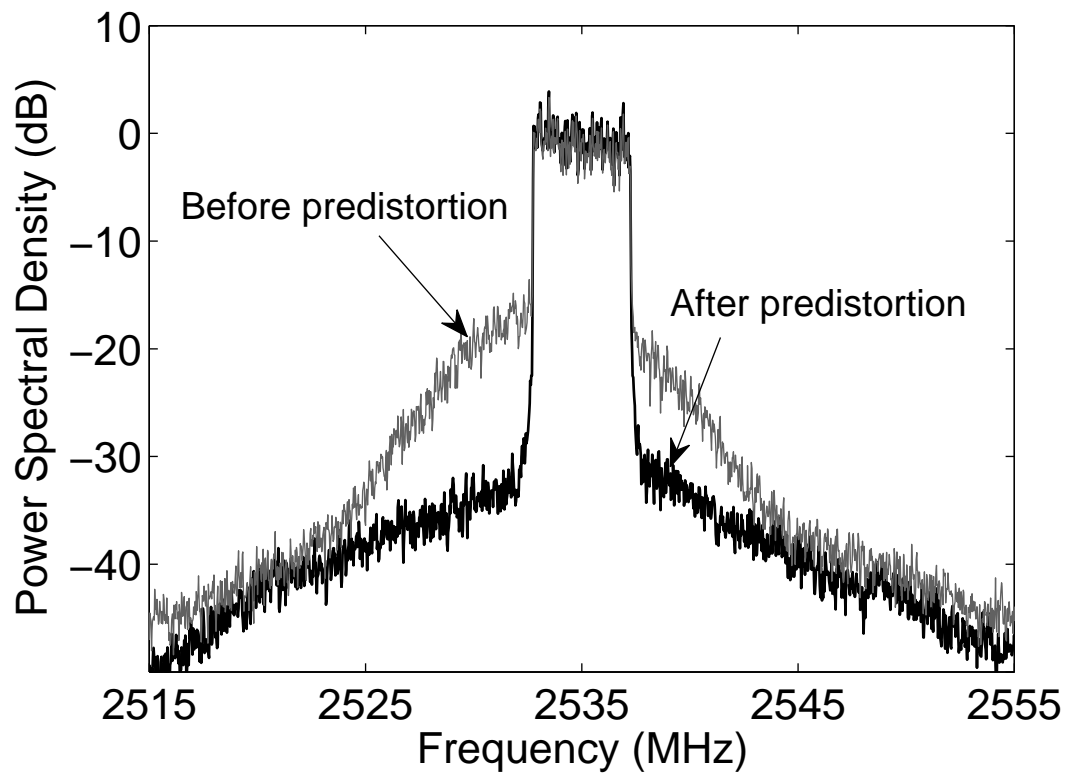


Figure 4.20: Normalized measured output power spectral density of single carrier 5 MHz LTE signal with 6.1-dB PAR before predistortion, and after pre-distortion. ($f_{CENTER} = 2.535$ GHz, $P_{OUT} = 27.6$ dBm.)

Table 4.1: Performance Summary of the Measured Envelope Amplifier

| Parameter | Values |
|-----------------------------|-----------------|
| Technology | 150 nm CMOS |
| Die Area | 1.5 mm x 1.0 mm |
| Supply Voltage | 5 V |
| Output Voltage | 0.5 V to 4.5 V |
| Voltage Gain | 14 dB |
| Output Power | 29.6 dBm |
| Bandwidth | 5 MHz |
| Envelope Amp. Efficiency | 78% |
| Average Switching Frequency | 2 MHz |

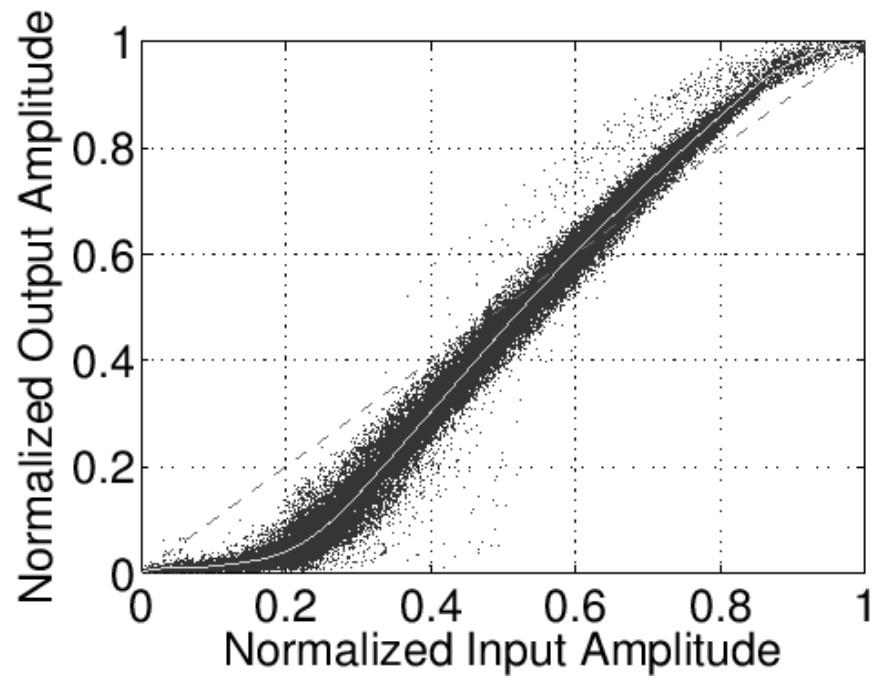
envelope amplifier superimposed on the measured output of the RF amplifier, and the two signals are aligned after synchronization process. In addition, memoryless DPD is carried out to compensate for the expected gain variation of the amplifier over the envelope tracking trajectory [6]. Figure 4.19 shows the picture of the test fixture with envelope amplifier and RF power amplifier.

The performance of the overall envelope tracking power amplifier was measured with a single carrier 5 MHz LTE uplink signal at 2.535 GHz. The peak-to-average power ratio of the LTE signal is 6.1 dB. The average measured power added efficiency of the ET power amplifier, including dissipation of the envelope amplifier, is 46% with an average output power of 27.6 dBm and a gain of 26.5 dB. At full output power, the peak envelope voltage was 4.5 V and the RMS (root-mean square) voltage was 2.3 V.

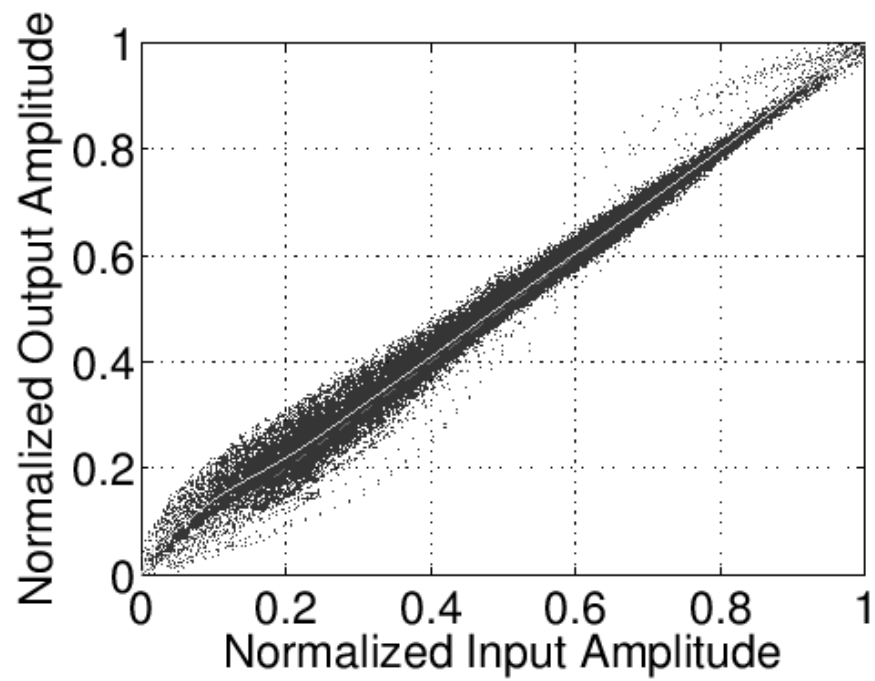
Table 4.2: Comparison to Previous Monolithic Envelope Tracking Work and the Work Presented in This Chapter

| Unit | Application | PAPR [dB] | Bandwidth [MHz] | Gain [dB] | Po [dBm] | PAE [%] | Technology | Envelope Amp. Efficiency [%] |
|-----------|-------------|-----------|-----------------|-----------|----------|---------|----------------------|------------------------------|
| [39] | WLAN | 8 | 20 | 11 | 20 | 28 | 0.18- μ m BiCMOS | 65 |
| [56] | CDMA | 5 | 1.25 | - | - | - | 0.35- μ m CMOS | 82* |
| [45] | LTE | 7.42 | 20 | >26 | 26.1 | 34.1 | 65 nm CMOS/HBT | 71* |
| [61] | LTE | 6 | 20 | 29 | 30 | 45 | 150 nm CMOS/HBT | 68 |
| This work | LTE | 6.1 | 5 | 26.5 | 27.6 | 46 | 150 nm CMOS/HBT | 78 |

* peak efficiency at the peak output power

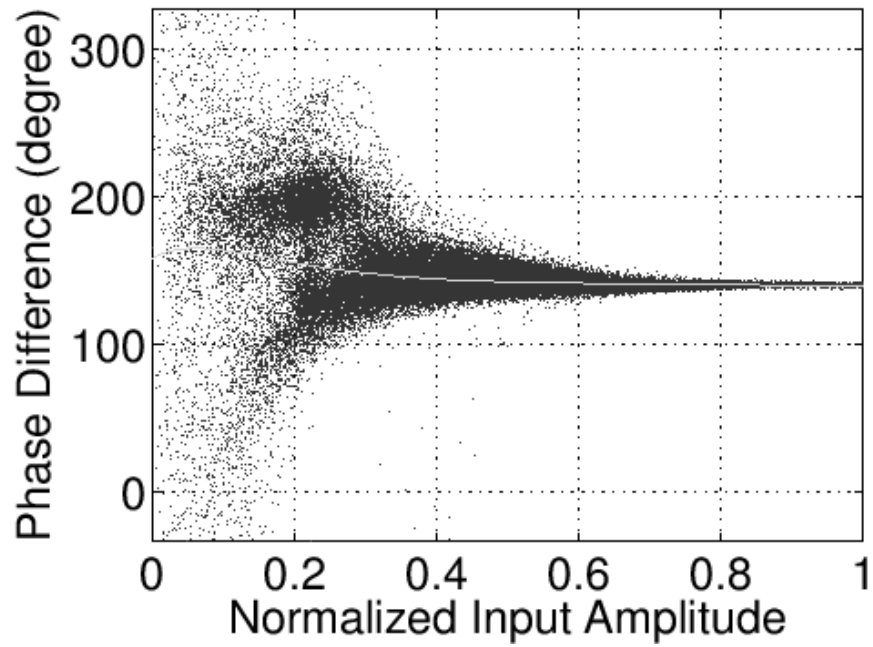


(a)

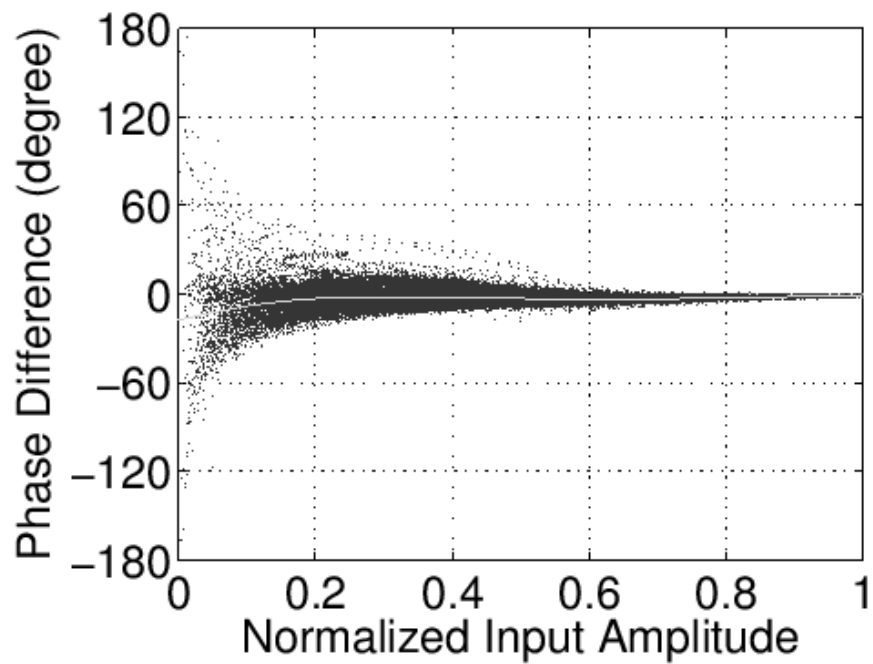


(b)

Figure 4.21: Measured: (a) AM-AM performance before pre-distortion and (b) AM-AM performance after memoryless pre-distortion.



(a)



(b)

Figure 4.22: Measured: (a) AM-PM performance before pre-distortion and (b) AM-PM performance after memoryless pre-distortion.

Figure 4.20 shows a comparison of the normalized output signal spectrum before and after digital pre-distortion (DPD). The ACLR performance is improved through DPD and the specifications are met. The ACLR specifications for a 5 MHz LTE uplink output signals are -33 dBc at the 5 MHz offset and -36 dBc at the 10 MHz offset. Figure 4.21 and Fig. 4.22 shows the measured AM-AM and AM-PM characteristics of before and after DPD. The scatter of the plotted data indicates a modest memory effect including measurement noise. The AM-AM distortion is negligible and the averaged AM-PM deviation is approximately 3 degrees after DPD. Table 4.2 summarizes a comparison of this work and the previously published envelope tracking power amplifiers with monolithic envelope amplifiers for handset applications. This comparison result indicates that a proposed envelope amplifier can be an attractive candidate for wideband high-efficiency ET PA applications.

4.5 Conclusion

This Chapter presented a high performance envelope tracking power amplifier, to achieve high efficiency and linearity for wide bandwidth handset applications. The overall PAE of the ET system is 46% at 27.6 dBm output power with an averaged CMOS envelope amplifier efficiency of 78%, and the linearity requirements are met after DPD. These results demonstrate the great potential of CMOS envelope amplifiers for the realization of high efficiency wideband LTE RF PA systems.

4.6 Acknowledgment

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Some of the material in this chapter is as it will appear in the following publications:

- M. Kwak, J. Jeong, M. Hassan, J. J. Yan, D. Kimball, P. M. Asbeck, and L. E. Larson, "High efficiency wideband envelope tracking power amplifier with direct current sensing for LTE applications," submitted to *IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*, 2012.
- M. Kwak, J. Jeong, M. Hassan, J. J. Yan, D. Kimball, P. M. Asbeck, and L. E. Larson, "Design of a high efficiency CMOS envelope amplifier with direct current sensing for handset RF power amplifiers," to be submitted to *IEEE Transactions of Microwave Theory and Techniques*, 2012.

The contributions from the co-authors are appreciated. The dissertation author was the primary researcher and the first author listed in these publications.

Chapter 5

Conclusion

For modern wireless communications, power amplifiers must provide output powers of several hundreds milli-watts for mobile-stations, and up to tens of watts for base-stations. The generation of high output power leads to a high DC power consumption, thus, the power consumption of transceivers is mainly determined by the power amplifier in the transmitter. In this reason, high efficiency RF power amplifier is critical in the modern transmitter design. In the traditional fixed supply voltage approach for a power amplifier, the efficiency is degraded at a large back-off to meet tight linearity requirements. By superimposing the envelope signal at the drain such that the RF amplifier operates consistently closer to saturation, the overall efficiency is improved and the generated heat is reduced dramatically. Due to the low breakdown voltage of the CMOS transistors, the high voltage envelope amplifier has been implemented with discrete components with high voltage process. Compared to these discrete solutions, an integrated circuits implementation for the envelope amplifier brings many benefits.

Hence, this dissertation focused on

- Presenting an architecture for high-voltage monolithic envelope amplifier in a BiCMOS DMOS technology for micro-base station RF power amplifier appli-

cations

- Presenting an wideband high-efficiency monolithic envelope amplifier in a CMOS technology for LTE mobile-stations.
- Implement the complete envelope tracking system to demonstrate wideband high-efficiency envelope tracking power amplifiers

First, a new high performance BiCMOS DMOS monolithic envelope amplifier is presented for the micro base-station applications. The design of monolithic envelope amplifiers for high voltage ($V_{DD} = 15$ V) envelope tracking applications, and the design techniques to solve the reliability issues with thin gate oxide is described. The overall envelope tracking system employing a GaN-HEMT RF transistor, and fully integrated high voltage envelope amplifier with a $0.35\mu\text{m}$ BiCMOS DMOS process, is demonstrated. The overall drain efficiency of the ET system is 51% at 34 dBm output power with an average high voltage envelope amplifier efficiency of 72%, and the linearity requirements are met after memory-effect DPD for a WCDMA signal with a PAPR of 7.7 dB. The results make this architecture an attractive candidate for monolithic integration of a high-voltage envelope amplifier for micro base station RF power amplifier applications.

In the second part, a high-efficiency wideband envelope tracking power amplifier for mobile LTE applications will be presented. The CMOS envelope amplifier with hybrid linear and switcher is designed in a 150 nm CMOS process. The envelope amplifier employs direct sensing of the linear stage current to reduce the propagation delay in the switcher. The strategy is demonstrated to improve the efficiency of the complete envelope tracking power amplifier system. The measured average efficiency of the envelope amplifier shows 78% and 73% with a 5 MHz and 20 MHz LTE signal respectively. The

envelope tracking power amplifier for a 5 MHz LTE including a GaAs HBT-based RF stage has overall power-added efficiency (PAE) above 46% with an average LTE output power of 27.6 dBm and a gain of 26.5 dB. These results demonstrate the great potential of CMOS envelope amplifiers for the realization of high efficiency wideband LTE RF PA systems.

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