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Pipeline ADC Design Methodology

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by

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To my parents for all the support.

In memory of my grandmother.

ABSTRACT OF THE DISSERTATION

Pipeline ADC Design Methodology

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Demand for high-performance analog-to-digital converter (ADC) integrated circuits (ICs) with optimal combined specifications of resolution, sampling rate and power consumption becomes dominant due to emerging applications in wireless communications, broad band transceivers, digital-intermediate frequency (IF) receivers and countless of digital devices. This research is dedicated to develop a pipeline ADC design methodology with minimum power dissipation, while keeping relatively high speed and high resolution.

Pipeline ADC is a mixed-signal system, which consists of sample and hold amplifier (SHA), sub-ADC, multiplying digital-to-analog Converter (MDAC) and bandgap voltage reference, comparator, switch-capacitor circuits and biasing circuits. This project set up a pipeline ADC design flow. It links all the specifications between the

system levels and circuit levels together. With this design flow, if the overall ADC specifications are given, such as resolution, sampling rate, voltage supply and input signal range, all the sub-block circuitry specifications are achieved.

This paper studies all the sub-block circuits of pipeline ADC first, and then come up with all the constraints and limitations for all the circuitry in term of speed and noises. Then a system level speed and power trade off consideration is explored in order to optimize the overall performance.

As verification of the proposed design methodology, a 10-bit 40MHz pipeline analog-to-digital converter prototype is developed in commercial TSMC 90nm CMOS technology: using op-amp sharing, dynamic biasing methods, it works in two modes: pipelined ADCs for high speed, cyclic ADC for low speed (only last stage runs, other stages are power off to save power). For pipeline mode, the total power consumption decrease as the sampling frequency drops.

Index terms: pipeline ADC, design methodology, CMOS, mixed-signal circuits

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List of Symbols and Abbreviations

Abbreviations	Definition
ADC	Analog-to-Digital Converter
BER	Bit Error Rate
BGR	Band-gap Reference
CMFB	Common-Mode Feedback
DAC	Digital-to-Analog Converter
DNL	Differential Non-Linearity
DR	Dynamic Range
DSP	Digital Signal Processing
ENOB	Effective Number Of Bits
FS	Full Scale
IF	Intermediate Frequency
INL	Integral Non-Linearity
LSB	Least Significant Bit
MDAC	Multiplying Digital-to-Analog Converter
MSB	Most Significant Bit
RF	Radio Frequency
SC	Switched Capacitor
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion

CHAPTER 1

INTRODUCTION

1.1 Motivation of ADC

In recent years, with the extensive implementation of digital computing and signal processing in communications, instrumentation, image processing and industrial control, analog to digital and digital to analog conversion applications in the field is expanding rapidly. Monolithic integration of technology, the novel circuit structure of integrated circuits, and advances in technology made the analog to digital and digital to analog conversion circuit design a great change, and continue to generate new areas of research and development.

At present, the electronic systems are in a trend of increasingly digitalization. Digital circuits and digital processing is almost everywhere. The main reason is: compared to the analog circuits, digital circuits with low noise sensitivity, strong anti-interference ability, high stability and wide adaptability, easy to design and automated testing, more extensive programmability features, but also because of advances in integrated circuit technology to continuously improve the performance of digital circuits. Large-scale integration (VLSI) technology allows each new generation of digital circuits to achieve higher speed, more features per chip, lower power consumption and cost. In addition, the progress of the improvement of the circuit structure and computer-aided

design (CAD) analysis and synthesis tools also promote the development of digital integrated circuits.

Although digital circuits advantages, and in many areas, it is gradually replacing analog circuit, but the physical environment of our existence cannot be separated from analog signal processing. First, the signals appearing in nature are almost always analog, such as temperature, pressure, time, speed, voltage, current, voice, luminous flux, etc. Secondly, the way of human perceives and keeps information is the analog mode.

In order to establish the interface of the digital processor and the analog world, data acquisition and reconstruction of the circuit is necessary. Therefore, Analog-to-Digital Convertor (ADC) and Digital-to-Analog Convertor (DAC) is very important and irreplaceable (Shown in Figure 1.1).

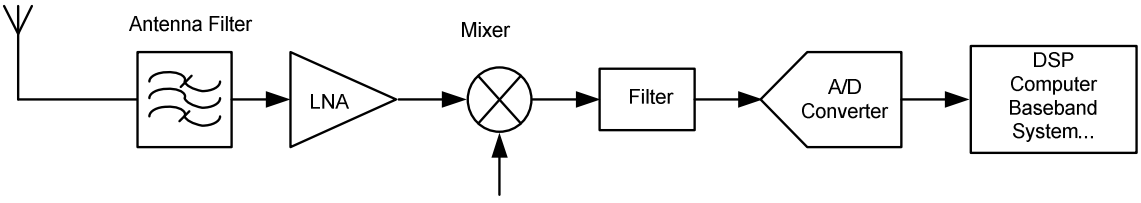


Figure 1.1 ADC in the Interface between Analog and Digital World.

ADC is a device that convert analog input signal into digital output signal. With the rapid development of digital computing and signal processing in electronic systems in the past few decades, it virtually transferred the world into a digital era. For a long time, as the bridge between the real analog world and the digital world, Analog-to-Digital Converters (ADCs) have been developed in different uni-directions to meet different

application requirements. Over-sampling sigma-delta ADCs, successive approximation ADCs and algorithmic ADCs pushing the resolution up to 24bits, traded off with the limited bandwidth, are widely employed in audio communication; Flash and folding and interpolating ADCs, featuring highest speed at the cost of low resolution (no more than 10-bit) and large power dissipation and area, are adopted in disk drive channels and magnetic data storage systems. Since 1990s, high-performance ADC ICs with optimized combined specifications of resolution, sampling rate and power consumption (as opposed to individual improvement) are in demand. For example, the IF frequencies in a typical direct-IF (intermediate frequency) receiver vary from 50MHz to 200MHz, which requires an ADC sampling rate up to 400MHz. Practically, the signal-to-noise ratio (SNR), dynamic range and linearity requirements suggest that a better than 14 bits resolution is necessary at affordable power dissipation. In addition, soft radio is proposed to digitize signal at radio frequency (RF) domain and sort everything to the powerful digital signal processing (DSP) IC chip, in order to bypass the obstacle originated from different wireless standards. The critical building block in soft radio is the high sensitivity (that is high SNR and high spurious free dynamic range (SFDR) ADC, with sampling frequency being pushed further to several Giga-Hertz and relatively lower power consumption, since the ADC must share the power budget with the other functional blocks in the same transceiver system.

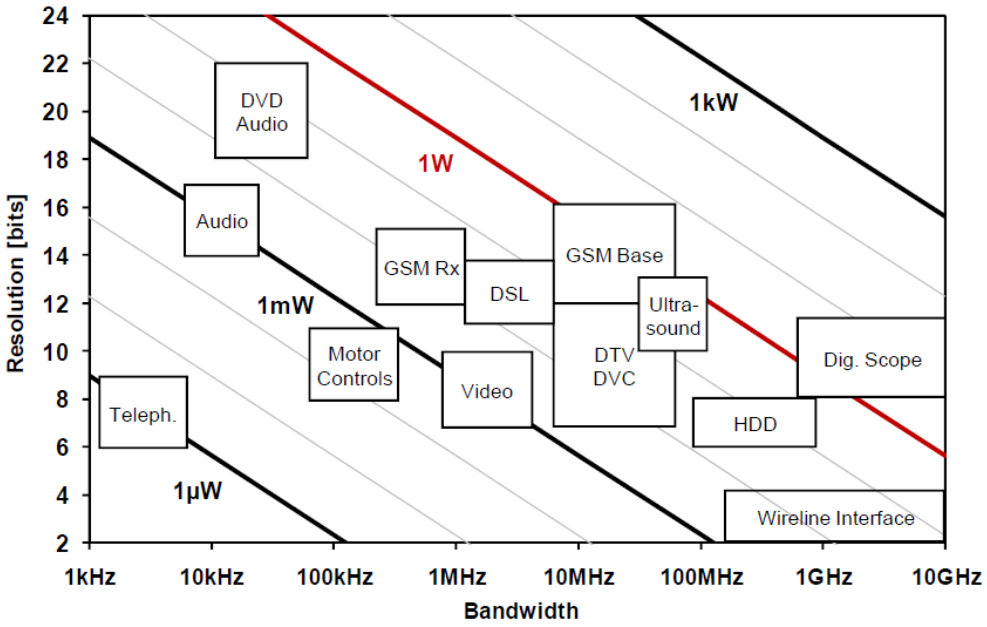


Figure 1.2 ADC Applications.

Market investigation results (shown in Figure 1.2) coming from commercial products of ADC manufactures (Analog Devices Inc.) indicate that ADC are widely used in many areas, such as communication, audio, computer, UWB, also the speed of ADC varies from less 100kHz to over GHz and the resolution varies from 6 to 22bits. To join with IC industry, this research focuses on the pipeline ADC whose resolution is 8~14bits and speed is 100k~200MHz in the mainstream CMOS process.

1.2 A/D Conversion Overview

1.2.1 ADC Definition

As the interface between the real world signals and the digital codes, ADCs play a major role in the data acquisition and digitizing process. ADC convert continuous change of analog signal with amplitude and time into digital signals, which are discrete changes in the amplitude and time. Shown in Figure 1.3 is a block diagram of this process. Figure 1.3 shows the block diagram of an ADC, which consists of three building blocks – sampler, quantizer and coder. Input signals are converted to discrete time sampled signal by the sample circuit under the sampling clock control. Hold circuits play the role of the circuit to maintain the sampled value unchanged in the transformation process.

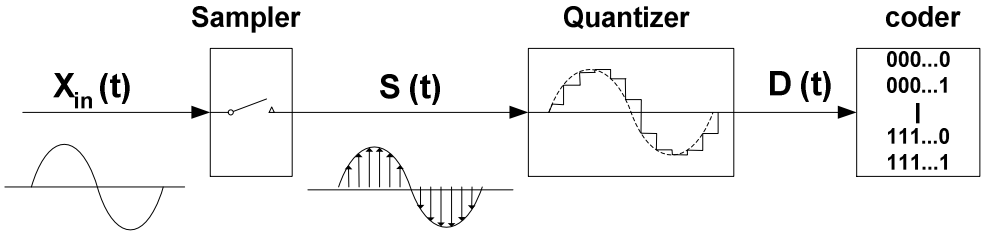


Figure 1.3 Analog-to-Digital Converter Block Diagram.

Sampler discretizes analog signal in time domain. The discrete-time continuous-amplitude signal is then mapped into a discrete level by quantizer, which implements a many-to-one transformer by approximating the signal to one of sub-divided quantization levels. Uniform quantization provides the minimum quantization error for a statistically equally distributed signal, while non-uniform quantization is a better choice for signals,

such as audio one, whose amplitude is not evenly distributed in the input range. For both the uniform and non-uniform quantization, a unique digital code is assigned to each quantization level. The analog-to-digital conversion process is fulfilled by providing a series of digital codes to represent the time-discrete and amplitude-discrete analog signal.

1.2.2 Main design direction of ADC performance

The first thing is high-speed. As the bandwidth of the signal source needs to be digitalized became wider and wider, so the audio, video, and RF ADC converters have to work at higher sampling rate.

Second is high-precision. Due to the growing dynamic range of the signal source needs to digitize, people have increasingly high quality requirements of data processing, so the accuracy of the converter continues to increase.

Third, it is easy for monolithic integration. At present, low-cost, low power consumption and high reliability of monolithic integration of the system on-chip system (SOC) has become a trend. Complete electronic systems are often mixed-signal systems, including digital circuits, analog circuits, analog to digital and digital to analog conversion circuit.

1.2.3 ADC Characterization

ADC performance is characterized by resolution, speed, power, INL, DNL and so on. It can be divided into two parts: static features and dynamic feature.

Resolution: ADC resolution is defined as the minimum input signal to make a change at digital output, usually expressed as the number of bits n of the output binary code. The resolution shows the resolving ability of the input signal. Theoretically, for an n-bit ADC, the minimum input voltage that can be resolved is VREF/2^n, equivalent to a quantitative unit of input voltage. Another term, called effective number of bits (ENOB), therefore, is introduced to measure the resolution for a pure sinusoidal signal accurately. It is defined as

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.1}$$

where SNDR represents signal-to-noise and distortion ratio.

- Quantization error (or quantization noise) is the difference between the original signal and the digitized signal. Hence, The magnitude of the quantization error at the sampling instant is between zero and half of one LSB. Quantization error is due to the finite resolution of the digital representation of the signal, and is an unavoidable imperfection in all types of ADCs.

- Differential Non-linearity (DNL). DNL error is defined as the difference between an actual step width and the ideal value of 1LSB (see Figure 1.4). For an ideal ADC, in which the differential nonlinearity coincides with DNL = 0LSB, each analog step equals 1LSB (1LSB = VFSR/2^N, where VFSR is the full-scale range and N is the resolution of the ADC) and the transition values are spaced exactly 1LSB apart. A DNL error specification of less than or equal to 1LSB guarantees a

monotonic transfer function with no missing codes. An ADC's monotonicity is guaranteed when its digital output increases (or remains constant) with an increasing input signal, thereby avoiding sign changes in the slope of the transfer curve.

- Integral Non-linearity (INL). INL error is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function from a straight line. The INL-error magnitude then depends directly on the position chosen for this straight line. At least two definitions are common: best straight-line INL and end-point INL. It is defined as the deviation of any single step from the ideal size and measured in LSBs. A less than $\pm 1 LSB$ DNL error and less than $\pm \frac{1}{2} LSB$ INL error specification guarantees no missing codes and a monotonic transfer function.

- Offset Error. Offset error identifies the horizontal difference between the actual transfer curve and the ideal one at the lowest transfer level. It is a figure-of-merit that measures the transfer curve matching at a single point and indicates the average error of the converter.

- Gain Error. Gain error, given as a percentage of the ideal input full-scale range, is reflected in the input/output transfer function as the slope deviation from the infinite resolution characteristic. Comparing with offset error, which can be measured at 1½ LSB above the most-negative end, gain error may be estimated at

1½ LSB below the most-positive end. Linear gain error doesn't introduce distortion as does nonlinear gain error.

Figure 1.4 demonstrates the static errors in the same ADC transfer curve.

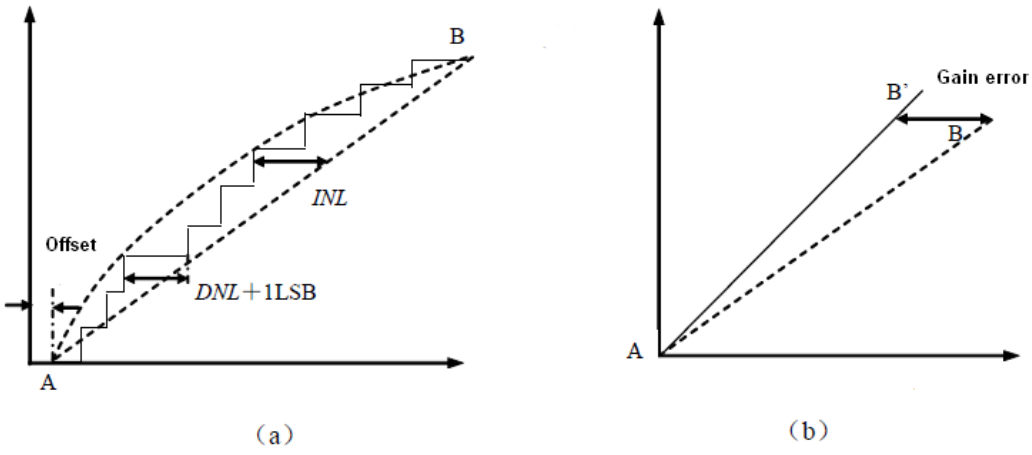


Figure 1.4 ADC Static Errors.

Speed: Analog-to-digital conversion speed is characterized by input bandwidth and sampling rate, which is defined as how many times the input analog signal is sampled per second and determined by the transient response parameters, such as settling time, slew rate and aperture jitter, of the internal blocks located in the analog signal path. The primary elements in the speed performance matrix are explained in this section.

· Aperture jitter. When the input signal has large slewing rate, all the SNR of S/H circuit will decrease because of the special problem introduced by jitter issue from sampling clock. In order to get the relationship between the maximum allowable slewing rate and sampling rate, as well as resolution, let's consider that the voltage uncertainty of the input signal caused by clock jitter is less than 1LSB, so the jitter

impact could be ignored. For a full scaled input signal $\mathrm{Vin} = \mathrm{Asin}\,2\pi\mathrm{ft}$, its maximum changing rate is $2\pi fmaxA$, so:

$$2\pi fmaxA \times \Delta t < 1LSB \tag{1.2}$$

$$2\pi fmaxA \times \Delta t < \frac{2\mathrm{A}}{2^n} \tag{1.3}$$

- Total harmonic distortion (THD). THD is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics (generally, only the first 5 harmonics are significant). THD of an ADC is also generally specified with the input signal close to full-scale, although it can be specified at any level.

- Signal-to-Noise Ratio (SNR). SNR (or sometimes called SNR-without-harmonics) is calculated from the FFT data the same as SINAD, except that the signal harmonics are excluded from the calculation, leaving only the noise terms. In practice, it is only necessary to exclude the first 5 harmonics, since they dominate. The SNR plot will degrade at high input frequencies, but generally not as rapidly as SINAD because of the exclusion of the harmonic terms. A few ADC data sheets somewhat loosely refer to SINAD as SNR, so you must be careful when interpreting these specifications and understand exactly what the manufacturer means. In a well-designed and matching converter, SNR presents an upper limit to both the static and dynamic performance and is characterized by a single tone or a multi tone measurement with a full scale sinusoidal input as

$$SNR_{dB} = 6.02N + 4.77 - 20\log\frac{Signal\_peak\_amplitude}{Signal\_rms\_value} \quad (1.4)$$

Where N is the resolution of ADCs. If the signal level is reduced, the value of SNR decreases and the ENOB decreases. It is necessary to add a correction factor for calculating ENOB at reduced signal amplitudes as shown in Equation (1.4)

- Signal-to-Noise and Distortion Ratio (SNDR). SNDR is the ratio of the rms value of the fundamental signal to the mean value of the root-sum-square of its harmonics plus all noise components (excluding dc). The bandwidth over which the noise is measured must be specified. In the case of an FFT, the bandwidth is dc to fs/2. (If the bandwidth of the measurement is dc to fs/2 (the Nyquist bandwidth), THD + N is equal to SINAD—see below). Be warned, however, that in audio applications the measurement bandwidth may not necessarily be the Nyquist bandwidth. The SINAD plot shows that the ac performance of the ADC degrades due to high-frequency distortion and is usually plotted for frequencies well above the Nyquist frequency so that performance in undersampling applications can be evaluated. SINAD plots such as these are very useful in evaluating the dynamic performance of ADCs.

- Spurious Free Dynamic Range (SFDR). Spurious free dynamic range is the ratio of the rms value of the signal to the rms value of the worst spurious signal regardless of where it falls in the frequency spectrum. The worst spur may or may not be a harmonic of the original signal. SFDR is an important specification in communications systems because it represents the smallest value of signal that

can be distinguished from a large interfering signal (blocker). SFDR can be specified with respect to full-scale (dBFS) or with respect to the actual signal amplitude (dBc).

Figure 1.5 illustrates the relationship among these dynamic parameters.

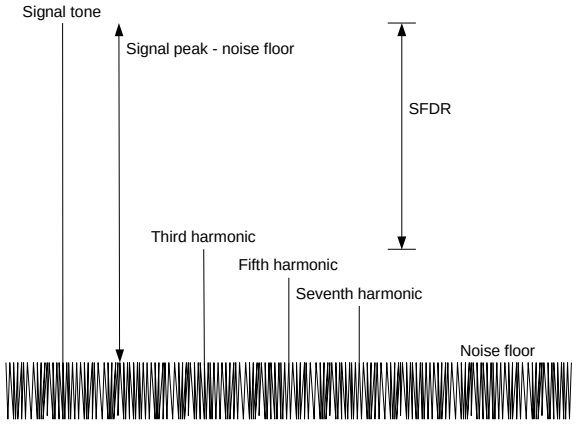


Figure 1.5 ADC Dynamic Parameters.

CHAPTER 2

ADC was first boosted in 1930s because of widely used PCM (Pulse Code Modulation) technology in telecommunication area. It changed the analog coding and decoding technology into digital signal processing technology. Until 1950s, with the emergence of high-speed digital computer and aircraft/missile data processing system, ADC has gained a further development.

After Microprocessors were well-developed in 1970s, it triggered a technological revolution in the field of digital signal processing and computer. In 1971, the first Monolithic ADC was designed as analog/digital interface circuitry. In the past 20 years, due to deep sub-micron integrated technology becomes more popular; it promotes a new area of analog integrated circuits: mixed signal integrated circuit. This chapter will briefly introduce all typical ADC, such as flash ADC, two-step ADC, pipline ADC and so on.

OVERVIEW OF ADC

2.1 AD Classification

According to relationship between sampling rate and signal frequency, ADC can be divided into three types: the Nyquist ADC, subsampling ADC, and oversampling ADC.

Nyquist ADC: in order to ensure accurate reconstruction of the original value theoretically, ADC must comply with the sampling theorem, the sampling frequency is greater than or equal to twice the highest frequency of the input signal. Since anti-aliasing filter cannot be an ideal low-pass characteristics, there must be a transition band, so the sampling frequency slightly higher than twice the bandwidth of the analog signal.

Sub-sampling ADC: input signal only occupies a small part of the band pass frequency, it is possible to make the sampling frequency smaller than the highest signal frequency, but to ensure that the sampled spectrum do not overlap.

Oversampling ADC, the sampling frequency is much higher than the Nyquist frequency. The following part of the digital filter circuit is used to remove noise outside the signal bandwidth. Oversampling technique can reduce the quantization noise level, in order to achieve high-precision.

According to performance, ADC can be divided into high-speed AD converter, and high accuracy AD converter.

Based on architecture differences, ADC can be divided into the serial structure (pipeline), parallel structure (time-interleaving), and serial and parallel AD converter.

2.2 Flash AD Converters

Flash converters are extremely fast compared to many other types of ADCs. It is also quite simple and, apart from the analog comparators, only requires logic for the final

conversion to binary. It can achieve extremely high speed (over 1Gsamples/second) with low resolution.

The typical structure of a 2bit flash ADC is shown in Figure 2.1. A Flash converter requires a huge number of comparators compared to other ADCs, especially as the precision increases.

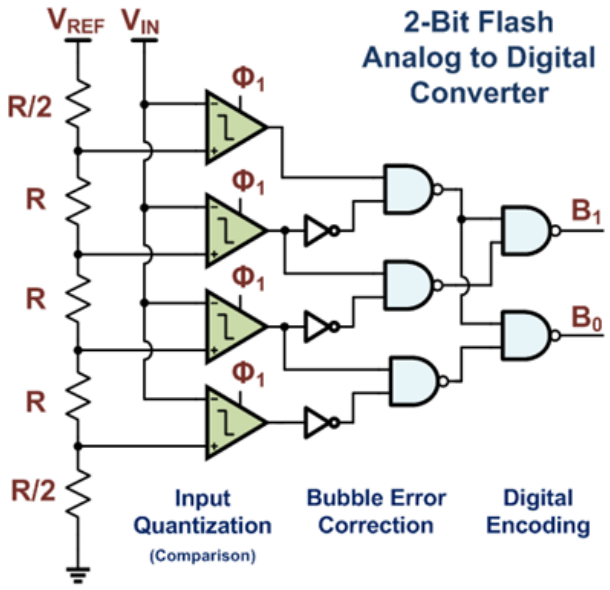


Figure 2.1 A Typical Structure of A Flash ADC.

An N-bit flash ADC needs a resistor ladder composing 2^N equal resistors. These resistor ladders generate all possible 2^N-1 voltage levels, then followed by2^N-1 comparators and digital encoders. Comparators are usually composed of a pre-amplifier used for sampling and amplifying the input signal, and a latch used for making final decision.

Each comparator samples the input signal and compares this signal to the reference voltage. Then the comparator generates a digital output “1” or “0” indicating whether the input signal is larger or smaller than the reference voltage assigned to that comparator. The digital outputs of the comparators are often referred to as thermometer codes, and these codes are encoded as 1-of-n codes. Finally, 1-of-n codes are converted to binary outputs.

This ADC requires a lot of the comparator, and thus the hardware cost of the power, area and other large input capacitance. Its resolution is limited by the accuracy of the reference voltage and the offset voltage of the comparator. For CMOS technology, it also need to trade-off between the small offset voltage and high conversion speed. Therefore, the structure is more commonly used in the occasion of the 6 ~ 8 precision. Flash ADC is the most classic high-speed AD converter, and other structures in the high-speed AD converter are evolved on this basis.

The flash AD converter key weakness is that the hardware cost has grown exponentially with the resolution. The number of comparators is 2^n-1. When the resolution is 8 or more, it requires very large power and area. Also, because the heavy used comparators and lack of front end sample and hold amplifier, it will bring some special non-ideal characteristics, such as the variations of the ladder reference voltage, the interference immunity of signal glitches variation, the sensitivity of sampling point of different input signal slew rate. These issues will impact the conversion accuracy.

When the difference between two input signals of the comparator is relative small, it will take longer period of time to go through in order to decide a stable logic output. This condition is called comparator metastability. If the instantaneous value of the input signal value of flash AD converter is very close to one of comparators reference voltage, then the comparator output will be a long time uncertain, may bring the wrong digital output.

We can take some approaches to reduce the probability of occurrence of metastable error. For example: adding the number of latch behind each comparator, so as to allow a longer time to rebuild the thermometer code, which is a simple solution, but the power consumption is higher. Thermometer code to binary decoding using pipelining mothed is another way; this method allows the output of the comparator to experience more reconstruction time, but each comparator output level as the input of a logic gate. In addition, using Gray code between thermometer code and binary code can also effectively inhibit the comparator metastability error. In Gray coding circuit, the input signal does not appear in more than one input gate,, allowing to increase the time of reconstruction with pipelining.

2.3 Two-Step Flash ADC

Because of the exponential growth of power dissipation, area, and input capacitance of a flash convert makes it impractical for resolution above 8 bits. Therefore,

trades-offs should be made between the resolution and the conversion rate. A two-step flash ADC is applied to trade speed for power dissipation and resolution.

A two-step flash ADC consists of a coarse flash ADC stage, a DAC, a subtractor and a fine flash ADC stage. Normally, a front-end sample-and-hold circuit and an inter-stage gain amplifier between the subtractor and the fine flash ADC are necessary. The block diagram in Figure 2.2.1 illustrates the structure of a two-step flash ADC.

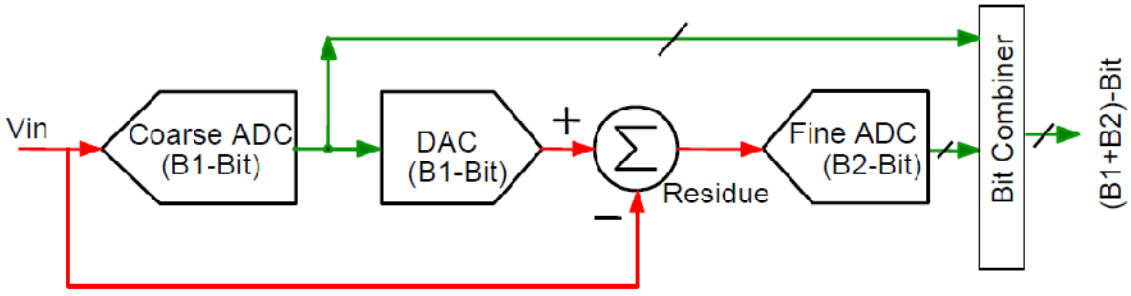


Figure 2.2 Two-Step Flash ADC.

In this type of ADC, the conversion takes two steps. During the first step, the most significant bits of the digital output are determined by the first stage flash ADC. Then a DAC converts this digital result back to an analog signal to be subtracted from the input signal. This residue is amplified by the inter-stage gain amplifier and then sent to the second stage flash ADC. The second stage flash determines the least significant bits of the digital output.

The resolution of the first coarse flash ADC is m bit, and that of second fine flash ADC is n bit. So the total digital output result ion is m+n. If digital correction is used, one of the flash ADC need residual bit, so the total resolution is larger m (or n) bit but smaller

than m+n bit. In flash ADC, comparators track the input signal for half of the sampling period, while make conversion for the other half of sampling period. However, for two-step ADC, because of extra DA conversion, subtraction, and second flash ADC work at same time, the speed of two-step ADC is limited.

The key principle of a two-step flash ADC is to amplify the residue of the coarse ADC, and this will largely reduce the number of comparators. Although the speed the two-step ADC is lower than flash ones. But the number of comparators is much smaller than that of flash ADC with same resolution: from 2^{n+m}-1 to $2^{n}+2^{m}$-2. So the power and area are decreased.

2.4 Oversampling AD Converters

An oversampling converter uses a noise-shaping modulator to reduce the in-band quantization noise to achieve a high degree of resolution. It can shape the quantization noise and push the majority of the inband noise to higher frequencies. It modulates the analog input signal to a simple digital code, normally a one-bit serial stream using a sampling rate much higher than the Nyquist rate.

To understand noise shaping, consider the block diagram of a sigma-delta modulator of the first order (Figure 2.3). It includes a difference amplifier, an integrator, and a comparator with feedback loop that contains a 1-bit DAC. (This DAC is simply a switch that connects the negative input of the difference amplifier to a positive or a negative reference voltage.) The purpose of the feedback DAC is to maintain the average output of the integrator near the comparator's reference level.

The density of "ones" at the modulator output is proportional to the input signal. For an increasing input the comparator generates a greater number of "ones," and vice versa for a decreasing input. By summing the error voltage, the integrator acts as a low-pass filter to the input signal and a high-pass filter to the quantization noise. Thus, most of the quantization noise is pushed into higher frequencies. Oversampling has changed not the total noise power, but its distribution.

If we apply a digital filter to the noise-shaped delta-sigma modulator, it removes more noise than does simple oversampling. This type of modulator (first-order) provides a 9dB improvement in SNR for every doubling of the sampling rate. For higher orders of quantization, we can achieve noise shaping by including more than one stage of integration and summing in the sigma-delta modulator.

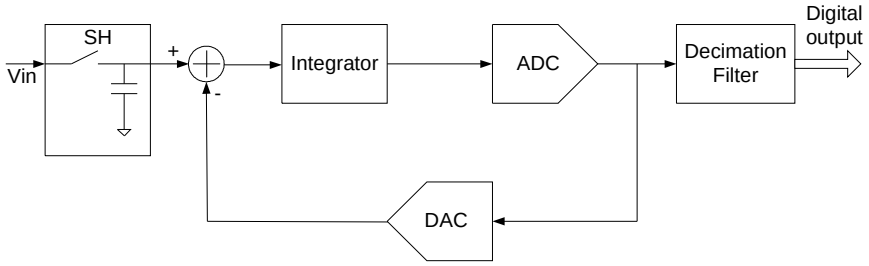


Figure 2.3 First Order Sigma-Delta ADC.

The oversampling ratio, called M, is a ratio of the clock frequency to the Nyquist frequency of the input signal. This oversampling ratio can vary from 8 to 256. The resolution of the oversampled converter is proportional to the oversampled ratio. The bandwidth of the input signal is inversely proportional to the oversampled ratio.

It is Very compatible with VLSI technology because most of the converter is digital High resolution. Single-bit quantizers use a one-bit DAC which has no INL or DNL errors. Provide an excellent means of trading precision for speed (16-18 bits at 50ksps to 8-10 bits at sampling rates of 5-10Msps).

Oversampled ADCs allow signal bandwidth to be efficiently traded for resolution. Noise shaping oversampled ADCs preserve the signal spectrum and shape the noise quantization spectrum. The modulator shapes the noise quantization spectrum with a high pass filter. This high-pass characteristic reduces the noise at low frequencies which is the key to extending the dynamic range within the bandwidth of the converter. The quantizer can be single or multiple bits. Single bit quantizers do not require linear DACs because a 1 bit DAC cannot be nonlinear. Multiple bit quantizers require ultra linear DACs. Modulators consist of combined integrators with the goal of high-pass shaping of the noise spectrum and cancellation of all quantizer noise but the last quantizer

2.5 Pipelined ADC

The pipelined analog-to-digital converter (ADC) has become the most popular ADC architecture for sampling rates from a few megasamples per second (Msps) up to 100Msps. Compared to the two-step flash ADC which has just two stages, pipeline ADCs have multiple cascades stages.

Resolutions range from eight bits at the faster sample rates up to 16 bits at the lower rates. These resolutions and sampling rates cover a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receivers, base stations, digital video (for example, HDTV), xDSL, cable modems, and fast Ethernet.

Applications with lower sampling rates are still the domain of the successive approximation register (SAR) and integrating architectures, and more recently, oversampling/sigma-delta ADCs. The highest sampling rates (a few hundred Msps or higher) are still obtained using flash ADCs. Nonetheless, pipelined ADCs of various forms have improved greatly in speed, resolution, dynamic performance, and low power in recent years.

Each stage of the pipeline ADC consists of a sample-and-hold circuit, a sub-ADC, a DAC, a subtractor and an inter-stage gain amplifier. The block diagram of a pipeline ADC is illustrated in Figure 2.4.

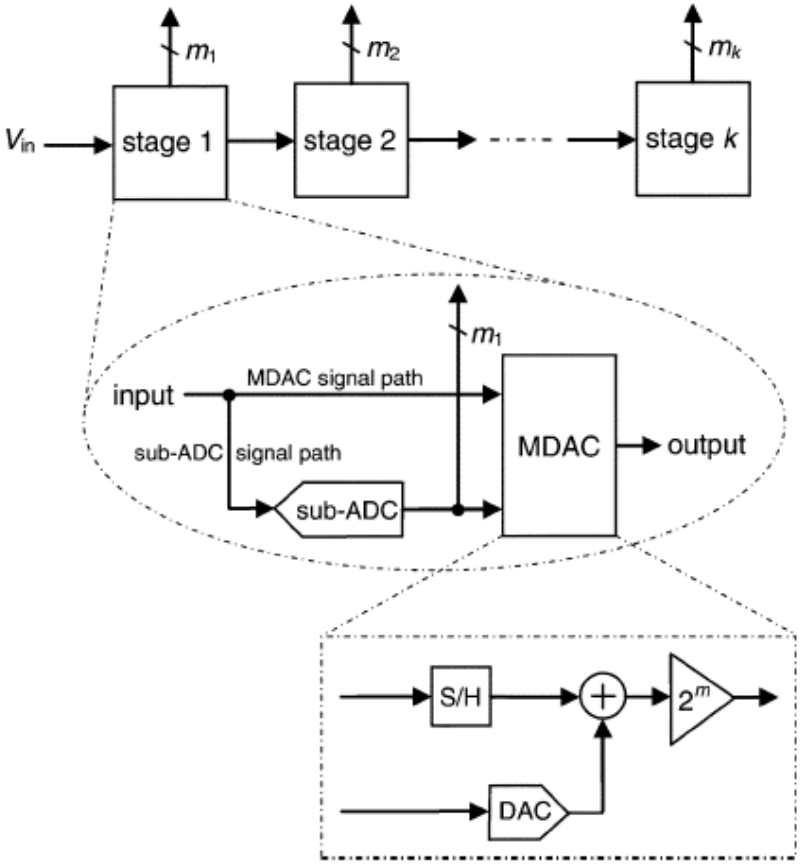


Figure 2.4 A Pipelined ADC.

In this schematic, the analog input, IN, is first sampled and held steady by a sample-and-hold (S&H), while the flash ADC in stage one quantizes it to n_1 bits. The n_1 bit output is then fed to a n_1-bit DAC, and the analog output is subtracted from the input. This "residue" is then gained up by a factor of G_1 and fed to the next stage (Stage 2). This gained-up residue continues through the pipeline, providing n_i bits per stage until it reaches the n_k-bit flash ADC, which resolves the last B_k bits. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-

correction logic. Note when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput.

The concurrency of the pipeline ADC makes the maximum conversion rate almost independent of the number of stages because the first stage determines the conversion rate, but there is a delay time since the signal must work through all stages before the complete digital outputs are generated. This delay could be an issue if the pipeline ADC is part of a feedback system [3]. In addition, the number of stages does have great impact on the noise performance, power dissipation, linearity and accuracy.

2.6 Summary of ADCs

Table 2.1 shows the differences of different ADCs. Flash ADC has the fast speed while lowest resolution. Oversampling (Sigma-delta) ADC can achieve over 20 bits resolution, but the sampling rate is lowest. Two-step flash ADC and pipeline ADC sit in the middle. However, pipeline ADC can get higher resolution but lower speech compared to two-step ADC.

So based on different application and requirement, ADC structure might not be the same. Flash ADC focus on radio, UWB, WiFi applications because of its high speed features. Two-step and pipeline ADC will be used for communication, video, image

sensor, and baseband systems. While oversampling ADC will be used for audio, communication, thermal sensing and precision test systems.

ADC	Resolution	SNR/dB	Fs/Hz	Power	Applications
Flash	4~6	30~46	>1G	higher	Radio, UWB, WiFi, high speed system
Two-step	8~10	44~60	500M	High	Communication, video
Pipeline	8~16	48~80	1M~200M	low	Communication, video, baseband system
Sigma-Delta	16~24	90~130	10M	lower	Audio, communications, precision test system

Table 2.1 Comparison of Different Types of ADCs.

CHAPTER 3

PIPELINE ADC BLOCK STUDY

Pipeline ADC uses two or more steps of subranging. First, a coarse conversion is done. In a second step, the difference to the input signal is determined with a digital to analog converter (DAC). This difference is then converted finer, and the results are combined in a last step. This can be considered a refinement of the successive-approximation ADC wherein the feedback reference signal consists of the interim conversion of a whole range of bits (for example, four bits) rather than just the next-most-significant bit. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size.

3.1 Basic Concept of Pipeline ADC

The principle of sub-ranging ADC can be pushed to the limit of having only one bit per stage. At this point, each flash ADC is nothing more than a simple comparator; also, the data is transferred in a pipeline fashion: when the data is sent to the second stage, another sampled data is fed to the first stage; the result is a latency delay equal to the number of stages. Since the pipeline ADC is pipelining the subranging structure, and the binary search in the sub-ADCs runs just as the mathematic division, the first stage decides the MSBs and the last stage sets the LSBs. The MSBs divide the full reference

range, while LSBs divide the sub reference range. The relationship between MSBs and LSBs is revealed in Figure 3.1.

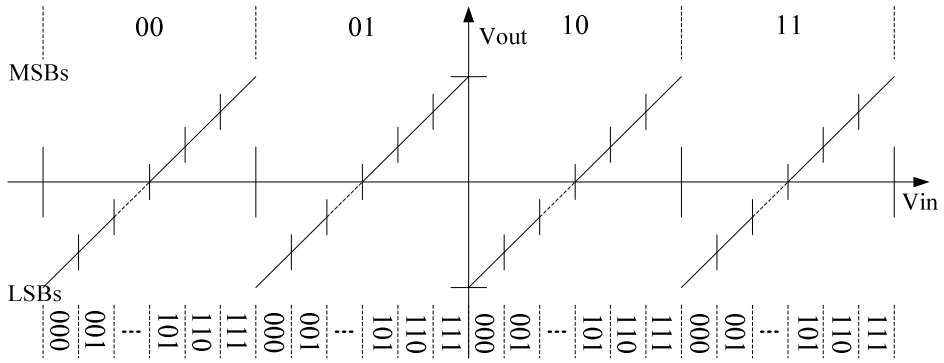


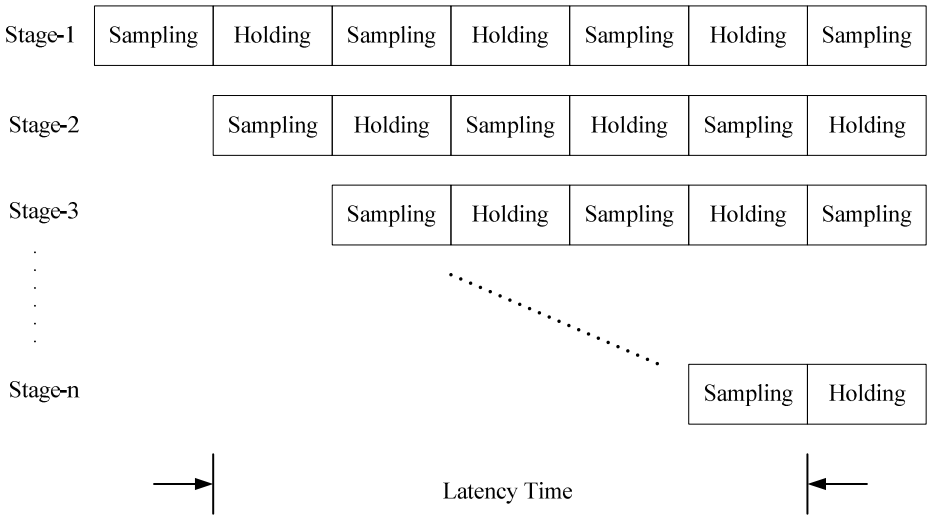
Figure 3.1 Pipeline ADC Transfer Curve.

A Pipeline ADC consists of a cascade of stages, each of which contains a low resolution ADC, DAC and amplifier, which successively convert the analog input into its digital representation, while processing the data in a pipe-lined manner.

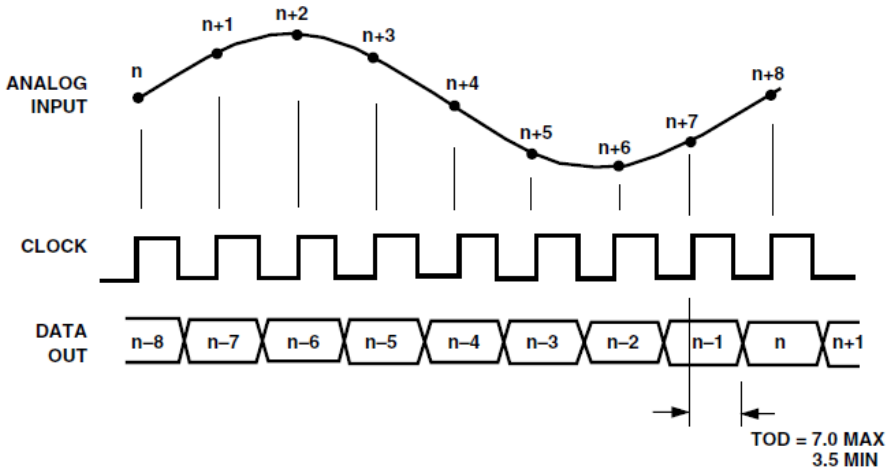
Pipeline ADCs are commonly used for power-efficient high-speed conversion of wide bandwidth input signals (e.g. 10 to 100 MHz). The ADC sampling frequency is usually the Nyquist frequency or lower using small OSRs (e.g. 2 or 4) and the ADC output code resolution is typically between 8 and 14-bit.

As a well-organized data processing system, the operation of the pipeline ADCs is under stringent timing control. Each stage performs data conversion in sampling and holding modes serially. The sampling and holding modes interleave between two adjacent stages and the digital output is valid after some clock cycles, called latency time, decided by the number of stages. This process is illustrated in Figure 3.2(a). Because

each sample must propagate through the entire pipeline before all its associated bits are available for combining in the digital-error-correction logic, data latency is associated with pipelined ADCs. In the example in Figure 3.2(b), this latency is about seven cycles.



(a)



(b)

Figure 3.2 (a) Stage Operation Modes in Pipeline ADC (b) data latency in pipeline ADC.

This timing scheme of the pipeline ADC is built up by the sample and hold circuit in each stage. During sampling mode, the switch controlled by the sampling clock is connected to the residue generated from the preceding stage and the signal is sampled on the sampling capacitor. When the hold clock comes, the switch is turned off and the signal stored on the sampling capacitor on one hand is converted to the thermometer codes by the sub-flash ADC, on the other hand, subtracts the estimated analog signal that is re-constructed by the D/A converter, to create the new residue as the input signal of the following stage. The thermometer codes from each stage are encoded to the binary ones and latched and added together to form the final m-bit digital output (where m is the resolution of the pipeline ADC) .The detailed pipeline architecture is shown in Figure 3.3.

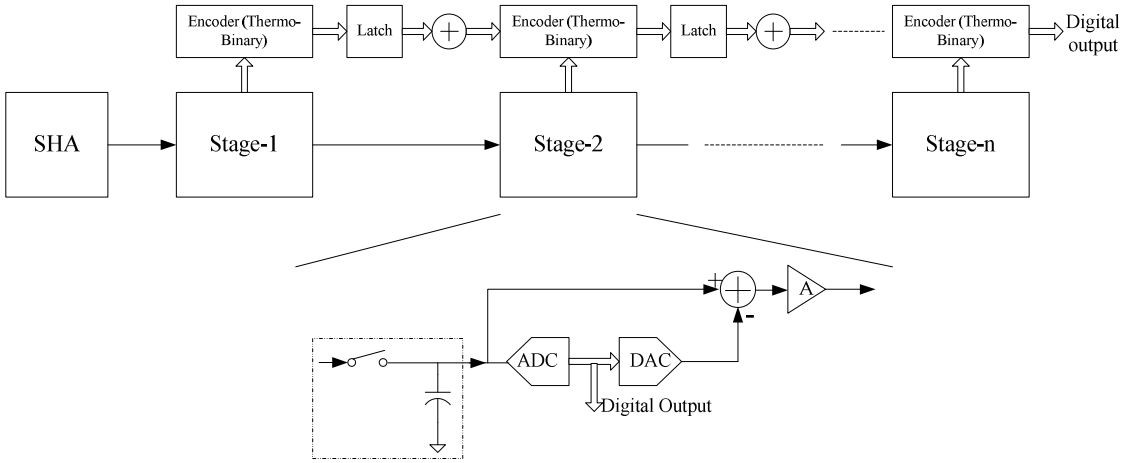


Figure 3.3 Detailed Pipeline ADC Architecture.

Pipeline ADC design includes system level design and block level design. For system level consideration, it consists of architecture, stages partition, power optimization, specification of sub-block circuits. Designer should consider what kind of

architecture the pipeline ADC should be: op-amp sharing, S/H circuits, dithering or not, how many bit one stage of MDAC should handle, how to minimize power and what the specification of sub-block should be, like op-amp DC gain and close-loop gain bandwidth.

So, it's a complex design trade-off matrix among resolution, thermal noise, power, input range, voltage supply, op-amp types, nonlinearity, and so on. It is shown on Figure 3.4. This work comes up with an optimized methodology of pipeline ADC design trade-off and finds all the connection among these important features. For example, as resolution increase, the requirement of thermal noise, which is related to KT/C, also become tight (SNR also increase). So as to minimize thermal noise, the sample capacitance in MDAC will increase; however, it will burn more power. If the input range goes up, the requirement of thermal noise will drop, but the selection of op-amp becomes to be one dominant issue.

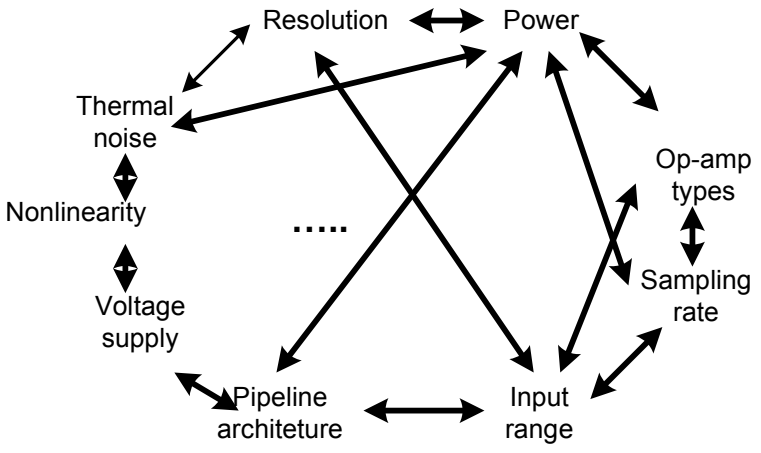


Figure 3.4 Pipeline ADC Design Matrix.

So, the methodology study of pipeline ADC design flow shows as following figures 3.5.

1.) Before designing pipeline ADC, first thing to know all the specification of ADC, like resolution, input signal range, maximum sampling rate, voltage supply and so on.
2.) Then, decide what kind of ADC architecture will be used, number of stages, sampling capacitor value.
3.) Define the block level circuits specification based on the first two steps. Like op-amp types, DC gain, closed-loop gain bandwidth, switch selections and so on.
4.) Design and simulation the block level circuits to beat the specification.
5.) Design and simulation the top level ADC.
6.) Run post simulation and corner, Monte Carlo simulation.
7.) If everything passes, the layout could be tape-out.

All the block level design is important, so we first study the block level circuits and will discuss the system level power optimization in the following chapter.

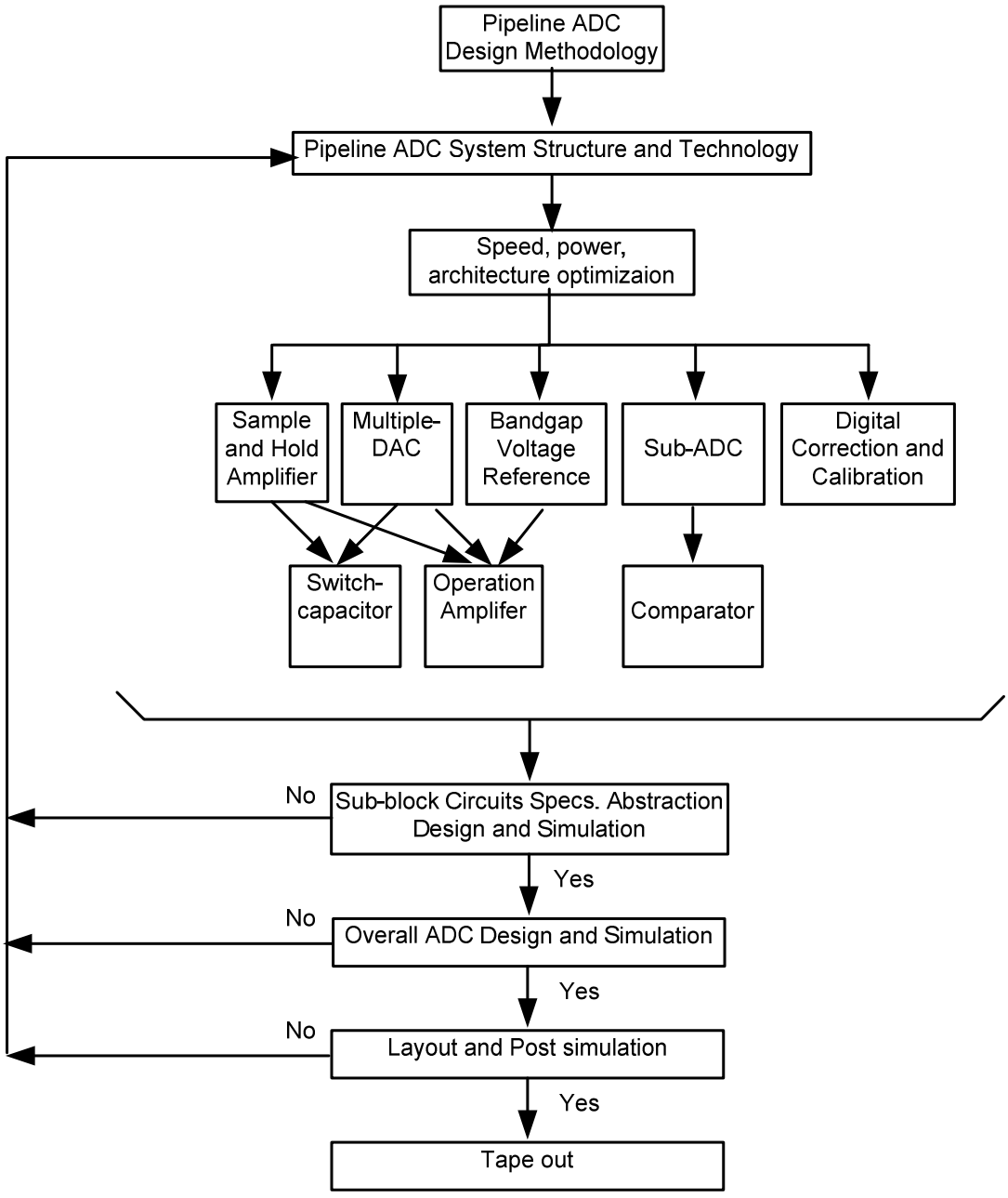
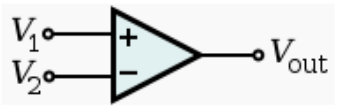


Figure 3.5 Pipeline ADC Design Flow.

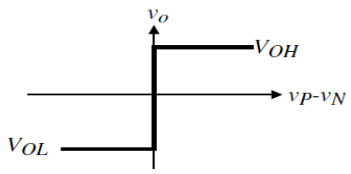
3.2 Comparator

A comparator is a device which compares two voltages or currents and switches its output to indicate which is larger. The most widely used ADCs process voltage signal, so here we only discuss voltage comparator. Its symbol is in figure 3.6 (a) and its ideal transform function is figure 3.6(b).

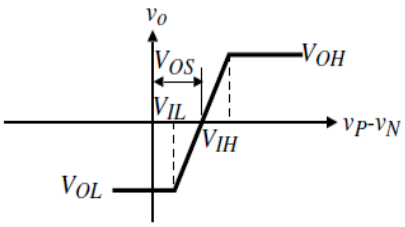


$$V_{out} = \begin{cases} V_{S+} & V_1 > V_2 \\ V_{S-} & V_1 < V_2 \end{cases}$$

(a)



(b)



(c)

Figure 3.6 (a) Comparator Symbol (b) Ideal Transform Function

(c) Practical Transform function.

The important Specifications of voltage comparator are gain A_V, offset V_{OS}, speed (step response), kickback noise and power consumption. The gain of ideal comparator is infinite, however the practical comparator gain is:

$$A_V = \frac{V_{OH}-V_{OL}}{V_{IH}-V_{IH}} \quad (3.1)$$

V_{OS} is the input voltage necessary to make the output equal to half of (V_{OH}+V_{OL}) when V_P=V_N. Comparator speed, kickback noise and power issue will be discussed in details in the following sections. There are mainly two type of voltage comparator: amplifier-type comparator and Latch-type comparator which is also called regenerative comparator.

3.2.1 Amplifier-type comparator

The natural choice to design a comparator is to use an amplifier. A small voltage at the input is then amplified to a value large enough to be detected by the following digital logic circuits.

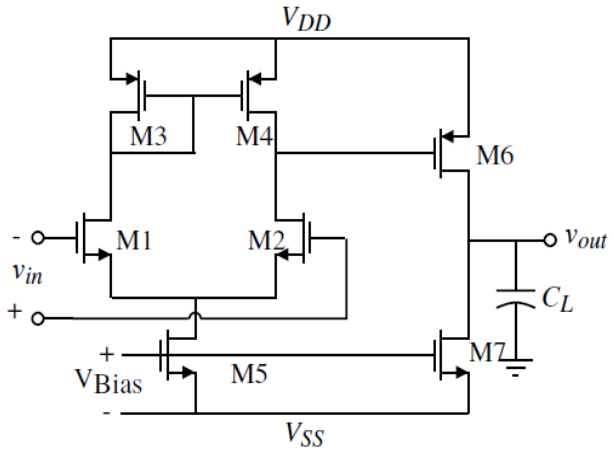


Figure 3.7 Amplifier-type Comparator.

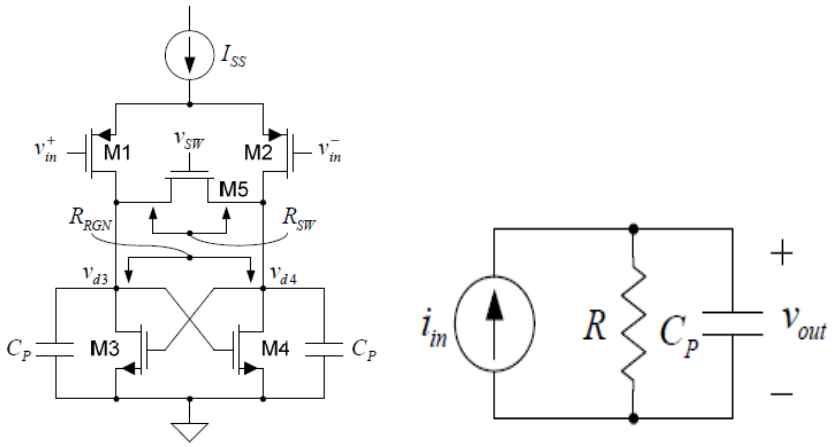
For pipeline/flash ADC design, we seldom use amplifier-type comparator. The reasons are:

1. It will always consume static power which means it is costly. The power of comparator in Figure 3.7 is $P=I_{M5} *V_{DD}+I_{M7}*V_{DD}$

2. The speed of amplifier-type comparator is slow, compared to latch-type comparator, there is no positive feedback in amplifier-type one, so the time response is slow. As a result it's difficult to achieve the performance needed for a 12 bit 50 MS/s AD converter [1].

3.2.2 Latch-type comparator

Figure 3.8 shows a typical latch-type comparator [9]. The most important feature of this type comparator is that the output of one amplifier is connected to the input of the other amplifier. These cross-couple connection makes a positive feedback in that loop, which results in faster time response compared with amplifier-type one.



(a) (b)

Figure 3.8 (a) Typical Latch-type Comparator (b) Equivalent Small Signal Model.

The input differential voltage is applied to a source-coupled pair, which produces signal currents that are loaded by the resistance $R_{SW}//R_{RGN}$. R_{SW} is the drain-source resistance of M_5 (drain-source resistances of M_1-M_4 are neglected). R_{RGN} is the resistance due to the regeneration of M_3-M_4 which has been shown to be equal to $-2/g_{m3}$. C_P represents parasitic capacitance on node V_{d3} and V_{d4}. The comparator works in two non-overlapped phases.

Phase one is reset mode: when the signal V_{SW} is high, the reset mode requires that the value of $R_{SW}//R_{RGN}$ be positive, which will be the case if M_5 is in triode and $R_{SW} < 2/g_{m3}$. In this mode, the stage behaves as a stable, low-gain differential amplifier with ($v_{d4} - v_{d3}$) being the differential output voltage. Phase two is regeneration mode: When V_{SW} goes low, R_{SW} becomes very large and hence $R_{SW}//R_{RGN}$ becomes negative. Under this condition, the stage is unstable and the magnitude of the output voltage will increase exponentially with time due to the negative time constants at the nodes v_{d3} and v_{d4}. Hence, this is called the regeneration mode. In operation, when the clock transitions from high to low any existing output voltage will regenerate until either v_{d3} or v_{d4} goes low and the other goes high.

Considering symmetry, the input current source i_{in} represents the drain current of M_1, the capacitor C_p represents the parasitic capacitance at v_{d3} , and the resistor R represents one-half of $R_{SW}//R_{RGN}$.

- Reset mode:
  - $R=R1= (R_{SW}//R_{RGN})/2>0$

– Time constant

$$\tau_1 = C_P R_1 = \frac{R_{SW} \parallel R_{RGN}}{2} C_P > 0 \tag{3.2}$$

– Output voltage

$$\Delta V_0 = A\Delta V_{in}(1 - e^{-\frac{t}{\tau_1}}) \tag{3.3}$$

- regeneration mode:
  - $R=R_2=R_{RGN}/2=-1/g_{m3}<0$
  - Time constant

$$\tau_2 = C_P R_2 = -\frac{1}{g_{m3}} C_P < 0 \tag{3.4}$$

  - Output voltage

$$\Delta V = \Delta V_0 e^{\omega_u t} = \Delta V_0 e^{\frac{t}{\tau_2}} \tag{3.5}$$

The final output voltage of these two phases is:

$$\Delta V_{finial} = \Delta V_0 e^{\frac{t}{\tau_2}} = A\Delta V_{in}(1 - e^{-\frac{t_1}{\tau_1}}) e^{\frac{t_2}{\tau_2}} \tag{3.6}$$

A smaller regeneration time constant τ_2 will create a full-scale output sooner. But it will reduce the sensitivity of the comparator to inputs after the start of regeneration. The reset time constant τ_1: A longer reset time constant will increase the sensitivity of the comparator to inputs before the start of regeneration.

There are mainly 3 types of latch-type comparator [10]: Static latched comparator, Class-AB latched comparator and Dynamic latched comparator. Before discuss these comparators, kickback noise is first introduced in figure 3.9: The large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called kickback noise.

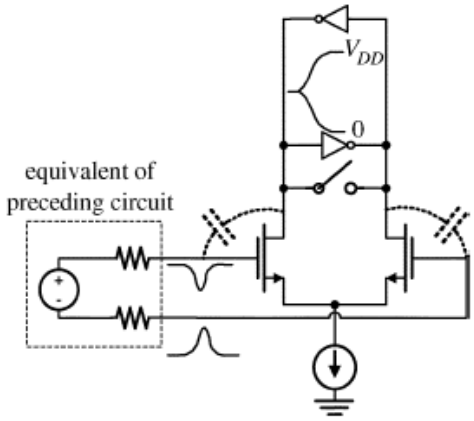


Figure 3.9 Kickback Noise.

3.2.3 Static latched comparator

The regeneration is done by two cross-coupled inverters (M_{3a}/M_{4a} and M_{3b}/M_{4b}). The power efficiency is poor, since the consumption is purely static. But it has low kickback noise because of slow regeneration process.

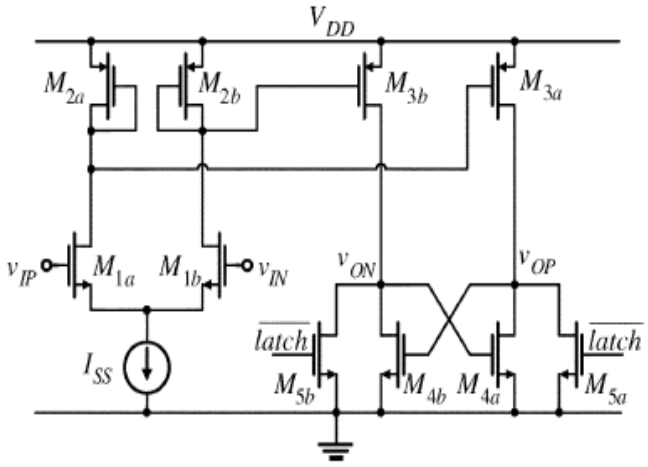


Figure 3.10 Static Latched Comparator.

3.2.4 Class-AB latched comparator

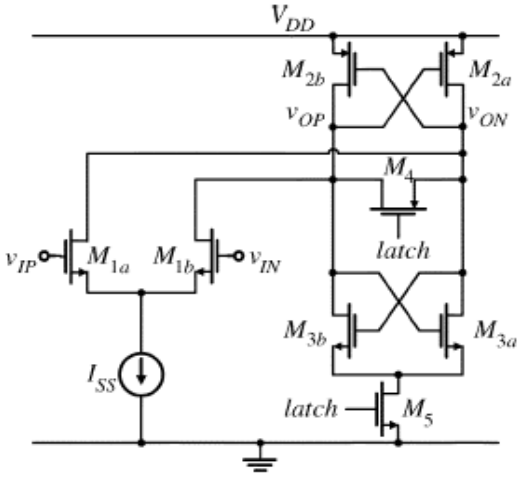


Figure 3.11 Class-AB Latched Comparator.

The regeneration is done by two cross-coupled CMOS inverters. Their current increases momentarily, during the regeneration process, to charge the output nodes faster. The drains of the input differential pair are directly connected to the regeneration nodes. The circuit reacts quicker to input variations, because there is only one pole. However, this increases the kickback noise; it still has supply current in the reset phase and after the regeneration finishes.

3.2.5 Dynamic latched comparator

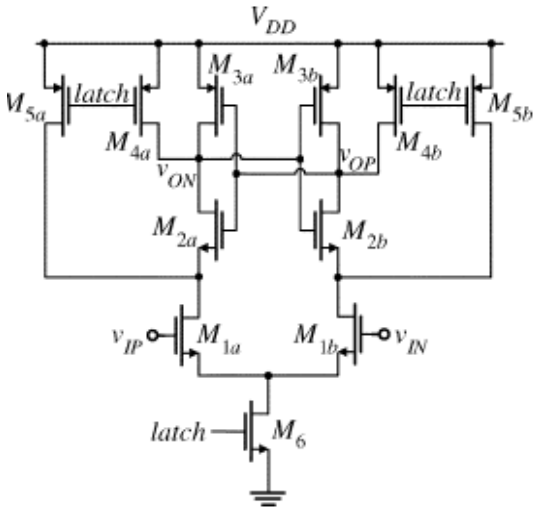


Figure 3.12 Dynamic Latched Comparator.

In dynamic latched comparators [10], the current only flows during the regeneration. After regeneration is completed, one output node is at V_{DD}; the other output and both drains of the differential pair have a 0-V potential. There is no supply current. This comparator has two kickback noise sources: voltage variations and the variation of the operating region of the differential pair transistors. In the reset mode: all the

transistors are cut-off (The gate, source and drain of M_{2a} and M_{2b} are all at V_{DD}). In the regeneration mode: at the very beginning, M_{1a} and M_{1b} are in saturation; M_{2a} and M_{2b} are cut-off, so no current runs through V_{DD} to ground. The current discharges parasitic capacitors C_{P1} at the M_1's drain. Until one of the transistor M_2 is turn on. When one of M_2 turns on, the voltage of its drain will decrease first, leading the opposite PMOS turns on. Then the regeneration begins to work.

Table 3.1 shows all the comparisons among those four types of comparators. And table 3.2 compares the time response of these comparators which indicate the speed performance.

Performance	Speed	Positive feedback	Power	Kickback noise	Area transistors
Amplifier	Slowest	None	Most	None	7
Static latch	Slow	Y	More	Less	11
Class-AB latch	Faster	Y	Less	More	9
Dynamic latch	Fastest	Y	Least	Most	11

Table 3.1 Performance Comparisons.

Time constant	τ_1	τ_2	Poles in pre-amp
Static latch	$\frac{1}{g_{m2}}C_{P1}+R_{SW}C_{P2}$	$-\frac{1}{g_{m3}}C_P$	2
Class-AB latch	$\frac{R_{SW}\,\|\|\,R_{RGN2}}{2}C_P$	$-(\frac{1}{g_{m2}+g_{m3}})C_P$	1
Dynamic latch	---	$-(\frac{1}{g_{m2}+g_{m3}})C_{P2}$	1

Table 3.2 Time Constant Comparisons.

From these tables, dynamic latch comparator is the fastest one and consumes least power. It doesn't even need reset time because of no RC time constant in that phase, but it has the largest kickback noise. Amplifier-type comparator is the most costly since it has a static current run through V_{DD} to ground all the time, however, it doesn't has kickback noise for no positive feedback loop exists.

3.2.6 Non-ideal problems in comparator

Offset and kickback noise interference are the mainly problems in comparators. In order to get offset as small as possible, one way is minimization; and anther is compensation or cancellation, that mechanism is much similar to offset compensation in OP-AMP, which will discussed in that section.

In order to minimize offset, pre-amplifier which is prior to comparator is introduced. The total offset is:

$$V_{os,in2}=V_{os,in,amp}+\frac{V_{os,in,latch}}{A} \tag{3.7}$$

The offset of latch is minimized by the factor of A (A is the gain of pre-amplifier). As we all the due to the well- symmetric topology of pre-amplifier, the pre-amplifier offset is rather smaller than latch one. We can also increase the area of pre-amplifier to get a less mismatching.

Isolation can minimize the voltage variations on the drains of the differential pair [10]. Those nodes are isolated from the regeneration nodes using switches, which open during the regeneration phase. An alternative path for the current of the differential pair must be provided, in order to keep the drain voltages near the values found in the reset phase. (Figure 3.13)

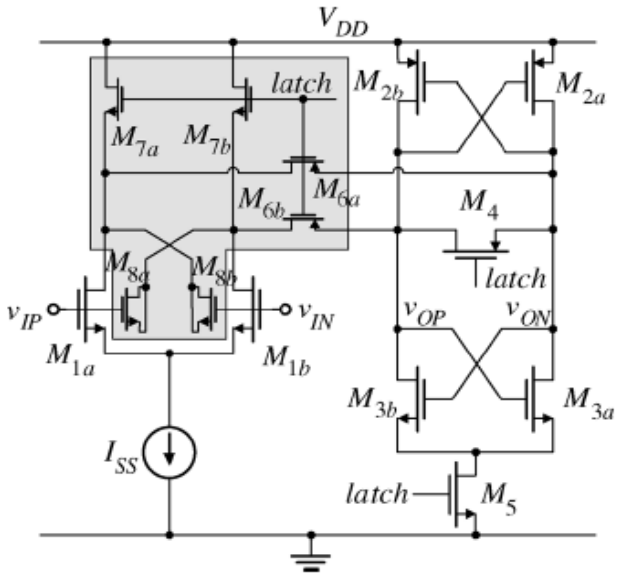


Figure 3.13 Minimizing Kickback Noise.

3.2.7 Specification abstraction

Offset requirement: the offset of comparator is required less than 1LSB in order to achieve no missing code. $V_{os}<V_{ref}/2^N$

Speed requirement:

1. Preamplifier:

   Any signal which is larger than 1LSB, should be amplified during reset mode.

   (a) For small differential input signal, which is a little bit larger than 1LSB: if the pre-amplifier has only one pole:

$$t_{setting} = \tau_1 \ln \frac{1}{1-\frac{\Delta V_0}{A}} < \frac{1}{2 f_{sample}} \tag{3.8}$$

   (b) For large differential input signal,

$$t_{setting} = \frac{\Delta V}{SR} = \frac{\Delta V \times C_P}{I} < \frac{1}{2 f_{sample}} \tag{3.9}$$

Sampling rate:

$$f_{sample} < \min\left\{ \frac{I}{2\Delta V \times C_P}, \frac{1}{2\tau_1 \ln \frac{1}{1-\frac{\Delta V_0}{A}}} \right\} \tag{3.10}$$

2. Latch

$$\Delta V = \Delta V_0 e^{\omega_u t} = \Delta V_0 e^{\frac{t}{\tau_2}} > V_{OH} - V_{OL} \Rightarrow t_{setting} > \tau_2 \ln\left(\frac{V_{OH} - V_{OL}}{\Delta V_0}\right)$$

$$\Rightarrow f_{sample} < \frac{1}{2t_{setting}} = \frac{1}{2\tau_2 \ln\left(\frac{V_{OH} - V_{OL}}{\Delta V_0}\right)} \tag{3.11}$$

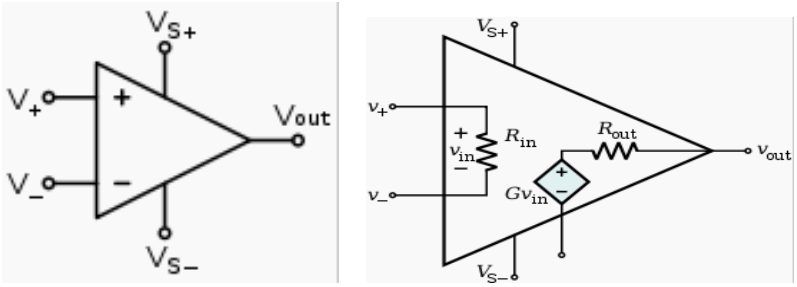
As a result, the final specifications of comparator are:

$$f_{sample} < \min\left\{\frac{I}{2\Delta V \times C_P}, \frac{1}{2\tau_1 \ln\frac{1}{1-\frac{\Delta V_0}{A}}}, \frac{1}{2\tau_2 \ln\left(\frac{V_{OH} - V_{OL}}{\Delta V_0}\right)}\right\} \tag{3.12}$$

$$\Delta V_0 > V_{os,latch}$$

3.3 Operational amplifier

An operational amplifier, which is often called an op-amp, is a DC-coupled high-gain electronic voltage amplifier with differential inputs and single or differential outputs. It is widely used as key block in SHA, MDAC and bandgap voltage reference of pipeline ADC. The notation of ideal op-amp is figure 3.14.



(a) (b)

Figure 3.14 (a) OP-AMP Notation, Ideal op-amp.

V+ is non-inverting input, V- is inverting input, Vout is op-amp output, V_{S+} is positive power supply and V_{S-} is negative power supply. For open loop op-amp $V_{out}=(V_+ - V_-)*A_{open\text{-}loop}$. $A_{open\text{-}loop}$ is the open-loop voltage gain of op-amp. The magnitude of the open-loop gain is typically very large, so open-loop operation results in op-amp saturation unless the differential input voltage is extremely small. Op-amps are usually applied to negative-feedback configurations system.

Since practical boundary conditions limit the op-amp performance, such as process specification (Vth, Cox, mobility, etc.), supply voltage and range, operating temperature and range and so on. So op-amp specifications are crucial constraints for the system. These features should be paid attention to:

a. Open loop gain
b. 3-dB bandwidth (dominant pole, Gain bandwidth product)
c. Settling time
d. Offset

e. Slew rate

f. Input common mode range (ICMR)

g. Output-voltage swing

h. Common-mode rejection ratio (CMRR)

i. Power supply rejection ratio (PSRR)

j. Output impedance

k. Noise (Dynamic range=Input swing/Noise)

l. Power consumption

The following section will discussed these configurations with different op-amp architectures.

3.3.1 Differential Op-amp architecture

This section only discusses four most popular and fundamental op-amp architectures.

a. Two-stage Op-amp

b. Telescopic Op-amp

c. Folded-cascode Op-amp

d. Gain-boosting Op-amp

3.3.2 Two-stage Op-amp

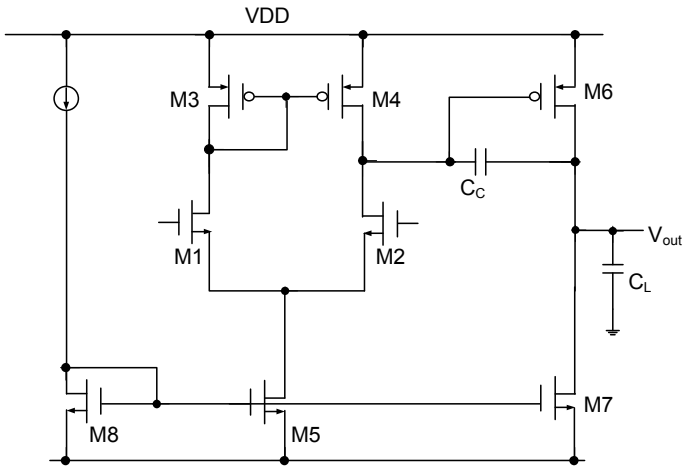


Figure 3.15 Two-stage Op-amps.

This is the simplest op-amp and it only consists of 8 transistors. The gain of the first stage is often larger than the gain of second stage. Because the higher gain the first stage has, the lower input referred noise and offset the op-amp it is. And in order to achieve high output swing, the second stage gain should be smaller. All the specifications of two-stage op-amp are in table 3.3.

DC Gain	$G = g_{m1}(r_{o2} \parallel r_{o4}) \cdot g_{m6}(r_{o6} \parallel r_{o7})$
Dominant pole	$\omega_{-3dB} = p_1 = \frac{-1}{G_{II} C_C (r_{o2} \parallel r_{o4})} = \frac{-1}{g_{m6}(r_{o6} \parallel r_{o7}) C_C (r_{o2} \parallel r_{o4})}$
Unity gain bandwidth	$GB = G \cdot \omega_{-3dB} = \frac{g_{m1}}{C_C}$
Non-dominant poles	$p_2 = \frac{-g_{m6}}{C_{II}} = \frac{-g_{m6}}{C_{gs6} + C_{gs7} + C_{db6} + C_{db7} + C_L}$, $p_3 = \frac{-g_{m3}}{C_{gs3} + C_{gs4} + C_{gd3} + C_{gd1} + C_{b3}}$

Slew rate	$SR = \frac{I_{M5}}{C_L}$
ICMR	$V_{DS5(sat)} + V_{GS1} \le V_{IC} \le V_{DD} - V_{SG3} + V_{th1}$
Output swing	$V_{out,pp} = V_{DD} - \lvert V_{OD6} \rvert - V_{OD7}$
Power dissipation	$P_{diss} = V_{DD}(I_{D5} + I_{D7}) = \frac{1}{2} V_{DD}(g_{m5} V_{OD5} + g_{m7} V_{OD7})$
Input referred noise	$\overline{V_n}^2 \approx 4kT\left(2\frac{2}{3g_{m1,2}} + 2\frac{2g_{m3,4}}{3g_{gm1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2} C_{ox} f} + 2\frac{K_P}{(WL)_{3,4} C_{ox} f}\frac{g_{m3,4}^2}{g_{gm1,2}^2}$

* V_{OD} is transistor overdrive voltage. $V_{OD} = V_{GS} - V_{th}$

Table 3.3 The Specifications of Two-stage Op-amp.

3.3.3 Telescopic Op-amp

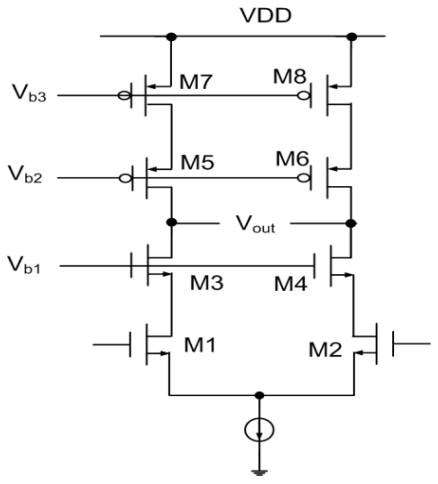


Figure 3.16 Telescopic Op-amp.

Telescopic op-amp only has one stage compared with two-stage op-amp. And its gain is as large as two-stage one. However, its output swing is 2*V_{OD} less than that of two-stage one. All the specifications of two-stage op-amp are in table 3.4.

DC Gain	$G = g_{m1}[(g_{m3}r_{o3}r_{o1}) \| (g_{m5}r_{o5}r_{o7})]$
Dominant pole	$\omega_{-3dB} = p_1 = \frac{-1}{C_L[(g_{m3}r_{o3}r_{o1}) \| (g_{m5}r_{o5}r_{o7})]}$
Unity gain bandwidth	$GB = G \cdot \omega_{-3dB} = \frac{g_{m1}}{C_L}$
Non-dominant poles	$p_2 = \frac{-g_{m3}}{C_{gs3} + C_{gd1} + C_{b3}}, p_3 = \frac{-g_{m5}}{C_{gs5} + C_{gd7} + C_{b5}}$
Slew rate	$SR = \frac{I_{ss}}{C_L}$
ICMR	$V_{ISS} + V_{GS1} \le V_{IC} \le V_{b1} - V_{GS3} + V_{th1}$
Output swing	$V_{out,pp} = 2[V_{DD} - (V_{OD1} + V_{OD3} + \lvert V_{OD5} \rvert + \lvert V_{OD7} \rvert + V_{ISS})]$
Power dissipation	$P_{diss} = V_{DD} I_{ISS} = \frac{1}{2} V_{DD}(g_{m1} V_{OD1} + g_{m2} V_{OD2})$
Input referred noise	$\overline{V_n}^2 = 4kT\left(2\frac{2}{3g_{m1,2}} + 2\frac{2g_{m7,8}}{3g_{gm1,2}^2}\right) + 2\frac{K_N}{(WL)_{1,2}C_{ox}f} + 2\frac{K_P}{(WL)_{1,2}C_{ox}f}\frac{g_{m7,8}^2}{g_{gm1,2}^2}$

* VOD is transistor overdrive voltage. $V_{OD} = V_{GS} - V_{th}$

Table 3.4 The Specifications of Telescopic Op-amp.

3.3.4 Folded-cascode Op-amps

Its gain is all most the same as the telescopic one, and the output swing is slightly larger than that of telescope one, $2*V_{OD}$. However the power consumption is twice larger of previous one, because two branches currents run through VDD to ground. One of great features in fold-cascode op-amp is its input signal is larger than other type op-amp. Take figure 3.17 as an example, the lowest input signal could be even less than ground potential. Table 3.5 shows all its specifications.

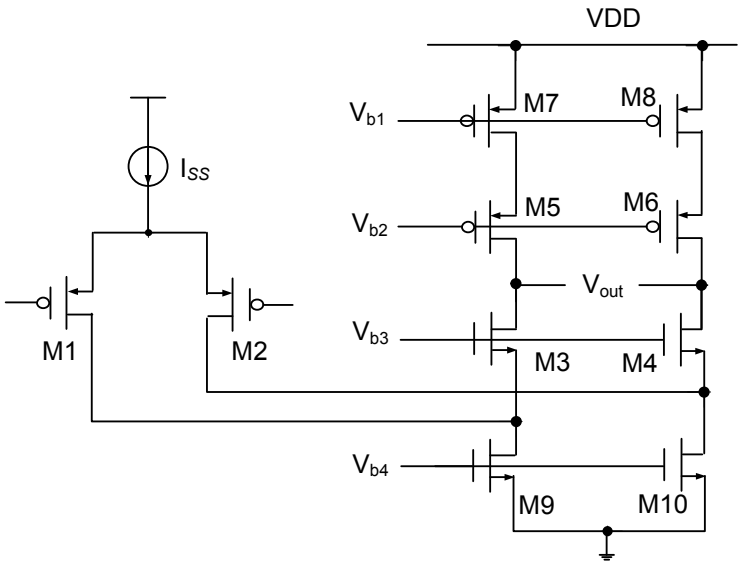


Figure 3.17 Folded-cascode Op-amps.

Its gain is all most the same as the telescopic one, and the output swing is slightly larger than that of telescope one, $2*V_{OD}$. However the power consumption is twice larger of previous one, because two branches currents run through V_{DD} to ground. One of great features in fold-cascode op-amp is its input signal is larger than other type op-amp. Take

figure 3.17 as an example, the lowest input signal could be even less than ground potential. Table 3.5 shows all its specifications.

DC Gain	$G = g_{m1}[(g_{m3}r_{o3}(r_{o9} \parallel r_{o1})) \parallel (g_{m5}r_{o5}r_{o7})]$
Dominant pole	$\omega_{-3dB} = p_1 = \dfrac{-1}{C_L[(g_{m3}r_{o3}(r_{o9} \parallel r_{o1})) \parallel (g_{m5}r_{o5}r_{o7})]}$
Unity gain bandwidth	$GB = G \cdot \omega_{-3dB} = \dfrac{g_{m1}}{C_L}$
Non-dominant poles	$p_2 = \dfrac{-g_{m3}}{C_{gs1} + C_{gd9} + C_{gs3} + C_{b3}}, p_3 = \dfrac{-g_{m5}}{C_{gs5} + C_{gd7} + C_{b5}}$
Slew rate	$SR = \dfrac{I_{ss}}{C_L}$
ICMR	$V_{OD9} - \lvert V_{th1} \rvert \le V_{IC} \le V_{DD} - V_{ISS} - \lvert V_{GS1} \rvert$
Output swing	$V_{out,pp} = 2[V_{DD} - (V_{OD3} + V_{OD9} + \lvert V_{OD5} \rvert + \lvert V_{OD7} \rvert)]$
Power dissipation	$P_{diss} = V_{DD}(I_{ISS} + I_{M7} + I_{M8}) = V_{DD}(I_{M9} + I_{M10})$ $= V_{DD}(g_{m1}V_{OD1} + g_{m7}V_{OD7})$
Input referred noise	$\overline{V_n}^2 = 4kT\left(2\dfrac{2}{3g_{m1,2}} + 2\dfrac{2g_{m7,8}}{3g_{m1,2}^2} + 2\dfrac{2g_{m9,10}}{3g_{m1,2}^2}\right)$ $+ 2\dfrac{K_P}{(WL)_{1,2}C_{ox}f} + 2\dfrac{K_P}{(WL)_{1,2}C_{ox}f}\dfrac{g_{m7,8}^2}{g_{m1,2}^2} + +2\dfrac{K_N}{(WL)_{1,2}C_{ox}f}\dfrac{g_{m9,10}^2}{g_{m1,2}^2}$

* VOD is transistor overdrive voltage. $V_{OD} = V_{GS} - V_{th}$

Table 3.5 The Specifications of Folded-cascode Op-amp.

3.3.5 Gain-boosting Op-amp

The output resistance of figure 3.18(a) is $R_{out}=g_{m2}r_{o2}r_{o1}$, when output of an amplifier is connected to the gate of M_2; non-inverting input of the amplifier is set to a fixed voltage V_b, and inverting input is connected to the drain of M1. The amplifier boosts the output resistance $R_{out}=A_1g_{m2}r_{o2}r_{o1}$.

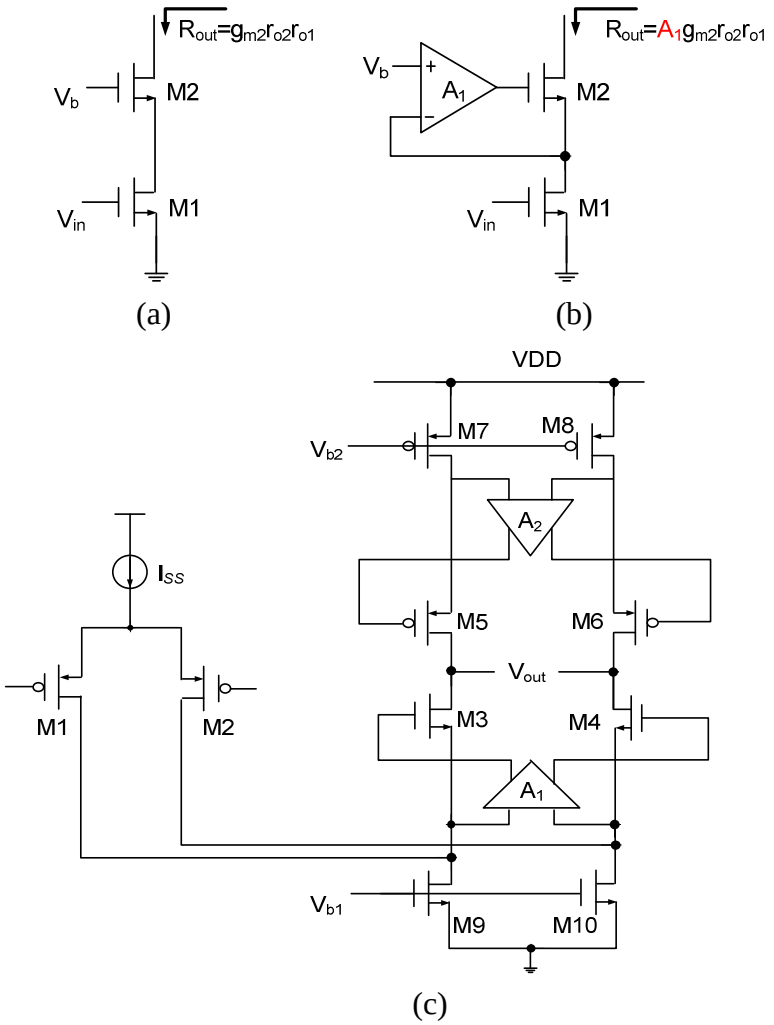


Figure 3.18(a, b) Gain Boosting Technology, (c) Folded-cascode Op-amp with Gain Boosting.

With this boosting technology, the gain of folded-cascode op-amp in Figure 3.18(c) significantly increases [19]. Table 3.6 shows all its specifications. Dominant pole, non-dominant poles, unity gain bandwidth, slew rate, ICMR, output swing is almost the same as folded-cascode one, only introducing more parasitic capacitors.

DC Gain	$G = g_{m1}[(A_1 g_{m3} r_{o3}(r_{o9} \parallel r_{o1})) \parallel (A_2 g_{m5} r_{o5} r_{o7})]$
Dominant pole	$\omega_{-3dB} = p_1 = \dfrac{-1}{C_L[(A_1 g_{m3} r_{o3}(r_{o9} \parallel r_{o1})) \parallel (A_2 g_{m5} r_{o5} r_{o7})]}$
Power dissipation	$P_{diss} = V_{DD}(I_{ISS} + I_{M7} + I_{M8}) + P_{A1} + P_{A2}$ $= V_{DD}(g_{m1} V_{OD1} + g_{m7} V_{OD7}) + P_{A1} + P_{A2}$
Input referred noise	$\overline{V_n}^2 = 4kT\left(2\dfrac{2}{3g_{m1,2}} + 2\dfrac{2g_{m7,8}}{3g_{m1,2}^2} + 2\dfrac{2g_{m9,10}}{3g_{m1,2}^2}\right)$ $+ 2\dfrac{K_P}{(WL)_{1,2} C_{ox} f} + 2\dfrac{K_P}{(WL)_{1,2} C_{ox} f}\dfrac{g_{m7,8}^2}{g_{m1,2}^2} + 2\dfrac{K_N}{(WL)_{1,2} C_{ox} f}\dfrac{g_{m9,10}^2}{g_{m1,2}^2}$ $+ \dfrac{\overline{i_{n,A1}}^2}{g^2_{m1,2}} + \dfrac{\overline{i_{n,A2}}^2}{g^2_{m1,2}} + \dfrac{\overline{v_{n,A1}}^2}{g^2_{m1,2} r_{o9}^2} + \dfrac{\overline{v_{n,A2}}^2}{g^2_{m1,2} r_{o9}^2}$

* V_{OD} is transistor overdrive voltage. $V_{OD} = V_{GS} - V_{th}$ P_{A1} and P_{A2} are power dissipation of additional amplifier A_1 and A_2.

Table 3.6 The Specifications of Gain-boosting Op-amp.

Table 3.7 shows the performance comparisons of these four types of op-amps. Two-stage has highest output swing, telescopic one has the fastest speed because of lowest parasitic capacitor; folded-cascode one has the largest ICMR. Gain-boosting op-amp gets the highest DC gain while the circuitry is the most complicated.

	DC Gain	Output swing	Speed	Power	Noise
Two- stage	Lowest	Highest	Slowest	Middle	Smallest
Telescopic	Middle	Smallest	fastest	least	Smaller
Folded-cascode	Middle	Middle	Middle	Middle	Bigger
Gain-boosting	Biggest	Middle	Middle	Most	Biggest

Table 3.7 The Performance Comparisons of Op-amps.

3.3 SHA AND MDAC

SHA is the most crucial building block in pipeline ADCs. It samples analog signal at one period, and holds the value at the other period. The purpose of this circuit is to hold the analogue value steady for a short time while the converter or other following system performs some operation that takes a little time. MDAC contains a DAC, a subtractor and an S/H amplifier. SHA and MDAC are discussed together, since the structures are the same. The key sub-block of SHA and MDAC is op-amp. Op-amps' speed, open loop gain, offset will be the limitation of the pipeline ADCs performance.

3.4.1 SHA

Figure 3.19 is the SHA [1, 12]. It works in two non-overlapped phases. The sampling capacitor is C and the parasitic capacitance at the input is pC. The capacitance bC and cC represent the load capacitance switched to the op-amp output on clock phase 2 and 1 respectively. The capacitor aC is the feedback capacitor to make a accurate SHA gain.

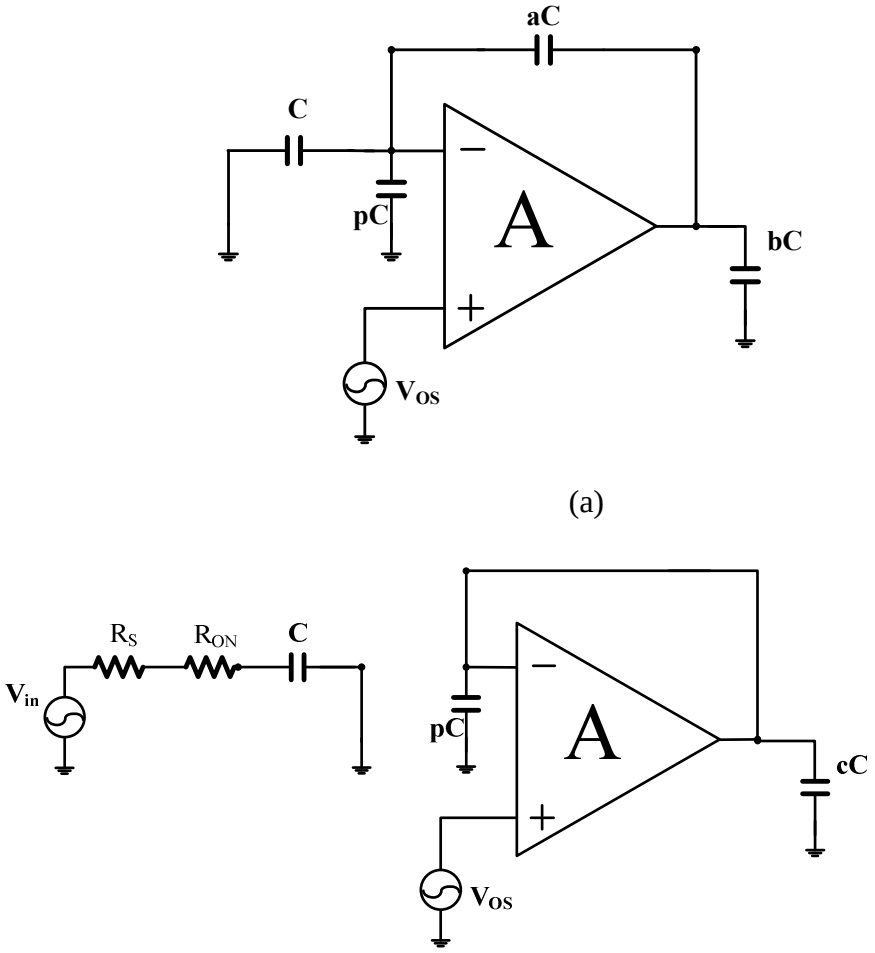


Figure 3.19 (a) SHA (b) Phase 1 (c) Phase 2.

Op-amp has input offset VOS and the finite open loop gain A which will impact the overall performance of SHA. At phase 1, the analog signal Vin samples on the capacitor C, the time constant is: $\tau_{sampling} = (R_{ON} + R_S)C$, and voltage on capacitor C is

$$\tau_{sampling} = (R_{ON} + R_S)CV_{cap} = V_{in}(1 - e^{-t/\tau_{sampling}}) \tag{3.13}$$

The relative settling error should be:

$$\varepsilon_{rP1} = \frac{V_{in} - V_{cap}}{V_{in}} = e^{-t/\tau_{sampling}} \tag{3.14}$$

The charge in C and pC are:

$$Q_{P1} = -CV_{in} + \frac{AV_{OS}}{A+1} pC \tag{3.15}$$

At phase 2, using small equivalent signal model, the transform function of SHA is:

$$\begin{aligned} \frac{V_{OUT}}{V_{IN}} &= \frac{-C(g_m - aCs)R_O}{aCR_O g_m + C + pC + aC + R_O[bC(C + aC + pC) + (C + pC)aC]s} \\ &\approx \frac{-(g_m - aCs)R_O}{aR_O g_m + R_O[b(C + aC + pC) + (C + pC)a]s} \end{aligned} \tag{3.16}$$

Time constant is $\tau_{amp} = \frac{C}{g_m}\frac{(a+b)(1+p)+ab}{a}$, and the dynamic relative settling error:

$$\varepsilon_{rP2} = \frac{V_{in} - V_{cap}}{V_{in}} = e^{-t/\tau_{amp}} \tag{3.17}$$

The charge at negative input terminal:

$$\begin{aligned} Q_{P2} &= (C + pC)V_- + aC(V_- - V_{OUT}) = (1 + p + a)CV_- - aCV_{OUT} \\ &= (1 + p + a)C(V_{OS} - \frac{V_{OUT}}{A}) - aCV_{OUT} \end{aligned} \tag{3.18}$$

The charges at that node during phase1 and phase2 should be the same:

$$\begin{aligned} & Q_{P2} = Q_{P1} \quad => \\ & (1 + p + a)C(V_{OS} - \frac{V_{OUT}}{A}) - aCV_{OUT} = -CV_{in} + \frac{AV_{OS}}{A+1} pC \\ & => V_{OUT} = \frac{V_{IN} + (1 + a + p)V_{OS} - \frac{AV_{OS}}{A+1} p}{a + \frac{1 + a + p}{A}} \end{aligned} \tag{3.19}$$

In order to achieve an accurate value of SHA, resolution and sampling rate requirements should be trade-off: the total errors consist of static error and dynamic error. The finite gain and input offset of op-amp and capacitance mismatch result in static error; for dynamic one, op-amp takes a certain time to reach the final value.

The worst error case: Vin=Vref, total error should be less than LSB.

- At phase1, both dynamic error and input referred noise will limit the performance

  Dynamic error:

$$\begin{aligned} & \varepsilon_{total} \approx \varepsilon_{dynamic} = \varepsilon_{rP1} = e^{-t/\tau_{sampling}} < \frac{1}{2^N} \\ & => t_1 > \tau_{sampling} \ln(2^N) = N\tau_{sampling} \ln 2 = N(R_{ON} + R_S)C \ln 2 \end{aligned} \tag{3.20}$$

Dynamic range:

- Input referred noise: $\overline{V_n}^2 = \frac{kT}{C}$ (3.21)

- If a sinusoidal signal is applied:

$$DR = \frac{\overline{V_{input}^2}}{\overline{V_n}^2} = \frac{\frac{1}{2}V_{input,swing}^2}{kT/C} \tag{3.22}$$

- ADC should make sure SNR<DR, it means all the valid input signal will be converted by the ADC, then:

$$\frac{\frac{1}{2}\left(\frac{V_{input,swing}}{2}\right)^2}{kT/C} > 1.5 \cdot 2^{2N} \Rightarrow C > \frac{12 \cdot 2^{2N} kT}{V_{input,swing}^2} \tag{3.23}$$

- At phase 2, both static and dynamic errors impact the performance. For partition error:

$$\varepsilon_{dynamic} < \frac{1}{2}\varepsilon_{total} = \frac{1}{2^{N+1}}, \quad \varepsilon_{static} < \frac{1}{2}\varepsilon_{total} = \frac{1}{2^{N+1}} \tag{3.24}$$

  - Dynamic error:

$$\varepsilon_{dynamic} \approx \varepsilon_{rP2} = e^{-t/\tau_{amp}} < \frac{1}{2^{N+1}}$$

$$\Rightarrow t_2 > \tau_{amp} \ln(2^{N+1}) = (N+1)\tau_{amp} \ln 2 = (N+1)\frac{C}{g_m}\frac{(a+b)(1+p)+ab}{a}\ln 2 \qquad (3.25)$$

$$\Rightarrow t_2 > (N+1)\frac{C}{g_m}\frac{(a+b)+ab}{a}\ln 2$$

- Static errors: op-amp offset, finite gain, input parasitic capacitance and feedback capacitance mismatch all impact the static error.
  - For perfect capacitance layout matching, a=1+/-0.1%;
  - Parasitic cap. Cgs=2/3(WL)Cox
  - The typical VOS without offset cancellation is 5mV~30mV.
  - Only if considering finite gain A, when Vin=Vref, the worst case:

$$V_{OUT} \approx \frac{V_{IN} + (2+\Delta a)V_{OS}}{1+\left(\Delta a + \frac{2+\Delta a + p}{A}\right)} \approx V_{IN}\left(1-\Delta a - \frac{2+\Delta a}{A}\right) + 2V_{OS}$$

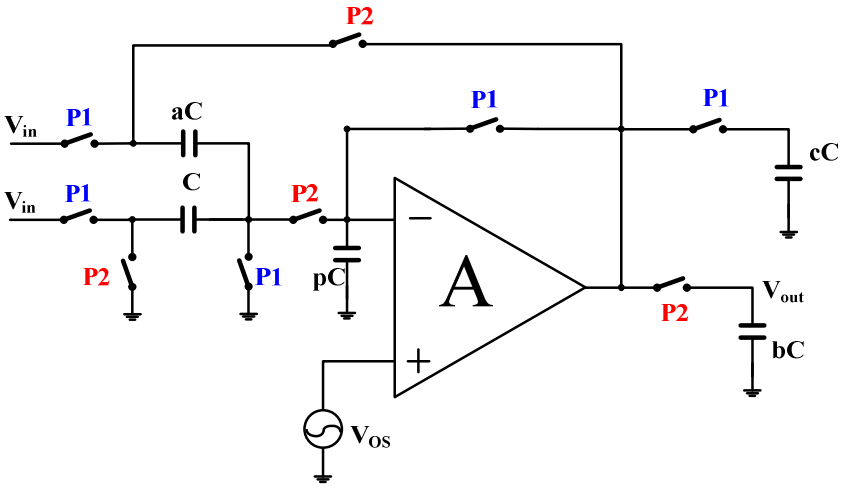
$$\left|\Delta a + \frac{2+\Delta a}{A}\right| V_{ref} < LSB \Rightarrow \left|\Delta a + \frac{2+\Delta a}{A}\right| V_{ref} < \frac{2V_{ref}}{2^N} \qquad (3.26)$$

$$\Rightarrow A > \frac{2+\Delta a}{\frac{1}{2^{N-1}} - \Delta a},$$

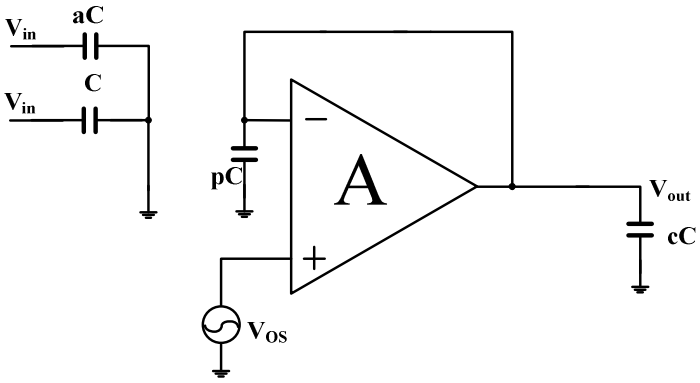
$$\frac{1}{2^{N-1}} > \Delta a > -\frac{2}{A+1} \Rightarrow \frac{1}{2^{N-1}} - \Delta a > 0 \Rightarrow N < -\frac{\lg \Delta a}{\lg 2} + 1$$

3.4.2 MDAC

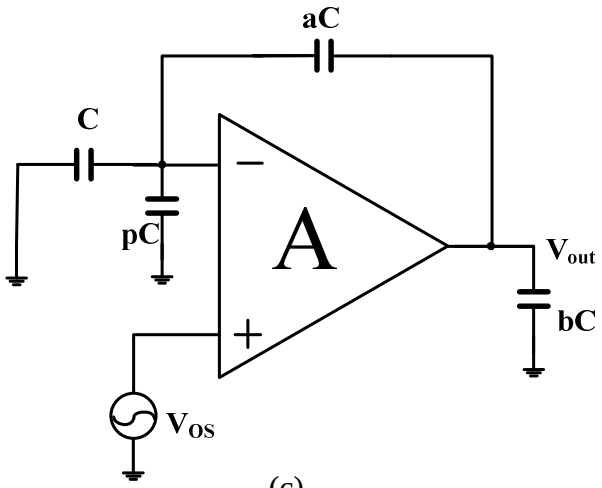
Figure 3.20 is the MDAC [1]. It works in two non-overlapped phases. The sampling capacitor is C and the parasitic capacitance at the input is pC. The capacitance bC and cC represent the load capacitance switched to the op-amp output on clock phase 2 and 1 respectively. The capacitor aC is the feedback capacitor to make an accurate MDAC gain.



(a)



(b)



(c)

Figure 3.20 (a) MDAC (b) Phase 1 (c) Phase 2.

With the same method of SHA, at the phase 1, the input signal samples on capacitor C and aC:

$$\begin{aligned} \tau_{sampling} &= (R_{ON} + R_S)(C + aC) \\ \varepsilon_{rP1} &= e^{-t/\tau_{sampling}} \\ Q_{P1} &= -(1+a)CV_{in} + \frac{AV_{OS}}{A+1}\, pC \end{aligned} \tag{3.27}$$

At the phase 2, the circuit is exactly the same as SHA in its phase2:

$$\begin{aligned} Q_{P2} &= (1+p+a)C(V_{OS} - \frac{V_{OUT}}{A}) - aCV_{OUT} \\ \tau_{amp} &= \frac{C}{g_m}\frac{(a+b)(1+p)+ab}{a}, \varepsilon_{rP2} = \frac{V_{in} - V_{cap}}{V_{in}} = e^{-t/\tau_{amp}} \end{aligned} \tag{3.28}$$

The charges during phase1 and phase2 should be the same:

$$Q_{P2} = Q_{P1} \quad => (1+p+a)C(V_{OS} - \frac{V_{OUT}}{A}) - aCV_{OUT} = -(1+a)CV_{in} + \frac{AV_{OS}}{A+1} pC$$

$$=> V_{OUT} = \frac{(1+a)V_{IN} + (1+a+p)V_{OS} - \frac{AV_{OS}}{A+1} p}{a + \frac{1+a+p}{A}}$$

$$\approx \frac{(1+a)V_{IN} + (1+a)V_{OS}}{a + \frac{1+a}{A}} = \frac{(1+\frac{1}{a})V_{IN} + (1+\frac{1}{a})V_{OS}}{1 + \frac{1+\frac{1}{a}}{A}} \approx (1+\frac{1}{a})(V_{IN} + V_{OS})\left(1 - \frac{1+\frac{1}{a}}{A}\right)$$

$$\approx \left(\frac{1}{a}+1\right)V_{IN}\left(1 - \frac{1+\frac{1}{a}}{A}\right) + (1+\frac{1}{a})V_{OS}$$

$$\left(\frac{1}{a}+1\right)\frac{1+\frac{1}{a}}{A}V_{ref} < LSB_{left} = \frac{2V_{ref}}{2^{N_{left}}} => A > 2^{N_{left}-1}\left(1+\frac{1}{a}\right)^2 \tag{3.29}$$

Reconsideration performance limitations in MDAC again:

$$\frac{1}{2f_S} > t_1 > \tau_{sampling} \ln(2^{N_{left}}) = N_{left}\tau_{sampling} \ln 2 = N_{left}(R_{ON} + R_S)C \ln 2$$

$$\varepsilon_{dynamic} < \frac{1}{2}\varepsilon_{total} = \frac{1}{2^{N_{left}+1}}, \quad \varepsilon_{static} < \frac{1}{2}\varepsilon_{total} = \frac{1}{2^{N_{left}+1}}$$

$$\frac{1}{2f_S} > t_2 > \tau_{amp} \ln(2^{N_{left}+1}) = (N_{left}+1)\tau_{amp} \ln 2 = (N_{left}+1)\frac{C}{g_m}\frac{(a+b)(1+p)+ab}{a} \ln 2$$

$$A > 2^{N_{left}-1}\left(1+\frac{1}{a}\right)^2$$

$$C > \frac{3 \cdot kT}{V_{input,swing}^2} 2^{2N-2} = \frac{1}{4}\mathrm{C}_{\text{previous}}$$

(3.30)

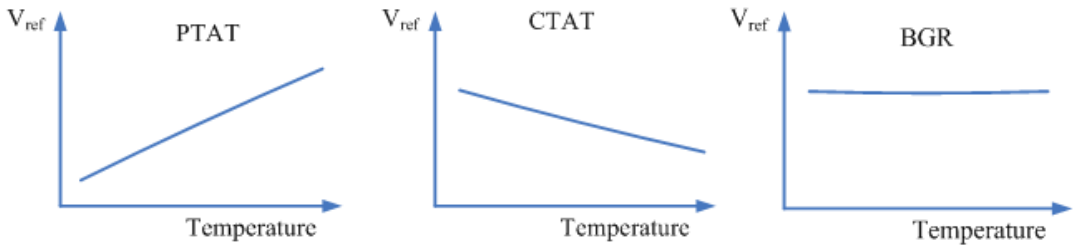
3.5 Voltage reference

Voltage Reference is a circuit used to generate a fixed voltage, Vref, which is independent of the power supply voltage VDD, temperature, and process variations. There are three types of voltage references in figure 3.21:

a. Proportional to absolute temperature (PTAT)

b. Complementary to absolute temperature (CTAT)

c. Very little changes with temperature (BGR)



(a) PTAT (b) CTAT (c) BGR

Figure 3.21 Voltage Reference.

Two of most important voltage Reference Specifications are temperature coefficient and PSRR.

a. Temperature coefficient The unit is ppm/^{o}C = 10-6/^{o}C (parts per million per degree C)

b. Power supply rejection ratio (PSRR): describe the amount of noise from a power supply that the voltage reference can reject.

$$PSSR = \frac{\Delta V_{DD}}{\Delta V_{ref}} \tag{3.31}$$

The smaller the temperature coefficient voltage reference is, the stable and accurate the system it is. And PSRR should be as large as possible, to minimize the voltage supply interference, especially in the mixed-signal systems, the analog voltage supply is noisy.

3.5.1 Bandgap reference

Bandgap reference circuits are necessarily and widely used in data-conversion systems, voltage regulators and memories. They can provide very stable references hardly dependent on temperature and external power supply.

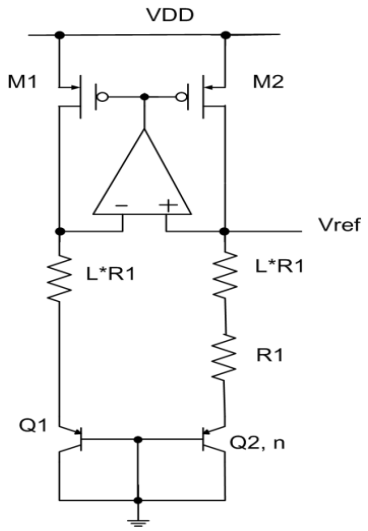


Figure 3.22 Bandgap Voltage Reference.

The basic idea of BGR is to add a proportional to absolute temperature (PTAT) voltage to the emitter-base voltage (VBE), so that the first-order temperature dependency

of the pn junction is compensated by the PTAT voltage, and a nearly temperature independent output is generated. The PTAT voltage is actually the thermal voltage (Vt) of the pn junction [28, 29, 30]. Thus the reference voltage is expressed as:

$$
\begin{aligned}
&V_{R1} = V_{BE1} - V_{BE2} = \Delta V_{BE} \Rightarrow I_{R1} = \frac{\Delta V_{BE}}{R_1} = \frac{V_T \ln n}{R_1} \\
&Vref = V_{BE2} + I_{R1}(R_1 + R_2) = V_{BE3} + \frac{V_T \ln n}{R_1}(R_1 + R_2) \\
&= V_{BE2} + V_T(1+L)\ln n \\
&\frac{\partial V_{ref}}{\partial T} = \frac{\partial V_{BE2}}{\partial T} + (1+L)\cdot\frac{k}{q}\ln n = 0 \\
&\frac{\partial V_{BE3}}{\partial T} \approx -1.6mV/C
\end{aligned}
\tag{3.32}
$$

3.5.2 Curvature-compensated BGR

The more accurate emitter-base voltage (VBE) of BJT is:

$$
V_{BE}(T) = V_{BG} - (V_{BG} - V_{BE0})\frac{T}{T_0} - (\eta - \alpha)V_T \ln\frac{T}{T_0}, \quad \eta \approx 4 \tag{3.33}
$$

- α=0, when the current in BJT is PTAT.
- α=1, when the current in BJT is temperature independent.

Because of logarithm function in that equation, higher order temperature coefficients exist. The previous BGR method only cancels the first order temperature coefficient. Curvature-compensated BGR in figure 3.5.3 cancels higher order temperature coefficient [33, 34, 35].

$$V_{BEQ3}(T) = V_{BG} - (V_{BG} - V_{BE0})\frac{T}{T_0} - \eta V_T \ln\frac{T}{T_0}$$
$$V_{BEQ1,2}(T) = V_{BG} - (V_{BG} - V_{BE0})\frac{T}{T_0} - (\eta - 1)V_T \ln\frac{T}{T_0} \qquad (3.34)$$
$$V_{NL} \cong V_{BEQ3}(T) - V_{BEQ1,2}(T) = V_T \ln\frac{T}{T_0}$$

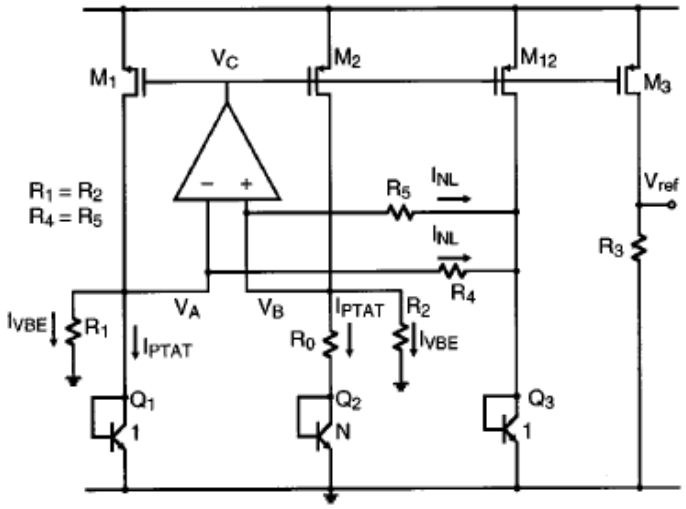


Figure 3.23 Curvature-compensated BGR.

Curvature compensation can be achieved by subtracting from both I1 and I2 a current proportional to VNL. where VT=KT/q and N is emitter area ratio of transistor Q1 and Q2. In the equation above, VtlnN/R1 is PTAT current compensating the first-order temperature dependency of VEBQ2/R2. Therefore, sum of I1 and I2 is nearly temperature independent. Besides, since emitter current of Q1 and Q3 are PTAT and temperature-independent respectively, (VEBQ2-VEBQ3)/R5 provides current to compensate higher-order temperature dependency in VEBQ2/R2.

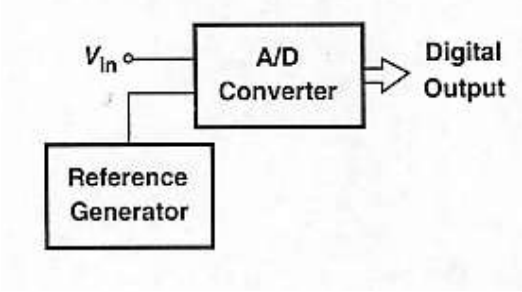
$$V_{out} = R_3\left(\frac{1}{R_1}V_{BE1} + \frac{V_T \ln n}{R_0} + V_{NL}\left(\frac{1}{R_{4,5}}\right)\right)$$
$$= \frac{R_3}{R_1}\left(V_{BE1} + \frac{R_1 \ln n}{R_0}V_T + V_{NL}\left(\frac{R_1}{R_{4,5}}\right)\right), R_{4,5} = \frac{R_1}{\eta - 1} \quad (3.35)$$

3.5.3 Bandgap voltage reference in pipeline ADC

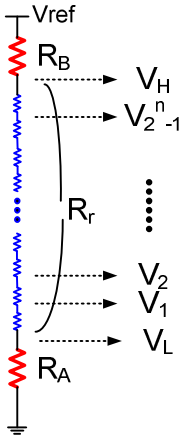
BGR does not only supply accurate voltage reference in ADC, but also generates biasing circuits. Since voltage reference is more accurate and crucial, biasing circuits in pipeline ADC associated with BGR are omitted. The higher the resolution of ADC is, the more accurate BGR is required. Because more decision levels are needed, so the voltage reference should be more detailed. Let's consider PSRR and Temperature coefficient impaction on nonlinearity and accuracy of ADC.

3.5.3.1 Nonlinearity

The reference generator (Figure 3.24a) in ADC is implemented by BGR. It compares the input signal with the reference by comparators. The simplest reference generator is figure 3.24(b). Supposing all the resistors are ideal and don't have mismatching or variations.



(a)



(b)

Figure 3.24 Reference Generator.

V_H is the highest possible input signal value and V_L is the lowest possible input signal value. And BGR generate a voltage reference V_{ref}.

$$\alpha_r = \frac{R_r}{R_{tot}}, \alpha_A = \frac{R_A}{R_{tot}}$$

$$V_H = \frac{R_r + R_A}{R_{tot}} V_{ref} = (\alpha_r + \alpha_A) \times V_{ref}$$

$$V_L = \frac{R_A}{R_{tot}} V_{ref} = \alpha_A \cdot V_{ref}$$

$$V_r = V_H - V_L = \alpha_r \cdot V_{ref}$$

$$\Delta = \frac{V_r}{2^n} = \frac{\alpha_r}{2^n} V_{ref} \tag{3.36}$$

Then all (2n-1)'s the decision levels are:

$For\ 1 \le i \le 2^n - 1$

$$V_i = V_L + i \times \Delta = \alpha_A \cdot V_{ref} + i \times \frac{\alpha_r}{2^n} V_{ref} = \left(\alpha_A + \alpha_r \times \frac{i}{2^n} \right) \times V_{ref} \tag{3.37}$$

$$V_{i+1} = V_L + (i+1) \times \Delta = \left(\alpha_A + \alpha_r \times \frac{i+1}{2^n} \right) \times V_{ref}$$

- DNL $DNL_i = \dfrac{V_{i+1} - V_i - \Delta}{\Delta}$
  - The ideal ADC DNLi=0 (0<i<2n)
  - Practical ADC: voltage reference varies. ΔVref is the variations of BGR. Vref is the ideal value.

$$V_{ref}' = V_{ref} + \Delta_{V_{ref}}$$

$$DNL_i = \frac{V_{i+1}' - V_i' - \Delta}{\Delta} = \frac{\left(\alpha_A + \alpha_r \times \frac{i+1}{2^n} \right) \times V_{ref}' - \left(\alpha_A + \alpha_r \times \frac{i}{2^n} \right) \times V_{ref}' - \Delta}{\Delta}$$

$$= \frac{\frac{\alpha_r}{2^n} \times V_{ref}' - \frac{\alpha_r}{2^n} \times V_{ref}}{\frac{\alpha_r}{2^n} \times V_{ref}} = \frac{\Delta_{V_{ref}}}{V_{ref}} \tag{3.38}$$

- INL

$$INL_i = \frac{V_i' - V_i}{\Delta} = \frac{\left(\alpha_A + \alpha_r \times \frac{i}{2^n} \right) \times V_{ref}' - \left(\alpha_A + \alpha_r \times \frac{i}{2^n} \right) \times V_{ref}}{\Delta}$$

$$= \frac{\left(\alpha_A + \alpha_r \times \frac{i}{2^n} \right) \Delta_{V_{ref}}}{\Delta} = \left(\frac{\alpha_A}{\alpha_r} 2^n + i \right) \frac{\Delta_{V_{ref}}}{V_{ref}} \tag{3.39}$$

  - When i=2n-1, INLi is maximum.

$$INL_{\max} = \left(\frac{\alpha_A}{\alpha_r} 2^n + 2^n - 1 \right) \frac{\Delta_{V_{ref}}}{V_{ref}} \tag{3.40}$$

In order to get no missing code, the requirement of DNL and INL should be:

$$\left| INL_i \right| \le \frac{1}{2},\ for\ all\ i; \quad \left| DNL_i \right| \le 1,\ for\ all\ i \tag{3.41}$$

BGR variations requirement should be:

$$\begin{cases} INL_{\max} = \left(\frac{\alpha_A}{\alpha_r} 2^n + 2^n - 1 \right) \frac{\Delta_{V_{ref}}}{V_{ref}} \le \frac{1}{2} \\ DNL_i = \frac{\Delta_{V_{ref}}}{V_{ref}} \le 1 \end{cases} \Rightarrow \Delta_{V_{ref}} \le \min \left[V_{ref}, \frac{V_{ref}}{2\left(\frac{\alpha_A}{\alpha_r} 2^n + 2^n - 1 \right)} \right] \tag{3.42}$$

3.5.3.2 Accuracy

- PSRR:

  The voltage reference should be varied less than half of 1 LSB; otherwise, wrong voltage comparisons are made. Let's suppose the voltage supply is not stable, varying by ΔVDD, So:

$$\Rightarrow PSRR = 20 \cdot \lg \left(\frac{\Delta V_{DD}}{\Delta V_{ref}} \right) \ge 20 \cdot \lg \left(\frac{\Delta V_{DD}}{V_{ref}} 2 \left(\frac{\alpha_A}{\alpha_r} 2^n + 2^n - 1 \right) \right)$$

$$> 20 \cdot \lg \left(\frac{\Delta V_{DD}}{V_{ref}} 2^{n+1} \left(\frac{\alpha_A}{\alpha_r} + 1 \right) \right) = 6.02(n+1) + 20 \lg \left(\frac{\Delta V_{DD}}{V_{ref}} \right) + 20 \lg \left(\frac{\alpha_A}{\alpha_r} + 1 \right) \tag{3.43}$$

- For example,
  - n=16bit, Vref=2.4V, VDD=3.3V, VL=1.1V, VH=2.225V

$$\alpha_A = \frac{1.1}{2.4}, \alpha_r = \frac{1.125}{2.4}, \Delta VDD = 0.25V$$

  - PSRR=6.02*17-20+6=88.6dB
  - If ΔVDD=10mV, PSRR=60.67dB

- The voltage temperature coefficient:

  The circuit temperature varies during working, which results in the voltage reference variations.

$$TCV_{ref} = \frac{\Delta V_{ref}}{V_{ref}\Delta T} \le \frac{1}{2\left(\frac{\alpha_A}{\alpha_r}2^n + 2^n - 1\right)\Delta T} < \frac{1}{2^{n+1}\left(\frac{\alpha_A}{\alpha_r} + 1\right)\Delta T} \tag{3.44}$$

  - For example,
    - n=16bit, Vref=2.4V, VDD=3.3V, VL=1.1V, VH=2.225V

$$\alpha_A = \frac{1.1}{2.4}, \alpha_r = \frac{1.125}{2.4}$$

$$TCV_{ref} = \frac{1}{2^{n+1}\left(\frac{\alpha_A}{\alpha_r} + 1\right)\Delta T} \approx \frac{2^{-18}}{\Delta T} \approx 3.814 \times 10^{-6} / \Delta T$$

CHAPTER 4

PIPELINE ADC POWER OPTIMIZATION

Typical pipeline ADCs categorized by single-bit and multi-bit per stage perform analog-to-digital conversion process in several stages following an SHA. Each stage is built up with one sub-flash ADC and one MDAC consisting of a switch capacitor DAC and a closed-loop residue amplifier. Three design issues – speed, resolution and power, constitute the performance matrix. The speed is often decided by the settling time of the sample and hold circuit and the residue amplifiers. Besides the non-full settling, capacitor mismatch and gain error due to the finite DC gain of the residue amplifier contribute to the conversion accuracy of data converters. Most of the power dissipation comes from the sample and hold circuit and the residue amplifiers. The potential optimization points in traditional pipelined ADCs are the speed limitation generated from the switch capacitor based closed-loop residue amplifiers, the accurate output range requirement on each stage due to the fixed reference ladder and the capacitor mismatch constrained by the process.

In this section, one optimized pipeline ADC method is proposed to release these design limitation by stage partition and op-amp power to comparator power ratio. The feasibility and performance improvement have been analyzed in detail. The major power dissipation components in each stage of pipeline ADC will be sub-ADC and MDAC. Biasing circuits, clock generators and digital circuitry are much smaller. So, it's

reasonable to neglect these power dissipations. Before structure optimization, some denotation should be clear:

- N as the total number of bits
- B as the number of bits/stage
- n as the number of stages
- F as the normalized total power
- R as ratio between the power consumed by MDAC and that by the comparator

4.1 Pipeline with identical stages

For pipeline ADC with identical stages, the same capacitors are used for all MDACs. To maintain the same speed, the same transconductance is required for the amplifier in each MDAC. So, each MDAC consumes the same power [21].

The total power consumption of the ADC normalized to that of the comparator is derived to be:

$$\begin{aligned} F &= \frac{P_{total}}{P_{comp}} = \frac{n \times P_{MDAC} + n \times (2^B - 2) \times P_{comp}}{P_{comp}} = \frac{n \times P_{MDAC}}{P_{comp}} + n \times (2^B - 2) \\ &= n \times \left[R + (2^B - 2) \right] = \frac{N-1}{B-1} \left[R + (2^B - 2) \right] \end{aligned} \tag{4.1}$$

Figure 4.1 indicates that the total power F increases much faster with the power ratio R for lower B because the number of stages and the number of MDACs required are much larger.

The global minimum value of F can be achieved for B=2 and R=1, which is not practical.

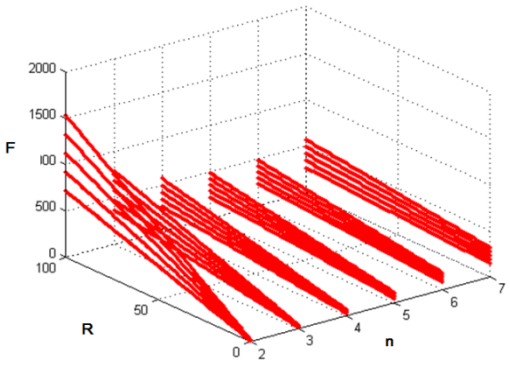


Figure 4.1 Power F vs. R and n.

Differentiating F and solving for Bopt:

$$
\begin{aligned}
F &= \frac{N-1}{B-1}\left[R+(2^B-2)\right] \\
\frac{\partial F}{\partial B} &= \frac{N-1}{B-1}2^B \ln 2 - \frac{N-1}{(B-1)^2}\left[R+(2^B-2)\right] \\
&= \frac{N-1}{(B-1)^2}\left\{2^B\left[(B-1)\ln 2-1\right]-R-2\right\}=0 \\
\Rightarrow R &= 2-2^B\left[1-(B-1)\ln 2\right]
\end{aligned}
\tag{4.2}
$$

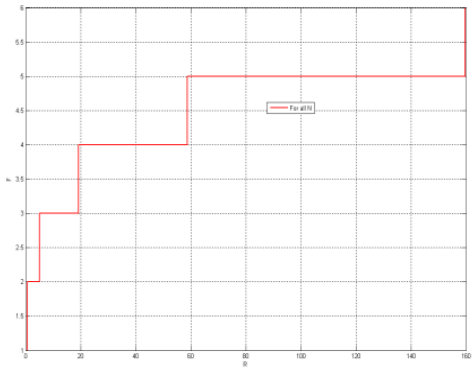


Figure 4.2 optimized power vs. R.

We can get the optimized R as figure 4.2. For every given R, we can get the fixed optimized B. Given a power ratio R, Bopt is independent of the total number of bits N. Fmin only depends on the minimum power dissipated by each stage, which is dependent on Bopt but independent of N [21].

4.2 Pipeline with capacitor scaling

In pipeline ADC, thermal noise kT/C contribution of a later stage is effectively attenuated by the gain of the previous stages.

$$\overline{V_{nin\_total}^{\,2}} = \overline{V_{n1}^{\,2}} + \frac{\overline{V_{n2}^{\,2}}}{A_1^{\,2}} + \ldots + \frac{\overline{V_{nn}^{\,2}}}{A_1^{\,2} A_2^{\,2} \ldots A_{n-1}^{\,2}} \tag{4.3}$$

- $\overline{V_{ni}}$ is the total input noise of the i-th stage.

- Ai is the i-th stage residue gain.

So the capacitor of later stages can be scaled down to reduce their power dissipation without increasing the kT/C noise significantly. In the figure 4.3, the capacitors are scaled down by a factor of S/stage, the power of MDAC can be reduced by the same factor without sacrificing the speed.

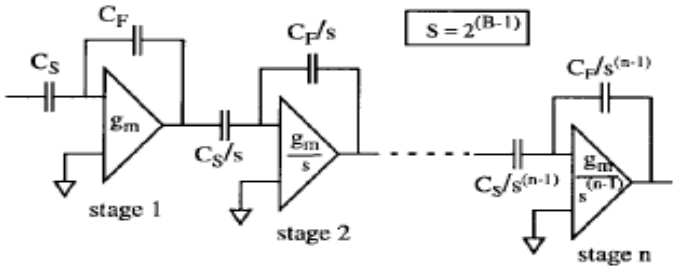


Figure 4.3 Capacitor Scaling Down.

The power consumption in MDAC mainly costs by amplifier. So,

$$
\begin{aligned}
&P_{MDAC} \approx P_{amp} = V_{DD} \times (k \times I_D) \\
&I_D = \frac{1}{2} g_m V_{OD} \\
&g_m = 2\pi \times GWB \times C_L \\
&V_{OD} \approx 5\% \times V_{DD} \\
&\Rightarrow P_{MDAC} \approx V_{DD} \times k \times \frac{1}{2} V_{OD} \times 2\pi \times GWB \times C_L = V_{DD} \times k \times V_{OD} \times \pi \times GWB \times C_L \\
&\qquad = 0.05 k\pi \times {V_{DD}}^2 \times GWB \times C_L
\end{aligned}
\tag{4.4}
$$

As the capacitor scales down by a factor of S, the power consumption is also decrease by the factor of S.

$$For\ C_{L(i+1)} = \frac{C_{L(i)}}{S} => P_{MDAC(i+1)} = \frac{P_{MDAC(i)}}{S}$$

$$P_{total} = P_{MDAC0} + P_{MDAC1} + ... + P_{MDAC(n)} + n \times (2^B - 2) \times P_{comp}$$

$$F = \frac{P_{total}}{P_{comp}} = \frac{\sum_{i=1}^{n} P_{MDAC(i)} + n \times (2^B - 2) \times P_{comp}}{P_{comp}} = \frac{1 - S^{-n}}{1 - S^{-1}} \frac{P_{MDAC0}}{P_{comp}} + n \times (2^B - 2)$$

$$= \frac{1 - S^{-\frac{N-1}{B-1}}}{1 - S^{-1}} R + \frac{N-1}{B-1} \times (2^B - 2) \tag{4.5}$$

a. For low power design, S should be larger;

b. For low noise design, S should be smaller.

a) If $S=G_i=2^{2(B-1)}$,

$$\max\left[\overline{V_{nin\_total}^{\ 2}}\right] = n \times \overline{V_{n1}^{\ 2}},\ \min\left[F\right] = \frac{1 - 2^{-2(N-1)}}{1 - 2^{-2(B-1)}} R + \frac{N-1}{B-1} \times (2^B - 2) \tag{4.6}$$

b) If S=1

$$\min\left[\overline{V_{nin\_total}^{\ 2}}\right] = \overline{V_{n1}^{\ 2}} \times \frac{1 - 2^{-2(N-1)}}{1 - 2^{-2(B-1)}},\ \max\left[F\right] = \frac{N-1}{B-1} R + \frac{N-1}{B-1} \times (2^B - 2) \tag{4.7}$$

The total power for capacitor scaling is always much smaller compared with identical stage case. For a low power ratio R, the total power F for the capacitor scaling case increases exponentially. The power contributed by MDACs is negligibly small and that the total power is basically from the sub-ADCs which depend exponentially on B [21].

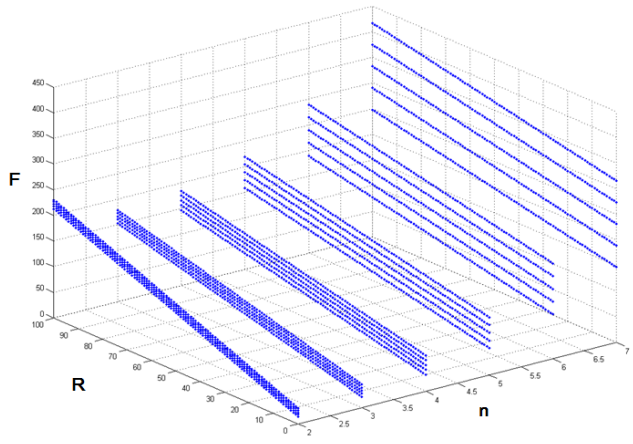


Figure 4.4 Normalized Power F vs. R and n.

Figure 4.4 illuminates that F varies linearly with R for a given N and B for both identical stages and capacitor scaling. F is less sensitive to the total number of bits N for low values of B. (With capacitor scaling, the power consumption of the first MDAC is dominant and that of the last few stages can be neglected. Increasing N and the number of stages n only increase the total power slightly).

$$
\begin{aligned}
&F = \frac{1-2^{-\frac{N-1}{B-1}}}{1-S^{-1}} R + \frac{N-1}{B-1} \times (2^B - 2) \\
&If\ S = 2^{B-1},\ F = \frac{1-2^{-(N-1)}}{1-2^{-(B-1)}} R + \frac{N-1}{B-1} \times (2^B - 2) \\
&\frac{\partial F}{\partial B} = -\frac{1-2^{-(N-1)}}{\left[1-2^{-(B-1)}\right]^2} R \times 2^{-(B-1)} \ln 2 - \frac{N-1}{(B-1)^2} \times (2^B - 2) + \frac{N-1}{B-1} \times 2^B \ln 2 = 0 \\
&\Rightarrow R = \frac{\frac{N-1}{B-1}\left[1-2^{-(B-1)}\right]^2}{2^{-(B-1)} \ln 2 \left[1-2^{-(N-1)}\right]} \times \left[2^B \ln 2 - \frac{(2^B - 2)}{B-1}\right]
\end{aligned}
\tag{4.8}
$$

Figure 4.5 tells that Bopt for capacitor scaling is dependent on the total number of bit N. the flat regions extend over wider ranges of the R because the power consumed by

MDACs are much smaller for later stages. As a result, it would require a much larger increase in R to compensate for an increase in B_{opt}.

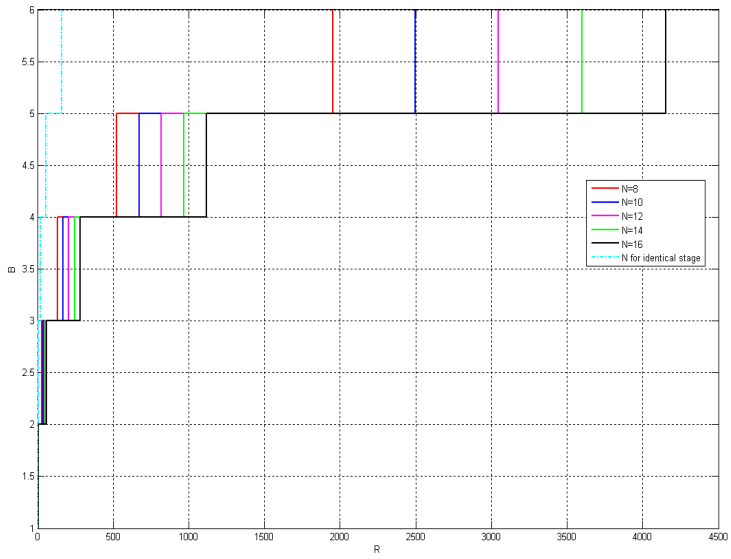


Figure 4.5 Optimized B vs. R.

4.3 Pipeline with resolution scaling

Capacitor scaling only minimizes the power consumption of MDACs and does not affect the power dissipation of sub-ADC. A scheme with no uniform bits/stage is considered to reduce the power contribution of sub-ADC to the whole system.

$$F = \frac{P_{total}}{P_{comp}} = nR + \sum_{i=1}^{n}(2^{B_i} - 2) = nR + \sum_{i=1}^{n} 2^{B_i} - \sum_{i=1}^{n} 2$$
$$= nR + \sum_{i=1}^{n} 2^{B_i} - 2n = n(R-2) + \sum_{i=1}^{n} 2^{B_i} \quad (4.9)$$
$$n = (B_1 + B_2 + ... + B_n + 1) - N$$

For N=16 bits pipeline ADC, the possible stage partition as follows:

1. 5-5-5-4
2. 4-4-4-4-4
3. 5-5-4-3-3
4. 5-4-4-4-3
5. 4-4-4-3-3-3
6. 4-3-3-3-3-3-3
7. 4-4-3-3-3-3-2
8. 4-4-4-3-3-2-2
9. 3-3-3-3-3-3-3-2
10. 4-3-2-2-2-2-2-2-2-2-2-2

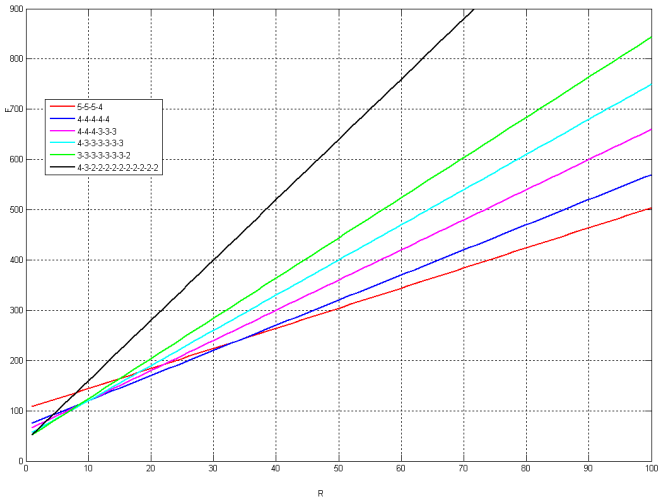


Figure 4.6 Optimized Power vs. R.

All the possible power consumption curves are drawn in figure 4.6. None of the bit patterns can yield a global minimum power for all power ratio R. From a low value of R, one pattern may achieve the local minimum power. As R becomes large enough, another pattern will take over. Both resolution scaling and capacitor scaling should be considered. $S=2^{Bi-1}$

$$P_{total} = \sum_{i=1}^{n} P_{MDAC(i)} + \sum_{i=1}^{n} P_{Sub-ADC(i)}$$

$$= \left(P_{MDAC1} + P_{MDAC2} + \ldots + P_{MDACn}\right) + \left[\left(2^{B_1} - 2\right) + \left(2^{B_2} - 2\right) + \ldots + \left(2^{B_n} - 2\right)\right] \times P_{comp}$$

$$= \left(P_{MDAC} + \frac{P_{MDAC}}{2^{B_2 - 1}} + \frac{P_{MDAC}}{2^{B_2 - 1} \times 2^{B_3 - 1}} + \ldots + \frac{P_{MDAC}}{\prod_{i=2}^{n} 2^{B_n - 1}} \right) + \left[\left(\sum_{i=1}^{n} 2^{B_i} \right) - 2n \right] \times P_{comp} \qquad (4.10)$$

$$F = \frac{P_{total}}{P_{comp}} = R \left(1 + \frac{2}{2^{B_2}} + \frac{2^2}{2^{B_2 + B_3}} + \ldots + \frac{2^{n-1}}{\prod_{i=2}^{n} 2^{B_n}} \right) + \left(\sum_{i=1}^{n} 2^{B_i} \right) - 2n$$

$$n = (B_1 + B_2 + \ldots + B_n + 1) - N$$

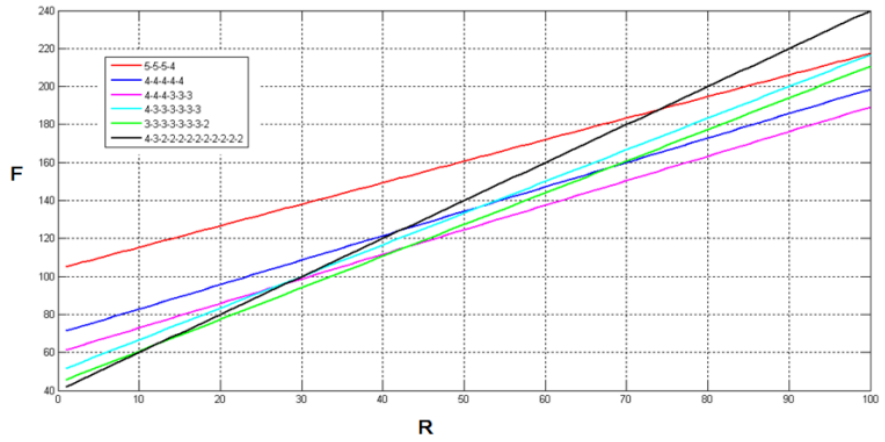


Figure 4.7 Optimized Power with Both Capacitor and Resolution Scaling vs. R.

Using different scaling factor S, the global minimum power dissipation would be quite different. In practice, due to technology and layout constraints, a minimum value of capacitor that can be used may exist [21]. Minimizing the total chip area may put an upper limit on the maximum capacitor value that can be designed. So, the capacitors for

the first few and last few stages may need to remain un-scaled, and the scaling scheme would not be as effective and would need to be modified.

4.4 Pipeline ADC power optimization with thermal noise

This section shows how to find optimized scaling factor and number of stages with power and thermal noise limitation with ADC specification. Figure 4.8 shows the pipeline ADC structures. Suppose the stages are identical expect the capacitance scaling. This means each stage has the same digital output, has the same op-amp structure but the power consumption might not be the same because of the capacitance scaling. On one hand, if N-bits pipeline ADC has only one stage, the parasitic capacitance of comparators is huge because this stage has 2^N-1 comparators.

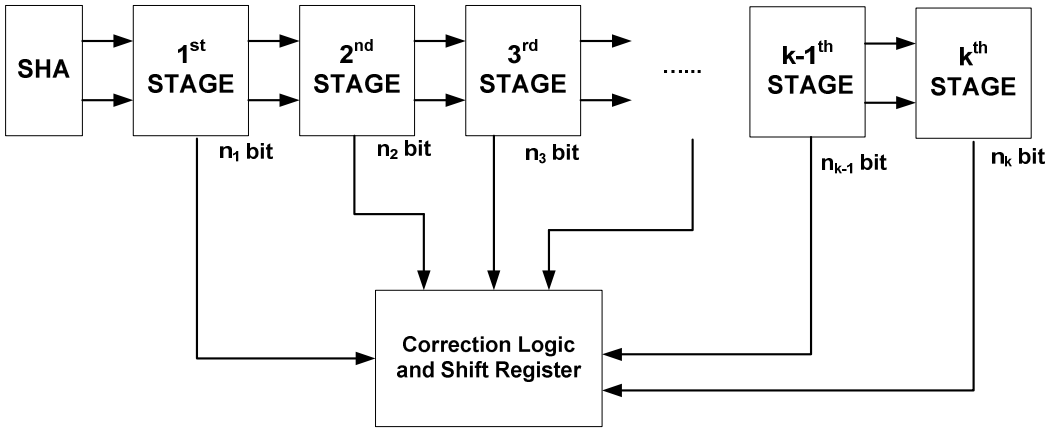


Figure 4.8 Pipeline ADC Structures.

As the N is 8~16 bits, the number of comparator is dominant. However, on the other hand, if each stage only has one bit digital output, N bit pipeline ADC need N

stages, every stage will have one op-amp, which consume lots of power. So, there must be same optimized partition for pipeline ADC, the number of stage must sit between 1 and N.

In pipeline ADC, thermal noise kT/C contribution of a later stage is effectively attenuated by the gain of the previous stages.

$$\overline{V_{nin\_total}^{\,2}} = \overline{V_{n1}^{\,2}} + \frac{\overline{V_{n2}^{\,2}}}{A_1^{\,2}} + \ldots + \frac{\overline{V_{nn}^{\,2}}}{A_1^{\,2}A_2^{\,2}\ldots A_{n-1}^{\,2}} \tag{4.11}$$

$\overline{V_{ni}}$ is the total input noise of the i-th stage, A_i is the i-th stage residue gain. The capacitor of later stages can be scaled down to reduce their power dissipation without increasing the kT/C noise significantly. In the left figure, the capacitors are scaled down by a factor of S/stage; the power of MDAC can be reduced by the same factor without sacrificing the speed. The follow is some definition of ADC. A_C is the close-loop gain; f is the feedback factor of op-amps. M is the number of stage. $C_{s,k}$ is the sampling capacitor of k^{th} stage; $C_{L,k}$ is the total load capacitor of k^{th} stage; C_{flash} is the total comparators capacitor of each stage. s is the scaling factor of pipeline ADC.[3]

$$A_C = 2^{n_s-1} \quad f = \frac{1}{A_C} \quad M = \left\lfloor \frac{N-1}{n_s-1} \right\rfloor$$

$$C_{s,k} = (A_C - 1)C_{F,k} \quad C_{L,k} = A_C C_{F,k+1} + C_{flash} \quad C_{flash} = 4A_C(A_C-1)C_{unit} \quad a = \frac{C_{unit}}{C_{s0}} \tag{4.12}$$

In MDAC, the most important noise sources are sampling switches and thermal noise in the op-amp. In the analysis we ignore flicker noise of op-amps and kickback noise from comparators.

So the total output noise generated by sampling switches of SHA is:

$$\overline{v_{in}^2} = \frac{2K_B T}{C_{s0} f_0},\ f_0 = \frac{C_{s0}}{C_{s0} + C_g} \tag{4.13}$$

The total output noise generated by sampling switches of MDAC is:

$$\overline{v_{in}^2} = \frac{2K_B T}{(C_s + C_F) f_0 A_C},\ f = \frac{C_F}{C_s + C_g + C_F} \tag{4.14}$$

Thermal noise contribution of op-amps is:

$$\begin{aligned} \beta &= \frac{\sum_{noise\ contributor} g_m}{g_{m,input}} \\ \overline{v_{in,diff}^2} &= \frac{\frac{4}{3}\beta K_B T}{\left[C_L + C_F(1-f)\right] f_0 A_C{}^2},\ f = \frac{C_F}{C_s + C_g + C_F} \end{aligned} \tag{4.15}$$

So, the total output thermal noise generated by op-amps of SHA is:

$$\overline{v_{in}^2} = \frac{2K_B T}{C_{s0} f_0} + \frac{\frac{4}{3}\beta K_B T}{\left[C_{L0} + C_{s0}(1-f)\right] f} \tag{4.16}$$

The total output thermal noise generated by op-amps of MDAC is:

$$\overline{v_{in,k}^2} = \frac{2K_BT}{f{A_C}^2 C_{F,k}} + \frac{\frac{4}{3}\beta K_BT}{{A_C}^2\left[C_{L,k} + C_{F,k}(1-f)\right]f} \tag{4.17}$$

As the results, the total input referred thermal noise of ADC is:

$$\begin{aligned}
&\overline{v_{tot,input}^2} = \overline{v_{in,SHA}^2} + \sum_{k=1}^{M} \frac{\overline{v_{in,k}^2}}{{A_C}^{2k}} \\
&= \frac{2K_BT}{C_{s0}}\left[1 + \frac{2\beta}{3}\frac{1}{C_{L0}/C_{s0}}\right] + \sum_{k=1}^{M}\frac{1}{{A_C}^{2k}}\frac{2K_BT}{{A_C}^3}\left[\frac{1}{C_{F,k}} + \frac{2\beta}{3}\frac{1}{C_{L,k} + C_{F,k}(1-f)}\right] \\
&= \frac{2K_BT}{C_{s0}}\left\{\left(1 + \frac{2\beta A_C}{3}\frac{1}{\frac{A_C}{A_C-1}s + 4A_C(A_C-1)a}\right) + \sum_{k=1}^{M}\frac{1}{{A_C}^{2k}}\frac{2K_BT}{{A_C}^3}\left[\frac{A_C-1}{s^k} + \frac{2\beta}{3}\frac{1}{\frac{A_C}{A_C-1}s^{k+1} + \frac{s^k}{A_C} + 4A_C(A_C-1)a}\right]\right\}
\end{aligned} \tag{4.18}$$

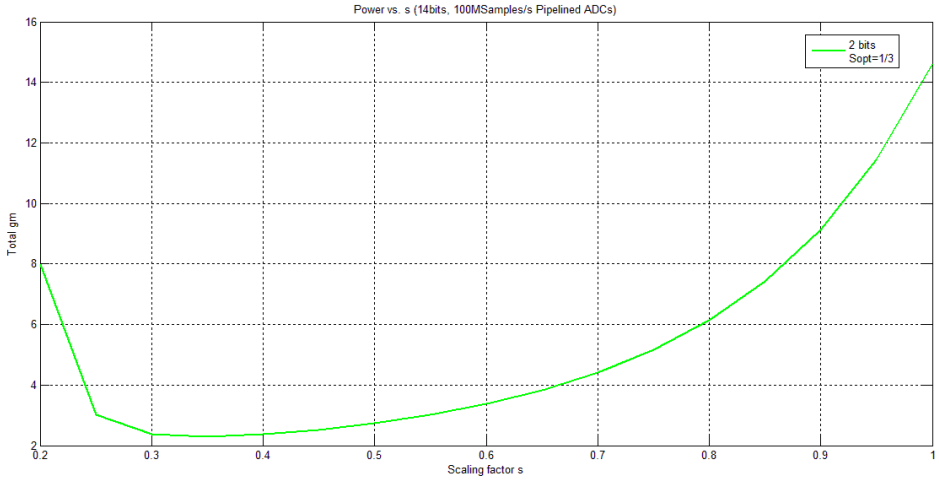
So all the input referred thermal noise must be smaller than quantizer error:

$$N_{thermal} = N_{quant} < \frac{LSB^2}{12} \tag{4.19}$$

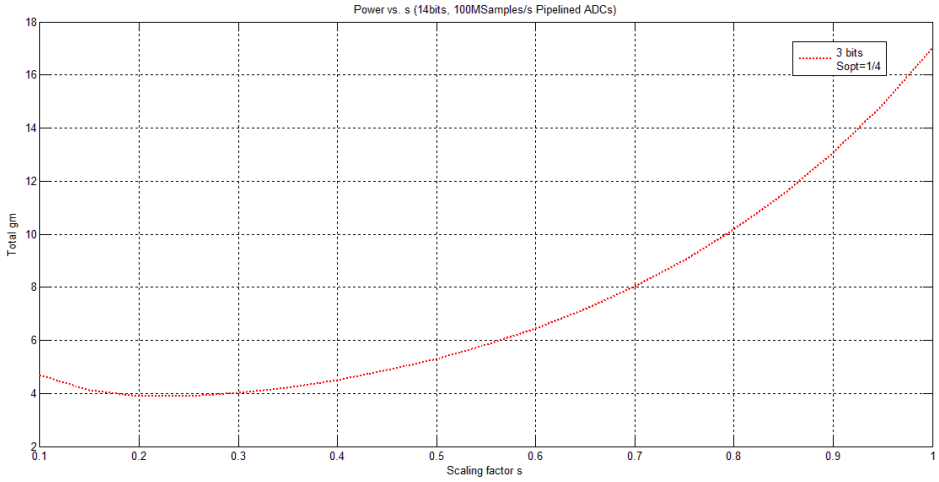
Then, we will get the minimum size of capacitors according to different scaling factors. The next step is to find the optimized scaling factor s. Let's consume power consumption in SHA and MDACs is proportional to $g_{m,input}$, then we can get the total g_m as follows:

$$\begin{aligned}
&\tau = \frac{C_L + C_F(1-f)}{fg_m} \Rightarrow g_{m,k} = \frac{C_{L,k} + C_{F,k}(1-f)}{\tau_k f} \\
&g_{m,total} = g_{m,0} + \sum_{k=1}^{M} g_{m,k} = \frac{C_{L,0}}{\tau_0} + \sum_{k=1}^{M}\frac{C_{L,k} + C_{F,k}(1-f)}{\tau_k f} \\
&\quad = \frac{C_{s0}A_C}{\tau_0}\left[\frac{s}{A_C-1} + 4(A_C-1)a\right] + C_{s0}A_C\left[\sum_{k=1}^{M}\frac{\frac{A_C}{A_C-1}s^{k+1} + \frac{1}{A_C}s^k + 4A_C(A_C-1)a}{\tau_k}\right]
\end{aligned} \tag{4.20}$$

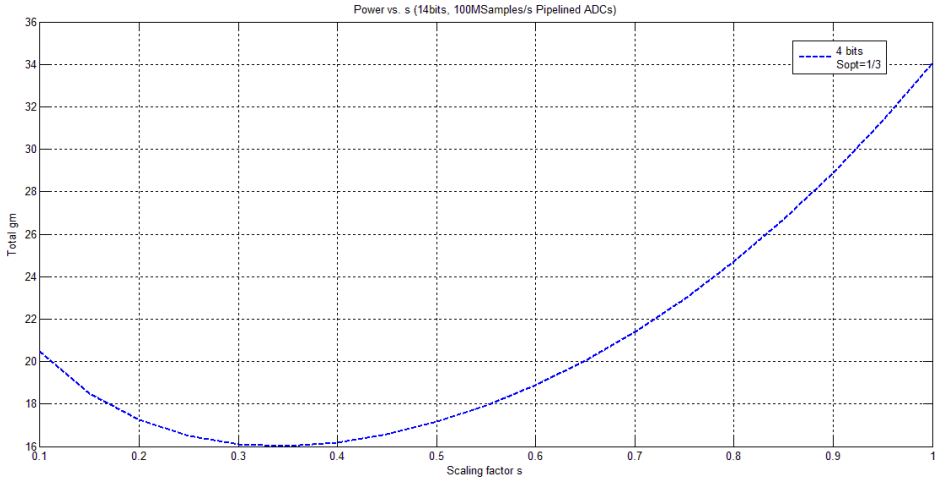
Figure 4.9 shows the power consumption with respect to capacitor scaling based on different stage partition. Figure 4.9(a) is the 2-bits per stage partition, and optimized scaling factor is 1/3; Figure 4.9(b) is the 3-bits per stage partition, and optimized scaling factor is 1/4; Figure 4.9(c) is the 4-bits per stage partition, and optimized scaling factor is 1/3; Figure 4.9(d) finds the overall optimized stage partition: 2-bits per stage is the best. Figure 4.9(e) shows the minimum capacitor of first stages with respect to scaling factor and different stage partition. As a result, the best choice of the most cases, if consider power optimization and thermal noise impact, is 2-bits per stage and the scaling factor should be 1/3.



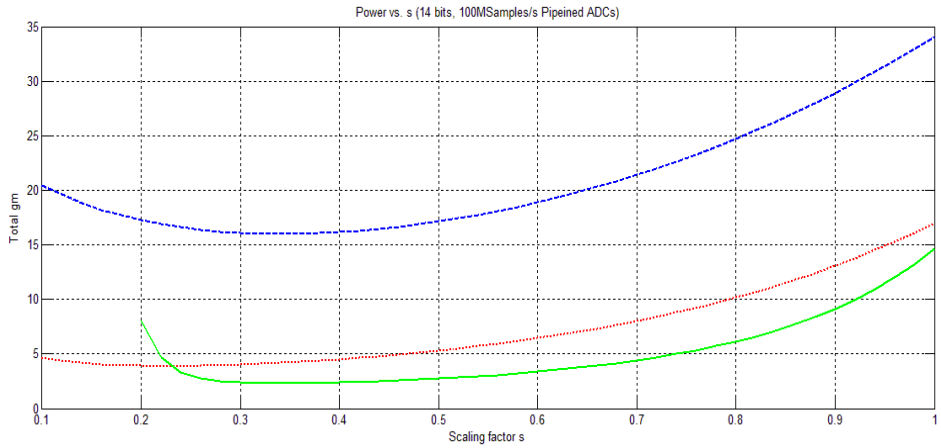
(a)


Power vs. s (14bits, 100MSamples/s Pipelined ADCs)
3 bits
Sopt=1/4
Total gm
Scaling factor s
18
16
14
12
10
8
6
4
2
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

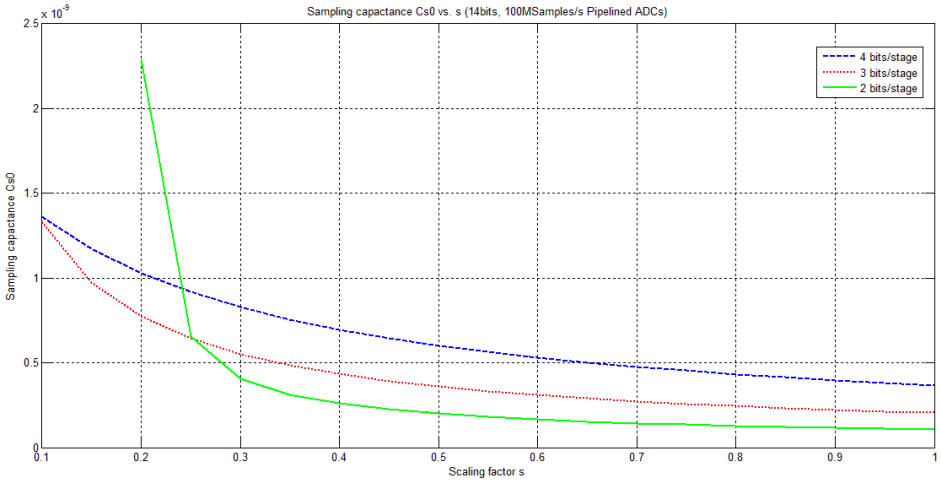
(b)


Power vs. s (14bits, 100MSamples/s Pipelined ADCs)
4 bits
Sopt=1/3
Total gm
Scaling factor s
36
34
32
30
28
26
24
22
20
18
16
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

(c)



(d)



(e)

Figure 4.9 Power vs. Capacitor Scaling Based on Different Stage Partition.

CHAPTER 5

PIPELINE ADC DESIGN EXAMPLE

5.1 State of art

There are various types of pipeline ADC design (sampling rate: 10M~500Msample/sec, resolution: 8~16 bits). Here only middle range sampling rate (around 40Msamples/sec) and middle range resolution (10 bits) are listed, since in the following section, one 40Msamples/sec, 10-bits pipeline ADC will present in order to verify the pipline design methodology.

	Technology	Bits	Bits/Stage	SNDR [dB]	Speed [Msamples/sec]	Power [mA]
Loloee 2002 [82]	0.18um	12	1-1-1-1-1-1-1-1-1-1-2	65	80	144.44
Bogner [83]	0.13um	14	3-3-2-2-4	64	100	150
Yoshioka [84]	90nm	10	1-1-1-1-1-1-1-1-1-3	56	80	13.3
Lee [85]	90nm	10	2-2-2-4	54	30	4.7
This work	90nm (3.3V IO)	10	1-1-1-1-1-1-1-1-1-2	55	40	12.7

Table 5.1 State of art

5.2 10-bits hybrid ADC specifications

Based on this pipeline ADC methodology study, this chapter presents a 10bit 40MHz power adaptive hybrid ADC with TSMC 90nmLP process: using op-amp sharing, dynamic biasing methods, it works in two modes: pipelined ADCs for high speed, cyclic ADC for low speed (only last stage runs, other stages are power off to save power). For pipeline mode, the total power consumption decrease as the sampling frequency drops.

This power adaptive Pipelined ADC has a target on applications in image sensor capturing, video processing, wireless communications, biomedicine, digital-intermediate frequency (IF) receivers and countless of digital devices. General pipelined ADC power consumption is almost the same no matter what sampling rate it works at. That's because the total current of the most power consuming component, OP-AMP, maintains the same. It will waste lots of power if ADC sampling rate is not reach to maximum. This new pipelined ADC has self-adaptive switched-capacitor biasing circuitry, which will help ADC reduce power when it works at low sampling rate while maintaining the same performance.

The specification of this hybrid ADC is shown in table 5.2; and the pins definition of pipeline ADC is shown in table 5.3.

	Our specs	Notes
Process	TSMC 90nm LP	
Resolution	10 bits	
Sampling Rate	maximum 40MHz/s	
Power Supply	2.2V~3.0V	For ADC core;
Input Range	1Vp-p	Peak-to-peak input range
Power Dissipation	2~14mA	Power listed excludes I/O buffer, reference voltage, and digital error correction power. Current is adaptive with sampling rate: For higher sampling rate, power consumption reaches to maximum.
DNL	Typical: +/- 0.3 LSB; Max: +/- 1 LSB	Mismatching and offset error will be reduced by self-correction and digital calibration. So, the DNL and INL will be small enough to guarantee no missing code/level.
INL	Typical: +/- 0.5 LSB; Max: +/- 1 LSB	
SFDR	53dB @ Low speed 50dB @ 40MHz/s	
SNDR	58dB @ Low speed 53dB @ 40MHz/s	
ENOB	9.3 bit	
Output mode	CMOS	
Digital Output	Offset binary output	

Table 5.2 Hybrid Pipeline ADC Specification.

Mode_control signal controls the ADC function. When Mode_control=1, the ADC works in pipeline way; while, if the Mode_control=0, the ADC works in cyclic way.

Pin	I/O type	Numbers	Notes
D1~D10	Output	10	10-bits digital output
VDD	Input	1	Power supply
GND	Input	1	Power supply
Mode_control	Input	1	ADC function controller
Vin+	Input	1	Differential signal input positive
Vin-	Input	1	Differential signal input negative
CLOCK	Input	1	Sampling clock
Vrefp	Input	1	Voltage reference
Vrefn	Input	1	Voltage reference
Vcom	Input	1	Voltage reference
Ibias	Input	1	Current biasing

Table 5.3 Pins Definition of Pipeline ADC.

5.3 Top level structure

Figure 5.1 shows the overall structure of hybrid ADC. It consist of 4stages MDAC (first 3 stages are identical, last stage works for pipeline and cyclic, its size is half

of the first 3 stages), dynamic biasing, control unit, non-overlapping clock generator and digital error correction.

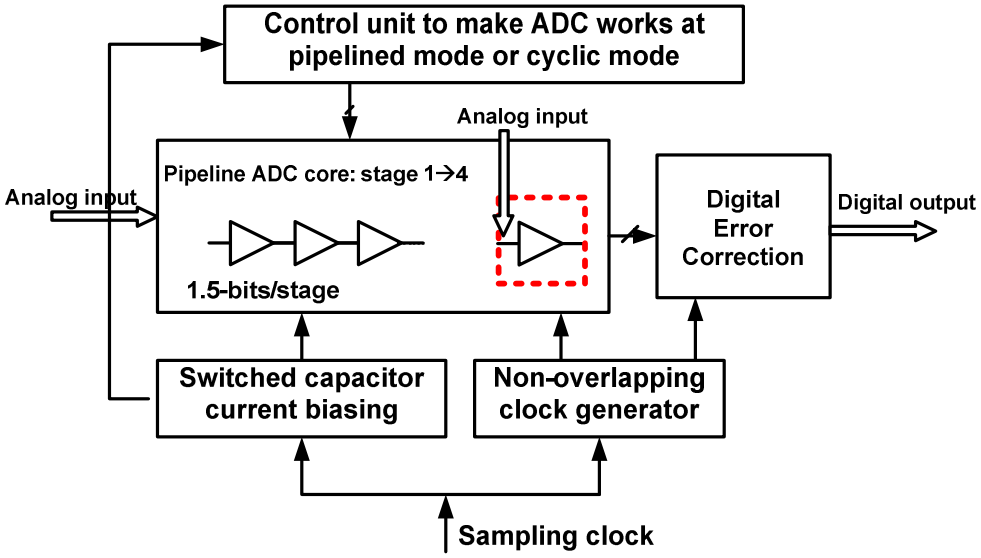


Figure 5.1 Hybrid ADC.

5.3 Sub-blocks structure

This section talks all the important sub-block schematic of hybrid ADC, which includes clock generator, dynamic biasing, comparator, MDAC, op-amps.

5.3.1 Non-overlapping clock generator

The non-overlapping clock generator (Figure 5.2) is built by digital inverters and nand gates. It will generate time delay and make two sets of non-overlapping clock: ph1 and ph2. At the same time, it will also generate ph1e and ph2e, whose falling edges are a

little bit earlier than that of ph1 and ph2. Ph1e and ph2e will be used in MDAC for bottom sampling capacitance technology.

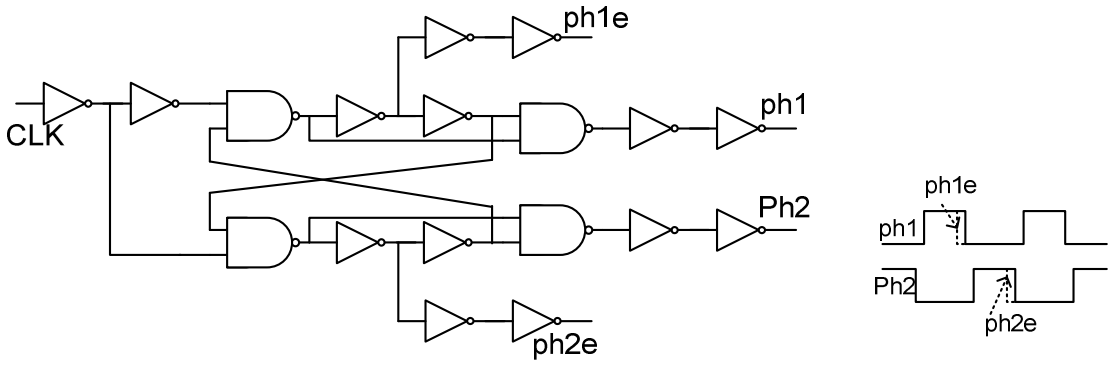


Figure 5.2 Non-overlapping Clock Generator.

5.3.2 Comparators

Section 3.2 shows three types of comparators. In this design, another comparator is used (shown in Figure 5.3). The advantage of this comparator is that it has self-biased voltage decision level:

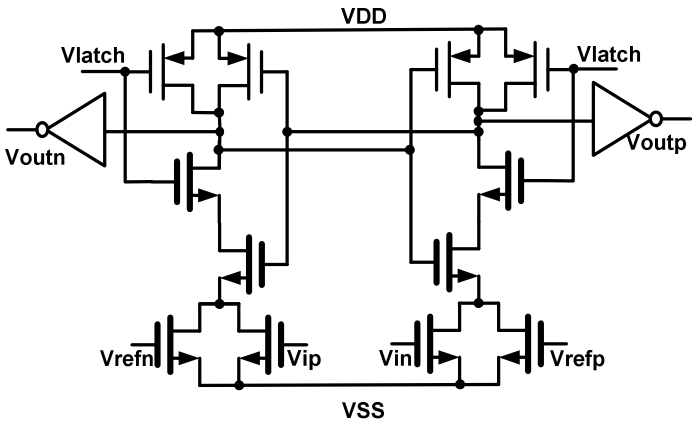


Figure 5.3 Comparator.

$$V_{ip} - V_{in} = \frac{(W/L)_1}{(W/L)_2}(V_{refp} - V_{refn}) \tag{5.1}$$

5.3.3 Switched capacitor current source

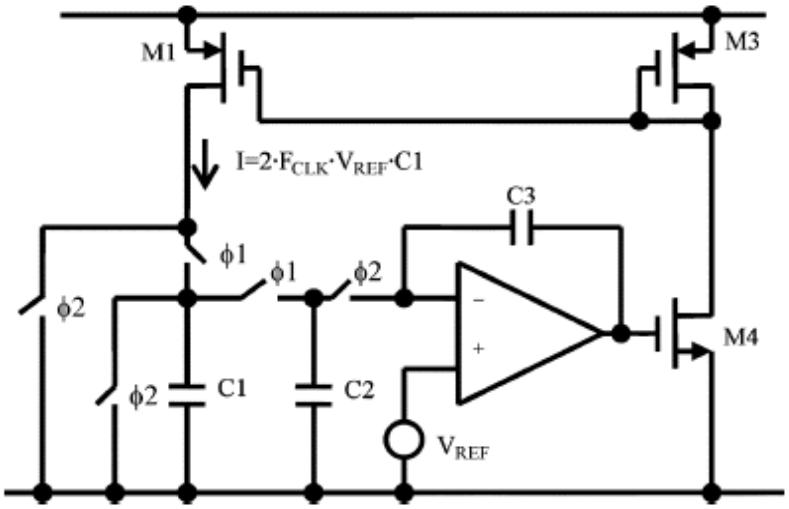


Figure 5.4 Dynamic Biasing.

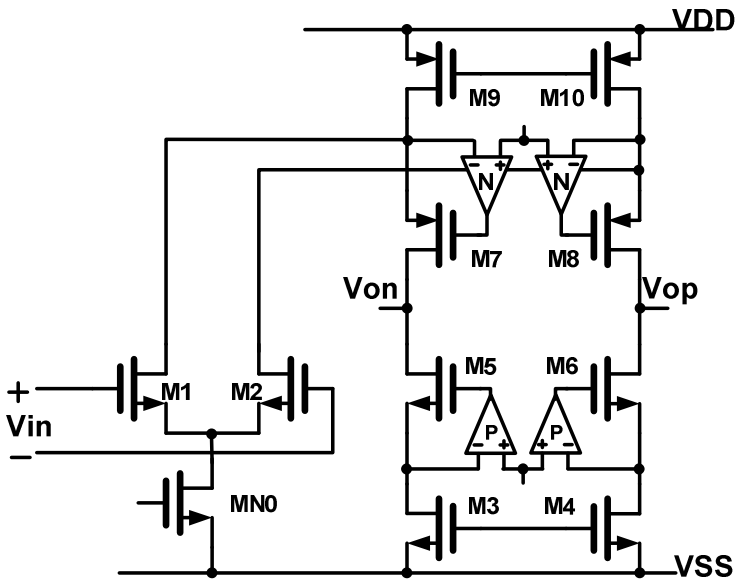
Switched capacitor can works as a resistor; so, current could be modulated with sampling rate. At high sampling rate, op-amps in MDACs need more power to make accurate data acquisition; however, at low frequency, op-amps has more time to compute, as a result, its power could be reduced by adaptive biasing circuitry, at the same time, maintaining the same function.

The current of op-amps might vary 10 times if working at quite different sampling rate, which could have input differential pairs worked in weak saturation or triode region.

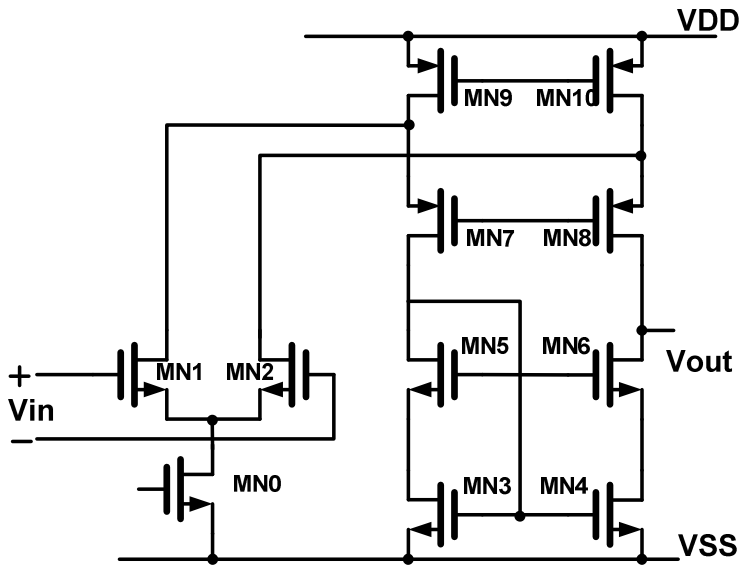
A control unit is applied to select whether ADC works pipelined normal mode or Low power cyclic mode.

5.3.4 OP-AMP

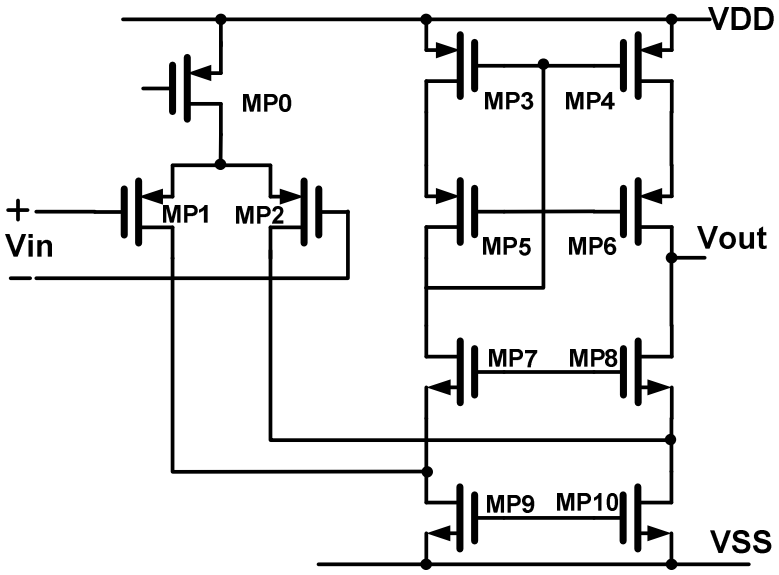
This design uses fold-cascoding op-amp, although telescopic op-amp is the most power efficient one. The reason is that fold-cascoding op-amp has larger output swing range. This is important, especially for dynamic biasing, because the current runs through transistors vary 10 times.



(a)



(b)



(c)

Figure 5.5 (a) Folded-cascade Op-amp with Gain Boosting (b) N-type Additional Op-amp (c) P-type Additional Op-amp.

5.3.4 MDAC

This design uses 1.5 bit per stage MDAC, and at the same time, using op-amp sharing. Traditional MDAC can only solve 1.5 bit per stage, and have 8 stages for 10 bit ADC. However, using op-amp, only 4 stages are enough. For traditional structures, op-amp only works at half the period: one half of the period for signal sampling to capacitors, at this time, op-amp does nothing; the other half of the period, op-amp amplifies the signals. So op-amp wastes half the power for waiting. Using op-amp sharing technology, one op-amp works for two stages, and it will work all the time. As shown in figure 5.6, now 1st, 2nd, 3rd stage are the same. They will get 6 sets of 2-bit output while only have 3 op-amps.

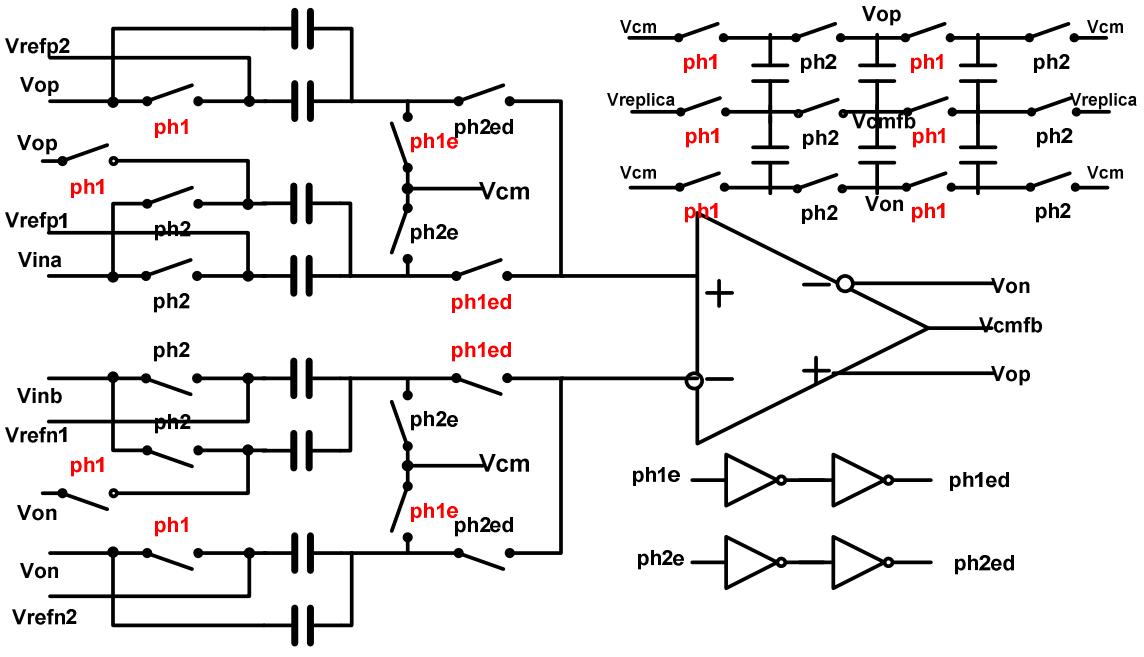


Figure 5.6 1st 2nd 3rd MDAC.

The last stage (Figure5.7) works in pipeline and cyclic way. So, in pipeline mode, switches of ph2_1 and ph2_2345 are turn off. So no signal connects Vina_cyc/Vinb_cyc to op-amp. It works as normal pipeline ADC. However, if ADC works in cyclic way: these switches of ph2_1 and ph2_2345 are turn on according to scheme of figure 5.8.

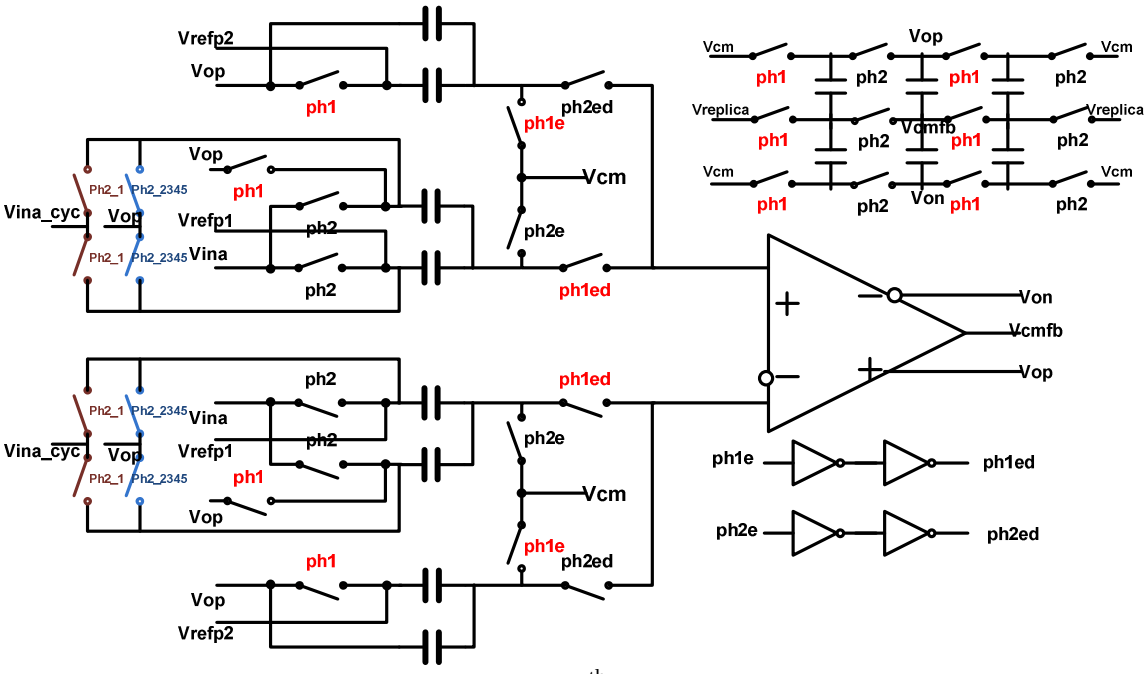


Figure 5.7 4th MDAC.

Using 1~5 counter to control the switches during cyclic processing.

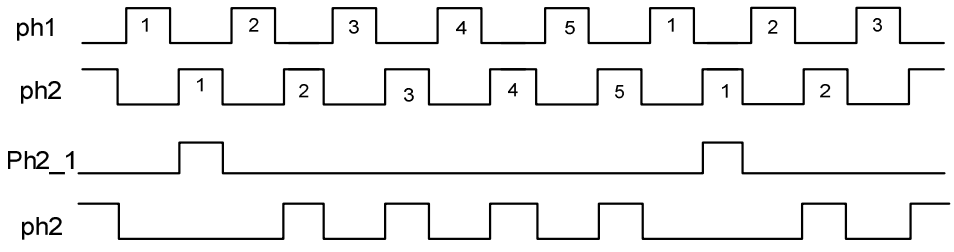


Figure 5.8 Phase Scheme of Cyclic ADC.

5.4 Overall layout

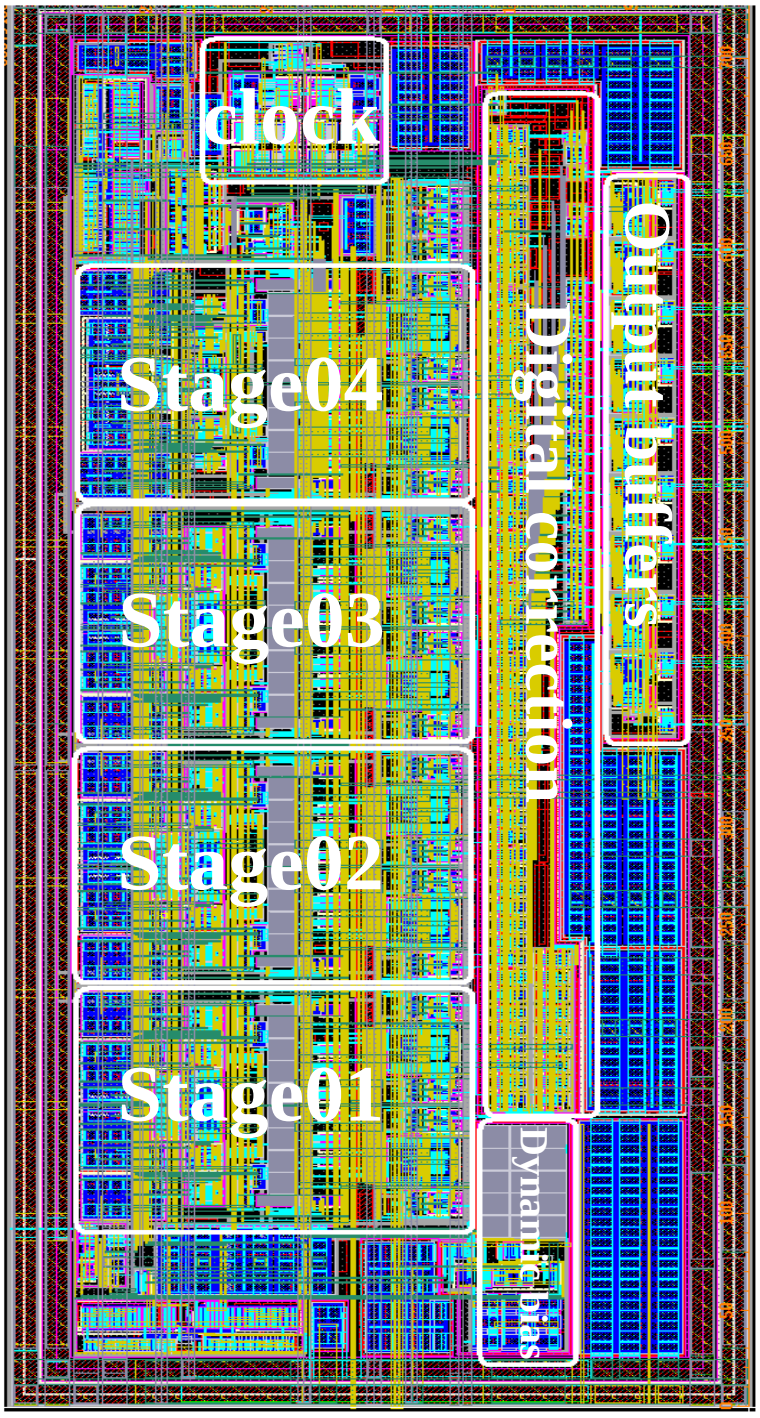


Figure 5.9 Layout.

As shown in figure 5.9, the overall area of hybrid ADC is 700um x 310um without pads.

5.5 Simulation results

Figure 5.10 shows the total power consumption with respect to sampling rate. If ADC works in pipeline mode, the total power consumption changes from 4.2 mA up to 12.2 mA, while the sampling rate increases from 4Msamples/second to 40 Msamples/second(blue curve). The black curve shows the total power consumption of cyclic mode, it's much smaller than pipeline mode, and almost constant, since only 4th stage are turn on, while other three stages and dynamic biasing circuitry are turn off.

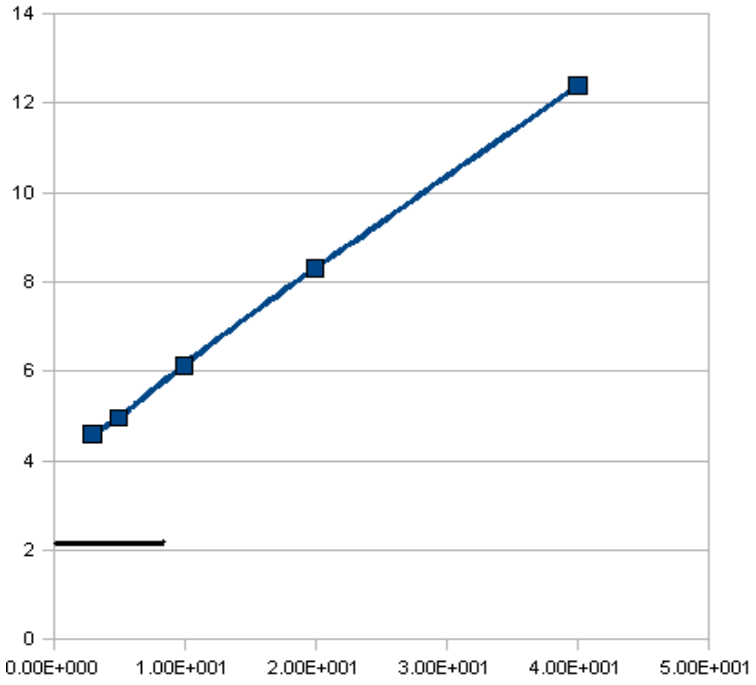


Figure 5.10 Total Power Consumption vs. Sampling Frequency.

If input signal is applied to a ramp signal, the output signal is upstairs signal. No-missing code occurs in Figure 5.11.

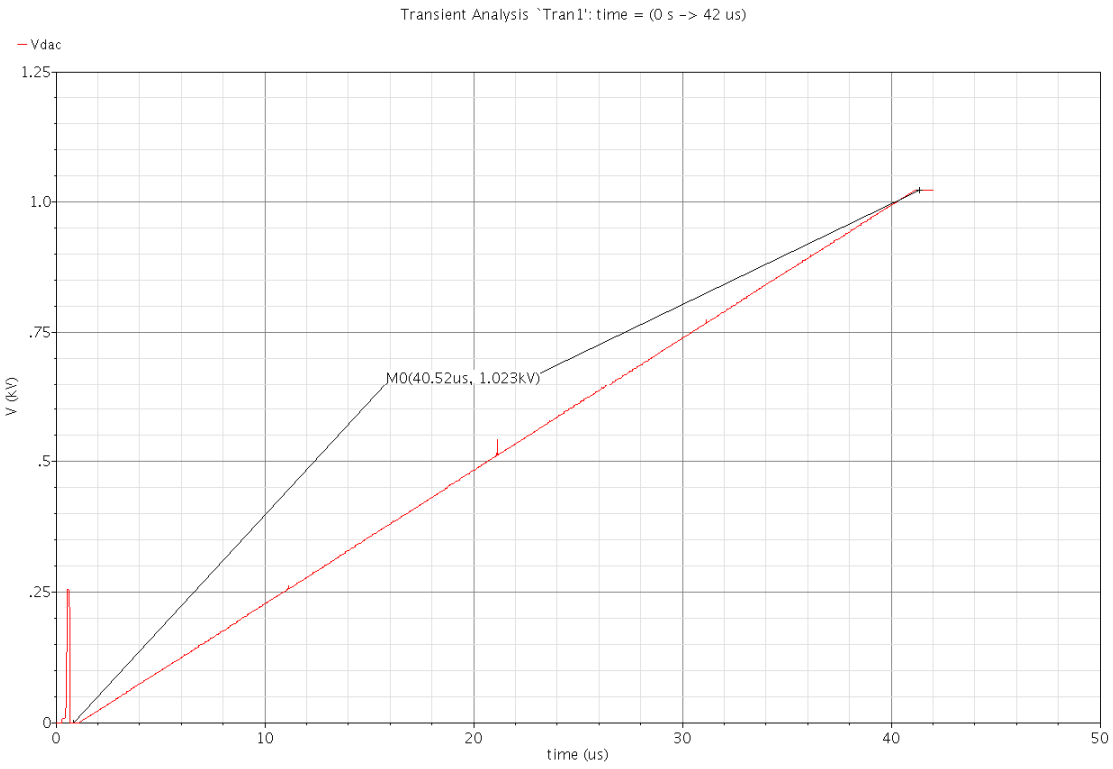
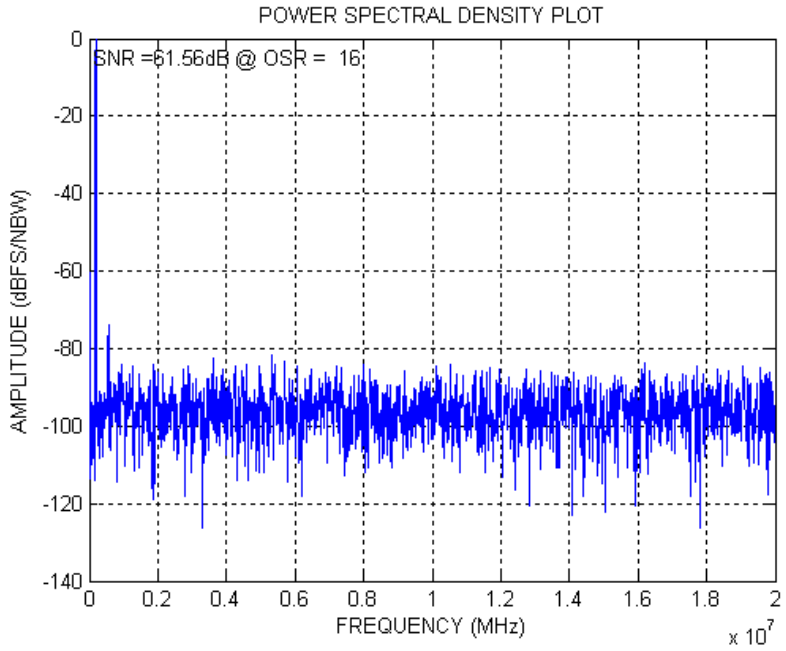
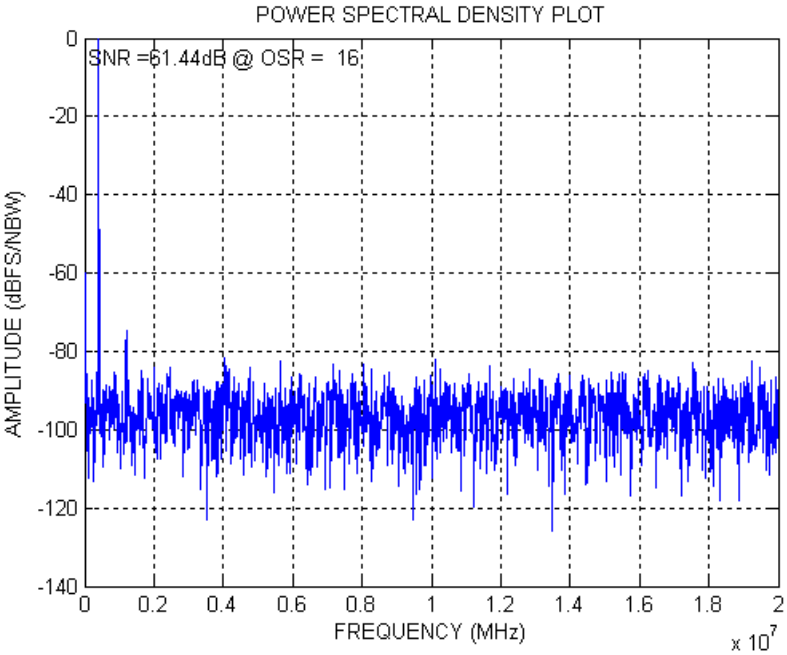


Figure 5.11 Ramp Signal to Verify Monotonicity.

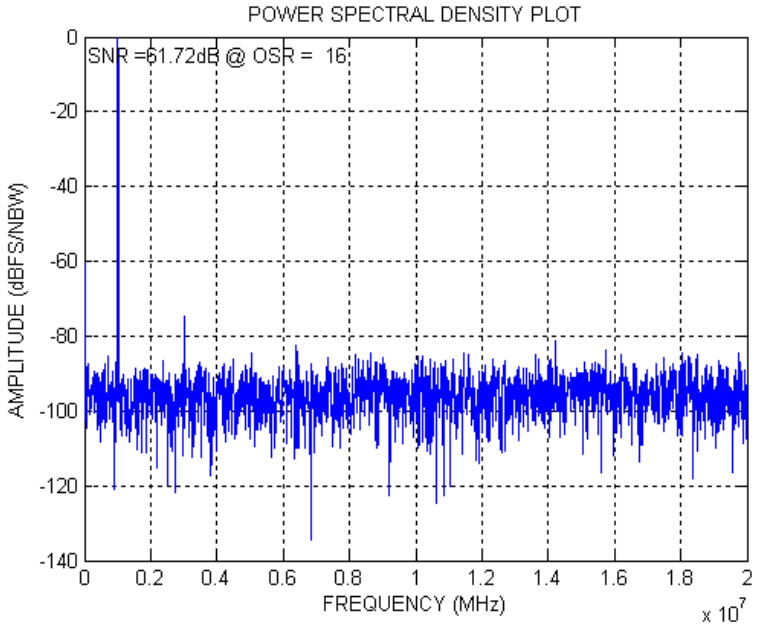
Figure 5.12 shows the spectrum analysis of different input signal frequency. The input signal frequency is: 185546.875Hz, 400390.625Hz, 1005859.375Hz, 3994140.625 Hz, 9970703.125 Hz, and 19697265.63Hz, while the sampling rate is the maximum rate: 40Msamples/second. The number of samples is 2^{12}=4096 points. Using FFT analysis, the SNR, ENOB results as follows (Figure 5.13).


POWER SPECTRAL DENSITY PLOT
SNR =61.56dB @ OSR = 16
AMPLITUDE (dBFS/NBW)
FREQUENCY (MHz)
x 10^7
0
-20
-40
-60
-80
-100
-120
-140
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

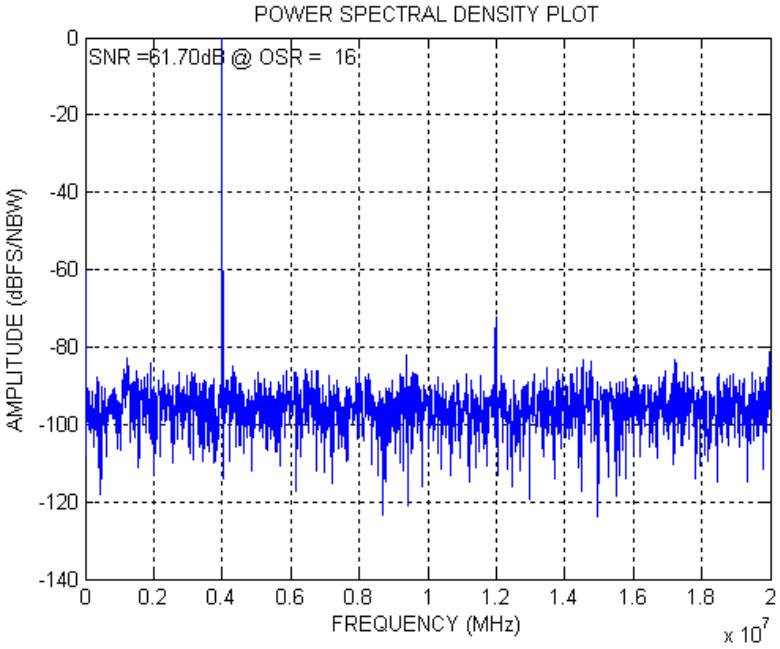
(a)


POWER SPECTRAL DENSITY PLOT
SNR =61.44dB @ OSR = 16
AMPLITUDE (dBFS/NBW)
FREQUENCY (MHz)
x 10^7
0
-20
-40
-60
-80
-100
-120
-140
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

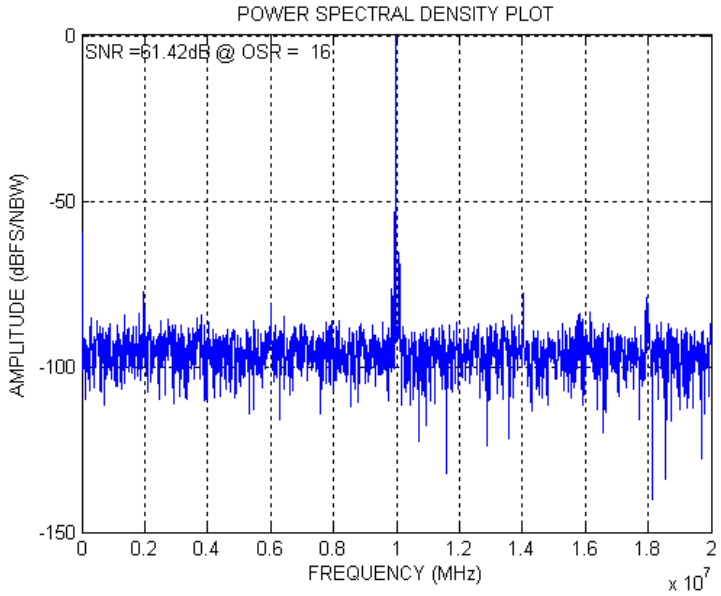
(b)


POWER SPECTRAL DENSITY PLOT
SNR =61.72dB @ OSR = 16
AMPLITUDE (dBFS/NBW)
FREQUENCY (MHz)
x 10^7
0
-20
-40
-60
-80
-100
-120
-140
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

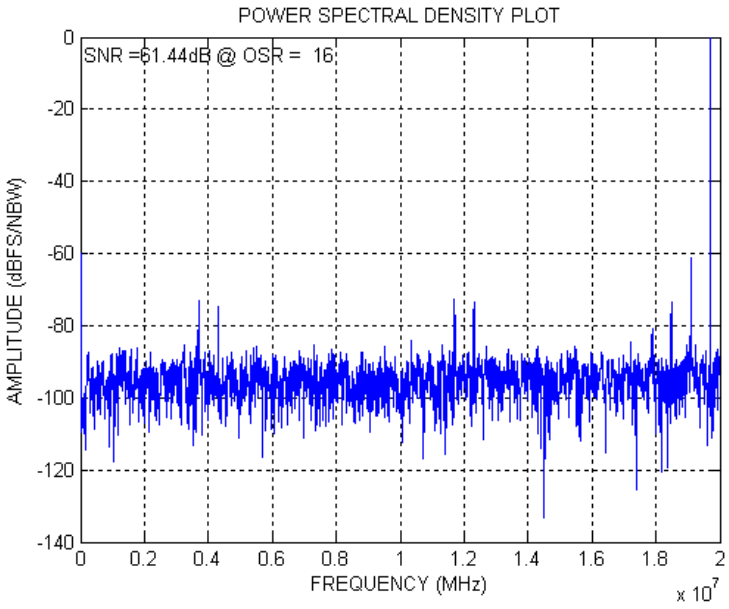
(c)


POWER SPECTRAL DENSITY PLOT
SNR =61.70dB @ OSR = 16
AMPLITUDE (dBFS/NBW)
FREQUENCY (MHz)
x 10^7
0
-20
-40
-60
-80
-100
-120
-140
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2

(d)

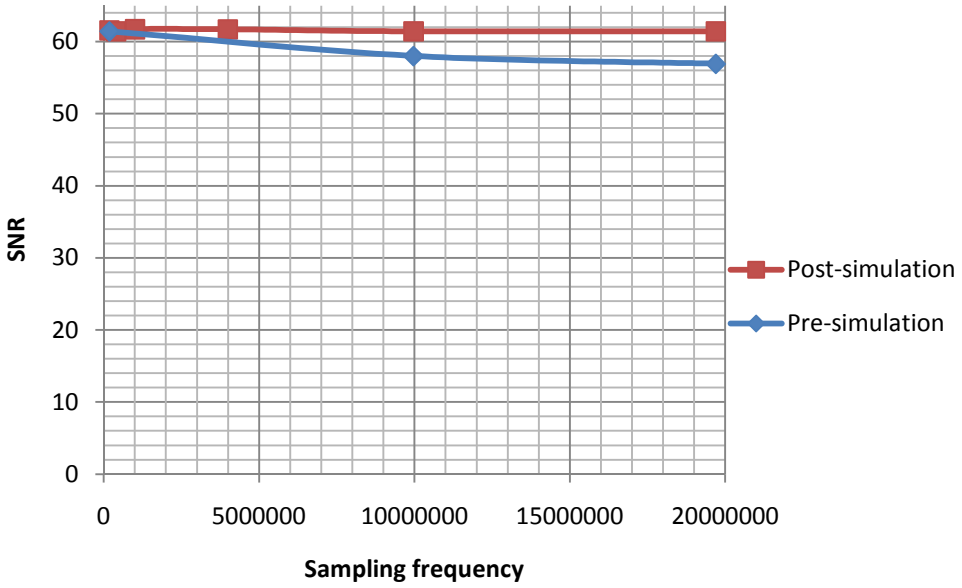


(e)



(f)

Figure 5.12 Spectrum Analysis.



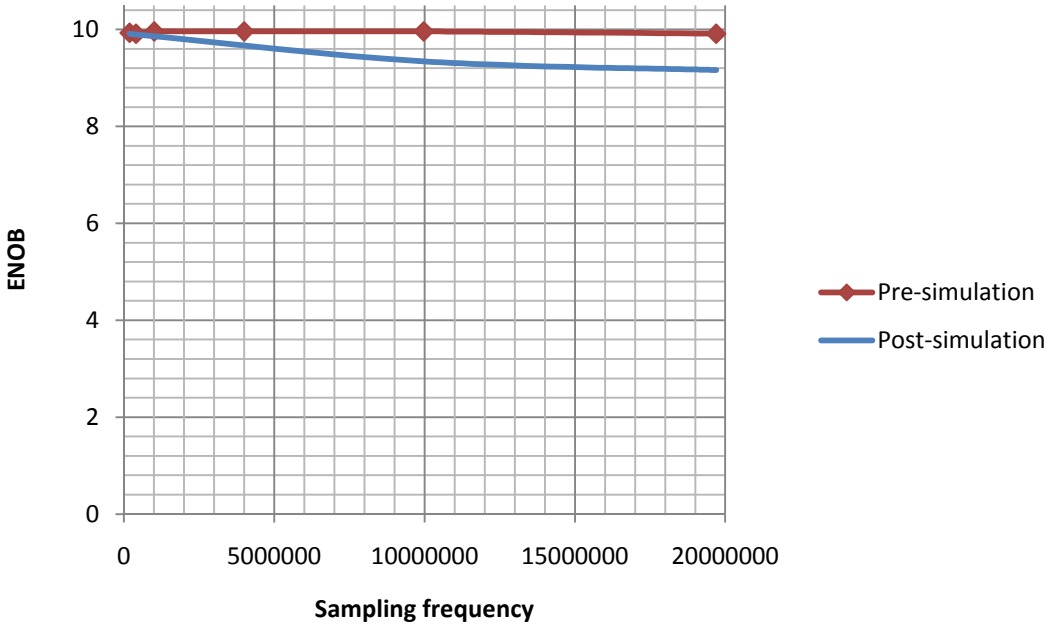


Figure 5.13 SNR and ENOB.

CHAPTER 6

CONCLUSIONS

6.1 Conclusions

The thesis presents a comprehensive pipeline ADC design methodology. The pipeline ADC design methodology provides a comprehensive and quantitative mapping matrix between system level ADC performance specs (e.g., power optimization, sampling rate, resolution, input voltage range, etc.) and the critical design parameters at block levels, such as, thermal noise limitation, op-amp selection in S/H and MDAC, DC gain and closed-loop gain bandwidth of op-amps requirement, sampling capacitor selection criterion etc.

The design methodology was verified by designing a 10-bit 40Msample/second hybrid ADC using TSMC 90nm IO device process. This hybrid ADC uses op-amp sharing method to save half number of stages, and, it can work in two modes: pipelined ADCs for high speed, cyclic ADC for low speed (only last stage runs, other stages are power off to save power).It also adapts dynamic biasing methods, so, for pipeline mode, the total power consumption decrease as the sampling frequency drops.

6.2 Future Work

First, offset of op-amp worse the pipeline ADC performance. For traditional MDAC, it's easy to implement offset cancellation technology, such as auto-zeroing, since op-amps works only in half of the period. So it can store the offset at the other half of the period, and subtract the offset then. While, using op-amp sharing method, op-amps are always working. So auto-zeroing cannot implement into it. Some advanced technology should be considered, such as chopping.

Second, digital calibration [38, 39, 42, 54, 56, 62, 65, 72, 78, 79, 81] would help improve ADC performance: SNR, SFDR, mismatching and so on. Based on this hybrid ADC design, new digital calibration scheme should be developed in the future in order to improve ADC performance.

REFERENCE

[1] Mikael Gustavsson, J. Jacob Wikner and Nianxiong Nick Tan, "*CMOS DATA CONVERTERS FOR COMMUNICATIONS*", Kluwer Academic Publishers, 2000.

[2] Jaehyun Lim, "*Analog-to-Digital Converters*", Department of Computer Science and Engineering, the Pennsylvania State University, Mixed Signal Chip Design Lab.

[3] David William Cline, "*Noise, Speed and Power trade-offs in Pipelined Analog-to-Digital Converter*", University of California at Berkeley.

[4] Behzad Razavi, "*Principles of Data Conversion System Design*", the Institute of Electrical and Electronics Engineers, Inc., New York, 1995.

[5] Yunchu Li, "*Design of High Speed Folding and Interpolating Analog-to-Digital Converter*", Texas A&M University, May 2003.

[6] Haideh Khorramabadi, "*Analog-Digital Interface Integrated Circuits*", Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, 2007.

[8] Christoph Sandner, et al, "*A 6-bit 1.2GSps Low-Power Flash ADC in 0.13μm Digital CMOS*", IEEE Solid-State Circuits Conference, Sept. 2004, pp.339-342.

[9] Thomas W. Matthews, "*On the Effective Sampling Time of Regenerative Comparators*", IEEE 2008

[10] Pedro M. Figueiredo and João C. Vital, "*LOW KICKBACK NOISE TECHNIQUES FOR CMOS LATCHED COMPARATORS*", IEEE ISCAS 2004.

[11] T. SUNDSTRÖM, A. ALVANDPOUR, "*A Kick-Back Reduced Comparator for a 4-6-Bit 3-GS/s Flash ADC in a 90nm CMOS Process*" IEEE MIXDES 2007

[12] Shan Jiang, Manh Anh Do, Kiat Seng Yeo, "*200-MHz CMOS Mixed-Mode Sample-and-Hold Circuit for Pipelined ADCs*", IEEE 2006 IFIPA.

[13] Wen-rong Yang, Jia-dong Wang, "*Design and Analysis of a High-speed Comparator in a Pipelined ADC*", IEEE Proceedings of HDP'07

[14] Yun Chiu, Paul R. Gray, "*A 14-b 12-MS/s CMOS Pipeline ADC With Over 100-dB SFDR*", IEEE JSSCC VOL. 39, NO. 12, DEC 2004

[15] Joao Goes, Joao C. Vital and Jose E. France, "*Systematic design for optimization of high-speed self-calibrated pipelined A/D Converters*", IEEE Trans on Circuits and systems II: Analog and digital processing, VOL.45, NO. 12, DEC., 1998

[16] Olujide A. Adeniran and Andreas Demosthenous, "*An Ultra-Energy-Efficient Wide-Bandwidth Video Pipeline ADC Using Optimized Architectural Partitioning*", IEEE Trans on Circuits and systems I: regular papers, VOL.53, NO. 12, DEC., 2006

[17] Shan Jiang, Manh Anh, "*An 8-bit 200MSample/s, Pipelined ADC with Mixed-Mode Front-End S/H Circuit*", IEEE Trans on Circuits and systems I: regular papers, Feb., 2006

[18] Athon Zanikopoulos, Pieter Harpe, "*Power Optimization for pipelined ADCs with Open-Loop Residue Amplifiers*", IEEE 2006

[19] Tlaas Bult and Govert J.G.M. Geelen, "*A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain*", IEEE JSSCC, VOL.25, NO.6, DEC, 1990.

[20] Wenhua Yang, Dan Kelly and Iuri, "*A 3-V 340-mV 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input*", IEEE JSSCC, VOL. 36, NO 12, DEC, 2001.

[21] Paulux T. F. Kwok and Howard C. Luong, "*Power Optimization for Pipeline Analog-to-Digital Converters*", IEEE Trans on circuits and systems II: Analog and digital processing, VOL. 46, NO. 5, MAY, 1999.

[22] Jaime Ramirez-Angulo, Lalitha Mohana Kalyani-Garimella, "*An Input Stage for the Implementation of Low-Voltage Rail to Rail Offset Compensated CMOS Comparators*", IEEE 21st International Conference on VLSI Design, 2008.

[23] Hsin-Shu Chen, Bang-Sup Song, and Kantilal Bacrania, "*A 14-b 20-MSamples/s CMOS Pipelined ADC*", IEEE JSSCC, VOL. 36, NO. 6, JUNE, 2001.

[24] Boris Murmann and Bernhard E. Boser, "*A 12-bit 75-MS/s, Pipelined ADC Using Open-Loop Residue Amplification*", IEEE JSSCC, VOL. 38, NO. 12, DEC., 2003.

[25] Sang-Min Yoo, Jong-Bum Park, Seung-Hoon Lee, and Un-Ku Moon, "*A 2.5-V 10-b 120-MSample/s CMOS Pipelined ADC Based on Merged-Capacitor Switching*", IEEE Trans on circuits and systems II: Express brief, VOL. 51, NO. 5, MAY 2004.

[26] Pedro M. Figueiredo, and Joao C. Vital, "*Kickback Noise Reduction Techniques for CMOS Latched Comparators*", IEEE Trans on circuits and systems II: Express brief, VOL. 53, NO. 7, JULY, 2006.

[27] Behzad Razavi, and Bruce A. Wooley, "*Design Techniques for High-Speed, High-Resolution Comparators*", IEEE JSSCC VOL. 27, NO. 12, DEC. 1992.

[28] Adriana Becker-Gomez, T. Lakshmi Viswanathan, and T.R Viswananthan, "*A Low-Supply-Voltage CMOS Sub-Bandgap Reference*", IEEE Trans on circuits and systems II: Express brief, VOL. 55, NO. 7, JULY, 2008.

[29] Ka Nang Leung, and Philip K. T. Mok, "*A Sub-1-V 15-pmm/oC CMOS Bangap Voltage Reference Without Requiring Low Threshold Voltage Device*", IEEE JSSCC VOL. 37, NO. 4, APRIL 2002.

[30] Raymond T. Perry, Stephen H. Lewis, and T.R. Viswanathan, "*A 1.4V Supply CMOS Fractional Bandgap Reference*", IEEE JSSCC VOL. 42, NO. 10, OCT. 2007.

[31] Hironori Banaba, Hitoshi Shiga and Koji Sakui, "*A CMOS Bandgap Reference Circuit with Sub-1-V Operation*", IEEE JSSCC VOL. 34, NO. 5, MAY 1999.

[32] Andrea Boni, "*Op-amps and Startup Circuits for CMOS Bandgap References with Near 1-V Supply*", IEEE JSSCC VOL. 37, NO. 10, OTC 2002.

[33] Ka Nang Leung, Philip K. T. Mok, and Chi Yat Leung, "*A 2-V 23-uA 5.3-ppm/oC Curvature-Compensated CMOS Bandgap Voltage Reference*", IEEE JSSCC VOL. 38, NO. 3, MARCH 2003.

[34] Ming-Dou Ker, and Jung-Sheng Chen, "*New Curveature-Compensation Technique for CMOS Bandgap Reference With Sub-1-V Operation*", IEEE Trans on circuits and systems II: Express brief, VOL. 53, NO. 8, AUGUST 2006.

[35] Abdelhlim Bendali and Yues Audet, "*A 1-V CMOS Current Reference With Temperature and Process Compensation*", IEEE Trans on circuits and systems I: Regular papers, VOL. 54, NO. 7, JULY, 2007.

[36] Waltari, M.; Halonen, K.A.I., "*1-V 9-Bit Pipelined Switched-Opamp ADC*", IEEE Journal of Solid-State Circuits, Volume 36, page 129 - 134, Jan 2001.

[37] Bo Xia; Valdes-Garcia, A.; Sanchez-Sinencio, E., "*A 10-bit 44-MS/s 20-mW Configurable Time-Interleaved Pipeline ADC for a Dual-Mode 802.11b/Bluetooth Receive*", IEEE Journal of Solid-State Circuits, Volume 41, page 530 - 539, 2006.

[38] Lee, K.-H.; Kim, Y.-J.; Kim, K.-S.; Lee, S.-H., "*14 bit 50 MS/s 0.18um CMOS pipeline ADC based on digital error calibration*", IEEE Journal of Solid-State Circuits, Volume 45, page 1067 - 1069, 2009.

[39] Dumont, S.; Gandy, P.; Erdmann, C.; Gamand, P., "*14-bit CMOS pipeline ADC with dual-calibration*", IEEE Journal of Solid-State Circuits, Volume 43, page 33 - 34, 2007.

[40] Kurose, D.; Ito, T.; Ueno, T.; Yamaji, T.; Itakura, T., "*55-mW 200-MSPS 10-bit Pipeline ADCs for Wireless Receivers*", IEEE Journal of Solid-State Circuits, Volume 41, page 1589 - 1595, 2006.

[41] Junhua Shen; Kinget, P.R., "*A 0.5-V 8-bit 10-Ms/s Pipelined ADC in 90-nm CMOS*", IEEE Journal of Solid-State Circuits, Volume 43, page 787 - 795, 2008.

[42] Seung-Hoon Lee; Young-Ju Kim; Hee-Cheol Choi; Gil-Cho Ahn, "*A 1.2-V 12-b 120-MS/s SHA-Free Dual-Channel Nyquist ADC Based on Midcode Calibration*", IEEE Journal of Solid-State Circuits, Volume 56, page 894 - 901, 2009.

[43] Van de Vel, H.; Buter, B.A.J.; van der Ploeg, H.; Vertregt, M., "*A 1.2-V 250-mW 14-b 100-MS/s Digitally Calibrated Pipeline ADC in 90-nm CMOS*", IEEE Journal of Solid-State Circuits, Volume 44, page 1047 - 1056, 2009.

[44] Jipeng Li; Un-Ku Moon, "*A 1.8-V 67-mW 10-bit 100-MS/s Pipelined ADC Using Time-Shifted CDS Technique*", IEEE Journal of Solid-State Circuits, Volume 39, page 1468 - 1476, 2004.

[45] Sang-Min Yoo; Jong-Bum Park; Seung-Hoon Lee; Un-Ku Moon, "*A 2.5-V 10-b 120-MSample/s CMOS Pipelined ADC Based on Merged-Capacitor Switching*", IEEE Transactions on Circuits and Systems II, volume 51, page 269 - 275, 2004.

[46] Hui Pan; Segami, M.; Choi, M.; Ling Cao; Abidi, A.A., "*A 3.3-V 12-b 50-MS/s A/D Converter in 0.6um CMOS with over 80-dB SFDR*", IEEE Journal of Solid-State Circuits, Volume 35, page 1769 - 1780, 2000.

[47] Yang, W.; Kelly, D.; Mehr, L.; Sayuk, M.T.; Singer, L., "*A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input*", IEEE Journal of Solid-State Circuits, Volume 36, page 1931 - 1936, 2001.

[48] Hui Liu; Hassoun, M., "*A 9-b 40-MSample/s Reconfigurable Pipeline Analog-to-Digital Converter*", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Volume 49, page 449 - 456, 2002.

[49] Miyazaki, D.; Kawahito, S.; Furuta, M., "*A 10-b 30-MS/s Low-Power Pipelined CMOS A/D Converter Using a Pseudodifferential Architecture*", IEEE Journal of Solid-State Circuits, Volume 38, page 369 - 373, 2003.

[50] Jong-Bum Park; Sang-Min Yoo; Se-Won Kim; Young-Jae Cho; Seung-Hoon Lee, "*A 10-b 150-MSample/s 1.8-V 123-mW CMOS A/D Converter With 400-MHz Input Bandwidth*", IEEE Journal of Solid-State Circuits, Volume 39, page 1335 - 1337, 2004.

[51] Byung-Geun Lee; Tsang, R.M., "*A 10-bit 50 MS/s Pipelined ADC With Capacitor-Sharing and Variable gm Opamp*", IEEE Journal of Solid-State Circuits, Volume 44, page 883 - 890, 2009.

[52] Sumanen, L.; Waltari, M.; Halonen, K.A.I., "*A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter*", IEEE Journal of Solid-State Circuits, Volume 36, page 1048 - 1055, 2001.

[53] Seung-Chul Lee; Young-Deuk Jeon; Jong-Kee Kwon; Jongdae Kim, "*A 10-bit 205-MS/s 1.0-mm2 90-nm CMOS Pipeline ADC for Flat Panel Display Applications*", IEEE Journal of Solid-State Circuits, Volume 42, page 2688 - 2695, 2007.

[54] Seung-Chul Lee; Kwi-Dong Kim; Jong-Kee Kwon; Jongdae Kim; Seung-Hoon Lee, "*A 10-bit 400-MS/s 160-mW 0.13um CMOS Dual-Channel Pipeline ADC Without*

Channel Mismatch Calibration", IEEE Journal of Solid-State Circuits, Volume 41, page 1596 - 1605, 2006.

[55] Mu-Chen Huang; Shen-Iuan Liu, "*A 10-MS/s-to-100-kS/s Power-Scalable Fully Differential CBSC 10-Bit Pipelined ADC With Adaptive Biasing*", IEEE Transactions on Circuits and Systems II, volume 57, page 11 - 15, 2010.

[56] Xiaoyue Wang; Hurst, P.J.; Lewis, S.H., "*A 12-Bit 20-Msample/s Pipelined Analog-to-Digital Converter With Nested Digital Background Calibration*", IEEE Journal of Solid-State Circuits, Volume 39, page 1799 - 1808, 2004.

[57] Yun Chiu; Gray, P.R.; Nikolic, B., "*A 14-b 12-MS/s CMOS Pipeline ADC With Over 100-dB SFDR*", IEEE Journal of Solid-State Circuits, Volume 39, page 2139 - 2151, 2004.

[58] Hsin-Shu Chen; Bang-Sup Song; Bacrania, K., "*A 14-b 20-MSamples/s CMOS Pipelined ADC*", IEEE Journal of Solid-State Circuits, Volume 36, page 997 - 1001, 2001.

[59] Byung-Geun Lee; Byung-Moo Min; Manganaro, G.; Valvano, J.W., "*A 14-b 100-MS/s Pipelined ADC With a Merged SHA and First MDAC*", IEEE Journal of Solid-State Circuits, Volume 43, page 2613 - 2619, 2008.

[60] Ali, A.M.A.; Dillon, C.; Sneed, R.; Morgan, A.S.; Bardsley, S.; Kornblum, J.; Lu Wu, "*A 14-bit 125 MS/s IF/RF Sampling Pipelined ADC With 100 dB SFDR and 50 fs Jitter*", IEEE Journal of Solid-State Circuits, Volume 41, page 1846 - 1855, 2006.

[61] Iizuka, K.; Matsui, H.; Ueda, M.; Daito, M., "*A 14-bit Digitally Self-Calibrated Pipelined ADC With Adaptive Bias Optimization for Arbitrary Speeds Up to 40 MS/s*", IEEE Journal of Solid-State Circuits, Volume 41, page 883 - 890, 2006.

[62] Hung-Chih Liu; Zwei-Mei Lee; Jieh-Tsorng Wu, "*A 15-b 40-MS/s CMOS Pipelined Analog-to-Digital Converter With Digital Background Calibration*", IEEE Journal of Solid-State Circuits, Volume 40, page 1047 - 1056, 2005.

[63] Kwak, S.-U.; Song, B.-S.; Bacrania, K., "*A 15-b, 5-Msample/s Low-Spurious CMOS ADC*", IEEE Journal of Solid-State Circuits, Volume 32, page 1866 - 1875, 1997.

[64] Yun-Shiang Shu; Bang-Sup Song, "*A 15-bit Linear 20-MS/s Pipelined ADC Digitally Calibrated With Signal-Dependent Dithering*", IEEE Journal of Solid-State Circuits, Volume 43, page 342 - 350, 2008.

[65] Serdijn, W. A., "*A 16-bit 65-MS/s Pipeline ADC With 80-dBFS SNR Using Analog Auto-Calibration in SiGe SOI Complementary BiCMOS*", IEEE Transactions on Circuits and Systems I, Volume 57, page 2575 - 2575, 2010.

[66] Devarajan, S.; Singer, L.; Kelly, D.; Decker, S.; Kamath, A.; Wilkins, P., "*A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS Pipeline ADC*", IEEE Journal of Solid-State Circuits, Volume 44, page 3305 - 3313, 2009.

[67] Mulder, J.; Ward, C.M.; Chi-Hung Lin; Kruse, D., "*A 21-mW 8-b 125-MSample/s ADC in 0.09-mm2 0.13um CMOS"*, IEEE Journal of Solid-State Circuits, Volume 39, page 2116 - 2125, 2004.

[68] Ahmed, I.; Johns, D.A., "*A 50-MS/s(35mW) to 1-kS/s(15uW) Power Scaleable 10-bit Pipelined ADC Using Rapid Power-On Opamps and Minimal Bias Current Variation*", IEEE Journal of Solid-State Circuits, Volume 40, page 2446 - 2455, 2005.

[69] Mehr, I.; Singer, L., "*A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC*", IEEE Journal of Solid-State Circuits, Volume 35, page 318 - 325, 2000.

[70] Byung-Moo Min; Kim, P.; Bowman, F.W., III; Boisvert, D.M.; Aude, A.J., "*A 69-mW 10-bit 80-MSample/s Pipelined CMOS ADC*", IEEE Journal of Solid-State Circuits, Volume 38, page 2031 - 2039, 2003.

[71] Andersen, T.N.; Hernes, B.; Briskemyr, A.; Telsto, F.; Bjornsen, J.; Bonnerud, T.E.; Moldsvor, O., "*A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18um Digital CMOS*", IEEE Journal of Solid-State Circuits, Volume 40, page 1506 - 1513, 2005.

[72] El-Sankary, K.; Sawan, M., "*A Digital Blind Background Capacitor Mismatch Calibration Technique for Pipelined ADC*", IEEE Transactions on Circuits and Systems II, Volume 51, page 507 - 510, 2004.

[73] Chuang, S.-Y.; Sculley, T.L., "*A Digitally Self-Calibrating 14-bit 10-MHz CMOS Pipelined A/D Converter*", IEEE Journal of Solid-State Circuits, Volume 37, page 674 - 683, 2002.

[74] Ahmed, I.; Johns, D.A., "*A High Bandwidth Power Scalable Sub-Sampling 10-Bit Pipelined ADC With Embedded Sample and Hold*", IEEE Journal of Solid-State Circuits, Volume 43, page 1638 - 1647, 2008.

[75] Sasidhar, N.; Youn-Jae Kook; Takeuchi, S.; Hamashita, K.; Takasuka, K.; Hanumolu, P.K.; Un-Ku Moon, "*A Low Power Pipelined ADC Using Capacitor and Opamp Sharing Technique With a Scheme to Cancel the Effect of Signal Dependent Kickback*", IEEE Journal of Solid-State Circuits, Volume 44, page 2392 - 2401, 2009.

[76] Ming-Huang Liu; Kuo-Chan Huang; Wei-Yang Ou; Tsung-Yi Su; Shen-Iuan Liu, "*A Low Voltage-Power 13-Bit 16 MSPS CMOS Pipelined ADC*", IEEE Journal of Solid-State Circuits, Volume 39, page 834 - 836, 2004.

[77] Honda, K.; Furuta, M.; Kawahito, S., "*A Low-Power Low-Voltage 10-bit 100-MSample/s Pipeline A/D Converter Using Capacitance Coupling Techniques*", IEEE Journal of Solid-State Circuits, Volume 42, page 757 - 765, 2007.

[78] Jen-Lin Fan; Chung-Yi Wang; Jieh-Tsorng Wu, "*A Robust and Fast Digital Background Calibration Technique for Pipelined ADCs*", IEEE Transactions on Circuits and Systems I, Volume 54, page 1213 - 1223, 2007.

[79] Ahmed, I.; Johns, D.A., "*An 11-Bit 45 MS/s Pipelined ADC With Rapid Calibration of DAC Errors in a Multibit Pipeline Stage*", IEEE Journal of Solid-State Circuits, Volume 43, page 1626 - 1637, 2008.

[80] Adeniran, O. A.; Demosthenous, A., "*An Ultra-Energy-Efficient Wide-Bandwidth Video Pipeline ADC Using Optimized Architectural Partitioning*", IEEE Transactions on Circuits and Systems I, Volume 53, page 2485 - 2497, 2007.

[81] Taherzadeh-Sani, M.; Hamoui, A.A., "*Digital Background Calibration of Capacitor-Mismatch Errors in Pipelined ADCs*", IEEE Transactions on Circuits and Systems II, Volume 53, page 966 - 970, 2006.

[82] Arash Loloee, Alfio Zanchi, Huawen Jin, Shereef Shehata, Eduardo Bartolome, "*A 12b 80MSps Pipelined ADC Core with 190mW Consumption from 3V in 0.18μm Digital CMOS*", ESSCIRC 2002.

[83] Peter Bogner, Franz Kuttner, Claus Kropf, Thomas Hartig, Markus Burian, Hermann Eul, "*A 14b 100MS/s Digitally Self-Calibrated Pipelined ADC in 0.13μm CMOS*", ISSCC 2006.

[84] Masato Yoshioka, Masahiro Kudo, Toshihiko Mori, Sanroku Tsukamoto, "*A 0.8V 10b 8OMS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing*", ISSCC 2007.

[85] Seung-Chul Lee, Kwi-Dong Kim, Jong-Kee Kwon, Jongdae Kim , "*A 4.7mW 0.32mm^2 10b 30MS/s Pipelined ADC Without a Front-End S/H in 90nm CMOS*", ISSCC 2007.