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UNIVERSITY OF CALIFORNIA, SAN DIEGO

Surface preparation for ALD of High-k dielectrics on InGaAs

A dissertation submitted in partial satisfaction of the requirements for the degree Doctor of Philosophy

in Materials Science and Engineering by Wilhelm Melitz

Committee in charge:

Professor Andrew Kummel, Chair Professor Prab Bandaru, Co-Chair Professor Peter Asbeck Professor Yuan Taur Professor Charles Tu

2012

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Co-Chair

Chair

University of California, San Diego 2012

DEDICATION

To my grandfather, Merritt Mauzy, whose memory pushes me to excel.

EPIGRAPH

"If you thought that science was certain – well, that is just an error on your part."

-Richard P. Feynman

TABLE OF CONTENTS

SIGNATURE PAGE iii
DEDICATION iv
EPIGRAPHv
TABLE OF CONTENTS vi
LIST OF SYMBOLS AND ABBREVIATIONS ix
LIST OF FIGURES xiii
LIST OF TABLES xvi
ACKNOWLEDGEMENTS xvii
VITA, PUBLICATIONS AND FIELD OF STUDY xxi
ABSTRACT OF THE DISSERTATION xxvi
CHAPTER 1
1.1 Chamber 1
1.2 Scanning Tunneling Microscopy2
1.2 Scanning Tunneling Microscopy 2 1.3 Scanning Tunneling Spectroscopy 3
1.2 Scanning Tunneling Microscopy 2 1.3 Scanning Tunneling Spectroscopy 3 1.4 Kelvin Probe Force Microscopy 4
1.2 Scanning Tunneling Microscopy 2 1.3 Scanning Tunneling Spectroscopy 3 1.4 Kelvin Probe Force Microscopy 4 1.5 KPFM operational mode: FM and AM mode 7
1.2 Scanning Tunneling Microscopy 2 1.3 Scanning Tunneling Spectroscopy 3 1.4 Kelvin Probe Force Microscopy 4 1.5 KPFM operational mode: FM and AM mode 7 1.6 Acknowledgements 10
1.2 Scanning Tunneling Microscopy 2 1.3 Scanning Tunneling Spectroscopy 3 1.4 Kelvin Probe Force Microscopy 4 1.5 KPFM operational mode: FM and AM mode 7 1.6 Acknowledgements 10 1.7 References 18
1.2 Scanning Tunneling Microscopy 2 1.3 Scanning Tunneling Spectroscopy 3 1.4 Kelvin Probe Force Microscopy 4 1.5 KPFM operational mode: FM and AM mode 7 1.6 Acknowledgements 10 1.7 References 18 CHAPTER 2 19
1.2 Scanning Tunneling Microscopy 2 1.3 Scanning Tunneling Spectroscopy 3 1.4 Kelvin Probe Force Microscopy 4 1.5 KPFM operational mode: FM and AM mode 7 1.6 Acknowledgements 10 1.7 References 18 CHAPTER 2 19 STS and KPFM Investigation of Fermi energy level Pinning Mechanism on InAs and InGaAs Clean Surfaces

2.2 Introduction	19
2.3 Experimental Technique	21
2.4 Results	23
2.4.1 Scanning Tunneling Microscopy (STM)	23
2.4.2 Scanning Tunneling Spectroscopy (STS)	25
2.4.3. Kelvin Probe Force Microscopy (KPFM)	28
2.5 Discussion	30
2.6 Summary	34
2.7 Acknowledgements	35
2.8 References	42
CHAPTER 3 Atomic Imaging of ALD Oxide Nucleation with TMA on As-rich InGaAs vs Ga/In-rich InGaAs(001) 4×2	45 (001) 2×4
3.1 Abstract	45
3.2 Introduction	45
3.2 Introduction3.3 Experimental Technique	45 48
3.2 Introduction3.3 Experimental Technique3.4 Results and Discussion	45 48 50
 3.2 Introduction 3.3 Experimental Technique 3.4 Results and Discussion	45 48 50 GaAs(001)-
 3.2 Introduction 3.3 Experimental Technique 3.4 Results and Discussion. 3.4.1 STM of TMA on In/Ga-rich InGaAs(001)-(4×2) and As-rich InGa(2×4). 	45 48 50 GaAs(001)- 50
 3.2 Introduction 3.3 Experimental Technique 3.4 Results and Discussion. 3.4.1 STM of TMA on In/Ga-rich InGaAs(001)-(4×2) and As-rich InGaAs(001)-(4×2) and As-rich InGaAs(02×4). 3.4.2 STS of TMA on InGaAs(001) (4×2) vs (2×4). 	45 48 50 GaAs(001)- 50 55
 3.2 Introduction 3.3 Experimental Technique 3.4 Results and Discussion. 3.4.1 STM of TMA on In/Ga-rich InGaAs(001)-(4×2) and As-rich InG(2×4). 3.4.2 STS of TMA on InGaAs(001) (4×2) vs (2×4). 3.4.3. AES of initial passivation of InGaAs(001) (4×2) vs (2×4). 	45 48 50 GaAs(001)- 50 55 56
 3.2 Introduction 3.3 Experimental Technique 3.4 Results and Discussion. 3.4.1 STM of TMA on In/Ga-rich InGaAs(001)-(4×2) and As-rich InG (2×4). 3.4.2 STS of TMA on InGaAs(001) (4×2) vs (2×4). 3.4.3. AES of initial passivation of InGaAs(001) (4×2) vs (2×4). 3.5 Summary 	45 48 50 GaAs(001)- 50 55 56 59

CHAPTER 475 InGaAs and InP surface preparation for ALD by hydrogen cleaning and improvement with high temperature anneal
4.1 Abstract75
4.2 Introduction
4.3 Experimental Technique79
4.4 Results and Discussion
4.4.1 InGaAs(001)-(4×2)
4.4.2 InP
4.5 Summary
4.6 Acknowledgements
4.7 References
CHAPTER 5
5.1 Abstract 109
5.2 Introduction
5.3 Experimental Technique 110
5.4 Results and Discussion
5.5 Summary
5.6 Acknowledgements
5.7 References

LIST OF SYMBOLS AND ABBREVIATIONS

Al	Aluminum
Å	Angstrom
As	Arsenic
ALD	Atomic Layer Deposition
AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscopy
AM	Amplitude Modulation
V _{Applied}	Applied Voltage
Be	Beryllium
С	Carbon
С	Capacitance
С	Celsius
CMOS	Complementary Metal Oxide Semiconductor
СВ	Conduction Band
CBM	Conduction Band Minimum
Ec	Conduction Band Energy
CPD	Contact Potential Difference
I	Current
0	Degree
DOS	Density of States
D _{it}	Density of Interface Traps
EOT	Effective Oxide Thickness

e⁻	Electron
eV	Electron Volt
F _{ES}	Electrostatic Force
E	Energy
et al	Et Alia
Fig.	Figure
E _F	Fermi Energy
E _{fs}	Fermi Energy of Sample
E _{ft}	Fermi Energy of Tip
FM	Frequency Modulation
Ga	Gallium
HOPG	Highly ordered pyrolytic graphite
HT	High Temperature
Hz	Hertz
н	Hydrogen
Ei	Incident Beam Energy
In	Indium
InAs	Indium Arsenide
In _x Ga _{1-x} As	Indium Gallium Arsenide
LEED	Low Energy Electron Diffraction
LL	Load Lock
К	Kelvin
KPFM	Kelvin Probe Force Microscopy

MOSFET	Metal Oxide Field Effect Transistor
min	Minute
μA	Microampere
ML	Monolayer
MBE	Molecular beam epitaxy
nA	Nanoampere
nm	Nanometer
N	Nitrogen
0	Oxygen
Р	Phosphorus
RT	Room Temperature
Vs	Sample Bias Voltage
V _{DC}	Sample Bias DC component
V _{AC}	Sample Bias AC component
STM	Scanning Tunneling Microscopy
STS	Scanning Tunneling Spectroscopy
S	Second
Si	Silicon
SCL	Space-charge-layer
W	Tungsten
lt	Tunneling Current
ТМА	Trimethyl Aluminum
UHV	Ultra High Vacuum

V	Volt
VB	Valence Band
VBM	Valence Band Maximum
E _V	Valence Band Energy
V _{CPD}	Voltage applied to minimize CPD
E _{Vac}	Vacuum Level Energy
ϕ_{sample}	Work function of sample
<i>Ф</i> tip	Work function of tip
XPS	X-ray Photoelectron Spectroscopy
Zn	Zinc

LIST OF FIGURES

Figure 1.1: Diagram of ultra high-vacuum (UHV) system chamber
Figure 1.2: Schematic diagram of basic STM circuit
Figure 1.3: Band diagram of tunneling mechanism occurring in STM 13
Figure 1.4: Schematic diagram of a basic STS circuit
Figure 1.5: Electronic energy levels of the sample and AFM tip 15
Figure 1.6: A typical inter-atomic force vs. distance curve
Figure 2.1: High resolution filled state STM of InAs(001)-(4×2) and ball-
stick diagram of surface reconstruction
Figure 2.2: STM of typical InGaAs(001)-(4×2) surface
Figure 2.3: High resolution filled state STM of InAs(110) surface and ball
and stick diagram of surface
Figure 2.4: Normalized STS spectra of InAs(001)-(4×2), cleaved
InAs(110) and InGaAs(001)-(4×2)
Figure 2.5: KPFM measured work functions from AM mode
measurement along with bulk bandgaps
Figure 2.6: Band diagram comparing STS and KPFM41
Figure 3.1: Filled state STM images for decapped, cleaned and TMA
dosed InGaAs 4×2 62
Figure 3.2: High resolution filled state STM images for TMA dosed
InGaAs 4×263
Figure 3.3: Filled state STM images for decapped, cleaned and TMA
dosed InGaAs 2×464

Figure 3.4: Ball-and-stick diagram for TMA on InGaAs 4×2 and 2×465
Figure 3.5: STS spectra for the TMA dosing on InGaAs 4×2 and 2×4 at
various temperatures
Figure 3.6: AES spectra for TMA and O2 on InGaAs 4×2
Figure 3.7: AES spectra for TMA and O2 on InGaAs 2×4
Figure 4.1: Filled state STM image of decapped surface, air exposed, 30
minutes dose of hydrogen at 380°C, and anneal to 460-480°C 94
Figure 4.2: Large STM image of decapped surface, air exposed and 30
minutes dose of hydrogen at 380°C, and anneal to 460-480°C 95
Figure 4.3: Processing matrix for hydrogen cleaning of InGaAs
Figure 4.4: STM images of surface after TMA dose at room temperature
and annealed to 250°C
Figure 4.5: STM image of InGaAs dose with atomic H for 30 minutes at -
40 °C directly after exposure to air for 30 minutes
Figure 4.6: Normalized STS spectra of decapped InGaAs(001)-(4×2),
hydrogen cleaned and TMA dosed surfaces
Figure 4.7: STM image of InP after 10 minutes dose of atomic H at 380
°C, and after 10 minutes dose of atomic H at 380 °C plus a high
temperature anneal to 470°C
Figure 4.8: STM image of InP 10 minutes dose of atomic H at 440 °C,
and 5 minute dose of atomic H at 460-480 °C

Figure 4.9: STM images of InP surface cleaned with atomic H for 5
minutes at 460-480 °C after TMA dosing at room temperature and
annealing to 250 °C 103
Figure 5.1 Topology and CPD of UHV cleaved InAs(110)
Figure 5.2 Cross-sectional view of MOSCAP gate stack. Top down view
of a single sample die. Schematic of the sample holder and
external contacts. Topology image of UHV cleaved GaAs
MOSCAP corresponding to the 0 V gate bias CPD image
Figure 5.3 n ⁺⁺ GaAs/GGO/ <i>n</i> -type GaAs MOSCAP at -1, 0, and +1V
external gate bias120

LIST OF TABLES

Table	1.1: Typical spatial and energy resolution of FM and AM mode	
	KPFM	.17
Table	3.1: AES atomic ratios for InGaAs(001)-(4×2) surface and dosed	
	surfaces	.67
Table	3.2: AES atomic ratios for InGaAs(001)-(2×4) surface and dosed	
	surfaces	.68
Table	4.1: Comparison of temperature and time of hydrogen dose of the	
	densities of etch pits, incomplete terraces, and percent of the	
	surface covered with etch either pits or incomplete terraces	.96

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xvii

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xviii

W. Melitz, J. Shen, A.C. Kummel, and S. Lee, "Kelvin probe force microscopy and its application". *Surface Science Reports* **66**, 1-27 (2011).

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W. Melitz, J. Shen, S. Lee, J.S. Lee and A.C. Kummel, "STS and KPFM Investigation of Fermi energy level Pinning Mechanism on InAs and InGaAs Clean Surfaces". *Journal of Applied Physics* **108**, 023711 (2010).

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xix

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PUBLICATIONS

- W. Melitz, T. Kent, R. Droopad, M. Holland, I. Thayne, and A.C. Kummel, "Atomic Imaging of ALD Oxide Nucleation with TMA on As-rich InGaAs(001) 2×4 vs Ga/In-rich InGaAs(001) 4×2" Submitted to *Journal of Chemical Physics* (2012).
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FIELD OF STUDY

Major Field: Physical Chemistry

Studies in Surface Science Professor Andrew C. Kummel

ABSTRACT OF THE DISSERTATION

Surface preparation for ALD of High-k dielectrics on InGaAs

by Wilhelm Melitz

Doctor of Philosophy in Materials Science and Engineering University of California, San Diego, 2012 Professor Andrew Kummel, Chair Professor Prab Bandaru, Co-Chair

The key for a successful gate-first process is when subsequent processing steps cannot degrade the semiconductor, the dielectric, or the oxide-semiconductor interfaces. For silicon, the only commercial ALD high-k fabrication process, which avoids processing induced damage, is a replacement gate process (a type of gate-last process). While preparing silicon for gate-last processing is straightforward, the key to a gate-last process for III-V semiconductors is the order and cleanliness of the III-V channel prior to dielectric deposition. Aggressive oxide thickness reduction (equivalent oxide thickness, or EOT, scaling) is needed to fabricate small gate length devices with small subthreshold swings. Furthermore, aggressive EOT scaling requires a very high uniform ALD nucleation density, with no pinholes due to surface contaminants.

The key barrier to solving a very practical problem is a surface chemistry challenge: develop a chemical process which removes nearly all air induced defects and contaminants and leaves the III-V surface flat and electrically active

xxvi

for high nucleation density ALD gate oxide deposition, which unpins the Fermi level.

The following study uses scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) to observe the removal of the oxide layer and restoration of the clean InGaAs surface reconstruction with atomic hydrogen cleaning, allowing for a gate-last or replacement-gate process. Along with surface cleaning STM and STS was used to characterize the initial passivation of InGaAs surfaces via ALD of trimethyl aluminum (TMA). The substrate temperature and initial surface reconstruction was critical to forming an unpinned passivation layer with a high nucleation density.

A method was developed to use Kelvin probe force microscopy (KPFM) as a tool for insightful feedback on the electrostatics of scaled MOSFET devices. KPFM is a unique technique for providing two-dimensional potential profiles inside a working device. A procedure is described to obtain high-resolution KPFM results on ultra-high vacuum (UHV) cleaved III-V MOSCAPs.

Chapter 1

Experimental Setup

1.1 Chamber

The majority of the dissertation was performed in an ultra high vacuum (UHV) chamber. An Omicron dual chamber system with a preparation and an analysis chamber is used. A schematic of the full chamber can be seen in Figure 1.1. The preparation chamber has an Oxford Research TC-50 thermal gas cracker, a Omicron x-ray photoelectron spectroscopy system, an auger electron spectroscopy single pass system, a tungsten filament for tip cracking, and a Stanford Research mass spectrometer. Sample decapping, hydrogen cleaning and sample annealing is performed in the preparation chamber. The base pressure of the preparation chamber is held below 1x10⁻¹⁰ Torr. The analysis chamber is equipped with an Omicron VT-STM/AFM microscope. Scanning tunneling microscopy (STM) and spectroscopy (STS) is performed in the analysis chamber, along with Kelvin probe force microscopy (KPFM). The base pressure of the analysis chamber is below 2x10⁻¹¹ Torr.

The chamber also contains a load lock (LL) system, used to transfer samples in and out of the preparation chamber. This LL system has been modified to contain sample heating and dosing of trimethyl aluminum (TMA), to replicate atomic layer deposition (ALD). The LL is baked before dosing to achieve a base pressure below 2x10⁻⁷ Torr. Strem Chemicals Inc, 98% TMA is used in dosing. A dose volume is filled with the vapor pressure of TMA, and then exposed to the LL, representing a pulse of TMA vapor.

1.2 Scanning Tunneling Microscopy

The predominant technique used for this dissertation is scanning tunneling microscopy (STM) [1], a diagram of STM can be seen in Figure 1.2. In STM, a metallic tip, usually tungsten, is positioned extremely close to the surface of the sample (~1nm). Next, a bias is applied to the tip relative to the sample. Electron quantum mechanic tunneling occurs between the tip and the sample surface. The tunneling current is proportional to the distance between the tip and the sample:

$$I \propto e^{-kz}$$
, (1.2.1)

where z is the distance between the tip and the sample and k is the coefficient describing the decay of the wave inside the vacuum barrier.

For STM imaging the tip is scanned over the surface, simultaneously monitoring the tunneling current. In constant current mode, the tip height is adjusted to maintain a constant tunneling current, the height is recorded to comprise a surface image, providing an extremely high resolution surface mapping. The resulting image is a convolution of the electrical properties of the surface, dependent on the density of states, and the surface structure. The electrical properties of the surface are also highly dependent on the bias applied to the tip relative to the sample. By adjusting the voltage the sample surface can be probed for different energies. Figure 1.3 illustrates the band alignment for two different scanning modes, filled and empty state imaging. A positive tip voltage, or a negative sample bias, is applied for filled state imaging, pushing the Fermi level of the tip below the valance band energy of the semiconductor surface and causing electrons from the sample surface to tunnel in to the tip (Figure 1.3a). A negative tip voltage, or a positive sample bias, is applied for empty state imaging, moving the Fermi level of the tip above the conduction band energy, causes electrons to tunnel from the tip to the surface (Figure 1.3b). The dependence of the tunneling on the sample bias can be further exploited to characterize the surface density of states (DOS) in scanning tunneling spectroscopy (STS).

1.3 Scanning Tunneling Spectroscopy

In STS using the STM, instead of scanning, by fixing the position of the tip on the surface and sweeping the bias, the local DOS can be extracted. A schematic of the system for STS can be seen in Figure 1.4. The sample bias (V_{DC}) is swept to measure I/V. A small AC signal is applied on top of the DC component for the lock-in to extract the dI/dV. STS measures the dynamic tunneling conductance which is proportional to the surface DOS [1; 2],

$$(dI/dV)/(I/V) \propto DOS_{sample}(E_F - eV)$$
(1.1.2)

The spectra can be used to determine the position of the surface Fermi level relative to the conduction band (CB) and valance band (VB). The Fermi level is defined as the zero sample bias. By taking spectra for both n- and p-type samples, the surface Fermi level can be determined to be pinned or unpinned. For an unpinned surface interface, the Fermi level position for n-type will be close to or in the CB, while the p-type would be near or in the VB. If the surface Fermi level is pinned, the measured Fermi level position will be located approximately in the same position for both n- and p-type samples. More descriptions detailed on STS can be found in the literature [1; 3-7].

1.4 Kelvin Probe Force Microscopy

The Kelvin probe force microscopy (KPFM) measures contact potential difference (CPD) between a conducting atomic force microscopy (AFM) tip and a sample. The CPD (V_{CPD}) between the tip and sample is defined as:

$$V_{CPD} = \frac{\phi_{tip} - \phi_{sample}}{-e}, \qquad (1.4.1)$$

where ϕ_{sample} and ϕ_{tip} are the work functions of the sample and tip, and *e* is the electronic charge. When an AFM tip is brought close to the sample surface, an electrical force is generated between the tip and sample surface, due to the differences in their Fermi energy levels. Figure 1.5 shows the energy level diagram of the tip and sample surface when ϕ_{sample} and ϕ_{tip} are different. Figure 1.5a depicts the energy levels of the tip and sample surface when separated by a distance *d* and not electrically connected (note, the vacuum levels are aligned but Fermi energy levels are different). Equilibrium requires Fermi levels line-up at steady state, if the tip and sample surface are close enough for electron tunneling. Upon electrical contact, the Fermi levels will align through electron current flow, and the system will reach an equilibrium state, Figure 1.5b. The tip and sample surface will be charged, and an apparent V_{CPD} will form (note, the Fermi energy levels are aligned but vacuum energy levels are

no longer the same, and a V_{CPD} between the tip and sample has formed). An electrical force acts on the contact area, due to the V_{CPD} . As shown in Figure 1.5c, this force can be nullified. If an applied external bias (V_{DC}) has the same magnitude as the V_{CPD} with the opposite bias, the applied voltage eliminates the surface charge in the contact area. The amount of applied external bias (V_{DC}) that nullifies the electrical force due to the V_{CPD} is equal to the work function difference between the tip and sample. The work function of the sample can be calculated when the tip work function is known.

By applying an AC voltage (V_{AC}) plus a DC voltage (V_{DC}) to the AFM tip, KPFM measures the work function of a sample. V_{AC} generates oscillating electrical forces between the AFM tip and sample surface, and V_{DC} nullifies the oscillating electrical forces that originated from CPD between tip and sample surface. The electrostatic force (F_{es}) between the AFM tip and sample is given by:

$$F_{es}(z) = -\frac{1}{2}\Delta V^2 \frac{dC(z)}{dz},$$
(1.4.2)

where *z* is the direction normal to the sample surface, ΔV is the potential difference between V_{CPD} and the voltage applied to the AFM tip, and dC/dz is the gradient of the capacitance between tip and sample surface. When $V_{AC}\sin(\omega t) + V_{DC}$ is applied to the AFM tip, the voltage difference ΔV will be:

$$\Delta V = V_{tip} \pm V_{CPD} = (V_{DC} \pm V_{CPD}) + V_{AC} \sin(\omega t)$$
(1.4.3)

Note that the \pm sign depends whether the bias (V_{DC}) is applied to the sample (+) or the tip (-) [8]. Substituting Eq. 1.4.3 in Eq. 1.4.2 gives the expression of the electrostatic force applied to the AFM tip:

$$F_{es}(z,t) = -\frac{1}{2} \frac{\partial C(z)}{\partial z} \left[\left(V_{DC} \pm V_{CPD} \right) + V_{AC} \sin(\omega t) \right]^2$$
(1.4.4)

This equation can be divided into three parts:

$$F_{DC} = -\frac{\partial C(z)}{\partial z} \left[\frac{1}{2} \left(V_{DC} \pm V_{CPD} \right)^2 \right]$$
(1.4.5)

$$F_{\omega} = -\frac{\partial C(z)}{\partial z} \left(V_{DC} \pm V_{CPD} \right) V_{AC} \sin(\omega t)$$
(1.4.6)

$$F_{2\omega} = \frac{\partial C(z)}{\partial z} \frac{1}{4} V_{AC}^2 \left[\cos(2\omega t) - 1 \right]$$
(1.4.7)

 F_{DC} (Eq. 1.4.5) results in a static deflection of the AFM tip. F_{ω} , with frequency ω , (Eq. 1.4.6) is used to measure the V_{CPD} . $F_{2\omega}$ can be used for capacitance microscopy [9]. When electrostatic forces are applied to the tip by V_{AC} with V_{DC} , additional oscillating components (due to the electrical force) will be superimposed to the mechanical oscillation of AFM tip. A lock-in amplifier is employed to measure the V_{CPD} , to extract the electrical force component with frequency ω (F_{ω}), a function of V_{CPD} and V_{AC} . The output signal of the lock-in amplifier is directly proportional to the difference between V_{CPD} and V_{DC} . The V_{CPD} value can be measured by applying V_{DC} to the AFM tip, such that the output signal of the lock-in amplifier is nullified, and F_{ω} equals zero. Subsequently, the value of V_{DC} is acquired for each point on the sample surface, composing a map of the work function or surface potential of the whole sample surface area.

Eq. 1.4.4 is derived from the capacitive energy between two parallel metal plates, and the equation is valid for CPD measurements on metallic surface. The space-charge-layer (SCL) on the surface of a semiconductor is well known, and the effect of the SCL has to be considered when measuring CPD on a semiconductor surface. Hudlet *et al.* analyzed the electrostatic force in metallic AFM tip/metallic surfaces and metallic AFM tip/semiconductor surfaces [10]. In the case of a semiconductor surface, F_{ω} is derived as:

$$F_{\omega} = -\frac{Q_s}{\varepsilon_0} \frac{C_I C_D}{C_I + C_D} V_{AC} \sin(\omega t) , \qquad (1.4.8)$$

where Q_s is total charge near the semiconductor surface due to the surface potential of the semiconductor, ε_0 is the dielectric constant, C_l is the capacitance associated with V_{AC} and the air gap between tip and sample, and C_D is the capacitance associated with V_{AC} and SCL in the semiconductor. For a semiconductor surface, the measured CPD is related to the surface potential, which differs from the work function of semiconductor materials, due to the SCL near the semiconductor surface.

1.5 KPFM operational mode: FM and AM mode

As previously described, AFM can detect atomic forces by AM or FM mode. The electrostatic force F_{ω} can also be detected either by AM or FM mode in KPFM. The AM mode KPFM measures F_{ω} directly from the amplitude of the cantilever oscillation at ω induced by V_{CPD} and V_{AC} . V_{DC} is applied to the AFM tip to null the measured amplitude, thereby measuring V_{CPD} . In FM mode KPFM, F_{ω}

is detected by the frequency shift at ω . V_{DC} is applied to the AFM tip to nullify the frequency shift, thereby measuring V_{CPD} .

KPFM extracts the topography concurrently with V_{CPD} , using an AFM tip. A method to separate the topographical signal from the V_{CPD} measurement is required. In the KPFM experimental setup, the V_{AC} is usually modulated at a frequency higher than the bandwidth of the topography feedback system to prevent cross-talk between topography and CPD measurement. In AM mode KPFM, topography is measured by the oscillation at the first resonance frequency of the AFM tip, and V_{CPD} is measured by the amplitude of the oscillation at the second resonance frequency of the AFM tip. A mechanically vibrated cantilever generally has several resonance peaks in the oscillation amplitude-frequency spectrum. The second resonance peak normally has a broader peak than the first resonance frequency peak. The amplitude of the second resonance peak is usually less than one-third of the first resonance frequency peak, and the frequency of the second resonance peak is typically 6 times the first resonance frequency [11]. V_{AC} is tuned to the second resonance frequency to excite the AFM tip by electrical force, while the first resonance frequency is assigned for the tip height control. Using these techniques, the topography and the V_{CPD} signal can be separated. Conversely, in FM mode KPFM, the AFM tip is mechanically excited at the first resonance frequency. V_{AC} induces a modulation of the electrostatic force, which is detected by the superimposed oscillation at the frequency variation of the mechanical oscillation of the AFM tip, leading to the separation of topography and V_{CPD} signal.
The spatial resolution of measuring V_{CPD} in FM mode KPFM is higher than in AM mode KPFM. Similar to the AM and FM mode AFM, the AM mode KPFM directly detects the electrostatic force by the oscillation of the cantilever. The FM mode KPFM detects the electrostatic force gradient by the frequency shift of the cantilever oscillation, which contributes to greater spatial resolution [11; 12]. However, the detection range of the force gradient is shorter than the force itself, explained by the inter-atomic force-distance curve.

Figure 1.6 shows the typical force-distance curve. In the attractive force regime, the force gradient (the derivative of the force-distance curve) becomes larger when the inter-atomic distance is small. As the inter-atomic distance increases, the force gradient becomes insignificant. Therefore, the detection of force gradient takes place mainly at the end of the AFM tip. Consequently, the detection of electrostatic force is considered long-range detection, whereas the detection of electrostatic force gradient is short-range detection. The electrostatic interaction takes place mainly between the tip apex and sample surface in the FM mode KPFM. The spatial resolution is approximately equal to the dimension of the tip apex in the FM mode KPFM. However, the electrostatic interaction from the sample includes both the tip and the cantilever in AM mode KPFM due to the long-range detection scheme. As a result, the spatial resolution of AM mode KPFM is reduced by an averaging effect between the tip and cantilever.

The energy resolution of measurements of V_{CPD} in AM mode KPFM is higher than in FM mode KPFM. AM mode KPFM measures the V_{CPD} from the resonance peak of the oscillating cantilever, greatly enhancing the signal-tonoise ratio [11; 13]. Conversely, FM mode KPFM detects the V_{CPD} through an FM demodulator [11], and additional noise is generated when the signal passes through the FM demodulator. Consequently, the energy resolution of AM mode KPFM is superior to FM mode KPFM, due to the high signal-to-noise ratio. The typical spatial and energy resolutions of V_{CPD} measurement by FM and AM mode KPFM are listed in Table 1.1.

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Figure 1.1: Diagram of ultra high-vacuum (UHV) system chamber. The scanning probe microscopy (SPM) chamber has a base pressure of $2x10^{-11}$ Torr. The SPM chamber contains an Omicron STM/AFM VT capable of performing STM, STS, atomic force microscopy (AFM), Kelvin probe force microscopy (KPFM). The preparation chamber has a base pressure of $1x10^{-10}$ Torr, and contains the atomic H cracker. The preparation chamber also contains a dual anode x-ray photoelectron source and analyzer, mass spectrometer, tip cracker, and auger electron spectroscopy (AES). The load lock is pumped by a turbomolecular pump to achieve a base pressure of 1×10^{-7} Torr. The turbomolecular pump is also used to remove any residual water in the load lock that might react with the TMA.



Figure 1.2: Schematic diagram of basic STM circuit.



Figure 1.3: Band diagram of illustrating tunneling mechanism occurring in STM, (a) Filled state imaging mode, (b) empty state imaging mode.



Figure 1.4: Schematic diagram of a basic STS circuit.



Figure 1.5. Electronic energy levels of the sample and AFM tip for three cases: (a) tip and sample are separated by distance *d* with no electrical contact, (b) tip and sample are in electrical contact, and (c) external bias (V_{dc}) is applied between tip and sample to nullify the CPD and, therefore, the tip-sample electrical force. E_{vac} is the vacuum energy level. E_{fs} and E_{ft} are Fermi energy levels of the sample and tip, respectively.



Figure 1.6. A typical inter-atomic force vs. distance curve. The force gradient (derivative of curve) is limited to the short-range tip-sample distances, while the force is long-ranged compared to the force gradient.

KPFM Mode	Spatial Resolution	Energy Resolution
FM	Possibly sub-nanometer resolution depending on tip apex	10 ~ 20 meV
AM	25 nm	5 meV

Table 1.1 Typical spatial and energy resolution of FM and AM mode KPFM.

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Chapter 2

STS and KPFM Investigation of Fermi energy level Pinning Mechanism on InAs and InGaAs Clean Surfaces

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2.1 Abstract

A comparison is made between the electronic structures determined in ultra high vacuum of three surfaces using scanning tunneling spectroscopy (STS) and Kelvin probe force microscopy (KPFM). STS and KPFM illustrates Fermi level pinning of clean InAs(001)-(4×2) and InGaAs(001)-(4×2) surfaces and near flat band conditions for InAs(110) cleaved surfaces. However, for InAs(001)-(4×2) and InGaAs(001)-(4×2) and InGaAs(001)-(4×2), STS and KPFM data show very different positions for the surface Fermi level on identical samples; it is hypothesized that the difference is due to the Fermi level measured by KPFM being shifted by a static charge dipole to which STS is much less sensitive.

2.2 Introduction

InAs and InGaAs have shown great promise as channel materials for metal oxide semiconductor field effect transistors (MOSFETs) because of extremely high electron mobility[1]. One limiting factor for the development of III-

19

V MOSFETs is the oxide/semiconductor interface quality. For growth of MOSFET gate oxides, atomic layer deposition (ALD) is employed to deposit gate oxides on the semiconductor by exposure to metal organic and oxidant gases. The goal of ALD is for the oxidants to selectively oxidize the metal precursor chemisorbates without oxidizing the substrate. A reconstruction of InAs(001) or InGaAs(001) with low reactivity to oxidants, such as the In-rich (4×2) surface reconstruction[2-4] is desirable to minimize substrate oxidation that can introduce surface states and degrade device performance.

Ultrahigh vacuum (UHV)-cleaved InAs(110) surfaces only contain In-As bonds with a similar structure to the cleaved GaAs surface[5]. For InAs(110), an idealized model of the surface has the surface atoms buckling into geometries which are relaxed with the particular dangling bonds on each type of atom: the As atoms have a sp^3 hybridized bonding geometry with a completely filled dangling bond while the In atoms have sp^2 hybridized bonding geometry with a completely filled completely empty dangling bond. The InAs(110) surface being unpinned is consistent with having completely filled and empty dangling bonds in a relaxed geometrical structure with low defect density and no partially filled dangling bonds. The InGaAs(110) surface is not studied here because InGaAs thin films are grown on other compound semiconductor wafers making it more challenging to perform cross-sectional studies.

The surface structure of InAs(001)-(4×2) has been studied using scanning tunneling microscopy (STM)[3; 6-8], reflection high-energy electron diffraction (RHEED)[7] and density functional theory (DFT)[3; 6; 9]. The InAs(001)-(4×2)

20

surface contains dicoordinated In row atoms and pairs of In homodimers in the trough. The tricoordinated In and As atoms normally have completely filled or empty dangling bonds. The homodimers or row dicoordinated In atoms on the InAs(001)-(4×2) surface could generate surface states, causing surface pinning. The InAs(001)-(4×2) surface shows electron accumulation and a surface dipole, caused by surface states. The InGaAs(001)-(4×2) surface structure is analogous to InAs(001)-(4×2), with some In atoms replaced with Ga atoms. The InGaAs(001)-(4×2) surface structure has also been studied with STM[4; 10], RHEED[10], and DFT[4; 11; 12]

A combination of Kelvin probe force microscopy (KPFM)[13; 14] and scanning tunneling spectroscopy (STS)[15-19] is used here to illustrate the pinning of clean InAs(001)-(4×2) and InGaAs(001)-(4×2) surfaces and unpinning of InAs(110) cleaved surfaces. In a comparison of STS and KPFM data, both show that the Fermi level of InAs(110) is unpinned. However, for InAs(001)-(4×2) and InGaAs(001)-(4×2), STS and KPFM show very different positions for the Fermi level on identical samples, which is hypothesized to occur because the Fermi level is shifted by a static surface charge dipole to which KPFM is sensitive, but STS is not.

2.3 Experimental technique

The InAs samples are commercially available InAs wafers (Wafer Tech) with a 200 nm thick InAs surface layer grown by molecular beam expitaxy (MBE). The *n*-type and *p*-type InAs substrates have 2 ×10¹⁸ cm⁻³ doping with S and Zn

dopants. The *n*-type and *p*-type MBE-grown InAs layers have 2×10^{18} cm⁻³ doping with Si and Be dopants. The InGaAs samples consist of commercially available InP wafers with a 0.2µm thick In_{0.53}Ga_{0.47}As surface layer grown by MBE. The InP substrate dopings for both *n*-type and *p*-type InAs are 2×10^{18} cm⁻³ with Si and Zn dopants. The MBE-grown InGaAs layers are doped *n*-type and *p*-type 2×10^{18} cm⁻³ with Si and Be dopants.

Following MBE growth, all samples are capped with a 50nm As₂ layer and shipped/stored under vacuum before loading into the UHV chamber. Sample preparation is performed in a preparation chamber with a base pressure of mid 10^{-10} Torr. The samples are first degassed at 150 °C followed by a two hour As₂ layer decapping at ~330 °C. After decapping, the samples are annealed at 450-470 °C to form the InAs(001)-(4×2) or InGaAs(001)-(4×2) surface reconstruction. For InAs(110), samples are degassed at 150 °C for several hours before cleaving in UHV.

An Omicron VT-AFM/STM analysis chamber, with a base pressure in the low 10⁻¹¹ Torr, is used for STM/STS and KPFM. An etched W wire is cracked in UHV and employed for STM/STS. STS can be performed with constant tipsample distance or with variable tip distance [18-22]. Variable tip STS is employed with Z variation of 0.1-0.3nm/V and tip sample distances of 0.2-0.5nm. KPFM was performed with commercial Pt coated silicon cantilevers from Asylum Research. Frequency modulation (FM)[23] and amplitude modulation (AM)[24] KPFM are performed with cantilevers with resonant frequencies of approximately 270kHz and 70kHz, respectively. KPFM measures the contact potential difference (CPD) between the sample and tip. The CPD is defined as

$$CPD = \varphi_{tip} - \varphi_{sample}, \qquad (2.3.1)$$

where φ_{iip} is the work function of the metallic tip, and φ_{sample} is the work function of the sample surface. The work function of Pt-coated tips is first calibrated with highly ordered pyrolytic graphite (HOPG) (φ_{HOPG} = 4.6 ± 0.1eV)[25] to convert the measured CPD to the absolute surface work function. The absolution surface work function of the sample can be calculated as follows

$$\varphi_{\text{sample}} = 4.6 \text{eV} + CPD_{\text{HOPG}} - CPD_{\text{sample}} . \qquad (2.3.2)$$

To determine an absolute work function with a scanning KPFM, a scan over a large area is taken, and the mean of the distribution of CPD at each point is employed as the sample CPD. A Pt coated silicon cantilever is used at a frequency set point of -50Hz relative to the resonant frequency of the cantilever, corresponding to a typical tip sample separation of approximately 3 nm. A scan of larger then 100x100nm is performed on both the sample and HOPG to determine CPD_{sample} and CPD_{HOPG}.

2.4 Results

2.4.1 Scanning Tunneling Microscopy (STM)

Figure 2.1 shows a high resolution STM image of an InAs(001)-(4×2) surface, with a unit cell indicated by the green rectangle. The STM image contains a row and trough structure consistent with the β 3'(4×2)[6] reconstruction

containing two row dicoordinated In atoms (arrow 1), four row tricoordinated edge As atoms (arrow 2) and two tricoordinated In homodimers located in the trough (arrows 3 and 4). In contrast to the InAs(110) surface, the InAs(001)-(4×2) surface reconstruction may have several potential defect sites including partially filled dangling bonds which introduce defects that can cause Fermi energy level pinning[26].

The InGaAs(001)-(4×2) surface structure is similar to InAs(001)-(4×2) with more surface defects. The structure is identical with some of the surface In atoms replaced with Ga atoms. Figure 2.2a shows a typical InGaAs(001)-(4×2) surface. Figure 2.2b illustrates a typical InAs(001)-(4×2) surface with the same length scale. Four kinds of defects are typically observed on InGaAs(001)-(4×2). The first is dark cuts in the rows (inset of Figure 2.2a). The second is bright dots above the trough or the row (inset of Figure 2.2b). The third is dark rows perpendicular to the In rows, (the rectangle in Figure 2.2a). The fourth is bright rows parallel to the In rows (the oval in Figure 2.2b). Figure 2.2 shows InGaAs(001)-(4×2) consistently has more defects than InAs(001)-(4×2)[12].

High resolution STM of a cleaved InAs(110) surface is shown in Figure 2.3. The periodic structure matches the bulk lattice spacing of 0.6nm × 0.4nm[5; 27]. The InAs(110) cross-sectional surface only contains heterogeneous In-As bonds and is atomically flat with few defects which would contribute defect states[5]. The As atoms are oriented in a sp^3 hybridized bonding configuration with a filled dangling bond in a simplified model. The In atoms are oriented in a sp^2 hybridized bonding configuration with an empty

dangling bond in a simplified model. Only the As atoms appear in the high resolution filled state STM because the surface As atoms have filled dangling bonds while surface In atoms have empty dangling bonds. The structure of InAs(110) is analogous to that of the GaAs(110)[20; 28].

2.4.2 Scanning Tunneling Spectroscopy (STS)

STS spectra were collected for both *n*-type and *p*-type $InAs(001)-(4\times 2)$. With no tip induced band bending, zero sample bias corresponds approximately to the location of the surface Fermi level relative to the conduction band minimum (CBM) and the valence band maximum (VBM)[20; 29]. As shown in Figure 2.4a, both *n*-type and *p*-type InAs(001)-(4×2) have zero sample bias near the CBM, consistent with the surface Fermi level being pinned *n*-type. For an unpinned surface, the Fermi level position, at zero bias, for *n*-type and *p*-type should have a shift relative to the VBM and CBM. Furthermore, the surface Fermi level for InAs(001)-(4×2) is known to be pinned at the CBM from ultraviolet photoelectron spectroscopy (UPS) and high resolution electron energy loss spectroscopy (HREELS) [30; 31] experiments. The STS for InAs(001)-(4×2) shows a band gap of 0.3eV, close to the expected band gap of 0.35eV and consistent with minimal tip induced band bending. If the surface Fermi level is pinned, the amount of tip induced band bending will be minimal, because surface states can be filled or empty to account for the work function difference between the W tip and the InAs(001)-(4×2) surface[32; 33].

The InAs(110) surface contains only filled or empty dangling bonds on tricoordinated atoms in relaxed geometries which should be electrically passive[26]. Therefore, the surface is expected to be unpinned. The STS (Figure 2.4b) image of InAs(110) in cross-section shows the Fermi level for ntype InAs(110) near the CBM and the Fermi level for p-type InAs(110) close to the VBM. The shift between *n*-type and *p*-type is about 0.2eV, consistent with an unpinned InAs surface. The STS for InAs(110) shows a band gap of around 0.2eV, however, the band gap of InAs is 0.35eV. The decrease in band gap is caused by the variable z spectroscopy used for the STS. When doing variable z, enhancement of the signal can occur on unpinned surfaces for low sample biases causing a smearing effect on the valence band (VB) and conduction band (CB)[20]. Tip-induced band bending should be minimal for InAs(110) because of the high doping level and the small band gap of the InAs sample. The high doping will reduce the space charge region formed by the contact potential difference of the W tip and the semiconductor. The small band gap will also provide a large density of states that will respond to the potential difference again reducing the amount of tip-induced band bending[32-34].

STS on InGaAs(001)-(4×2) has an advantage over STS on InAs(001)-(4x2), because the band gap of InGaAs is 0.74eV (compared to InAs of 0.35eV), which produces more consistent spectra. InGaAs(001)-(4×2) is expected to have similar electronic properties to InAs(001)-(4×2) because the surface reconstructions are effectively the same except the group III atoms on InGaAs(001)-(4x2) surfaces are a weighted random mixture of In and Ga atoms.

However, in Figure 2.4c, the Fermi level (zero bias position) as determined by STS is located near the VBM or midgap for both *n*-type and *p*-type, consistent with $InGaAs(001)-(4\times 2)$ being pinned p-type or midgap. Note that the position of the zero bias relative to the VBM for both InGaAs(001)-(4×2) and InAs(001)-(4×2) is approximately the same, 0.3eV above the VBM. The valence band offset for InGaAs and InAs of ~0.1eV[35] which positions the Fermi level measure with STS for both InGaAs(001)-(4×2) and InAs(001)-(4×2) at the same position within 0.1eV. The STS indicates the surface Fermi level positions of InGaAs and InAs (4×2) surfaces are roughly at the same energy relative to the VB. A wide range of positions for the surface Fermi level of InGaAs(001) have been reported. As explained below, UPS measurements of the Fermi level position should be consistent with STS measurements of the Fermi level position. To our knowledge, no UPS results on decapped MBE grown InGaAs/InP have been published. UPS results on metal-organic vapor phase epitaxy (MOVPE) InGaAs/InP show the surface Fermi level ~0.4eV above the VBM[36]. Photoluminescence spectroscopy (PL) and Metal Insulator Semiconductor (MIS) structures on InGaAs indicated the position of the surface Fermi level is ~0.5 eV However, these studies did not document the above the VBM[37; 38]. reconstruction or the UHV cleaning method so the difference in Fermi level position between the previous studies and the present one may be due to differences in the reconstruction or UHV preparation.

2.4.3 Kelvin Probe Force Microscopy (KPFM)

The KPFM results for both the $InAs(001)-(4\times2)$ and the InAs(110) surfaces are shown in Figure 2.5. The KPFM data is consistent with the STS results showing the $InAs(001)-(4\times2)$ surface reconstruction is pinned and the InAs(110)surface is unpinned. KPFM shows the pinned surface $InAs(001)-(4\times2)$ work function is much lower than the expected value from bulk properties, consistent with an electron accumulation layer and/or dipole on the surface.

Figure 2.5 (left) shows AM mode KPFM for both the *n*-type and *p*-type InAs(001)-(4×2) surfaces. The measured surface work functions of *n*-type and *p*-type InAs(001)-(4×2) are 4.39 ± 0.01 eV and 4.43 ± 0.01 eV, respectively, with a cantilever calibration error of ± 0.1 eV. The cantilever calibration error arises from the uncertainty of the absolute work function of HOPG. The electron affinity of InAs is 4.9eV, which puts the surface work function of *n*-type and *p*-type InAs(001)-(4×2), 0.51eV and 0.47eV, respectively, above the CBM. AM mode KPFM shows consistent results with a standard deviation of 0.016eV and a full width half maximum less than 0.011eV over several samples. FM mode KPFM on *n*-type and *p*-type InAs(001)-(4×2) surface reconstruction being pinned deep in the conduction band, in accordance with an electron accumulation and/or surface dipole.

Figure 2.5 (middle) shows both the AM mode KPFM for *n*-type and *p*-type InAs(110) cross-section surfaces. The KPFM results on the InAs(110) cross-

sectional surface agrees with the STS results, showing work functions of *n*-type and *p*-type near the theoretical bulk values. The measured surface work functions of *n*-type and *p*-type InAs(110) are 4.84 ± 0.01 eV and 5.35 ± 0.01 eV, respectively, with a cantilever calibration error of ±0.1eV. The bulk Fermi energy level position for *n*-type InAs is approximately 0.5eV above the VBM for a doping density of 1×10^{18} cm⁻³[39; 40]. The bulk Fermi level p-type InAs for doping concentration of 1×10^{17} cm⁻³ is 0.09eV above the VBM[40]. If the bulk work functions are measured for *n*-type and *p*-type, a difference of 0.41eV should be observed. KPFM shows a 0.51 ±0.2eV difference. The measured difference of *n*-type and *p*-type is consistent with flat band conditions[18]. AM mode KPFM showed consistent results, with a standard deviation of 0.011eV, and a full width half maximum less than 0.015eV over several samples. FM mode KPFM is also performed with *n*-type and *p*-type InAs(110) cross-sectional surfaces having a surface work functions of 4.83 ±0.1eV and 5.31 ±0.1eV, respectively. KPFM on the InAs(110) cross-sectional surface demonstrates that the surface Fermi energy level is unpinned.

Figure 2.5 (right) shows AM mode KPFM for both the *n*-type and *p*-type InGaAs(001)-(4×2). The surface work functions of *n*-type and *p*-type are 4.25 ± 0.01 eV and 4.24 ± 0.01 eV, respectively, with a cantilever calibration error of ± 0.1 eV. AM mode KPFM showed consistent results with a standard deviation of 0.056eV and a full width half maximum less then 0.011eV over several samples. FM mode KPFM shows *n*-type and *p*-type InGaAs(001)-(4×2) surfaces having work functions of 4.1 ± 0.1 eV and 4.1 ± 0.1 eV. The electron affinity of InGaAs is

4.5eV, and the KPFM data would therefore suggest that the surface Fermi level of *n*-type and *p*-type InGaAs(001)-(4×2) is 0.25eV and 0.26eV above the conduction band edge. KPFM shows the InGaAs(001)-(4×2) a smaller work function than expected surface, indicating an electron accumulation and/or surface dipole[37; 38]. As discussed below, however, we postulate that this difference arises from the presence of a surface dipole that shifts the surface Fermi level measured by KPFM relative to that measured by other techniques such as STS or photoemission.

2.5 Discussion

STS and KPFM of the InAs(001)-(4×2) surfaces show one notable difference. For STS on InAs(001)-(4×2), the surface Fermi energy level appears in the band gap near the CBM, while KPFM shows the surface work function deep into the conduction band. It is proposed that the difference of the surface Fermi level between STS and KPFM is due to an intrinsic difference in the two methods. KPFM is extremely sensitive to fixed charges and surface dipoles, while it is proposed that the band-edge energies and surface Fermi level positions measured by STS are much less sensitive to fixed surface charge. STS measures the dynamic tunneling conductance which is proportional to the surface density of states (DOS)[19; 41],

$$(dI/dV)/(I/V) \propto DOS_{sample}(E_F - eV).$$

(2.5.1)

Figure 2.6a-b shows the band bending due to the surface states, indicated in the orange region, along with the effective surface work function caused by the surface dipole, indicated by red region. Figure 2.6a illustrates the different tunneling mechanisms in STS for InAs(001)-(4×2) in the presence of a static charge layer located on the surface. The solid arrow indicates the conditions under positive sample bias where the tunneling current is dominated by electrons from the tip to empty conduction band states, ignoring the static charge layer. The dashed arrow points to the conditions under negative sample bias where the tunneling is dominated by electrons from the static charge layer. The static charge might influence the absolute tip-sample distance in STS, which will have a slight, but negligible, effect on the measured tunneling. For STS to ignore the states charge the static charge would need to be located physically closer to the tip than the surface states responsible for the pinning of the surface Fermi level.

If the static charge or surface dipole is a thin layer above the surface states it is possible to have little or no influence on the amount of band bending in the semiconductor, because the surface states have already pinned the Fermi level. Optical based techniques measure the amount of band bending at the surface relative to the bulk, therefore optical based techniques would also not observe the presence of a static charge layer. Ultraviolet photoelectron spectroscopy (UPS) on InAs(001)-(4×2) shows the surface Fermi level 0.3-0.5eV above the VBM [30; 43]. The difference in Fermi level position is dependent on the surface preparation method. Samples prepared with ion-bombardment and

annealing, show surface Fermi level 0.5eV above the VBM, while decapped InAs is located 0.3eV above the VBM [44; 45]. The InAs(001)-(4×2) samples used in this paper are decapped MBE grown wafers so the surface Fermi level near the CBM is expected. No significant difference in the position of the surface Fermi level between UPS and STS is observed. Both UPS and STS consistently show both *n*-type and *p*-type InAs(001)-(4×2) are pinned near or in the conduction band. However, an estimated difference in the position of surface Fermi level between UPS/STS and KFPM is 0.4-0.51eV for InAs(001)-(4×2).

The main differences between STS and KPFM are the interactions with fixed surface charge or surface dipole. Figure 2.6b shows a band diagram illustrating a potential drop across a surface dipole influencing the measured surface work function of *n*-type InAs(001)-(4×2) with KPFM. Two potential features might cause a surface dipole: surface defects or strained surface atoms. Defects, like step edges or dislocations, can be traps sites exhibiting long time constants, acting as fixed charges. The InAs(001)-(4×2) surface has strained atoms or a strained reconstruction[12] producing charge transfers from bulk atoms to the surface atoms, and potentially causing fixed surface dipoles. A small amount of charge transfer can cause a significant potential drop at the surface. To simplify, the charge transfer is assumed to be perfectly perpendicular to the surface and spread over one atomic layer. The density of trapped charge on the surface required to account for a 0.4-0.51eV potential difference between STS and KPFM is estimated with the following equation,

$$V_{dipole} = \frac{q Q_{fixed} \Delta q r}{\varepsilon_0}, \qquad (2.5.1)$$

where ε_0 is the vacuum permittivity, r is the one atomic layer (~3Å), and Δq is the charge transfer per defect (assumed to be one). A density of fixed charge of Q_{fixed} \approx 7.3-9.3×10¹² cm⁻² could generate a dipole voltage drop of 0.4-0.51eV.

The existence of surface states and fixed charges on InAs(001)-(4×2) is further supported by comparing the STS and KPFM results to the InAs(110) surface, known to be unpinned, with a low defect density. Cleaved InAs(110) has flat band conditions[5; 18]. The work functions of the InAs(110) crosssectional surfaces measured with KPFM are 4.84 ± 0.1 eV and 5.35 ± 0.1 eV for *n*type and *p*-type. A difference of 0.2 ± 0.4 eV is estimated for STS and KPFM on *n*-type InAs(110). The STS error can be as high as ± 0.3 eV[41]. With few surface states, STS will be extremely sensitive to any potential difference between the tip and the surface and is more susceptible to tip-induced band bending[32-34]. For *p*-type, the difference between the two measurements for both STS and KPFM is within the measurement error. The STS and KPFM results for the InAs(110) cross-sectional surface indicate the expected results for an InAs surface having low defect density and low static charge density.

The density of surface defects also influences the static charge. The defect densities on InGaAs(001)-(4×2) are higher than InAs(001)-(4×2). STS for both InGaAs(001)-(4×2) and InAs(001)-(4×2) show the surface Fermi level approximately 0.3eV above the VBM. The STS results for InGaAs(001)-(4×2) are consistent with the Fermi level position measured with UPS and PL showing

the surface Fermi level in the bandgap. The estimated difference in the position of surface Fermi level between PL/UPS/STS and KFPM for InGaAs(001)-(4×2) is 0.4-0.69eV, corresponding to a fixed charge density of $Q_{fixed} \approx 7.3-12 \times 10^{12}$ cm⁻². The fixed charge is likely to be caused by a combination of the strained surface reconstruction and the surface defects.

2.6 Summary

STS and KPFM was performed on InAs(001)-(4×2), InAs(110) and InGaAs(001)-(4×2). STS shows InAs(001)-(4×2) and InGaAs(001)-(4×2) are pinned 0.3eV above the VBM while InAs(110) is consistent with flat band conditions. The KPFM results are consistent with the InAs(110) STS results. The measured CPD for InAs(001)-(4×2) and InGaAs(001)-(4×2) indicates the presence of static charge. It is proposed that the discrepancy between STS and KPFM is due the differential influence of static charges or surface dipoles on these techniques. It is proposed that STS ignores any static charge because the measurement observes only current flow into/from partially filled states. Conversely, KPFM is highly sensitive to static charge because KPFM minimizes the electrostatic forces between the surface and the tip. By combining STS and KPFM to probe clean surfaces, the surface states and the static charges can be measured for surfaces with a large number of static charges.

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Figure 2.1: (a) High resolution filled state STM of $InAs(001)-(4\times 2)$ and ball-stick diagram of surface reconstruction. Scan size is 11x11nm.



Figure 2.2: (a) 100x100nm filled state STM of typical InGaAs(001) surface. (b) 100x100nm filled state STM of typical InAs(001) surface.



Figure 2.3: High resolution filled state STM of InAs(110) surface and ball and stick diagram of surface. Scan size is 11x11nm.



Figure 2.4: Normalized $(dI/dV)/\overline{(I/V)}$ spectra of (a) InAs(001)-(4×2), (b) cleaved InAs(110) and (c) InGaAs(001)-(4×2) using variable-z STS. Δz for spectra ranges from 0.1-0.3nm/V. I/V is smoothed before $(dI/dV)/\overline{(I/V)}$ is calculated [17].



Figure 2.5: KPFM measured work functions from AM mode measurement along with bulk bandgaps. The n-type (blue) and p-type (red) work functions are measured on separate samples. The rectangles indicate the band gap energies calculated from the bulk electron affinities and bandgaps. (Left) InAs(001) surfaces have n-type and p-type surface work functions pinned in the conduction band. (Middle) InAs(110) surfaces have unpinned bulk-like work functions. (Right) InGaAs(001) surfaces have n-type and p-type and p-type surface work functions pinned in the conduction band.



Figure 2.6: (a) Band diagram illustrating the dominate tunneling mechanisms during STS on n-InAs(001). The presence of a surface dipole is of little effect to the tunneling conditions. The position of the surface Fermi level is pinned near the CBM caused by surface states. (b) Band diagram illustrating the effects of a surface dipole has large effect upon the CPD of n-type InAs(001) measured with KPFM.

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Chapter 3

Atomic Imaging of ALD Oxide Nucleation with TMA on As-rich InGaAs(001) 2×4 vs Ga/In-rich InGaAs(001) 4×2

3.1 Abstract

Formation of a contaminant free, flat, electrically passive interface to a gate oxide such as a-Al₂O₃ is the critical step in fabricating III-V MOSFETs; while the bulk oxide is amorphous, the interface may need to be ordered to prevent electrical defect formation. A two temperature in-situ cleaning process is shown to produce a clean, flat group III or group V rich InGaAs surface. The dependence of initial surface reconstruction and dosing temperature of the seeding of aluminum with trimethylaluminum dosing is observed to produce an ordered unpinned passivation layer on InGaAs(001)-(4×2) surface at sample temperatures below 190 °C. Conversely, the InGaAs(001)-(2×4) surface is shown to generate an unpinned passivation layer with a seeding temperature up to 280 °C. For both reconstructions, the chemical drive force is consistent with formation of As-Al-As bonds. The optimal seed layer protects the surface from background contamination.

3.2 Introduction

III-V semiconductors and high-k oxides for metal oxide semiconductor field effect transistors (MOSFET) are an alternative/complementary technology to traditional silicon MOSFETs because of their potentially high drive currents at low source-drain voltage [1]. To enable low power MOSFET operation, there are

45

several requirements. (1) The MOSFET must have a low gate voltage which requires a small equivalent oxide thickness (EOT), below 1 nm, so the oxide growth must be nucleated in each unit cell. (2) The semiconductor channel must have a high mobility and high saturation velocity so the oxide-semiconductor interface must be extremely flat. (3) The subthreshold swing must be close to ideal which necessitates a low interfacial trap density (D_{it}) so the oxide-semiconductor interfaces must have a low defect density. To form a low defect oxide/III-V interface, the semiconductor surface may need to be clean prior to oxide nucleation and the oxide-semiconductor interface may need be ordered to minimize defect formation. (4) Remote phonon scattering needs to be minimized which is usually achieved by having the first gate oxide layer be ALD deposited amorphous Al₂O₃ [2].

Surface channel III-V MOS devices can be fabricated with atomic layer deposition (ALD) high-K gate-first processes [3-6] which are similar to SiO₂ growth on silicon or ALD of high-K on silicon [7-11]. The key for a gate-first process is that subsequent processing steps cannot degrade the semiconductor, the dielectric, or the oxide-semiconductor interfaces. For silicon, the only commercial ALD high-k fabrication process is a replacement gate process (a type of gate-last process) to avoid processing induced damage [12]. Some work has been reported on replacement gates on III-Vs [13]. While preparing silicon for gate-last processing is straightforward, preparing an ordered clean III-V semiconductor surface for gate-last processing is a challenge. It has been shown that ALD of trimethylaluminum (TMA) [14; 15] or

tetrakis(ethylmethylamino)hafnium (TEMAH) [16] on III-V has self-cleaning properties by reducing the presence of As-O and Ga-O bonds. Recently, a combination of atomic hydrogen and TMA has shown an improvement of the D_{it} over just traditional TMA cleaning [17]. However, for high quality dielectric semiconductor interfaces, further reduction or cleaning of native oxide may be required and the interface must be atomically flat. Furthermore, aggressive oxide thickness reduction (equivalent oxide thickness or EOT scaling) is needed to fabricate small gate length devices with small subthreshold swings, and aggressive EOT scaling requires a very uniform ALD nucleation density with no pinholes [18]. The key barrier to a very practical problem is a simple surface chemistry challenge: development of a chemical process, which removes nearly all air induced defects and contaminants and leaves the III-V surface flat and electrically active for high nucleation density ALD gate oxide deposition, which unpins the Fermi level.

This study investigates the surface preparation for ALD of Al₂O₃ on In_{0.53}Ga_{0.47}As via atomic hydrogen cleaning and the initial passivation and gate oxide nucleation via TMA. It has been previously shown that atomic hydrogen cleaning can produce In/Ga-rich InGaAs surface with defect densities similar to decapped samples [19]; here it will be shown that the As-rich surface can also be produced with atomic hydrogen cleaning with low defect density and an unpinned electronic structure. Using in-situ scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS), the nucleation properties and electronic structure of TMA of hydrogen cleaned/annealed InGaAs(001)-(2×4) and (4×2)

surfaces are compared on the atomic scale as a function of dosing temperatures. MOSCAP studies by Huang et al. have shown that TMA based a-Al₂O₃ oxide growth at elevated temperature on 2×4 produces a lower D_{it} in comparison to the TMA dosing at elevated temperature on 4×2 [20]. Although the 2×4 surface may be more prone to formation of As oxides during ALD oxide growth, TMA is known to bond strongly to As atoms and therefore to be more efficient for reducing As_2O_3 formation than reducing Ga or In oxide formation [21, 22]. The present study, probes the initial bonding of TMA on the 2×4 and 4×2 surfaces as a function of temperature to determine if the formation of the initial monolayer determines the differences in electronic properties of gate oxides grown on these two reconstructions. By understanding the ordered bonding of TMA on different reconstructions, the mechanism of chemical passivation and electronic passivation can be elucidated for TMA on III-V surfaces. For both the As-rich 2×4 and the In/Ga rich 4×2 reconstructions, the bonding of the TMA reactions products and the passivation of the dangling bonds is consistent with the chemical driving force being the formation of As-Al-As bonds.

3.3 Experimental Technique

In the present study, two sample types were employed. The "capped" samples have an As₂ cap on a 0.2 μ m thick In_{0.53}Ga_{0.47}As layer grown by MBE on commercially available InP wafers. The MBE-grown InGaAs layers are doped *n*-type and *p*-type with a doping concentration of 2×10¹⁸ cm⁻³ of Si and Be dopants. Following MBE growth, the samples are capped with a 50 nm As₂ layer

and shipped/stored under vacuum before being loaded into the Ultra-high vacuum (UHV) chamber. The As₂ capped samples allow for comparison of pristine samples to air exposed/H cleaned samples. The "uncapped" samples have a 0.05 μ m thick In_{0.53}Ga_{0.47}As layer grown by MBE on commercially available InP wafer, without an As₂ cap. The uncapped samples are shipped/stored in air. The samples are loaded into an Omicron UHV chamber with base pressure below 1x10⁻¹⁰ Torr.

Capped samples are decapped in UHV at 330-360 °C and annealed to 380-420°C or 450-470 °C to form the InGaAs(001)-(2×4) or (4×2) surface reconstructions. Further details concerning the decapped samples and preparation methods are published in references [19; 23]. The uncapped samples are cleaned with atomic hydrogen in UHV using an Oxford Applied Research TC-50 thermal gas cracker in the preparation chamber at optimized sample temperatures and dose times with a H₂ pressure of $1-2\times10^{-6}$ Torr [19]. To form the As-rich InGaAs(001)-(2×4) surface reconstruction, the atomic hydrogen cleaning and post deposition annealing is performed at 270-290 °C. To form the In/Ga rich InGaAs(001)-(4×2), a higher temperature atomic hydrogen cleaning at 380-400 °C is performed followed by a post deposition anneal to 450-470 °C. Further details of atomic hydrogen cleaning to achieve the InGaAs(001)-(4×2) surface have been previously reported [19].

After decapping or surface cleaning, the samples are transferred *in situ* to an analysis chamber containing an Omicron variable temperature atomic force/scanning tunneling microscopy (AFM/STM) with a base pressure of

49

2x10⁻¹¹ Torr. STM provides atomic resolution of the surface morphology while scanning tunneling spectroscopy (STS) [24-27] is performed to determine the electrical quality of the surface. STS studies show that the clean InGaAs(001)-(4×2) surface reconstruction is pinned consistent with the presence of strained In/Ga dimers [19; 23; 28], therefore, to show the surface will be unpinned upon suitable oxide deposition, surface passivation is required. Auger electron spectroscopy (AES) was also performed in the preparation chamber using a Phi 10-155 cylindrical-Auger.

TMA is synergistic because it electrically passivates the surface, chemically passivates (i.e. protects the surface against oxidation), and provides a monolayer nucleation density required for very thin gate oxide formation [22]. The deposition of TMA is performed in the load lock, again allowing for sample transfer *in situ*. The load lock is first baked over night until it reaches a base pressure below 1×10^{-7} Torr to avoid water contamination (commercial ALD tools employ hot walls, which is a similar but faster technique). The sample is exposed to 1×10^{-6} -1×10^{-2} Torr of TMA vapor for 5 seconds at a fixed temperature. The samples are transferred into the preparation chamber for PDA, and AES. The samples are transferred back into the load lock where they are exposed to $\sim 10,000L$ of O₂, by leaking in a diluted gas mixture of 20% O₂ in helium.

3.4 Results and Discussion

3.4.1 STM of TMA on In/Ga-rich InGaAs(001)-(4×2) and As-rich InGaAs(001)-(2×4)

Figure 3.1a shows the STM image of the decapped InGaAs(001)-(4×2) surface. A similar surface can be formed with atomic hydrogen cleaning of air exposed surfaces at 380 °C followed by a PDA to 450-470 °C. The clean InGaAs(001)-(4×2) surface contains In/Ga dimers along with some defects, bright rows [29] indicated by an oval and dark rows [30] indicated by a rectangle in Figure 3.1a. After the InGaAs(001)-(4×2) surface is exposed to TMA vapor < 1x10⁻³ Torr for 5-10 sec with a sample temperature 24-190 °C, the surface undergoes an adsorbate induced surface reconstruction, details of this This low reconstruction can be seen in previously published results [22]. temperature TMA dosed surface exhibits a 90° rotation in the surface rows, and has row spacing is 0.8 nm, as shown in Figure 3.1b. The TMA surface reconstruction demonstrates high nucleation density and self-limiting behavior, ideal for aggressive EOT scaling. However, the surface passivation is quite different from the typical temperatures employed for Al₂O₃ ALD, 270-300 °C [17; 20; 31]. If the InGaAs(001)-(4×2) surface is exposed to TMA vapor < 1×10^{-3} Torr for 5-10 sec with a sample temperature above 250 °C, the surface again undergoes 90° change in row direction; however, the row spacing is doubled to 1.7 nm, Figure 3.1c. For the higher temperature TMA dosed surface, some second layer growth is observed. A black square in Figure 3.1c indicates a bright feature in STM that is consistent with second layer growth.

To further illustrate the difference between the two TMA surface reconstructions, higher resolution STM images are shown in Figure 3.2. Figure 3.2a shows the lower temperature dosing with the self-limiting highly

ordered adsorbate structure and a high nucleation density with 0.8 nm row spacing. While this high density passivation is ideal, this deposition process would require two temperature processing since typically Al₂O₃ ALD temperature is 270-300 °C. On the 280 °C TMA dosed surface, Figure 3.2b, the TMA still exhibits the self-limiting highly order adsorbate structure, just with wider spacing. Figures 2(c and e) show low coverage images of the low and high temperature TMA structures on the 4×2 surface. Besides the spacing being different between the low and high temperature structures the high temperature structure is ~0.05 nm taller than the In/Ga 4×2 rows, while the low temperature structure is the same height as the In/Ga 4×2 rows.

The InGaAs(001)-(2×4) surface contains As-dimers, and the surface has a low defect density in contrast to the 4×2 surface. Figure 3.3a shows a decapped InGaAs(001)-(2×4) with the classic zig-zag structure which is a mixture of single and double As-dimers [23]. The 2×4 surface does contain some narrow terraces indicated in rectangular box in Figure 3.3a. The As-rich 2×4 can be formed from an air exposed surface by lowering the atomic hydrogen cleaning temperature to 280 °C, Figure 3.3b. The atomic hydrogen cleaned surface shows more surface roughness than the decapped surface which is not ideal for high mobility channels. However, it may be possible to form lower roughness surfaces with optimization of the dosing and annealing times and temperatures. Lower roughness was observed with a PDA at 280 °C, Figure 3.3c, but the roughness reduction via PDA was greater on the 4×2 surface. Atomic hydrogen has been shown to convert atomic As and As₂O₃ into AsH₃ and/or H₂O [32]. The high

temperature hydrogen cleaning producing the In/Ga rich surface is consistent with atomic hydrogen at around 400 °C removing As on GaAs [33; 34] as well as the desorption of As oxides and As_2/As_4 occurs around 400 °C [33; 34]. The low temperature hydrogen cleaning forming the clean As-rich 2x4 surface implies that hydrogen does not react with As at 280 °C but the hydrogen still reduces the In, Ga, and As oxides to 280 °C.

After the InGaAs(001)-(2×4) is exposed to TMA vapor < 1×10^{-3} Torr for 5-10 sec at a sample temperature of 24 °C or 280 °C, the surface maintains its row direction, but loses the zig-zag characteristic seen on the clean 2×4 surface, Figure 3.3d. The TMA dosed on the 2×4 surface shows high nucleation density and self-limiting behavior, i.e. no second layer growth. This implies that in contrast to the 4x2 surface, the As rich 2x4 surface can be cleaned and functionalize at maximum density at 280 °C which is the typical growth temperature of ALD Al₂O₃ gate oxide. The wider temperature range for maximum density TMA chemisorption on the 2×4 surface is consistent with the 2×4 surface having As-As dimers (382.0 ± 10.5 kJ mol⁻¹, the bonding enthalpies used are from the gas phase) which should strongly bond to the aluminum atom, Al-As (202.9± 10.5 kJ mol⁻¹) in the expected dissociative chemisorption product, dimethyl aluminum since one As-As bond will be replaced with two As-Al bonds in As-Al(CH₃)₂-Al bonding geometry [35].

Figure 3.4 illustrates possible bonding models for the clean and TMA dosed surfaces for both the 4×2 and 2×4 reconstructions. One model of the clean 4×2 contains a In/Ga row with In/Ga-dimers in the trough [28; 36],

Figure 3.4a. The TMA dosed and annealed below 190 °C induce a surface reconstruction that rotates the row order 90° with 0.8 nm row spacing [22], shown in Figure 3.4b. At a higher dosing or annealing temperatures, it is hypothesized that some methyl groups desorb leaving dangling bonds on the aluminum atoms. Another model of the clean 4×2 surface is shown in Figure 3.4d based on a model for InAs and InSb 4×2 [37; 38]. The respective model for the TMA dosed and annealed surface below 190 °C again induces a surface reconstruction to generate a row order of 90° with 0.8 nm row spacing, Figure 3.4e. Furthermore, at higher dosing or annealing temperatures some methyl groups desorb leaving dangling bonds. The dimethyl-aluminum bonded to the surface is tetrahedral coordinated; therefore, if a methyl desorbs, the dangling bond should be directed along the [110] direction. In STM, row spacing of 1.7 nm are observed suggesting the dangling bonds occurring every other row. The rows on the high temperature TMA dosed 4×2 shown in Figure 3.2d are ~0.05 nm taller than the In/Ga rows and have a row spacing of 1.7 nm. Further experiments or calculations are needed to support this model. However, the presence of dangling bonds for the high temperature TMA dosed 4×2 surface is consistent with the pinned electronic structure as shown below. The clean 2×4 surface contains rows of single or double As-dimers [23], Figure 3.4g. It is hypothesized that the aluminum atom in the TMA chemisorption product breaks the As-dimers to form two AI-As bonds; this would also generate a high nucleation density of AI on the surface as shown in Figure 3.4h.

3.4.2 STS of TMA on InGaAs(001) (4×2) vs (2×4)

The STS spectra for clean n-type and p-type InGaAs(001)-(4×2) as shown in Figure 3.5(a and b). For the decapped surface (solid blue curves), Fermi level on both the n-type and p-type samples is positioned near the valance band (VB) indicating the decapped surface is pinned. After TMA dosing of the n-type InGaAs(001)-(4×2) surface at 190°C, the spectra for n-type shifts relative to the pinned clean surface; for the 190°C TMA dose surface the Fermi level on n-type is near the conduction band edge while on p-type it is near the valence band edge consistent with an unpinned interface. Conversely, after TMA dosing on the n-type InGaAs(001)-(4×2) surface at 240°C, the spectra is similar to the decapped surface consistent with pinning. The data is consistent with the existence of a maximum dosing temperature for formation of a good electrical interface between the clean 4×2 and the initial seed layer of TMA. This difference correlates with the different adsorbate induced surface reconstructions: the unpinned 0.8 nm spacing TMA and the pinned 1.7 nm spacing TMA reconstruction. The spectra suggest that the initial seed layer needs to be performed at lower temperatures to achieve an unpinned interface, requiring a change in sample temperatures in the oxide growth.

The spectra for the 2×4 surface suggest a different trend. Figure 3.5(c and d) show the spectra for n-type and p-type InGaAs(001)-(2×4). On the decapped 2×4 surface (solid blue curves), the surface Fermi level for n-type is near the conduction band and near the VB for p-type consistent with the surface being unpinned. After TMA dosing on the n-type InGaAs(001)-(2×4) at 280 °C,

the surface Fermi level remains approximately in the same position, suggesting the TMA leaves the surface unpinned. The spectra are consistent with the initial TMA seed layer maintaining an unpinned surface at higher temperature consistent with the strong bonding the TMA chemisorption product to the As-As dimers.

3.4.3 AES of initial passivation of InGaAs(001) (4×2) vs (2×4)

Table 3.1 shows the atomic ratios of relative concentrations of the C, O, and AI for the clean and dosed InGaAs(001)-(4×2) surfaces, and the corresponding spectra are shown in Figure 3.6. Using the intensity of the major auger transition peak, the atomic ratios can be estimated [39]. For the LMM transition of aluminum the intensity was estimated by the average of four different peak fittings. The total spectrum was either normalized to the In MNN transition or a low energy As peak that is just slightly higher in energy than the AI peak. The intensity was measured by taking the difference between the clean surface and the peak when the spectrums were aligned to either the valley just below or above the aluminum peak. The errors reported are from the standard deviation of these measured intensities along with the normalized noise, taken in an energy range with no peaks.

After dosing the clean 4×2 with TMA, an aluminum peak can be clearly seen in Figure 3.6. The percentages for the aluminum peak are difficult to extract because the peak overlaps other low energy In, Ga, and As peaks. An estimate of the aluminum concentrations are 2.07 ±0.3% for the 24 °C and 2.36 $\pm 0.3\%$ for the 280 °C dosed surfaces. With the model shown in Figure 3.4, if only the first layers were detected with AES the saturation coverage of aluminum would be $\sim 6\%$, however, AES has an interaction depth $\sim 1-2$ nm. The carbon concentrations increased to over 12% for both the 24 °C and 280 °C TMA dose. in carbon concentration is consistent with dissociative The increase chemisorption of TMA to the surface breaking Al-methyl bonds, and chemisorption of the dissociated methyl to the surface introducing site blocking which restricts more aluminum bonding. Furthermore, the presence of methane or ethyl byproducts from the dosing source can produce an increase in the carbon contamination. With a constant following or hot wall system, these by produces maybe be reduced. The slight increase in aluminum coverage on the 280 °C surface is consistent with some of the chemisorbed methyl that blocks further dissociative chemisorption of TMA at 24 °C desorbing at 280 °C. During the 280 °C anneal in the preparation chamber a large pressure burst is observed also consistent with further desorption.

After, the decapped 4×2 surface was exposed to 15,000L of O_2 , the oxygen increased to 7.8 ±0.1% while the carbon remained below 3%, top row Figure 3.6. With the interaction volume of AES, 7.8 ±0.1% is a reasonable concentration for saturation coverage of oxygen on the ln/Ga rich surface. It should be noted that the dosing conduit for the O_2 is a Teflon tube that is not baked, so background water may be present. After TMA dosing the surfaces were again exposed to 15,000L of O_2 . The 24 °C TMA dosed surface which was subsequently annealed to 200 °C shows better resistance to oxygen and carbon

contamination in comparison to the higher temperature TMA dosed surface. In STM, it was shown in Figure 3.1 that the higher temperature TMA dose on the 4×2 surface showed a wider row spacing allowing for more oxygen or carbon to react with dangling bonds or undercoordinated In, Ga or As surface atoms. It was also shown, in Figure 3.5, that the higher temperature surface was pinned, which usually occurs when surface atoms have dangling bonds or are undercoordinated. In Figure 3.6, the exposure of O_2 to the decapped clean surface decreases the low energy Ga and As peaks suggesting substrate oxidation. For the 25 °C or 280 °C TMA dosed surface, O₂ exposure induces a 5 eV shift of the aluminum peak to lower energy (dashed arrow), consistent with Al-O bonding [40] and less substrate oxidation. During the post deposition anneal the aluminum scavenges for oxygen, because the AI-O (511 \pm 3 kJ mol⁻¹) bond is stronger than the As-O(481 \pm 8 kJ mol⁻¹), Ga-O (353.5 \pm 41.8 kJ mol⁻¹) or In-O $(320 \pm 41.8 \text{ kJ mol}^{-1})$ bonds [35]. It should be noted that the increase in aluminum concentration after O₂ exposure is due to the combination of the decrease in the low energy Ga peaks, a shift in the aluminum peak, and any residual TMA remaining in the ALD chamber.

The respective data for TMA and O₂ dosing on the InGaAs 2×4 surface is shown in Table 3.2 and the spectra can be seen in Figure 3.6. The aluminum concentration on the 2×4 surface show similarities to that of the 4×2 surface, consistent with a high nucleation density of aluminum breaking the surface Asdimers and makes two Al-As bonds. The AES atomic ratios for aluminum, carbon and oxygen for the 24 °C and 280 °C dosed 2×4 surfaces support the results seen in STM showing nearly identical surface structures. The slight difference in aluminum concentration could be caused by a reduction of site blocking at elevated temperatures.

The decapped surface exposed to 15,000L of O₂ shows an increase of oxygen to 5.1 ±0.1% and the carbon concentration increased to 9.6 ±0.1%, top row Figure 3.7. The large oxygen and carbon concentration would correlate to a monolayer of reactance on the As-rich surface. This sensitivity to carbon is a clear difference between the 2×4 and 4×2 surfaces, it is expected that the 2×4 surface is more reactive and therefore more susceptible to background contamination. After TMA dosing the surfaces were exposed to 15,000L of O₂. The 280 °C TMA dosed 2×4 surfaces shows a shift in the aluminum peak of 5 eV to lower energy, consistent with Al-O bonding. However, the 24 °C TMA dosed 2×4 resembles a decrease in the low energy Ga and As peaks similar to that of the oxidized decapped surface. The higher temperature TMA dosed surface, therefore, shows an improvement in protecting the reactive 2×4 surface from carbon or oxygen reactions.

3.5 Summary

Atomic hydrogen cleaning is able to restore InGaAs(001)-(4×2) or (2×4) surface allowing for a gate-last or replacement-gate process. Formation of an electrical passive interface after TMA reaction on the InGaAs(001)-(4×2) requires atomic hydrogen cleaning around 380 °C followed by a PDA to 450-470 °C and initial seeding of TMA at sample temperature below 190 °C. The lower

temperature seeding of InGaAs(001)-(4×2) with TMA shows a high nucleation density of aluminum that is less prone to oxygen reaction than a higher temperature seeding, while exhibiting an unpinned interface. Higher temperature (>190 C) seeding with TMA on the 4×2 illustrates a non-ideal surface, which is more prone to carbon and oxygen contamination and exhibits a pinned interface. For the InGaAs(001)-(2×4), the atomic hydrogen cleaning and formation of an unpinned interface after TMA reaction can be achieved at a more ideal ALD temperature of 280 °C while maintaining a high nucleation density. Furthermore, the high temperature seeding shows an improvement in the protection of the surface in comparison to the lower temperature dosed surface from background carbon and oxygen consistent with formation of very strong As-AI-(CH3)x bonds. The advantage of the 4×2 gate-last process is that it can produce extremely flat surfaces but requires multiple temperature changes making it difficult to maintain a clean surface. On the other hand the 2×4 gate-last process can be achieved at the same temperature as common AI_2O_3 growth temperatures, however my have a higher surface roughness. For both the As-rich 2×4 and the In/Ga rich 4×2, the surface chemistry of TMA is consistent with the dominant driving force being the formation of strong As-Al-As bonds which create an electrically passive interface and protect the surface from oxidation.

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Figure 3.1. Filled state STM images (100 ×100 nm²) (a) decapped InGaAs(4×2). Oval indicates bright defects, rectangle indicates dark defects. Arrow indicates row direction. (b) ~1,000 L room temperature dose of TMA @ P=1e⁻⁴ Torr on the 4×2 surface, showing a 90° change in the surface order with 0.8 nm spaced rows, indicated by arrow. This surface structure is observed for dosing temperatures from room temperature to 190 °C. (c) ~1,000 L 280 °C TMA dose @ P=1e⁻⁴ Torr and anneal to 290 °C on 4×2 surface, showing the same 90° change with increase row spacing of 1.7 nm. Insets are 10 ×10 nm² STM images of respective images. Black square indicates bright features, most likely second layer growth.



Figure 3.2. Filled state STM images (50 ×50 nm²) (a) ~1,000 L 190 °C dose of TMA @ P=1e⁻⁴ Torr on the 4×2 surface, showing an ordered surface with 0.8 nm spaced rows. (b) ~100 L 250 °C TMA dose @ P=1e⁻⁴ Torr on 4×2 surface, showing an ordered surface with increased row spacing of 1.7 nm. Insets are 10 ×10 nm² STM images of respective images. (c) Low coverage TMA dose on 4×2 dosed at room temperature and annealed to 200 °C. (d) Line traces for low coverage scans. Solid line for the room temperature dose and anneal to 200 °C. Dotted line for the room temperature dose and anneal to 300 °C. (e) Low coverage TMA dose on 4×2 dosed at room temperature dose and anneal to 300 °C.



Figure 3.3. Filled state STM images ($100 \times 100 \text{ nm}^2$) (a) decapped InGaAs(2×4) (b) uncapped InGaAs sample annealed for 30 min at 280 °C followed by 30 min hydrogen (1800 L) dose at 285 °C. (c) After post deposition anneal at 290 °C for 30 min. (d) After a ~1,000L dose of TMA at 285 °C, the surface shows similar structure as decapped 2×4 surface. The ordered TMA surface is seen over a wide range of temperatures (24-285 °C) and pressures ($5e^{-6} - 1e^{-3}$ Torr), and a low dangling bond density is observed with the doses > $1e^{-4}$ Torr. At much higher pressures the surface looks amorphous. While the 2×4 row direction and symmetry are preserved, the row structure is modified.



Figure 3.4. Ball-and-stick diagram based on the model from Feldwinn *et al.* [36] of (a) the clean 4×2 surface, (b) the adsorbate induced reconstruct of TMA dosed below 190 °C on 4×2 and annealed [22], (c) a possible model of the higher temperature adsorbate induced reconstruct of TMA on the 4×2 reconstruction containing dangling bonds. Ball-and-stick diagram based on the model from Goryl *et al.* [37] and Kumpf *et al.* [38] of (d) the clean 4×2 surface, (e) a possible adsorbate induced reconstruct of TMA dosed below 190 °C on 4×2 and annealed, (f) a possible model of the higher temperature adsorbate induced reconstruct of TMA on 4×2 containing dangling bonds. Ball-and-stick diagram based on the model from TMA on 4×2 containing dangling bonds. Ball-and-stick diagram based on the model from Shen *et al.* [23] of (g) the clean 2×4 surface with double or single dimer unit cells, and (h) the TMA dosed surface on the double or single dimer unit cells. Note it is possible CH₃ groups may also be adsorbed on the surface.



Figure 3.5. STS spectra for the TMA dosing on InGaAs 4×2 and 2×4 at various temperatures. (a) Spectra for n-type InGaAs 4×2 showing both the decapped and 250 °C TMA dose have a surface Fermi level near the Valence Band (VB) while the TMA dosed at 190 °C surface are near the Conduction Band (CB). (b) All the spectra show the surface Fermi levels are near the VB. The 4×2 spectra indicate the TMA surface reconstruction at 190 °C with 0.8 nm spacing are unpinned while the TMA dosed surfaces at temperatures above 250 °C with 1.7 nm spacing are pinned. (c) Spectra for n-type InGaAs 2×4 showing both the decapped and 280 °C TMA dose have a surface Fermi level near the Conduction Band (CB). (d) Both the decapped and 280 °C TMA dosed surfaces the surface Fermi levels are near the Valence Band (VB). The 2×4 spectra indicate the TMA leaves the surface unpinned over a wider processing window.

Table 3.1: AES atomic ratios for InGaAs(001)-(4×2) surface and dosed surfaces. The values are the average of four fittings of the AI peak, either normalized to the In peak or a low energy Ga peak. The percent does not correspond to the fraction of a monolayer but instead is the percent of the total Auger signal from In, Ga, As, AI, C, and O. All clean surfaces show an atomic concentration of carbon <3% and oxygen <1%, demonstrating the initial surface is extremely clean. It is noted the carbon and oxygen levels are a function of Auger spectroscopy conditions since the Auger electron gun deposits carbon and oxygen on the surface, efforts were taken to minimize the amount. The ideal aluminum coverage based on the model in Fig 4 is 6% but since the Auger samples multiple layers, the observed aluminum coverage at surface saturation is lower.

	С	0	AI
Clean 4x2	1.8 ± 0.1%	0.2 ± 0.1%	0.0 ± 0.1%
02	1.6 ± 0.1%	7.8 ± 0.1%	0.0 ± 0.1%
Clean 4x2	2.5 ± 0.1%	0.7 ± 0.1%	0.0 ± 0.1%
24 C TMA	14.2 ± 0.2%	1.1 ± 0.1%	2.1 ± 0.3%
02	16.9 ± 0.2%	1.2 ± 0.2%	2.5 ± 0.4%
Clean 4x2	3.3 ± 0.1%	0.6 ± 0.1%	0.0 ± 0.1%
280 C TMA	12.5 ± 0.1%	1.1 ± 0.1%	2.4 ± 0.3%
02	18.7 ± 0.1%	2.3 ± 0.1%	4.0 ± 0.1%

Table 3.2: AES atomic ratios for InGaAs(001)-(2×4) surface and dosed surfaces.
All clean surfaces show an atomic concentration of carbon <5% and oxygen <2%,
demonstrating the initial surface is extremely clean.

	С	0	AI
Clean 2x4	3.4 ± 0.1%	1.9 ± 0.1%	0.0 ± 0.1%
02	9.6 ± 0.1%	5.1 ± 0.1%	0.0 ± 0.1%
Clean 2x4	4.8 ± 0.2%	2.0 ± 0.2%	0.0 ± 0.2%
24 C TMA	9.7 ± 0.2%	1.9 ± 0.2%	1.9 ± 0.5%
02	16.3 ± 0.3%	3.0 ± 0.3%	3.2 ± 0.9%
Clean 2x4	1.3 ± 0.2%	0.5 ± 0.1%	0.0 ± 0.1%
280 C TMA	9.9 ± 0.1%	0.8 ± 0.1%	2.4 ± 0.4%
02	10.6 ± 0.2%	0.9 ± 0.1%	2.3 ± 0.6%



Figure 3.6. Normalized 3 keV AES spectra for 10,000-50,000 L TMA dosing and 15,000 L O₂ on InGaAs 4×2. Spectra for the aluminum (Left) carbon (Middle) and oxygen (Right) peaks. All spectra were taking using a lock-in to extract dN/dE using a 15 KHz 0.5 V modulation voltage, a lock-in time constant of 3ms and a sweep speed of 1 eV/S. The spectra shown are normalized to the indium peak. The indium, gallium and arsenic peaks (not shown) where consistent before and after dosing. (Top row) Spectra for the clean 4×2 surface dosed only with O₂ and anneal to 280 °C. (Middle row) Spectra for 4×2 surface dosed with TMA at room temperature and annealed to 200 °C, followed with an O₂ dose and anneal to 200 °C. (Bottom row) Spectra for 4×2 dosed with TMA at 280 °C and annealed to 280 °C, followed by an O₂ dose anneal to 280 °C. (Black solid) Decapped InGaAs 4×2, (Blue dashed) TMA dosed surface and (Red dotted) after O2 exposure. Dotted arrow in upper left indicates the lowering of the bulk signal with The dashed arrow middle left indicates the shift in the oxvgen reaction. aluminum peak with exposure to oxygen.



Figure 3.7. Normalized 3 keV AES spectra for 10,000-50,000 L TMA dosing and 15,000 L O₂ on InGaAs 2×4. Spectra for the aluminum (Left) carbon (Middle) and oxygen (Right) peaks. All spectra were taking using a lock-in to extract dN/dE using a 15 KHz 0.5 V modulation voltage, a lock-in time constant of 3ms and a sweep speed of 1 eV/S. The spectra shown are normalized to the indium peak. The indium, gallium and arsenic peaks (not shown) where consistent before and after dosing. (Top row) Spectra for the clean 2×4 surface dosed only with O₂ and anneal to 280 °C. (Middle row) Spectra for 2×4 surface dosed with TMA at room temperature and annealed to 280 °C, followed with an O₂ dose and anneal to 280 °C. (Bottom row) Spectra for 2×4 dosed with TMA at 280 °C and annealed to 280 °C, followed by an O₂ dose anneal to 280 °C. (Black solid) Decapped InGaAs 2×4, (Blue dashed) TMA dosed surface and (Red dotted) after O₂ exposure. Dotted arrow in upper left indicates the lowering of the bulk signal with The dashed arrow middle left indicates the shift in the oxvgen reaction. aluminum peak with exposure to oxygen.

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Chapter 4

InGaAs and InP surface preparation for ALD by hydrogen cleaning and improvement with high temperature anneal

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4.1 Abstract

Using in-situ atomic scale imaging with scanning tunneling microscopy/spectroscopy, a combination of atomic hydrogen dosing, annealing, and trimethyl aluminum dosing is observed to produce an ordered unpinned passivation layer on air exposed InGaAs(001)-(4×2) surface with only monatomic steps. This shows that conventional gate-last semiconductor processing can be employed to make a variety of electronic devices even on air exposed compound semiconductors. A similar atomic H cleaning procedure has been demonstrated to produced an ordered passivation layer on air exposed InP(001).

4.2 Introduction

Commercial III-V semiconductor devices such as high electron mobility transistors (HEMPTs) and heterostructure bipolar transistor (HBTs) all employ interfaces, which are grown in-situ in vacuum systems to avoid air contamination of the III-V surfaces. However, these devices are not suitable for practical logic

75

applications such as microprocessors because they cannot be scaled in size and have large off-state leakage currents. At present, the only device design which offers the compact size and low off-state currents required for microprocessors is the metal oxide semiconductor field effect transistor (MOSFET). Present MOSFETs are fabricated on silicon, but higher levels of integration (more devices per unit area) are limited by power dissipation; therefore, several hundred research papers are published each year upon development of MOSFETs using III-V semiconductors, especially InGaAs [1]. To enable low power MOSFET operation, a low supply voltage is required, the semiconductor must have high mobility and high saturation velocity, the oxide-semiconductor interface must have a low density of interface trap states (D_{it}), and the oxide-semiconductor interface must be nearly atomically flat to insure high mobility at high field strength.

Surface channel III-V MOS devices can be fabricated with atomic layer deposition (ALD) high-K gate-first processes [2-5] which are similar to silicon processes for SiO₂ growth on silicon or ALD of high-K on silicon [6-10]. The key for a gate-first process is that subsequent processing steps cannot degrade the semiconductor, the dielectric, or the oxide-semiconductor interfaces. For silicon, the only commercial ALD high-k fabrication process is a replacement gate process (a type of gate-last process) to avoid processing induced damage [11]. While preparing silicon for gate-last process is the order and cleanliness of the III-V channel prior to dielectric deposition. It has been shown that ALD of

trimethyl aluminum (TMA) [12; 13] or tetrakis(ethylmethylamino)hafnium (TEMAH) [14] on III-V has self-cleaning properties by reducing the presence of As-O and Ga-O bonds. However, for high quality dielectric semiconductor interfaces, further reduction or cleaning may be required and the interface must be atomically flat. Furthermore, aggressive oxide thickness reduction (equivalent oxide thickness (EOT) scaling) is needed to fabricate small gate length devices with small subthreshold swings, and aggressive EOT scaling requires a very high uniform ALD nucleation density with no pinholes due to surface contaminants [15]. The key barrier to solving a very practical problem is a surface chemistry challenge: development of a chemical process, which removes nearly all air induced defects and contaminants and leaves the III-V surface flat and electrically active for high nucleation density ALD gate oxide deposition which unpins the Fermi level.

While InGaAs(001) is the most common channel material for high mobility channels, InP(001) has been used successfully as a capping layer on the narrower bandgap InGaAs(001) channel. By using the InP layer, the energy level of the defects can be controlled. However, minimal trap and fixed charge density at the oxide/InP(001) interface are still critical issues. The purpose of comparing InP to InGaAs is motivated by recent results using an InP layer on scaled MOSFETs [16; 17]. The wide bandgap layer might influence the energy levels of the density of interface trap states (D_{it}) loacted at the oxide/semiconductor interface and their impact on the on and off currents. If the D_{it} of the dielectric/InP interface moves higher towards the conduction band edge

of the InP capping layer and away from the energy levels in the InGaAs bandgap over which the Fermi level is modulated, an improvement in device performance may occur. For InP, the Fermi level pinning position is usually 0.12eV below the conduction band edge [18]. The InP layer may also act as an electrostatic control layer which would confine carriers in the channel, and the mobility of the carriers might improve by decreasing surface scattering. The surface scattering in the channel with an oxide/InP/InGaAs stack should be better than for a simple surface channel oxide/InGaAs stack because the latticed matched In_{0.53}Ga_{0.47}As and InP should produce a well ordered interface with low surface roughness in comparison to an InGaAs/oxide interface.

Atomic hydrogen cleaning of III-V semiconductors has been investigated [19-25]. Traditional atomic hydrogen cleaning is performed at elevated temperatures as a surface preparation for molecular beam epitaxial (MBE) growth. This study investigates the hydrogen cleaning at 24°C and 380°C with post cleaning annealing to determine the influences of cleaning temperature and annealing temperature on electronic structure as well as surface defects, roughness, and step density. Atomic hydrogen has been shown to unpin GaAs [25], however, it induces surface etching [24; 26; 27]. It has been shown that the atomic hydrogen etch rate for silicon is lower at 700°C compared to room temperature (RT) [28]. However, for GaAs, the atomic hydrogen [29]. Etching must be minimized since it can induce surface roughness, which is incompatible with the thin channel structures required in low power highly scaled devices [10;

30; 31]. By employing scanning tunneling microscopy (STM) to probe in-situ hydrogen cleaned surfaces, the surface features can be studied at the atomic level.

4.3 Experimental Technique

In the present study, the samples are 0.2µm thick $In_{0.53}Ga_{0.47}As$ layer grown by MBE on commercially available InP wafers. The MBE-grown InGaAs layers are doped *n*-type and *p*-type with a doping concentration of 2×10¹⁸ cm⁻³ of Si and Be dopants. Following MBE growth, all samples are capped with a 50nm As₂ layer and shipped/stored under vacuum before being loaded into the Ultrahigh vacuum (UHV) chamber. The As₂ capped samples allow for comparison of pristine samples to air exposed/H cleaned samples. The samples are loaded into an Omicron UHV chamber with base pressure below 1×10⁻¹⁰ Torr. Samples are decapped in UHV and annealed at 450-470 °C to form the InGaAs(001)-(4×2) surface reconstruction in the preparation chamber. Further details concerning the samples and preparation methods are published in reference [32].

The order and defect density of decapped surface is quantified with scanning tunneling microscopy (STM) in the analysis chamber with a base pressure of 2×10^{-11} Torr. Afterwards, the decapped samples are transferred to the load lock and exposed to air for 0.5-30 minutes. Using an Oxford Applied Research TC-50 thermal gas cracker in the preparation chamber, the sample is cleaned with atomic hydrogen at various sample temperatures and dose times with a H₂ pressure of $1-2 \times 10^{-6}$ Torr. The percent of atomic hydrogen from the

thermal cracker at 65 watts is ~50%; the thermal cracker was operated at 60 watts. The percentage of atomic hydrogen at the sample surface is a mixture of the recombined background H_2 and the direct stream from the thermal cracker. The background H_2 should be inert; therefore, the reduction in surface oxides is assumed to be from the atomic hydrogen produced with the thermal cracker, however, the exact dose of atomic hydrogen is unknown since the measured pressure includes both the direct and background H and H₂ sources. Following the hydrogen cleaning, the sample is annealed to 460-480°C to regain the InGaAs(001)-(4×2) surface reconstruction, and STM is employed to determine the reconstruction, defect density, and surface roughness. The TC-50 thermal cracker employs a hot iridium tube to crack the H₂ molecules thereby avoiding contamination that can occur with hot tungsten filaments and or formation of ions that can occur with a plasma source; both metal contamination and ion bombardment probably would negatively influence surface cleaning, ordering, and electronic passivation [33; 34].

A similar sample procedure was used for the InP samples. The InP samples employed in this study are from an InP wafer with 1µm of InGaAs channel layer doped with 4×10¹⁸ cm⁻³ of Si channel layer and a 2nm InP undoped surface top layer. The samples were first degassed for several hours at 150 °C, followed with an exposure of atomic H to remove the oxide. The surface was inspected with STM to determine the quality of the cleaned surface. A comparison to a decapped surface was not performed because InP does not have an equivalent capping and decapping method used for the InGaAs. The
goal is to use the same surface preparation from InGaAs on InP to prepare the surface for an ALD gate oxide deposition. After atomic H cleaning, the InP surface was exposed to $1 \times 10^{-3} - 1 \times 10^{-2}$ Torr of TMA vapor for 5 seconds at room temperature (RT) followed by a 250 °C anneal in the preparation chamber.

STM provides atomic resolution of the surface morphology, but scanning tunneling spectroscopy (STS) [35-38] is performed to determine the electrical quality of the surface. The decapped InGaAs(001)-(4×2) surface reconstruction is pinned, consistent with the presence of strained In/Ga dimers[32; 39; 40], therefore, for the surface to be unpinned upon suitable oxide deposition, surface electrical passivation is required. TMA is synergistic because it both electrically passivates the surface and provides the monolayer nucleation density required for very thin gate oxide formation [41]. The deposition of TMA is performed in the load lock. The load lock is first baked over night until it reaches a base pressure below 1 x10⁻⁷ Torr to avoid water contamination (commercial ALD tools employ hot walls, which is a similar but faster technique). The sample is exposed to $1x10^{-3}$ -1x10⁻² Torr of TMA vapor for 5 seconds at room temperature (RT) followed by a 250°C anneal in the preparation chamber.

4.4 Results and Discussion

4.4.1 InGaAs(001)-(4x2)

Figure 4.1a shows an STM image of the decapped InGaAs(001)-(4×2) surface. The decapped surface includes two distinct defects: dark horizontal features (black rectangle) and bright vertical features (white rectangle). Similar

defects have been studied on $InAs(001)-(4\times 2)$, which has effectively the same surface structure as InGaAs(001)-(4×2). The dark horizontal features are described as missing-row-dimers [42], and the bright vertical features are described as the same In/Ga row dimers in the 4×2, however with 8Å spacing instead of 17Å [43]. There are some variation in the bright vertical features, probably caused by excess atoms bridge bonding between the As row edge atoms. After the InGaAs(001)-(4×2) surface is exposed to air for 0.5 minutes, an amorphous film is observed by STM, shown in Figure 4.1b. Note the surface was annealed to 200°C in order to achieve stable STM images. The oxide film of the As-rich 2×4 surface consist primarily of As₂O₃, Ga₂O₃, and In₂O₃ [22], and the In-rich 4×2 should have similar oxides with different ratios. Figure 4.1c shows a surface exposed to air for 30 minutes followed immediately by atomic hydrogen cleaning at 380°C for 30 minutes. The hydrogen cleaned surface shows dark features (red rectangle) consistent with monolayer etch pits; however, there is a reduction in the other defects observed on the decapped surface. Figure 4.1d shows the hydrogen cleaned surface after a 460-480°C anneal 10 minutes showing an increase in terrace size and uniformity. If the sample was not cleaned with hydrogen and only annealed to 460-480°C anneal for 10 minutes, the STM image resembles that of Figure 4.1b. The densities of horizontal dark defects (black rectangle) appear to be similar to the decapped surface while the vertical defects are drastically reduced. There are some bright vertical defect features, but these structures appear different from the features on the initial

decapped surfaces. The difference in structure is probably caused by removal of excess atoms by atomic hydrogen from the 8Å spacing row dimers.

To further investigate the defect densities and etch features, a set of images was recorded over a larger area. Figure 4.2a is a 500×500nm² STM image of the decapped surface showing ~242 (manually counted) of the bright vertical defect features with large terraces. After exposure to air for 30 minutes (no anneal) and a 30 minute dose of hydrogen at 380°C, the number of bright vertical defects is reduced to ~58 in Figure 4.2b; however, the STM image shows reduction in terrace size because of the dark monolayer deep etch features. Finally, if the sample is annealed to 460-480°C the bright defect features are further reduced to ~28 in Figure 4.2c, and the terrace size is restored to almost the same size as the decapped surface.

The atomic hydrogen induced etching features reduce the terrace sizes. There are two types of etching features, dark pits, inset Figure 4.2b, which shows removal of surface atoms in the plane of the terrace and incomplete terraces, inset Figure 4.2c, which illustrates a terrace that has been almost completely etched with only a residual amount remaining. Comparing the decapped sample to the 30 minute high temperature (HT) atomic hydrogen dosed without anneal sample, it is clear that there is a sharp increase in the etch pits. After a HT anneal, the surface shows a distinct improvement as seen in Figure 4.2c.

To quality the effect of annealing on etching feature density, the number of etch pits per unit area, the number of incomplete terraces per unit area, and the average fraction of the surface covered by etch pits and incomplete terraces was quantified. As shown in Table 4.1, for the 30 minute 380°C hydrogen clean surface, HT annealing reduces the density of dark etch pits by almost a factor of 50 and the percent coverage of the surface with etching features after annealing is reduced by almost a factor of 3. The hydrogen cleaned and annealed surface has etch feature densities similar to that of the decapped surface. The quantitative analysis shows that an air exposed sample after hydrogen cleaning and HT anneal is very similar surface to that of the decapped surface except the etch features are smaller on the hydrogen cleaned HT annealed surface while the similar features are larger on the decapped sample.

Figure 4.3 compares temperature and time of an air exposed samples cleaned with hydrogen; all samples are annealed to 460-480°C after hydrogen dosing. The temperature and the time influence the densities and surface coverage of etching features. The densities of etch pits, densities of incomplete terraces, and the percent surface coverage for the STM images in Figure 4.3 are presented in Table 4.1. The HT hydrogen dosing shows an improvement over the room temperature dosing (RT hydrogen) in the etch feature percent coverage of the surface. The 30 minute RT hydrogen dosed surface shows a lower density of etch pits compared to the 5 minute RT hydrogen dosed surface; however, the 30 minute RT hydrogen dosed surface is dominated by the incomplete terrace features, most likely due to the hydrogen dose which has etched more the 70% of the original terraces. At elevated temperatures, it appears that the surface atoms have enough mobility during hydrogen dosing to either reduce multilayer etching or repair the effects of multilayer etching. A similar process in which

surface mobility reduces roughness is well known on the GaAs surface in migration enhanced epitaxy [44; 45]. The 30 minute RT hydrogen dosed surface has bright and dark features, indicated by black squares. In Figure 4.3e the bright features range from 2-6 nm where the dark features range from 1.5-4.2 nm. Figure 4.3c of the HT hydrogen does surface does not show any of these bright or dark features indicating that the etching is uniformly occurring over the surface. This is consistent with an annealing process occurring simultaneously with etching for 380°C hydrogen dosing preventing multilayer etching while at 25°C only etching occurs.

Besides etch pits, step edges are a major defect that can reduce carrier mobility in the channel, because steps usually contain dangling bonds due to the undercoordinated bonding configuration. Using the Scanning Probe Image Processor (SPIP)'s grain analysis tool, the fraction of the surface covered in edge features was quantified (step edges, horizontal and vertical defects). Typical decapped surfaces (Fig 3a) have a 5.6% surface coverage of step edges. For samples with a 380°C sample temperature during hydrogen dosing, Figure 4.3b-c, show an improvement in comparison to the room temperature hydrogen dosing, Figure 4.3d-e. Typical surfaces after 30 minute air expose and 5 minute atomic hydrogen cleaning at 380°C followed by 460-480 °C have 7.6% step coverage (Fig 3b), close to that of the decapped surface.

Typical surfaces after a 30 minute air expose and a 30 minute atomic hydrogen cleaning at 380 °C followed by 460-480 °C have 13.9% surface coverage of step edges (Figure 4.4c), close to that of the decapped surface

consistent with the annealing removing most etching induced step formation. The RT hydrogen dosed samples even with a high temperature anneal were not as flat as the decapped samples with a percent coverage of edges of 13.4% and 15.4% for 5 and 30 minutes dose followed by 460-480 °C anneal. The role of sample temperature of surface morphology indicates that at 380°C surface mobility is enhanced resulting in smoother surfaces; however, at higher temperatures the etch rate might be increased because GaAs[29] atomic hydrogen etch rate increase with temperature.

Figure 4.5 shows STM images of atomic H cleaning at -40 °C. Directly after exposure to air for 30 minutes, the sample was dosed with atomic H for 30 minutes at -40 °C with a final anneal of 460-480 °C, Figure 4.5a. The surface shows large bright islands probably from residual oxide left after the atomic H cleaning. At sub O°C temperatures, the surface will condense water which might not be able to desorb during atomic H cleaning at -40 °C. However, if the sample is first annealed to drive off any residual water before cleaning, a -40 °C atomic H cleaning results in a surface morphology similar to the RT atomic H cleaned surface. Figure 4.5b shows a surface exposed to air for 30 minutes then annealed to 200 °C in UHV for 1.5 hours prior to atomic H cleaning for 30 minutes at -40 °C with a final anneal of 460-480 °C. The only major difference observed between the RT and the -40 °C atomic H dose surfaces is the number of steps on a 500×500 m² STM image. The surface shown in Figure 4.5b is consistent with inhomogeneous etching during atomic H cleaning at -40 °C.

The atomic hydrogen induced removal of the oxide layer involves multiple reactions. Atomic hydrogen can reduce Ga_2O_3 to Ga_2O and H_2O [22; 23; 27], and desorption of Ga_2O occurs at ~400°C on GaAs and InGaAs[23; 46]. The influence of atomic hydrogen on In oxides has been assumed to be similar to that of Ga oxides [22]. Atomic hydrogen has been shown to convert atomic As and As_2O_3 into AsH_3 and/or H_2O [47]. Atomic hydrogen on 400°C samples of GaAs and InGaAs is known to remove As[22; 23]. Furthermore, the desorption of As oxides and As_2/As_4 occurs around 400°C [22; 23]. This hydrogen induced volatilization of As is consistent with the reduction of any excess As defects on the hydrogen clean surfaces in the present study. The absence of any oxides in the present study is likely due to the >300 Langmuir exposure which reduces any Ga_2O_3 or In_2O_3 to suboxides which are volatilized during annealing along with any As oxides.

To determine the electrical quality of the InGaAs(001)-(4×2) surface, electrical passivation is required because the decapped surface is pinned [32]. Following atomic hydrogen cleaning, the surface was exposed to TMA at room temperature and annealed to 250°C; an STM image of the TMA dosed surface can be seen in Figure 4.4. The TMA induces a surface reconstruction creating a bulk like bonding configuration between the AI atoms and the surface As atoms[41]. The TMA passivation layer has horizontal rows of dimethyl aluminum. The surface is a highly ordered self-limiting layer that has high nucleation density. The self-limiting and high nucleation density is necessary for EOT scaling. The STM image of the TMA dosed surface shows this surfaces satisfies the key processing conditions for gate oxide deposition: an atomically flat, high nucleation density, and electrically unpinned as shown below by STS.

The STS spectra for n-type and p-type decapped InGaAs can be seen in Figure 4.6. The Normalized $(dI/dV)/(\overline{I/V})$ spectra is proportional to the local density of states of the surface [48; 49]. The STS was performed with a modulation frequency of 1 kHz, a lock-in time constant of 20 ms, and a T-raster of 40 ms; therefore, it is sensitive to all trap states with a lifetime less then 1 ms. In the spectra, the zero sample bias is the Fermi level position of the surface relative to the bands. For the decapped surface (solid blue curves), Fermi level on both the n-type and p-type samples is positioned near the valence band (VB) indicating the decapped surface is pinned. After air exposure and hydrogen cleaning for 5 minutes at room temperature followed by a 460-480°C anneal, the spectra look almost identical to the decapped surface, shown by the blue and green curves in Figure 4.6a for n-type InGaAs. This is also the case for p-type at room temperature, spectra not shown. STS spectra for the dark horizontal defects, bright vertical defects, and step edges were taken (not shown). The STS spectra for the defects showed a slight change in the relative signal intensity of the filled and empty states, however the differences were not enough to draw any significant conclusions. For InGaAs(001)-(4×2), the clean defect-free reconstructed surface is pinned which would make single defect site STS very difficult because the background signal from the reconstructed surface would dominated the local signal.

To demonstrate that atomic hydrogen cleaning not only restores the surface morphology but also the electrical characteristics, TMA is deposited to document the surface Fermi level unpinning. The spectra for the TMA dosed surface (dot dash red curves) shows the surface Fermi level near the conduction band (CB) for n-type samples, Figure 4.6a, and near the VB for p-type samples. Therefore, Figure 4.6c is consistent with the surface Fermi level being unpinned. For further details on the energy and density of remaining trap states, capacitance voltage measurements on Metal-Oxide-Semiconductor capacitor (MOSCAP) are needed, but these require extensive processing.

The STS results were also performed on surfaces cleaned with hydrogen for 5 minutes with a sample temperature of 380°C followed by a 460-480°C anneal. The spectra for n-type and p-type InGaAs can be seen in Figure 4.5b and d, respectively. Spectra directly after the hydrogen cleaning and after annealing were also taken, showing almost identical features to that of the decapped surface, spectra not shown. Within the limitations of STS, the surface electrical quality appears the same for the air exposed surface cleaned with hydrogen at RT and 380°C with a 460-480°C anneal. However, the STM indicates that there might be a difference in D_{it} based on the densities of etching features between RT and 380°C with a 460-480°C anneal.

4.4.2 InP

Figure 4.7a shows a STM image of InP after degassing an a 10 minute dose of atomic H at 380 °C. The surface shows removal of the native oxide by

89

atomic H exposure. The native oxide reduction by atomic H of InP, InPO₄, to H_2O , PH_3 , PH_2 , InH, and In has been reported in literature [50]. Others report the reductions of InPO₄, In(PO₃)₃, and In₂O₃ [19; 51]. Most reports are consistent with atomic H lowering the cleaning temperature for InP, and the exposure time for InP needed to clean the native oxide being longer than for GaAs. Five minute exposures to atomic H were also performed, not shown, which also had large bright features and partial coverage of the clean ordered surface. As shown in Fig 7, 10 minute exposures of InP to atomic H showed residual bright features that are most likely uncleaned oxide.

After 10 minute atomic H dose and high temperature annealing the InP surface shows some etch features indicated by the inset in Figure 4.7b. These etch features are different from that of InGaAs: they are much larger and deeper. Unlike InGaAs etch features, these InP etch features do not decrease in density with a high temperature anneal to 470 °C, Figure 4.7b. The InP etch features could either be an etch pit to the InGaAs channel layer or impurities in the InP layer. The origin of these dark etch features is difficult to determine because a comparison to a decapped InP sample can not be performed. Fortunately, the density of the InP etch features can be controlled by the temperature during atomic H cleaning.

Other dosing parameters produced different surface reconstructions. Figure 4.8a shows a mixed surface reconstruction obtained after a 10 minute atomic H dose at 440 °C. Conversely, after atomic H dosing at higher temperatures, 460-480 °C, the results obtained show a single surface reconstruction, Figure 4.8b. The surface reconstruction highly resembles that of the InGaAs(001)-(4×2) which is consistent STM of InP reported in literature [52]. Further studies on this surface are needed to ensure that at higher temperatures the InP layer is not fully etched and the remaining surface is the InGaAs channel.

Figure 4.9 shows STM images of an InP surface cleaned with atomic H for 5 minutes at 460-480 °C and dosed with TMA at room temperature followed by a 250 °C anneal. The InP surface after TMA exposure resembles that of the InGaAs surface after TMA exposure. The new ordered monolayer is perpendicular to that of the original InP rows, and has 8Å spacing between the horizontal rows. An inset in Figure 4.9 shows the horizontal ordered monolayer more clearly.

The primary difference in surface quality between InP and InGaAs is the terrace sizes. With the present processing condition, the InP has slightly smaller terrace sizes. Furthermore, the atomic H cleaned InP(100) surface lacks the dark horizontal defects and the bright vertical defects observed on the decapped InGaAs surface. Conversely, the InP surface has more bright island features indicated by the rectangle in Figure 4.8.

4.5 Summary

In summary, atomic hydrogen cleaning is able to restore the InGaAs(001)-(4×2) reconstruction after air exposure. With STM, the removal of the oxide layer and restoration of the clean InGaAs surface reconstruction is observed, allowing for a gate-last or replacement-gate process. STS of InGaAs shows the electrical quality of the hydrogen cleaned surface is similar to that of an As₂ decapped surface; more importantly, the STS is consistent with unpinning after air exposure, hydrogen cleaned and annealed surface followed by an organic metal molecule which also acts as an electrical passivation and nucleation layer for oxide ALD. The difference between room temperature annealing, allowing for a wide process window that must be optimized for etch rates compatible with the device structure. The key process, which is common to both room temperature anneal which reduces the step edge density and increases the terrace size. The process can easily be implemented with other hydrogen sources as long as the atomic hydrogen is free from high-energy ions and chemical contaminants.

Atomic H was also performed on a 2nm InP layer on top of the InGaAs channel. STM showed that variation of the temperature of the sample during atomic H cleaning had a strong effect on the surface reconstruction. After cleaning at high temperature, the surface behaved very similar to that of InGaAs for TMA exposure, creating a highly ordered monolayer

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W. Melitz, J. Shen, T. Kent, R. Droopad, P. Hurley and A.C. Kummel. "Atomic Imaging of Atomic H Cleaning of InGaAs and InP for ALD". *ECS Transactions* **35** (4), 175-189 (2010).



Figure 4.1: 100×100nm² filled state STM image of a) decapped surface, b) air exposed and annealed to 200°C surface, c) surface after 30 minutes air exposure followed by 30 minutes dose of hydrogen at 380°C, and d) after high temperature anneal to 460-480°C. The black rectangles show dark horizontal defect features, white rectangles indicate vertical bright defect features and red rectangles show dark surface features seen after hydrogen dosing which might be from surface etching.

95



Decapped surface

30min air exposure 30min H dose @380°C

460-480°C anneal

Figure 4.2: 500×500nm² filled state STM image of a) decapped surface, b) 30 minutes air exposure followed by 30 minutes dose of hydrogen at 380°C, and c) after high temperature anneal to 460-480°C. The terrace sizes improve with high temperature annealing. The hydrogen dosed surface shown in (b) has a large amount of dark surface features which are no longer present in (c). The inset in (b) indicates are large (black arrow) and small (white arrow) etching features caused by hydrogen exposure. The inset in (c) indicates a small terrace (black arrow) which is consistent with an incomplete terrace. The images are corrected for global tilt.

Table 4.1: Comparison of temperature and time of hydrogen dose of the densities of etch pits, incomplete terraces, and percent of the surface covered with etch either pits or incomplete terraces. The HT anneal is 460-480°C. The densities are calculated by counting the number of sites on a 500×500nm². The total percent coverage was calculate by taking the area of a large terrace and determining the percent of that area which is occupied by either the dark etch pits or the incomplete terraces. Every sample but the decapped sample was exposed to air prior to hydrogen cleaning. The values in table are of one sample but illustrate the trend between processing conditions. For the decapped sample there are features that resemble the etching features, however are not etching features, they are counted to give a comparison of hydrogen cleaned surfaces to that of the decapped surface.

Sample	Density of etch pits (/µm²)	Density of incomplete terraces (/µm ²)	Percent surface coverage of defects	Average size of etching feature (nm ²)
Decapped	20	20	6-7%	1500
30min 380°C dose, no HT anneal	50,000	60	28%	5.6
30min 380°C dose with HT anneal	1000	60	10%	100
5min 380°C dose with HT anneal	100	200	4%	130
30min 24°C dose with HT anneal	100	1000	14%	130
5min 24°C dose with HT anneal	800	40	16%	190



Figure 4.3: 500×500nm² filled state STM images of a) a typical decapped InGaAs(001) surface, with a surface step coverage (SSC) of 5.66%. For STM images b)-e) all samples after decapping then exposed to air for 30 minutes followed by hydrogen cleaning and annealing to 460-480°C. b) Shows a STM image of a sample dosed with hydrogen at a sample temperature of 380°C for 5 minutes with SSC= 7.65%. c) Is for 30 minutes at 380°C with SSC=13.9%. d) Sample is dosed with hydrogen at 24°C for 5 minutes with SSC=13.4%. e) Is for 30 minutes at 24°C with SSC=13.4%. e) Is for 30 minutes at 24°C with SSC=15.4%.



Figure 4.4: 40×40 nm² filled state STM images of surface after TMA dose at room temperature and annealed to 250°C. The inset shows an expanded view of 7×7 nm² indicated by black square. The surface shows high ordered horizontal row features (indicated by white arrow), consistent with a surface reconstruction.



30 min air exposure 30 min H dose @ -40 °C 460-480 °C anneal

30 min air exposure 200 °C anneal 30 min H dose @ -40 °C 460-480 °C anneal

Figure 4.5: 500×500nm² filled state STM image of InGaAs a) dose with atomic H for 30 minutes at -40 °C directly after exposure to air for 30 minutes. The images shows a high density of islands most likely unreduced oxide that was not full desorbed at low temperatures. b) STM image of a surface dose with atomic H at -40 °C for 30 minutes with a 200 °C anneal between air exposure and atomic H cleaning. The initial anneal before cleaning indicates the removal of water and other lower adsorbates can assist in the cleaning procedure.



Figure 4.6: Normalized $(dI/dV)/(\overline{I/V})$ spectra using variable-z STS of decapped InGaAs(001)-(4×2) (solid blue), 30 minutes air exposed and hydrogen cleaned for 30 minutes (dashed green) and room temperature dose of TMA followed by 250°C anneal (dot dash red) Spectra for n-type InGaAs with hydrogen cleaning at 24°C (a) and 380°C (b). Spectra for p-type InGaAs with hydrogen cleaning at 24°C (c) and 380°C (d). Δz for spectra ranges from 0.1-0.3nm/V. I/V is smoothed before $(dI/dV)/(\overline{I/V})$ is calculated [38]. The 0.4V shift in the VB side of the dot dash red curve for the n-type (a) and (b) and the absence of a shift in the p-type (c) and (d) indicates an unpinned surface Fermi level.



10 min H dose @ 380 °C

10 min H dose@380 °C + 470 °C anneal

Figure 4.7: 500×500nm² filled state STM image of InP a) after 10 minutes dose of atomic H at 380 °C, and b) after 10 minutes dose of atomic H at 380 °C plus a high temperature anneal to 470°C. The STM images show an InP after atomic H exposure generates a flat surface with the large etch features. The density of the etch features does not significantly decrease with high temperature annealing. The inset shows an example of one etch features present on an InP sample.





5 min H dose @ 460-480 °C

Figure 4.8: 100×100 m² filled state STM image of InP a) 10 minutes dose of atomic H at 440 °C, and b) 5 minute dose of atomic H at 460-480 °C. The STM images shows, at lower dosing temperatures, a mixed surface reconstruction is obtained as shown by the mixture of rows along the [110] and [11 0] directions. Conversely, for higher temperature atomic H cleaning, a single surface reconstruction is observed with rows directed only along the [110] direction. The surface reconstruction highly resembles that of the InGaAs(001)-(4×2) which is consistent STM of InP reported in literature [52]. The black box in (b) indicates bright defect features. These bright defect features reconstruction.



TMA dose at RT 250C anneal

Figure 4.9: 40×40 nm² filled state STM images of InP surface cleaned with atomic H for 5 minutes at 460-480 °C after TMA dosing at room temperature and annealing to 250 °C. The inset shows an expanded view of 25×25 nm² image. The ordered surface reconstruction appears the same as the TMA dose on InGaAs.

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Chapter 5

Tip Cleaning and Sample Design for High Resolution MOSCAP x-KPFM 5.1 Abstract

Kelvin probe force microscopy (KPFM) is a unique technique that can provide two-dimensional potential profiles inside a working device. A procedure is described to obtain high-resolution KPFM results on ultra-high vacuum (UHV) cleaved III-V MOSCAPs. Two tip preparation methods: field emission and Cr coating show reproducible high spatial and energy resolution KPFM images. A unique sample design has been developed which is compatible with UHV crosssectional KPFM (x-KPFM). Key design features are high density of devices on the cleave face, a buried device interface, and a cleavable gate contact. Using x-KPFM, the first UHV cleaved MOSCAP surface potential mapping is demonstrated.

5.2 Introduction

In order to effectively scale semiconductor devices, new techniques for device characterization are needed to image design operation on the nanoscale for both optimizations of device design and manufacturing. Kelvin probe force microscopy (KPFM) measures the two-dimensional potential profile of a surface [1]. KPFM can be used to probe passive and active devices, doping profiles [2], heterostructures [3; 4], diodes [5; 6], solar cells [7-9], etc. Cross-sectional KPFM (x-KPFM) in air of operational MESFETs [10; 11] has been preformed. However, x-KPFM in ultra high vacuum (UHV) likely provides a more accurate image of the

true potential inside working devices because it avoids surface oxidization and chemisorption that may influence the surface potential. The key requirements for x-KPFM as a practical method for probing nanoscale devices are (1) high spatial resolution, (2) high energy resolution, (3) samples compatible with external biasing and (4) samples designed to give flat cleaves in UHV. In the present paper, two tip preparation methods to achieve high spatial and energy resolution are reported. Energy resolution of better than 15 meV and spatial resolution better than 5 nm is demonstrated at a step edge of the InAs(110) surface with a potential peak induced by dangling bonds similar to that of GaAs(110) and GaP(110) [12]. In addition, an example design for MOSCAP samples compatible with UHV x-KPFM, external biasing and flat cleaving is demonstrated.

5.3 Experimental Technique

All experiments are performed in an Omicron VT-AFM/STM chamber with a base pressure 1-3 x 10⁻¹¹ Torr and an attached preparation chamber with a base pressure 1-3 x 10⁻¹⁰ Torr. For KPFM, a conductive atomic force microscopy (AFM) cantilever is used. A bias is applied to the tip to minimize the electrostatic force between the surface and the tip caused by the contact potential difference (CPD). Conductive cantilevers are commercially available; however, these cantilevers are not atomically sharp (nominally tip radius ~15nm) because several layer of metal are usually coated over the silicon based cantilever. One of the simplest but less consistent ways of forming sharp tips is by gently crashing a silicon cantilever with a native insulating oxide into a sample surface to remove the native oxide while maintaining tip sharpness [13; 14]. With field emission cleaning, it is possible to resharpen the apex after it has become dulled unless the cantilever has been damaged. Physical vapor deposition (PVD) is employed to deposit a few nanometers of metal onto sharp silicon cantilever to fabricate high-resolution KPFM cantilevers [15; 16], but this method requires calibration experiments and high quality coating equipment. Both the tip cracking and the nanoscale metal coating methods are employed in the current study.

The first tip preparation method is tip cracking of the native oxide on silicon tips via field emission. Tip cracking is performed on the same commercially available highly doped silicon cantilevers from NANOSENSORs. In order to perform tip cracking in UHV, the tip holder is modified so that the silicon cantilever is grounded while in the tip carrier. The cantilever is first degassed for several hours at 150 °C in UHV. Afterwards, a tungsten filament is positioned close to the apex of the cantilever and with a high voltage (2 - 4 kV) is applied until a pressure burst and 5-20 μ A of emission current are measured. The emission current is maintained for several seconds to allow for ample cleaning. After field emission the cantilever has adequate conduction and sharpness needed for high resolution KPFM.

The second, tip preparation method is coating of a silicon cantilever with an e-beam evaporator Cr. A SSS-NCHR cantilever from NANOSENSORs (having nominal tip radius less than 2nm) is coated with 3 to 5 nm of Cr. The coating extends from the apex to the contact for the applied bias. After coating, the tip is transferred to the UHV chamber and degassed for several hours at 150 °C in UHV. With the Cr coated cantilevers, topography and potential changes at the step edges on InAs(110) can be imaged simultaneously as seen in Figure 5.1. Figure 5.1c shows the topographic line profile of the step edge having height difference of 2Å which is very close to theoretical value, and the surface potential line profile shows a ~150 mV CPD increase at the step edge. The CPD increase at the step edge can be attributed to dangling bonds at the step edge; the CPD increase at step edges has also been observed in GaAs(110) and GaP(110) surfaces[12]. These results show that high spatial resolution, less than 5 nm, and high energy resolution, about 15 mV, have been achieved. Tips cleaned with field emission show similar resolution to the tips coated with Cr. Both of these tip preparation methods provide adequate spatial and energy resolution required for performing x-KPFM on scaled MOSCAPs.

While the first requirement for high resolution KPFM is a sharp tip, the second requirement is a flat surface. In KPFM, the topology and CPD signals are independently measured insuring that under ideal conditions there is no influence on the measured CPD from the topology. However, scanning parameters (loop gain, frequency set point, and scanning speeds) need to be adjusted to compensate for the large topographical features thereby reducing the sensitivity of the CPD signal. Furthermore, large topographical features frequently damage the apex of the tip reducing the spatial resolution. In order to perform x-KPFM on an operational nanoscale MOSCAPs, a MOSCAPs design is needed which is both compatible with external biasing in UHV KPFM and which can be cleaved to provide flat surfaces.

The MOSCAP gate stack design used is illustrated in Figure 5.2a. The gate stack is $SiO_2/100 \text{ nm n}^{++}$ GaAs/32 nm GGO/*n*-type GaAs. The 100nm n⁺⁺ GaAs layer acts as the gate material for the MOSCAP structure. Degenerately doped n⁺⁺ GaAs is chosen for the gate because it cleaves flat, allowing the gate to be included in the CPD image, and it provides ample conduction to minimize contact resistances. The SiO₂, GaAs, and GGO layers are blanket deposited. The SiO₂ is patterned allowing for a large 2 mm x 2 mm contact pads to be made through the to the n⁺⁺ GaAs gate electrodes, Figure 5.2b. A back side contact is made to the semiconductor substrate. The SiO₂ layer is critical for two reasons: (a) the sample edge tends to have a rough cleave and (b) KPFM scanning at the edge of the sample is extremely abusive to the cantilever thereby reducing the resolution. The SiO₂ layer acts as a spacer between the edge of the sample and edge of the device, thereby, avoiding both edge roughness at the device and KPFM scanning at the edge of the sample.

For *in situ* cleaving for x-KPFM of MOSCAPs, the mechanical stability of the contacts and precisely controlling the location of the cleave face are critical. The sample is clamped into the sample holder making a stable contact to the backside contact and the frontside gate contact pad, Figure 5.2c. Prior to introducing the sample to UHV, a nick is scribed on the top face of the sample to control the location of the cleave face. The sample is placed in UHV and degassed at 150 °C for several hours, and then cleaved at a temperature between -100 °C and 20 °C.

5.4 Results and Discussion

A topology image from KPFM on the n^{++} GaAs/GGO/GaAs MOSCAP sample is shown in Figure 5.2d (corresponding to the CPD image for 0 V gate bias Figure 5.2e) at the MOS interface. A Cr coated SSS-NCHR cantilever is used for the cross-sectional KPFM. The contour lines in Figure 5.2d occur at increments of 10 nm. The topology image shows that the n^{++} GaAs gate cleaves flat, allowing for the gate layer to be imaged with high resolution. Most of the topographical features are located in the SiO₂ layer showing that the insulating cap layer properly protects the MOS interface from cleaving damage. In the area of the MOS interface less than 10nm of topographical change occurs in the ydirection. The 30nm change along the x-direction is caused by the sample being slightly tilted in the sample holder, but this tilt does not significantly influence the scanning parameters required to achieve high resolution.

The very high-resolution two-dimensional CPD image in Figure 5.2e of the 0V gate bias CPD map shows a depletion distance of 130nm, which is consistent with a lightly doped substrate. The high-resolution image also shows that the charge in the oxide is uniformly distributed. The potential changes in the semiconductor are expected to be confined to the depletion region directly under the oxide, so very little potential change should occur in the bulk substrate. The measured CPD shows a slight but negligible potential change in the substrate most likely caused by substrate resistance.

Several checks were performed to confirm the high-resolution image in Figure 5.2e is an accurate representation of the charge in the gate oxide and the

depletion region. An external bias was applied to the gate with respect to the substrate shown in Figure 5.3. Figure 5.3a shows 1000nm line traces at -1, 0 and +1V gate bias of n⁺⁺ GaAs gate MOSCAP. The CPD of the n⁺⁺ GaAs gate follows the applied bias, indicating ohmic contact between the metal contact pads and the n^{++} GaAs gate. High-resolution x-KPFM line traces in Figure 5.3a show that the potential changes in the semiconductor channel are consistent with the depletion widths and barrier heights changing over the range of gate biases. The CPD profiles in Figure 5.3a clearly show the typical electrical defects in the oxide. At 0V gate bias, the oxide has a positive bias with respect to the gate due to fixed charge. Full two-dimensional potential profiles of the planar MOSCAP structures can be seen in Figure 5.3b. The contour lines in Figure 5.3b occur at increments of 100 mV. The $CPD = \phi_{sample} - \phi_{tip} + V_{external}$, where ϕ_{tip} is the work function of the tip, ϕ_{sample} is the work function of the sample, and $V_{external}$ is the potential change caused by the external bias. The two-dimensional potential profiles in Figure 5.3b also show a high density of contour lines at the n⁺⁺ GaAs/GGO/GaAs interface, signifying that the potential drop is occurring over the oxide and/or the semiconductor channel.

The CPD profile, Figure 5.3a, of the MOS interface corresponds to the expected work function offsets of n^{++} GaAs and *n*-type GaAs(110) surface. The cleaved GaAs(110) surface is known to be unpinned [17; 18]. The work function of *n*-type GaAs should be larger than the work function of n^{++} GaAs, which

means the substrate should have a lower CPD value. The CPD of n⁺⁺ GaAs is 0.18V larger than the substrate.

5.5 Summary

Two tip cleaning methods have been demonstrated showing high spatial and energy resolution for KPFM. High spatial resolution is critical for KPFM to be able to image potential profiles in scaled devices. A MOSCAP sample design for UHV x-KPFM was demonstrated. An insulating cap and a cleavable gate are incorporated into the MOSCAP design to improve the cleave face inside the MOSCAP thereby maintaining high KPFM resolution and low damage to the KPFM tip apex. The insulating cap embeds the devices thereby removing the active MOSCAP device from the edge of the sample. By using an n⁺⁺ GaAs gate, the gate can also be included in the two-dimensional potential profile. The first operation UHV cleaved MOSCAP device imaged with KPFM is demonstrated, illustrating the potential changes from the external bias on the gate and semiconductor substrate. This work is a promising step toward further x-KPFM study of working MOSFETs device.
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The dissertation author is the primary investigator and author of these papers:

W. Melitz, J. Shen, T. Kent, R. Droopad and A.C. Kummel, "InGaAs surface preparation for ALD by hydrogen cleaning and improvement with high temperature anneal." *Journal of Applied Physics* **110**, 013713 (2011).

W. Melitz, J. Shen, T. Kent, R. Droopad, P. Hurley and A.C. Kummel. "Atomic Imaging of Atomic H Cleaning of InGaAs and InP for ALD". *ECS Transactions* **35** (4), 175-189 (2010).



0 10 20 30 40 50^{1.3} Figure 5.1: 100 nm x 100 nm (a) topology and (b) CPD of UHV cleaved InAs(110). (c) Line profiles indicated by the white line in (a) and (b) showing the topography and the potential spike at the step edge.



Figure 5.2: (a) Cross-sectional view of MOSCAP gate stack. (b) Top down view of a single sample die. Dashed line indicates location of nick on surface prior to entering UHV. (c) Schematic of the sample holder and external contacts. (d) 1000 nm ×1000 nm topology image of UHV cleaved GaAs MOSCAP corresponding to the 0 V gate bias CPD image. Contour lines occur at 10 nm increments. (e) 1000×1000nm high resolution CPD image at 0 V gate bias. Contour lines occur at 100 mV increments.



Figure 5.3: (a) 1000 nm line traces of n^{++} GaAs/GGO/ *n*-type GaAs MOSCAP at - 1, 0, and +1V external gate bias. (b) 1000 nm ×1000 nm CPD images at -1V, (c) 0 V and (d) +1 V gate bias. Contour lines occur at 100 mV increments.

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