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Compact Models for Future Generation CMOS

By

Darsen Duane Lu

A dissertation submitted in partial satisfaction of the
requirements for the degree of
Doctor of Philosophy

in

Engineering — Electrical Engineeing and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Chenming Hu, Chair
Professor Ali M. Niknejad
Professor Sourav Chatterjee

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Darsen Duane Lu

Abstract

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University of California, Berkeley

Professor Chenming Hu, Chair

Multiple-gate MOSFETs with superior short channel control are expected to replace planar CMOS in the near future. An accurate and computationally efficient compact transistor model is necessary to simulate circuits in multiple-gate MOSFET technologies. In this dissertation research, a compact multiple-gate MOSFET model, BSIM-MG is developed. BSIM-MG includes independent multi-gate compact model BSIM-IMG and common multi-gate compact model BSIM-CMG. We focus on BSIM-IMG for multiple-gate MOSFETs with independent front- and back-gates. The basic formulations for surface potential, drain current and charge are derived and verified against TCAD simulations with excellent agreements. The model preserves important property of multi-gate MOSFETs such as volume inversion. Non-ideal effects including short channel effects, length dependent back-gate coupling, transport models, leakage currents, parasitic resistances and capacitances, temperature effects and self heating are considered in the model. The model expressions are carefully formulated so that the symmetry of the source and drain is preserved. Rules for maintaining symmetry are discussed in this dissertation.

For the common multi-gate transistor model BSIM-CMG, the basic expressions have been improved so that it is compatible with a novel non quasi-static effects modeling technique — charge segmentation. In addition, a parasitic source/drain resistance model is developed, including three components: the contact resistance, the spreading resistance, and the bias-dependent extension resistance. Both BSIM-CMG and BSIM-IMG models are verified against TCAD and measured data.

The use of the FinFET compact model to model manufacturing variation in a FinFET technology is further explored. The model matches measured data well for both the nominal case and the statistical distribution for NMOS threshold voltage as well as the read static noise margin. A non-Gaussian threshold voltage distribution is observed for nFET devices, and the compact model successfully captures the distribution. We further outlined and demonstrated a Monte-Carlo based procedure for designing FinFET SRAM cells using the extracted variation information.

Technology scaling has enabled numerous CMOS analog circuits for low cost radio-frequency applications. The modeling of MOSFET thermal noise becomes very important. In the final part of this dissertation research, a new thermal noise model is developed for the industry standard BSIM4 model that enhances the existing thermal noise formulation in BSIM4. The model is verified against a segmented channel MOSFET model as well as measured data. It is implemented in Berkeley SPICE3 and is ready for industry use. A method to port the model to BSIM-MG for thermal noise modeling in multi-gate MOSFETs is also presented.

Dedicated to my family

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Chapter 1

Introduction

1.1 CMOS Scaling and its Challenges

Over the past several decades, the size reduction of CMOS circuits has fueled the growth of the microelectronics industry. The manufacturing cost of integrated circuits has decreased exponentially, making countless new applications available to the general public. In the past CMOS technology advances relied on the improving manufacturing capabilities. The minimum manufacturable line width has decreased year by year. Surprisingly, the basic structure of the MOSFET has not changed much.

Simple scaling has become more and more challenging due to fundamental device-physics reasons [1]. At the device gate length (L) less than 100nm, further reduction in L has yielded limited improvements in performance due to velocity saturation [2] and source velocity limit [3]. For this reason, the strained silicon technology has been put into production [4]. The scaling of gate dielectric also poses a challenge. As the physical thickness of the SiO_2 gate dielectric (T_{ox}) is scaled beyond 1.2nm, quantum mechanical tunneling current from the gate into the channel becomes significant [5]. Further reduction in T_{ox} will result in large static leakage current and large power consumption even when the device is turned off. Therefore at around the 45nm node, high-K gate dielectric is used to scale down the effective oxide thickness (EOT) without increasing the gate tunneling current. Metal gate electrodes are also used to eliminate the unwanted poly-silicon gate depletion effect [6]. Even with these advances, there is little room left for EOT scaling. This means the gate control of the channel can not be made much stronger, therefore channel length can not be made much shorter lest the drain exerts a proportionately large control leading to excessive short-channel effects and high off-state transistor leakage. A new approach is needed to allow future reduction of channel length. The multi-gate structure is a promising approach [7].

1.2 Multi-gate MOSFET — the Future CMOS Transistor Structure

1.2.1 Advantages of Multi-gate MOSFETs

The main advantage of the multi-gate devices is the improved short channel effects. Since the channel (body) is controlled electrostatically by the gate from multiple sides, the channel is better-controlled by the gate than in the conventional transistor structure. Unwanted leakage components are reduced and a small transistor can be used to continue the cost reduction through miniaturization. Improved gate control also provide lower output conductance, i.e., smaller $\frac{dI_{ds}}{dV_{ds}}$ in the current saturation region. This provides greater voltage gain, which is beneficial to analog circuits as well as to the noise tolerance of digital circuits.

A second advantage of the multi-gate devices is the improved on-state drive current (I_{on}) and therefore faster circuit speed. I_{on} improvement arises from several reasons [8]. Reduction of channel doping reduces impurity coulombic scattering. Reduced channel doping reduces the electric field normal to the SiO_2 interface and therefore reduces the surface roughness scattering. Finally, a promising multi-gate structure, FinFET, provides a larger channel width with a small footprint area. This raises I_{on}, which is handy for driving a large capacitive load such as long interconnect.

A third advantage is the reduced manufacturing variation. In the absence of channel dopants, the effect of random dopant fluctuation (RDF) is minimized. Lower SRAM supply voltage for the FinFET multi-gate technology compared to traditional bulk MOSFET technology has been experimentally demonstrated [9].

The advantages of multi-gate devices is well known and demonstrated in many FinFET technologies [10, 11, 12, 13].

1.2.2 Various Flavors of Multi-gate MOSFET

There are different flavors of multi-gate MOSFETs. Several examples are shown in Fig. 1.1.

Perhaps the best known example is the FinFET [14]. The FinFET consists of a thin silicon body (the fin) and a gate wrapping around its top and two sides. The ITRS [15] considers it the candidate to replace planar MOSFETs for the aforementioned benefits of multi-gate transistor and because a FinFET is relatively easy to fabricate. FinFETs can be made on either bulk or SOI substrates, creating the bulk FinFET (Fig. 1.1(a)) or the SOI FinFETs (Fig. 1.1(b)). In some FinFET processes the oxide hard mask on top of the fin is not removed, creating the double-gate FinFET (Fig. 1.1(c)). In double-gate FinFETs the top surface of the fin does not conduct current, whereas in triple-gate FinFETs (Figs. 1.1(a)(b)) the side surfaces and the top surface all conduct current.

Another example of multi-gate MOSFET is the all-around gate device (Fig. 1.1(d)). It consists of a pillar-like body surrounded by the gate dielectric and the gate. The nanowire

MOSFET [16] is one example of all-around gate devices. Depending on the fabrication process, the channel may be either vertically [17] or horizontally [16] oriented.

Optionally, a FinFET can have two separated gates that are independently biased. This can be achieved by removing the top portion of the gate of a regular FinFET using chemical mechanical polishing, forming the independent double-gate FinFET (Fig. 1.1(e)) [18].

Independent double-gate MOSFETs may also be made as a planar device [19]. The planar double-gate SOI (Fig. 1.1(f)) is essentially a planar SOI MOSFET with a thin buried oxide (labeled as BOX). A heavily-doped region in silicon under the buried oxide acts as the back-gate. Unlike the front-gate, the back-gate is primarily used for tuning the device V_{th}. The buried oxide is usually thick such that the back-gate cannot induce an inversion layer at the back surface. V_{th} tuning can be used to compensate for variability in IC manufacturing from chip to chip or even circuit to circuit within the same chip. Doing so improves the IC speed and power consumption. It can also be used to dynamically raise or lower V_{th} circuit by circuit within a chip in response to the need for less leakage or more speed. This is a very effective means of managing power consumption.

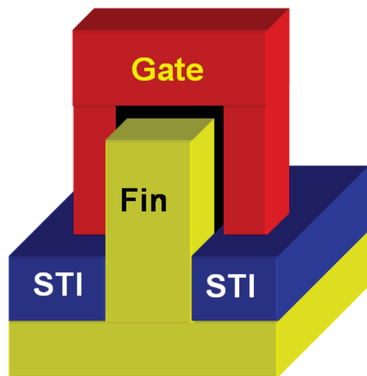
1.3 Multi-gate CMOS Modeling

1.3.1 BSIM-MG: A BSIM-family Model for Multi-gate MOSFET

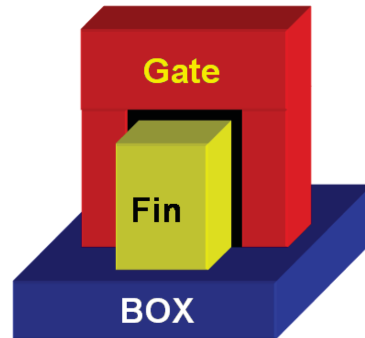
Given the advantages of multi-gate MOSFETs, it is likely that they will be used in future CMOS technologies. A production-worthy multi-gate compact model (SPICE model) which allows efficient circuit design is needed.

The BSIM (Berkeley Short-channel IGFET Model) series compact models have served the industry for 20 years [20, 21, 22]. BSIM3 and BSIM4 industry standard models have been widely used for the simulation of planar bulk MOSFETs. As technology advances, new compact models are developed to support new device architectures and incorporate new device physics. BSIMSOI [23, 24] was developed to model partially-depleted, fully-depleted and dynamically-depleted SOI devices. In this dissertation research, BSIM-MG [25] [26] is developed for circuit simulation of multi-gate MOSFETs.

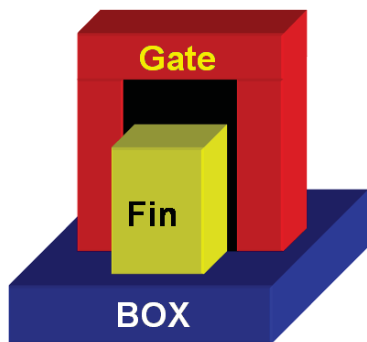
The difference between BSIM-MG and other BSIM models lies not only in the difference in device structure, but also in the modeling technique it has used. In particular, source-drain symmetry [27] is maintained for BSIM-MG. Therefore unlike BSIM3 and BSIM4, the second derivative of the drain current and charge are continuous across $V_{ds} = 0$. This is a result of careful mathematical derivation and thorough testing to ensure the modeling or each physical effect in the compact model does not violate source/drain symmetry. During the course of developing BSIM-MG, we have learned several rules which ensures MOSFET symmetry is not broken. These rules will be discussed in this thesis.



(a) Triple-gate FinFET on Bulk Si

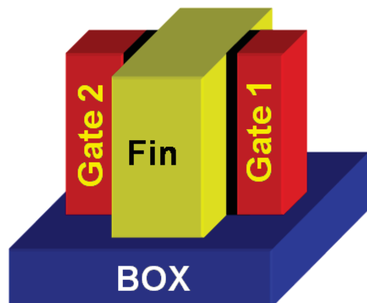


(b) Triple-gate FinFET on SOI



(c) Double-gate FinFET on SOI

(d) All-around Gate



(e) Independent Double-gate FinFET on SOI

(f) Planar Double-gate SOI

Figure 1.1: Illustration of various flavors of multi-gate FETs. (SOI: silicon-on-insulator layer; BOX: buried oxide)

1.3.2 BSIM-IMG and BSIM-CMG

It is likely that more than one flavor of multi-gate MOSFETs will be used in production for different purposes. Therefore the compact model should ideally cover as many of these flavors as possible. We have classified multi-gate MOSFETs into two main categories: independent multi-gate (IMG) and common multi-gate (CMG) MOSFETs.

IMG refers to independent double-gate MOSFETs with two separate gates. The front- and back-gate stacks are allowed to have different gate workfunctions, biases, dielectric thicknesses and materials. Independent-gate FinFET (Fig. 1.1(e)) and the planar double-gate SOI (Fig. 1.1(f)) belong to this category.

CMG refers to a special case where the gates are "on and the same." The gate stacks of CMG MOSFETs have identical gate workfunction, bias and dielectric thickness and material. Regular FinFETs and all-around gate MOSFETs (Figs. 1.1(a)-(d)) fall into to this category.

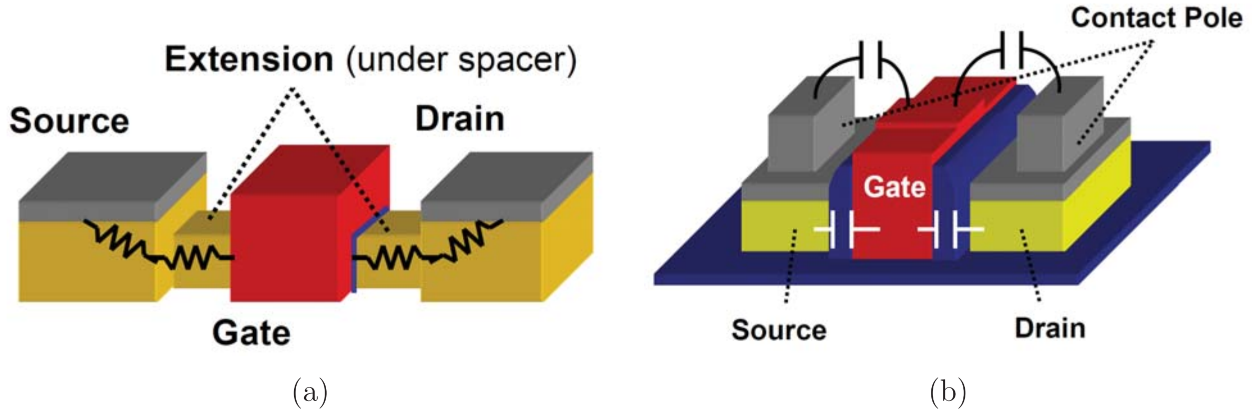
Two separate compact models BSIM-IMG and BSIM-CMG are developed for IMG and CMG devices, respectively.

1.4 Modeling Parasitic Resistances and Capacitances in the FinFET Multi-Gate Device

Despite the advantages of multi-gate structures, there are a few challenges. From a device point of view, one of the challenges is the larger parasitic resistances and capacitances in the three-dimensional structure.

Take the FinFET multi-gate structure for example, a thin fin must be used for good short channel control. This results in a larger parasitic source/drain series resistance (R_{ds}) due to the small cross sectional area of the fin extension (Fig. 1.2(a)). In order to minimize R_{ds}, a raised source/drain structure is often used [28]. The raised source/drain is often formed by a selective epitaxial growth process, which creates a non-rectangular raised source/drain cross section. Modeling of this three dimensional structure becomes very different from bulk MOSFETs. Therefore in this dissertation we investigated in the modeling of parasitic source/drain resistances in FinFETs.

Another important parasitic component is the outer fringe capacitances (Fig. 1.2(b)), which is made larger after enlarging the source and drain with a raised source/drain structure. The modeling of capacitances are becomes difficult in the three-dimensional FinFET compared with planar MOSFETs. We will briefly discuss about the modeling of parasitics capacitances as well.



(a) (b)

Figure 1.2: (a) Illustration of source/drain series resistance in the FinFET structure (b) parasitic fringe capacitances

1.5 Variation in FinFET SRAM Cells

One important roadblock for transistor size reduction is the random fluctuation of the number of dopant atoms in the MOSFET channel, called random dopant fluctuation (RDF) effect, which increases the variation in device threshold voltage (V_{th}) [1] [29]. Since the standard deviation of V_{th} due to RDF is inversely proportional to $\sqrt{WL}$, circuits with small device dimensions such as the SRAM cell is especially susceptible to RDF.

RDF is a fundamental source of variation, which can not be eliminated as long as the channel is highly doped. Perhaps the only way to fight RDF is to reduce the channel doping. This is not possible for conventional bulk MOSFETs since heavy doping is required to control the short channel effects and subthreshold leakage. However, ultra thin-body (UTB) devices such as silicon-on-insulator (UTBSOI) MOSFETs [30] and especially UTB multi-gate devices like the FinFET [14] have much better short-channel behavior. In fact reducing the body thickness presents a new scaling path to allow future device size reduction in addition or in lieu of the past dependence on EOT reduction and channel doping escalation.

In the absence of doping in multi-gate devices, RDF is reduced. Perhaps the largest impact of this is on SRAM cells, since it typically has much smaller width compared to digital logic circuits and much larger variation. FinFET presents an excellent opportunity to reduce the variation of SRAM, enabling lower supply voltages and lower power consumption.

However, this is not to say that the variation in FinFET is unimportant. Line edge roughness [31] is expected to dominate FinFET variation through short channel effects. Therefore, unlike planar bulk MOSFETs, the resulting V_{th} distribution, for example, may be non-Gaussian, and is more difficult to model.

Simulation study that focuses on FinFET SRAM variation is often carried out using TCAD tools [32]. However, when a large number of simulation is needed, TCAD tools may

not be fast enough, and a compact model may be necessary.

In this dissertation, we will discuss about a simulation study that we have carried out using BSIM-MG. We extracted parameters for the BSIM-MG model using stand alone FinFET drain current data. Subsequently variation sources are added to the BSIM-MG model. A Monte Carlo simulation script is constructed in order to translate physical parameter variation to the distribution of electrical characteristics such as threshold voltage, read/write static noise margin, and power consumption. We adjusted the standard deviation of physical parameter variation so that the simulated electrical characteristic distribution matches measurement distribution. We then use the calibrated statistical model to re-design the SRAM, and analyze the sensitivity of variation to various design parameters.

One interesting result we have found is the non-Gaussian distribution of V_{th} in SRAM transistors. This could be the result of a non-linear mapping of physical dimensions of the FinFET to V_{th}. BSIM-MG is able to account for this because it models the dependence of V_{th} on the gate length and fin thickness well.

1.6 Thermal Noise Modeling for Planar and Multi-gate Transistors

Scaling is important for digital circuits for lower cost, enhanced performance and lower power per function. Thus multi-gate MOSFETs was introduced. Scaling is also important for analog circuits for high frequency applications of CMOS. With the advance of technology, recently a 60GHz transceiver has been demonstrated in 90nm CMOS [33].

In CMOS wireless/RF applications, the modeling of thermal noise is particularly important. In an RF receiver, a low noise amplifier (LNA) boosts the incoming wireless signal to prevent further degradation of the signal-to-noise ratio. One of the main factor that determines the noise performance of an LNA is the channel thermal noise of the amplifying MOSFETs. Therefore accurate modeling of thermal noise is required.

We have enhanced the industry standard BSIM4 [22] with a new thermal noise model. This model accurately accounts for the drain thermal noise, induced gate thermal noise, as well as the correlation between the two. It is implemented in Berkeley SPICE3 and released for industry use.

For the future multi-gate MOSFETs, very little thermal noise data is available. Nevertheless, we believe the physics remains similar to planar MOSFETs and the same thermal noise model can be easily adopted for multi-gate MOSFETs as well.

1.7 Dissertation Goals and Outline

The goal of this dissertation research is to develop compact models for nanoscale CMOS technology, with particular emphasis on multi-gate MOSFET compact models.

Chapter 2 focuses on the derivation of the core model for multi-gate MOSFETs with independent front- and back-gates, BSIM-IMG. This includes the calculation of surface potential and the derivation of the basic drain current and terminal charge formulations. The model is verified with TCAD tools. We also briefly describe the enhancements to the BSIM-CMG drain current model. For a complete description of the core model of BSIM-CMG, the readers may refer to [34].

Chapter 3 summarizes the techniques we have used to maintain model symmetry in BSIM-MG. We present five basic rules for formulating equations to ensure symmetry, and several examples for the rules.

Chapter 4 describes a parasitic source/drain resistance model for the FinFET multi-gate structure, including the bias-dependent extension resistance, the spreading resistance, and a transmission line based contact resistance component. The model is verified against three dimensional numerical simulation.

In chapter 5, we applied the BSIM-MG model to study the modeling of manufacturing variation of FinFET SRAM cells. A Monte Carlo simulation framework that simultaneously accounts for both global and local variation is developed. The model is calibrated to measured FinFET threshold voltage and static noise margin distributions.

Finally, chapter 6 describes a new thermal noise model that is derived for the industry standard BSIM4. The model is verified against segmented channel transistor, as well as measured thermal noise data.

An overall summary of this dissertation is presented in Chapter 7. Chapter 7 highlights the key research contributions and future research directions are suggested.

Chapter 2

Basic Formulations of Multiple-Gate MOSFET Compact Models

2.1 Core Models of BSIM-CMG and BSIM-IMG

As we mentioned in chapter 1, the common multi-gate (CMG) and independent multi-gate (IMG) MOSFETs are modeled separately due to the different device structure and operation. The models are named BSIM-CMG and BSIM-IMG, respectively. The difference in device structures leads to different boundary conditions for the Poisson's equation. Therefore BSIM-CMG and BSIM-IMG have very different core models[1].

First of all, BSIM-CMG has one less terminal compared to BSIM-IMG because all the gates are tied together. A reduced number of nodes means faster SPICE simulation. Therfore, for computational efficiency reasons the two devices should use two different models.

In addition, the core model for BSIM-CMG is somewhat simpler than that of BSIM-IMG. For both models, the values of surface potential need to be computed by finding the root of the non-linear input voltages equation (IVE) that relates the surface potential to terminal voltages. For BSIM-CMG the IVE has only one unknown. Good convergence is achieved through either Newton Raphson iteration or non-iterative analytical approximations [25]. On the other hand, the IVE of BSIM-IMG contains two equations and two unknowns. A special treatment is needed for surface potential computation in BSIM-IMG, making the model more complex than BSIM-CMG.

Furthermore, BSIM-CMG models common multi-gate MOSFETs, in which channel doping is likely needed to achieve multiple V_{th}. Therefore channel doping is included as part of the core model for BSIM-CMG. On the other hand, BSIM-IMG models independent-gate devices, which has a back-gate terminal that can be used to achieve multiple V_{th}. Therefore the channel is likely lightly doped. In BSIM-IMG, a lightly-doped channel is assumed for

[1] The core model includes the calculation of surface potential, and the basic drain current and terminal charge formulations

core model derivation. This simplifies the mathematics and improves computational efficiency. For IMG devices with a lightly doped body, a bias-independent V_{th} correction term is sufficient to model doping.

Although the core model are different, they have very similar real device effect models. These include mobility degradation, velocity saturation, gate tunneling current, channel length modulation, gate induced drain leakage current, and many others. Some of the equations are conveniently taken from bulk transistor models such as BSIM4, since the physics are the same.

In this dissertation, we will focus on the core model of BSIM-IMG, as a treatment on the BSIM-CMG core model is already available in [34]. For BSIM-CMG, an improvement to the core I-V model is presented in the end of this chapter.

2.2 Modeling Double-gate Fully-depleted SOI MOSFETs with BSIM-IMG

The fully-depleted SOI (FDSOI) MOSFET is a promising CMOS replacement. It has the advantage of superior control of short channel effects when the body is very thin because unwanted leakage paths through the buried channel are eliminated.

However, the field originating from the drain can still be coupled to the channel through the buried oxide (BOX) [35]. To prevent this the buried oxide thickness must be scaled as well [36]. The silicon beneath the buried oxide is heavily doped to act as a back-gate that shield the field from the drain. An addition advantage for a back-gated design is that it allows dynamic threshold voltage (V_{th}) control. By selectively raising V_{th} in idle circuit blocks by back-gate biasing, static leakage current can be significantly reduced without hurting the active-state performance [19]. Furthermore, multiple V_{th} flavors in the same circuit can be achieved with back-gate biasing instead of channel doping, which causes larger variation, or multiple work function gates, which significantly increases process complexity. Therefore from a device point of view, an ideal FDSOI has a thin BOX.

BSIM-IMG models FDSOI devices with a thin BOX. With a heavily doped layer beneath the BOX acting as a second gate, the thin BOX FDSOI MOSFET is essentially an independent double-gate MOSFET. In fact we have developed BSIM-IMG with this target device in mind.

Several compact models for independent double-gate MOSFETs are available in the literature [37, 38, 39, 40, 41, 42, 43, 44]. Pei et al. [37] and Reyboz et al. [38] model the current and charge of independent DG MOSFETs with explicit expressions. Both models show good agreements with TCAD simulations. However, the formulations used in the models are known to violate source-drain symmetry — an important requirement for certain analog applications [45]. Other independent DG models do not have this symmetry issue [39, 40, 41, 42, 43, 44]. However, they are surface potential based and the surface potential

is described in implicit forms. Iterative techniques such as Newton Raphson are required inside the model, which from our experience significantly degrades computational efficiency [46].

Recently, explicit approximations of surface potential have been developed for planar bulk MOSFETs [47] and symmetric (common) double-gate MOSFETs [25, 48] and are robust and computationally efficient. In this work, we developed such explicit approximation for independent DG MOSFETs. The computational efficiency of the new approximation are proven by measuring the runtime of the compiled and optimized version of the approximation. In addition, drain current and terminal charge expressions are derived. The results are verified by comparing it with TCAD [49] simulations without the use of fitting parameters.

Non-ideal effects such as short channel and quantum effects, field dependent mobility, leakage currents and device parasitics are added to model real devices. The Gummel Symmetry Test [27, 45] is performed to verify the symmetry of drain current and charge with respect to $V_{ds} = 0$. The full model including non-ideal effects is implemented in Verilog-A [50]. Good convergence is demonstrated through transient simulation of a large coupled ring oscillator circuit.

2.3 Core Model of BSIM-IMG

2.3.1 Modeling Framework

The basic model formulation for the independent double-gate FDSOI MOSFET is developed based on the 2-dimensional schematic cross section shown in Fig. 2.1. This view corresponds to a horizontal cross section of the independent-gate FinFET (Fig. 1.1(e)) or a vertical cross section along the length direction of the planar double-gate SOI MOSFET (Fig. 1.1(f)). A silicon channel with thickness T_{si} is sandwiched between the front- and back-gate stacks. The two gate stacks are allowed to have different work functions (Φ_{g1}, Φ_{g2}), materials (metal or heavily doped semiconductor), dielectric thicknesses (T_{ox1}, T_{ox2}), and dielectric constants (ϵ_{ox1}, ϵ_{ox2}). The energy band diagram of this system at the flat-band condition is shown in Fig. 2.2. Without loss of generality, we focus on an n-type device throughout this chapter.

The silicon body is assumed to be lightly-doped and fully-depleted. Back-gated FDSOI MOSFETs will likely have a lightly-doped body to minimize random fluctuation effects [29] and to increase mobility. In addition, with a thin body, heavy doping is not needed for controlling short channel effects. V_{th} is set by back-gate biasing or work function adjustment instead of channel doping.

2.3.2 Explicit Approximation for Surface Potential

In this section, we develop a method to approximately solve the Poissons equation and obtain explicit analytical expressions for the surface potentials and the inversion carrier density per

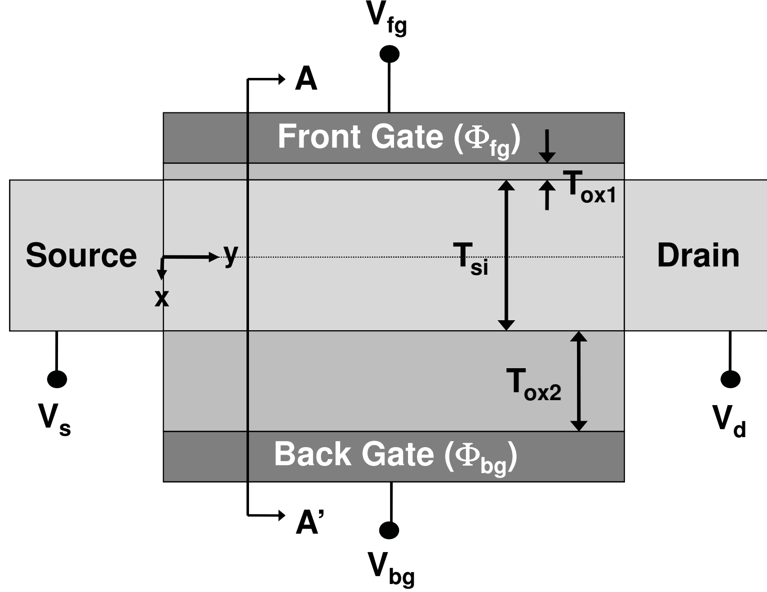


Figure 2.1: Basic framework for modeling independent double-gate MOSFETs.

area (Q_{inv}). The results are verified with TCAD simulations. Since there is no neutral body for fully-depleted devices, it is convenient to choose the quasi-Fermi level at the source as a reference for the potential (ψ). In this dissertation we define ψ in the silicon body as follows:

$$\psi = -\frac{E_c - E_f(source)}{q} \tag{2.1}$$

where E_c is the conduction band energy and $E_f(source)$ is the quasi Fermi level at the source. The surface potentials, $\psi_{s1} = \psi|_{x=-Tsi/2}$ and $\psi_{s2} = \psi|_{x=+Tsi/2}$ are the potentials at the front- and back-silicon/oxide interfaces, respectively.

In the ideal long channel case, the potential distribution in the silicon channel is governed by the 1-dimensional Poisson's equation:

$$\epsilon_{si}\frac{d^2\psi(x,y)}{dx^2} = qN_c \cdot \exp\left[\frac{q(\psi(x,y) - V_{ch}(y))}{kT}\right] \tag{2.2}$$

where ϵ_{si} is the dielectric constant of silicon, N_c is the conduction band density of states of silicon, and V_{ch} is the channel voltage (the electron quasi Fermi level potential relative to the source). The Boltzmann's approximation is used for the inversion carrier density. The charge contribution of ionized dopants is neglected since the body is lightly-doped. We focus on an n-type device and neglect the contribution of holes.

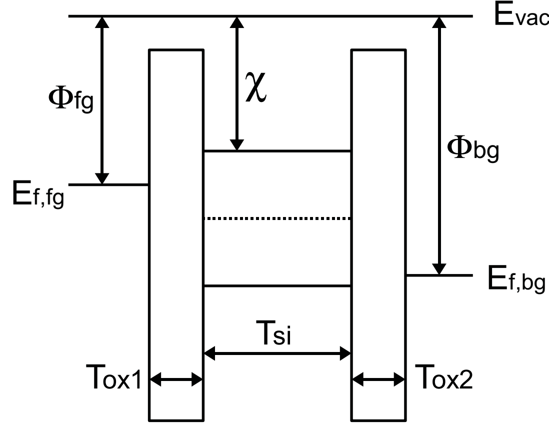


Figure 2.2: Energy band diagram at flat-band condition corresponding to the $A - A'$ cutline in Fig. 2.1. χ is the electron affinity.

The continuity of displacement field at the front and back interfaces gives the following relation of the surface electric fields ($E_{s1} = -\frac{d\psi}{dx}|_{x=-Tsi/2}$ and $E_{s2} = -\frac{d\psi}{dx}|_{x=Tsi/2}$) and surface potentials:

$$C_{ox1(2)}\left(V_{fg(bg)} - \Delta\Phi_{1(2)} - \psi_{s1(2)}\right) = \epsilon_{si} E_{s1(2)} \tag{2.3}$$

where $C_{ox1(2)} = \epsilon_{ox1(2)}/T_{ox1(2)}$ are the front(back) oxide capacitances, and $\Delta\Phi_{1(2)}$ are the workfunction differences of the front-gate (back-gate) and the N+ source.

Equation (2.3) is the boundary condition for the ordinary differential equation (ODE), equation (2.2). The analytical solution to this problem is known [51, 52]. However, it requires the solving of a set of two coupled non-linear equations:

$$V_{fg} - \Delta\Phi_1 - V_{ch} = r_0 + \frac{2kT}{q}\ln\left[\frac{2\beta}{\sinh(\alpha-\beta)}\right] + r_1\beta\coth(\alpha-\beta) \tag{2.4}$$

$$V_{bg} - \Delta\Phi_2 - V_{ch} = r_0 + \frac{2kT}{q}\ln\left[\frac{2\beta}{\sinh(\alpha+\beta)}\right] - r_2\beta\coth(\alpha+\beta) \tag{2.5}$$

r_0, r_1 and r_2 are constants; α and β are unknowns. Unfortunately this set of coupled equations is very difficult to solve. Iterative techniques are either computationally expensive or have convergence problems [46]. A non-iterative technique is therefore desirable for a compact model. In the rest of this section we will show how this can be achieved.

Multiplying $\frac{d\psi}{dx}$ on both sides of Equation (2.2) and integrating from $x = -\frac{T_{si}}{2}$ to $x = \frac{T_{si}}{2}$, we obtain:

$$E_{s1}^2 - E_{s2}^2 = \frac{2N_c kT}{\epsilon_{si}} \left\{ \exp\left[\frac{q(\psi_{s1} - V_{ch})}{kT}\right] - \exp\left[\frac{q(\psi_{s2} - V_{ch})}{kT}\right] \right\} \tag{2.6}$$

For FDSOI devices it is desired to have inversion carriers concentrated at the front surface, since short channel effects such as V_{TH} roll-off and drain induced barrier lowering (DIBL) are less prominent in such a condition. For this reason we can assume the carrier density at the back interface is negligible compared to that at the front interface, and the second exponential term in Equation (2.6) can be neglected. Neglecting that term and substituting E_{s1} with 2.3, we obtain,

$$\left[\frac{C_{ox1}(V_{fg} - \Delta\Phi_1 - \psi_{s1})}{\epsilon_{si}}\right]^2 = E_{s2}^2 = \frac{2N_c kT}{\epsilon_{si}} \exp\left[\frac{q(\psi_{s1} - V_{ch})}{kT}\right] \tag{2.7}$$

In Equation (2.7), E_{s2} is a function of ψ_{s2}, making it difficult to find an explicit approximation. To overcome this difficulty, E_{s2} is approximated by assuming a constant displacement field in the vertical direction between the two gates, including the front oxide, the silicon body, and the back oxide,

$$E_{s2} = \frac{(V_{fg} - \Delta\Phi_1) - (V_{bg} - \Delta\Phi_2)}{\frac{\epsilon_{si}}{\epsilon_{ox}}(T_{ox1} + T_{ox2}) + T_{si}} \tag{2.8}$$

This simplification reduces the number of unknowns in Equation (2.7) to one. We can then solve Equation (2.7) and obtain $\psi_{s1}^{(1)}$ (ψ_{s1} without perturbation) using a computationally efficient explicit approximation similar to that described in [47]. The details of this explicit approximation are described in [46].

Equation(2.8) is a good approximation when the transistor is biased in weak inversion and the carrier density in the body is insignificant. In strong inversion, however, a two-dimensional electron gas forms at the front surface, and the displacement field in the front oxide is quite different from that in the body and the back oxide. To further improve the accuracy of the model in strong inversion, a perturbation step is employed to refine ψ_{s1}. The back surface field is estimated using.

$$E'_{s2} = \frac{\psi_{s1}^{(1)} - (V_{bg} - \Delta\Phi_2)}{\frac{\epsilon_{si}}{\epsilon_{ox}} T_{ox2} + T_{si}} \tag{2.9}$$

where a constant displacement field is assumed in the body and the back oxide, but this field is not assumed to be the same as that in the front oxide. Substituting E_{s2} with E'_{s2} in Equation (2.7), we obtain $\psi_{s1}^{(2)}$ (ψ_{s1} with perturbation).

The inversion carrier per area, Q_{inv} and the back surface potential, ψ_{s2}, are computed as functions of ψ_{s1} through the Poissons Equation (2). The details on the calculation of

ψ_{s2} and Q_{inv} are given in the Appendix A. The model is verified with TCAD for an ideal long channel device without the use of any fitting parameters. In Fig. 2.3, ψ_{s1} and ψ_{s2} are plotted versus front-gate voltage (V_{fg}) for different values of $V_{ch}(y)$, corresponding to different positions along the channel. Good agreement between the model and TCAD is achieved. In Fig. 2.3 we compared the surface potential solutions with and without perturbation. Without perturbation, ψ_{s1} is reasonably accurate (In Fig. 2.3(a) the curves with and without perturbation overlap). But a large deviation is observed for ψ_{s2} (Fig. 2.3(b)). Since ψ_{s1} is accurate we use it to compute E'_{s2} in Equation (2.8). We then obtain accurate ψ_{s1} and ψ_{s2}.

For an FDSOI device with a thick buried oxide in sub-threshold operation, the potential throughout the body is almost constant. Therefore the inversion carrier density is proportional to the body thickness. This is sometimes referred to as volume inversion [53]. The surface potential approximation preserves this important property, as shown in Fig. 2.4.

2.3.3 Drain Current Model

In this subsection, a drain current model for long channel FDSOI MOSFETs is derived and verified with TCAD.

The charge sheet approximation [54] is often used for deriving the MOSFET drain current, as in [26]. Although it simplifies the derivation of drain current and charge, it introduces some error in the moderate inversion region. In this work we show that Ids can be derived for FDSOI MOSFETs in closed form without involving the charge sheet approximation.

The drain current is derived based on drift diffusion transport:

$$I_{ds} = \mu \cdot W \cdot Q_{inv}(y) \cdot \frac{dV_{ch}(y)}{dy} \tag{2.10}$$

where μ is the carrier mobility. For simplicity μ is treated as a constant during derivation. However, in the final compact model μ is replaced with the vertical field-dependent effective mobility. For a lightly-doped body, the unit area inversion charge density can be expressed as:

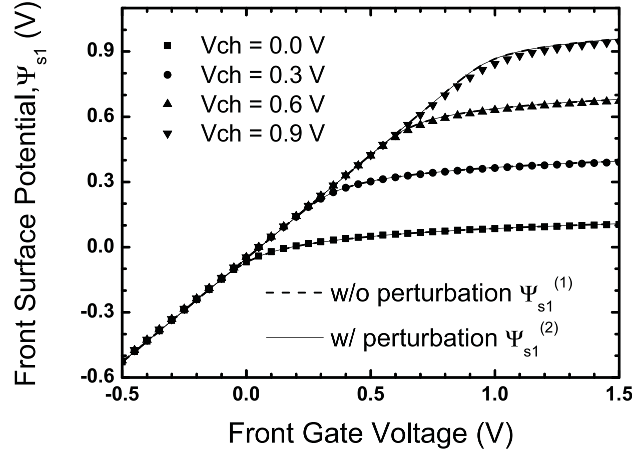
$$Q_{inv} = \sqrt{2N_c kT\epsilon_{si} \exp\left[\frac{q\left[\psi_{s1}(y) - V_{ch}(y)\right]}{kT}\right] + \left(\epsilon_{si}E_{s2}\right)^2} - \epsilon_{si}E_{s2} \tag{2.11}$$

based on Equations (2.3), (2.7) and the Gauss law. We differentiate Equation (2.11) with respect to the channel position, y and simplify it into a form suitable for Ids integration:

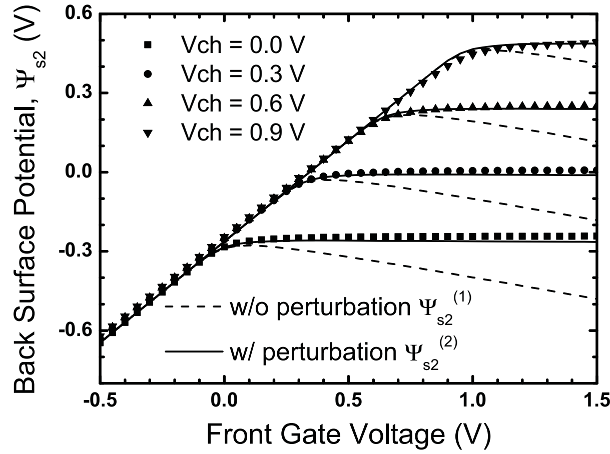
$$\eta \cdot \frac{kT}{q} \cdot \frac{dQ_{inv}(y)}{dy} = Q_{inv}(y)\frac{d}{dy}\left[\psi_{s1}(y) - V_{ch}(y)\right] \tag{2.12}$$

where

$$\eta = 2 - \frac{2\epsilon_{si}\tilde{E}_{s2}}{\tilde{Q}_{inv} + 2\epsilon_{si}\tilde{E}_{s2}} \tag{2.13}$$



(a)



(b)

Figure 2.3: (a) Front surface potential versus front-gate bias with varying channel voltage. The curves with and without perturbation overlaps. (b) Back surface potential versus front-gate bias (T_{ox1} = 1.2 nm, T_{ox2} = 20 nm, T_{si} = 15 nm, V_{bg} = 0, $q\Phi_{g1} = 4.05$ eV, $q\Phi_{g2} = 5.17$ eV). The surface potentials are obtained in TCAD by setting $V_{ds} = V_{ch}$ in a long channel (L = $10\mu m$) DG MOSFET structure and extracting the surface potential at the drain end of the channel. (Symbols: TCAD; Lines:Model)

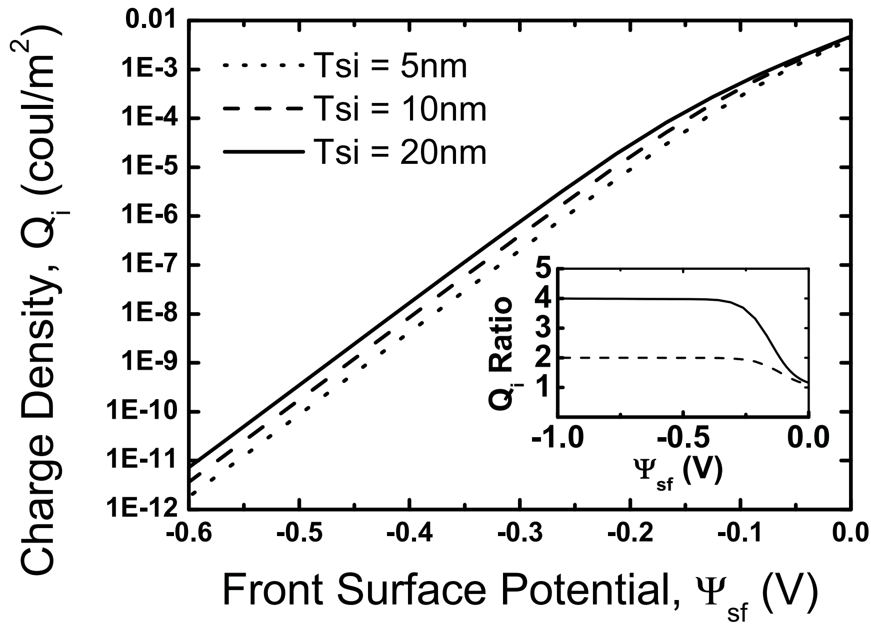


Figure 2.4: Inversion charge density (Q_{inv}) versus front surface potential (ψ_{s1}) for $T_{si} = 5$ nm, 10 nm and 20 nm. In sub-threshold operation carrier density is proportional to the body thickness if T_{ox2} is very large. This important property is preserved by the newly developed surface potential approximation. Inset shows Q_{inv} for $T_{si} = 10$ nm and $T_{si} = 20$ nm, both normalized to the $T_{si} = 5$ nm case. ($T_{ox1} = 1.2$ nm; $T_{ox2} = 10$ μm).

η varies from 1 in sub-threshold to 2 in strong inversion. The exact form of η is with $\tilde{E}_{s2} = E_{s2}(y)$ and $\tilde{Q}_{inv} = Q_{inv}(y)$, both being a function of y. However to simplify the derivation of I_{ds} we approximate $E_{s2}(y)$ and $Q_{inv}(y)$ using their average source-side (y = 0) and drain-side (y = L) values, $\bar{E}_{s2}$ and $\bar{Q}_{inv}$ so that η becomes independent of position. In equation (2.12), $Q_{inv}(y)$ can be expressed based on Gauss law as

$$Q_{inv}(y) = C_{ox1}\left[V_{fg} - \Delta\Phi_1 - \psi_{s1}(y)\right] - \epsilon_{si} E_{s2}(y) \tag{2.14}$$

To make integration possible, we interpolate $E_{s2}(y)$ as a linear function of the surface potential [55]. We substitute Equations (2.12) and (2.14) into Equation (2.10) and perform integration from source to drain. This gives:

$$I_{ds} = \mu \cdot \frac{W}{L} \cdot \left[\frac{Q_{inv,s} + Q_{inv,d}}{2}(\psi_{s1,d} - \psi_{s1,s}) + \eta \cdot \frac{kT}{q}(Q_{inv,s} - Q_{inv,d})\right] \tag{2.15}$$

$\psi_{s1,s}$ and $\psi_{s1,d}$ are obtained by solving for surface potential at $V_{ch} = 0$ and $V_{ch} = V_{ds}$, respectively. $Q_{inv,s}$ and $Q_{inv,d}$ are calculated from $\psi_{s1,s}$ and $\psi_{s1,d}$, respectively. For long channel devices, Equation(2.15) naturally saturates at high drain bias due to pinch-off. For short channel devices, however, saturation happens before pinch-off due to velocity saturation. This is modeled by replacing Vds with an effect drain voltage, as in [55].

Figs. 2.5 – 2.10 verify the drain current model by comparing it with TCAD. In Fig. 2.5, V_{TH} is plotted versus back-gate voltage (V_{bg}) for both symmetric and asymmetric double-gate devices operating in the independent-gate model. The independent-gate FinFET [18] is one example of independent-gate devices with symmetric gate stacks. The model agrees well with TCAD at different T_{ox2}. The larger slope for thin back-oxide devices is due to the stronger coupling from the back-side. Fig. 2.6 shows I_{ds} versus V_{fg} for different T_{ox1}. Fig. 2.7 shows I_{ds} versus V_{ds} at several V_{fg}. Fig. 2.8 shows the transconductance (g_m) versus V_{fg} at both linear and saturation modes. In all cases, the model agrees well with TCAD simulations without the use of any fitting parameters, reflecting the inherent predictability and scalability of the model. The effect of not using perturbation and the effect of using the charge sheet approximation (obtained by setting $\eta = 1$ in Equation (2.15)) are also shown in Figs. 2.6 - 2.8 for comparison.

Fig. 2.9 verifies the transconductance efficiency, g_m/I_{ds}. Fig. 2.10 shows the relative error of various models compared to TCAD. With the charge sheet approximation the Ids peak error is about 14% in moderate inversion (without perturbation for ψ_{s1} calculation). Replacing the Ids equation with (2.15) improves the accuracy. Perturbation further improves the accuracy so that the peak error becomes about 2%. This error can be simply reclaimed by using some amount of flexible fitting parameters if needed, as is done in a practical compact model.

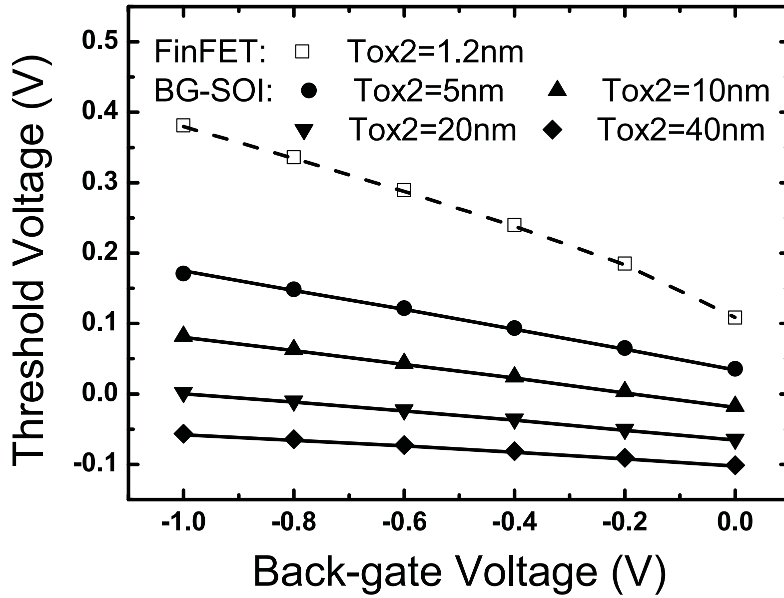


Figure 2.5: Threshold voltage versus front-gate bias. Solid lines and closed symbols: back-gated FDSOI structure with varying back oxide thickness ($T_{si} = 15nm$, $T_{ox1} = 1.2nm$, $V_{ch} = 0$, $\Phi_{g1} = 4.05V$, $\Phi_{g2} = 5.17V$); dashed lines and open symbols: independent-gate FinFET structure [18] ($T_{ox1} = T_{ox2} = 1.2nm$, $T_{si} = 15nm$, $\Phi_{g1} = 4.4V$, $\Phi_{g2} = 4.4V$). The threshold voltage is extracted using a constant current definition ($100nA \cdot W/L$). (Symbols: TCAD; Lines: Model)

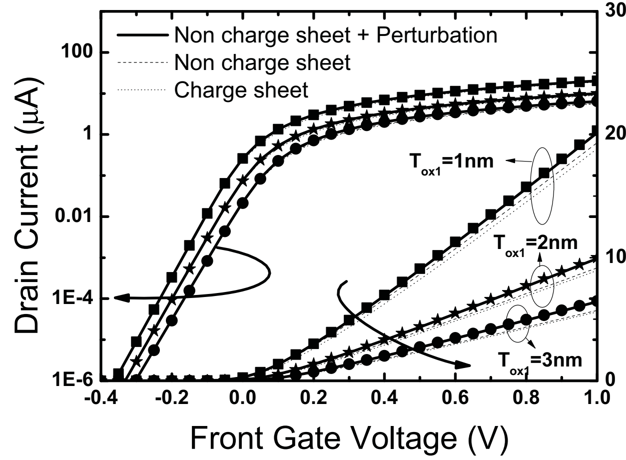


Figure 2.6: Drain current versus front-gate voltage for different front dielectric thicknesses. ($T_{si} = 15nm$, $T_{ox2} = 20nm$, $V_{bg} = 0$, $V_{ds} = 50mV$, $\Phi_{g1} = 4.05V$, $\Phi_{g2} = 5.17V$) (Symbols: TCAD; Lines: Model)

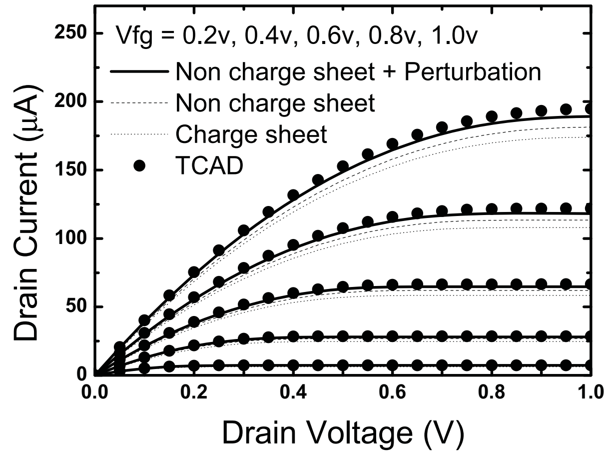


Figure 2.7: Drain current versus drain voltage for different front-gate bias. ($T_{si} = 15nm$, $T_{ox1} = 1nm$, $T_{ox2} = 20nm$, $V_{bg} = 0$, $\Phi_{g1} = 4.05V$, $\Phi_{g2} = 5.17V$) (Symbols: TCAD; Lines: Model)

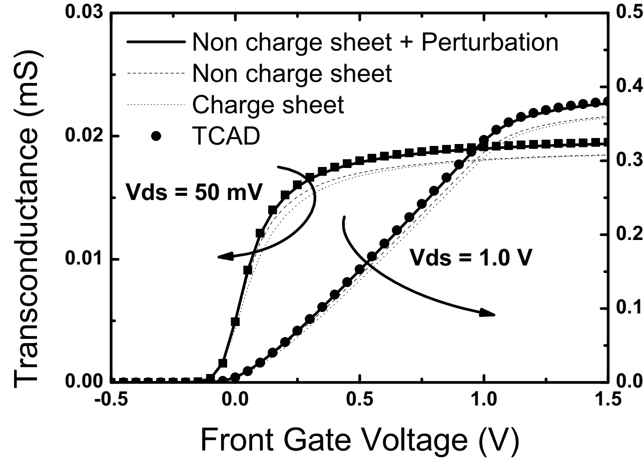


Figure 2.8: Transconductance versus front-gate voltage at $V_{ds} = 50mV$ and $V_{ds} = 1.0V$. The transconductance in TCAD is extracted from small-signal simulations. ($T_{si} = 15nm$, $T_{ox1} = 1.2nm$, $T_{ox2} = 20nm$, $V_{bg} = 0$, $\Phi_{g1} = 4.05V$, $\Phi_{g2} = 5.17V$) (Symbols: TCAD; Lines: Model).

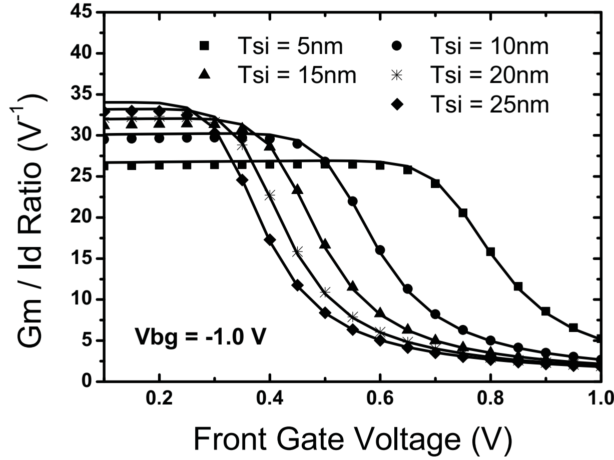


Figure 2.9: Transconductance efficiency (g_m/I_{ds}) versus front-gate voltage for different silicon body thicknesses. ($T_{ox1} = T_{ox2} = 1.2$nm, $V_{bg} = -1V$, $\Phi_{g1} = 4.4$V, $\Phi_{g2} = 4.4$V) (Symbols: TCAD; Lines: Model).

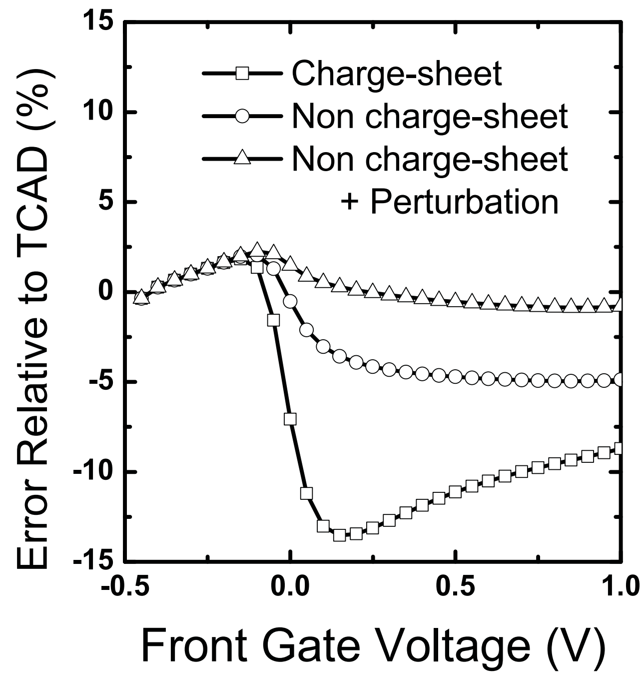


Figure 2.10: Percentage error in I_{ds} versus V_{fg} relative to TCAD for the charge-sheet model, the non-charge-sheet model, and the non-charge-sheet model with surface potential perturbation. ($T_{si} = 15nm$, $T_{ox1} = 1.0nm$, $T_{ox2} = 20nm$, $V_{bg} = 0$, $\Phi_{g1} = 4.05V$, $\Phi_{g2} = 5.17V$)

2.3.4 Capacitance Model

The C-V model for long channel back-gated FDSOI MOSFETs is derived using the charge-based approach, which preserves charge conservation [56]. In FDSOI, the exact expression for inversion charge density (Q_{inv}) is quite complex. Nevertheless, as long as the back surface does not enter inversion, we may approximate Q_{inv} as follows:

$$Q_{inv}(y) = C_{ox1}\left[V_{fg} - \Delta\Phi_1 - \psi_{s1}(y)\right] + \frac{C_{ox2}C_{si}}{C_{ox2}+C_{si}}\left[V_{bg} - \Delta\Phi_2 - \psi_{s1}(y)\right] \tag{2.16}$$

where $C_{si} = \epsilon_{si}/T_{si}$ is the body capacitance. Here Q_{inv} is decomposed into two components: the first term representing the charge due to the front oxide capacitor; the second term representing the charge due to the back oxide capacitance (C_{ox2}) in series with the body capacitance (C_{si}). Substituting Equation (2.16) into Equation (2.15) and utilizing current continuity, we obtain the relation of ψ_{s1} and y as follows:

$$\begin{aligned} y &= \mu C_{ox1}\frac{W}{I_{ds}}\left(\psi_{s1}(y) - \psi_{s1,s}\right) \\ &\left\{V_{fg} - \Delta\Phi_1 - \frac{\psi_{s1,s}+\psi_{s1}(y)}{2} + \gamma_c \cdot \left[V_{bg} - \Delta\Phi_2 - \frac{\psi_{s1,s}+\psi_{s1}(y)}{2}\right] + \eta \cdot \frac{kT}{q}(1+\gamma_c)\right\} \end{aligned} \tag{2.17}$$

where $\gamma_c = (C_{ox2} \parallel C_{si})/C_{ox1}$. Utilizing Equation (2.17) we may derive expressions for the total charge associated with each terminal of the device. The charge associated with the front-gate is obtained by integrating the front-gate charge density from source to drain:

$$\begin{aligned} Q_{fg} &= W\int_0^L C_{ox1}\left[V_{fg} - \Delta\Phi_1 - \psi_{s1}(y)\right] dy \\ &= C_{ox1}WL\left\{V_{fg} - \Delta\Phi_1 - \frac{\psi_{s1,s}+\psi_{s1,d}}{2} + \frac{B(\psi_{s1,d}-\psi_{s1,s})^2}{6\left[A - B(\psi_{s1,d}+\psi_{s1,s})\right]}\right\} \end{aligned} \tag{2.18}$$

where

$$A = V_{fg} - \Delta\Phi_1 + \gamma_c \cdot (V_{bg} - \Delta\Phi_2) + \eta \cdot \frac{kT}{q}(1+\gamma_c) \tag{2.19}$$

$$B = \frac{1+\gamma_c}{2} \tag{2.20}$$

Similarly, the charge associated with the back-gate is derived:

$$\begin{aligned} Q_{bg} &= W\int_0^L \frac{C_{ox2}C_{si}}{C_{ox2}+C_{si}}\left[V_{bg} - \Delta\Phi_2 - \psi_{s1}(y)\right] dy \\ &= \gamma_c \cdot \left\{Q_{fg} - C_{ox1} \cdot WL \cdot \left[(V_{fg} - \Delta\Phi_1) - (V_{bg} - \Delta\Phi_2)\right]\right\} \end{aligned} \tag{2.21}$$

To obtain the drain charge we follow the Ward-Dutton charge partition scheme [57].

$$
\begin{aligned}
Q_d &= W\Bigg(\int_0^L C_{ox1}\left[V_{fg}-\Delta\Phi_1-\psi_{s1}(y)\right]\frac{y}{L}dy \\
&\quad + \int_0^L (C_{ox2} \parallel C_{si})\left[V_{bg}-\Delta\Phi_2-\psi_{s1}(y)\right]\frac{y}{L}dy\Bigg) \\
&= -\frac{C_{ox1}WL}{2}\Bigg\{(V_{fg}-\Delta\Phi_1)+\gamma_c(V_{bg}-\Delta\Phi_2)-(1+\gamma_c)\cdot\Bigg[\frac{\psi_{s1,s}+2\psi_{s1,d}}{3}+ \\
&\quad \frac{B(\psi_{s1,d}-\psi_{s1,s})^2}{6[A-B(\psi_{s1,s}+\psi_{s1,d})]}-\frac{B^2(\psi_{s1,d}-\psi_{s1,s})^3}{30[A-B(\psi_{s1,s}+\psi_{s1,d})]^2}\Bigg\}
\end{aligned} \tag{2.22}
$$

Finally, the source charge is calculated from all the other components by charge neutrality:

$$
Q_s = -Q_{fg} - Q_{bg} - Q_d \tag{2.23}
$$

The C-V model is verified by comparing transcapacitances to small-signal TCAD simulations in Figs. 2.11 and 2.12. In Fig. 2.11, transcapacitances C_{sd}, C_{ds}, C_{ss} and C_{dd} are plotted versus V_{ds}. At $V_{ds}=0$, C_{ss} and C_{dd} are equal; C_{sd} and C_{ds} are equal, reflecting the source-drain symmetry of the C-V model. In Fig. 2.12, transcapacitances $C_{fg,fg}$, $C_{s,fg}$, $C_{d,fg}$ and $C_{bg,fg}$ are plotted versus V_{fg}. In both plots, the model matches TCAD very well in both linear and saturation mode without the use of any fitting parameters.

2.4 Core Model of BSIM-CMG

The core model of BSIM-CMG is described fairly well in [34, 52]. In this section we present and enhanced I-V model that makes it compatible with a charge segmentation based non quasi-static core model.

2.4.1 Background

Non quasi-static (NQS) effects is important for devices operating near its cutoff frequency. Since the device cutoff frequency is a strong function of L, NQS is often encountered in circuits with a mixture of long channel and short channel devices [58].

In BSIM-CMG, NQS effects is modeled using the charge segmentation method[2]. Fig. 2.13 illustrates the basic concept. The transistor in question is divided into N segments

[2]In BSIM-CMG, there are many options for modeling NQS effects, selected by the user through the parameter $NQSMOD$. When $NQSMOD=1$ the equivalent gate resistor NQS model is activated. When $NQSMOD=3$ the charge segmentation method is activated.

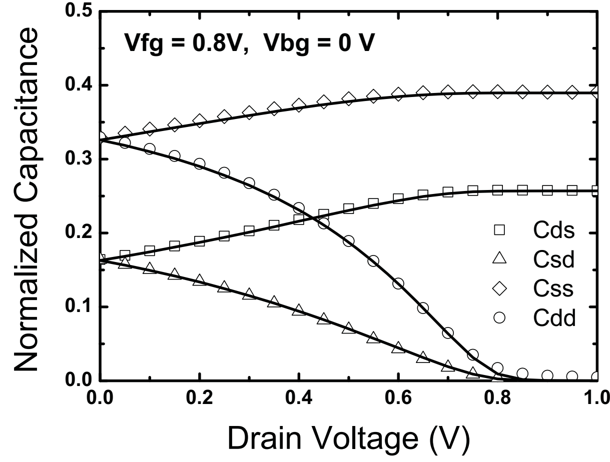


Figure 2.11: Transcapacitances C_{ds}, C_{sd}, C_{ss} and C_{dd}, normalized to $C_{ox1}WL$, versus drain voltage. ($T_{si} = 15nm$, $T_{ox1} = 1.2nm$, $T_{ox2} = 20nm$, $V_{fg} = 0.8V$, $V_{bg} = 0$, $q\Phi_{g1} = 4.05eV$, $q\Phi_{g2} = 5.17eV$) (Symbols: TCAD; Lines: Model)

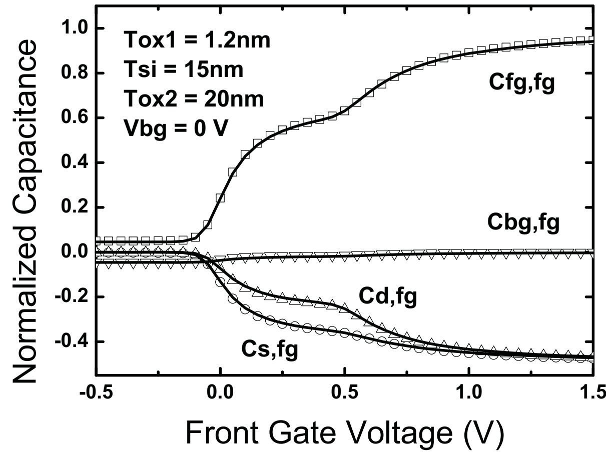


Figure 2.12: Transcapacitances $C_{fg,fg}$, $C_{d,fg}$, $C_{s,fg}$ and $C_{bg,fg}$, normalized to $C_{ox1}WL$, versus front-gate voltage. ($T_{si} = 15nm$, $T_{ox1} = 1.2nm$, $T_{ox2} = 20nm$, $V_{ds} = 0.5V$, $V_{bg} = 0$, $\Phi_{g1} = 4.05V$, $\Phi_{g2} = 5.17V$) (Symbols: TCAD; Lines: Model)

with equal length. The voltage at the segment boundary is used to represent the inversion charge density (q_i) at the location. The quasi-static DC current and charge can be expressed in terms of inversion charge densities at the source (q_{is}) and drain (q_{id}) ends. For the non quasi-static case, the same expression is used to calculate the DC current and charge associate with each segment. They are expressed as function of the inversion carrier density at the segment boundaries.

The advantage of this approach is the input voltage equation does not have to be solved for each segment (to calculate surface potential). Instead, SPICE automatically computes the inversion charge density at each segment boundary. This is the main advantage of this approach compared to the NQS effect model in [59].

One requirement for this type of segmentation is the consistency of current with the quasi-static case. In other words, at low operating frequency the NQS effects model must give the same result as the quasi-static model. The current expression of BSIM-CMG automatically satisfy this because [34]

$$I_{ds,qs} = \frac{1}{L}\left[h(Q_{is}) - h(Q_{id})\right] \tag{2.24}$$

. For an N-segmented NQS model we can show that

$$I_{ds,nqs} = \frac{1}{N} \cdot \left\{ \frac{1}{L/N}\left[h(Q_{is}) - h(Q_{i1}) + h(Q_{i1}) - h(Q_{i2}) + \cdots - h(Q_{id})\right] \right\} = I_{ds,qs} \tag{2.25}$$

. We have also verified this through simulation.

On the other hand, the quasi-static C-V model as described in [34] is not perfectly consistent with the I-V. The quasi-static C-V is derived using a simpler charge sheet based I-V as the current continuity relation, since the full I-V is too complicated. As a result, the quasi-static C-V becomes inconsistent with the NQS C-V, which utilizes the full I-V to compute inversion charges at each segment boundary.

We would like to have to have an accuracy of the full I-V. We would also like a simpler I-V so that C-V can be consistently derived based on that. In the next section, we propose a solution that satisfies both requirements.

2.4.2 Simple Non Charge Sheet I-V Model

The drain current expression derived in [34] is repeated here for convenience:

$$I_{ds} = \mu \cdot \frac{W_{eff}}{L} \cdot \left[\frac{Q_i^2}{2\,C_{ox}} + 2\,V_t\,Q_i - V_t \cdot (5C_{Si}V_t + Q_B)\;ln\left(5V_tC_{Si} + Q_B + Q_i\right) \right]_d^s \tag{2.26}$$

The last term in the above equation is what causes difficulty in terminal charge integration. We simplify it using the relation

$$Q_0 \cdot \ln\frac{Q_0 + Q_s}{Q_0 + Q_d} \approx \frac{Q_0}{Q_0 + \frac{Q_{is}+Q_{id}}{2}} \cdot (Q_{is} - Q_{id}) \tag{2.27}$$

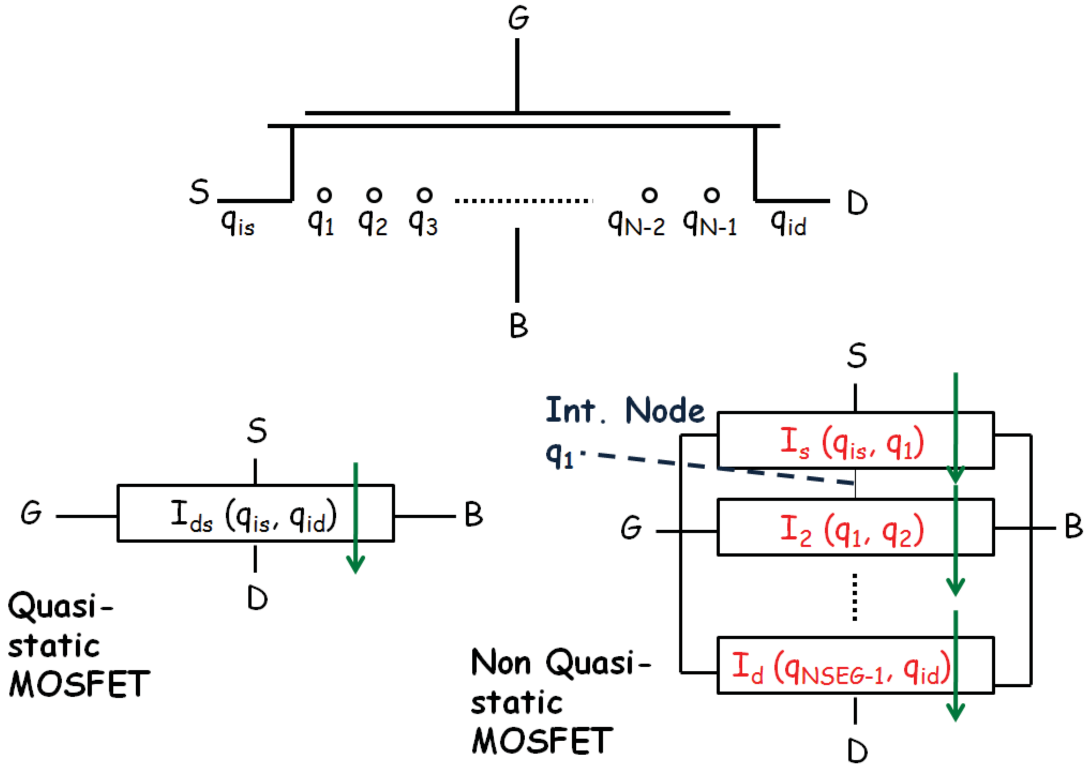


Figure 2.13: Illustration of the charge-segmentation method for non quasi-static effects modeling

The full I_{ds} expression becomes

$$I_{ds} = \mu \cdot \frac{W_{eff}}{L} \cdot \left[\frac{{Q_{is}}^2 - {Q_{id}}^2}{2C_{ox}} + \eta \cdot V_t \cdot (Q_{is} - Q_{id}) \right] \tag{2.28}$$

where

$$\eta = 2 - \frac{Q_0}{Q_0 + \frac{Q_{is}+Q_{id}}{2}} \tag{2.29}$$

Equation (2.28) is simple enough that analytical expressions for terminal charges can be derived, provided that η is treated as a constant during integration.

To verify the accuracy of the newly derived expression, we compare it with two-dimensional TCAD simulations [49]. Fig. 2.14 – 2.16 show the errors of drain current, transconductance, and transconductance efficiency for a common multi-gate device with a lightly-doped body. On the same graph we showed the results for four different cases: charge sheet (CS), original BSIM-CMG I-V model (Dunga), I_{ds} model given in [48] (Taur), and equation (2.28). As expected, the charge sheet model has the largest error. The error for the remaining cases are all below 3%. [48] has the smallest error. The difference between the original BSIM-CMG I-V and this work is only visible for the high drain bias case. Fig. 2.17 verifies that for the heavy doping case the difference due to the equation change is also small. [48] is not included in Fig. 2.17 because it only models the lightly-doped case.

2.5 Real Device Effects and Source Drain Symmetry

The core model itself is insufficient to model real devices since it is derived under several assumptions such as constant carrier mobility and the gradual channel approximation. **Real device effect** corrections are necessary in order to capture all non-ideal effects observed in silicon data. BSIM4 model already models planar bulk transistors well. BSIM-MG takes a similar approach accounted for these effects.

One challenge of real device effect modeling is to maintain the physical symmetry of the MOSFET source and drain. Some of the real device effect corrections in BSIM4 have caused symmetry problems. Although many of them are used in BSIM-MG, they are modified and carefully tested so that source-drain symmetry is no longer an issue. The source/drain symmetry is often validated using the Gummel Symmetry Test [27]. Fig. 2.18 is an example of the Gummel Symmetry Test that confirms the symmetry of BSIM-IMG. The same test has been done for BSIM-CMG as well. The symmetry of terminal charge expression is conducted using the charge symmetry test as proposed in [45]. A detailed discussion about symmetry is provided in chapter 3.

Some real device effects considered in BSIM-CMG and BSIM-IMG are listed as follows:

1. V_{th} roll off with L

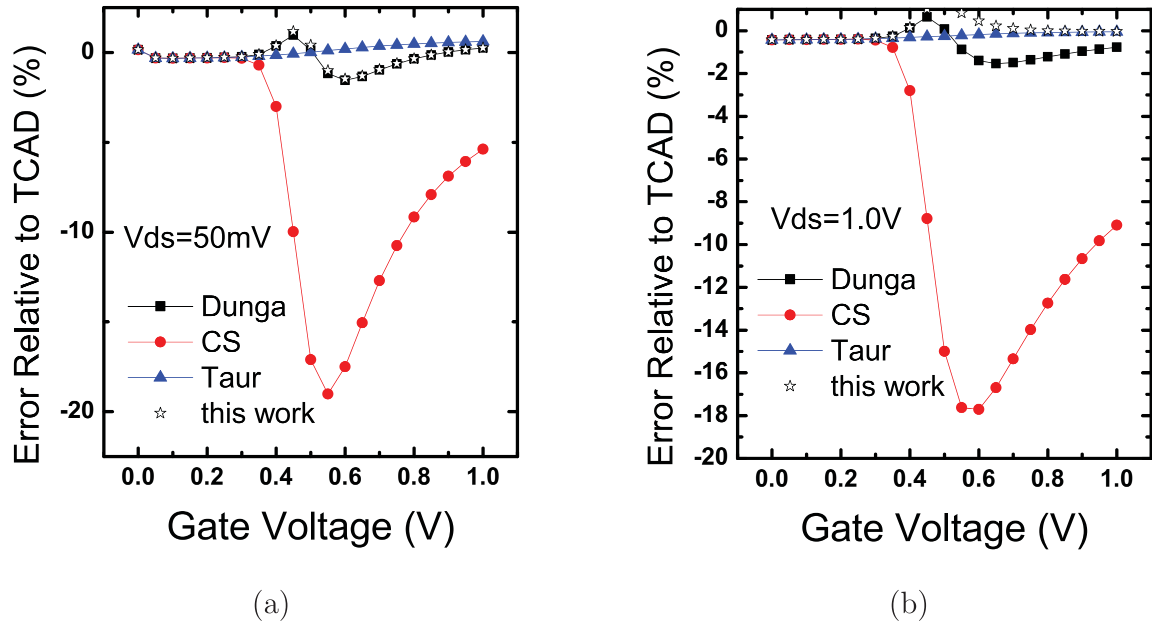
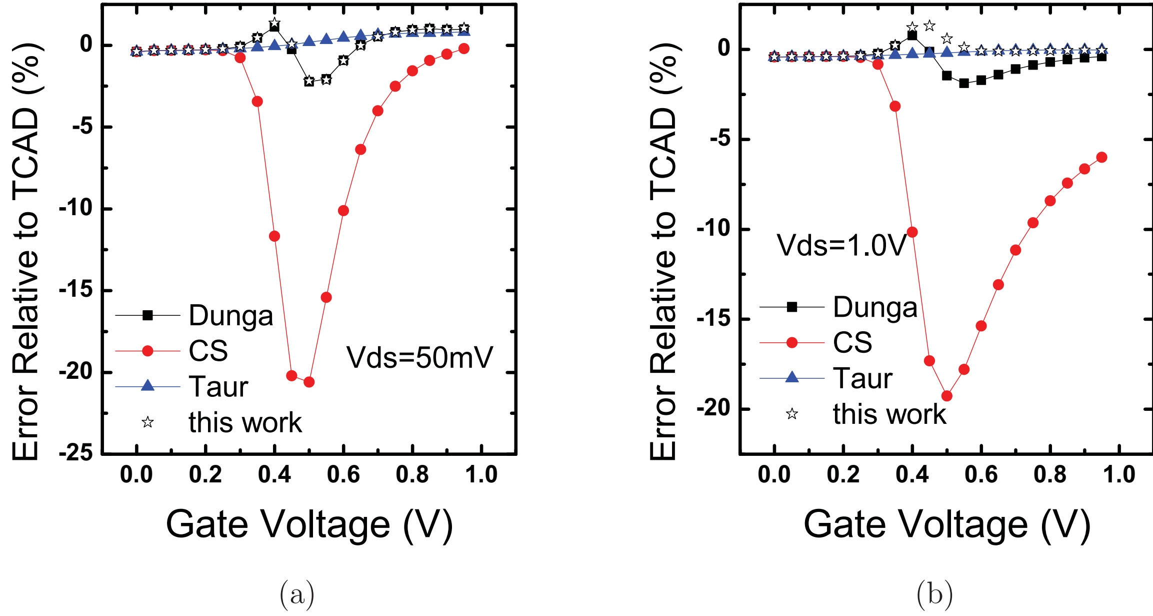


Figure 2.14: Error plot for drain current using TCAD as a reference

2. Drain induced barrier lowering
3. Sub-threshold swing degradation
4. Degradation of back-gate V_{th} control with reduced L (BSIM-IMG only)
5. Vertical field dependent carrier mobility
6. Quantum Mechanical Effects
7. Velocity saturation
8. Channel length modulation
9. Output resistance degradation due to DIBL
10. Gate-induced drain leakage
11. Gate tunneling current
12. Parasitic source/drain resistances
13. Overlap, inner fringe and outer fringe capacitances



(a) (b)

Figure 2.15: Error plot for the transconductance using TCAD as a reference

14. Impact ionization current

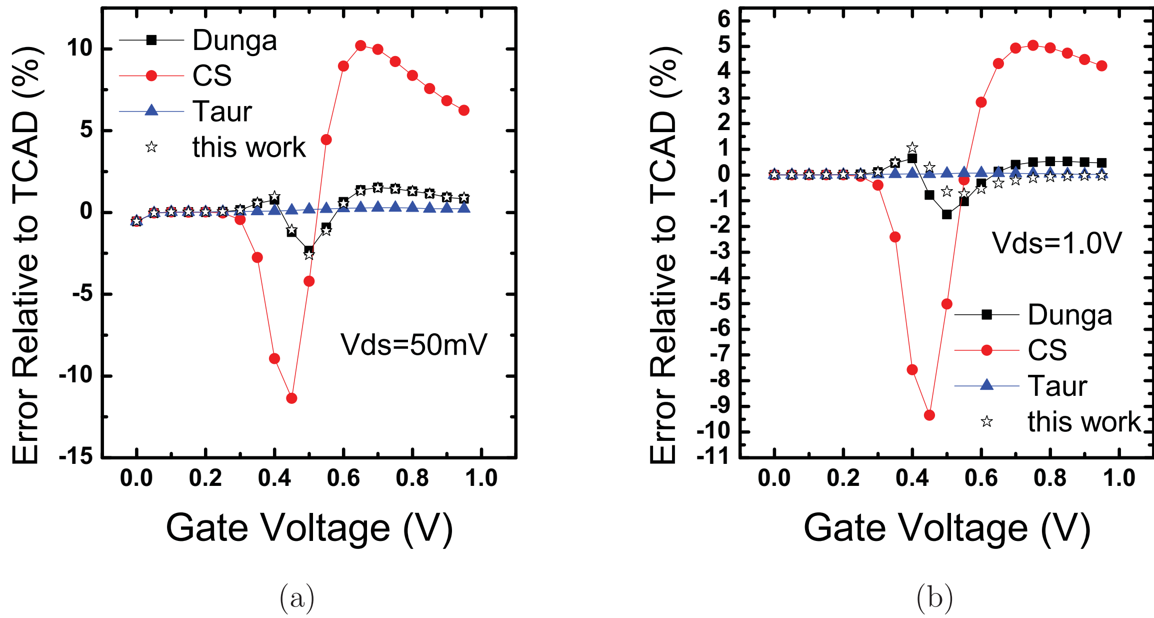
15. Temperature effects and self-heating

With these models implemented, BSIM-IMG is able to capture most real device characteristics. Detailed description of these real device effect models are available in the BSIM-MG user's manuals [60, 61] and two book chapters [62, 52].

The full BSIM-MG models including real device effects are validated by performing global extraction on measured data. BSIM-CMG is calibrated to measured FinFET data [63, 64] and BSIM-IMG is calibrated to an ETSOI technology [65] through an internship.

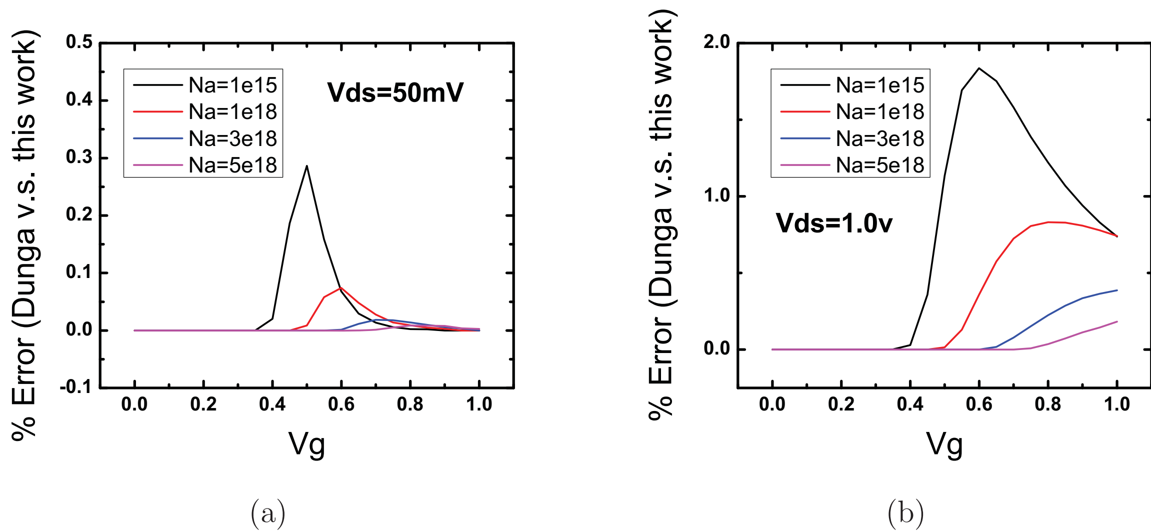
2.6 Model Convergence

To use a compact model in practical circuit simulation applications, its convergence property is essential. We have tested the convergence of the BSIM-IMG Verilog-A model in a circuit consisting of ten 101-stage ring oscillators. The ring oscillators are coupled together by $1k\Omega$ resistors, forming a circuit with a total of 2,020 transistors. Both DC and transient simulations are performed in HSpice [66] with its internal Verilog-A compiler. No convergence issue is observed.



(a) (b)

Figure 2.16: Error plot for transconductance efficiency, g_m/I_d using TCAD as a reference.



(a) (b)

Figure 2.17: Error plot for drain current at different doping levels.

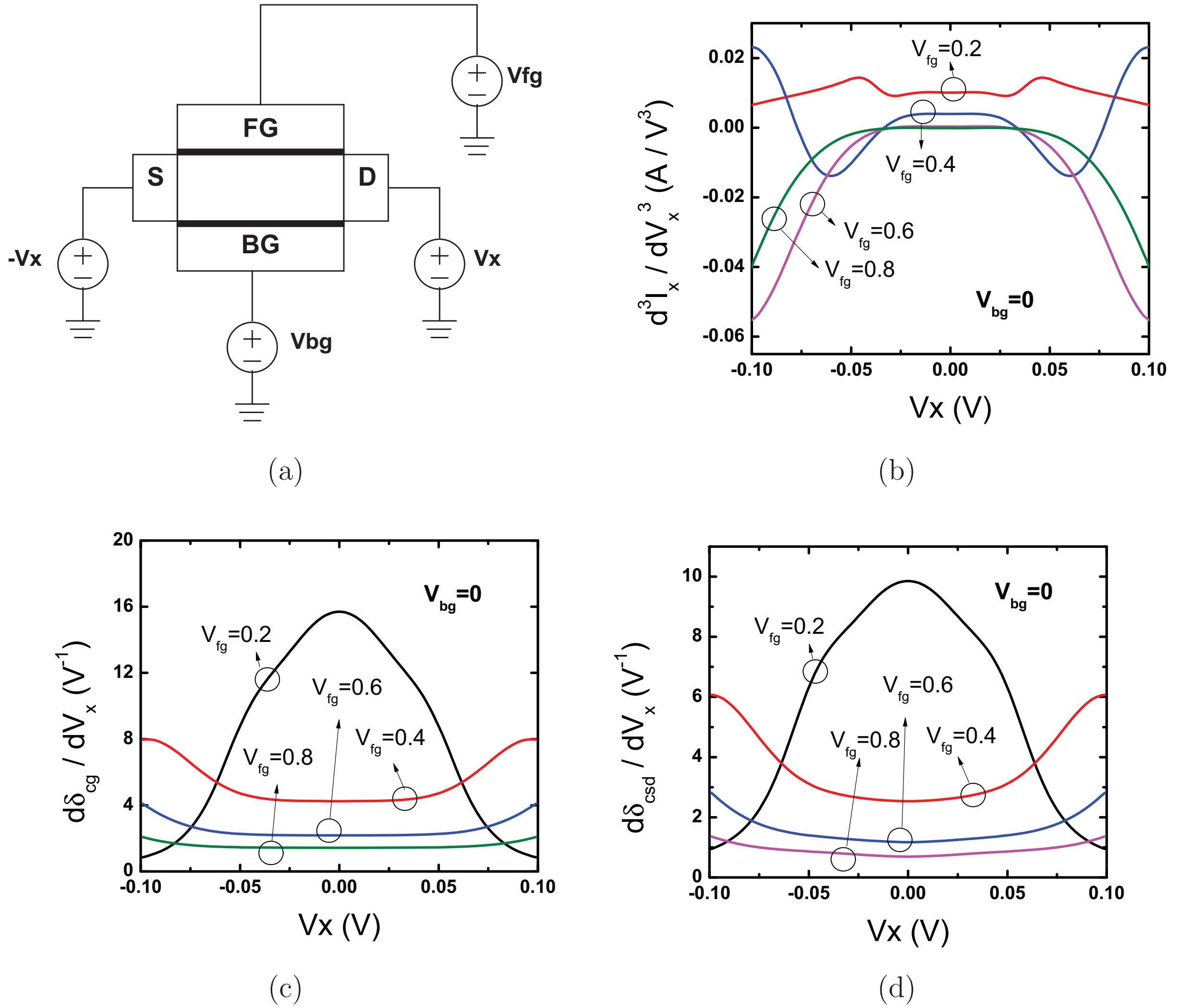


Figure 2.18: (a) Simulation setup for the Gummel symmetry test [27]. (b) 3rd derivative of I_x with respect to V_x. (c)(d) 3rd derivative of δ_{cg} and δ_{csd} with respect to V_x. δ_{cg} and δ_{csd} are evaluated using the methodology given in [45]. The continuity of curves at $V_x = 0$ reflexes symmetry. Real device effects are turned on for these tests.

Both BSIM-CMG and BSIM-IMG have been extensively evaluated by the industry for use in future multiple-gate technologies. This ensures the convergence of both models are thoroughly tested.

2.7 Computational Efficiency Study

Surface potential based model eliminates the need for empirical smoothing between the weak and strong inversion regions. At the same time, however, the calculation of surface potential itself may be time consuming. In this section, we present a study on the computational time of several numerical methods for multi-gate MOSFET surface potential calculation.

2.7.1 Evaluation Methodology

To evaluate the computation time for a numerical task, we implement it as a function in C language. A piece of time evaluation code calls the function N times. The times at the start and the end of this entire process are recorded and the time difference is divided by N. The result is recorded as t_{sample}.

t_{sample} evaluated using our method can be expressed as:

$$t_{sample} = \frac{t_{init} + N \cdot (t_{actual} + t_{loop})}{N} \tag{2.30}$$

where t_{init} time is the overhead associated with reading the system timer and starting the loop which calls the function N times; t_{loop} is the overhead associated with the loop control and the function call. By choosing a large N we can eliminate t_{init}. t_{loop} can be computed by evaluating an empty function call. The empty function call serves as the control group in this experiment.

In a real computing environment the speed may change depending on the load of the machine, even without other computationally expensive task running. Therefore we measure many samples and take the average. A small standard deviation usually reflexes a stable system condition.

To demonstrate the use of this evaluation methodology, we evaluated the time of several transcendental functions (Table 2.1). The results show that transcendental functions are much more time consuming than floating point division and multiplication [3]. Therefore it is important to reduce the number of transcendental fucntions used in the compact model. Observe that the computation time of transcendental functions depends on its input parameter. It may also depend on the processor (e.g. whether there is built in instruction sets for trigonometric functions) and the math library used.

[3] After examining the assembly code it was found that each multiplication or division instructions are accompanied with two memory operations

Table 2.1: Computation time evaluation results for transcendental functions ($N = 10^7$; 10 samples measured; Processor: Intel Quad Core Xeon CPU 2.9GHz; OS: Linux Kernel 2.6.18 64 bit; C Library: glibc-2.5)

Function	Input Range	Mean (ns)	STDEV (ns)	Function time (ns)
Empty Function	N/A	2.4	0.0044	
Sin	$-\frac{\pi}{2} \to \frac{\pi}{2}$	23.7	0.123	21.3
Sin	$\frac{\pi}{2} \to \frac{3\pi}{2}$	42.8	0.192	40.4
Cos	$-\frac{\pi}{2} \to \frac{\pi}{2}$	27.2	0.139	24.8
Tan	$-\frac{\pi}{2} \to \frac{\pi}{2}$	55.9	0.234	53.5
Ln	$-10^{-10} \to 10^{10}$	57.8	0.159	55.4
ArcTan	$-6400 \to 6300$	33.6	0.254	31.2
ArcCos	$-1 \to 1$	37.0	0.124	34.6
Sinh	$-16 \to 16$	77.4	0.073	75.0
Exp	$-16 \to 16$	31.2	0.187	28.8
Sqrt	$0 \to 1$	19.6	0.116	17.2
10 Multiplications	$0 \to 1$	20.7	0.099	1.83
10 Divisions	$0 \to 1$	102.5	0.477	10.0

STDEV: standard deviation

Table 2.2: Computation time evaluation results for surface potential calculations in BSIM-CMG ($N = 10^6$; 20 samples measured; $V_{ch} = 0$, $V_{gs} - V_{fb} = 0.7$)

Function	Mean (μs)	Standard Deviation (ns)
COREMOD=0 Newton Iteration	3.76	3.61
COREMOD=0 Analytical	2.17	4.43
COREMOD=1 Analytical	1.40	3.25
Cylindrical-gate Mode	1.34	4.29

2.7.2 Computational Efficiency of Surface Potential Calculation in BSIM-CMG

In BSIM-CMG there are several options for surface potential calculation. If the user selects COREMOD=1 the input voltage equation which assumes a lightly-doped body is solved analytically. If COREMOD=0 another input voltage equation that allows a heavily-doped body is solved analytically using the perturbation method [67]. For cylindrical-gate devices, still another input voltage equation is solved [68].

We have also attempted to compute surface potential of COREMOD=0 using Newton Raphson iteration. This method is also included in the speed comparison.

The computational time evaluation result is shown in Table 2.2. Newton iteration (2 iterations) is relatively slow, therefore we did not include it in the final BSIM-CMG code. COREMOD=0 with explicit approximation is faster. COREMOD=1 is even faster and is the right choice for lightly-doped device. The cylindrical-gate surface potential calculation is the fastest.

2.7.3 Computational Efficiency of Surface Potential Calculation in BSIM-IMG

The same method is applied to BSIM-IMG to evaluate the speed of three different numerical methods.

Two iterative algorithms that numerically solve exact boundary value problem (Equations (2.2) and (2.3)) are used as references: the 2-dimensional Newton Raphson method and the shooting method [46]. As shown in Fig. 2.19, the explicit approximation described in section 2.3.2 is several times faster than the iterative methods. To put the results in perspective, we also performed transient simulation of a 17-stage ring oscillator using the BSIM4 model [22] on the same machine in HSpice [66]. The simulation length is chosen to be large enough

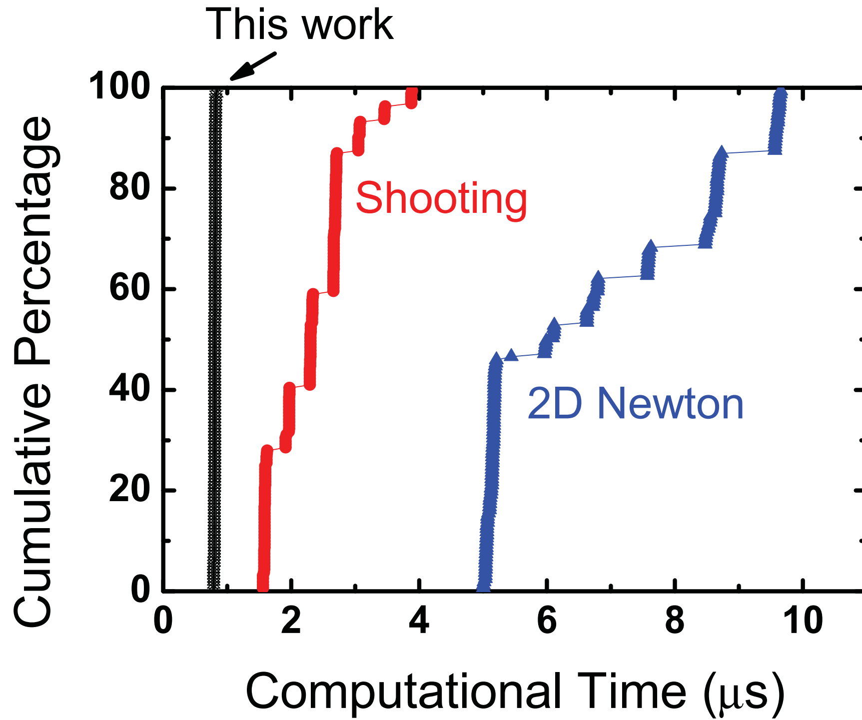


Figure 2.19: Computational time comparison of the explicit surface potential approximation (this work) and two iterative methods [46]. The front-gate voltage is swept from $1.135V$ to $1.665V$ in steps of $0.4V$. The back-gate voltage is swept from $1.135V$ to $0.065V$ in steps of $0.4V$. Five runtime evaluations are performed at each bias condition. Each runtime evaluation is performed by measuring the CPU time of 1,000,000 surface potential calculations.

that the initial setup time is negligible. The average runtime is 9.87 ls per instance per iteration. Therefore, the runtime of the explicit surface potential approximation is only 9% of the BSIM4 runtime (or 18% if both source and drain surface potential calculations are considered). In addition, without the perturbation step the computational time is further reduced by a factor of 1.5.

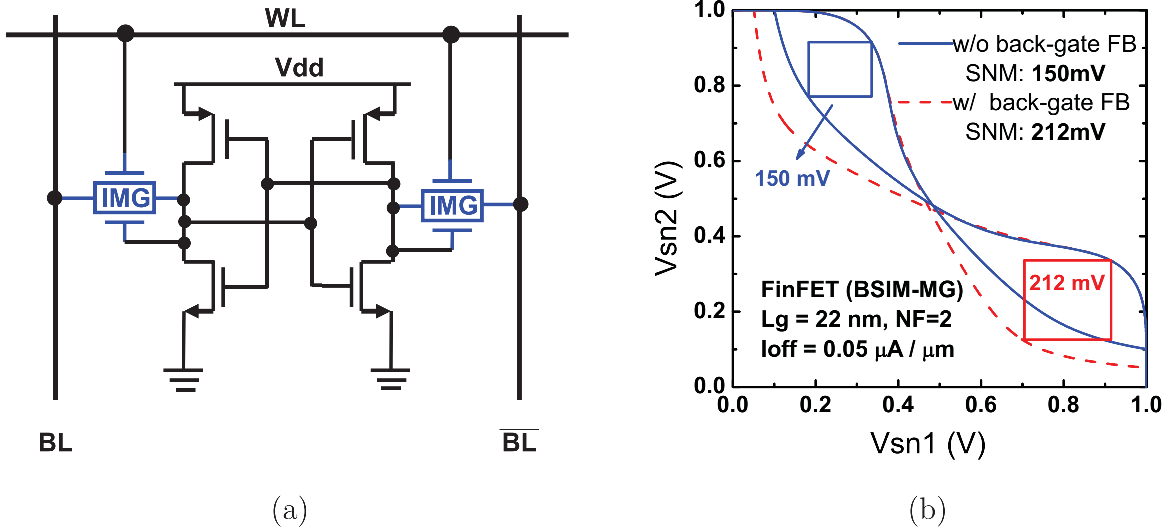


Figure 2.20: Read margin simulation for a FinFET SRAM cell with and without back-gate dynamic feedback. (a) Circuit schematic. (b) Butterfly plots and read margin extraction results. BSIM-IMG model is used for the independent-gates FinFETs and BSIM-CMG [25] is used for the common-gate FinFETs

2.8 Circuit Simulation using BSIM-IMG and BSIM-CMG

2.8.1 FinFET SRAM with Back-gate Dynamic Feedback

Back-gate dynamic feedback is a useful technique to improve the read margin of FinFET SRAM cells while not significantly reducing the write margin [32]. This circuit can be simulated with BSIM-IMG and BSIM-CMG. Fig. 2.20(a) shows the circuit schematic. The two access transistors are independent-gates FinFETs and are modeled with BSIM-IMG. The four transistors in the inverter pair are common-gate FinFETs and are modeled with BSIM-CMG [25]. For the control case, all six transistors are common-gate FinFETs modeled with BSIM-CMG. Fig. 2.20(b) shows the simulated butterfly curves for the 6-T SRAM cell. The significantly-improved read margin due to back-gate feedback is well-predicted by the model. This trend is consistent with mixed-mode TCAD simulation performed in [32].

The current limitation of the BSIM-IMG model is it underestimates current conduction at the back surface. Since the back-channel of the independent-gate FinFET will be inverted during write operation, we cannot simulate the write margin of dynamic-feedback FinFET SRAM.

2.8.2 Dynamic Threshold Voltage Tuning to Combat Variation in Back-gated FDSOI

The BSIM-IMG model is also used to explore the tuning of device variations by biasing the back-gate of IMG devices. Most likely this scenario is encountered in a back-gate FDSOI technology. In the scenario where devices in different circuit blocks have slightly different body thickness (T_{si}) and gate length (L_g) due to within-die variation, we can apply back-gate bias to tune off this variation. We simulate I_{on}, I_{off} of an n-type IMG device and the delay per stage of an IMG-based 17-stage ring oscillator in the presence of tuning.

With increasing body thickness, V_{th} increases due to the finite body doping. Therefore, I_{on} and I_{off} decrease (Fig. 2.21(b)), and the ring oscillator delay increases (Fig. 2.21(a)). V_{th} variation can be tuned out with proper choice of the back-gate voltage (V_{bg}) for both n-type and p-type devices (Fig. 2.21(a)). This tunes out the delay and I_{on} variation. However the trend of I_{off} is reversed because the sub-threshold slope for thick-body devices is slightly larger and I_{off} is larger, even though V_{th} is tuned out.

The same experiment is applied to the case of gate length variation. By back-gate biasing, we tune out the delay variation (Fig. 2.21(c)). Since gate length variation is related to both V_{th} variation and capacitance variation, to achieve a uniform delay V_{th} must be "over-tuned". In other words, after tuning V_{th} decreases with increasing gate length. As a result, both I_{on} and I_{off} increases with gate length after tuning.

2.9 Summary

Computationally efficient core models are developed for both common multi-gate MOSFETs and independent multi-gate MOSFETs. For independent multi-gate, an explicit approximation for surface potentials and integrated charge density is derived based on the Poissons equation. This approximation preserves important properties of the back-gated FDSOI MOSFET such as volume inversion. Drain current and terminal charge expressions are derived without using the charge sheet approximation. The model shows excellent agreements with ideal TCAD simulations without the use of any fitting parameters. For common multi-gate, an existing core drain current expression is simplified so that it is compatible with charge segmentation based non quasi-static effects implementation. No obvious change in accuracy is observed.

Non-ideal effects are integrated with the core models and implemented into Verilog-A based BSIM-CMG and BSIM-IMG compact models. Drain current and charge symmetry tests are performed, showing continuity of the model at $V_{ds} = 0$. The models exhibit good convergence properties. Computational efficiency of several surface potential numerical methods are evaluated for both BSIM-CMG and BSIM-IMG. For both cases we chose explicit approximation methods due to their efficiency and robustness.

We use BSIM-CMG and BSIM-IMG to simulate dynamic feedback FinFET SRAM cells

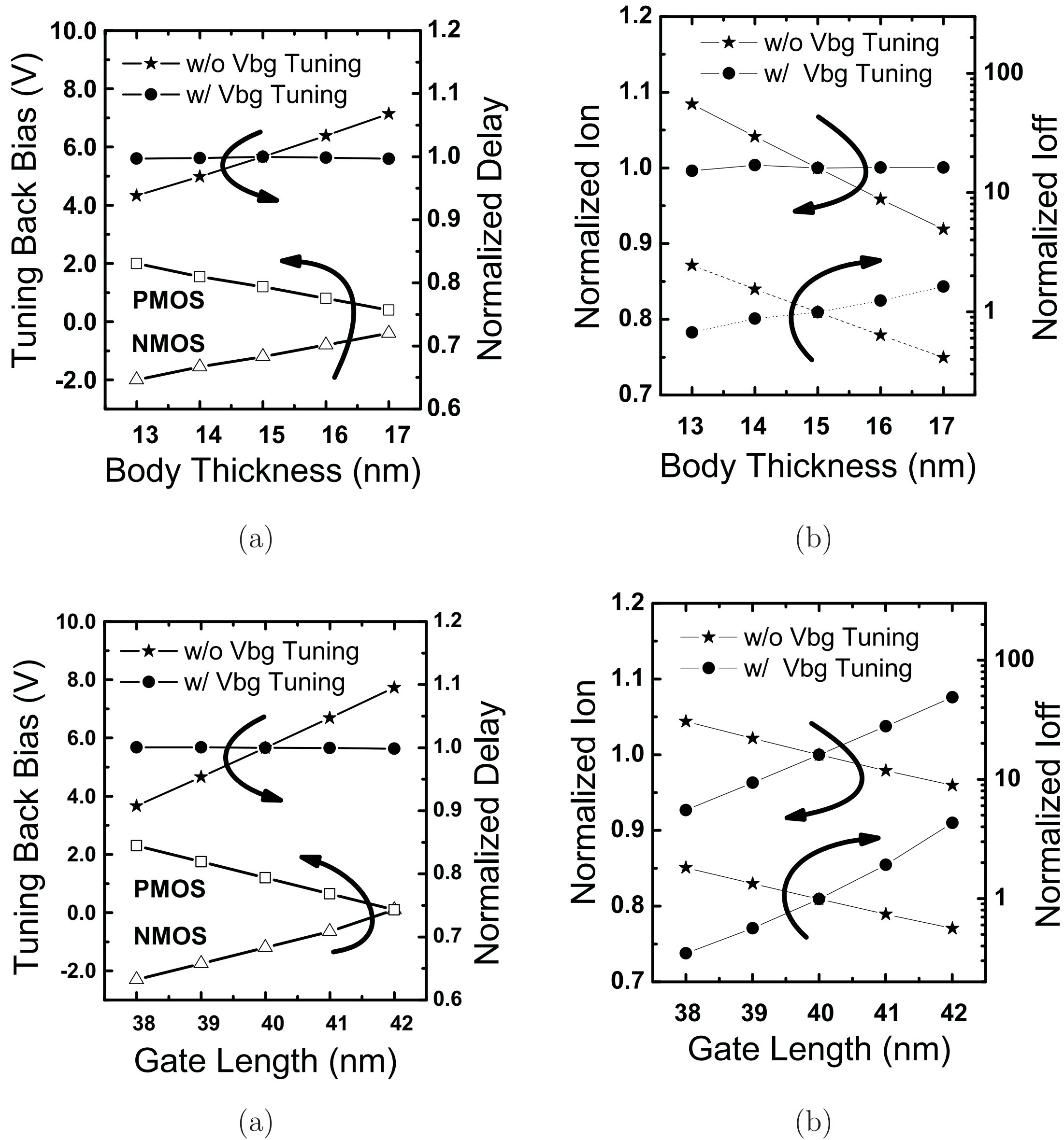


Figure 2.21: Device variation tuning using back-gated SOI MOSFET. (a) Gate delay variation due to body thickness variation can be tuned out by biasing the back gate. (b) The same back gate voltages tunes out I_{on} nearly completely but reverses the trend of I_{off}. (c) Gate delay variation due to gate length variation can also be tuned out by biasing the back gate. (d) The same back gate voltages reverses the trend of both I_{on} and I_{off}. The gate delays shown here are extracted from a 17 stage ring oscillator simulation.

and device variation tuning using back gate bias, highlighting its use for both circuit and technology development.

Chapter 3

Symmetry in MOSFET Compact Models

The MOSFET is a physically symmetric device. Therefore ideally in a device model the drain to source current (I_{ds}) and the terminal charges should remain the same when the source terminal and the drain terminal are swapped.

However, all MOSFET compact models employs approximations in one form or another. Once in a while these approximation are such that the source terminal and the drain terminal are not treated in the same way. For example, the body effect is often modeled as a function of body-to-source voltage, but not the body-to-drain voltage. This may cause the device model to violate symmetry.

To overcome this issue, most device models has a ”source-drain swapping” feature. When the device operation switches from the forward mode ($V_{ds} > 0$) to the reverse mode ($V_{ds} < 0$), the model automatically swaps the source terminal with the drain terminal, forcing the model to be symmetric. This, however, creates a discontinuity in the higher order derivatives at $V_{ds} = 0$ if the model is not symmetric to begin with. Therefore it is crucial to ensure the model equations are symmetric with respect to $V_{ds} = 0$.

In this chapter we will provide several guidelines on how source/drain symmetry is maintained, using BSIM-MG as an example.

3.1 Symmetry Definition and the Gummel Symmetry Test

If the device model is symmetric, the following relation is satisfied:

$$I_{ds}(V_d, V_g, V_s, V_b) = -I_{ds}(V_s, V_g, V_d, V_b) \tag{3.1}$$

The Gummel Symmetry Test (GST) [27] is the standard method for checking symmetry of a device model. A typical biasing setup for a GST is shown in Fig. 3.1. The dependent

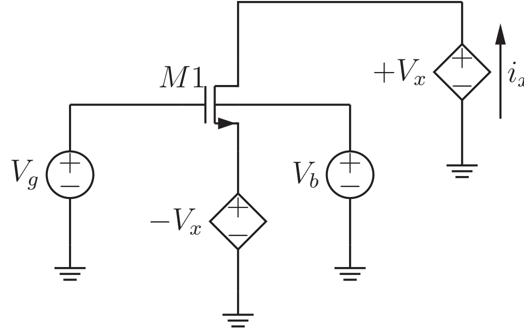


Figure 3.1: Biasing condition for the Gummel Symmetry Test

current sources V_x and $-V_x$ are swept from negative to positive and the drain-to-source current I_x is measured. Under this bias condition Equation (3.1) can be re-written as

$$I_x(V_x, V_g, -V_x, V_b) = -I_x(-V_x, V_g, V_x, V_b) \tag{3.2}$$

According to the above equation, for a fixed V_g and V_b the drain to source current I_x is an odd function of V_x. The Gummel Symmetry Test is able to verify this. Furthremore, suppose I_{ds} is a smooth function that is ∞-continuous, the 1st, 3rd, 5th, ... derivatives are even functions, and the 2nd, 4th, 6th, ... derivatives are odd functions. This can also be verified by plotting the derivatives of $I_x(V_x)$.

3.2 Symmetry of MOSFET Core Models

Typically the basic equations of a SPICE-oriented MOSFET compact model is developed by deriving drain current and terminal charge expressions for an ideal device with constant carrier mobility and no short channel effects. Such ideal device model is often referred to as the **core model**. For example, the core model for BSIM4 [22] is basically the square law model [8], and that of the PSP model [59] is a simplified version of the surface potential based Pao-Sah model [69].

A physically derived core model should be automatically symmetric. In this section we present several examples, including the square law model for drain current of planar bulk MOSFETs, and the surface-potential-based BSIM-CMG and BSIM-IMG core models.

3.2.1 Square Law Model

Since we are mainly concerned about the continuity near $V_{ds} = 0$, we focus on the square law model in the linear region. For the square law model in the linear region, the drain current

is expressed as:

$$\begin{cases} I_{ds} = \mu C_{ox}\frac{W}{L}(V_{gs} - V_{th} - \frac{m}{2}V_{ds})V_{ds} \\ V_{th} = V_{th0} + (m-1)V_{sb} \end{cases} \tag{3.3}$$

where V_{th0} is the threshold voltage at zero body and channel bias. The above equation can be re-written into a symmetric form:

$$I_{ds} = \mu C_{ox}\frac{W}{L}\left[V_g - \frac{m(V_s + V_d)}{2} + (m-1)V_b - V_{th0}\right] \cdot (V_d - V_s) \tag{3.4}$$

The condition given by Equation (3.1) is satisfied. Therefore the drain current model is symmetric. We have verified this using the Gummel Symmetry Test in MATLAB [70] up to the third derivative.

3.2.2 BSIM-IMG Core Model

The drain current expression of BSIM-IMG is given by Equation (2.15). Swapping all 's' subscripts with 'd' subscripts, we have

$$\mu \cdot \frac{W}{L} \cdot \left[\frac{Q_{inv,d} + Q_{inv,s}}{2}(\psi_{s1,s} - \psi_{s1,d}) + \eta \cdot \frac{kT}{q}(Q_{inv,d} - Q_{inv,s})\right] = -I_{ds} \tag{3.5}$$

provided η is unchanged under source and drain swapping. Since η is expressed as a function of the averages of the source-die and drain-side values of E_{s2} and Q_{inv}, it is indeed unchanged under source and drain swapping.

3.2.3 BSIM-CMG Core Model

It is easy to see that the form of Equation (2.24) automatically guarantees symmetry because swapping the 's' and 'd' subscripts negates I_{ds}. Perhaps a more interesting question is why the drain current expression in another earlier publication, [67], is symmetric. The expression is repeated here for convenience:

$$I_{ds} = \mu C_{ox}\frac{W}{L} \cdot \left[V_{gs} - V_{fb} - \frac{\psi_{ss} + \psi_{sd}}{2} - \frac{Q_b}{C_{ox}} + \frac{kT}{q}\right](\psi_{sd} - \psi_{ss}) \tag{3.6}$$

This is explained as follows. A property of the surface potential is reference invariance:

$$\psi_s(V_{gs}, V_{ch}) + x = \psi_s(V_{gs} + x, V_{ch} + x) \tag{3.7}$$

This is due to that fact that surface potential is raised by x if the reference point of all input parameters are lowered by x. For the case of BSIM-CMG this is valid and can be proven mathematically. In Equations (2.27)-(2.29) of [34], if we were to raise the solution of ψ_s,

ψ_0, ψ_1, V_{gs} and V_{ch} all by the same amount, the set of three input voltage equations are still satisfied. We can utilize reference invariance, Equation (3.7), to express the drain side surface potential in a different way:

$$\psi_{sd} = \psi_s(V_{gs}, V_{ds}) = \psi_s(V_{gs} - V_{ds}, 0) + V_{ds} \tag{3.8}$$

Equation (3.6) becomes

$$I_{ds} = \mu C_{ox}\frac{W}{L} \cdot \left[\frac{V_{gs} + V_{gd}}{2} - V_{fb} - \frac{\psi_s(V_{gs}, 0) + \psi_s(V_{gd}, 0)}{2} - \frac{Q_b}{C_{ox}} + \frac{kT}{q}\right](\psi_{sd} - \psi_{ss}) \tag{3.9}$$

which is negated when we swap V_{gs} with V_{gd}; ψ_{ss} with ψ_{sd}. Therefore I_{ds} satisfies symmetry.

3.3 Rules for Incorporating Real Device Effects

The core model expressions are modified to consider **real device effects**. Real device effects in MOSFETs include field-dependent mobility, short-channel V_{th} degradation, leakage currents, parasitic resistances, parasitic capacitances and many others.

For the overall model to satisfy source-drain symmetry, real device effects must be properly incorporated in the model with symmetry considerations. In this section, we present 5 possible methods of modifying the core model to incorporate real device effects without disturbing symmetry. We refer to these methods as **symmetry operations**

Operation 1 *Adding an even function $e(V_{ds})$ to one of the terminal voltages, V_z so that the new input voltage becomes $V_{z,eff} = V_z + e(V_{ds})$. 'z' can be any terminal other than 's' or 'd'.*

Proof: Without loss of generality, we consider the case where 'z' represents the gate terminal, 'g' in a conventional bulk MOSFET. The original drain current expression satisfies symmetry, therefore I_{ds} is an odd function of V_{ds}. In other words,

$$I_{ds}(V_d, V_g, V_s, V_b) = -I_{ds}(V_s, V_g, V_d, V_b) \tag{3.10}$$

is satisfied for all input conditions. After adding $e(V_{ds})$, the new I_{ds} is still an odd function of V_{ds}:

$$I_{ds}(V_d, V_g + e(V_d - V_s)), V_s, V_b) = -I_{ds}(V_s, V_g + e(V_s - V_d), V_d, V_b). \tag{3.11}$$

Therefore Operation 1 preserves symmetry. QED.

One example of this operation is the introduction of drain induced barrier lowering (DIBL) in BSIM-MG [25].

$$V_{g,eff} = V_g + c \cdot V_{dsx} \tag{3.12}$$

where c is a constant and

$$V_{dsx} = \sqrt{V_{ds}^2 + 0.01} - 0.1 \tag{3.13}$$

$c \cdot V_{dsx}$ is an even function of V_{ds}. The drain current is calculated as

$$I_{ds}(V_d, V_{g,eff}, V_s, V_b) \tag{3.14}$$

Another example is the modeling of the back-gate coupling effect in BSIM-IMG [1] [26] through an effective back-gate-to-source voltage:

$$\begin{aligned} V_{bgs,eff} &= V_{bgs} + k \cdot \left(V_{bgs} + \frac{V_{dsx} - V_{ds}}{2} \right) \\ &= V_{bgs} + k \cdot \frac{V_{dsx} + V_{bgs} + V_{bgd}}{2} \end{aligned} \tag{3.15}$$

where k is a constant. The second term on the right hand side of Equation (3.15) is also an even function of V_{ds}. Therefore symmetry is preserved.

Operation 2 *Replacing a constant c with an even function of V_{ds} that lies within the valid range of c.*

Proof: The original I_{ds} expression is an odd function of V_{ds} for all $c \in \mathbb{A}$, therefore,

$$I_{ds}(V_d, V_g, V_s, V_b; c) = -I_{ds}(V_s, V_g, V_d, V_b; c). \tag{3.16}$$

If c is replaced with an even function $e(V_{ds}) \in \mathbb{A}$, I_{ds} is still an odd function since

$$I_{ds}(V_d, V_g, V_s, V_b; e(V_d - V_s)) = -I_{ds}(V_s, V_g, V_d, V_b; e(V_s - V_d)). \tag{3.17}$$

QED .

One example of this operation is the modeling of sub-threshold swing in BSIM-MG. By replacing kT/q with nkT/q, where

$$n = 1 + \frac{C_{it} + C_{dsc} + C_{dscd} \cdot V_{dsx}}{C_{ox}} \tag{3.18}$$

, we model the drain bias dependence of subthreshold swing without disturbing symmetry. C_{it}, C_{dsc}, C_{dscd} and C_{ox} are bias-independent.

Operation 3 *Multiplying I_{ds} with an even function of V_{ds}*

This operation is the same as rewriting I_{ds} as $I_{ds} \cdot 1$ and replacing constant 1 with an even function of V_{ds}. Therefore Operation 3 is a special case of Operation 2 and it satisfy symmetry.

One example of this operation is the modeling of vertical field dependent mobility:

$$I'_{ds} = \frac{I_{ds}}{1 + UA \cdot (E_{eff})^{EU}} \tag{3.19}$$

where UA and EU are constnats. E_{eff} is a function of the average charge, q_{ia}, which is an even function of V_{ds}. Therefore E_{eff} is an even function of V_{ds} or V_x.

[1] Early versions of BSIM-IMG.

Operation 4 *Symmetrically adding external elements*

External elements are current or voltages sources or circuit elements:

1. whose values depend directly on node voltages, and
2. are independently attached to the transistor nodes.

If two external elements are symmetrically added to the MOSFET subcircuits, i.e., whatever is done to the source-side is done to the drain side, the model will remain symmetric.

One example of external element addition is the modeling of series source and drain resistances in the BSIM-family models[2]. The source resistance, R_s, is a function of V_{gs}; the drain resistance, R_d, is a function of V_{gd}. Both have the same functional form:

$$R_s(V_{gs}) = \frac{1}{Weff^{WR}} \cdot \left(RSWMIN + \frac{RSW}{1 + PRWG \cdot V_{gs,eff}} \right) \tag{3.20}$$

$$V_{gs,eff} = \frac{1}{2}\left[V_{gs} - V_{fbsd} + \sqrt{(V_{gs} - V_{fbsd})^2 + 10^{-4}} \right] \tag{3.21}$$

$$R_d(V_{gd}) = \frac{1}{Weff^{WR}} \cdot \left(RDWMIN + \frac{RDW}{1 + PRWG \cdot V_{gd,eff}} \right) \tag{3.22}$$

$$V_{gd,eff} = \frac{1}{2}\left[V_{gd} - V_{fbsd} + \sqrt{(V_{gd} - V_{fbsd})^2 + 10^{-4}} \right] \tag{3.23}$$

R_s and R_d are symmetrically attached to the source and drain nodes, respectively, as shown in Fig. 3.2. It is clear that when $RSW = RDW$ and $RDWMIN = RDWMIN$, the model is symmetric.

If RSW and RDW are not identical, the model will not be symmetric. Therefore it is important to use the un-swapped V_{gs} and V_{gd} to compute R_s and R_d so that even with non-identical source and drain side parameters there will be no discontinuity issue.

There are a few other examples of external element addition, such as the modeling of gate induced drain leakage current and the gate to source/drain tunneling current.

Operation 5 *Adding terms in the form of* $e(V_{ds}) \cdot (V_{ds} - V_{dseff})$

The following effective drain to source voltage, V_{dseff}, is proposed in [55]:

$$V_{dseff} = \frac{|V_{ds}|}{[1 - c \cdot |V_{ds}|^{2\kappa}]^{\frac{1}{2\kappa}}} \tag{3.24}$$

[2]rdsMod=1, or external resistance model.

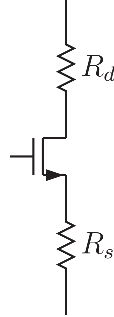


Figure 3.2: Illustration of source and drain series resistances in BSIM models

where $c = \frac{1}{{V_{dsat}}^{2\kappa}}$. κ can only take on integer values. Both BSIM-MG and PSP models use this V_{dseff} expression. However, unlike [55] κ is allowed to take on non-integer values for better fitting to data. For the V_{ds} smoothing to be meaningful we assume $2\kappa > 0$. Define

$$k(V_x) = |V_{ds}| - V_{dseff} = |V_x| \left\{ 1 - \frac{1}{\left[1 + c \cdot |V_x|^{2\kappa}\right]^{\frac{1}{2\kappa}}} \right\} \tag{3.25}$$

Since the absolute function is taken, $k(V_x)$ is automatically an even function of V_x. However, it is important to check its continuity at $V_x = 0$. From the above equation we observe that $k(0^-) = k(0^+) = 0$. We further examine this function by taking the derivatives of k. The first derivative is

$$k'(V_x) = \operatorname{sgn}(V_x) \left\{ 1 - \frac{1}{\left[1 + c \cdot |V_x|^{2\kappa}\right]^{\frac{1}{2\kappa}}} \right\} + cV_x|V_x|^{2\kappa-1} \cdot \left[1 + c|V_x|^{2\kappa}\right]^{-\frac{1}{2\kappa}-1} \tag{3.26}$$

$k'(0^-) = k'(0^+) = 0$ is satisfied. The second derivative is

$$\begin{aligned} k''(V_x) &= c|V_x|^{2\kappa-1}\left[1 + c|V_x|^{2\kappa}\right]^{-\frac{1}{2\kappa}-1} \\ &\quad +c\left[|V_x|^{2\kappa-1} + V_x \cdot (2\kappa-1)|V_x|^{2\kappa-2} \cdot \operatorname{sgn}(V_x)\right] \cdot \left[1 + c|V_x|^{2\kappa}\right]^{-\frac{1}{2\kappa}-1} \\ &\quad + \cdots \end{aligned} \tag{3.27}$$

$k''(0^-) = k''(0^+) = 0$ is satisfied provided $2\kappa > 1$. The third derivative is

$$\begin{aligned} k'''(V_x) &= c|V_x|^{2\kappa-2}\operatorname{sgn}(V_x)\left[1 + c|V_x|^{2\kappa}\right]^{-\frac{1}{2\kappa}-1} + c \cdot \Bigg[(2\kappa-1)|V_x|^{2\kappa-2}\operatorname{sgn}(V_x) \\ &\quad +(2\kappa-1)|V_x|^{2\kappa-2}\operatorname{sgn}(V_x) + V_x(2\kappa-1)(2\kappa-2)|V_x|^{2\kappa-3}\Bigg] \cdot \left[1 + c|V_x|^{2\kappa}\right]^{-\frac{1}{2\kappa}-1} \\ &\quad + \cdots \end{aligned} \tag{3.28}$$

$k'''(0^-) = k'''(0^+) = 0$ is satisfied provided $2\kappa > 2$. In fact the derivatives of $k(V_x)$ vanish up to the $n'th$ derivative for $2\kappa > n-1$. Note that in BSIM-MG 2κ is represented by the parameter $MEXP$.

Consequently, we can add terms containing $(V_{ds} - V_{dseff})$ in the drain current expression without breaking the continuity of the model at $V_{ds} = 0$ up to the $2\kappa + 1$'th derivative.

One example of this operation is the addition of channel length modulation to the core model of BSIM-MG. To model channel length modulation, an M_{clm} factor is multiplied to the drain current expression.

$$M_{clm} = 1 + \frac{1}{C_{clm}} \ln\left[1 + \frac{V_{ds} - V_{dseff}}{VASAT} \cdot C_{clm}\right] \tag{3.29}$$

The symmetry of this expression is verified in MATLAB. We implemented the square law model. The effective drain voltage expression, Equation (3.24) is used. Source drain swapping is implemented. The channel length modulation parameter is chosen such the there is significant slope change in the saturation part of the $I_d - V_{ds}$ curve. Fig. 3.3 shows the testing result for three different V_{gs} values: 0.6V, 0.8V and 1.0V. Correct parity is demonstrated. In addition, there is no discontinuity at $V_{ds} = 0$. Note that when we plot the 6th derivative, we see discontinuity (Fig. 3.4). This is true regardless of whether channel length modulation is implemented, as we will discuss later.

3.4 Relation of Source/Drain Swapping and Continuity

Most MOSFET compact models uses source/drain swapping to force the model to be symmetric. With source/drain swapping the drain current is

$$I'_{ds} = \begin{cases} I_{ds}(V_d, V_g, V_s, V_b) & V_d > V_s \\ -I_{ds}(V_s, V_g, V_d, V_b) & V_d < V_s \end{cases} \tag{3.30}$$

where I_{ds} is the drain current expression without swapping. In other words, the source and drain are exchanged and the drain current is negated when V_{ds} is negative. As a result, symmetry is always satisfied for I'_{ds}, regardless of the form of I_{ds}.

However, for most cases, the analytical form of I'_{ds} is different at positive versus negative drain biases. Consequently I'_{ds} cannot be ∞-continuous at $V_{ds} = 0$. An exception to this is when I_{ds} itself preserves symmetry (Equation (3.1) is satisfied). When I_{ds} is symmetric to begin with, swapping will have no effect. Therefore **in models that utilizes the swapping technique, discontinuity in I_{ds} or the derivatives of I_{ds} can be prevented by using analytical expressions that preserves symmetry to describe the drain current**. The same argument holds for charge as well.

3.5 Discussion on the Formulation of Effective Drain-to-source Voltage

To first order the core drain current in surface potential based MOSFET models is proportional to the surface potential difference, $(\psi_{sd} - \psi_{ss})$ [3]. Near $V_{ds} = 0$ at high gate bias the following approximation is valid:

$$I_{ds} \propto (\psi_{sd} - \psi_{ss}) \approx V_{dseff} \tag{3.31}$$

V_{dseff} appears because in the compact model we use V_{dseff} instead of V_{ds} to calculate the drain surface potential ψ_{sd}. We can re-write Equation (3.31) as:

$$I_{ds} \propto V_{dseff} = V_{ds} - k(V_{ds}) \tag{3.32}$$

where $k(V_{ds})$ is given in the end of section 3.3. We have shown that

$$k^{(n)}(0^{-}) = k^{(n)}(0^{+}) = 0 \tag{3.33}$$

holds up to $n = \lfloor 2\kappa + 1 \rfloor$. So the derivatives at $V_{ds} = 0$ is continuous up to the n'th order. Beyond n the derivative of k becomes discontinuous. One example is shown in Fig. 3.4.

Consequently, surface potential based models that uses equation 3.24 to calculate the effective drain to source voltage is not ∞-continuous at $V_{ds} = 0$. However, for most practical purposes it is sufficient, since circuit simulators only need a finite number of derivatives.

3.6 Summary

In this chapter we introduced the definition and testing methodology for MOSFET symmetry. We have mathematically proven that three core models – the square law model and the surface potential based core model of BSIM-IMG and BSIM-CMG are symmetric. Five "symmetry operations" are presented that serve as guidelines in making real device effect corrections to the current and charge. We showed that when a symmetry operation is applied to modify a symmetric model, the final model is still symmetric. Several examples of the application of symmetry operations are given. We discussed about the role of source/drain swapping on continuity, showing that by using analytical expressions that satisfy symmetry to describe current and charge, there will be no discontinuity at $V_{ds} = 0$. We also discuss about the effect drain voltage expression, showing that in real compact models continuity at zero drain bias is only preserved up to a finite derivative order.

[3] This relationship is exact for [59, 67]. For the latest BSIM-CMG or BSIM-IMG which does not use the charge sheet approximation for drain current calculation this is also a good approximation

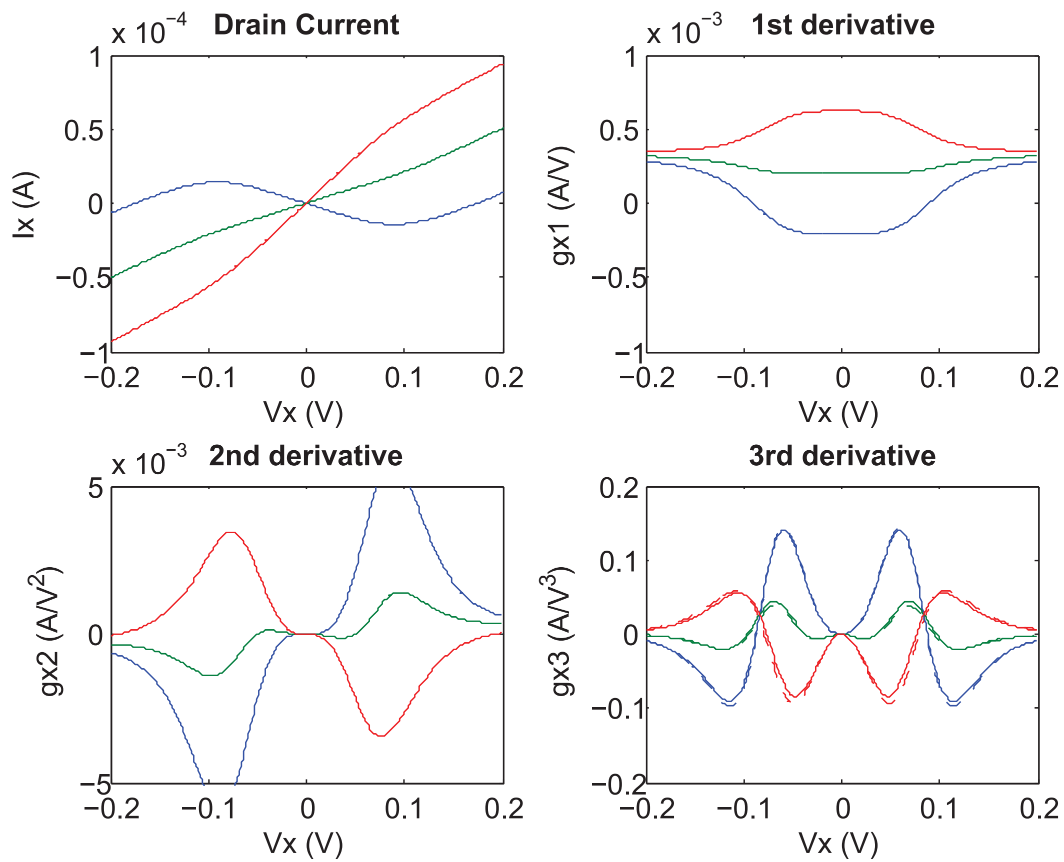


Figure 3.3: Symmetry testing for the channel length modulation model addition. The dashed lines are for $VASAT = 30$ so that there is very little channel length modulation effect. The solid lines are for $VASAT = 3$ where channel length modulation causes a significant change in $I_d - V_{ds}$. $2\kappa = 4$

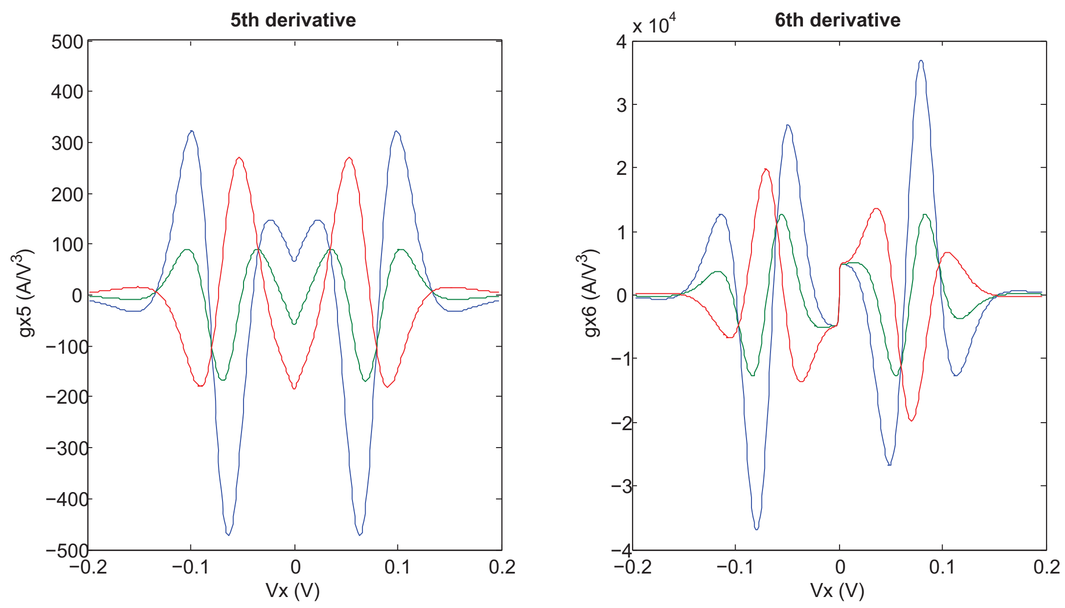


Figure 3.4: Symmetry testing: 5th and 6th derivative. $2\kappa = 4$

Chapter 4

Modeling of FinFET Parasitic Source and Drain Resistances

FinFETs [14] will likely be used in mainstream CMOS production in the near future. In previous chapters, we have discussed about the modeling of intrinsic device behavior of multi-gate MOSFETs, which include the FinFET. Another modeling aspect, which is perhaps equally challenging, is the parasitic resistances and capacitances. In the FinFET, parasitic resistances and capacitances are not only larger than planar MOSFET, but also more difficult to model due to the complex three dimensional geometry.

Parasitic resistances in the FinFET include the gate resistance and the source/drain resistance. The gate resistance is present due to the finite conductivity of the gate material. At DC the gate current is very small, so the gate resistance does not alter the transistor's DC behavior. However, it does impact the delay of CMOS circuits during switching. A compact analytical model for gate resistances in FinFETs was developed in [71]. Another important parasitic resistance component is the source/drain resistance. The source/drain resistance is usually more significant compared to the gate resistance. This is especially true with the recent introduction of the metal gate technology [6], in which highly-conductive metal is used as the MOSFET gate material. The 2010 ITRS roadmap for semiconductors [72] predicts that for 21nm high performance multi-gate technologies, the source/drain series resistance is as large as 26% of the NMOS on-state channel resistance(R_{on})[1]. An accurate model for source/drain resistance in FinFETs is needed.

Several models for source/drain resistances in FinFETs have been proposed. Dixit [73] proposed a comprehensive source/drain resistance model for double-gate MOSFET with lithography-defined source and drain, and verified it with TCAD and measured data. Tekleab [74] extended it to consider more than one contact surfaces. However these models are limited to rectangular source/drain contacts. FinFETs are expected to have several fins in parallel to have sufficient current driving capability. Research has shown that high layout density can

[1] R_{on} is defined as the supply voltage (V_{dd}) divided by the saturation drive current ($I_{d,sat}$).

be achieved if the multi-fins are enlarged and eventually merged using a selective epitaxial growth process, forming a connected three-dimensional raised source/drain contact [28, 75]. The cross section of such raised source/drain is likely non-rectangular. This needs to be considered. Moreover, it has been shown that the performance of fully-depleted FinFET is the best with an underlaped source/drain [76, 77]. Devices with underlaped source and drain have large bias-dependent source/drain resistance. However, both [73] and [74] consider bias-independent resistances only.

In this chapter, we developed a compact model for bias and geometry-dependent parasitic resistance for FinFETs with selective-epi-grown raised source/drain contacts. We will show that the model is applicable to raised source/drain FinFETs with non-rectangular source/drain cross section. To verify the model and demonstrate its predictivity, we will compare it with three dimensional TCAD simulations. In addition, we will also discuss about the modeling of bias-dependent source and drain resistances in the FinFET with source/drain underlap. The newly developed model is implemented in soon-to-be industry standard, BSIM-CMG [25].

The modeling of parasitic capacitances is equally important to accurately capture circuit performance. A separate model for geometry-dependent capacitances in FinFET was developed by Lin et al. [78] and implemented in BSIM-CMG.

4.1 FinFET Device Structure and Symbol Definitions

In this study we consider FinFETs in which the selective epitaxial growth (SEG) process is applied to merge individual fins. Single-fin FinFETs and multi-fin FinFETs will likely co-exist on the same wafer. Therefore we assume both single-fin and multi-fin FinFET will be subject to source/drain SEG, even though fin-merging is not necessary for single-fin FinFETs.

A 3-dimensional drawing of the raised source/drain FinFET is shown in Fig. 4.1. For simplicity we are showing only one fin of the multi-fin FinFET. The thin silicon channel, or the fin, is wrapped on three sides by the gate stack. The source and drain silicon are enlarged by SEG to reduce resistances. For multi-fin FinFETs, a larger source and drain also makes contacting easier. The thin region not covered by the gate is the extension region. It is not subject to SEG because it is protected by the spacer (not shown in figure) during epitaxial growth. The metallic region on top of the raised source and drain is the silicide. For single-fin FinFETs, depending on the process, the silicide may wrap around the RSD on three sides.

Fig. 4.2 is the cross sectional view of a FinFET along the source-to-drain direction. The insulating material on top of the fin and beneath the gate with height $TMASK$ is the hard mask. In many FinFET processes, a hard mask is used for fin etching and is left on top of the fin and is never removed. Since the top surface of the fin channel does not conduct current, the device becomes a **double-gate FinFET**. In other processes, no hard mask is

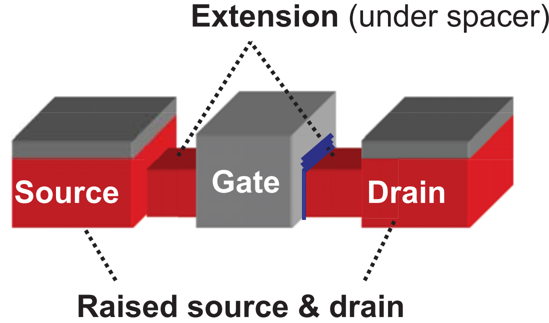


Figure 4.1: Bird-eye view of a raised source/drain FinFET

used. Instead $TMASK = T_{ox}$ and the top surface has current conduction. Such FinFET is a **triple-gate FinFET**. FinFETs may also be classified by substrate type into SOI FinFETs and bulk FinFETs. For example, Fig. 4.2 shows an SOI FinFET, which has its fin situated on top of the buried oxide. Table 4.1 lists the definition of symbols.

Selective epitaxial growth results in faceted RSD [28]. The final RSD may look something like the drawing in Fig. 4.3. The corresponding cross sectional diagram, cut in the direction parallel to the gate, is shown in Fig. 4.4.

The cross sectional area of the raised source/drain is A_{rsd}. For generality the source/drain resistance is modeled as function of A_{rsd} regardless of its shape. A_{rsd} in a structure like Fig. 4.4 is given by:

$$A_{rsd} = FPITCH \cdot HFIN + [TFIN + (FPITCH - TFIN) \cdot CRATIO] \cdot HEPI \quad (4.1)$$

where $CRATIO$ is the ratio of corner area filled with silicon to the total corner area. In the example given in Fig. 4.4, $CRATIO$ is 0.5.

Most FinFET devices in a digital circuit will have multiple fins. For multi-fin devices, the source/drain resistance is modeled as a function of the total area and perimeter, which is given by:

$$A_{rsd,total} = A_{rsd} \times NFIN + ARSDEND \quad (4.2)$$

$$P_{rsd,total} = (FPITCH + DELTAPRSD) \times NFIN + PRSDEND \quad (4.3)$$

$ARSDEND$ and $PRSDEND$ are the end components associated with the first and last fins.

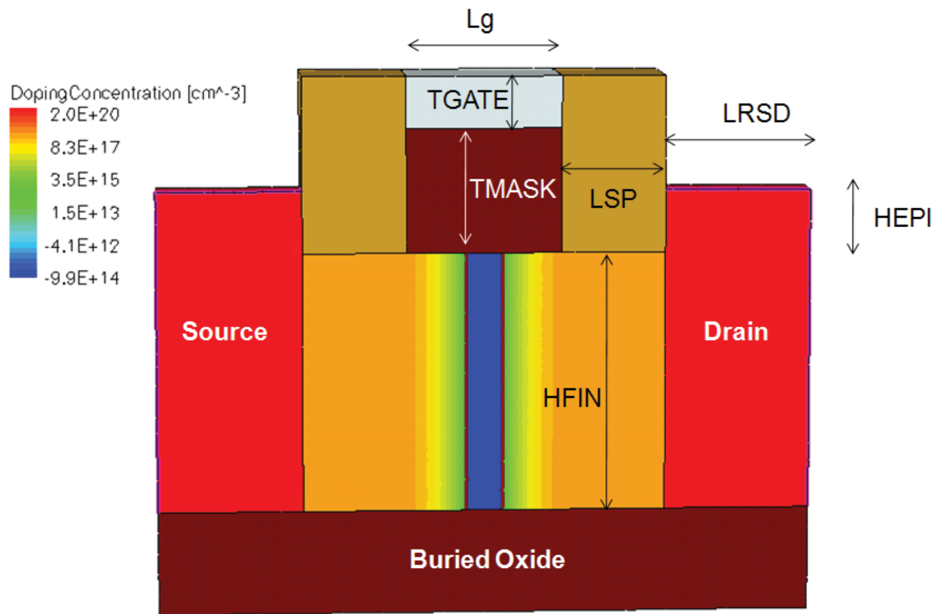


Figure 4.2: Cross section of a raised source/drain double-gate FinFET and symbol definition. This figure is a simulation structure in Sentaurus TCAD[79].

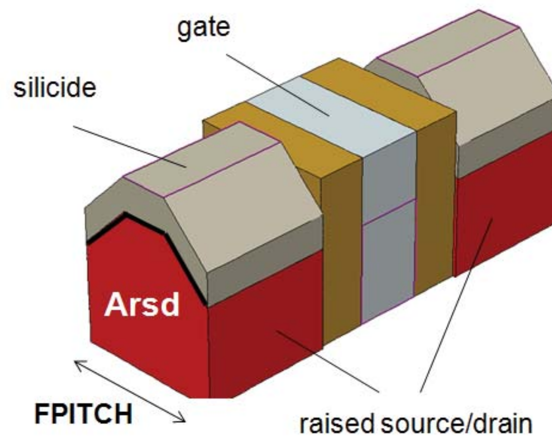


Figure 4.3: Bird-eye view of a FinFET with non-rectangular epi and top silicide. This figure is a simulation structure in Sentaurus TCAD[79].

Table 4.1: Symbol definition

Parameter name	**Definition**
L_g	Gate length
LSP	Spacer thickness
$LRSD$	Raised source/drain length
$HFIN$	Fin height
$TGATE$	Gate height
$HEPI$	Height of epitaxial silicon above fin
$FPITCH$	Fin pitch of the multi-fin FinFET
$TFIN$	Fin thickness
$CRATIO$	Ratio of the corner area filled with silicon to the total corner area
$NFIN$	Total number of fins in the FinFET
A_{rsd}	Per-fin component of the raised source/drain area
$ARSDEND$	End component of raised source/drain area
$DELTAPRSD$	Correction term for silicide/epitaxial silicon interfacial length per fin
$PRSDEND$	End component of silicide/epitaxial silicon interfacial length

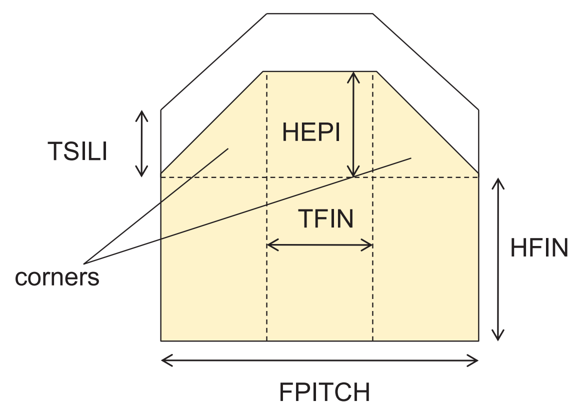


Figure 4.4: 2-D cross section of a FinFET with non-rectangular epi and top silicide

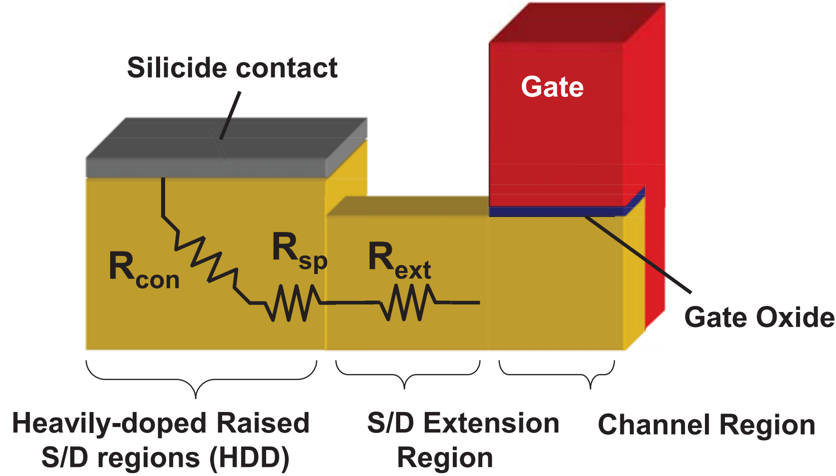


Figure 4.5: Illustration of the three components of the FinFET source/drain resistance

4.2 Modeling of Geometry Dependent Source/Drain Resistances in FinFETs

The FinFET source/drain resistance can be separated into three components, as illustrated in Fig. 4.5:

1. **Contact Resistance**(R_{con}): the combined resistance due to the raised source/drain region bulk resistivity and the silicon/silicide interface resistance

2. **Spreading Resistance**(R_{sp}): the resistance due to current spreading from the source/drain extension into the raised source/drain

3. **Extension Resistance**(R_{ext}): the bias-dependent resistance in the thin source/drain extension region under the spacer

We will discuss about each of these components in the following three subsections.

4.2.1 Contact Resistance

The contact resistance model accounts for both the bulk resistivity in the raised source/drain region and contact resistance at the silicon/silicide interface. Since the resistance is distributed, it is difficult to separate the two into individual resistors.

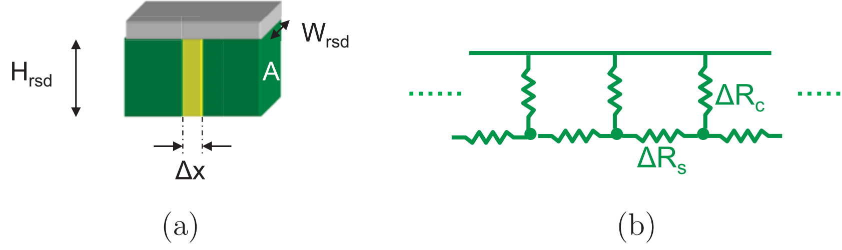


Figure 4.6: Resistance network considered for contact resistance derivation

To consider the distributed effect, we partition the raised source/drain region into infinitesimally thin vertical slices (Fig. 4.6(a)). The slices are connected in a resistance network as shown in Fig. 4.6(b). For each slice, there is a bulk resistance component,ΔR_s between adjacent slices, and a contact resistance component, ΔR_c from each slice to the contact. The bulk resistance component is given by

$$\Delta R_s = \rho \cdot \frac{\Delta x}{H_{rsd} \cdot W_{rsd}} \tag{4.4}$$

where ρ is the bulk resistivity, which is given by

$$\rho = \frac{1}{q \cdot N_{rsd} \cdot \mu_{rsd}} \tag{4.5}$$

. N_{rsd} is the raised source/drain region doping concentration. We assume the raised source/drain region is in-situ doped during selective epitaxial growth and is uniformly doped. The mobility μ_{rsd} is calculated using Masetti's model [80] as function of N_{rsd}. The contact resistance component is given by

$$\Delta R_c = \frac{\rho_c}{\Delta x \cdot W_{rsd}} \tag{4.6}$$

where ρ_c is the specific contact resistivity in units of $\Omega - cm^2$.

Equations (4.4) and (4.6) are valid only for rectangular contacts. To generalize it to any contact shape and multi-fin devices, we express them in terms of the raised source/drain cross sectional area and the interface peripheral length:

$$\begin{cases} \Delta R_s = \rho \cdot \dfrac{\Delta x}{A_{rsd,total}} \\ \Delta R_c = \dfrac{\rho_c}{\Delta x \cdot P_{rsd,total}} \end{cases} \tag{4.7}$$

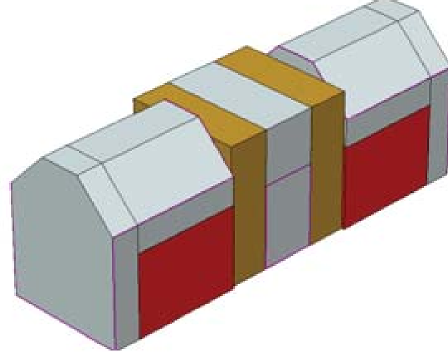


Figure 4.7: FinFET with a non-rectangular epi and silicide on top and two ends. This figure is a simulation structure in Sentaurus TCAD[79].

The transmission line model (TML) [81] is applied to solve this problem. By solving a differential equation we obtain the total contact resistance:

$$R_{con} = \rho \cdot \frac{L_T}{A_{rsd,total}} \cdot \frac{\eta \cdot \cosh(\alpha) + \sinh(\alpha)}{\eta \cdot \sinh(\alpha) + \cosh(\alpha)} \tag{4.8}$$

where

$$L_T = \sqrt{\frac{\rho_c \cdot A_{rsd,total}}{\rho \cdot P_{rsd,total}}} \tag{4.9}$$

$$\alpha = \frac{L_{rsd}}{L_T} \tag{4.10}$$

$$\eta = \frac{\rho_c \cdot A_{rsd,total}}{\rho \cdot L_T \cdot A_{term}} \tag{4.11}$$

A_{term} is the silicon/silicide area at the two ends of the FinFET for a structure like Fig. 4.7. A special case is for a FinFET without the end contacts, so that $A_{term} = 0$. Equation (4.8) reduces to

$$R_{con} = \rho \cdot \frac{L_T}{A_{rsd,total}} \cdot \coth(\alpha) \tag{4.12}$$

Note that Equation (4.12) is similar to but more general compared to the contact resistance formula in [73] and [74], since it can model non-rectangular raised source/drain cross sectional geometry.

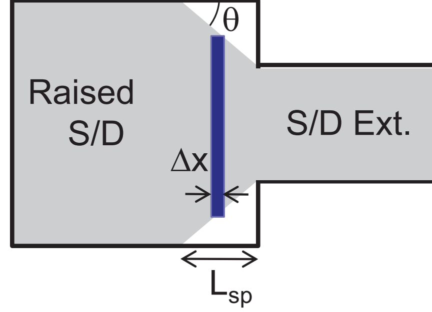


Figure 4.8: Illustration of current spreading from the source/drain extension region into the raised source/drain region

4.2.2 Spreading Resistance

When current flows from the source/drain extension region into the raised source/drain region, it spreads out gradually. This results in an increase in total resistance. We model this resistance increase as a new component, the spreading resistance. In some articles this spreading phenomenon is also called current crowding.

The top view of the raised source/drain and extension regions is shown in Fig. 4.8, with the gray area representing the region through which the current flows. We assume a constant spreading angle θ in order to obtain a closed form expression for spreading resistance.

We first consider a case where the cross sections of the extension and the raised source/drain are both squares. In between, each current flow cross section is also a square. We assume the side length of the squares increase linearly with position. Consequently each slice in the spreading region with thickness Δx has resistance of

$$\Delta R = \frac{\rho \cdot \Delta x}{\left(\sqrt{A_{fin}} + 2 \cdot x \cdot \tan\theta\right)^2} \tag{4.13}$$

where A_{fin} is the cross sectional area of the fin extension, which is

$$A_{fin} = H_{fin} \cdot T_{fin} \tag{4.14}$$

. The resistance in the spreading resistance is given by an integral from 0 to L_1:

$$R = \int_0^{L_1} \frac{\rho \cdot dx}{\left(\sqrt{A_{fin}} + 2 \cdot x \cdot \tan\theta\right)^2} \tag{4.15}$$

where L_1 satisfies the following relation:

$$2 \cdot L_1 \cdot \tan\theta = \sqrt{A_{rsd}} - \sqrt{A_{fin}} \tag{4.16}$$

. After carrying out the integration, we obtain the total resistance in the spreading region

$$R = \frac{\rho \cdot \cot\theta}{2}\left(\frac{1}{\sqrt{A_{fin}}} - \frac{1}{\sqrt{A_{rsd}}}\right) \tag{4.17}$$

If we carry out the same analysis for a circular-shaped fin extension and a circular-shaped raised source/drain, we will obtain a similar result

$$R = \frac{\rho \cdot \cot\theta}{\sqrt{\pi}}\left(\frac{1}{\sqrt{A_{fin}}} - \frac{1}{\sqrt{A_{rsd}}}\right) \tag{4.18}$$

. To be more general we express the resistance in the spreading region as

$$R = \frac{\rho \cdot \cot\theta}{s}\left(\frac{1}{\sqrt{A_{fin}}} - \frac{1}{\sqrt{A_{rsd}}}\right) \tag{4.19}$$

where the shape parameter, s depends on the shape of the fin extension and the raised source/drain.

We can also calculate R', the total resistance in the same region if there were no spreading.

$$R' = \frac{\rho \cdot L_1}{A_{rsd}} = \frac{\rho \cdot \cot\theta}{s \cdot A_{rsd}}\left(\sqrt{A_{rsd}} - \sqrt{A_{fin}}\right) \tag{4.20}$$

Since the spreading resistance is defined as the increase in resistance, it is the difference between R and R', which is

$$R_{sp} = \frac{\rho \cdot \cot\theta}{s} \cdot \left(\frac{1}{\sqrt{A_{fin}}} - \frac{2}{\sqrt{A_{rsd}}} + \frac{\sqrt{A_{fin}}}{A_{rsd}}\right) \tag{4.21}$$

We define

$$R_0 = \rho\left[\frac{1}{\sqrt{A_{fin}}} - \frac{2}{\sqrt{A_{rsd}}} + \frac{\sqrt{A_{fin}}}{A_{rsd}}\right] \tag{4.22}$$

and let

$$R_{sp} = K \cdot R_0 \tag{4.23}$$

where the slope factor K is

$$K = \frac{\cot\theta}{s} \tag{4.24}$$

. We hypothesize that K is insensitive to the device geometry in the range we are interested in.

To test the hypothesis, three-dimensional TCAD simulations are performed to compute R_{sp}. We simulate test structures that consist of a uniformly-doped silicon block with contacts

on both sides, as illustrated in Fig. 4.9(a). The specific contact resistivity is set to a very small value so that its effect is negligible[2]. The doping concentration is set to $N_{sd} = 2 \times 10^{20} cm^{-3}$. The dimension of the left-side contact is fixed at $H_{rsd} = 60nm$ and $W_{rsd} = 45nm$. The height of the right-side contact varies from $H_{fin} = 30nm$ to $H_{fin} = 60nm$ in steps of $5nm$, and the width varies simultaneously from $T_{fin} = 15nm$ to $T_{fin} = 45nm$ in steps of $5nm$. For each case five different raised source/drain length, L_{rsd} are simulated. The spreading resistance is extracted subtracting out the resistance of the non-spreading case. The non-spreading case is when $W_{rsd} = T_{fin}$ and $H_{rsd} = H_{fin}$.

In Fig. 4.9(b) we plotted the spreading resistance versus R_0. We also fitted Equation (4.23) to data. The best fit is obtained at $K = 0.7$. The model and data agree reasonably well, suggesting that the constant-K is a valid assumption.

4.2.3 Extension Resistance

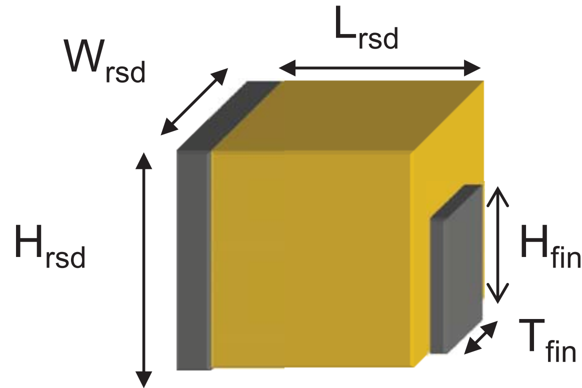
By extension resistance (R_{ext}) we are referring to the resistance in the fin extension region under the spacer. The modeling of extension resistance is quite complex. It requires knowledge of the doping profile in the extension region, which is often not accurately known in a real production environment. The profile shape may vary from process to process. In addition, the physical picture is complicated by surface accumulation due to the fringe field originating from the gate, which results in bias dependence.

To simplify the problem, we make several assumptions about the spacer configuration and doping profile, as illustrated in Fig. 4.10. In the figure, the gate and spacers are qualitatively sketched and horizontally aligned to the doping profile plot. We assume the spacer (with length L_{sp}) consists of two parts: an offset spacer (with length L_{off}) and a main spacer. Implantation of the extension doping is performed after the offset spacer is deposited but before the main spacer forms. As a result, the doping is horizontally uniform under the main spacer, but starts decaying with a Gaussian profile under the offset spacer. N_{ext} is the doping concentration at the boundary of the region under the offset spacer and the region under the main spacer.

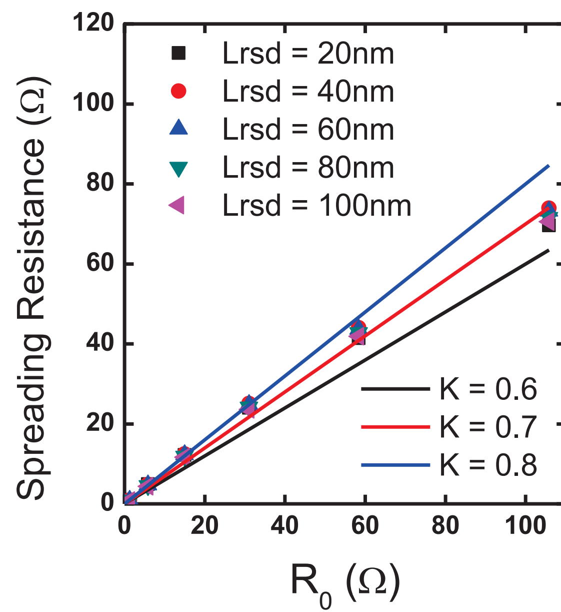
The extension resistance is modeled in one bias-dependent accumulation resistance component and two bias-independent bulk resistance components, and combined into a resistance network as shown in Fig. 4.11.

The accumulation resistance (R_{acc}) represents the conductive path at the surface of the source/drain extension due to charge accumulation induced by the gate fringe fields [73]. The accumulation resistance is significant and needs to be properly considered, especially for devices with little or no source/drain to gate overlap and have a relatively small doping concentration at the gate edge. The accumulation resistance is modeled using the following

[2] ρ_c is set to $10^{-12}\Omega - cm$ in TCAD simulation. In Sentaurus TCAD we are not allowed to set ρ_c to zero.



(a)



(b)

Figure 4.9: Extraction of spreading resistance: (a) Drawing of the test structure and (b) Plot for extracting the slope factor, K.

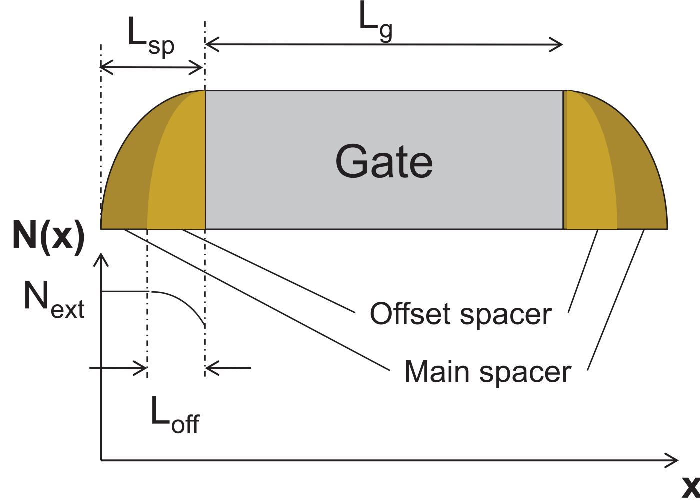


Figure 4.10: Doping profile and spacer configurations considered for R_{ext} modeling.

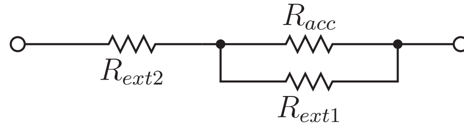


Figure 4.11: Sub-circuit for resistance modeling in the accumulation region

expression:

$$R_{acc} = \frac{R_{acc0}}{H_{fin} \cdot (V_{gs(d)} - V_{fbsd})} \tag{4.25}$$

where V_{fbsd} is the flatband voltage at the source and drain. The accumulation resistance is inversely proportional to the conduction charge density, which is proportional to $V_{gs(d)} - V_{fbsd}$.

The bulk resistance of the fin extension is modeled in two separate components: R_{ext1} and R_{ext2}. R_{ext1} represents the bulk resistance of the fin beneath the accumulated part of the source/drain. We assume it is partially under the offset spacer and partially under the main spacer. R_{ext1} is given by

$$R_{ext1} = \frac{R_{ext1,0}}{H_{fin} T_{fin}} \tag{4.26}$$

We have lumped the complex doping profile and mobility change due to doping into the variable $R_{ext1,0}$.

Further away from the gate, there is no accumulation at the surface but only conductivity

in the bulk of the fin. We model it with the following expression:

$$R_{ext2} = \frac{R_{ext2,0} \cdot (L_{sp} - \Delta L_{ext})}{H_{fin} T_{fin}} \tag{4.27}$$

, where we have assumed R_{ext2} is located under the main spacer where the doping is horizontally uniform.

After combining the three resistance components into a network as shown in Fig. 4.11, we obtain the full expression for extension resistance:

$$R_{ext} = \left(\frac{R_{acc0}}{H_{fin}(V_{gs(d)} - V_{fbsd})} \right) \parallel \left(\frac{R_{ext1,0}}{H_{fin} T_{fin}} \right) + \frac{R_{ext2,0} \cdot (L_{sp} - \Delta L_{ext})}{H_{fin} T_{fin}} \tag{4.28}$$

The above equation can be simplified to

$$R_{ext} = \frac{\frac{R_{ext1,0}}{H_{fin} T_{fin}}}{1 + \frac{R_{ext1,0}}{T_{fin} R_{acc0}} \cdot (V_{gs(d)} - V_{fbsd})} + \frac{R_{ext2,0} \cdot (L_{sp} - \Delta L_{ext})}{H_{fin} T_{fin}} \tag{4.29}$$

, which, interestingly, turns out to have the same bias dependence as the BSIM4 model [22] [3]:

$$Rs = \frac{1}{W_{eff}} \left[\frac{RSW}{1 + PRWG \cdot (V_{gs} - V_{fbsd})} + RSWMIN \right] \tag{4.30a}$$

$$Rd = \frac{1}{W_{eff}} \left[\frac{RDW}{1 + PRWG \cdot (V_{gd} - V_{fbsd})} + RDWMIN \right] \tag{4.30b}$$

Although not formally documented, surface accumulation in planar MOSFET could be the physical origin of Equation (4.30a).

Its worth noting that so far we have ignored the effect of the gate voltage dependence of the effective channel length (L_{eff}) on R_{ds}. Later on we will show by TCAD simulations that such effect is usually negligible.

4.3 Verification

In this section, verification of the model with three dimensional TCAD simulation will be presented. The details of the TCAD simulation setup, the separation of bias-dependent and bias-independent source/drain resistances, and the comparison of model versus TCAD simulation will be discussed. In addition, we will present our findings that traditional slope-intercept method overestimates L_{eff}, and the physical L_{eff} must be extracted by other means.

[3] $PRWB$ is set to 0. We consider the case when $RDSMOD = 1$, which activates the external resistance model,

4.3.1 TCAD Simulation Setup

Three dimensional numerical simulations of the FinFET is carried out using Sentaurus tools. In this section the details of the simulation setup is presented.

The simulation grid is created with Sentaurus Structure Editor [82] and mesh generation program Noffset3D [83]. A bird eye view of the FinFET simulation structure is shown in Fig. 4.12. Due to symmetry, only one half of the FinFET needs to be simulated. This reduces the total number of grid points by half and speeds up the simulation with no change in accuracy. The spacer is intentionally made transparent to show the fin extension region. The raised source/drain is wrapped around by silicide. In other words, the top and sides of the raised source/drain, as well as the end planes, which has a normal vector in the source-to-drain direction, are in contact with silicide. With a hard mask on top of the fin, the structure is a double-gate FinFET. Moreover, the device is situated on top of the buried oxide, therefore it is an SOI FinFET. The nominal geometry considered in this study is a linearly scaled version of that of a manufacturable FinFET technology [84]. Table 4.2 lists the nominal FinFET geometry and other simulation parameters used for TCAD simulation.

The current-voltage characteristics is simulated using Sentaurus Device [79] with the drift-diffusion model in Sentaurus Device. Doping-dependent mobility is modeled using the Masseti mode [80]. Mobility degradation at high vertical fields is accounted for with the Enhanced Lombardi Model [85, 79]. Velocity saturation is modeled using the Extended Canali Model [86, 79]. Quantum mechanical effects are not turned on in TCAD to avoid convergence issues. Since the main impact of quantum effects is an increase in inversion layer thickness, we lump the inversion layer thickness as part of the equivalent oxide thickness (EOT). The impact of quantum effects on the source/drain region is mainly the lowering of Schottky barrier height, and thus the specific contact resistivity (ρ_c) at the source/drain [87]. By specifying ρ_c directly rather than having Sentaurus Device calculate it, we avoid the pitfall of not taking Schottky barrier height lowering due to quantum effects into account. For the nominal case we set $\rho_c = 10^{-8}\,\Omega - cm$, as reported by ITRS [88] as the currently achievable value of specific contact resistivity. Lower contact resistivity values may be achievable [89, 87]. Since the analytical model we developed is scalable, it can model those low ρ_c values as well.

4.3.2 Device Optimization

We use metal gate in the simulation, and assume ideal threshold voltage (V_{th}) tuning through gate work function engineering is possible. We optimize the FinFET doping profile for maximum drive current (I_{on}) at a constant I_{off}/W_{eff} of $1nA/\mu m$ by altering the extension doping, N_{ext}, and the offset spacer width L_{off} (Fig. 4.13). For all extension doping concentrations, I_{on} versus L_{off} are bell-shaped curves. When the offset spacer is too thin, the extension doping encroaches into the channel and degrade the sub-threshold swing, forcing V_{th} to be very high for the same I_{off} and reducing I_{on}. On the other hand, when the offset spacer is too

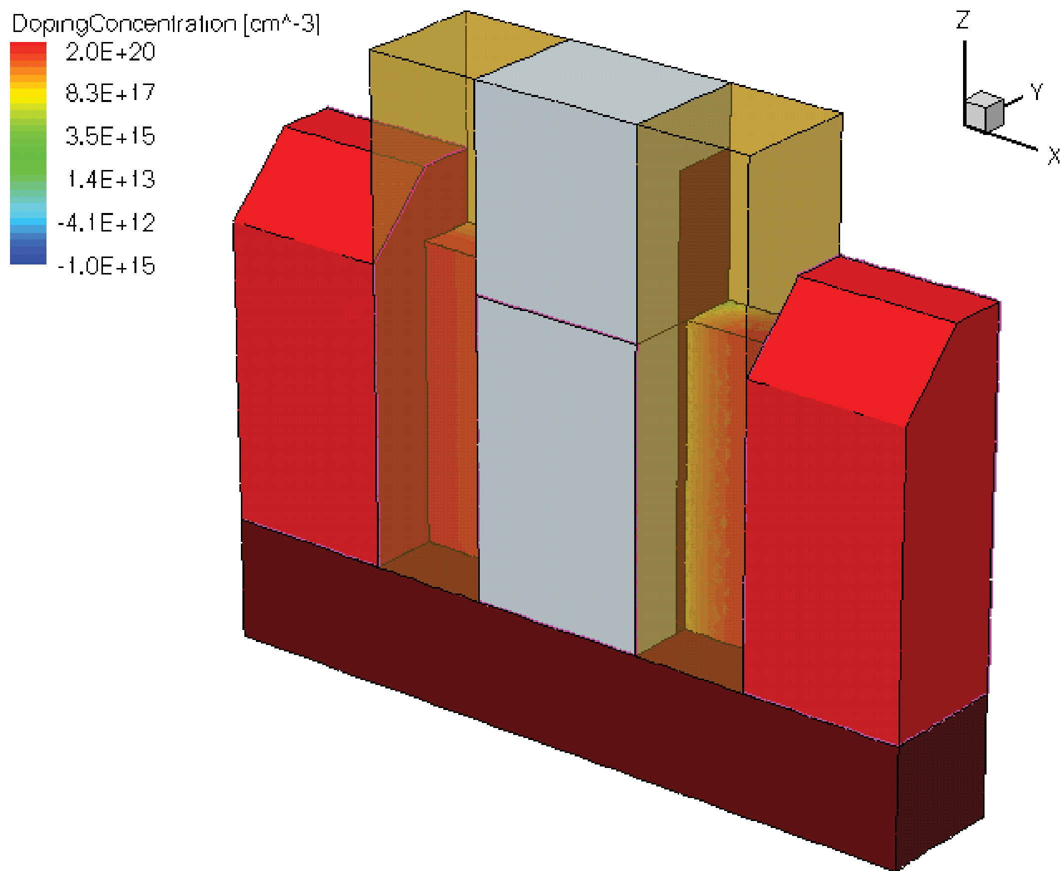


Figure 4.12: Bird-eye view of the FinFET structure for TCAD simulation displayed using Tecplot SV. The nitride spacer is intentionally made semi-transparent to make the fin extension visible.

Table 4.2: Nominal FinFET geometry and other simulation parameters used for TCAD simulation

Parameter Name	Description	Nominal Value
L_g	Physical Gate Length	$15\,nm$
EOT	Equivalent Oxide Thickness	$1.0\,nm$
T_{fin}	Fin Thickness	$10\,nm$
H_{fin}	Fin Height	$25\,nm$
H_{rsd}	Raised source/drain height	$31\,nm$
T_{mask}	Oxide hard mask thickness	$12\,nm$
L_{off}	Offset spacer width	$6\,nm$
L_{rsd}	Raised source/drain length	$14\,nm$
L_{sp}	Source/drain spacer width	$10\,nm$
T_{epi}	Horizontal epi thickness	$6\,nm$
N_{ext}	Source/drain extension doping	$2 \times 10^{20}\,cm^{-3}$
N_{rsd}	Raised source/drain epi doping	$2 \times 10^{20}\,cm^{-3}$
N_{body}	Fin body doping	$10^{15}\,cm^{-3}$
LDG	Lateral doping gradient in extension	$2.5\,nm/dec$
ρ_c	Contact resistivity	$10^{-8}\,\Omega - cm^2$
V_{dd}	Supply voltage	$0.9\,V$

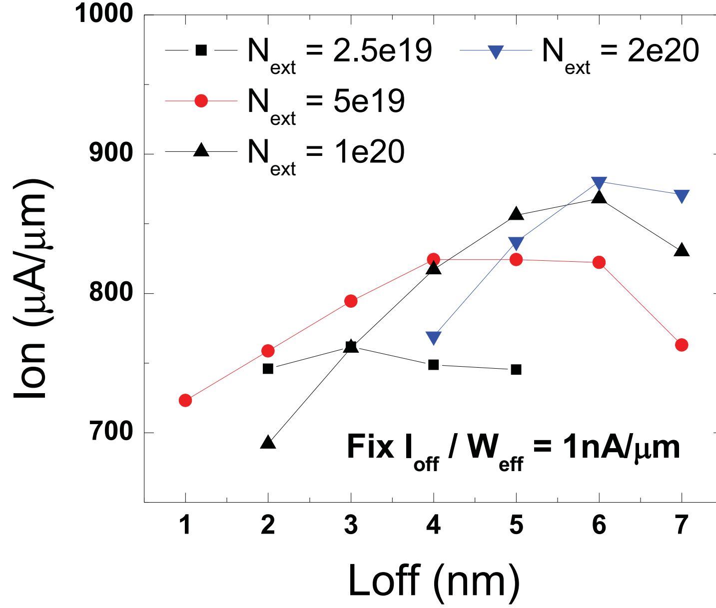


Figure 4.13: Optimization of the offset spacer width (L_{off}) and fin extension doping (N_{ext}) for maximum on current.

thick, the effective channel length becomes very large, the source/drain resistance becomes significant, and on current is degraded. Maximum I_{on} is achieved with $N_{ext} = 2 \times 10^{20} cm^{-3}$ and $L_{off} = 6nm$. The corresponding metal gate work function for $1nA/\mu m$ off current is $4.603\,eV$.

As we will show later, L_{eff} with to this offset spacer length ranges from about $16\,nm$ to $20\,nm$ for $V_{gs} < V_{dd}$. Therefore the optimal device has an underlapped source/drain design. The same conclusion was given in [90] and [91]. Note that we have assumed band-to-band tunneling leakage (or gate induced drain leakage) is small enough and its effect on I_{off} can be neglected.

4.3.3 Extraction of Source and Drain Resistances

Traditionally L_{eff} and the source/drain series resistance are extracted by plotting the channel resistance $R_{total} = V_{ds}/I_d$ versus the design gate length L_{des} at several gate overdrive values $V_{gs} - V_{th}$ at $V_{ds} = 50mV$ and finding their interception point [92]. There are two potential issues:

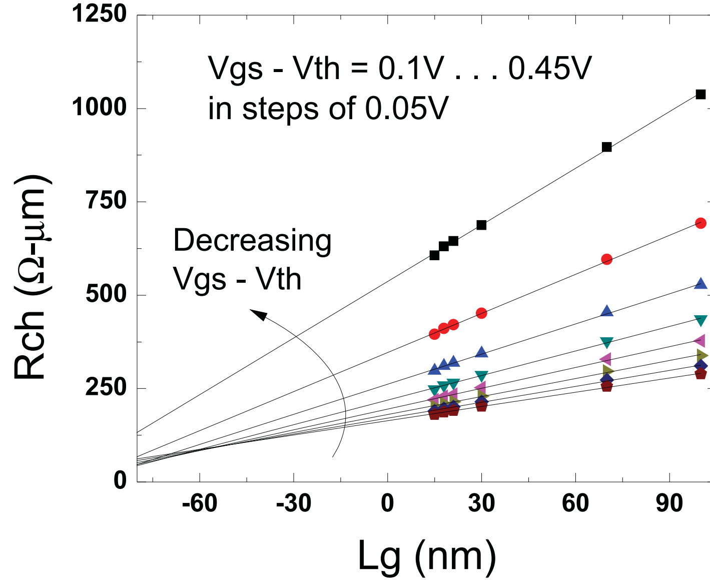


Figure 4.14: The total channel resistance R_{total} versus physical gate length L_g at several gate overdrive, $V_{gs} - V_{th}$, for the optimized device described in Section 4.3.2. V_{th} is obtained by extrapolating $I_d - V_{gs}$ at the point with maximum g_m.

1. The average channel mobility is a function of the gate length due to, for example, angled halo implant near the source/drain that suppresses sub-surface leakage current

2. The source/drain resistance is a function of gate bias

The former is less of an issue for fully-depleted FinFETs since halo implant is usually unnecessary for FinFETs. On the other hand, the source/drain resistance has significant bias-dependent since the conductivity of the fin extension near the gate edge is modulated by the gate fringe field. The bias dependence is expected to be more significant for devices with little or no source/drain overlap, as is the nominal case in this study. As a consequence, L_{eff} and R_{ds} extracted using the traditional method are likely quite different from their physical values. To illustrate this, we performed TCAD simulation for R_{total} versus L_g and fitted the results to linear curves (Fig. 4.14). The extrapolated curves intersect at approximately $L_g = -50nm$. If we had assumed there is no bias dependence, we would have concluded there is a $25nm$ underlap on each side, which is unlikely given the device structure we have. Moreover, the intersection point itself is a function of bias.

Table 4.3: Extraction of ΔL from TCAD

V_{gs} (V)	$V_{gs} - V_{th}$ (V)	X_{DC} nm	$n_e(X_{DC})$ cm^{-3}	L_{eff} nm	ΔL nm
0.45	0.042	2.43	5.85×10^{17}	15.88	-0.88
0.495	0.087	2.22	1.09×10^{18}	16.51	-1.51
0.54	0.132	1.99	1.81×10^{18}	16.98	-1.98
0.585	0.177	1.76	2.85×10^{18}	17.58	-2.58
0.63	0.222	1.55	4.21×10^{18}	18.02	-3.02
0.675	0.267	1.37	5.87×10^{18}	18.49	-3.49
0.72	0.312	1.22	7.76×10^{18}	18.84	-3.84
0.765	0.357	1.09	9.83×10^{18}	19.11	-4.11
0.81	0.402	0.99	1.21×10^{19}	19.35	-4.35
0.855	0.447	0.91	1.55×10^{19}	19.69	-4.69
0.9	0.492	0.83	1.93×10^{19}	20.08	-5.08

In this study an alternative method for source/drain resistance extraction is used. The total channel resistance is given by

$$R_{total}(V_{gs}) = R_{ds}(V_{gs}) + \frac{L_g - \Delta L(V_{gs})}{\mu C_{ox} W_{eff}(V_{gs} - V_{th} - \frac{V_{ds}}{2})V_{ds}} \tag{4.31}$$

While it is difficult to extract $R_{ds}(V_{gs})$ and $\Delta L(V_{gs})$ simultaneously, if $\Delta L(V_{gs})$ is know we can find $R_{ds}(V_{gs})$ as the zero crossing of the R_{total} versus L_g curve. $\Delta L(V_{gs})$, defined as the point at which the electron concentration at the inversion charge centroid is equal to the background doping, can be extracted from TCAD simulation. This extraction method is carried out and the results listed in Table 4.3.

L_{eff} is plotted versus gate overdrive, $V_{gs} - V_{th}$ in Fig. 4.15 for a 15nm device. For convenient usage we conduct a second order polynomial fit, which gives

$$L_{eff}(nm) = 15.34 + 14.06 \cdot V_{gt} - 9.42 \cdot V_{gt}^2 \tag{4.32}$$

, or,

$$\Delta L(nm) = 0.34 + 14.06 \cdot V_{gt} - 9.42 \cdot V_{gt}^2 \tag{4.33}$$

,

With this model of $\Delta L(V_g)$, we can now calculate $R_{ds}(V_g)$. Fig. 4.16 shows R_{ds} versus V_g for two cases. For one case, we apply Equation (4.33) and find the total source and

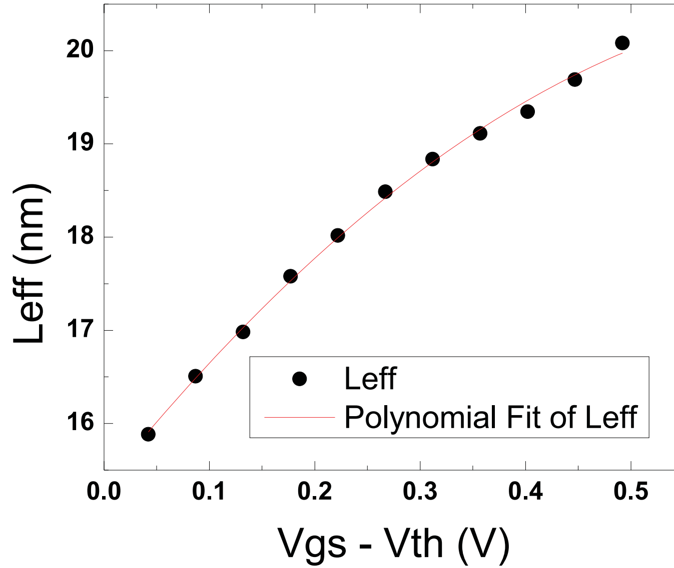


Figure 4.15: Effective channel length as function of gate overdrive

drain resistance at $L_g = \Delta L$. For another case, we assume $\Delta L = 0$. The result is similar, suggesting that the bias dependence of ΔL is not a significant factor for determining R_{ds}. From now on, we will extract the source/drain resistance using $\Delta L = 0$, which is perhaps more realistic since ΔL is not exactly know for experimental FinFETs.

In Section 4.2.3 we showed that the bias-dependent source/drain resistance is given in a form like Equation (4.30a). We further assume $RSW = RDW$ and $RSWMIN = RDWMIN$ for symmetry reasons and carry out fitting to obtain:

$$R_{ds}(\Omega - \mu m) = 107.5 + \frac{95.0}{1 + 7.54 \cdot (V_{gs} - V_{fbsd})} + \frac{95.0}{1 + 7.54 \cdot (V_{gd} - V_{fbsd})} \tag{4.34}$$

The above expression fits data very well from $V_{gs} - V_{th} = 0.1V$ to $V_{gs} - V_{th} = 4.2V$, suggesting the resistance network in Fig. 4.11 is a good description of the resistances in the extension region. The fitting is shown in Fig. 4.17, in which we emphasized the low V_{gs} part.

Parameters $R_{ext1,0}$ and $R_{acc,0}$ can be extracted from the bias dependent part of Equation (4.34). On the other hand, the bias independent part (with a value of 107.5) includes part of the extension resistance (R_{ext2}), the spreading resistance, and the contact resistance. The latter two do not have extra parameters to be determined, so parameters $R_{ext2,0}$ and ΔL_{ext} of R_{ext2} can be extracted by matching the bias independent part. We plot R_{ds} versus the spacer thickness (L_{sp}) and conducted a linear fit, as shown in Fig. 4.18. The model fits

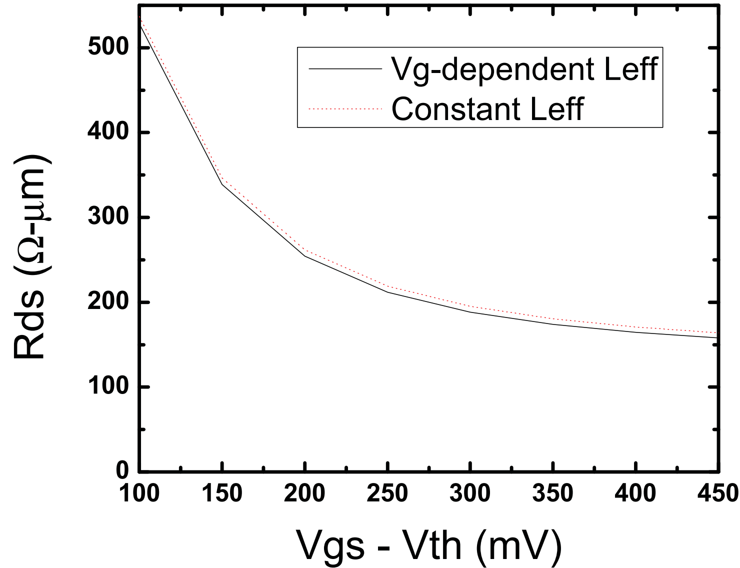


Figure 4.16: Source/drain resistance as function of gate overdrive

TCAD very well. The extracted model parameters are summarized in Table 4.4.

To verify Equation (4.8) we also plot the total source/drain resistance versus raised source/drain length (L_{rsd}) in Fig. 4.19. The model agrees with TCAD well without the need to introduce fitting parameter for the contact resistance.

4.4 Discussion

In Fig. 4.20, the individual resistance components are separately plotted. For our nominal case, assuming a specific contact resistivity of $10^{-8}\Omega - cm^2$, the extension resistance is much larger than the contact resistance even at $V_{gs} = V_{dd}$. This is possibly due to the underlapped source/drain design. A strong bias dependence (Fig. 4.17) suggests that at low V_{gs} the FinFET performance is degraded. To achieve minimum delay, optimizing I_{on} may not be the best strategy. A better strategy may be to optimize the effective current (I_{eff}) to consider low bias regions as well, which may likely result in more source/drain overlap.

Fig. 4.17 also suggests that the spreading resistance is a relatively small component. Therefore although the constant angle approximation is somewhat arbitrary, it may be sufficient for the purpose of FinFET source/drain resistance modeling. That also explains why a separate TCAD structure is needed for spreading resistance extraction: the spreading resis-

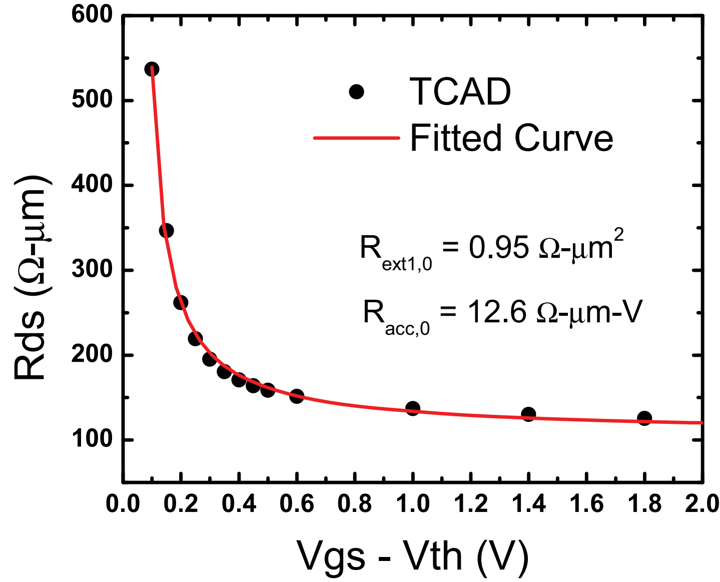


Figure 4.17: Source/drain resistance as function of gate overdrive ($V_{th} = 0.408V$)

Table 4.4: Summary of extracted parameters

Parameter Name	Value	Units
$R_{ext1,0}$	0.95	$\Omega - \mu m^2$
$R_{acc,0}$	12.6	$\Omega - \mu m \cdot V$
$R_{ext2,0}$	12.0	$\Omega - \mu m$
ΔL_{ext}	3.3	nm

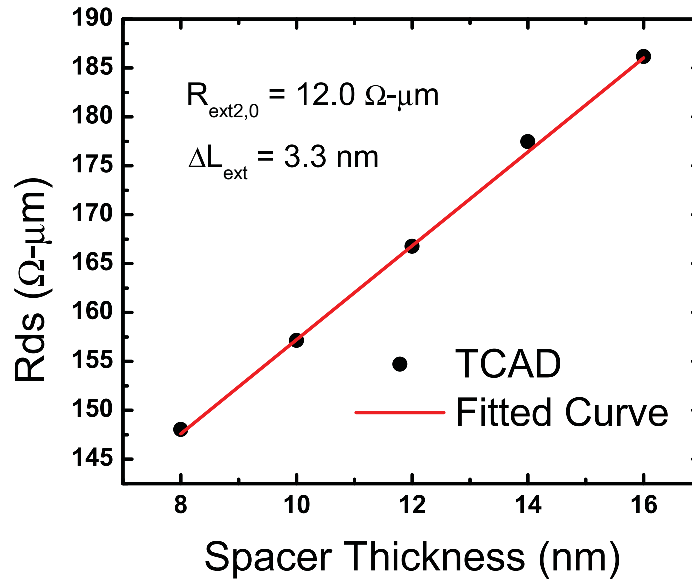


Figure 4.18: Source/drain resistance as function of spacer thickness at $V_{gs} = 0.9V$, $V_{ds} = 50mV$. The channel resistance has been subtracted out.

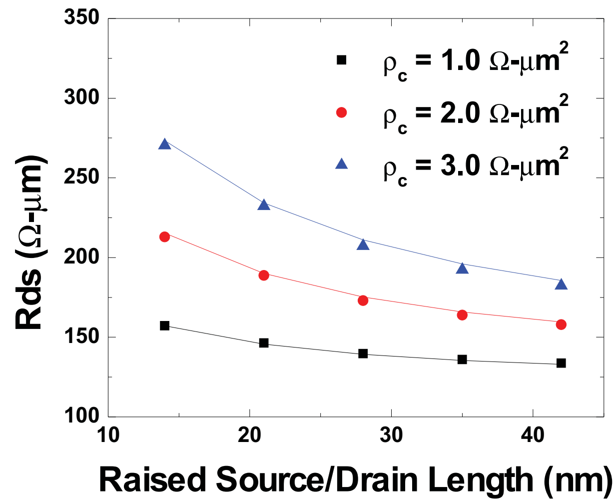


Figure 4.19: Source/drain resistance as function of raised source/drain length at $V_{gs} = 0.9V$, $V_{ds} = 50mV$. The channel resistance has been subtracted out.

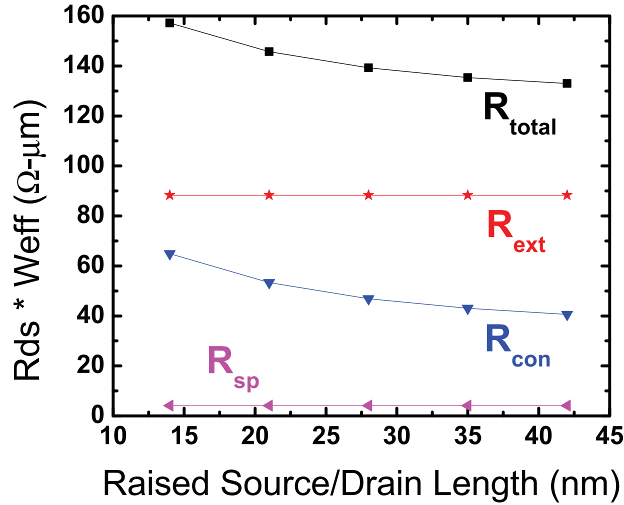


Figure 4.20: Breakdown of source/drain resistance into individual components: contact resistance (R_{con}), extension resistance (R_{ext}) and spreading resistance (R_{sp}).

tance is so small that it is difficult to separate from other components in a more sophisticated test structure.

The saturation of contact resistance at around $30nm$ suggests that further lengthening the source/drain may not be as useful. For the top-contact case, this conclusion may be changed. In practice, however, the raised source/drain length is likely determined based on process considerations.

4.5 Conclusion

We have developed a parasitic source/drain resistance for the FinFET structure with particular focus on the raised source/drain structure. Transmission-line based contact resistance model predicts the dependence on epi height, fin pitch, contact length, cross sectional shape of the epi, and many others, and models various different contact silicidation schemes. Spreading resistance and extension resistance expressions are also developed. The extension resistance exhibits bias dependence due to the fringe field originating from the gate. We have validated the model against TCAD. The extension resistance model is able to capture the gate bias dependence of R_{ds} well even for underlapped device where the resistance has strong bias dependence. After performing a breakdown to examine each individual components, it was found that the spreading resistance is negligibly small, and the extension and contact resistances are the dominant components.

Chapter 5

Compact Modeling of Variation in FinFET SRAM Cells

FinFET will be used in production CMOS soon. One important question is how the device variation will change with the shift in technology. In this chapter we present a compact model based study of FinFET variation. In particular, we focus on SRAM cells, as it is one of the most important circuit in modern chip design. We will show that the FinFET V_{th} distribution is non-Gaussian, and the physics-based BSIM-CMG model is able to capture that. [64][93]

5.1 Introduction

Power consumption of embedded SRAM is a significant concern in state-of-the-art processors. Lowering the supply voltage (V_{dd}) effectively saves power. However, V_{DD} scaling for conventional SRAM is limited by the random variation of the device threshold voltage (V_{th}), because of random dopant fluctuation (RDF) effects, which are expected to increase with technology scaling. On the other hand, high doping is not required for multi-gate devices such as FinFETs [14]. In such devices, V_{th} variation is smaller and V_{DD} can be scaled to lower voltages [84]. These devices will likely be used in future CMOS technologies. In the absence of RDF, variation in V_{th} will originate mainly from the lithography-defined gate length (L) and fin thickness (T_{fin}). It is crucial that these variation sources in multi-gate devices are modeled. Numerical simulations based on finite-element methods or TCAD (technology CAD) tools are useful for technology evaluation and design exploration of FinFET-based SRAM cells (see, for example, the work by Guo et al. [32]). Mixed-mode TCAD simulations can be combined with Monte Carlo simulations to predict the impact of device variation on circuit performance. Many simulations are needed, however, and such a task is time-consuming. An efficient compact model (or SPICE model) such as BSIM-CMG [25] is more suitable. The model employs physical expressions to capture the effect of device parameters

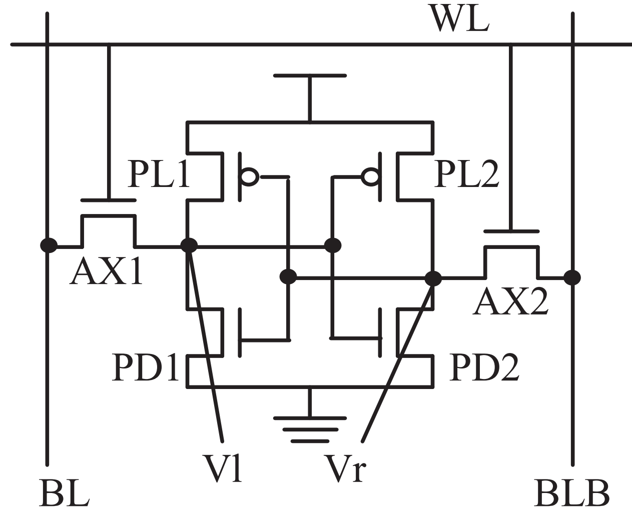


Figure 5.1: Schematic of the 6T SRAM cell (AX: access; PL: pFET load; PD: pull-down; Vl: left-node voltage; Vr: right-node voltage.)

such as L and T_{fin} on the electrical characteristics of multi-gate devices. Through proper parameter extraction, the effects of these variation sources can be captured. In this article, we present a procedure to model variation in FinFET SRAM cells using BSIM-CMG, which we used in a study for the design and optimization of a six-transistor (6T) FinFET SRAM cell. We review design considerations of FinFET SRAM cells and the advantages of multi-gate devices, and give a brief overview of BSIM-CMG. We explain the process of separating global and local variation components and of calibrating variation to data.

5.2 SRAM Design Considerations

Four design metrics quantify the read/write stability and performance of an SRAM cell (see Fig. 5.1):

A read static noise margin characterizes the read stability of the SRAM cell. The RSNM is defined as the side length of the maximum square that can fit inside the butterfly curve (see Fig. 5.2). We form a butterfly curve by plotting the voltage transfer characteristics of the two inverters in an SRAM cell when both the bit line (BL) and word line (WL) are biased at V_{DD}. If the two squares inside the butterfly curve do not have equal side lengths, we define RSNM as the side length of the smaller square.

A second metric, word-line write margin (WLWM), characterizes the cells write stability

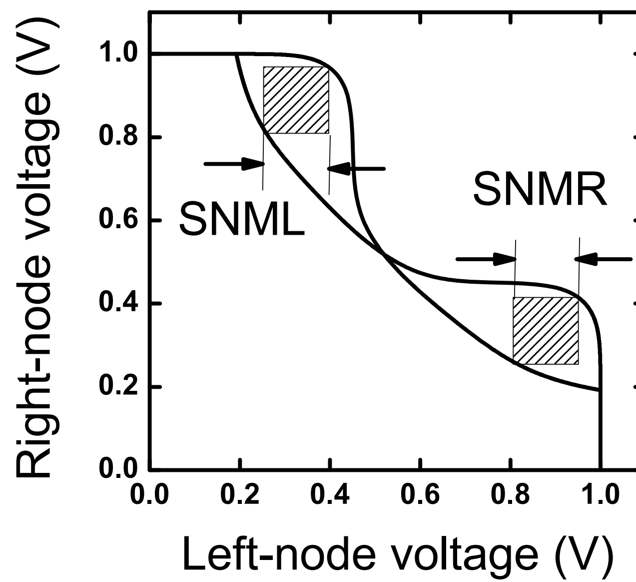


Figure 5.2: Definition of the read static noise margin: the smaller of the left static noise margin (SNML) and the right static noise margin (SNMR)

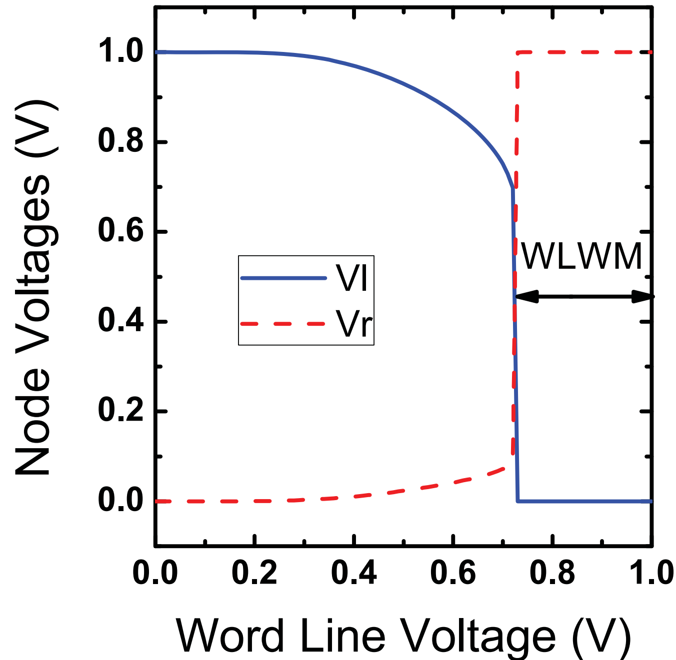


Figure 5.3: definition of word-line write margin (WLWM). The bit line (BL) is biased at 0 V, the $\overline{BL}$ is biased at 1.0 V, and the word line (WL) is swept from 0 V to 1.0 V to mimic a write operation. When the WL reaches $V_{DD} - WLWM$, the cell state is flipped.

[94]. A write operation in SRAM is typically carried out at a WL voltage of V_{DD}. WLWM is the maximum amount by which the WL voltage can be lower than V_{DD} and still allow a successful write (see Fig. 5.3).

A third metric is access time. During a read/write operation, the WL is raised only for a short period of time. The read/write access time is defined as the minimum time needed to carry out a successful read/write operation. The performance of the SRAM depends on the access time. The fourth metric to be considered is static leakage power. Even when both WL and BL are set to 0, the cells power consumption is finite due to the MOSFET leakage currents. Unlike the read/write margin and access time for which each cell must meet a given criterion, as far as static leakage power is concerned, we are more interested in the total power consumption of the SRAM array. Scaling V_{DD} will reduce total power consumption; however, the RSNM, WLWM, and access time metrics will be degraded if V_{DD} is lowered. This can be resolved by using FinFETs to replace conventional MOSFETs.

5.3 FinFET SRAM Advantages and Challenges

In the FinFET the electrostatic control is improved as a result of gate control from multiple sides of the fin. Short-channel effects such as subthreshold swing degradation, V_{th} roll-off with L, and drain-induced barrier lowering (DIBL) are improved. In addition, high doping that suppresses leakage paths in conventional MOSFETs is no longer required, because leakage is suppressed by the FinFETs thin body. In addition to these improvements, there are five consequences of SRAM stability and performance.

First, improved subthreshold swing leads to lower V_{th} for a given off-state leakage current. The onstate current per device width (W) is enhanced. For SRAM cells, the read and write access times are shortened. Second, V_{th} rolls off less rapidly with L. As a result, V_{th} variation is smaller for a given L variation. This leads to a lower V_{DD} and less power consumption. Third, in lightly doped multi-gate devices, RDF resulting from body doping becomes insignificant, further reducing V_{th} variation. Fourth, a smaller DIBL effect leads to a smaller output conductance ($\frac{dI_D}{d_{V_{DS}}}$) in the saturation region, which leads to sharper voltage transfer characteristics. This will improve the read static noise margin of SRAM cells.

Finally, unlike conventional MOSFET devices, where the value of W can lie in a continuous interval, the effective width (W_{eff}) of multi-gate devices can have only discrete values. The FinFETs W_{eff} is typically defined as

$$W_{eff} = N_{fin} \cdot (2H_{fin} + T_{fin}) \tag{5.1}$$

where N_{fin} is the total number of fins, H_{fin} is the fin height, and T_{fin} is the fin thickness. H_{fin} and T_{fin} are usually fixed for a given technology. N_{fin} can have only integer values. This might not seriously affect logic devices in which W_{eff} is large, but it could limit the design space for circuits, such as SRAM cells, that include small devices. Given that tuning of W_{eff} is limited, the optimization of L might be needed for SRAM cell design.

5.4 Modeling V_{th} Variation due to Gate Length and Fin Thickness Variation

Modeling multigate devices and predicting the performance of circuits requires a compact model. We use BSIM-CMG for this purpose.

The most important variation sources in a FinFET are L and T_{fin}, which influence device V_{th} through short-channel effects. In BSIM-CMG, the following expression models V_{th} roll-off and DIBL [95]:

$$\Delta V_{TH} = \frac{-0.5 \cdot DVT0}{\cosh\left(DVT1 \cdot \frac{L}{\lambda}\right) - 1} \cdot (V_{bi} - \phi_s) + \frac{-0.5 \cdot ETA0}{\cosh\left(DSUB \cdot \frac{L}{\lambda}\right) - 1} \cdot V_{DS} \tag{5.2}$$

where V_{bi} is the built-in potential of the source-to-body junction; ϕ_s is the surface potential in strong inversion; DVT0, DVT1, ETA0, and DSUB are fitting parameters. The first term

models V_{th} roll-off with decreasing L at low drain bias (V_{DS}); the second term models V_{th} reduction with increasing V_{DS} due to DIBL. λ is the scale length for the FinFET and has been given by Lin [96] as follows:

$$\lambda = \frac{0.5}{\sqrt{\frac{1}{\frac{\epsilon_{si}}{2\epsilon_{ox}}\left(1+\frac{\epsilon_{ox}T_{fin}}{4\epsilon_{si}T_{ox}}\right)T_{fin}T_{ox}} + \frac{1}{4{H_{eff}}^2}}} \tag{5.3}$$

where

$$H_{eff} = \sqrt{\frac{H_{fin}}{8}\left(H_{fin} + 2\frac{\epsilon_{si}}{\epsilon_{ox}}T_{ox}\right)} \tag{5.4}$$

H_{fin} is the height of the fin, T_{ox} is the oxide thickness, and ϵ_{si} and ϵ_{ox} are the dielectric constants of silicon and oxide. In addition, the on-state current, gate capacitance, gate-induced drain leakage current, and output conductance depend on physical parameters such as L, T_{fin}, H_{fin}, and T_{ox}. These effects are considered in BSIM-CMG as well.

5.5 Modeling Variation in SRAM Cells

Device variation is often separated into local and global components [97, 98]. Local variations of individual transistors within the SRAM cell are uncorrelated — the transistors vary independently of one another. On the other hand, global variations of cell transistors are fully correlated — all transistors vary at the same time.

Monte Carlo simulations are useful for extracting a statistical distribution of design metrics, as in our study. To consider local and global variation at the same time, each model parameter (such as H_{fin}, T_{fin}, L, or T_{ox}), which we denote P, is calculated using the following expression:

$$P_{ij} = P_{nominal} + \Delta P_{Global,j} + \Delta P_{Local,ij} \tag{5.5}$$

P_{ij} denotes the parameter value for the ith transistor during the jth Monte Carlo run. $P_{nominal}$ is a fixed nominal component. The global variation component $\Delta P_{Global,j}$ is generated for each Monte Carlo run and applied to all transistors in the SRAM cell. The local variation component $\Delta P_{Local,ij}$ is generated for each transistor for each Monte Carlo run. Both $\Delta P_{Global,j}$ and $\Delta P_{Local,ij}$ follow a Gaussian distribution.

A distinct FinFET characteristic is the discrete number of fins (N_{fin}). The conventional way to model a multiple-fin device is to multiply the drain current and charge of a single-fin device by N_{fin}. However, this implicitly assumes that the variations of the multiple fins are fully correlated with one another. To properly capture local variation, multiple-fin devices should be modeled with multiple single-fin instances instead. Each instance is given its own local variation component.

5.6 Statistical Design Procedure for FinFET SRAMs

The conventional circuit design strategy focuses on the nominal case. Variability-aware simulation is performed only at the final stage of the design to correct possible parametric or functional failures in the worst-case scenario. However, as the amount of variation increases with technology scaling, a variability aware design strategy is needed.

Fig. 5.4 shows a variation-aware design procedure for FinFET SRAM cells. Known physical parameters, such as the dimensions of the FinFET, are provided to the model. Other nominal model parameters for BSIM-CMG are extracted from current-voltage and capacitance-voltage measurements of stand-alone FinFET devices. One parameter set is extracted for the L range of interest without using parameter binning [21]. Global variation is determined from either process information (e.g., film thickness distribution) or, if available, electrical measurements of variation (e.g., oxide capacitance distribution). Local variation is extracted by calibrating a Monte Carlo simulation to electrical measurements. Both global and local variations are included in Monte Carlo using Equation 5.5. Local variation is adjusted so that the simulated distributions agree with the measurements. A more detailed description of the Monte Carlo Simulation Procedure is given in Appendix B.

The SRAM cell is optimized for two cases: $NF_{PD} = 1$ and $NF_{PD} = 2$, where NF_{PD} is the number of fins of the pull-down devices. The number of fins for all the other devices is fixed to 1. Conventional SRAM has an optimal β of around 1.5, where β is the ratio of the pull-down devices W_{eff} to that of the access device. Therefore, for an SRAM cell with a 1-fin access device, either $NF_{PD} = 1$ or $NF_{PD} = 2$ can be optimal. The strength of the pFET load must be weaker than the access nFET. Because pFETs are generally weaker than nFETs, a 1-fin device is usually sufficient. Although the effect of surface orientation and strain could result in more-symmetric nFET and pFET mobility, upsizing the access device would necessitate also upsizing the pulldown device, and this would require too much area.

The cell is optimized on the basis of two criteria

- V_{DD} must be low enough that the total power consumption meets the specification.
- RSNM, WLWM, and access time must satisfy the criterion $\mu - Z\sigma > 0$ (where μ is the mean, σ is the standard deviation, and Z is an empirical constant, which depends on the SRAM array size and typically ranges from 5 to 6), so that the cell failure probability is sufficiently low.

In the second criterion, both μ and are extracted from a large number of Monte Carlo simulations. (In this study, 1,000 Monte Carlo simulations are performed for each μ and σ.) For design metrics whose distributions are not Gaussian, similar criteria can be derived from its cumulative distribution function. The parameters that characterize their distributions can be extracted from the Monte Carlo simulations using, for example, maximum likelihood estimation.

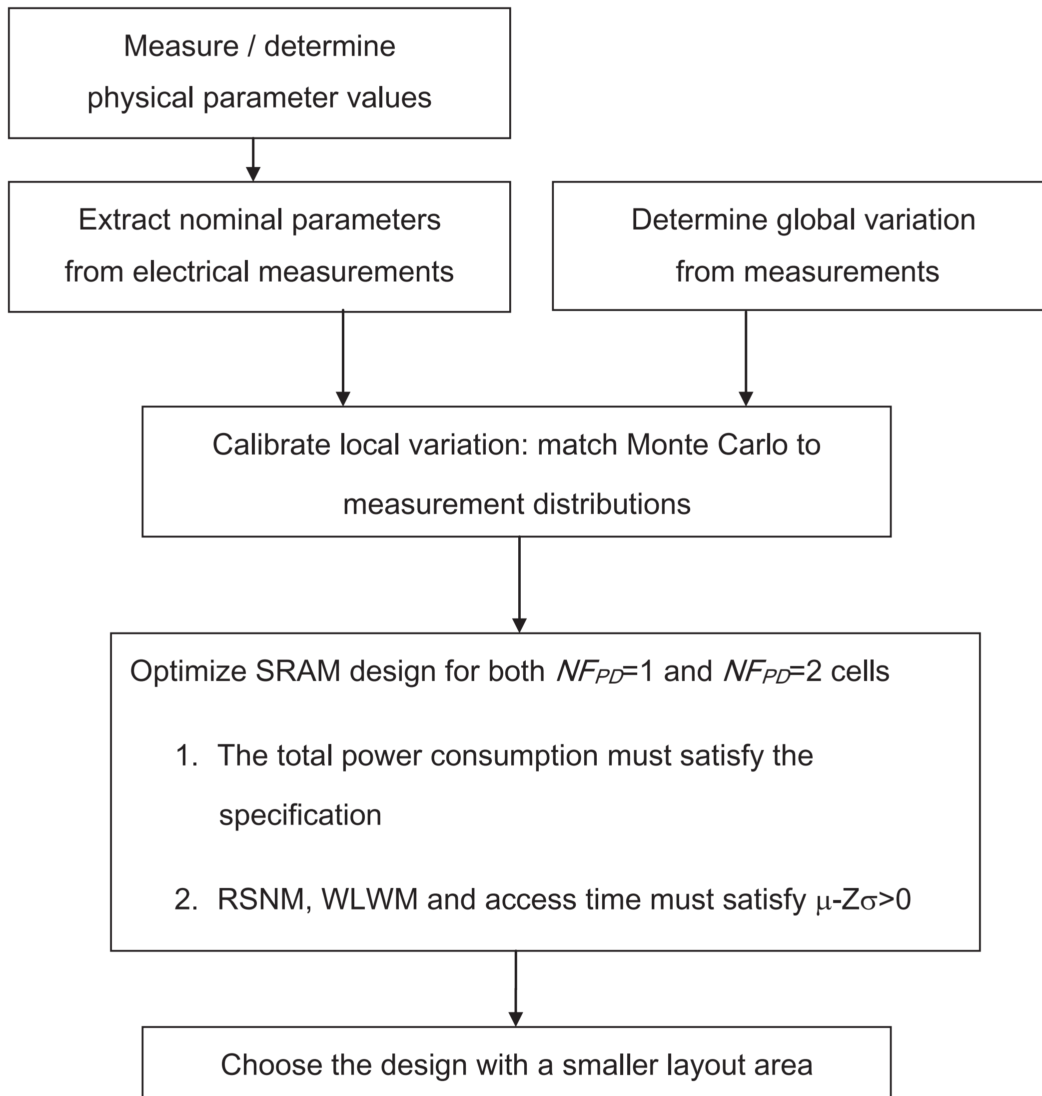


Figure 5.4: Variation-aware design procedure for FinFET SRAM cells.

Under the two constraints, the SRAM cell is optimized for minimal area (or minimal L for the devices). Both $NF_{PD} = 1$ and $NF_{PD} = 2$ cell layouts are drawn, and the one with the smaller area is chosen.

5.7 Experimental Verification

5.7.1 Device Fabrication

FinFETs with 60nm fin height (H_{fin}), 30nm fin width (T_{fin}), SiON gate dielectric with $1.9nm$ equivalent oxide thickness (EOT), 10nm TiN gate and lightly-doped channels are fabricated on SOI wafers [99, 25, 11]. Both stand-alone FinFETs and 6T FinFET SRAM cells are fabricated. The stand-alone devices have 20 fins in parallel; The SRAM cells use single-fin or double-fin devices.

5.7.2 Nominal Parameter Extraction

The nominal parameters of BSIM-MG are extracted from I-V measurements of stand-alone FinFETs. One set of parameters is extracted from devices with L ranging from $75nm$ to $1\mu m$. As shown in Fig. 5.5, the drain current (I_d) versus gate voltage (V_{gs}) for p-type FinFETs in both linear (Fig. 5.5(a)) and saturation (Fig. 5.5(b)) modes are well-captured over the entire range of L.

5.7.3 Adjustment for SRAM FETs

FinFETs in SRAM cells and stand-alone FinFETs do not have identical physical dimensions and electrical characteristics due to the influence of neighboring patterns. To account for this, we simulate butterfly curves of the SRAM cell, compare it with measured ones, and adjust L to account for lithography variation. Fig. 5.6 shows the simulated and several measured butterfly curves on the same graph. The discrepancy of the uncorrected model may be caused by a modeled V_{th} value of the pull-down nFETs (PD1, PD2) that is too low. This difference is resolved through the correction of L (Table 5.1, Fig. 5.6). Since only half-cell measurement is available in this study, the butterfly curves are obtained by measuring one curve and mirroring.

5.7.4 Calibration of Variation

To model variation in SRAM cells, we consider physical parameters such as L, H_{fin}, T_{fin} and EOT. Each is assumed to follow a Gaussian distribution.

To determine the influence of RDF, we assumed that the number of dopants in the channel followed a Poisson distribution. The standard deviation of doping concentration

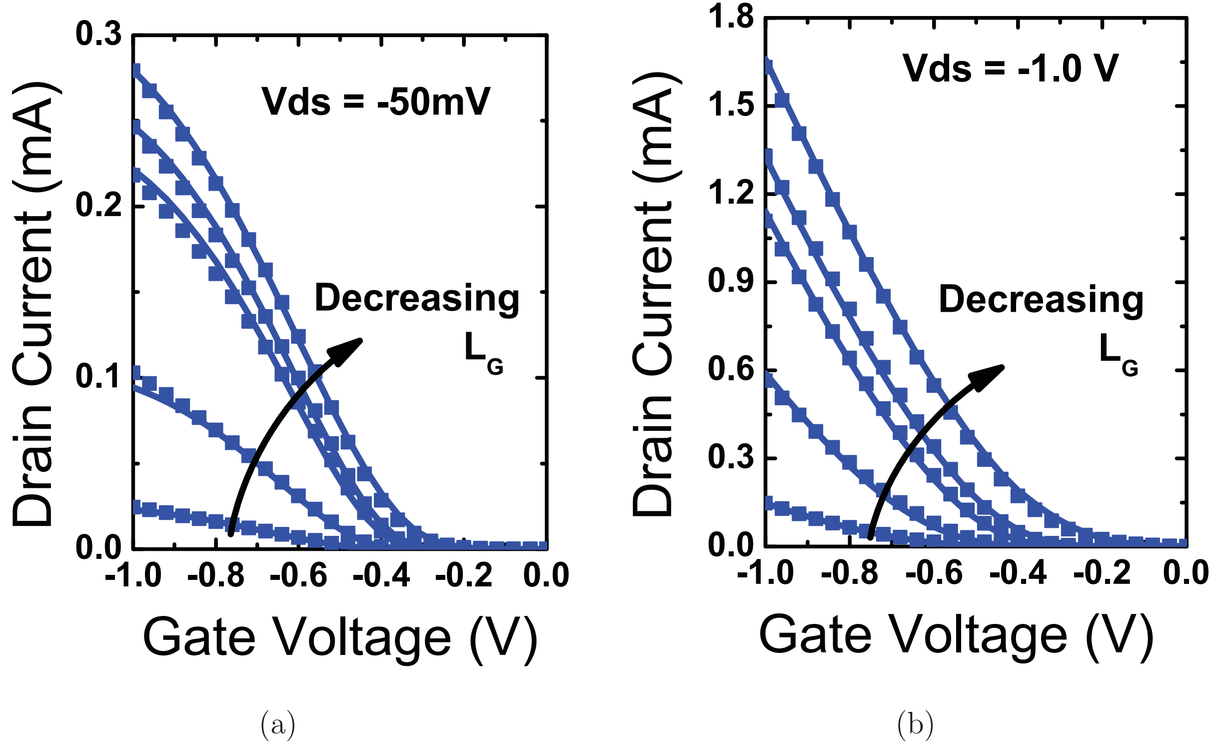


Figure 5.5: $I_d - V_{gs}$ for p-type FinFET devices at (a) $V_{ds} = -50mV$ and (b) $V_{ds} = -1.0V$. L=75nm, 85nm, 95nm, 235nm and 1μm. Model (lines) and measured data (symbols) agree well.

Table 5.1: Gate Length Correction

NF_{PD}	ΔL_{AX} (nm)	ΔL_{PD} (nm)	ΔL_{PL} (nm)
1	+10	+15	+20
2	+0	+20	+20

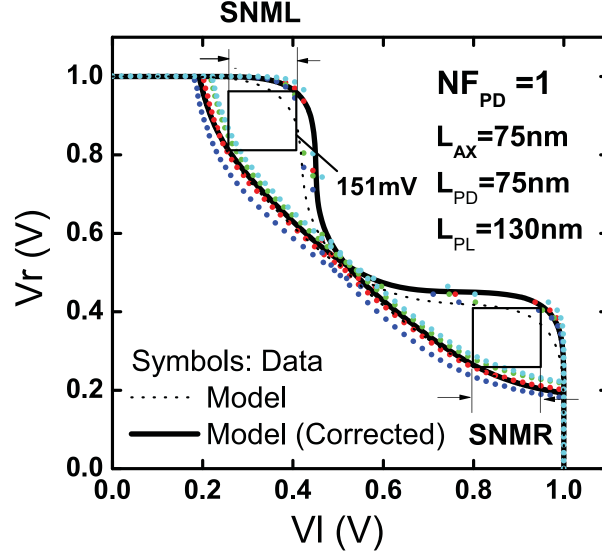


Figure 5.6: Simulated and several measured butterfly curves of SRAM cells. ($NF_{PD} = 1$).

due to RDF is

$$\sigma N_{ch} = \sqrt{\frac{N_{ch}}{LT_{fin}H_{fin}}} \tag{5.6}$$

With $L = 75nm$, $T_{fin} = 30nm$, $H_{fin} = 60nm$, and $N_{ch} = 2 \times 10^{15}cm^{-3}$, σN_{ch} is 3.8×10^{15}. The corresponding change in V_{th} is approximately

$$\Delta V_{TH} = \frac{qT_{fin}\Delta N_{ch}}{2C_{ox}} \approx 0.501mV \tag{5.7}$$

The influence of random dopants is extremely small. Therefore, in our experiment, we didnt consider RDF effects resulting from dopants in the lightly doped fin.

Global variation is assumed to be $3\sigma = 10\%$ of the nominal value for each parameter, where σ is the standard deviation. Local mismatch is determined by matching the Monte Carlo simulated read static noise margin (SNM) distribution to measurements.

Butterfly curves of 378 SRAM cells are measured. 189 of the SRAM cells have $NF_{PD} = 1$; the other 189 have $NF_{PD} = 2$. The read SNM of the cells are extracted from the butterfly curves using the conventional method. The 3σ value of local mismatch is found to be $3.1nm$ for T_{fin} and $12.6nm$ for L. We neglect the local variation in H_{fin} and EOT, whose values are not determined by lithography conditions. Fig. 5.7 shows the good agreement of Monte Carlo simulated read SNM distributions with measurements. A few SRAM cells show read SNM much lower than others (4 cells have 0V SNM).

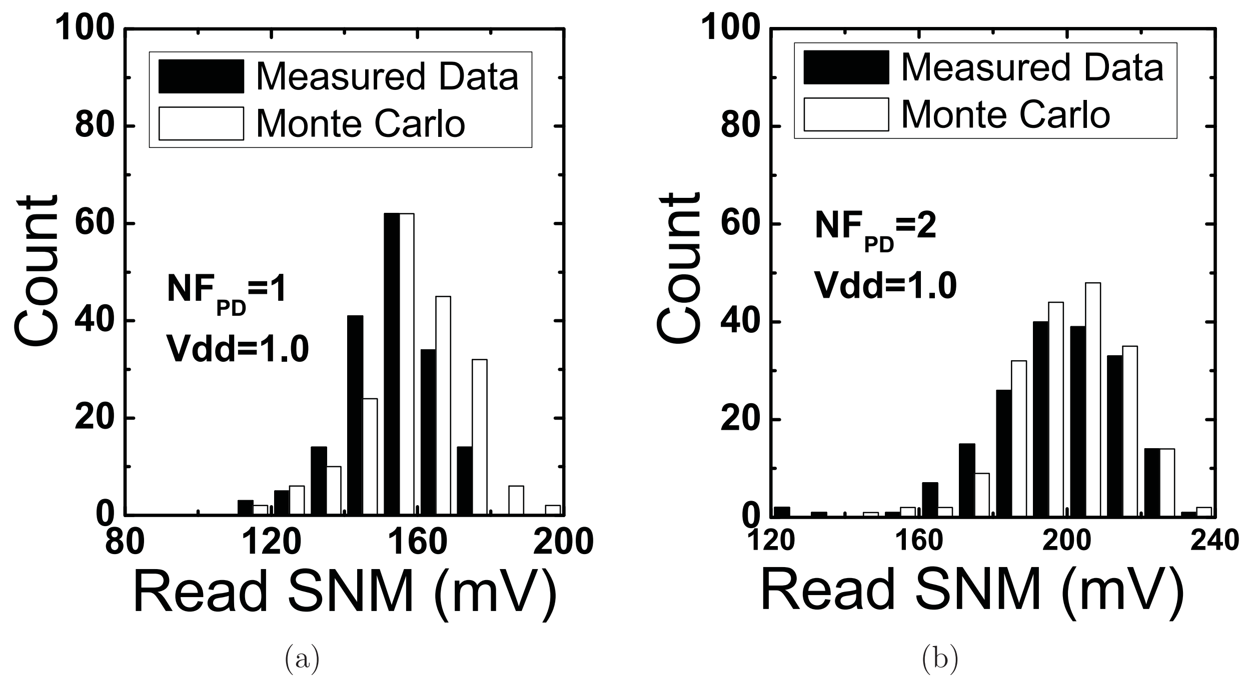


Figure 5.7: Read SNM distribution of SRAM cells with pull-down nFETs containing (a) 1 fin (b) 2 fins. ($V_{dd} = 1.0V$)

5.8 FinFET SRAM Cell Design Exercise

The gate length of each transistor and NF_{PD} are optimized under the constraint that both the read margin and the write margin must satisfy

$$p_{fail} < \Phi(-5.5) \approx 1.9 \times 10^{-8} \tag{5.8}$$

where p_{fail} is the read (write) failure probability of a given cell. $\Phi(x)$ is the cumulative distribution function of a standard Gaussian distribution.

5.8.1 Design Criterion for Read and Write Operations

The word line sweeping write margin (WLWM) follows a Gaussian distribution [98]. Therefore Equation (5.8) translates to the widely-used criterion for the mean (μ) and σ of WLWM:

$$\mu_{WLWM} - 5.5\sigma WLWM > 0 \tag{5.9}$$

Equation (5.9) is adopted as the design criterion for write operation. For read operation, both SNML and SNMR (defined in Fig. 5.6) are Gaussian but

$$readSNM = min(SNML, SNMR) \tag{5.10}$$

is not [98]. Therefore Equation (5.9) cannot be directly applied to the read SNM. However, we observe that

$$p_{fail} < \Phi(-5.5) = 1 - [1 - \Phi(-z)]^2 \tag{5.11}$$

where $\Phi(-z)$ is the probability that SNML is less than zero. Solving Equation (5.11), we obtain $z = 5.62$. Therefore we use

$$\mu_{SNML} - 5.62\sigma_{SNML} > 0 \tag{5.12}$$

as the design criterion for read operation.

5.8.2 Cell Optimization

We first study the effect of changing NF_{PD} and V_{dd}. NF_{PD} is varied from 1 to 3 at $V_{dd} = 0.8$ and $V_{dd} = 1.0$. 1000 Monte Carlo circuit simulations are performed for each combination of NF_{PD} and V_{dd} (Fig. 5.8). The strength of the pull-down nFET increases with NF_{PD}. Therefore with increasing NF_{PD}, $SNML$ is improved and $WLWM$ is slightly degraded. At $NF_{PD} = 1$, $SNML$ does not satisfy the design criterion given by Equation (5.12). However, this will be overcome through further optimization of L. V_{dd}=0.8 is chosen for low power operation.

Next L of the access transistor and the pFET load are optimized for the two cases: $NF_{PD} = 1$ and $NF_{PD} = 2$. $NF_{PD} = 3$ is not considered since both $SNML$ and $WLWM$

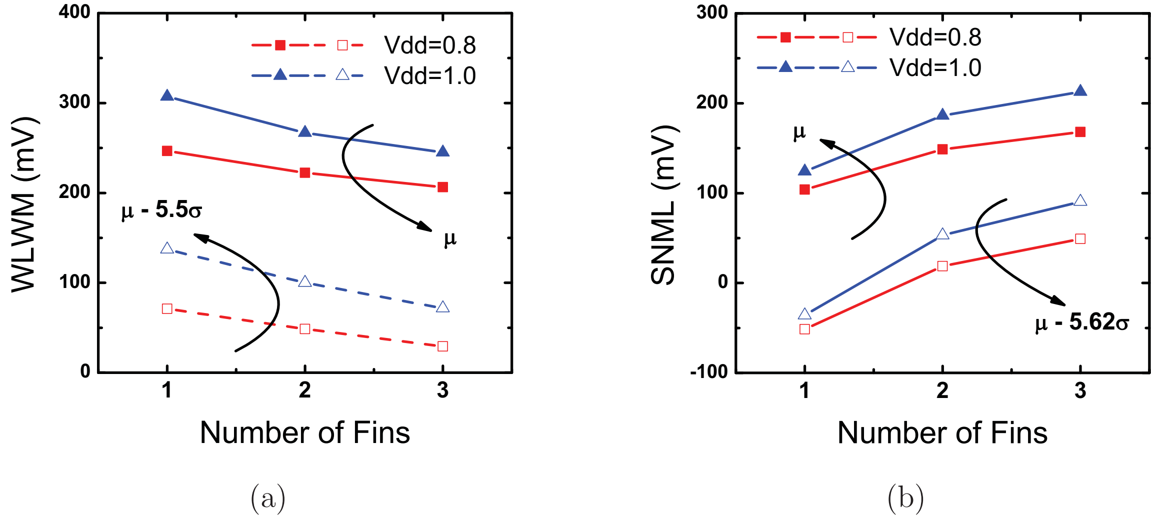


Figure 5.8: (a) Word line sweep write margin ($WLWM$) and (b) $SNML$ (defined in Fig. 5.6) versus fin number of pull-down nFETs for $V_{dd} = 0.8$ and $V_{dd} = 1.0$. ($L_{NA} = 75nm$, $L_{PD} = 75nm$, $L_{PL} = 130nm$)

constraints are satisfied at $NF_{PD} = 2$ with a smaller cell area. For $NF_{PD} = 2$, L of the access transistor is chosen to be the minimum value ($75nm$) since the design constraints are already satisfied (Fig. 5.8). For $NF_{PD} = 1$, we vary L of the access transistor from 75nm to 105nm and perform Monte Carlo simulations (Fig. 5.9). The minimum access transistor L that satisfy the SNML constraint is 90nm (Fig. 5.9(a)). At 90nm the WLWM constraint is also satisfied (Fig. 5.9(b)). Similar optimization is performed for L of the pFET load for both $NF_{PD} = 1$ and $NF_{PD} = 2$. Table 5.2 summarizes the optimization results. The cell area is estimated according to the 65nm design rule [99]. When $NF_{PD} = 1$ the cell area is about 30% smaller due to the smaller number of fins.

Table 5.2: Gate Length Optimization Result

NF_{PD}	L_{AX} (nm)	L_{PD} (nm)	L_{PL} (nm)	Area (μm^2)
1	90	75	90	0.702
2	75	75	95	1.027

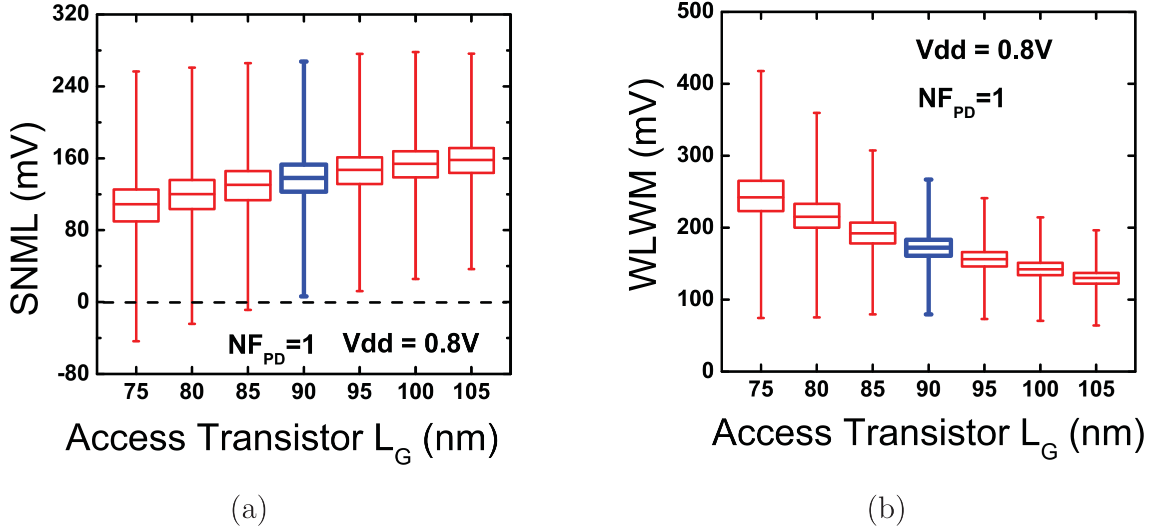


Figure 5.9: (a) SNML (defined in Fig. 5.6) versus access transistor gate length. Whiskers mark $\mu \pm 5.62\sigma$. (b) word line sweeping write margin (WLWM) versus access transistor gate length. Whiskers mark $\mu \pm 5.5\sigma$. (V_{dd}=0.8, 1 fin pull-down nFET)

5.9 Sensitivity Analysis

To further analyze the optimized cell, Monte Carlo simulation is performed with local mismatch added to one pair of transistors at a time. Global variation is switched off. Fig. 5.10(a) shows the contribution of each transistor to read SNM variation. The pull-down nFET has the largest contribution. Therefore, increasing L of the pull-down nFET may be another option to reduce variability. Fig. 5.10(b) shows that the variation of WLWM is primarily due to access transistor variation. This is reflected in Fig. 5.9(b), where we see a strong L dependence of WLWM variation. The static leakage power is dominated by the pull down nFET. Therefore it has the largest contribution to leakage variation (Fig. 5.10(c)).

5.10 Improved Variation Calibration Method

In section 5.7.4 we assumed T_{fin} and L variation are the same in percentage terms. Therefore T_{fin} with a nominal value of 22nm has a 3σ variation of 14%, which is $3.1nm$; L with a drawn value of 90nm also has a 3σ variation of 14%, which is $12.6nm$.

We assumed the two to be the same because in practice it is difficult to separate the two, since both of them contribute to V_{th} variation through short channel effects. However, if the physical source for both variations are LER, then a better assumption is perhaps the same

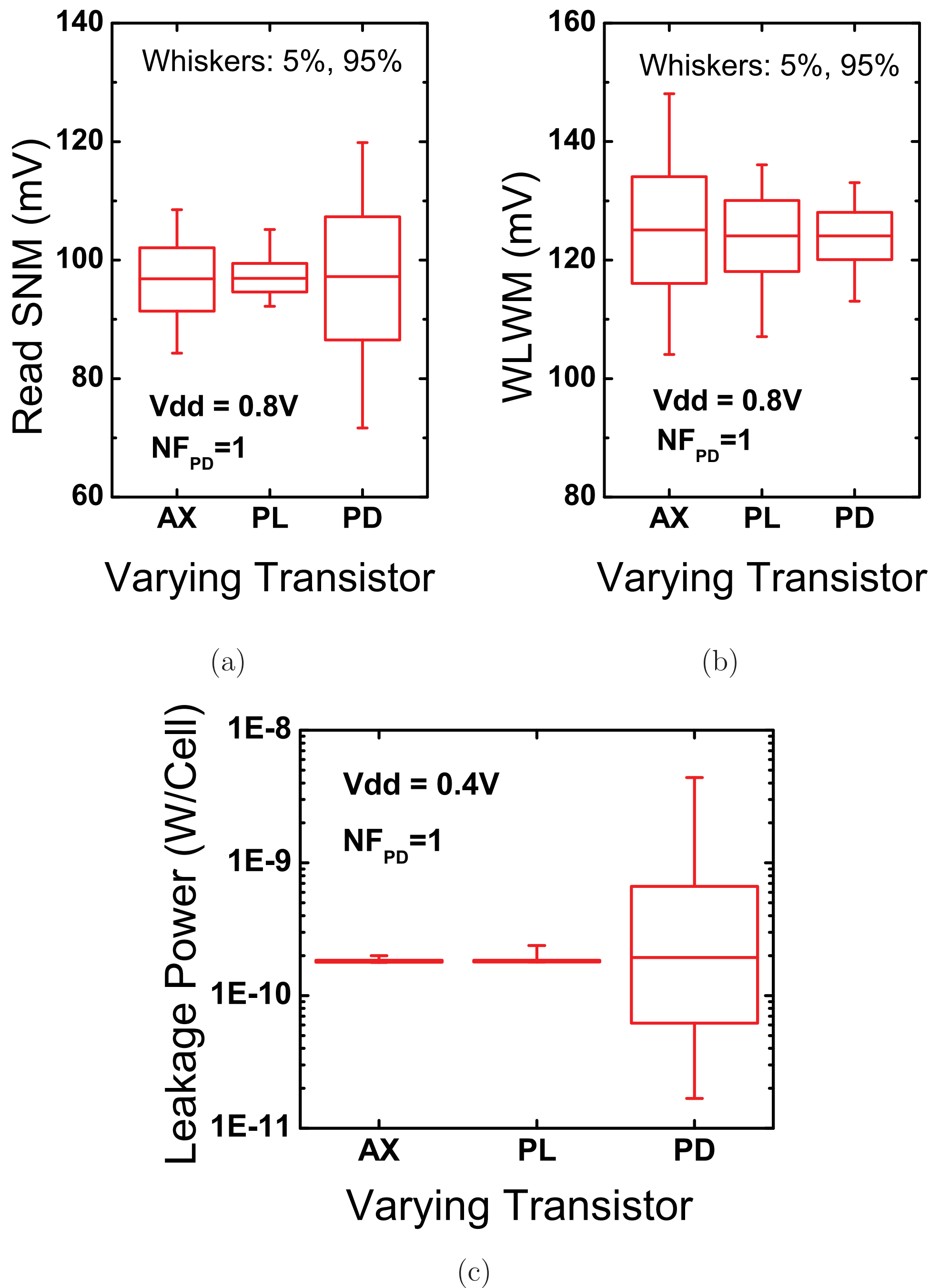


Figure 5.10: Impact of access (AX), pFET load (PL), and pull-down (PD) device variation on (a) read static noise margin ($V_{dd} = 0.8V$), (b) word line sweeping write margin (WLWM) ($V_{dd} = 0.8V$) and (c) static leakage power per cell ($V_{dd} = 0.4V$). (Whiskers mark the 5% and 95% quantiles. $L_{AX} = 90nm$, $L_{PL} = 90nm$, $L_{PD} = 75nm$)

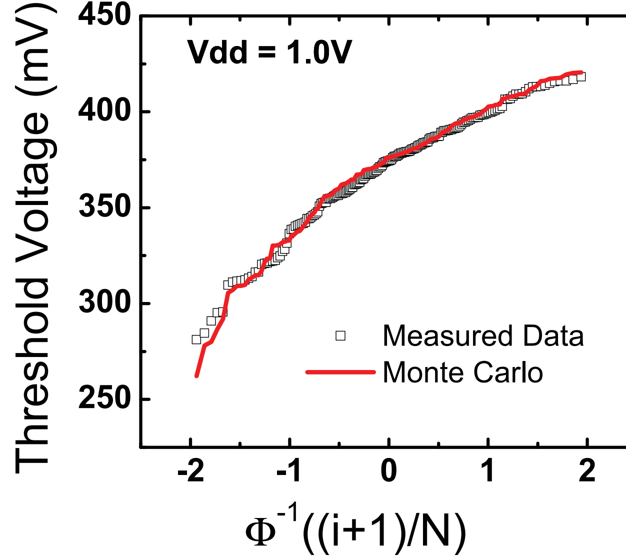


Figure 5.11: A normal plot showing the pull-down device V_{th} distribution from measurements and Monte Carlo simulations. $\Phi(x)$ is the cumulative distribution function of the standard normal distribution. ($N_{fin} = 1$, $L = 75nm$, $\sigma L = \sigma T_{fin} = 2.5nm$ for the pull-down device.)

variation in absolute terms.

In an improved calibration method [93], we calibrated Monte Carlo to both RSNM and pulldown device V_{th} distributions. The local variation in T_{fin} and L were assumed to be equal in absolute terms. The pFET load and access device variations were assumed to be equal to each other, but different from the pulldown device variation. The pull-down device variation (σ_{PD}) was calibrated to its V_{th} distribution. The pFET load and access device variation ($\sigma_{PL,AX}$) were calibrated to the cell RSNM distribution. The results were as follows: $3\sigma_{PD} = 7.5nm$ and $3\sigma_{PL,AX} = 6.0nm$ for $NF_{PD} = 1$; $3\sigma_{PD} = 6.0nm$ and $3\sigma_{PL,AX} = 9.0nm$ for $NF_{PD} = 2$. The differences in variation were possibly due to the different lithography conditions. Fig. 5.11 shows the measured and simulated distributions of the pull-down device V_{th}. Because V_{th} is an exponential function of L, variation in L has a greater impact on V_{th} when it is shifted in the negative direction than when it is shifted in the positive direction. As a result, the distribution we achieved was slightly skewed. By choosing physical parameters (L, T_{fin}) instead of electrical parameters (e.g., V_{th}) to model variation, we are able to capture the non-Gaussian distribution.

5.11 Conclusion

We have developed and demonstrated a procedure to model variation in FinFET-based SRAM cell, and use it for statistical design. An important conclusion is that non-Gaussian threshold distribution is observed, and our physical compact simulation framework captures that. Although this article has focused on six-transistor FinFET SRAM cells, the same procedure can be extended to cells with more transistors, or those employing nonrail-to-rail word-line and bit-line voltages. In the future, we hope to investigate how to separate global variation into a systematic component that depends on the chip position on the wafer and a random component. We would also like to extend this study to other multi-gate device structures, such as independent double-gate FETs, in which the critical variation sources must be modeled differently.

Chapter 6

Thermal Noise Modeling for BSIM4 and BSIM-MG

As wireless hand-held devices become ubiquitous nowadays, RF CMOS circuit design has turned into a very important topic. In designing the basic circuit blocks in these systems, such as the low noise amplifier in an RF front-end receiver, we need to pay particular attention to reducing the noise contribution of the signal processing circuitry itself. Therefore, the accurate modeling of electronic noise is essential. Thermal noise modeling is of particular importance, as it is dominant over flicker noise at RF frequencies.

In this chapter we will discuss about the modeling of MOSFET thermal noise. In MOSFETs, the channel noise is coupled to both the drain and the gate terminals [100]. The noise coupled to the drain terminal through the channel resistance network is called the **drain noise**; the noise coupled to the gate terminal through the gate capacitance is called the **induced gate noise**. Both noise components need to be modeled as functions of the bias condition and the device geometry. Since the drain noise and the induced gate noise have the same physical origin, they are statistically correlated. Therefore it is also important to model the correlation coefficient.

The MOSFET drain noise is known to be a function of the total inversion charge density in the channel, as can be derived using Nyquist's method [101, 102]. Van der Ziel [100] has developed analytical expressions for induced gate noise in field effect transistors, as well as the correlation coefficient. Modern short channel transistors operate in the high lateral field region. Velocity saturation must be considered to properly model channel conductance, and therefore thermal noise. This can be achieved by deriving noise expressions including velocity saturation using an impedance field method [103]. In [103], noise expressions are derived and verified with a finite element thermal noise simulation tool. In another work, noise expressions are derived using Langevin's method [104] and verified with a segmented channel transistor model [105]. The segmented channel model automatically produces the induced gate noise from the channel conductance and channel noise. It has been shown that induced gate noise generated from the segmented channel model agrees with measured noise

data [106].

Besides velocity saturation, other important physical phenomena need to be considered. Most importantly, for short channel devices operating in saturation mode, the drain noise parameter γ is larger than the long channel theoretical value $\frac{2}{3}$. It was reported that channel length modulation is the dominant mechanism that causes this excess noise [106, 107]. In another study, the large γ is attributed partly to drain induced barrier lowering [108].

To be able to use the noise models in real circuit design, it is important to have them implemented in the de facto industry standard BSIM models. BSIM3v3 [109] models the drain noise, but not the induced gate noise. Therefore a new **holistic thermal noise model** that accounts for both the drain noise and the induced gate noise was developed [110] and released to the public along with the first version of BSIM4 [22] in 2000. An independent research group has shown the holistic thermal noise model gives similar results as the Van Der Ziel model in most practical conditions [111].

Nevertheless, the holistic thermal noise model does have some shortcomings. First of all, the correlation factor between the drain noise and the induced gate noise has an incorrect value. Second, the drain noise model has discrepancy with theory in the moderate inversion region. Finally, in strong inversion in linear operation mode, the drain noise has slight disagreement with theory.

In this chapter we show why the holistic thermal noise model is not able to model the correlation factor accurately. A new set of expressions for the drain thermal noise, induced gate thermal noise, and the correlation factor will be developed for BSIM4. We will implement these expressions in Berkeley SPICE3 [112]. A novel method for implementing correlated noise sources in SPICE3 will be presented. The new model will be validated with a segmented channel model without the use of fitting parameters. We will also validate the model by fitting it to measured data. We will further demonstrate that the new model is valid from weak inversion to strong inversion. Finally, we will discuss about and attempt to model the large thermal noise γ in short channel devices.

6.1 Review: BSIM4 Thermal noise model

The BSIM model (as of version 4.6.5) offers two options for thermal noise: the charge-based thermal noise model and the holistic thermal noise model. Users can select the former by setting the parameter $tnoiMod = 0$ or the latter by $tnoiMod = 1$.

6.1.1 Charge-Based Thermal Noise Model

The charge-based model is introduced since BSIM3. It expresses the drain noise (S_{id}) as function of the total inversion charge in the body, Q_{inv}, hence its name "charge-based." (for

the derivation of this model, see, for example, [101]):

$$S_{id} = 4kT\frac{\mu_{eff}}{L_{eff}^2}(-Q_{inv}) \tag{6.1}$$

The charge-based thermal noise model also considers the effect of series resistance when $rdsMod = 0$. The S_{id} expression considering series resistance effects is:

$$S_{id} = \frac{4kT}{R_{ds} + \frac{L_{eff}^2\cdot(-Q_{inv})}{\mu_{eff}}} \tag{6.2}$$

Unfortunately when $tnoiMod = 0$ the induced gate noise (S_{ig}) is not modeled. In other words, $S_{ig} = 0$ for $tnoiMod = 0$.

6.1.2 Holistic Thermal Noise Model

To improve upon the noise model in BSIM3, the holistic thermal noise model is introduced along with the release of BSIM4 in year 2000. It is based on a noise partition concept [110] and considers both S_{id} and S_{ig}. Fig. 6.1 is the schematic representation of this model. The MOSFET noise is modeled using two independent noise sources: a voltage noise source $\overline{v_d^2}$ at the source side and a current noise source $\overline{i_d^2}$ that flows from the drain to the source:

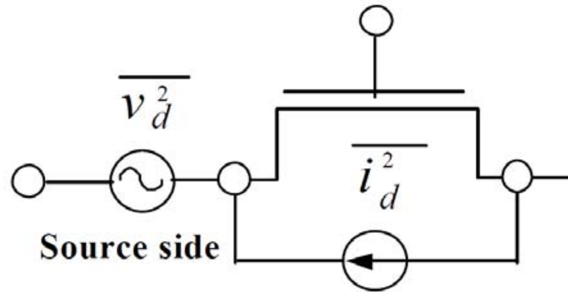


Figure 6.1: Schematic representation of the BSIM4 holistic thermal noise model ($tnoiMod = 1$) [110]

$$\frac{\overline{v_d{}^2}}{\Delta f} = 4kT\cdot\theta_{tnoi}^2\frac{V_{dseff}}{I_{ds}} \tag{6.3}$$

$$\begin{aligned}\frac{\overline{i_d{}^2}}{\Delta f} = 4kT\cdot\frac{V_{dseff}}{I_{ds}}\cdot[G_{ds}+\beta_{tnoi}\cdot(G_m+G_{mbs})]^2 \\ -\frac{\overline{v_d{}^2}}{\Delta f}\cdot(G_m+G_{ds}+G_{mbs})^2\end{aligned} \tag{6.4}$$

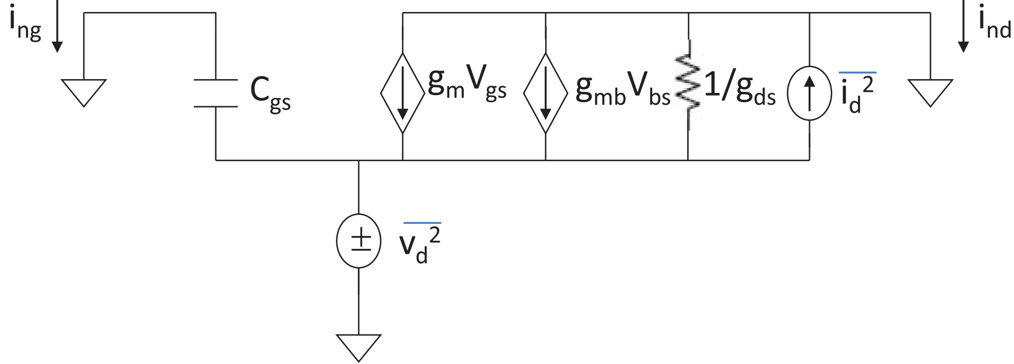


Figure 6.2: Simplified AC equivalent circuit for noise analysis

where

$$\beta_{tnoi} = RNOIA \cdot \left[1 + TNOIA \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right] \tag{6.5}$$

$$\theta_{tnoi} = RNOIB \cdot \left[1 + TNOIB \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right] \tag{6.6}$$

RNOIA, RNOIB, TNOIA and TNOIB are adjustable parameters. L_{eff} is the effective channel length, V_{gsteff} is the effective gate overdrive, which is approximately $V_{gs} - V_{th}$, E_{sat} is the saturation horizontal field, and V_{dseff} is the effective drain voltage [22].

Since $\overline{v_d{}^2}$ is located at the source, it contributes to both the induced gate noise (through C_{gs}) and the drain noise. $\overline{i_d{}^2}$ also contributes to the drain noise[1]. Therefore the total drain noise has contribution from both $\overline{v_d{}^2}$ and $\overline{i_d{}^2}$. The drain noise contribution from $\overline{v_d{}^2}$ is fully correlated with the induced gate noise because they have the same origin, while the drain noise contribution from $\overline{i_d{}^2}$ is uncorrelated with the induced gate noise because they have different origins. The end result is that the drain noise is partially correlated with the induced gate noise. This is consistent with the concept developed in the Van Der Ziel model [100].

We will show here that noise magnitudes predicted by Equations (6.3) and (6.4) agree with the Van der Ziel model [100] for the long channel case when then MOSFET is biased in saturation. Consider the small signal equivalent circuit shown in Fig. 6.2. We tie the source, drain, gate and body terminals to ground and carry out a small signal analysis. The

[1]Here we have assumed the source series resistance is small. In this case $\overline{i_d{}^2}$ is not coupled to the gate and has zero contribution to S_{ig}.

drain noise is

$$\frac{\overline{i_{nd}^2}}{\Delta f} = \frac{\overline{i_d^2}}{\Delta f} + \frac{\overline{v_d^2}}{\Delta f} \cdot (G_m + G_{ds} + G_{mbs})^2 \tag{6.7}$$

We find that the second term in Equation (6.4) cancels with the contribution of $\overline{v_d^2}$. We then have,

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT \cdot \frac{V_{dseff}}{I_{ds}} \cdot [G_{ds} + \beta_{tnoi} \cdot (G_m + G_{mbs})]^2 \tag{6.8}$$

When the source is grounded, the gate noise is just $|j\omega C_{gs}|^2$ times $\overline{v_d^2}$:

$$\frac{\overline{i_{ng}^2}}{\Delta f} = 4kT \cdot \theta_{tnoi}^2 \frac{V_{dseff}}{I_{ds}} \cdot \omega^2 {C_{gs}}^2 \tag{6.9}$$

Consider the square law model [8] in saturation region. We have the following relations:

$$V_{dseff} = V_{dsat} = \frac{V_{gs} - V_{th}}{m} \tag{6.10a}$$

$$I_{ds} = I_{dsat} = \mu C_{ox} \frac{W}{2mL} (V_{gs} - V_{th})^2 \tag{6.10b}$$

$$G_{d0} = \mu C_{ox} \frac{W}{L} (V_{gs} - V_{th}) \tag{6.10c}$$

$$\frac{V_{dseff}}{I_{ds}} = \frac{2}{G_{d0}} \tag{6.10d}$$

$$G_m = \mu C_{ox} \frac{W}{mL} (V_{gs} - V_{th}) = \frac{G_{d0}}{m} \tag{6.10e}$$

$$\frac{dV_{th}}{dV_b} = -\alpha \tag{6.10f}$$

$$\begin{aligned} G_{mb} &= \frac{dI_{dsat}}{dV_b} = \frac{dI_{dsat}}{dV_{th}} \cdot \frac{dV_{th}}{dV_b} \\ &= \mu C_{ox} \frac{W}{mL} (V_{gs} - V_{th}) \cdot \alpha = \frac{G_{d0}}{m} \cdot \alpha \end{aligned} \tag{6.10g}$$

$$m = 1 + \alpha \tag{6.10h}$$

$$G_{d0} = G_m + G_{mb} \tag{6.10i}$$

Since we are focusing on the saturation region, $G_m >> G_{ds}$. Therefore Equation (6.8) can be approximated as:

$$\frac{\overline{i_{nd}}^2}{\Delta f} = 4kT \cdot \frac{V_{dseff}}{I_{ds}} \cdot [\beta_{tnoi} \cdot (G_m + G_{mbs})]^2 \tag{6.11}$$

From Equations (6.11), (6.10d) and (6.10i), we have

$$\frac{\overline{i_{nd}}^2}{\Delta f} = 4kT \cdot 2{\beta_{tnoi}}^2 \cdot G_{d0} \tag{6.12}$$

Setting β_{tnoi} to its default value of $\sqrt{\frac{1}{3}} \approx 0.577$ [111] we obtain the famous drain thermal noise expression:

$$\frac{\overline{i_{nd}}^2}{\Delta f} = 4kT \cdot \gamma \cdot G_{d0} \tag{6.13}$$

where $\gamma = \frac{2}{3}$. This agrees with the long channel theoretical value [106].

Similarly, for the gate noise, we use Equations (6.9) and (6.10d) and set θ_{tnoi} to its default value of $\sqrt{\frac{2}{15}} \approx 0.37$ [111] [2]. We obtain:

$$\frac{\overline{i_{ng}}^2}{\Delta f} = 4kT \cdot \frac{4}{15} \cdot \frac{\omega^2 C_{gs}^2}{G_{d0}} \tag{6.14}$$

which agrees with the long channel theoretical value [106].

With a similar analysis, we now show that the correlation factor does not agree with the long channel theoretical value. The cross correlation is given by

$$\overline{i_{ng} {i_{nd}}^*} = \overline{(j\omega C_{gs} v_d)\left[(G_m + G_{mb} + G_{ds}){v_d}^* + {i_d}^*\right]} \tag{6.15}$$

We again assume $G_{ds} << G_m + G_{mb}$ and use Equations (6.10i) and (6.15). Also, since the noise sources v_d and i_d are uncorrelated, the term $\overline{v_d {i_d}^*} = 0$. We obtain

$$\begin{aligned} \overline{i_{ng} {i_{nd}}^*} &= j\omega C_{gs} \cdot G_{d0} \cdot 4kT \cdot \frac{2}{15} \frac{2}{G_{d0}} \\ &= j\omega C_{gs} \cdot 4kT \cdot \frac{4}{15} \end{aligned} \tag{6.16}$$

However, the theoretical value of the cross correlation is [113]

$$\overline{i_{ng} {i_{nd}}^*} = j\omega C_{gs} \cdot 4kT \cdot \frac{1}{6} \tag{6.17}$$

[2] The default value of θ_{tnoi} was modified from 0.37 to 0.5164 in BSIM4.4.0 by mistake. As a result, the default gate noise model in BSIM4.4.0 or later deviates from the long channel theoretical value. In practice, however, the value of θ_{tnoi} can be easily adjusted through the fitting parameter $RNOIB$.

Therefore the BSIM4 holistic thermal noise model overestimates the cross correlation by a factor of 1.6. As a result, the cross correlation coefficient $c = \sqrt{\frac{\overline{i_{ng} i_{nd}^*}}{\overline{i_{ng}^2} \, \overline{i_{nd}^2}}}$ is overestimated by a factor of 1.6. This is not surprising because with the noise subcircuit in Fig. 6.1, there is no way to independently tune the induced gate noise magnitude and the correlation coefficient at the same time.

6.1.3 Verification with Circuit Simulation

We have evaluated the holistic thermal noise model with a modelcard based on the 130nm Predictive Technology Model [114] [3]. The evaluation is performed in HSpice [66] with the ".lin" analysis. The 2-port noise parameters is calculated by Hspice and converted to the real and imaginary parts of the cross correlation coefficient (c) with a MATLAB script using the formula given in [115].

The results are illustrated in Fig. 6.3. As expected, the drain noise, S_{id} is independent of frequency, whereas the induced gate noise, S_{ig} is proportional to frequency squared (Fig. 6.3(a)). Fig. 6.3(b) shows the real and imaginary parts of the correlation coefficient, c. At low frequencies c is purely imaginary with a value of 0.6. Since the theoretical value is 0.395, the holistic thermal noise model overestimates the correlation by about a factor of 1.6, as we predicted in Section 6.1. Beyond approximately 100GHz, the real part of c starts to emerge. This is an artifact of the quasi-static model beyond the device cutoff frequency (f_T). According to [115], the cross correlation is given by

$$\overline{i_{ng}^* i_{nd}} = (Y_{11} + Y_{12})(Y_{21} + Y_{22})^* \overline{v_d^2} \tag{6.18}$$

Beyond f_T, in a quasi static model the imaginary part of Y_{21} becomes non-zero [58]. When it is multiplied with Y_{11}, which is supposed to have a large impginary part, a real component in the correlation appears. Fig. 6.3(c) shows the simulation of short circuit current gain. Indeed the short circuit current gain drops to 1 around 100GHz, so f_T is around 100GHz. Beyond f_T the device becomes non quasi-static and a quasi-static model is insufficient. Fig. 6.3(d) shows the simulation of Y parameters. As expected from a quasi static model, the imaginary parts of Y_{21} and Y_{22} starts to dominate beyond f_T.

The observation of a real correlation factor has already been reported in [115]. Fig. 6.4 is an example simulation result.

6.2 Derivation of New Thermal Noise Model

The derivation of thermal noise is well known in the literature [116] [117] [103]. In this study, the general method for thermal noise derivation is applied to the BSIM model. We derive

[3] Instead of using the latest version of BSIM4, we have used BSIM4.0. This is to avoid a bug introduced in BSIM4.3.0. In fact, the bug was discovered during this study, and subsequently corrected in BSIM4.6.4.

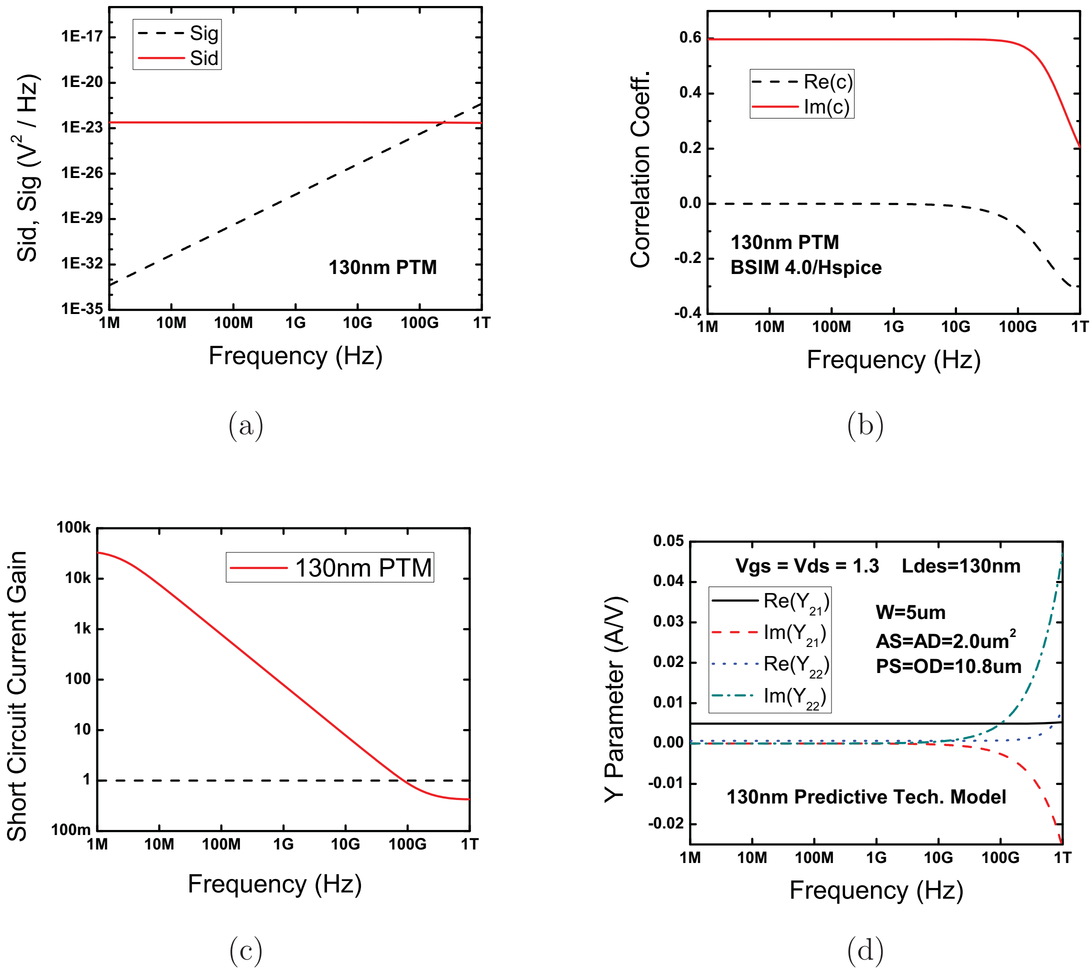


Figure 6.3: Evaluation of (a) drain noise and induced gate noise, (b) real and imaginary parts of the correlation coefficient, (c) device cutoff frequency and (d)Y_{21} and Y_{22} for the 130nm BSIM4-based predictive technology model [114]. ($L = 130nm$, $tnoiMod = 1$, $fnoiMod = 0$)

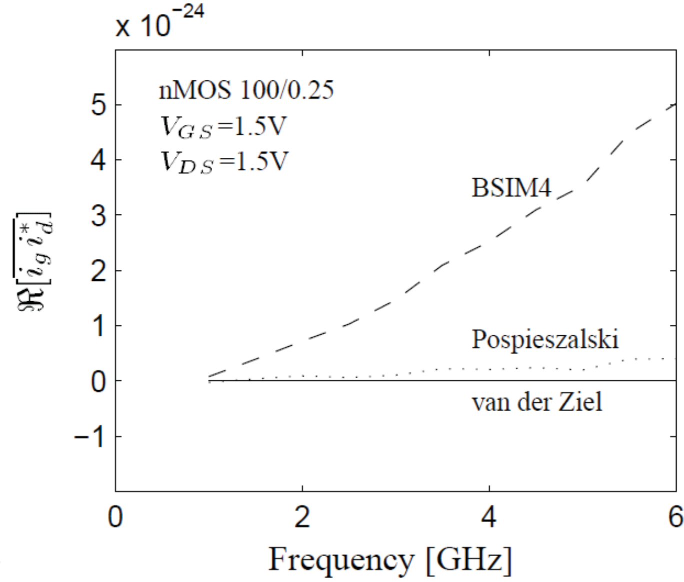


Figure 6.4: The evaluation of the real part of $\overline{i_{ng}{}^* i_{nd}}$ in BSIM4 [115]

expressions for thermal noise based on the channel conductance formulation of the BSIM model.

We may either use the Klaassen Prins method [116] [117] or the Green's Function approach [103] for thermal noise derivation. Both yield the same result. In this section we will show the derivation using the Klassen Prins method since the mathematics is somewhat simpler.

6.2.1 Drain Noise

In this subsection we derive expressions for the drain thermal noise. One assumption we will make here is that loading effects due to the gate capacitance is negligible. To be specific, we will not consider the small signal current flowing into the gate terminal in the Kirchoff's Current Law (KCL) equations when we calculate the drain noise. The same assumption is made in [117, 105]

We start with the basic drain current expression of BSIM and BSIM models [21]:

$$I_D = \frac{g_0(V)\frac{dV(x)}{dx}}{1 + \frac{1}{E_{sat}}\frac{dV(x)}{dx}} \tag{6.19}$$

where the channel conductance without velocity saturation, $g_0(V)$, is given by

$$g_0(V) = \mu_{eff} W C_{ox} V_{gsteff} \left(1 - \frac{V}{V_b}\right) \tag{6.20}$$

We apply the Langevin's method [104] to compute the small signal noise current flowing to the drain terminal, i_D. By replacing I_D with $I_D + i_D(t)$, replacing V with $V + v$, and adding a Langevin noise source h(x,t) to the right hand side of Equation (6.19), we obtain

$$I_D + i_D(t) = \frac{g_0\left(V(x) + v(x,t)\right)}{1 + \frac{1}{E_{sat}}\frac{d}{dx}\left[V(x) + v(x,t)\right]} \cdot \frac{d}{dx}\left[V(x) + v(x,t)\right] + h(x,t) \tag{6.21}$$

After re-arranging some terms, the 0'th order terms cancel. We focus on the first order terms and ignore the second order terms. Equation (6.21) becomes

$$\left[i_D(t) - h(x,t)\right] \cdot \left(1 + \frac{1}{E_{sat}}\frac{dV(x)}{dx}\right) + \frac{I_D}{E_{sat}}\frac{dv(x,t)}{dx} = \frac{d}{dx}\left[g_0(V(x)) \cdot v(x,t)\right] \tag{6.22}$$

The above expression is integrated from $x = 0$ to $x = L$. With boundary conditions $v(0,t) = 0$ and $v(L,t) = 0$. The terms containing $v(x,t)$ all become zero. We have

$$i_D(t) = \frac{1}{L_{vsat}} \int_0^L h(x,t) \cdot \left[1 + \frac{1}{E_{sat}}\frac{dV(x)}{dx}\right] dx \tag{6.23}$$

The autocorrelation function of $i_D(t)$ is

$$\overline{i_D(t) i_D(t+s)} = \frac{1}{{L_{vsat}}^2} \int_0^L \int_0^L \overline{h(x,t) h(x',t+s)} \cdot \left[1 + \frac{1}{E_{sat}}\frac{dV(x)}{dx}\right] \left[1 + \frac{1}{E_{sat}}\frac{dV(x')}{dx'}\right] dx dx' \tag{6.24}$$

According to the Wiener-Khintchine theorem [118, 119], we may convert the autocorrelation function to noise spectral density:

$$S_{id}(f) = \frac{1}{{L_{vsat}}^2} \int_0^L \int_0^L S_h(x,x',f) \left[1 + \frac{1}{E_{sat}}\frac{dV(x)}{dx}\right] \left[1 + \frac{1}{E_{sat}}\frac{dV(x')}{dx'}\right] dx dx' \tag{6.25}$$

We assume the thermal noise sources at different points in the channel are uncorrelated. With this assumption the cross-spectral intensity can be written as

$$S_h(x,x',f) = 4kT \cdot \frac{g_0(x)}{1 + \frac{1}{E_{sat}}\frac{dV(x)}{dx}} \delta(x' - x) \tag{6.26}$$

Substituting the above expression into Equation (6.25) and applying the sifting property of the δ function, we obtain

$$S_{id}(f) = \frac{4kT}{{L_{vsat}}^2} \int_0^L g_0(x) \left[1 + \frac{1}{E_{sat}}\frac{dV(x)}{dx}\right] dx \tag{6.27}$$

We perform a change-of-variable using Equation (6.19) and obtain

$$S_{id}(f) = \frac{4kT}{I_D {L_{vsat}}^2} \int_0^{V_{DS}} g_0^2(V) dV \tag{6.28}$$

The same expression is given in [105] except the definition of L_{vsat} is different. Since in the BSIM4 model, the lateral field dependent mobility is expressed in terms of $\frac{dV}{dx}$ rather than $\frac{d\psi}{dx}$, we express L_{vsat} in terms of V_{ds} rather than ψ_{ds}.

An alternative way of deriving the drain current expression is to use a Green's Function approach [103] with the incremental mobility model, which gives the same result.

We substitute $g_0(V)$ with the BSIM4 channel conductance expression (Equation (6.20)) and perform integration from the source end to the drain end. The final drain noise expression is

$$\begin{cases} S_{id} = 4kT \cdot \gamma \cdot g_{d0} \\ \gamma = \frac{2}{3} \cdot \frac{L}{L_{vsat}} \cdot \frac{1+\eta+\eta^2}{1+\eta} \end{cases} \tag{6.29}$$

where

$$\eta = 1 - \frac{V_{dseff}}{V_b} \tag{6.30}$$

and

$$g_{d0} = \mu_{eff} C_{ox} \frac{W}{L} V_{gsteff} \tag{6.31}$$

6.2.2 Induced Gate Noise

The channel thermal noise is coupled not only to the drain terminal, but also to the gate terminal. In this section, we derive an expression for the induced gate thermal noise.

The fluctuation of gate current is caused by the fluctuation of gate charge. The total gate charge of the MOSFET can be expressed as the charge density integrated from source to drain

$$Q_g = WC_{ox} \int_0^L \left[V_{gs} - V_{th} - V(x)\right] dx \tag{6.32}$$

Performing small signal analysis and differentiate both sides of the equation, we have

$$i_G = -WC_{ox} \int_0^L j\omega v(x) dx \tag{6.33}$$

where we have used the relation $i_G = \frac{d}{dt} Q_G$ on the left hand side and replaced the time derivative with $j\omega$ on the right hand side.

To compute $v(x)$, we re-arrange Equation (6.22) into an integral from 0 to y:

$$v(y) = \frac{1}{g(y)} \int_0^y \left[i_D(t) - h(x,t)\right] \frac{g_0(x)}{g(x)} dx \tag{6.34}$$

where

$$g(x) = \frac{g_0(x)}{1 + \frac{1}{E_{sat}}\frac{dV}{dx}} \tag{6.35}$$

Combining Equation (6.33) and (6.34), we have

$$i_G = -j\omega C_{ox} W \int_0^L \frac{1}{g(y)} \int_0^y \left[i_D - h(x)\right] \frac{g_0(x)}{g(x)} dx\, dy \tag{6.36}$$

Next, we write down the autocorrelation function $\overline{i_G{}^* i_G}$, replace $\overline{i_G{}^* i_G}$ with spectral density S_{ig}, and replace all $\overline{h(x,t)h(x',t)}$ terms with $4kTg(x')\delta(x-x')$. The derivation is tedious and several pages long. We will not show the details here but only present the final result:

$$S_{ig} = \frac{\omega^2 W^2}{{L_{vsat}}^2} \frac{4kT}{I_d^5} C_{ox}^2 \int_0^{V_{ds}} {g_0}^2(v) \left[\int_0^{V_{ds}} (u-v) g_0(u) du\right]^2 dv \tag{6.37}$$

The above equation is also a special case of [105] with a different L_{vsat} expression.

To develop induced gate noise expressions for the BSIM4 model, we substitute $g_0(V)$ with Equation (6.20) and carry out the integration. The final expression is

$$\begin{cases} S_{ig} = 4kT \cdot \delta \cdot \dfrac{\omega^2 (C_{ox} W L)^2}{g_{d0}} \\ \delta = \dfrac{16}{135} \cdot \left(\dfrac{L_{vsat}}{L}\right)^3 \cdot \dfrac{1 + 5\eta + \frac{21}{2}\eta^2 + 5\eta^3 + \eta^4}{(1+\eta)^5} \end{cases} \tag{6.38}$$

6.2.3 Correlation

In this subsection, we derive an expression for the correlation $\overline{i_d{}^* i_g}$. From Equations (6.23) and (6.36) we can write down the correlation:

$$\overline{i_d{}^* i_g} = -\frac{j\omega C_{ox} W}{{L_{vsat}}^2} \cdot \int_0^L h(w,t) \frac{g_0(w)}{g(w)} dw \cdot \tag{6.39}$$

$$\int_0^L \int_0^y \left[\int_0^L h(z,t) \frac{g_0(z)}{g(z)} dz - L_{vsat} \cdot h(x,t)\right] \frac{g_0(x)}{g(x)} dx \cdot \frac{1}{g(y)} dy \tag{6.40}$$

After simplification we obtain the cross spectral density:

$$S_{ig,id} = 4kT \cdot \frac{-j\omega W C_{ox}}{I_D^3 {L_{vsat}}^2} \int_0^{V_{ds}} {g_0}^2(V) \int_0^{V_{ds}} g_0(U) \cdot (V-U)\, dU\, dV \tag{6.41}$$

Next, we substitute the BSIM4 channel conductance expressions in Equation (6.41) to obtain $S_{ig,id}$ in terms of variables available in the BSIM4 model.

$$\begin{cases} S_{ig,id} = 4kT \cdot j\omega C_{ox} W L \cdot \epsilon \\ \epsilon = \dfrac{1}{9} \dfrac{L_{vsat}}{L} \dfrac{1 + 3\eta - 3\eta^2 - \eta^3}{(1+\eta)^3} \end{cases} \tag{6.42}$$

Finally, the correlation coefficient is given by

$$\begin{aligned} c &= \frac{S_{ig,id}}{\sqrt{S_{id}S_{ig}}} \\ &= j\frac{\epsilon}{\sqrt{\delta \cdot \gamma}} \end{aligned} \tag{6.43}$$

From Equation (6.42) we know the correlation coefficient goes to zero at $V_{ds} = 0$. The physical reason for this is explained as follows. Suppose there is a macroscopic voltage noise source $\overline{v_1}^2$ at location x along the channel, and the transfer function from this noise source to the drain current and the gate current are g_{1d} and $j\omega c_{1g}$, respectively. Because of symmetry, there must be another macroscopic voltage noise source of the same magnitude at location $L-x$. The transfer function from that noise source to the drain current and the gate current are $-g_{1d}$ and $j\omega c_{1g}$, respectively. For the noise source at location x, its contribution to the correlation $\overline{(i_d{}^* i_g)}$ is $j\omega c_{1g} g_{1d}\overline{v_1}^2$. For the noise source at location $L-x$, its contribution is $-j\omega c_{1g} g_{1d}\overline{v_1}^2$. The two cancel each other, so the total contribution is zero. This condition is only true when $V_{ds} = 0$. At non-zero V_{ds}, the charge distribution is not symmetric and the effect of macroscopic noise sources at symmetric locations no longer cancel.

Alternatively we can argue mathematically that since the MOSFET device structure is symmetric, if we simply swap the source and drain, the correlation coefficient should change its sign. Therefore the correlation coefficient must be an odd function of V_{ds} (Gummel Symmetry Test condition). Also we expect the correlation coefficient to be a smooth function. Therefore the correlation must be zero at $V_{ds} = 0$.

6.2.4 Verification

To verify that the derivation is correct, we compare the new analytical model with a segmented transistor model.

The segmented transistor model is a sub-circuit consisting of ten instances of single transistor models connected in series, as illustrated in Fig. 6.5. Each instance is given a length parameter that is one tenth of the total transistor length because it only represents one tenth of the transistor channel. In this study, each instance is a Verilog-A based **simple segmentable BSIM** model, which we developed specifically for the purpose of verifying the new noise model.

In each segment of *simple segmentable BSIM* we only implement a drain noise source, but not an induced gate noise source. When connected in a segmented transistor model, the induced gate noise will be automatically generated through capacitive coupling from the segment boundary nodes to the external gate terminal. Moreover, the automatically generated induced gate noise is correlated with the drain noise, just like it is in a real transistor. Therefore it can be used for the purpose of verification.

For simplicity, the *simple segmentable BSIM* does not consider real device effects such as vertical field induced mobility degradation, external source and drain resistance, drain

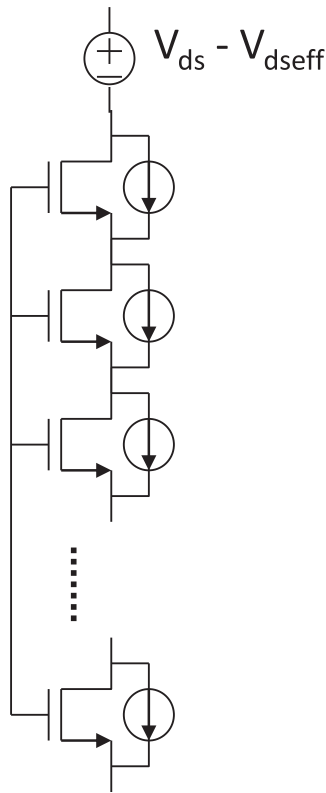


Figure 6.5: Illustration of the segmented transistor model

induced barrier lowering, channel length modulation and many others. It also uses different smoothing functions compared to the official BSIM4 model, in order for its drain current and terminal charge densities to match those of a single transistor model of the same total length in the quasi-static condition. The Verilog-A code for *Simple Segmentable BSIM* is available in Appendix C.

Note that in the segmented transistor model a voltage source connects the drain of the top-most instance to the external drain terminal, as shown in Fig. 6.5. This voltage source is used for modeling drain voltage saturation.

We first verify the behavior of the analytical model for the long channel case. Velocity saturation is neglected for this verification [4]. The results are shown in Fig. 6.6. In Figs. 6.6(a)(b) we see that in saturation mode, both the holistic thermal noise model ($tnoiMod = 1$) and the new model matches segmentation for drain noise (S_{id}) and induced gate noise (S_{ig}). In the linear region, the new model agrees with segmentation better then the holistic thermal noise model. Fig. 6.6(c) shows the correlation coefficient for the three cases. As expected, the new model agrees with segmentation better in both linear and saturation modes. Also, as expected, the correlation coefficient goes to zero at $V_{ds} = 0$. Fig. 6.6(d) shows the saturation mode drain noise and induced gate noise versus frequency. The discrepancy at high frequencies is due to loading effects of the gate capacitors, which we did not consider during the derivation of the new model. This happens at frequencies higher than the transistor cutoff frequency, in which non quasi-static effects are prominent.

Next, we verify the model for the short channel case. Velocity saturation is considered and the saturation velocity is set to $10^5 m/s$. The results are shown in Fig. 6.7. In all cases, the analytical model agrees with segmented channel model well. It's worth noting that the drain noise and induced gate noise have opposite dependence on L and V_{gs}. At higher V_{gs}, the channel conductance is larger, therefore the noise current is larger. However, the noise voltage is smaller, so the gate noise is smaller. At larger L, the channel conductance is smaller, therefore the drain noise current is smaller. However, the induced gate noise current is larger owing to a small channel conductance and large total gate capacitance. These trends are consistent with experimental observation [106].

Without velocity saturation, the model predicts a correlation coefficient that is independent of L and V_{gs}. With velocity saturation, the correlation coefficient becomes a function of both L and V_{gs}.

6.3 Thermal Noise in the Weak Inversion Region

In Section 6.2, we have derived expressions for MOSFET thermal noise in the strong inversion region. For the weak inversion region, however, the results are no longer accurate. It can be

[4]We set VSAT=$10^9 m/s$

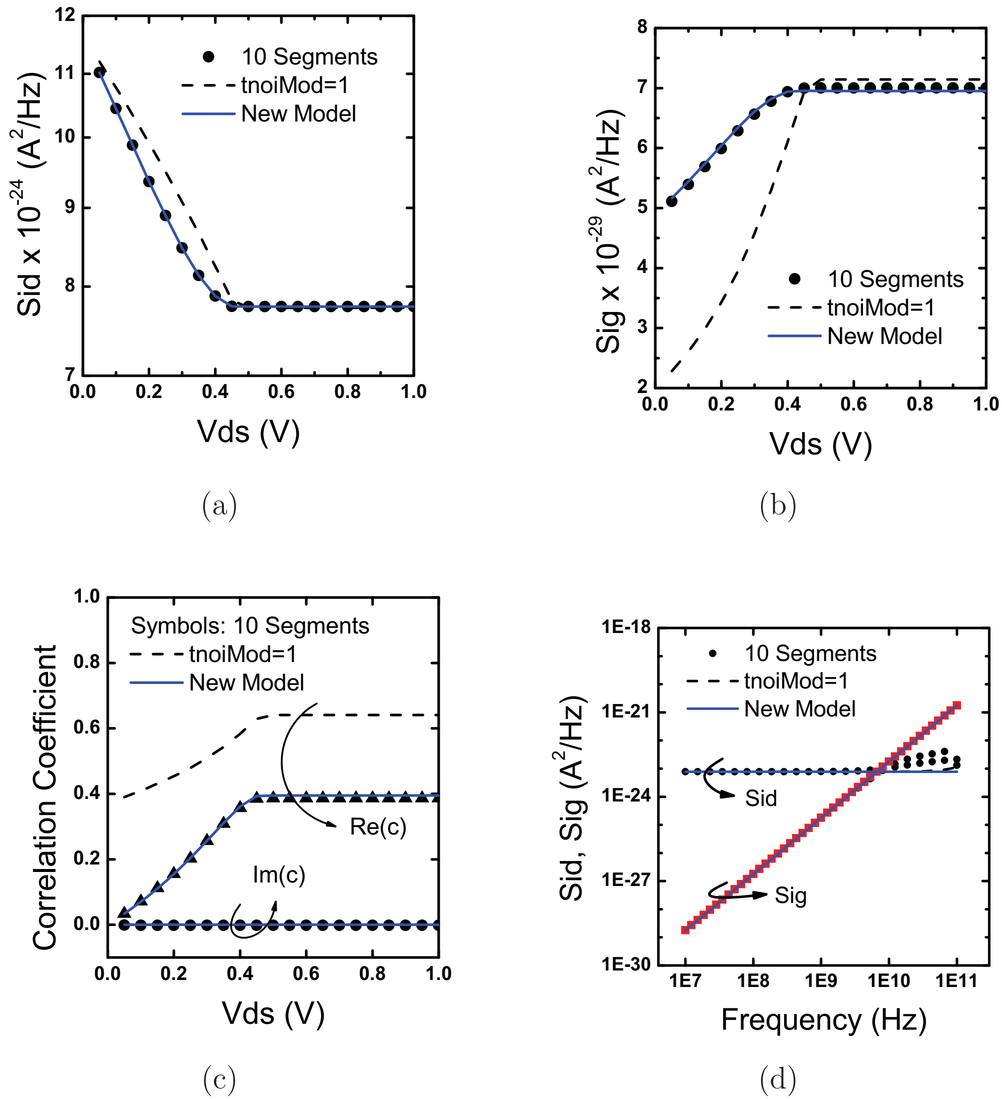


Figure 6.6: Verification of the new thermal noise model: (a) drain noise versus V_{ds} (b) induced gate noise versus V_{ds} (c) real and imaginary parts of the correlation coefficient versus V_{ds} (d) drain noise and induced gate noise versus frequency ($L = 1\mu m$; $f = 20MHz$; simulation performed with *simple segmentable BSIM*)

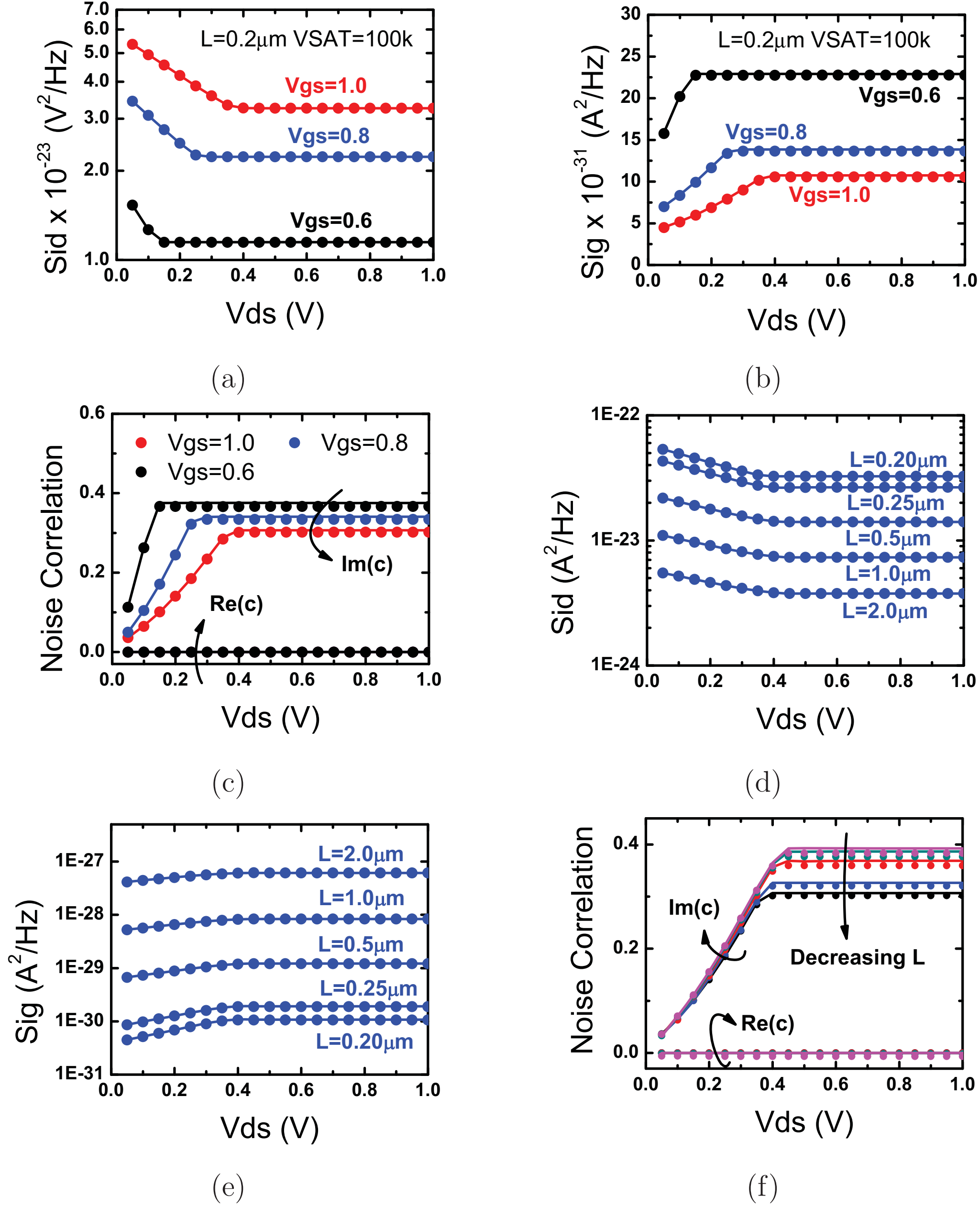


Figure 6.7: Verification of the new thermal noise model for short channel devices. (a)-(c) verify V_{gs} and V_{ds} dependence at $L = 0.2\mu m$. (a) drain noise (b) induced gate noise (c) real and imaginary parts of the correlation coefficient. (d)-(f) verify V_{ds} and L dependence at $V_{gs} = 1.0$. (d) drain noise (e) induced gate noise (f) real and imaginary parts of the correlation coefficient. ($f = 20MHz$; saturation velocity $VSAT = 100k$; simulation performed with *simple segmentable BSIM*)

shown mathematically that γ is subject to the following limitation:

$$\frac{2}{3} < \gamma = \frac{2}{3} \cdot \frac{1 + \eta + \eta^2}{1 + \eta} < 1 \tag{6.44}$$

This is confirmed by simulation (Fig. 6.8). On the other hand, theoretical calculations yield $\gamma = \frac{1}{2}$ in weak inversion [120].

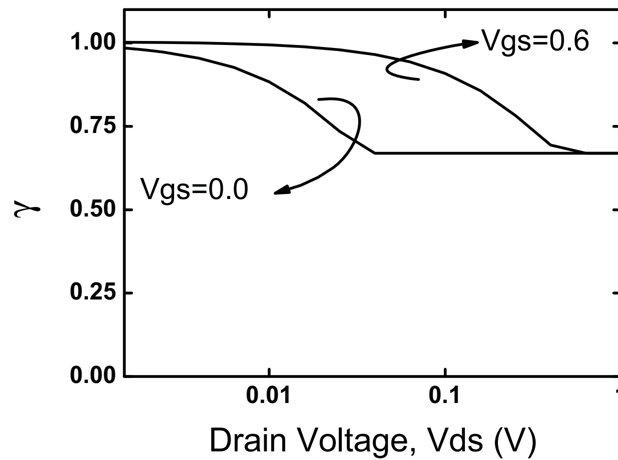


Figure 6.8: γ parameter versus the drain voltage for the model derived in Section 6.2. At $V_{gs} = 0$ at high drain bias, the value of γ is overestimated.

The physical reason for this discrepancy is the failure to consider diffusion current. In weak inversion, where diffusion dominates, the channel conductance is exponentially dependent on the channel voltage:

$$g_0(V) = \mu W C_{ox} V_{gsteff} \cdot \exp(-V/V_t)$$

whereas in Section 6.2 we assumed a linear dependence (Equation (6.20)).

In this section we develop noise expressions that is valid from weak to strong inversion, and verify its asymptotic behavior.

6.3.1 Derivation of Thermal Noise Expressions Valid in All Regions of Operation

Unlike in BSIM4, the channel conductance expression for charge-based models such as EKV [121] and BSIM5 [122] are valid from weak to strong inversion. Therefore, we use it to derive noise expressions valid in all regions of operation.

The MOSFET channel conductance expressed in terms of inversion charge is:

$$g_0(V) = \mu W C_{ox} V_t q_i(V) \tag{6.45}$$

where $q_i(V)$ is the inversion charge density normalized to C_{ox} and the thermal voltage V_t.

Since, as shown in Section 6.2, the integrals for calculating noise are with respect to the channel voltage V instead of q_i, we need to derive the jacobian, $\frac{dV}{dq_i}$ first. From the BSIM5 model [122]:

$$\frac{dV}{dq_i} = \left(-\frac{V_t}{A_{bulk}}\right)\frac{q_i + A_{bulk}}{q_i} \tag{6.46}$$

where A_{bulk} is the bulk charge linearization factor [5]. Substituting Equations (6.45) and (6.46) into Equations (6.28), (6.37), and (6.41) and carry out the integration, we obtain expressions for noise spectral density in terms of q_i:

$$S_{id} = 4kT \cdot \mu C_{ox}\frac{W}{L_{vsat}}V_t\left[\frac{q_{is}+q_{id}}{2} + \frac{(q_{is}-q_{id})^2}{12\left(\frac{q_{is}+q_{id}}{2}+A_{bulk}\right)}\right] \tag{6.47a}$$

$$\begin{aligned} S_{ig} = {} & 4kT \cdot \frac{(C_{ox}WL)^2\omega^2}{12\mu C_{ox}\frac{W}{L}V_t}\left(\frac{L_{vsat}}{L}\right)^3 \\ & \left\{\frac{\frac{q_{is}+q_{id}}{2}}{\left(\frac{q_{is}+q_{id}}{2}+A_{bulk}\right)^2} - \frac{\left[6\left(\frac{q_{is}+q_{id}}{2}\right)+A_{bulk}\right](q_{is}-q_{id})^2}{60\left(\frac{q_{is}+q_{id}}{2}+A_{bulk}\right)^4} + \frac{(q_{is}-q_{id})^4}{144\left(\frac{q_{is}+q_{id}}{2}+A_{bulk}\right)^5}\right\} \end{aligned} \tag{6.47b}$$

$$S_{ig,id} = -j\omega \cdot 4kT \cdot C_{ox}WL\left(\frac{L_{vsat}}{L}\right)\left[\frac{q_{is}-q_{id}}{12\left(\frac{q_{is}+q_{id}}{2}+A_{bulk}\right)} - \frac{(q_{is}-q_{id})^3}{144\left(\frac{q_{is}+q_{id}}{2}+A_{bulk}\right)^3}\right] \tag{6.47c}$$

where q_{is} and q_{id} are the normalized charge densities at the source end and drain end, respectively.

Since quantities q_{is} and q_{id} are not available in the BSIM4 model, we need to convert the above spectral density expressions into BSIM4-friendly forms containing variables such as V_{gsteff}, I_{ds}, V_{dseff}, ... etc. The conversion is illustrated in Table 6.1. First, we find the asymptotic forms of q_{is} and q_{id} in weak inversion, strong inversion saturation (pinch-off) mode, and strong inversion linear mode ($V_{ds} = 0$). Then, we compute the asymptotic forms of two special expressions that appear in the spectral density formula, as listed in the last two rows of Table 6.1 in columns 2-4. Finally, we find BSIM4-friendly expressions that has the correct asymptotic behavior.

[5] BSIM5 equations are derived based on an ideal retrograde doping profile, in which case the bulk charge is a linear function of the inversion carrier density, q_i, in strong inversion.

Table 6.1: Conversion of source (q_{is}) and drain charge (q_{id}) density based expressions to BSIM4-friendly expressions. (WI: Weak Inversion; SI: Strong Inversion)

Charged-based expressions	Asymptotic form			BSIM4-friendly expressions
	WI	SI	SI	
	$V_{ds} >> \frac{kT}{q}$	pinch-off	$V_{ds} = 0$	
q_{is}	$\frac{V_{gsteff}}{V_t}$	$\frac{V_{gsteff}}{V_t}$	$\frac{V_{gsteff}}{V_t}$	
q_{id}	0	0	$\frac{V_{gsteff}}{V_t}$	
$\frac{q_{is}+q_{id}}{2} \cdot V_t$	$\frac{V_{gsteff}}{2}$	$\frac{V_{gsteff}}{2}$	V_{gsteff}	$V_{gsteff}\left(1 - \frac{V_{dseff}}{2V_b}\right)$
$(q_{is} - q_{id}) \cdot V_t$	V_{gsteff}	V_{gsteff}	0	$V_{gsteff} \cdot \frac{V_{dseff}}{V_b}$

After carrying out the conversion according to Table 6.1, we obtain:

$$S_{id} = 4kT \cdot \gamma \cdot g_{d0} \tag{6.48a}$$

$$\gamma = \frac{L}{L_{vsat}}\left[\frac{1+\eta}{2} + \frac{(1-\eta)^2}{6\left[(1+\eta) + \frac{2V_t A_{bulk}}{V_{gsteff}}\right]}\right] \tag{6.48b}$$

$$S_{ig} = 4kT\frac{\omega^2 \cdot (C_{ox}WL)^2}{g_{d0}} \cdot \delta \tag{6.48c}$$

$$\delta = \frac{1}{6}\left(\frac{L_{vsat}}{L}\right)^3 \cdot \left[\frac{1+\eta}{\left[(1+\eta) + \frac{2A_{bulk}V_t}{V_{gsteff}}\right]^2} - \frac{\left[6(1+\eta) + \frac{2A_{bulk}V_t}{V_{gsteff}}\right](1-\eta)^2}{15\left[(1+\eta) + \frac{2A_{bulk}V_t}{V_{gsteff}}\right]^4} + \frac{(1-\eta)^4}{9\left[(1+\eta) + \frac{2A_{bulk}V_t}{V_{gsteff}}\right]^5}\right] \tag{6.48d}$$

$$S_{igid} = -j\omega \cdot 4kT \cdot C_{ox}WL \cdot \epsilon \tag{6.48e}$$

$$\epsilon = \frac{1}{6} \cdot \frac{L_{vsat}}{L}\left[\frac{1-\eta}{\left[(1+\eta) + \frac{2A_{bulk}V_t}{V_{gsteff}}\right]} + \frac{(1-\eta)^3}{3\left[(1+\eta) + \frac{2A_{bulk}V_t}{V_{gsteff}}\right]^3}\right] \tag{6.48f}$$

where

$$g_{d0} = \mu C_{ox}\frac{W}{L}V_{gsteff} \tag{6.49}$$

Note that the above spectral density expressions become identical to Equations (6.29),

(6.38), and (6.42) if we were to set all $\frac{2A_{bulk}V_t}{V_{gsteff}}$ terms to zero. Since in strong inversion $\frac{2A_{bulk}V_t}{V_{gsteff}}$ is negligible compared to the $(1+\eta)$ term, the behavior of the new model does not change much in strong inversion. In fact, simulation shows that with the new model, in the strong inversion saturation region, S_{id} is reduced by less than about 2%, the correlation coefficient increases by about 6%, and the gate noise is reduced by about 11%.

6.3.2 Verifications

To verify the model, we plot γ versus drain voltage in both weak and strong inversion, as suggested in [123]. The model exhibits correct asymptotic values for the long channel case, as shown in Fig. 6.9: In weak inversion, γ goes from near 1 at zero drain bias to $\frac{1}{2}$ when $qV_{ds} >> kT$; in strong inversion γ goes from near 1 at zero drain bias to $\frac{2}{3}$ in saturation mode. In weak inversion when $qV_{ds} >> kT$, the drain noise is approximately equal to the shot noise value, $2qI_{ds}$, as expected [123]. As shown in Fig. 6.9(b), the analytical models all converge to $2qI_{ds}$ in weak inversion.

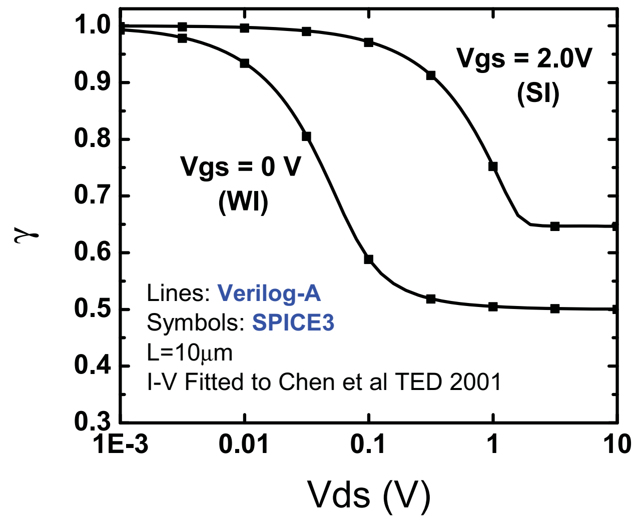
Notice that we have implemented and tested the model in both Verilog-A and SPICE3. Verilog-A is a convenient tool for verification. On the other hand, the standard release of the BSIM4 model is done in SPICE3 in C language.

We have also verified the model by fitting it to measured noise data from [113]. ICCAP is used for fitting. Fig. 6.10 shows the comparison of the extracted model to measured data. Basic parameters for modeling mobility degradation (U0, UA, UB), thershold voltage and DIBL (VTH0, ETA0), velocity saturation (VSAT) and bulk charge effects (A0, AGS) are extracted from drain current DC data. For modeling the drain noise, we have used the following expression:

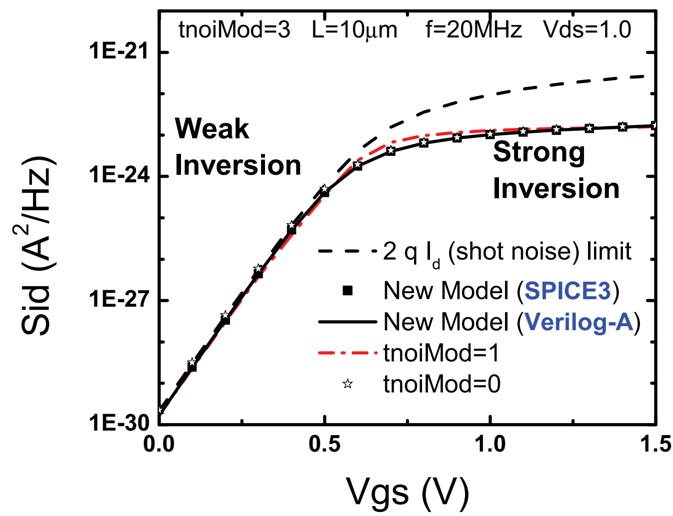
$$S_{id} = 4kT \cdot \gamma g_{d0} \cdot \underbrace{3 \cdot \beta_{tnoi}^2}_{excess\ drain\ noise} \tag{6.50}$$

$$\beta_{tnoi} = RNOIA \cdot \left[1 + TNOIA \cdot L_{eff} \cdot \left(\frac{V_{gsteff}}{E_{sat}L_{eff}}\right)^2\right] \tag{6.51}$$

The $3 \cdot \beta_{tnoi}^2$ term is multiplied to the original expression (Equation 6.48a) to allow some tuning flexibility. The default value of $RNOIA$ is 0.577, which means $3 \cdot \beta_{tnoi}^2 = 1$ by default. We are able to fit the drain noise versus gate voltage with $RNOIA = 0.75$ and $TNOIA = 0$. This corresponds to a γ value of 1.13 instead of the long channel theoretical value 0.67. Therefore although we are able to capture the bias and length dependences of drain noise, we need to scale the model by a factor of 1.7. This is possibly due to excess drain noise, as we will discuss in Section 6.5.

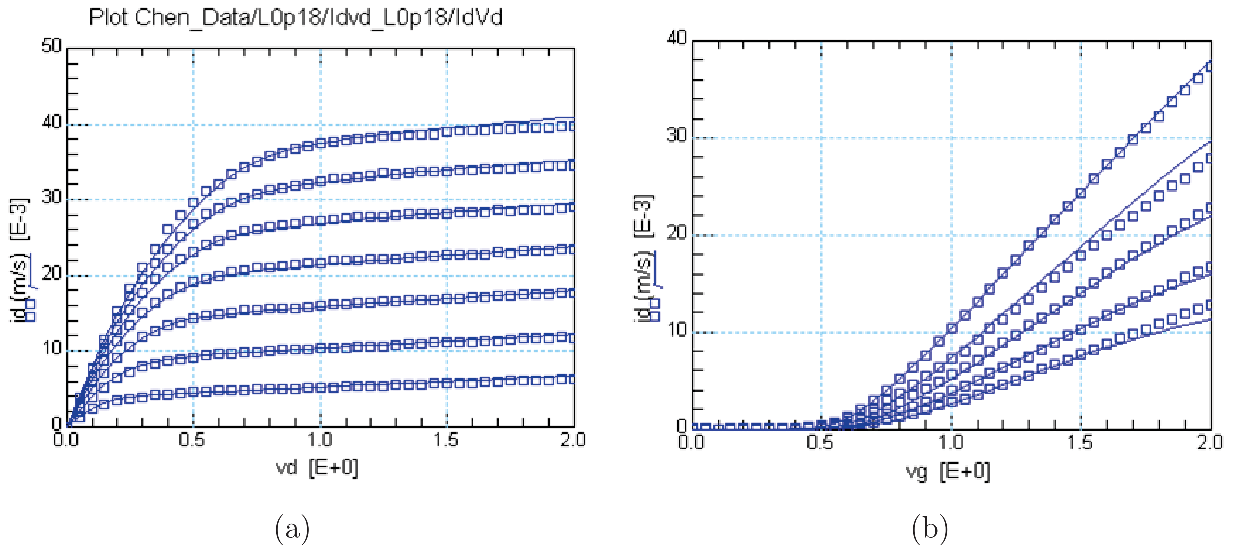


(a)

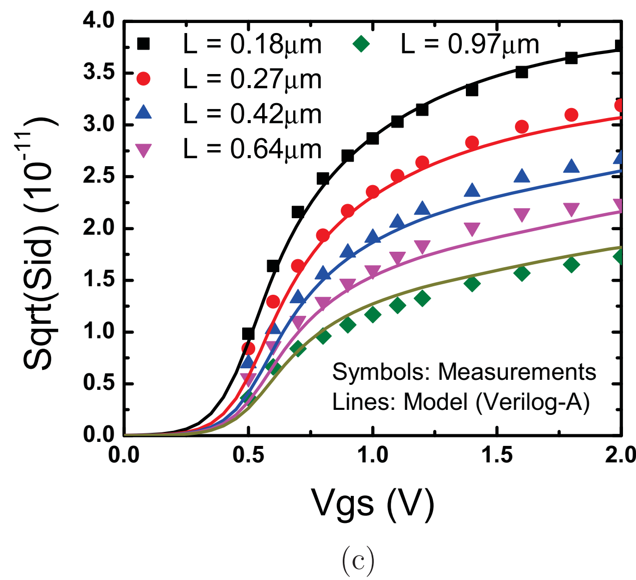


(b)

Figure 6.9: Validation of the drain noise model for both weak and strong inversion. (a) γ versus drain voltage at weak ($V_{gs} = 0$) and strong ($V_{gs} = 2.0$) inversion (b) Drain noise versus gate voltage. In weak inversion drain noise coincides with $2qI_d$.



(a) (b)



(c)

Figure 6.10: Parameter extraction results for (a) $I_d - V_{ds}$ at $L = 0.18\mu m$, (b) $I_d - V_{gs}$ at five different gate lengths ($0.97\mu m$, $0.64\mu m$, $0.42\mu m$, $0.27\mu m$ and $0.18\mu m$), and (c) drain noise (S_{id}) at those gate lengths. The measured data shown here is digitized from [113]

6.4 Implementing Correlated Noise Sources in SPICE3

To utilize the new noise expressions in circuit simulation, they must be implemented in a compact model. In this section we will discuss about how correlated noise sources are implemented in BSIM4 in Berkeley SPICE3 [112]. The same technique is applicable to other circuit simulators as well.

Alternatively, correlated noise sources can be implemented as part of a compact model in the form of Verilog-A code. In that case what we will discuss in this section does not apply. As of today's Verilog-A standard, one or more new nodes need to be introduced to model correlated noise. In the Verilog-A version of the PSP model, two additional nodes are added to model correlated drain and gate thermal noise [59]. A tutorial on the implementation of correlated noise sources in Verilog-A is available in the public domain [124].

6.4.1 Implementation

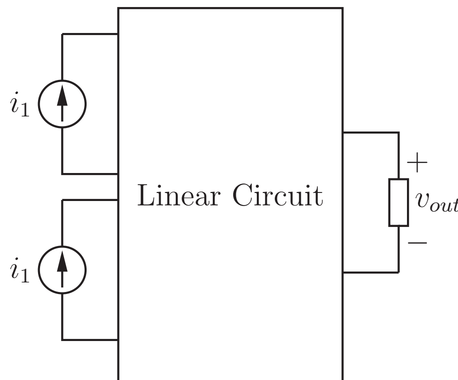


Figure 6.11: Circuit for illustrating the concept of noise gain

In SPICE3, noise simulation of an analog circuit block is performed by analyzing its small signal equivalent circuit, containing several current noise sources, and calculating the total noise contribution at an output terminal of interest.

Fig. 6.11 shows an example noise analysis problem with two current noise source, i_1 and i_2. The noise magnitude of interest is that across the load element v_{out}. Since a small signal circuit is linear, the transfer function from each current source to the output is also linear. For the system in Fig. 6.11, we can write:

$$v_{out} = Z_1 \cdot i_1 + Z_2 \cdot i_2 \tag{6.52}$$

where Z_1 and Z_2 are the transimpedance from $i_{1(2)}$ to v_{out}. In SPICE3, Z_1 and Z_2 are computed efficiently using the adjoint system method [125, 126].

In the original SPICE3 code, the current noise sources are assumed to be uncorrelated. Therefore the output noise is given by [6]

$$\overline{v_{out}^2} = \|Z_1\|^2 \cdot \overline{i_1^2} + \|Z_2\|^2 \cdot \overline{i_2^2} \tag{6.53}$$

However, when the two noise sources are correlated, the cross term $\overline{i_1{}^* i_2}$ is no longer zero and Equation (6.53) is no longer valid.

To model partially-correlated noise sources, we divide the one of the noise sources, say i_1, into an uncorrelated component ($i_{1,u}$) and a component that is fully-correlated with the other noise source i_2 ($i_{1,f}$):

$$i_{1,f} = |c| \cdot i_1 \tag{6.54}$$

$$i_{1,u} = \sqrt{1 - |c|^2} \cdot i_1 \tag{6.55}$$

The above partition method ensures the two noise component adds up to the total noise:

$$\overline{i_1^2} = \overline{i_{1,f}^2} + \overline{i_{1,u}^2} \tag{6.56}$$

Since $i_{1,f}$ and i_2 are fully correlated, we may assume i_2 is at a phase ϕ ahead of $i_{1,f}$. Without loss of generality, the output due to the fully correlated parts can be written as

$$v_{out,f} = \|i_{1,f}\| \cdot Z_1 + \|i_2\| e^{j\phi} \cdot Z_2 \tag{6.57}$$

Finally, the total output noise, expressed in terms of noise magnitudes of i_1 and i_2, is

$$\begin{aligned} \overline{v_{out}^2} &= \left\| \|i_{1,f}\| \cdot Z_1 + \|i_2\| e^{j\phi} \cdot Z_2 \right\|^2 + \overline{i_{1,u}^2} \cdot \|Z_1\|^2 \\ &= \left\| |c| \cdot \sqrt{\overline{i_1^2}} \cdot Z_1 + \sqrt{\overline{i_2^2}} \cdot e^{j\phi} \cdot Z_2 \right\|^2 + \sqrt{1 - |c|^2} \cdot \overline{i_1^2} \cdot \|Z_1\|^2 \end{aligned} \tag{6.58}$$

We have implemented the above expression in SPICE3 by re-writing its noise calculation formula. The details are available in Appendix D.

In the case of correlated drain and gate noise in CMOS, $\overline{i_1^2}$ is the drain noise, $\overline{i_2^2}$ is the induced gaet noise, $|c| = \frac{\epsilon}{\sqrt{\gamma \cdot \delta}}$ is the correlation coefficient and $\phi = \frac{\pi}{2}$.

6.4.2 Verification

To verify the implementation of correlated noise in SPICE3, we simulate the noise figure of a common-source low noise amplifier (LNA) circuit and compare the outcome with theoretical

[6] Please refer to `$(SPICE_DIRECTORY)/src/lib/ckt/nevalsrc.c` for the source code of the function `NevalSrc()`, which is used to calculate gain and output noise contribution

calculations. The circuit schematic is shown in Fig. 6.12. MOSFET M1 is biased in saturation at $V_g = 0.6V$ and $V_d = 1.0V$ through large inductors L_{bias1} and L_{bias2}. C_{thru1} and C_{thru2} are large AC coupling capacitors. The output of the LNA is loaded with a 50Ω noiseless resistor. Matching network L_m and C_m is designed so that the minimum noise figure occurs when R_p is approximately 50Ω. For simplicity we turned off flicker noise, parasitic source and drain resistance noise, and gate resistance noise in the SPICE3 simulation.

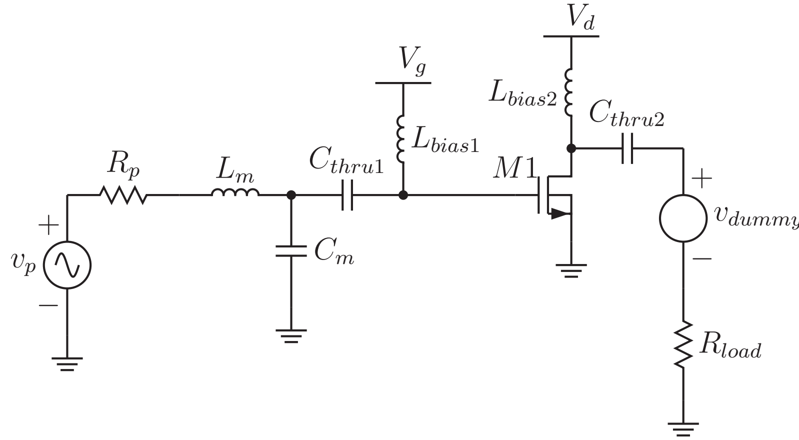


Figure 6.12: Common-source low noise amplifier circuit

To be able to tune the correlation coefficient in SPICE3, we introduce a new fitting parameter $RNOIC$, so that

$$c = j\frac{\epsilon}{\sqrt{\delta \cdot \gamma}} \cdot \frac{RNOIC}{0.395} \tag{6.59}$$

The theoretical noise figure is calculated using the following expression:

$$F = 1 + \frac{S_{ig}(1-|c|)^2 \|\frac{Y_{21}}{Y_s+Y_{11}}\|^2 + \left\| \sqrt{S_{ig}}(-j|c|)\frac{Y_{21}}{Y_s+Y_{11}} + \sqrt{S_{id}} \right\|^2}{4kTG_s \|\frac{Y_{21}}{Y_s+Y_{11}}\|^2} \tag{6.60}$$

where the equivalent source admittance Y_s is given by

$$Y_s = \frac{1}{R_p + j\omega L_m} + j\omega C_m \tag{6.61}$$

and the source conductance is

$$G_s = Re(Y_s) \tag{6.62}$$

The values of C_m, L_m, S_{id}, S_{ig}, c, Y_{11} and Y_{21} are listed in table 6.2.

We simulate the noise figure versus source resistance, R_p in SPICE3 for two different values of correlation coefficients, $c = j0.0473$ and $c = j0.395$ and compare with theoretical

Table 6.2: Parameter values for the common-source LNA in Fig. 6.12

Parameter name	**Value**
Frequency	1GHz
L_m	$133nH$
C_m	$148fF$
Width of $M1$	$50\mu m$
Length of $M1$	$0.13\mu m$
S_{id}	1.447052×10^{-21}
S_{ig}	2.709046×10^{-27}
Y_{11}	$2.208424 \times 10^{-16} + j3.004073 \times 10^{-4}$
Y_{21}	$6.007558 \times 10^{-2} - j1.048002 \times 10^{-4}$
c (RNOIC=0.85)	j0.395
c (RNOIC=0.1)	j0.0473

calculations. The result is shown in Fig. 6.13. We can see that the minimum noise figure occurs when R_p is about 50Ω, as we designed, for the case of $c = j0.395$. Also, the minimum noise figure and the optimum source resistance are both a function of the correlation coefficient. On the same graph we also show the theoretical calculation results. The SPICE3 simulation results match the theoretical calculation very well.

6.5 Modeling Excess Noise for Short Channel Devices

The long channel theoretical value of γ is $\frac{2}{3}$ in the saturation region. For short channel devices, however, the measured γ is usually larger than $\frac{2}{3}$ (see, for example, [108]). In this section, we will disscuss about the several possible explanation:

1. **Hot Carrier Effects:** Since carriers in the MOSFET channel has finite kinetic energy, the electron temperature [7] (T_e) is higher than the equilibrium lattice temperature (T). When this effect is significant these electrons become "hot carriers." Quantitative relation of T_e, the electron velocity, and the horizontal electric field is given by [127]

$$\frac{\frac{3}{2}k(T - T_e)}{\tau_e} = q\mathcal{E}v \tag{6.63}$$

[7] Without loss of generality, we focus on n-type devices in this discussion

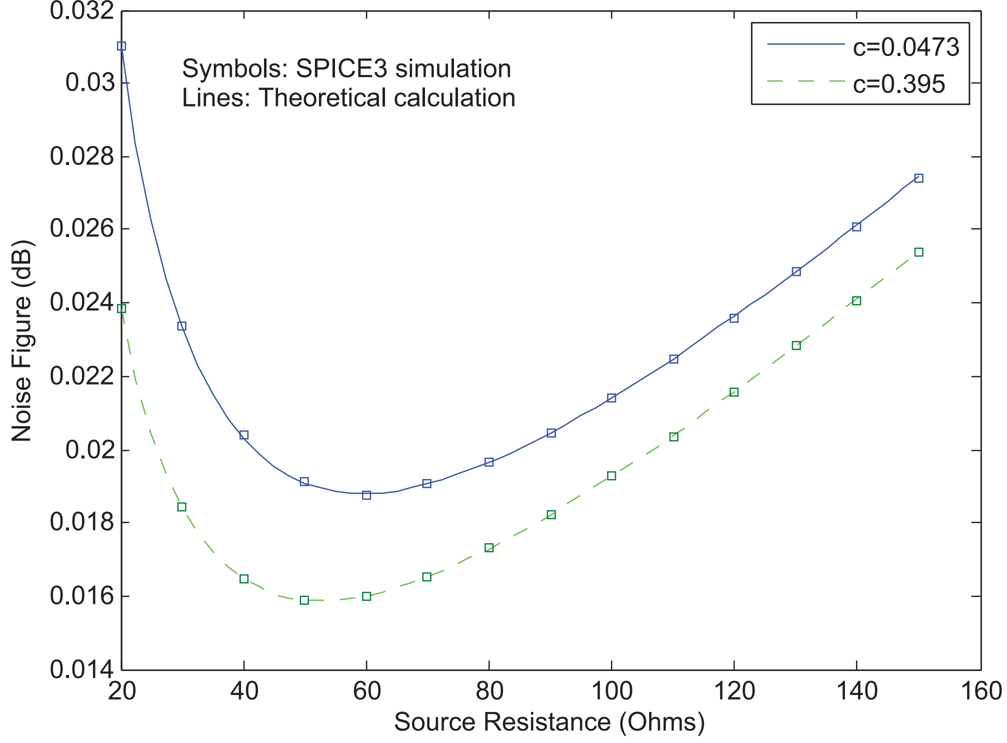


Figure 6.13: Common-source LNA simulation results

It is possible to account for hot electrons in the drain noise expression by simply replacing T with T_e in Equation (6.28):

$$S_{id} = \frac{1}{I_d L_{vsat}^2} \int_0^{V_{DS}} 4kT_e g_0(V)^2 dV \tag{6.64}$$

If we carry out the integration, we obtain a new expression for γ:

$$\begin{aligned} \gamma \;&=\; \frac{2}{3}\left(\frac{L_{vsat}}{L}\right)^{-1}\left[\frac{1+\eta+\eta^2}{1+\eta} + \right. \\ &\left. \frac{\mu_0 q \tau_e (1+\eta)}{2kTL_{vsat}^2} \cdot V_{ds}^2 \cdot \left[1 - \frac{V_b(1+\eta)}{2E_{sat}L_{vsat}} \ln\left(1 + \frac{1-\eta}{\frac{V_{ds}(1+\eta)}{2E_{sat}L_{vsat}} - 1}\right)\right]\right] \end{aligned} \tag{6.65}$$

The above expression predicts an increasing γ with decreasing channel length, as shown in Fig. 6.14. Klein [128] has modeled drain noise due to hot carrier effects with similar assumptions. On the other hand, in [105] it is argued that hot carrier effects should not be taken into account explicitly to avoid double-couting of non-equilibrium effects. Deen and Chen [107] showed that hot electron effects may not be important. Given these uncertainties we decided not to include hot electron effects in the new thermal noise model.

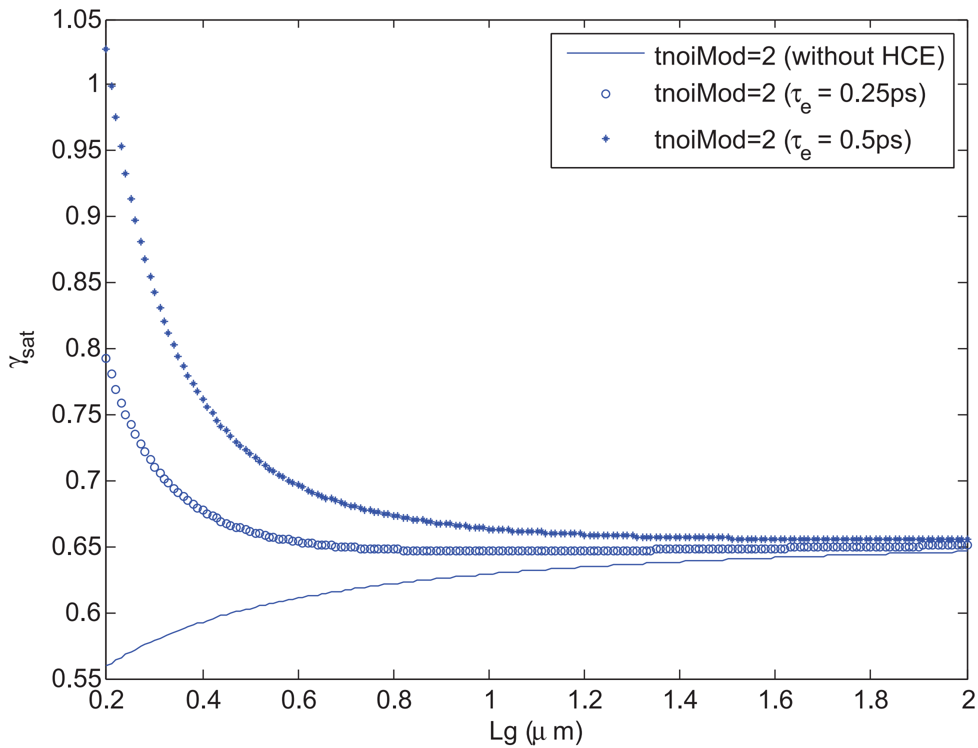


Figure 6.14: Length dependence of γ with and without considering hot carrier effects (HCE). In the curve without HCE, γ decreases with decreasing channel length due to velocity saturation.

2. **Drain Induced Barrier Lowering (DIBL):** According to the long channel thermal noise theory, γ is independent of L and V_{ds} in saturation region. However, for short channel devices, the threshold voltage decreases with increasing V_{ds} due to DIBL,

causing G_{d0} to increase with V_{ds} even in the saturation region. As a result, from Equation 6.48a, γ increases with V_{ds} in the saturation region. The newly developed thermal noise model, as implemented in BSIM4, automatically take this into account. This is because the noise is expressed in terms of V_{gsteff}, which represents the inversion charge density at the source normalized to C_{ox}, and V_{gsteff} increases with V_{ds} when the DIBL effect is turned on. There is no need to explicitly model DIBL in the thermal noise expressions. To confirm this, we simulate the drain noise using BSIM4 with different values of ETA0 [8]. Fig. 6.15 shows the simulation results. As expected, γ increases with V_{ds} in the saturation region. The slope is approximately proportional to ETA0. Moreover, the shape of γ versus V_{ds} is consistent with the model and experimental data in [129].

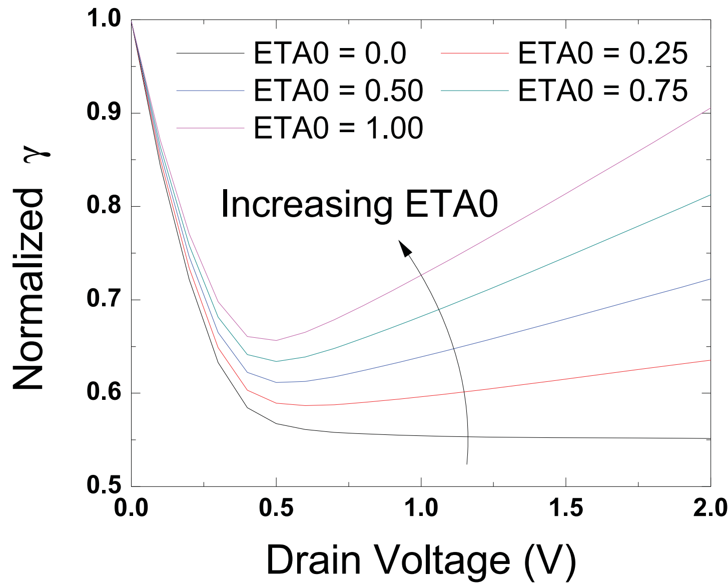


Figure 6.15: SPICE simulation results showing the drain bias dependence of γ in the presence of DIBL effects. For the modelcard we have used, the amount of V_{th} shift due to DIBL is $0.119 \times V_{ds}(V) \times ETA0$.

3. **Channel Length Modulation:** Equations (6.48a-f) are derived for the gradual channel region of the MOSFET. Therefore, in those expressions the length (L) to be used is the electrical channel length, L_{elec}, which does not include the length of the velocity saturation region, rather than L_{eff}. In the presence of the channel length modulation effect, L_{elec} shrinks with increasing drain bias, causing the thermal noise γ to increase

[8] ETA0 is a parameter in BSIM4 to model DIBL effects

with drain bias. This is a significant contributor to the excess drain current thermal noise [107]. In BSIM4, the drain current model takes channel length modulation into account with a multiplication factor $1 + \frac{1}{C_{clm}} \ln\left(\frac{V_A}{V_{Asat}}\right)$. Since both I_{ds} and S_{id} are proportional to $1/L$, we may account for the channel length modulation effect in the drain current noise by multiplying the same factor to γ:

$$\gamma' = \gamma \cdot \left[1 + \frac{1}{C_{clm}} \ln\left(\frac{V_A}{V_{Asat}}\right)\right] \tag{6.66}$$

where C_{clm}, V_A and V_{Asat} are defined in the BSIM4 User's Manual [130]. Note that the drain noise contribution due to noise in the velocity saturation region is neglected in this study. Since the channel conductance in the velocity saturation region is small, we don't expect it to have a significant contribution.

6.6 Thermal Noise Modeling for BSIM-MG

Although multi-gate CMOS devices are being extensively studied for its digital applications, at the present time thermal noise data for multi-gate CMOS devices are still very limited. Nevertheless, since multi-gate MOSFETs are based on the same metal-oxide-semiconductor gate stack as planar bulk MOSFETs, we expect the thermal noise to behave similarly. For multi-gate devices, it is reasonable to model thermal noise in the same framwork as bulk MOSFETs.

In Section 6.3 we already developed expressions for noise in terms of inversion carrier densities at the source and drain, which is Equations (6.47a-c). We can use the same model for BSIM-MG, with a slight modification.

One unique feature of fully-depleted multi-gate devices is the absence of bulk charge effects. Therefore, we need to modify the jacobian (for bulk it is Equation 6.46) to

$$\frac{dV}{dq_i} = -V_t \cdot \frac{q_i + \xi}{q_i} \tag{6.67}$$

where ξ is given in Section XX, Equation XX. If we carry out the integration, the final result will be the same as Equations (6.47a-c) but with all A_{bulk} terms replaced with ξ.

6.7 Conclusion and Future Work

In this work we developed analytical expressions for the MOSFET channel thermal noise, including the drain noise, the induced gate noise, and the correlation coefficient. The expressions are successfully implemented in the BSIM4 model as part of Berkeley SPICE3. In the past, SPICE3 does not support the modeling of correlated noise sources. With a slight

modification in the SPICE3 code, we are able to carry out the implementation and verify it with a low noise amplifier noise figure simulation. The model is valid in all regions of operation, including weak inversion and strong inversion. In strong inversion, we have verified the model with a segmented channel transistor. In weak inversion, the asymptotic behavior is consistent with theory. Excess drain noise for short channel devices is also studied. We modeled excess noise due to channel length modulation and drain induced barrier lowering. Hot carrier effects and noise originating in velocity saturation region is neglected, since they are likely insignificant.

Although we have confirmed that the model fits drain noise data presented by Chen and Deen, more verification is needed to verify the induced gate noise model and the correlation coefficient model to measured data, and to verify the drain bias dependence of the drain current noise model. Another possible noise source, the avalanche noise, is yet to be studied. One additional aspect that needs to be further examined is the frequency dependence of noise. Although generally drain current noise has no frequency dependence, there has been reports of excess noise at very high frequency for devices operating in the non quasi-static regime.

Chapter 7

Conclusions

7.1 Summary and Future Research Directions

In this section, the contribution of this dissertation research is summarized and future research directions are suggested.

7.1.1 Independent Multi-gate MOSFET Model BSIM-IMG

Achieving computational efficiency and accuracy simultaneously for surface potential calculation for independent double-gate FETs is challenging, even with the approximations for long channel devices [46]. In this dissertation research, we have derived an approximation for the surface potential, which is explicit and therefore robust and computationally efficient. Accurate core drain current formulation is derived without making the charge sheet approximation. Terminal charge model is also developed. The core model, along with all real device effect models, are implemented into BSIM-IMG. The model has good convergence, accuracy, and computational efficiency, and is validated with both TCAD and experimental data. Through an internship, a global extraction methodology for BSIM-IMG was developed and tested on a real ETSOI technology [65].

One future research direction is to enhance BSIM-IMG to also support the independent-gate FinFET [18], another type of multi-gate device with independent front- and back-gate control. The independent-gate FinFET can be used for several novel applications, including the single transistor mixer [131] and dynamic feedback FinFET SRAM [32]. Yet another novel device that needs dual-gate inversion the top-and-bottom double gate MOSFETs for sensor applications.

For dual gate inversion a computationally efficient numerical method for surface potential calculation that supports dual-gate inversion is needed. The drain current model that supports dual-gate inversion is available [34]. However, a new terminal charge model and the enhancement of real device effect modeling are required.

Another model that needs to be added to BSIM-IMG is the effective oxide capacitance due to quantum effects.

7.1.2 Common Multi-gate MOSFET Model BSIM-CMG

The basic core model for common multi-gate MOSFETs, as well as the modeling of short channel effects, quantum effects and corner effects was researched in prior dissertation works [34, 96]. In this dissertation, an enhanced version of the core model is derived, making BSIM-CMG compatible with a novel computationally efficient way of implementing non quasi-static effect models — charge segmentation. In addition, various real device effect models are added into BSIM-CMG, including temperature dependence, thermal and flicker noise models, self heating, parasitic fringe capacitances [78] and parasitic source/drain resistances. A new core model for cylindrical gate FETs has also been implemented into BSIM-CMG, making it suitable for applications such as nanowire and cylindrical-gate FET modeling [17]. Furthermore, a global extraction methodology for multi-gate FETs is developed and tested on a real FinFET technology [63].

In the future, cylindrical-gate FETs are expected to be widely used by the industry for memory technologies, due to the significant benefits in area reduction by using vertical cylindrical-gate devices [17]. Geometry-dependent parasitics are likely to be very different from the FinFETs. Compact models for parasitic resistances and capacitances in vertical cylindrical-gate FETs need to be developed.

7.1.3 Symmetry of MOSFET Compact Models

In order to use compact models for devices operating at $V_{ds} = 0$ in analog circuits, such as the passive mixer, the model equations must exhibit symmetric characteristics to avoid discontinuity at the $V_{ds} = 0$ point due to source and drain swapping. In this dissertation, it is proven that the physically derived core models for BSIM-MG preserves source-drain symmetry. Furthermore, five rules for adding real device effect corrections on top of a symmetric model are described in detail. We have learned these rules while implementing real device effect models into BSIM-CMG and BSIM-IMG and performing thorough testing. These rules serve as important guidelines for future compact device model developers.

In the future, these rules can be applied to different compact models. Modifying BSIM4 to satisfy these requirements may be difficult due to the number of real device effect models that needs modifications. An ongoing work is the development of the charge-based BSIM6, which already has a symmetric core model. Real device effect corrections are currently being added according to the symmetry guidelines.

For threshold based model it is possible to implement a V_{dseff} function that makes the model ∞-continuous at $V_{ds} = 0$ [132]. However, most existing surface potential based compact models are not ∞-continuous at $V_{ds} = 0$. This is due to the form of the smoothing function for the effect drain to source voltage, V_{dseff}. Therefore, another useful research

direction is to find a novel way to implement V_{dseff} in surface potential based models to ensure continuity in high order derivatives.

7.1.4 Modeling Source and Drain Resistances for the FinFET

In this dissertation, we have developed compact models for source/drain resistances in FinFETs with raised source and drain, considering both the geometry and bias dependences. Analytical expressions are derived for the extension resistance, spreading resistance, and contact resistance. The transmission-line based contact resistance model predicts the dependence of R_{ds} on geometrical parameters such as the cross sectional shape and area of the raised source and drain, and considers various different contact silicidation schemes. The extension resistance exhibits bias dependence due to the fringe field originating from the gate. Good agreement with TCAD simulation is observed. A breakdown analysis shows that the extension and contact resistances are the dominant components.

In the future, we would like to further validate the model using experimental test structures, which is not available at the time this dissertation research is carried out.

7.1.5 Compact Modeling of Variation in FinFETs

BSIM-CMG is used to study manufacturing variation in FinFET SRAM cells. A Monte Carlo simulation framework is develop to consider both local and global variation. Various sources of variation, such as the fin height, fin thickness, gate length, and gate dielectric thickness are included. An important conclusion of this study is that non-Gaussian threshold distribution is observed, and our physical compact simulation framework is able to captures that.

In the future, the same procedure can be applied to independent-gate FinFETs, once a model that supports back-gate inversion becomes available. A more thorough investigation of FinFET SRAM variation requires more data to be collected. In this work, global variation is assumed to have a standard deviation that is 10% of the nominal parameter value. One possible improvement of the modeling procedure is to separate global and local variation through additional calibration. Another improvement is to be able to find out the analytical form of the measurement distributions. For example, the threshold voltage is an exponential function of gate length variation, therefore it may follow a lognormal distribution. The advantage of this is the ability to predict yield at the distribution tail without running billions of Monte Carlo runs.

7.1.6 Thermal Noise Modeling

Thermal noise is crucial for high frequency analog CMOS circuits. The final part of this dissertation work is to derive analytical expressions to model thermal noise. The expressions are verified against a segmented channel transistor. The drain noise part is also verified with experimental data collected from the literature. The result of the analytical model is

implemented in the industry standard BSIM4 model. It is also suitable for implementation in BSIM-MG.

The validation of induced gate noise and correlation coefficient is somewhat more difficult, mainly due to measurement challenges. Therefore a future work is to validate the model with advanced CMOS technologies for the induced gate noise and noise correlation. Moreover, the length dependence of drain noise needs to be further validated for sub-45nm devices, as the noise behavior may change due to the different transport mechanism. Furthermore, although thermal noise is generally considered frequency independent, such assumption is only valid in the quasi static regime. Near the non quasi-static regime, thermal noise can be frequency dependent. This needs to be modeled in order to design very high frequency analog CMOS.

7.2 Conclusion

Multiple-gate MOSFETs will be used for future CMOS. In preparation for this, two multiple-gate MOSFET compact models are developed: BSIM-CMG for common multi-gate MOSFETs, and BSIM-IMG for independent multi-gate MOSFETs. Special attention is paid to accuracy, computational efficiency, and robust convergence, making these model suitable for circuit simulation in the next generation CMOS technology. The model is complete and contains most features necessary for analog and digital simulations, including short channel effects, mobility, output conductance, and leakage models, all parasitic resistance and capacitances, electronic noise models, temperature dependence and self heating, etc. By following five symmetry rules we successfully made the model satisfy Gummel Symmetry and suitable for analog circuit design. We will use these rules to further guide our future compact model development.

Addition topics related to MOSFET modeling are studied, including the access resistance modeling for raised source and drain FinFETs, the manufacturing variation in FinFET SRAM cells, and thermal noise. The results we obtained serve as guidelines for future device design, device modeling, and circuit design.

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Appendix A

Back Surface Potential and Inversion Charge Calculation in BSIM-IMG

In this appendix we show how the integrated charge density (Q_{inv}) and the back surface potential (ψ_{s2}) are calculated as function of the front surface potential (ψ_{s1}). We first re-write Equation (2.6) in a more general form:

$$\left(\frac{d\psi}{dx}\right)^2 - A \cdot \exp\left(\frac{q(\psi - V_{ch})}{kT}\right) = D \tag{A.1}$$

where $A = \frac{2N_c kT}{\epsilon_{si}}$ and D is the determinant, which is position-independent. D can be calculated as function of ψ_{s1} by evaluating Equation (A.1) at the front surface, or $x = -\frac{T_{si}}{2}$. To integrate Equation (A.1) we consider the following two cases:

1. $D < 0$:

   $D < 0$ is the solution for which a potential minimum exists. There are 3 possible locations for the potential minimum ψ_0 [51], as illustrated in Fig. A.1. ψ_0 may be located in between ψ_{s1} and ψ_{s2} (Fig. A.1(a)), to the left of ψ_{s1} (Fig. A.1(b)), or to the right of ψ_{s2} (Fig. A.1(c)). The three possibilities are handled in a unified manner. First, we find t_{01}, the spatial distance from ψ_{s1} to ψ_0. Integrating equation (A.1) we have,

$$x = \pm\left(\frac{2kT}{q\sqrt{-D}}\right)\cos^{-1}\left[\sqrt{-\frac{D}{A}\exp\left(-\frac{q(\psi - V_{ch})}{kT}\right)}\right] + c_1 \tag{A.2}$$

   Evaluating equation (A.1) at ψ_0, we obtain,

$$-\frac{D}{A}\exp\left(-\frac{q(\psi_0 = V_{ch})}{kT}\right) = 1 \tag{A.3}$$

. t_{01} is calculated by evaluating equation (A.2) at ψ_{s1} and ψ_0 and taking the absolute value of the difference.

$$t_{01} = \left| \left(\frac{2kT}{q\sqrt{-D}} \right) \cos^{-1} \left[\sqrt{-\frac{D}{A} \exp\left(-\frac{q(\psi_{s1} - V_{ch})}{kT} \right)} \right] \right| \tag{A.4}$$

Next, t_{02}, the distance from ψ_0 to ψ_{s2} is computed as follows:

$$t_{02} = \begin{cases} |T_{si} - t_{01}| & E_{s1} > 0 \\ T_{si} + t_{01} & E_{s1} \leq 0 \end{cases} \tag{A.5}$$

Finally, ψ_{s2} is calculated as a function of t_{02} using the inverse function of equation (A.4):

$$\psi_{s2} = V_{ch} - \frac{kT}{q} \ln \left\{ \frac{A}{-D} \cos^2 \left[\left(\frac{q\sqrt{-D}}{2kT} \right) t_{02} \right] \right\} \tag{A.6}$$

The electric field at the back surface is given by:

$$E_{s2} = -\frac{\partial \psi_{s2}}{\partial t_{02}} = -\sqrt{-D} \tan \left[\left(\frac{q\sqrt{-D}}{2kT} \right) t_{02} \right] \tag{A.7}$$

2. $D > 0$:

   $D > 0$ is the solution for which there is no potential minimum (top curve in Fig. A.1(d)). We again integrate equation (A.1) as follows

$$T_{si} = \int_0^{T_{si}} dx = sgn(E_{s1}) \cdot \int_{\psi_{s1}}^{\psi_{s2}} \frac{d\psi}{\sqrt{A \cdot \exp\left(\frac{q(\psi - V_{ch})}{kT} \right) + D}} \tag{A.8}$$

   The result is (different from equation (A.2) because of the sign of D):

$$\psi_{s2} = V_{ch} + \frac{kT}{q} \ln \left[\frac{D}{A} \left(\frac{2C}{1 - C^2} \right)^2 \right] \tag{A.9}$$

   where

$$C = \left[\sqrt{\frac{D}{A} \exp\left(-\frac{q(\psi_{s1} - V_{ch})}{kT} \right) + 1} - \sqrt{\frac{D}{A} \exp\left(-\frac{q(\psi_{s1} - V_{ch})}{kT} \right)} \right] \times \exp \left[-sgn(E_{s1}) \frac{q\sqrt{D}}{2kT} T_{si} \right] \tag{A.10}$$

   The electric field at the back surface is

$$E_{s2} = -\frac{\partial \psi_{s2}}{\partial T_{si}} = -sgn(E_{s1}) \cdot \sqrt{D} \frac{1 + C^2}{1 - C^2} \tag{A.11}$$

Finally, regardless of the sign of D, the inversion carrier density is given by Gauss' Law:

$$Q_{inv} = \epsilon_{si}(E_{s1} - E_{s2}) \tag{A.12}$$

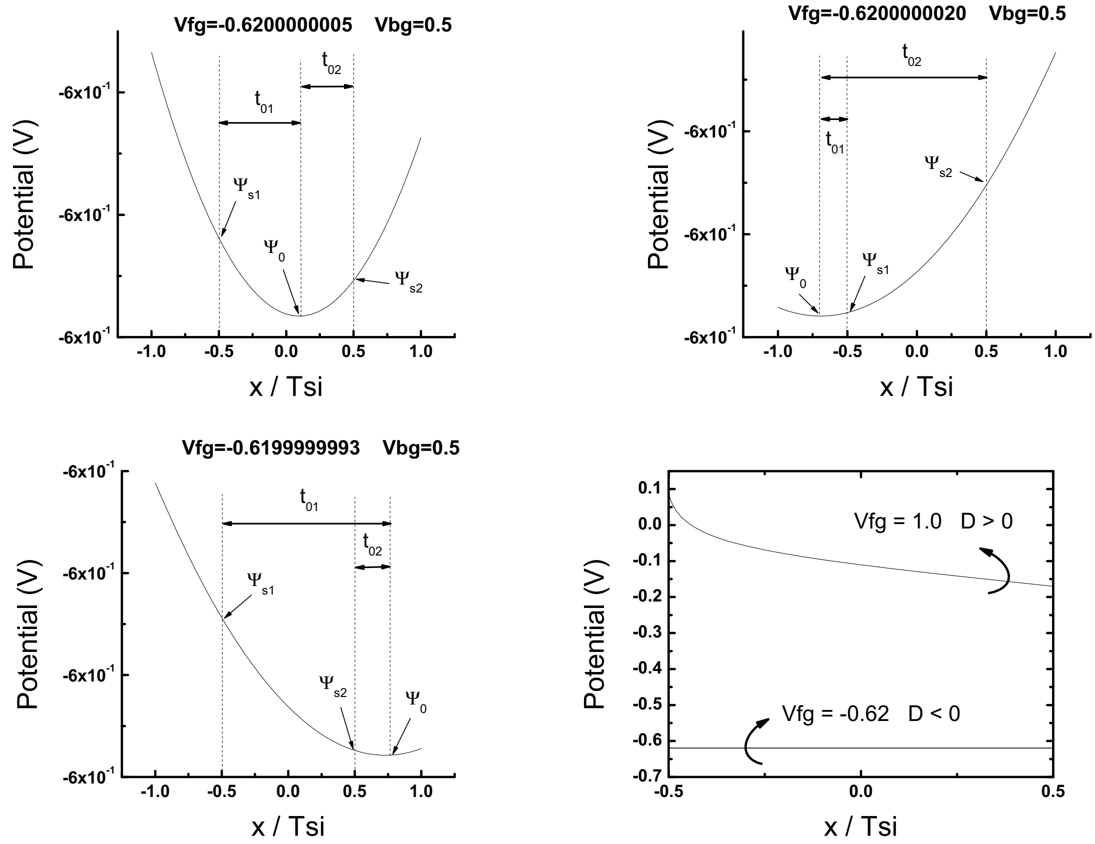

Figure A.1: Solution to the Poisson's equation when (a) $D < 0$ and the potential minimum (ψ_0) is located inside the body; (b)(c) $D < 0$ and ψ_0 is located outside the body; (d) $D > 0$ and there is no potential minimum [51]. The $D < 0$ cases are also plotted in (d) for comparison. The back-gate voltage is fixed at $V_{bg} = 0.5$. The front-gate voltage varies, as listed in the figures. ($T_{ox1} = 1.2nm$, $T_{si} = 15nm$, $T_{ox2} = 20nm$, $\Phi_{g1} = 4.05V$, $\Phi_{g2} = 5.17V$)

Appendix B

Monte Carlo Based Framework for FinFET SRAM Variation Simulation

In this appendix we describe the Monte Carlo framework for the simulation of FinFET SRAM variation for the study in chapter 5.

The framework is written in the Perl programming language. It consists of a main Perl script, `variation3.pl` and many input files that describes the variation information.

`sram.subckt` is a sub-circuit netlist that describes the six transistor SRAM cell. There can be 6, 8 or 10 instances of BSIM-CMG in the sub-circuit depending on the number of fins there are for the pull down device. `sram.subckt` is used by three netlist files, `halfcell.sp`, `fullcell.sp` and `wlwm.sp` for the simulation of various design metrics, including the read and write butterfly curves, I_{crit} from n-curve simulations [99], leakage power (P_{leak}), and the word line write margin (WLWM). The three netlist files are passed to HSpice to run circuit simulation. The outputs are collected by the Perl script to analyze the design metrics. A TCL script written by Dr. Leland Chang was used for extracting the read and write static noise margins from the SRAM butterfly curves. The three netlist files uses the modelcard file `tempcard.m` for BSIM-CMG to describe individual FinFET transistors. `tempcard.m` includes all the nominal parameters described by `nominal.dat` but the parameters values are modified to include variation information. The variation is generated by a Gaussian random number generator according to the local and global variation information described by `globalvar.dat` and `localvar.dat`. `globalvar.dat` describes the global variation of parameters H_{fin}, L_g, T_{fin} and T_{ox}. `localvar.dat` is a table that describes the local variation of each parameter (L_g and T_{fin}) for each transistor. For multi-fin pull down devices, each fin is modeled by one instance of BSIM-CMG in order to properly model local variation.

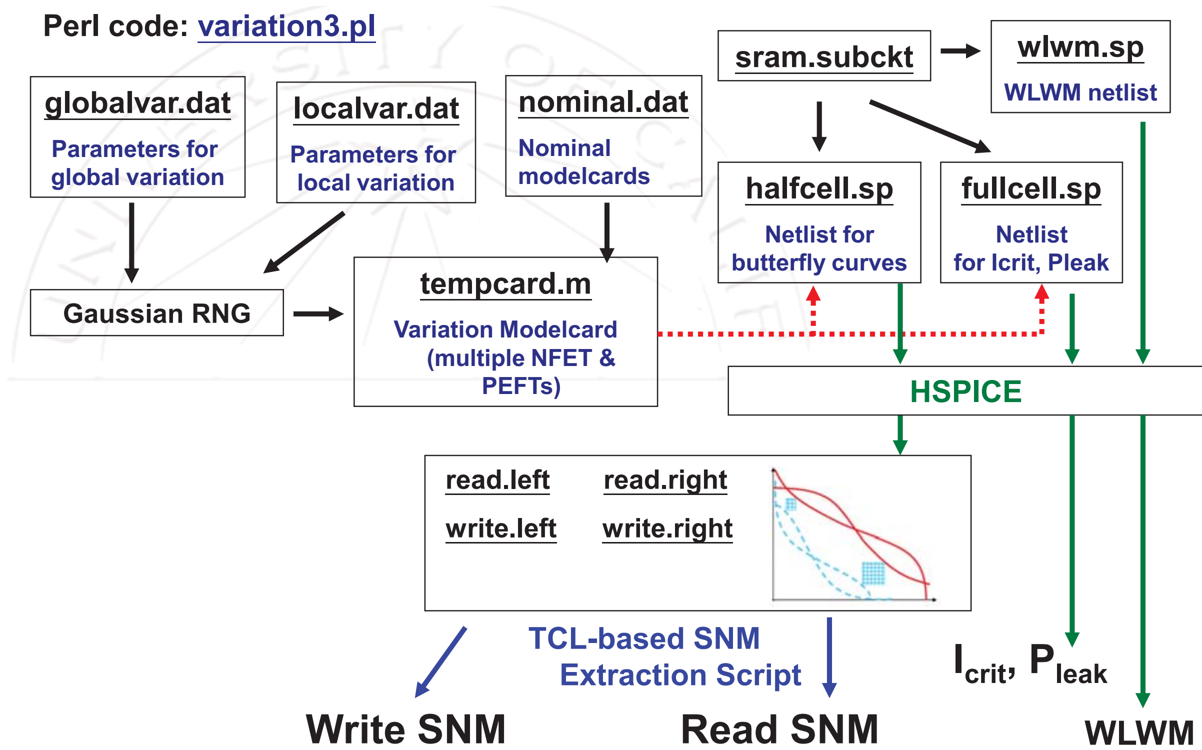

Figure B.1: Monte Carlo Script for FinFET SRAM Variation Simulation

Appendix C

Simple Segmentable BSIM

Following is the Verilog-A code for the simple segmentable BSIM, which is developed for the purpose of verifying the new thermal noise model:

```
// Simple BSIM by Darsen Lu

‘include "disciplines.vams"
‘include "constants.vams"

‘define EPSOX   (3.9 * 8.8542e-12)
‘define EPSSI   (11.7 * 8.8542e-12)
‘define Vtm0    0.0258
‘define q       1.602e-19
‘define ni      1.1e16

module simplebsim(d, g, s, b);

    inout      d, g, s, b;
    electrical d, g, s, b, si, di, nigid;

    parameter integer ISSEGMENT = 0;
    parameter real TOX = 1.0e-9;
    parameter real U0 = 300e-4;
    parameter real ABULK = 1.3;
    parameter real VTH0 = 0.4;
    parameter real NFACTOR = 1.0;
    parameter real NCH = 1.0e22;
```

```
    parameter real VOFF = -0.08;
    parameter real DELTA = 1.0e-5;
    parameter real PCLM = 1.3;
    parameter real XJ = 150e-9;
    parameter real W = 1.0e-6;
    parameter real L = 1.0e-6;
    parameter real VSAT = 8.0e4;
    parameter real VFBCV = -1.0;
    parameter integer TNOIMOD = 0;
    parameter real NTNOI = 1.0;
    parameter real RNOIA = 0.577 from (-inf:inf);
    parameter real RNOIB = 0.37 from (-inf:inf);
    parameter real TNOIA = 1.5e6 from (-inf:inf);
    parameter real TNOIB = 3.5e6 from (-inf:inf);

    real vgs, vgd, vds, vbs, vbd, devsign;
    real cox, phib, phis, cdep, vth, vgsteff, vb, ids;
    real Esat, EsatL, vdsat, vdseff;
    real T0, T1, T2, T3, T4, T5, T0sq;
    real Qg, Qb, Qd, Qs, Qinv, Gtnoi;
    real T, gseltd, gdeltd;
    real npart_beta, npart_theta, gspr, gdpr, IdovVds;
    real Gm, Gds, Gmb, igsquare, Lvsat, noicorl, sigrat, sid;

    analog begin

        vgs = V(g, si);
        vds = V(di, si);
        vbs = V(b, si);

        T = $temperature;

        if(vds < 0) begin
            T0 = vgs - vds;
            T1 = -vds;
            T2 = vbs - vds;
            vgs = T0;
            vds = T1;
            vbs = T2;
```

```
        devsign = -1;
    end else begin
        devsign = 1;
    end
    vbd = vbs - vds;
    vgd = vgs - vds;

    cox = `EPSOX / TOX;
    phib = `Vtm0 * ln(NCH / `ni);
    phis = phib + 0.45;
    cdep = sqrt(`q * NCH * `EPSSI / (2 * phis));

    vth = VTH0 + (ABULK - 1.0) * (-vbs);

    // Vgsteff smoothing (modified)
    T1 = vgs - vth;
    vgsteff = 0.5 * (T1 + sqrt(T1 * T1 + 1.0e-5));

    vb = (vgsteff + 2.0 * `Vtm0) / ABULK;

    Esat = 2.0 * VSAT / U0;
    EsatL = Esat * L;

    if(ISSEGMENT != 0)
        vdsat = (vgsteff + 2.0 * `Vtm0) / ABULK;
    else
        vdsat = EsatL * (vgsteff + 2.0 * `Vtm0) /
            (ABULK * EsatL + vgsteff + 2.0 * `Vtm0);
    T0 = vdsat - vds - DELTA;
    vdseff = vdsat - 0.5 * (T0 +
        sqrt(T0 * T0 + 4 * DELTA * vdsat));

    Lvsat = L * (1.0 + vdseff / EsatL);
    IdovVds = U0 * cox * W / Lvsat * vgsteff *
        (1.0 - 0.5 * vdseff / vb);

    ids = IdovVds * vdseff;

    if(devsign < 0) begin
```

```
        ids = -ids;
    end


    // Charge
    T1 = 12.0 * (vgsteff - 0.5*ABULK*vdseff);
    if(TNOIMOD == 0)
        Qinv = cox * W * L * (vgsteff - 0.5*ABULK*vdseff +
            ABULK*ABULK*vdseff*vdseff / T1);
    Qg = cox * W * L  * (vgsteff + vth - VFBCV - phis -
        0.5*vdseff + ABULK * vdseff * vdseff / T1);
    Qb = cox * W * L  * (VFBCV - vth + phis + 0.5*(1-
        ABULK)*vdseff - (1 - ABULK) * ABULK * vdseff *
        vdseff / T1);
    Qd = -cox * W * L  * (0.5 * vgsteff - 0.5*ABULK*vdseff +
        12.0 * ABULK * vdseff * (vgsteff*vgsteff/6.0 -
        ABULK * vdseff * vgsteff / 8.0 +
        ABULK * ABULK * vdseff * vdseff / 40.0) / T1 / T1);
    Qs = -(Qg + Qb + Qd);

    // Current Assignment
    I(di, si) <+ ids;

    // Rds_eltd
    gseltd = 1.0e3;
    gdeltd = 1.0e3;
    I(s, si) <+ gseltd * V(s, si);
    I(d, di) <+ gdeltd * V(d, di);

    // Noise
    gspr = gseltd;
    gdpr = gdeltd;
    if(TNOIMOD == 0) begin
        T0 = 1.0 - vdseff / (2.0 * vb);
        T1 = 2 - T0 - T0;
        T2 = U0 * W / Lvsat * cox * vgsteff;
        T3 = 1.0 - T1 + T1 * T1 / 3.0;
        Gtnoi = NTNOI * T2 * T2 / IdovVds * T3;
    end else if(TNOIMOD == 1) begin
```

```
        T5 = vgsteff / EsatL;
        T5 = T5 * T5;
        npart_beta  = RNOIA * (1.0 + T5 * TNOIA * L);
        npart_theta = RNOIB * (1.0 + T5 * TNOIB * L);
        Gm = ddx(ids, V(g));
        Gds = ddx(ids, V(di));
        Gmb = ddx(ids, V(b));
        T0 = Gm + Gmb + Gds;
        T0 = T0 * T0;
        igsquare = npart_theta * npart_theta * T0 / IdovVds;
        T1 = npart_beta * (Gm + Gmb) + Gds;
        T2 = T1 * T1 / IdovVds;
        Gtnoi = T2 - igsquare;

        if (vds >= 0.0)
        gspr = gspr * (1.0 + npart_theta * npart_theta
                * gspr / IdovVds);
        else
            gdpr = gdpr * (1.0 + npart_theta * npart_theta
                * gdpr / IdovVds);
    end else begin
        T0 = 1.0 - vdseff / (2.0 * vb);
        T1 = 2 - T0 - T0;
        T2 = U0 * W / Lvsat * cox * vgsteff;
        T3 = 1.0 - T1 + T1 * T1 / 3.0;
        Gtnoi = T2 * T2 / IdovVds * T3;
        T0sq = T0 * T0;
        T4 = (8.0 * T0sq * T0sq + 4.0 * T0sq * T0 +
            3.0 * T0sq - 5.0 * T0 + 1.25) /
            (135.0 * T0sq * T0sq);
        sigrat = Lvsat * Lvsat / (U0 * vgsteff)
            * sqrt(T4 / T3);
        noicorl = ((3.0 * T0 - 1.0) / (T0sq * T0) - 2.0)
            * T0 / (18.0 * sqrt(T3 * T4));
    end
    sid = 4 * `P_K * T * Gtnoi;

    if(TNOIMOD < 2) begin
        I(di, si) <+ white_noise(sid, "thermal");
```

```
        end else begin
            I(nigid) <+ white_noise(sid, "thermal");
            I(di, si) <+ white_noise(
                (1.0 - noicorl*noicorl)*sid, "thermal");
            I(di, si) <+ noicorl*V(nigid);
            I(g, si) <+ ddt(V(nigid)*sigrat);
        end
        I(nigid) <+ V(nigid);   // for correlated noise

        I(d,di) <+ white_noise(4 * `P_K * T * gdpr, "Rd");
        I(s,si) <+ white_noise(4 * `P_K * T * gspr, "Rs");

        if(V(di, si) < 0) begin
            T1 = Qs;
            Qs = Qd;
            Qd = T1;
        end

        I(g, si) <+ ddt(Qg);
        I(b, si) <+ ddt(Qb);
        I(di, si) <+ ddt(Qd);

    end

endmodule
```

Appendix D

Code Listing: Evaluating Output Noise Contribution of Correlated Noise Sources

In this appendix we list the modified parts of the SPICE3 code for computing the noise contribution of the partially correlated gate and drain noise, as a supplement to Section 6.4.

In BSIM4, which is part of SPICE3, noise-related calculations are performed in `b4noi.c`. The following code is an excerpt of `b4noi.c`, in which the evaluation of output noise densities, `noizDens[BSIM4IDNOIZ]` and `noizDens[BSIM4CORLNIOZ]` are illustrated. Note that variables `GammaGd0` (the drain noise normalized to $4kT$), `ctnoi` (correlation coefficient) and `sigrat` (the ratio of the induced gate noise to the drain noise at $\omega = 1$) are available from earlier calculations based on the formula given in Section 6.3.

```
T2 = GammaGd0;
T3 = ctnoi * ctnoi;
T4 = 1.0 - T3;

/* Evaluate output noise contribution of the uncorrelated part of    */
/*   drain noise                                                      */
NevalSrc(&noizDens[BSIM4IDNOIZ],
         &lnNdens[BSIM4IDNOIZ], ckt,
         THERMNOISE, here->BSIM4dNodePrime,
         here->BSIM4sNodePrime, T2 * T4);

/* Add frequency dependence; limit Sig so that it never exceeds Sid  */
omega = 2.0 * M_PI * data->freq;
```

```
T5 = omega * sigrat;
T6 = T5 * T5;
T7 = T6 / (1.0 + T6);

/* Evaluate output noise contribution of the correlated drain        */
/*   noise and induced gate noise                                    */
if (here->BSIM4mode >= 0)  {
    NevalSrc2(&noizDens[BSIM4CORLNOIZ],
              &lnNdens[BSIM4CORLNOIZ],
              ckt,
              THERMNOISE,
              here->BSIM4dNodePrime,
              here->BSIM4sNodePrime,
              T2 * T3,
              here->BSIM4gNodePrime,
              here->BSIM4sNodePrime,
              T2 * T7,
              0.5 * M_PI);
}
else
{
    NevalSrc2(&noizDens[BSIM4CORLNOIZ],
              &lnNdens[BSIM4CORLNOIZ],
              ckt,
              THERMNOISE,
              here->BSIM4sNodePrime,
              here->BSIM4dNodePrime,
              T2 * T3,
              here->BSIM4gNodePrime,
              here->BSIM4dNodePrime,
              T2 * T7,
              0.5 * M_PI);
}
```

`NevalSrc()` is defined in the original SPICE3 code to evaluate the output noise contribution of independent noise sources, whereas `NevalSrc2()` is a newly defined function for evaluating the output noise contribution of fully-correlated noise sources. `NevalSrc2()` is

listed here [1] :

```
/*
 * NevalSrc2 (noise, lnNoise, ckt, type, node1, node2, param, node3,
 *            node4, param2)
 *   This routine is a modified version of NevalSrc() that computes
 *   the output noise due to two fully-correlated noise sources. It is
 *   useful for implementing correlated gate and drain noises in MOSFETs.
 */


#include "spice.h"
#include "cktdefs.h"
#include "const.h"
#include "noisedef.h"
#include "util.h"
#include "suffix.h"

void NevalSrc2 (noise, lnNoise, ckt, type, node1, node2, param1, node3,
                node4, param2, phi21)

double *noise;
double *lnNoise;
CKTcircuit *ckt;
int type;
int node1;
int node2;
double param1;
int node3;
int node4;
double param2;
double phi21;     /* Phase of signal 2 relative to signal 1 */

{
    double realVal1, imagVal1;
    double realVal2, imagVal2;
    double realOut, imagOut, param_gain;
```

[1]The function `NevalSrc2()` can be found in **nevalsrc2.c** in the release of BSIM4.6.6 or later versions

```
    double T0, T1, T2, T3;

    realVal1 = *((ckt->CKTrhs) + node1) - *((ckt->CKTrhs) + node2);
    imagVal1 = *((ckt->CKTirhs) + node1) - *((ckt->CKTirhs) + node2);
    realVal2 = *((ckt->CKTrhs) + node3) - *((ckt->CKTrhs) + node4);
    imagVal2 = *((ckt->CKTirhs) + node3) - *((ckt->CKTirhs) + node4);
    T0 = sqrt(param1);
    T1 = sqrt(param2);
    T2 = T1 * cos(phi21);
    T3 = T1 * sin(phi21);
    realOut = T0 * realVal1 + T2 * realVal2 - T3 * imagVal2;
    imagOut = T0 * imagVal1 + T2 * imagVal2 + T3 * realVal2;
    param_gain = (realOut*realOut) + (imagOut*imagOut);
    switch (type)
    {
        case SHOTNOISE:
            *noise = 2.0 * CHARGE * FABS(param_gain);
           *lnNoise = log( MAX(*noise,N_MINLOG) );
            break;
        case THERMNOISE:
            *noise = 4.0 * CONSTboltz * ckt->CKTtemp * param_gain;
            *lnNoise = log( MAX(*noise,N_MINLOG) );
            break;
    }
}
```