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Hybrid Silicon Photonics for Optical Interconnects

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(Invited Paper)

***Abstract*—In this paper, we review the hybrid silicon photonic integration platform and its use for optical links. In this platform, a III/V layer is bonded to a fully processed silicon-on-insulator wafer. By changing the bandgap of the III/V quantum wells (QW), low-threshold-current lasers, high-speed modulators, and photodetectors can be fabricated operating at wavelengths of 1.55 μm. With a QW intermixing technology, these components can be integrated with each other and a complete high-speed optical interconnect can be realized on-chip. The hybrid silicon bonding and process technology are fully compatible with CMOS-processed wafers because high-temperature steps and contamination are avoided. Full wafer bonding is possible, allowing for low-cost and large-volume device fabrication.**

***Index Terms*—Integrated optoelectronics, optoelectronic devices, semiconductor lasers, silicon-on-insulator (SOI) technology.**

I. Introduction

ENERGY efficiency is currently high on the agenda in the field of photonics for communications and interconnects. Data centers alone are estimated to consume about 2% of the overall electricity worldwide, with about 15%–30% of this power spent on interconnects [1]. Therefore, a more energy efficient solution for interconnects can have a large impact in the global energy consumption.

The ever-increasing demand for bandwidth in telecommunications has caused the replacement of electronic data transmission by optical data transmission in networks and links exceeding the 10-m length over the past 30 years [2]. The main reason is that the consumed power in an electronic link scales with the bandwidth and length. In an optical link, this dependence of the power consumption is far less due to high-bandwidth and low-loss optical (single-mode) fibers. However, there is an offset in power consumption due to the electronic–optical conversion in the transmitter and the optical–electronic conversion in the receiver, and hence, until recently, the use of optical links was only favorable for lengths down to about 10 m.

With the advance of photonic integration technology and the replacement of whole arrays of discrete optical components with photonic integrated circuits (PICs), the energy efficiency of optical links has severely improved. These PICs are able to target higher bandwidths due to techniques like wavelength-division multiplexing (WDM) on-chip and have lower overall loss due to the elimination of coupling losses. An example of a single chip that is able to transmit and receive data at 1.6 Tb/s is shown in [3]. Moreover, the technology of photonic integration leads to reduced costs, and hence, optical links are currently being used in the shorter lengths and active optical cables based on PICs are commercially available [4].

The question then arises whether and when photonics will penetrate into the even shorter links, i.e., card-to-card, chip-to-chip, and even on-chip interconnects and replace the electronic links. Generally, there are three main considerations. First of all the energy consumption of such an optical link should be lower than an electronic link. For on-chip interconnects, there is even an upper limit on energy consumption. The International Technology Roadmap for Semiconductors estimates an upper boundary of 200 W for the amount of heat that can be removed from a chip in a cost-effective way [5].

A second consideration is the required interconnect density and the available (cross-sectional) area for it. Next generation system architectures require around 80 Tb/s [6] up to 780 Tb/s per chip expected in 2022 [1]. With data rates of 10–20 Gb/s per channel, this means that the required number of channels is in the order of thousands to tens of thousands. Fiber optic configurations will quickly become too complicated with this channel count and more integrated approaches are currently explored for intrasystem interconnects, such as optical printed circuit board technology based on polymer waveguides for board and backplane interconnects [7].

For interchip and on-chip interconnects, there is even less space available and more dense integration technologies should be considered. It can be calculated that electrical interconnects cannot handle a capacity of $\sim$100 Tb/s because they cannot reach the required level of integration density: a bus of interconnects simply does not fit in the circumference of a chip [1]. For photonic interconnects, this means that high-index contrast

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waveguides are required. Generally, both silicon [8] and indium phosphide (InP) [9] based integration platforms are able to obtain these levels of integration density. However, to accomodate an architecture for the required (tens) of thousands channels is a significant implementation challenge. Dense WDM seems the only feasible approach, and in [6], an approach is proposed with 250 waveguides transmitting 64 wavelengths, i.e., making a total of 16 000 channels that can run at 10 Gb/s. Such an architecture can be implemented in a single layer. As an intermediate approach, a combination of electronic and optical interconnects on a chip has been proposed, using the relatively long and high-bandwidth optical links to distribute data and/or clock signals over the chip surface to smaller areas of the chip, while maintaining the electronic interconnects within these smaller areas [10]. We further note that connections to sources and detectors can be small, in the order of 30–50 μm pitch and at 15–25 μm width. This can be realized by using a through via to a driver chip or another layer of metal, as is generally done for infrared display or detector bonding to CMOS circuitry, i.e., connecting over 1 million elements [11].

The third consideration is the material or technology that can be used. For the longer (telecommunication) fiber optical links, there are no restrictions in the material of choice for photonic integration. Typically, silica-based planar lightwave circuits (PLCs) are used for WDM (de)multiplexers [12] and InP-based devices are used as semiconductor optical amplifiers (SOAs), detectors, and sources [9], [13], [14]. Further integration can be achieved by, e.g., integration of multiplexers, sources, and detectors on a single InP chip [3]. However, for interchip and on-chip interconnects high-index contrast is necessary and integration of the photonic layer with the electronic chip is required.

Since a CMOS-chip is silicon based, photonic integration of optical functionalities on silicon is the most obvious option. Despite several attempts [15], [16], making an electrically pumped silicon-based laser with high enough efficiency is not possible yet. This is mainly due to the indirect bandgap of silicon. As a result, a combination of silicon photonics with a group III/V material-based source is currently the most viable option. Generally, there are two approaches possible. The first and most straightforward approach is to use an off-chip laser source [17]. This chip can be a (single or array) vertical-cavity surface-emitting laser-type laser flip-chip bonded to the silicon chip [18]. Another option for an off-chip source is to use a single multimode or mode-locked laser (MLL) that is able to generate a full WDM-mode comb at once [19], [20].

The second approach to combine silicon with III/V materials is to heterogeneously integrate the III/V source directly on the silicon chip using either molecular wafer bonding or divinylsiloxane–benzocyclobutene (DVS–BCB) adhesive wafer bonding [21]. Devices can then be fabricated on the chip and no alignment afterward is required. The full photonic layer, including passive components like filters, splitters, etc., can actually be realized in III/V material bonded on a silicon wafer using a membrane approach [22].

In this paper, we will review the hybrid silicon platform and its impact on the performance of interconnects. In this platform, III/V wafers or dies are bonded to a fully processed silicon-on-insulator (SOI) wafer using molecular bonding. The fabrication technology and general device structure are discussed in Section II. By changing the bandgap of the bonded III/V material, different functionalities can be realized. Continuous wave (CW), single-frequency sources and multimode, and mode-locked sources are discussed in Section III. High-speed modulators and receivers are discussed in Sections IV and V, respectively. In Section VI, a quantum well (QW) intermixing technology is reviewed that allows for integration of different bandgap devices on a single chip and in a single device. This paper concludes in Section VII.

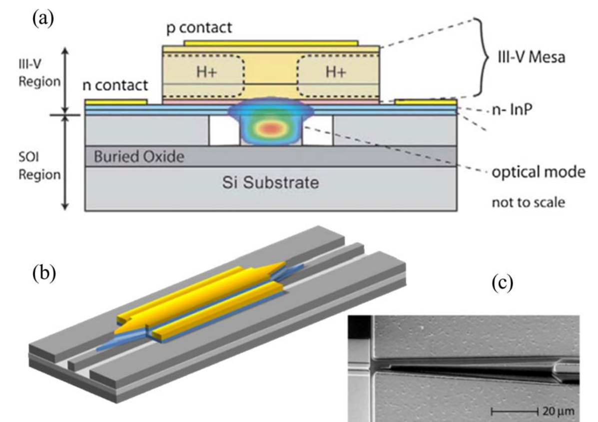


Fig. 1. (a) Cross section of the hybrid Si evanescent device. (b) Schematic of the transition taper of a passive silicon waveguide to an active hybrid section and *vice versa*. (c) SEM picture of a taper [26].

II. Hybrid Silicon Platform

A. General Device Structure and Mode Characteristics

The cross section of the hybrid silicon evanescent waveguide device is shown in Fig. 1 [23]. It consists of a III-V AlGaInAs-based multiple QW epitaxial layer structure bonded to a SOI rib or ridge waveguide. The device fabrication process can be divided into three major parts. First, the silicon waveguides and any other desired (passive) devices, such as arrayed waveguide gratings, couplers, and splitters, are fabricated in a CMOS fabrication process. Next, the III–V epitaxial layer structure is transferred to the silicon waveguides through an O_2 plasma-assisted, low-temperature bonding process. Finally, postprocessing of the III–V layers is done after bonding, to control the flow of current through the structure to ensure efficient optical gain to the waveguide mode. By tuning the bandgap of the III/V QWs lasers, electroabsorption modulators (EAMs) and phase modulators can be made.

AlGaInAs-based QWs are advantageous for uncooled laser operation at elevated temperatures [24]. However, high-quality AlGaInAs QWs are more difficult to obtain and relatively high-nonradiative surface recombination can increase lasing threshold currents. An alternative approach is to use InGaAsP-based QWs. Lasers with good performance have been reported in [25] using this approach. Threshold current density and threshold voltage in this work are 30%–40% lower than in [23].

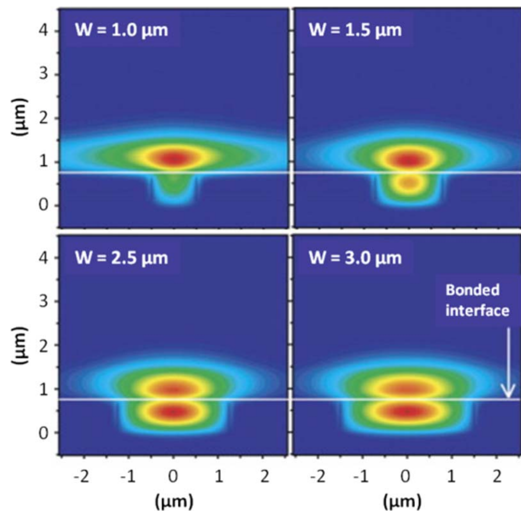


Fig. 2. Calculated optical mode for waveguide widths of 1.0 μm up to 3.0 μm using the Rsoft Beamprop simulation software.

The optical-mode characteristics are determined by the silicon rib waveguide dimensions. Fig. 2 shows the calculated optical mode with a fixed waveguide height for various waveguide widths. It can be seen that as the waveguide becomes wider, the mode is pulled more into the silicon region, with the same trend being seen for variation of the waveguide height. This feature can be used to tailor each device's overlap with the QWs and as a result, e.g., its optical gain characteristics. For example, lasers could be designed with narrower waveguides, which increase high modal gains to achieve lower thresholds, while amplifiers in an adjacent section of the wafer could be designed to have wide waveguide widths to increase the saturation power of the amplifier.

Transitions between a hybrid waveguide and a passive silicon circuit, e.g., waveguides, are achieved by tapering the III/V layer, as shown in Fig. 1(b) and (c). These tapers are fabricated by a self-aligned process using the contact metal as hard mask, hereby ensuring good contact over the entire taper length. These tapers typically have a transition loss of 0.6 to 1.2 dB. This loss is mainly due to the finite-tip width of around 0.5 μm, as limited by the resolution of an I-line stepper, and the sidewall roughness induced scattering [26]. The effects of nonuniform current injection in the taper have not been quantified separately.

In summary, the hybrid silicon technology can integrate active components, such as sources, modulators, and detectors, on an SOI photonic chip. The silicon processing is fully completed before the III/V wafer bonding takes place and all backend processing can take place outside of the CMOS foundry, thereby avoiding contamination. The maximum temperature during the backend III/V process is 350 °C, which is not detrimental for the silicon chip. As a result, we can conclude that this approach is fully compatible with the CMOS processes currently used. Full 150-mm InP wafer bonding has also been shown [27]. This means that with this process densely integrated CMOS-compatible photonic layers or PICs can be made in large volume and at low cost. If only a small part of the PIC contains active elements or when actives are grouped together, e.g., a detector or laser array, a die-bonding approach might be more cost-effective [28].

B. Hybrid Silicon Platform for Interconnects

For on-chip interconnects, a full network including passive components like filters, (de)multiplexers, splitters, combiners, and of course waveguides has to be integrated. In silicon, low-loss waveguides can be made, with losses down to 0.2 dB/cm [29] and a variety of filter elements is available [8], [30]. In this paper, we do not discuss these components in detail. We limit ourselves with the estimation that this network will add to a loss of about 10 dB per link, from transmitter to receiver [6]. If the silicon waveguide loss is too high for an application, e.g., for long delay lines, silica-based waveguides [12] can be integrated with a silicon chip to further reduce waveguide losses [31].

This paper focuses on the transmitter and receiver side of an optical link. Miller [1] presents the design criteria for future optical links to be competitive with or advantageous over electronic links. For off-chip interconnects, the system energy per bit should be less than 1 pJ (or less than 1 mW per Gb/s) to be competitive and about 100 fJ to be advantageous. Since this is the total energy including electronics, this means that optical output device energies should be in the order of tens of femtojoules per bit maximum. For on-chip interconnects, this system energy is 50–200 fJ/bit to be competitive. However, to accommodate the required data capacity, while having a maximum processor power usage of 200 W, this requirement actually decreases to 10–30 fJ/bit.

So concluding, it can be stated that for short-reach interconnects, these numbers have to be met by optical links to be more energy efficient than electronic links. When these numbers can be met, optical links will replace electronic links also on the shorter lengths scales around 1 m and below, just like they have replaced electronic links at the longer length scales over 10 m. We note that even at the very small distances across a chip surface, electronics links can consume significant power, e.g., about 2 pJ per bit for a 2-cm line [1]. In the following, we will present an overview of the transmitters (sources and modulators) and receivers that have been realized in the hybrid silicon platform.

III. Sources

A. Single-Frequency Sources

Although Fabry–Pérot (FP) type lasers having cleaved and/or polished facets are the most commonly used laser diode, they cannot be integrated on a chip with other components. As a result, these lasers are not useful for on-chip interconnects. In the following, we review sources that can be connected to and integrated with other components on the same chip.

1) Hybrid Silicon DFB Lasers: The DFB laser consist of a 360-μm-long quarter wavelength shifted hybrid silicon grating with a grating κ of $\sim$247 cm^{-1}, and reflectivity peak at $\sim$1600 nm. Fig. 3(a) shows the device layout. The laser has a 200-μm long gain region, with a cross section, as shown in Fig. 1. Tapers from the gain region to the passive silicon waveguide are

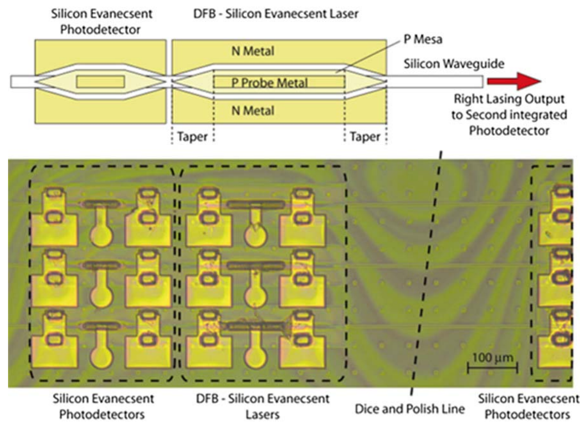


Fig. 3. (Top) Hybrid silicon DFB device layout. (Bottom) Microscope image of the DFB laser with integrated photodetectors.

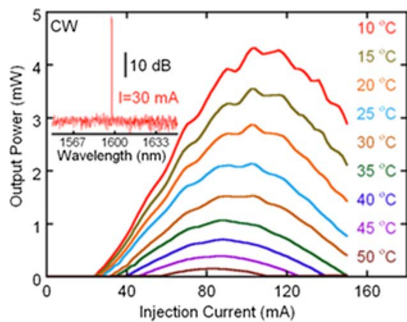


Fig. 4. LI curve for stage temperatures of 10 to 50 °C. (Inset) The lasing spectrum at 30 mA injection current, showing a single-mode operation span over a 100-nm wavelength range.

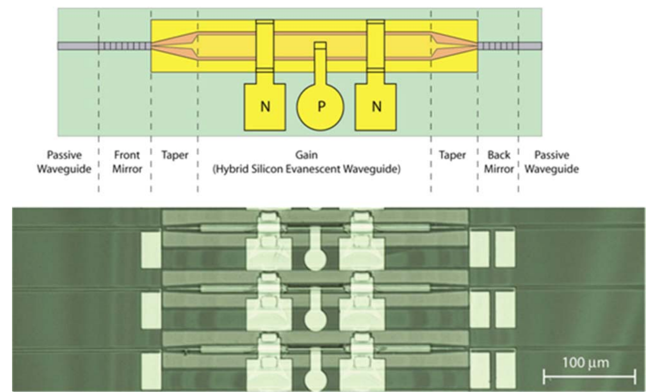


Fig. 5. (Top) DBR laser top-view schematic and microscope image.

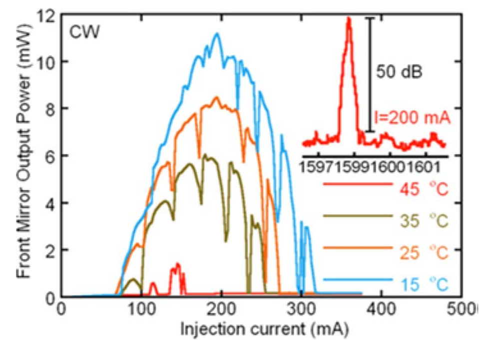


Fig. 6. DBR laser LI curve for various temperatures measured at the front mirror. (Inset) The lasing spectrum at 200-mA injection current, showing a single-mode operation with 50-dB side-mode suppression ratio (SMSR).

80 μm long. They are formed by linearly narrowing the III–V mesa region above the silicon waveguide (see Fig. 1). This adiabatically transforms the mode from the hybrid waveguide to the passive silicon waveguide allowing for losses on the order of 1.2 dB per taper and reflections on the order of 6×10^{-4}. Hybrid silicon photodetectors are placed on both sides of the laser in order to enable on-chip testing of the DFB laser performance. The photodetectors are 240 μm long including the two 80-μm-long tapers. The detector to the right is placed 400 μm away in order to allow room for dicing and polishing for off-chip spectral tests. More details can be found in [32].

The light–current (*LI*) characteristics of the DFB laser are measured on chip by collecting light out of both sides of the laser with the integrated photodetectors. To determine the laser power output, 100% internal quantum efficiency of the photodetectors is assumed in order to conservatively assess the laser performance. It can be seen from Fig. 4 that at 10 °C, the lasing threshold is 25 mA, with a maximum output power of 4.3 mW. This corresponds to a threshold current density of 1.4 kA/cm^2. The maximum lasing temperature is 50 °C. The laser has a 13-Ω device series resistance. This value scales appropriately with the 4.5-Ω resistance measured on 800-μm-long FP lasers with similar III–V mesa dimensions [23].

The lasing spectrum is taken by dicing off the right photodetector, polishing, and antireflection coating the silicon waveguide output facet. Light is collected with a lensed fiber into a spectrum analyzer with a 0.08-nm resolution bandwidth. Fig. 4 (inset) shows the optical spectrum at 30 mA injection current. The laser has a lasing peak of 1599.3 nm and a side-mode suppression ratio of 50 dB. It can be seen that the laser operates single mode over a 100-nm span. The laser linewidth is measured by using the delayed self-heterodyne method [33]. A minimum linewidth is measured at a laser output power of 1.8 mW with a convoluted Lorentzian linewidth of 7.16 MHz corresponding to a 3.6-MHz linewidth, a typical value for commercial DFB lasers.

2) Distributed Bragg Reflector Lasers: The distributed Bragg reflector (DBR) laser consists of two passive Bragg reflector mirrors placed 600 μm apart to form an optical cavity, as shown schematically in Fig. 5. The gratings have an etch depth and duty cycle of 25 nm and 75%, respectively, leading to a grating strength, κ of 80 cm^{-1}. The back and front mirror lengths are 300 and 100 μm, resulting in power reflectivity of 97% and 44%, respectively. A 440-μm-long silicon evanescent gain region and two 80-μm-long tapers are placed inside the cavity. The tapers are electrically driven in parallel with the gain region in order to minimize absorption. More details can be found in [32].

The CW laser output power is measured with an integrating sphere at the front mirror of the laser. The front mirror output *LI* characteristic is shown in Fig. 6. The device has a lasing

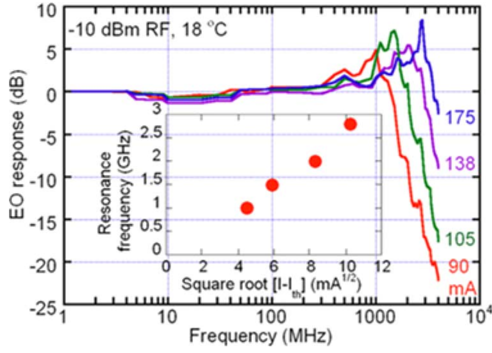


Fig. 7. Photodetected frequency response of the DFB laser for three different bias currents with a stage temperature of 18 °C and (inset) plot of resonance frequency versus the square root of current above threshold.

threshold of 65 mA and a maximum front mirror output power, of 11 mW, leading to a differential quantum efficiency of 15%. The taper transmission loss can have a significant impact on the threshold current, and therefore, it affects many important laser characteristics, such as wall plug efficiency and resonance frequency. If we use our estimations of the material and laser properties, calculations show that the taper loss of 1.2 dB increases the threshold current by a factor of 2 due to the accumulated loss through four taper transitions in one round trip through the cavity. We estimate that a reduction in the single-pass taper losses to 0.5 dB would reduce this factor to 1.2. The laser operates up to a stage temperature of 45 °C. The kinks in the *LI* are from mode hopping [32]. The device has a lasing turn-ON voltage of 2.6 V and a series resistance of 11.5 Ω. The lasing spectrum is shown in Fig. 6 with a lasing peak at 1597.5 nm when driven at 200 mA.

Fig. 7 shows the photodetected electrooptic response of the laser combined with all connected components under small signal modulation. A 2-pF device capacitance was extracted from the S11 measurement, resulting in an *RC*-limited bandwidth of 7 GHz. Fig. 7 (inset) shows the resonance frequency versus the square root of dc drive current above threshold, which has a roughly linear dependence as expected. Under higher modulation powers the resonance peak becomes significantly dampened. The 3-dB electrical bandwidth at 105 mA is ∼2.5 GHz. This laser has been successfully modulated at 2.5 and 4.0 Gb/s with extinction ratios (ERs) of 8.7 and 5.5 dB, respectively [32]. Improving the laser design to decrease the threshold current and increase the differential gain is expected to significantly improve the modulation bandwidth in future devices.

3) Electrically Pumped Compact Microring Lasers: Lasers with ring or disk resonator geometries are attractive on-chip light sources, since they require no gratings or facets for optical feedback. Practical use of such a device in an interconnect requires power efficient, CW operation, high-speed direct modulation, and operation at elevated temperature.

Fig. 8 shows the schematic of the hybrid silicon microring laser. The laser consists of a III–V ring resonator on top of a silicon disk with the same diameter. The fundamental whispergallery mode shifts toward the resonator edge as shown by a beam propagation method (BPM) simulated-mode profile in the inset of Fig. 8(a). This mode has confinement factors of 15.2% and 51.7% in the active region and silicon, respectively. A silicon bus waveguide connects the microring laser with two integrated photodetectors with a length of 180 μm. More details about the device design and fabrication can be found in [34]. We note that in our current approach, the etching of the silicon ring is done after the III/V etching, using a self-aligned process, and hence, strictly speaking not CMOS-compatible. However, with the decreasing overlay specifications of state-of-the-art lithography tools, we expect that in the future this can be changed.

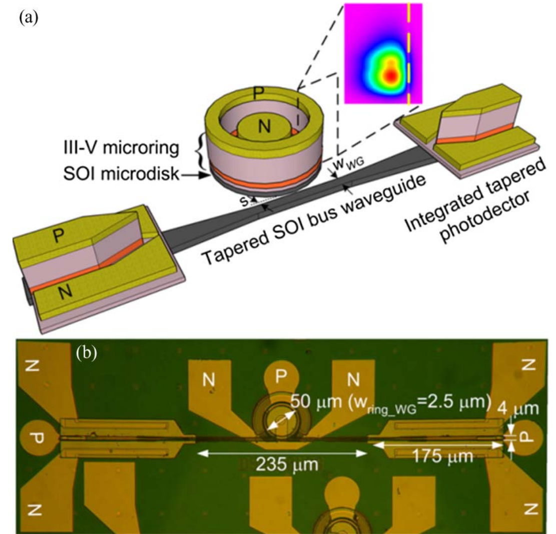


Fig. 8. (a) Schematic of compact hybrid silicon ring resonator laser with BPM-mode profile and integrated, tapered photodetectors. Variables of coupling gap s and bus waveguide width $w_{\rm WG}$ are labeled. (b) Microscopic image of a finished device with critical dimension labeled.

Fig. 9 shows the LI characteristics of devices with (a) 150 nm and (b) 250 nm coupling gaps, and a 0.6-μm bus waveguide width. For these coupling gaps, the minimum threshold currents are 8.37 and 5.97 mA at 10 °C, respectively. These correspond to current densities of 2.02 and 1.43 kA/cm^2, assuming uniform carrier distribution in the active region. Threshold voltages measured at room temperature (RT $= 20\,^\circ$C) are 1.39 V ($I_{\rm th} = 9.56$ mA) and 1.33 V ($I_{\rm th} = 7.61$ mA), which lead to laser turn-ON powers of 13.29 and 10.12 mW. The average series resistance of 24 devices is 31.4 Ω at RT. Devices with coupling gaps of 150 and 250 nm lase up to a stage temperatures of 40 °C and 65 °C, respectively.

As the coupling gap increases from 50 to 250 nm, outcoupling coefficient equivalent to mirror loss for straight devices decreases exponentially from 0.03 to 1.28×10^{-5} based on 2-D finite-difference time-domain (FDTD) simulation.

Fig. 10 shows the calculated 3-dB bandwidth for injection current 10, 20, and 30 mA as a function of device diameter (cavity length), using parameters and assumptions as mentioned in [34]. These estimates result in ∼5 mA threshold current for a 50-μm microring laser. No thermal effect is taken into account in this calculation. In order to achieve 3-dB bandwidth of 10 GHz, the 50-μm-diameter device needs to be driven with 20 mA bias current, i.e., $4 \times I_{\rm th}$. Devices with smaller dimension have smaller

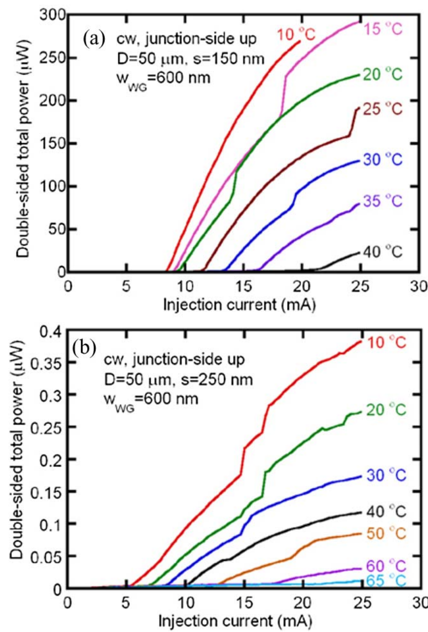


Fig. 9. LI characteristic of microring lasers with coupling gap of (a) $s = 150$ nm and (b) $s = 250$ nm at various stage temperatures. Output power is the sum of the response of both integrated photodiodes assuming 1 A/W responsivity.

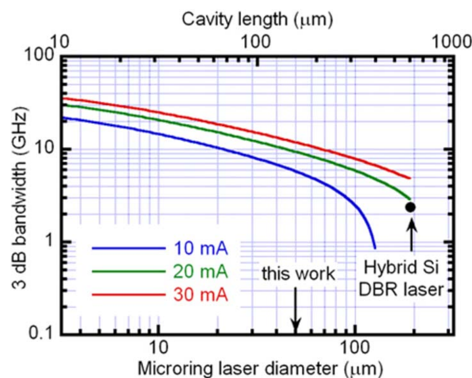


Fig. 10. Calculated 3-dB bandwidth as a function of microring laser diameter (cavity length) for 10, 20, and 30 mA injection current. Black dot represents experimental 3-dB bandwidth of 2.5 GHz measured on a hybrid Si DBR laser without about $1.6 \times I_{\rm th}$ bias current [35].

threshold and require less injection current to reach 10 GHz, 3 dB bandwidth. Clearly, employing short cavity devices (e.g., microring lasers) is an efficient approach to further increase the direct modulation bandwidth without sacrificing low-power dissipation. Increased thermal impedance poses a major obstacle for all compact devices.

For these lasers, there are several fundamental limits for decreasing the threshold. These include the volume of the active region volume, which is related to the device dimension, the internal cavity loss and modal gain, which are related to the confinement factor, and the injection efficiency and mirror loss, which are related to the power outcoupling of the rings. If these factors are kept constant, the active region volume will be the dominant factor that determines threshold.

Compared with InP disks BCB bonded on SOI [21], the major difference is vertical confinement of the light. In BCB-bonded disks, most of the light is confined in the III–V disk, and hence, their modal gain is higher than the hybrid silicon microring. Moreover, due to a different carrier injection scheme, these cavities can be made smaller and very low thresholds below 1 mA can be achieved. Limitations on BCB-bonded disks are the high-thermal impedance and limited output power.

4) Conclusion: The link power budget is to a large extent determined by the receiver sensitivity. This sensitivity (at bit error rate (BER) 10^{-9}) is typically -10 dBm for 40 Gb/s operation down to -20 and -25 dBm for PIN or APD receivers, respectively, at lower speeds of 2.5 Gb/s [36]. So assuming a 10-dB link loss [6], this means that for a single channel a power of between -15 to -10 dBm is needed. All the sources presented here are capable of generating this power level, though at relatively large injection currents of 8 mA up to 65 mA for a microring laser and DBR laser, respectively. Power consumption for these devices is 11 and 160 mW, respectively. This means that if we are able to directly modulate a microring laser at 10 Gb/s, as calculated earlier, power consumption will be around 1 pJ/bit. The threshold current, and hence, the power consumption of the DBR laser can be significantly lowered by using a shorter cavity and possibly high-index contrast gratings [37]. Moreover, the modulation speed can be increased with a shorter cavity. For the microring, the Q-factor of the cavity will have to be increased, but it seems feasible to go below the 1-mA threshold, as is also shown in [38]. Having modulation speeds of over 10 Gb/s will then bring the power consumption down to the 100 fJ/bit level.

B. MLL Sources

MLLs are able to generate short optical pulses. The optical spectrum of these pulses can be broadband and the modes have a fixed spacing, defined by the cavity length. This makes these lasers ideal sources for a multiwavelength mode comb that can be used for WDM applications [19], [20]. To implement such a network on-chip frequency-selective modulators and detectors are needed, as explained in [6]. One option is to use broadband modulators and detectors in combination with filter elements like arrayed-waveguide gratings (AWGs), but these components tend to have a large footprint. Another options is to use resonant elements, such as cascaded microrings [39].

Such a frequency-comb laser eliminates the need for multiple laser drivers and stabilizers and wavelength lockers, as are typically used in nowadays WDM systems, where multiple single-frequency lasers are employed, and hence, is far more energy efficient. Once the MLL is stabilized, which can be done by a low-power RF driver [40], only one wavelength locker is needed to stabilize all the channels on a WDM grid. The challenge with using these lasers diodes is to achieve a suitable optical bandwidth to provide the required number of WDM channels. In [41], an 18-nm bandwidth, 50-GHz MLL is reported, i.e., having 45 channels. A 10-nm, 10-GHz MLL is presented in [42]. It is interesting to note that both these broadband MLLs have been realized using quantum-dot gain material

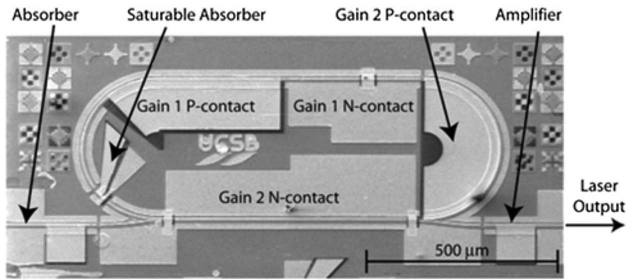


Fig. 11. Scanning electron micrograph of a racetrack mode-locked silicon evanescent laser.

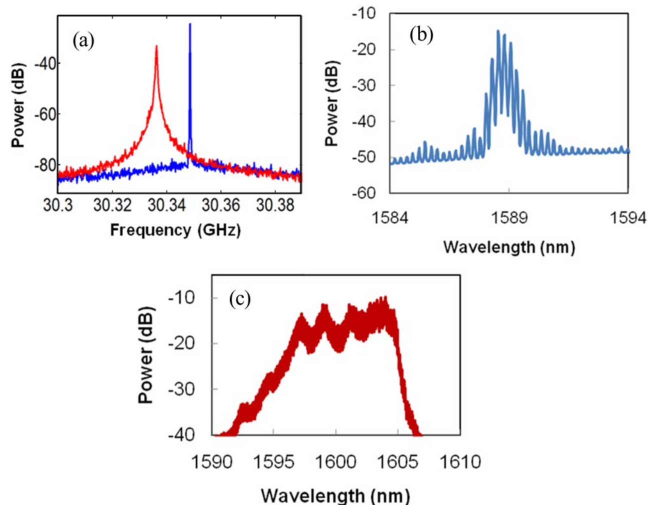


Fig. 12. (a) RF-frequency span of 100 MHz around the mode-locking frequency for passive and hybrid mode locking of the 30-GHz racetrack laser. (b) Logarithmic scale optical spectrum of the 30-GHz racetrack laser. (c) Logarithmic scale optical spectrum of the 10-GHz FP laser.

and the large bandwidth is ascribed to the large inhomogeneous broadening.

MLLs have been realized in the hybrid silicon platform both in FP-type configurations at 10 and 40 GHz [43] and in a racetrack configuration at 30 GHz [44]. They have been operated both under passive-mode locking and hybrid-mode locking, i.e., applying an RF signal to the saturable absorber. The racetrack MLL is shown in Fig. 11. The 40-GHz FP-type laser and 30-GHz racetrack laser show a stable operation under passive-mode locking, with RF linewidths in the order of 2–3 MHz at -20 dB, as shown in Fig. 12(a). Hybrid-mode locking narrows down the RF linewidth, indicating a more stable operation due to the synchronization with the electrical clock. The timing jitter (1 kHz–100 MHz integration range) is 0.36 ps at 14 dBm of RF power. We note that this value for the input RF power can be severely decreased in future designs by matching the electrical impedance of the saturable absorber [40]. Typical pulse durations for these lasers are in the order of 6–10 ps.

For WDM application, it is important that the output of the MLL has a large optical bandwidth, i.e., the width of the mode comb. For the 30-GHz racetrack and the 40-GHz FP lasers, this 3-dB bandwidth is, however, limited to below 1 nm [see Fig. 12(b)]. This is not sufficient, since this means that only 2–3 modes can be used in the WDM system without having the need for excessive equalization. Much more promising is the operation of a 10-GHz FP laser, which shows a 9-nm optical bandwidth at a relatively large injection current Fig. 12(c). The combination of increased self-phase modulation in the longer gain cavity and the larger number of modes that can lase with the higher injection current are assumed to be responsible for the broad optical spectrum. This spectrum can, in principle, support 100 modes spaced at 10 GHz for WDM applications. We note that the spectrum is relatively flat, which is favorable for WDM applications. Such lasers can be operated at 10 mW output power and around 250 mW electrical power consumption [23], [32]. If over 100 modes are available, which can be modulated at 10 Gb/s, e.g., by an EAM, this means that the energy consumption per bit is in the order of 0.1–0.3 pJ/bit.

Measurements of the optical linewidths show that these are broad, at around 225 MHz. However, injection with a narrow linewidth CW laser can decrease the linewidth for all the modes. Preliminary experiments have shown that the optical linewidth could be decreased down to 100 kHz, i.e., the linewidth of the injected CW mode.

So concluding, it can be stated that the hybrid silicon MLLs have promising characteristics for use as a mode-comb source. Optical injection with a single-mode laser and electrical RF injection in the saturable absorber have been shown to stabilize the laser fully, i.e., the mode position and the mode spacing. This effectively limits the number of controls for the complete mode comb to two elements.

For future on-chip interconnect networks [6], it is estimated that when an off-chip laser source is used for the on-chip network, an optical power of 0.8 W will be necessary. Such high-power lasers can be achieved by using low confinement and large mode area waveguide structures [45]. As shown in Fig. 2, the mode characteristics and the confinement can be adjusted by changing the waveguide width and high-saturation power lasers can be made. Furthermore, the hybrid silicon technology has a clear advantage over the conventional InP-based MLLs. Two-photon absorption is around two orders of magnitude lower in silicon waveguides as compared to InP [46]. This allows for higher power densities, and consequently, higher pulse peak powers in the silicon waveguide.

As a last point, it has to be mentioned that wall-plug efficiency of diode lasers is higher than other options, e.g., fiber lasers. As such these hybrid silicon MLLs are a very promising candidate for this application, where high-power operation is required.

IV. Modulators

Modulators are necessary when a MLL is used as a multiwavelength comb source or when the direct modulation frequency of single-frequency lasers is not high enough for the system requirements. In this section, we present two types of modulator, namely an EAM and a Mach–Zehnder-type modulator (MZM).

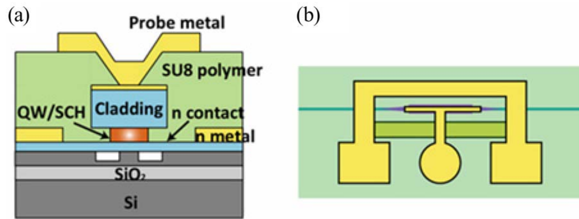


Fig. 13. (a) Cross section of both EAM and MZM at the hybrid section. (b) Schematic top view of an EAM.

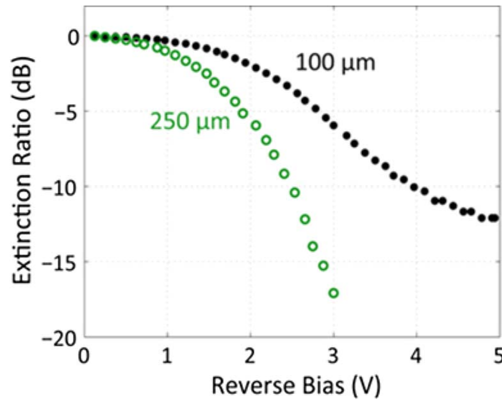


Fig. 14. ER at 1550 nm for 100- and 250-μm-long EAMs.

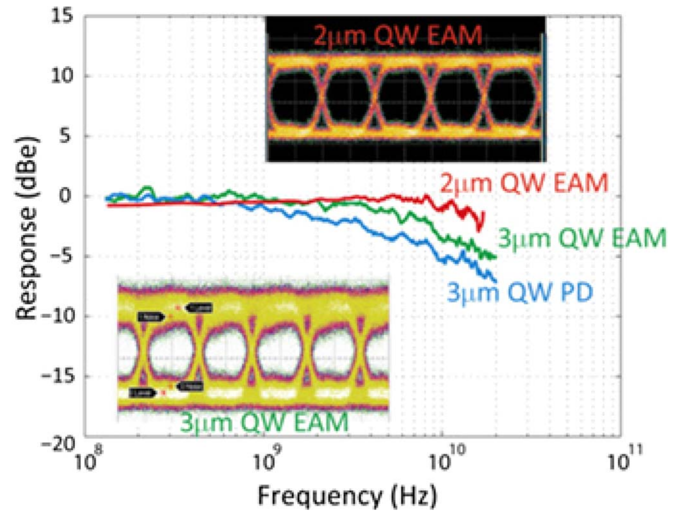


Fig. 15. Response curves of two 100-μm-long EAMs with different QW section widths of 2 and 3 μm, The response of a photodetector (PD) is also given. Inset shows the eye diagrams.

A. EAM

A cross section of the EAM modulator is illustrated in Fig. 13(a). Two 60-μm hybrid tapers, laterally tapered in both silicon and III–V layers, are used to minimize reflection and mode mismatch loss through adiabatically transforming the optical mode. The InP cladding mesa is 4 μm wide, while the QW and separated confinement heterostructure (SCH) layers are undercut to reduce the total device capacitance [47]. In general, the EAM has a very small footprint around 100 μm, such that the device can be easily operated above 10 GHz with careful design of the active region to control the overall *RC* cutoff frequency. Fig. 13(b) shows the top view of a single EAM with simple dc probe pads for both p- and n-contact. Further details can be found in [48].

Fig. 14 shows the relative ER at wavelength of 1550 nm under various reverse biases. More than 10 dB ER can be achieved with less than 4 V bias for a 100-μm-long device. For a longer device with 250 μm absorber, it only takes 2.5 V to achieve 10 dB ER. The propagation loss of the hybrid waveguide is around 3.6 dB/mm by measuring devices loss with different absorber lengths. A pair of cascade EAMs reversely biased at 5 V were used to measure the on-chip loss of the fabricated 100-μm EAM. The on-chip loss is around 3 dB mainly due to the excess loss from both tapers.

To investigate the high-speed performance of the EAM, the frequency response was measured. As shown in Fig. 15, two 100-μm-long EAMs with different QW undercuts were measured. The device with 3-μm-wide QW section has a series resistance around 30 Ω and capacitance of 0.2 pF at 2 V bias, which corresponds to a cutoff frequency around 10 GHz. The modulators are also driven with a $2^{31} - 1$ pseudorandom bit sequence (PRBS) to explore the performance of large signal modulation. Peak to peak driving voltage of 0.82 V is used to produce the clear eye diagram with 5 dB ER. We can further improve the speed with a more aggressive QW undercut. The device with 2-μm-wide QW section dropped the capacitance to around 0.1 pF and produces a 3-dB bandwidth over 16 GHz. The downside is the reduction of the QW volume, which leads to increase of driving voltage due to a decrease of the overlap of the optical mode with the QWs. The open eye diagram with 6 dB ER is taken with much higher voltage swing of 3.2 V peak-to-peak.

We note that the voltage swing of this EAM can be below 1 V at 5 dB ER, which is essential for compatibility with CMOS technology. The energy consumption of such EAMs is estimated to be around 20 fJ/bit.

B. MZM

MZMs are commonly designed using a coplanar waveguide (CPW) electrode design. However, for a CPW incorporating a PIN diode, the electrical field penetrates into the diode and propagation losses of the electrical signal tend to be large. In order to reduce the propagation loss, it is important to ensure that the propagating electrical fields have minimal overlap with the doped semiconductor. In this design, a capacitively loaded (CL) travelling wave electrode (TWE) is implemented. As illustrated in Fig. 16(a), the small pads extending from the transmission line can provide the necessary electrical signal to drive the device, while the TWE is kept away from the semiconductor. Furthermore, the phase velocity of the electrical signal can be adjusted by changing the distributed capacitance of the transmission line. This can help to reduce velocity mismatch between the electrical and optical signal. The cross section of the loaded region is depicted in Fig. 16(b). More details about the fabrication can be found in [49].

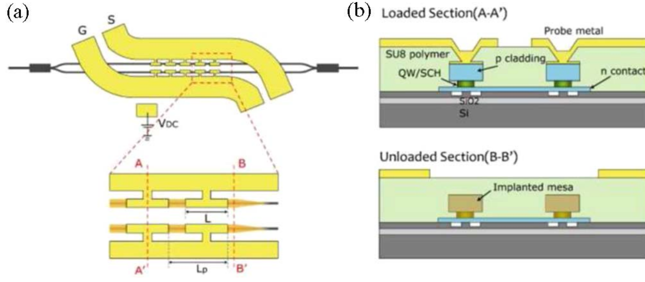


Fig. 16. (a) Top view of a device with a CL slotline electrode. (b) Cross section of loaded (along A–A') and unloaded sections (along B–B') of the hybrid waveguide.

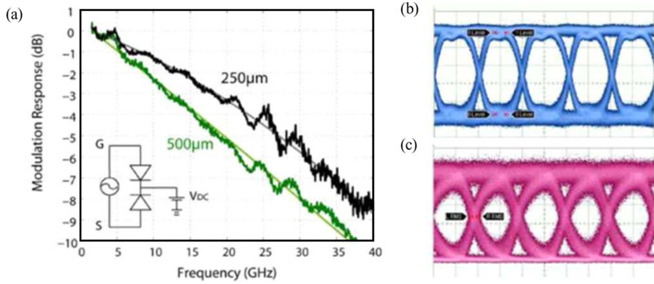


Fig. 17. (a) Experimental frequency responses for the MZMs. (b) Driven electrical signal out from the BERT tester at 25 Gb/s. (c) Modulated signal after the modulator for a 500-μm MZM.

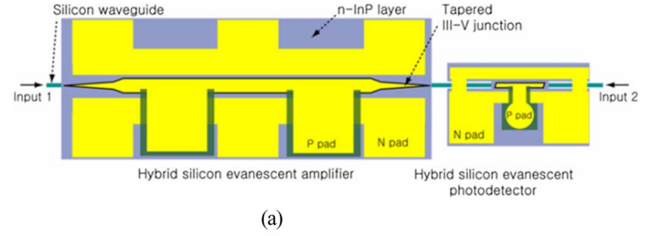
The frequency response of the MZM is shown in Fig. 17(a). The 3-dB cutoff frequencies of a 250- and 500-μm device are about 18 and 12.5 GHz, respectively. The large signal modulation was also characterized. As can be seen in Fig. 17(c), the modulated eye at 25 Gb/s is clearly open with 11 dB ER, which to the best of our knowledge is the best ER above 10 Gb/s for any silicon-based modulator. The energy consumption of this MZM is estimated to be 1.8 pJ/bit.

So concluding, it can be stated that hybrid silicon modulators operating at these high frequencies of 25 Gb/s and higher offer a clear advantage over all-silicon modulators, where modulation bandwidth is typically limited [8]. In terms of energy efficiency, these hybrid silicon modulators will be important for high-speed links, since absolute power consumption of the interconnect is relatively independent of modulation speed, whereas the efficiency (energy per bit) increases with speed [1].

V. Receivers

Combining hybrid silicon amplifiers and photodetectors on a single platform can lead to more practical, better-performing optoelectronic photoreceivers. Hybrid silicon photodetectors are interesting, since their absorption edge can easily be extended beyond the 1600-nm regime by engineering III–V QWs.

In Fig. 18, a hybrid silicon preamplified receiver is shown. It is comprised of an optical amplifier and a waveguide photodetector. The transition between the passive silicon waveguide and the hybrid waveguide of the amplifier is formed by tapers, as presented in Section II, Fig. 1. The same III–V epitaxial structure is used for the amplifier and the detector. The total length of the amplifier and the detector is 1240 and 100 μm, respectively.



(a)

(b)

Fig. 18. (a) Top view of a hybrid silicon evanescent preamplified receiver. (b) SEM picture of eight integrated devices with amplifiers.

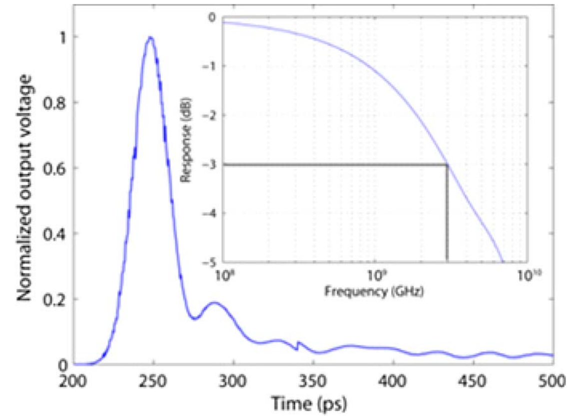


Fig. 19. Impulse response (0.6-ps input pulse) of the detector. The inset shows the Fourier transform of the impulse response.

Fig. 18(b) shows an array of these receivers. Further device details can be found in [26].

For a 1.2-mm-long structure, the maximum gain is 9.5 dB at 300 mA. The quantum efficiency of the 100-μm detector is 50%. By putting the two together, the responsivity of the receiver increases to 5.7 A/W with preamplification. The device shows 0.5 dB saturation at a photocurrent of 25 mA.

The device bandwidth is measured as 3 GHz by time-domain impulse response (see Fig. 19; inset shows bandwidth). The resistance–capacitance-limited bandwidth is estimated to be 7.5 GHz though. This indicates that the device speed is primarily constrained by the current III–V layer design. A higher bandwidth can be achieved by using QWs with a smaller valence band offset and a thinner SCH layer to reduce the hole transit time. BER measurements for a nonreturn to zero 2.5 Gb/s PRBS shows a receiver sensitivity of -17.5 dBm [26].

Recently, an improved bandwidth using an InGaAs/InP-based hybrid silicon photodetector [50] was reported. The bandwidth was measured to be 6 GHz, and open eye diagrams were

obtained up to 12.5 GHz. Higher speeds are achievable by careful design of the photodiode. For example, wafer-bonded InP/InGaAs-based photodetectors having a bandwidth of 20–25 GHz were reported in [51] and [52], showing the potential for the hybrid silicon approach.

VI. Full-Integration Platform

The devices presented here, i.e., sources, modulators, and receivers, have different bandgaps of the III/V QWs for operation around wavelengths of 1.55 μm. A full transmitter, however, will probably consist of a combination of a single-frequency source and a modulator, either MZM or EAM. Also, on-chip interconnects will require a combination of sources, modulators, and detectors integrated on the same chip.

There are different ways how different bandgap QWs can be integrated on the same chip. One option is by regrowth techniques, where part of the QWs are etched away and areas with a different or no QW are regrown [53]. This option is probably not suitable for wafer bonding techniques as required by the hybrid silicon platform due to nonflat surface topology at the butt–joint interfaces. Another option is to bond separate dies with different bandgaps on a single SOI wafer [38]. This option constrains the design flexibility, however, since components requiring the same bandgap have to be placed together.

In this section, an approach based on QW intermixing (QWI) is presented. This technology can, for example, be used to integrate a source with a modulator. A sampled-grating (SG) DBR laser integrated with an InGaAsP/InP EAM is shown. Details of this work can be found in [54].

A. QWI

The QWI process in this paper is based on implant enhanced intermixing in combination with selective removal of an InP buffer [55]. Details of the QWI process and the as-grown hybrid laser III–V base structure are shown in Fig. 20(a)–(e). By selectively masking and implanting the QWs, three different bandgaps are created in the wafer.

Fig. 21 shows photoluminescence (PL) spectra from the three bandgaps in the SG–DBR–EAM. Good uniformity of the PL full-width at half-maximum can be seen for all three bandgaps, indicating consistent material quality for the modulator, gain, and mirror regions [56]. The EAM has a 50-nm blue-shifted bandgap and the low-loss mirrors of the SG-DBR have an 80-nm blue-shifted bandgap. It has to be noted that the QWI takes place before wafer bonding, and hence, it is fully compatible with standard CMOS processing.

B. SG–DBR–EAM Laser

A cross section of the completed SG–DBR–EAM is shown in Fig. 22. The grating was etched into the III/V wafer before bonding. The laser portion of the integrated SG–DBR–EAM consists of five electrically isolated sections. A taper is used to transition the optical mode from the hybrid waveguide with both III–V and Si to a purely silicon waveguide, as shown in Fig. 1. The design of the integrated SG–DBR–EAM uses a 650-μm backside absorber, 760-μm-long rear mirror, 80-μm-long phase section, 550-μm-long gain region, a 780-μm-long front mirror, a 200-μm-long EAM, and a 100-μm-long taper.

The laser uses a 20-μm-wide III–V mesa in the gain, mirror, phase, and backside absorber regions and a 4-μm-wide mesa in the modulator. The measured loss and κ of the III–V gratings

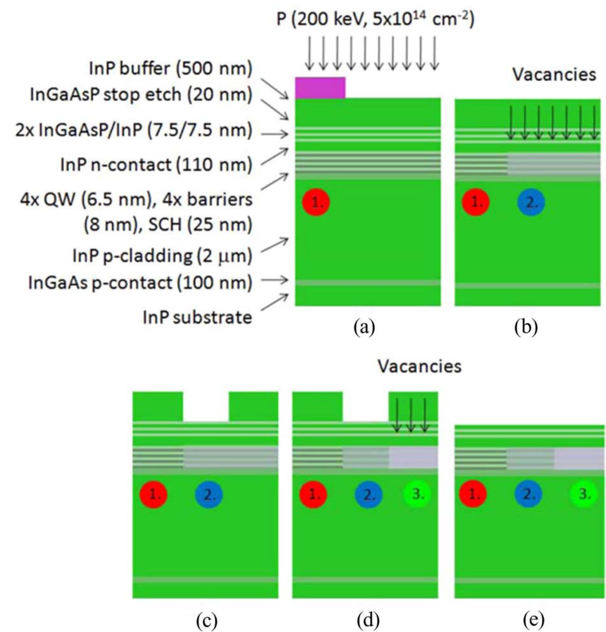


Fig. 20. Overview of the QWI process used for the hybrid laser. The three bandgaps realized are numbered 1, 2, and 3. (a). Implantation of P into InP buffer with SiNx mask to preserve the as-grown bandgap. (b) Diffusion of vacancies through QWs and barriers via rapid thermal annealing (RTA) for bandgap 2. (c) Removal of InP buffer layer to halt intermixing. (d) Diffusion of vacancies via RTA for bandgap 3. (e) Removal of InP buffer layer and InGaAsP stop etch layer.

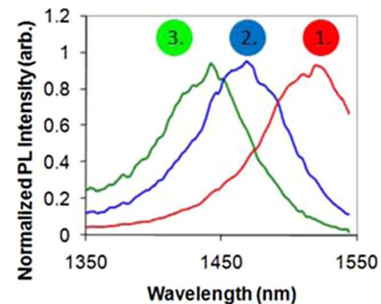


Fig. 21. Normalized PL spectra from the three bandgaps utilized in the SG–DBR–EAM devices.

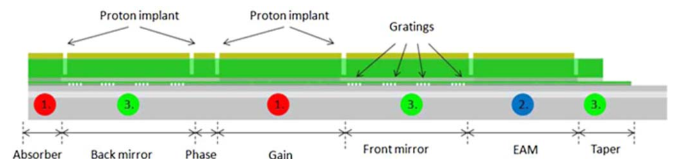


Fig. 22. Cut away of a hybrid silicon SG–DBR–EAM shown with four front mirror and back mirror grating bursts. Proton implantation is used for electrical isolation between various laser sections. The active, modulator, and passive bandgaps are labeled 1, 2, and 3, respectively.

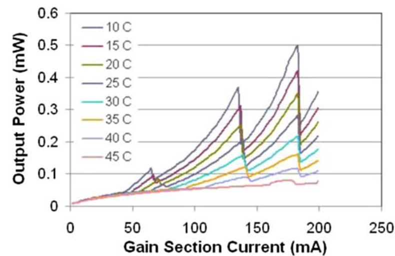


Fig. 23. Output power gain current measurement results for SG-DBR at stage temperatures from 10 to 45 °C.

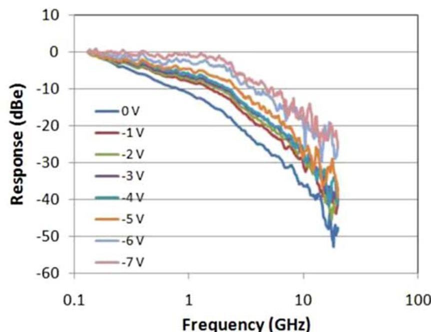


Fig. 24. Electrical to optical small signal response of integrated EAMs in the SG–DBR–EAM with a 2.5-μm-wide silicon waveguide.

was 165 cm^{-1} and 3 dB/100 μm, respectively, for a 2-μm-wide Si waveguide and 100 nm etch depth (into the III–V).

The integrated SG–DBR–EAM CW LI characteristics are shown in Fig. 23. For a device with a 2.5-μm-wide Si waveguide, CW operation is achieved up to 45 °C with output power up to 0.5 mW at 10 °C and 170 mA of gain current. Dips in the LI characteristics are due to temperature induced cavity-mode hops. With this laser tuning over four supermodes can be achieved at wavelengths of 1524, 1518, 1512, and 1554 nm with side-mode suppression >35 dB [54].

The integrated EAMs show extinction >5 dB at -6 V reverse bias depending on the wavelength of operation. Shorter wavelengths show more efficient operation than longer wavelengths due to the proximity between the modulator band edge and the operating wavelength. The bandwidth of the integrated modulators depends largely on the applied dc reverse bias achieving greater than 2 GHz with a 6 V bias, as can be seen in Fig. 24. The series resistance of the modulator is 40 Ω. The large variation in frequency response is due to carrier diffusion effects as photocurrent is generated outside the 4 μm ridge and diffuses toward the center of the structure. It is possible to improve both the bandwidth and extinction performance of the modulator by increasing the number of QW in the base structure and using an undercut III–V QW design as in [48].

VII. Conclusion

The information and communication technology industry is currently responsible for 1.3% of the global CO_2 emission, a number, that is, expected to double by 2020 [57]. Since a large amount of this power consumption is in interconnects. It is clear

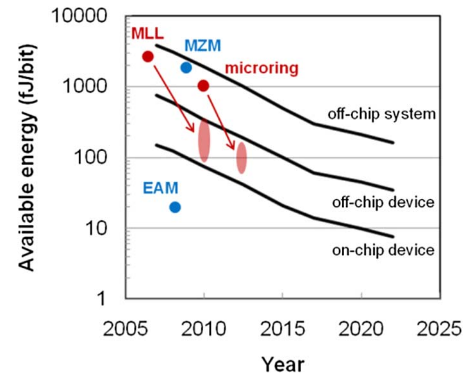


Fig. 25. Estimated roadmap for the available energy for off-chip interconnects (top line) and for off-chip and on-chip optical output devices (middle and bottom lines), as presented by Miller [1]. The hybrid silicon sources presented in this work (red), their expected performance increase (red arrows), and the hybrid silicon modulators (blue) are mapped on this roadmap.

that more energy efficient interconnect technologies can have a large impact on the global energy consumption.

In this paper, we have discussed a novel technology, the hybrid silicon platform. We have reviewed the work on sources, modulators, and receivers. We have shown that single-frequency sources, such as microrings or DBR-lasers can be miniaturized. Threshold current, and hence, power consumption can potentially be decreased to a level that is competitive with the energy consumption in electronic links. Also, we have shown that in the hybrid silicon platform MLLs can be made that have outputs with large optical bandwidths. By stabilizing the output in repetition rate and by locking the frequency of one of the modes, a mode comb is created that can be used as a multiwavelength source for WDM applications.

High-speed modulators have been discussed and successful operation of an EAM modulator with modulation speed of 25 Gb/s has been shown. This result allows for high-speed optical links on silicon photonic chips, where modulation speeds are typically limited. Although the speed of the first realizations of hybrid silicon receivers was still limited to 6 GHz, a high sensitivity of -17.5 dBm was shown, which is useful for power efficient links.

As a last point, we have shown that with technologies like QWI, these different components can be integrated on a single silicon chip. Successful demonstration of QWI has been shown by integrating an EAM with a SG-DBR laser, making a complete transmitter that can be modulated with speeds larger than 2 Gb/s.

In Fig. 25, we have mapped the results in this paper on the roadmap presented by Miller [1]. Three important conclusions can be drawn. First of all EAMs are the preferred technology over MZMs, since their energy consumption is about two orders of magnitude lower and well within the requirements for the next years. Second, using on-chip sources with low enough energy consumption will be a challenge, even with the projected values presented in this paper. This leads to the third conclusion, namely that an off-chip multiwavelength source, e.g., a MLL, seems to be the most promising approach for meeting the targets in the roadmap up to 2022.

In summary, the hybrid silicon technology offers a complete set of components for optical interconnects, which can, in principle, all be realized on a single chip. Moreover, the fabrication technology is compatible with current CMOS processing. So concluding, it can be stated that this platform is very promising for future on-chip and off-chip interconnects and might pose a more energy efficient solution for high-speed and high-bandwidth systems.

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REFERENCES

[1] D. A. B. Miller, "Device requirements for optical interconnects to silicon chips," *Proc. IEEE*, vol. 97, no. 7, pp. 1166–1185, Jul. 2009.

[2] A. Benner, M. Ignatowski, J. A. Kash, D. M. Kuchta, and M. B. Ritter, "Exploitation of optical interconnects in future server architectures," *IBM J. Res. Dev.*, vol. 49, no. 4/5, pp. 755–775, 2005. [Online]. Available: http://www.zurich.ibm.com/st/photonics/interconnects.html

[3] R. Nagarajan, M. Kato, J. Pleumeekers, P. Evans, D. Lambert, A. Chen, V. Dominic, A. Mathur, P. Chavarkar, M. Missey, A. Dentai, S. Hurtt, J. Bäck, R. Muthiah, S. Murthy, R. Salvatore, C. Joyner, J. Rossi, R. Schneider, M. Ziari, H.-S. Tsai, J. Bostak, M. Kauffman, S. Pennypacker, T. Butrie, M. Reffle, D. Mehuys, M. Mitchell, A. Nilsson, S. Grubb, F. Kish, and D. Welch, "Large-scale photonic integrated circuits for long-haul transmission and switching," *J. Opt. Netw.*, vol. 6, pp. 102–111, 2007.

[4] Blazar (LUX5010A), 40 Gigabit active optical cable (2009, Oct.). [Online]. Available: http://www.luxtera.com/

[5] (2007). [Online]. Available: http://www.itrs.net/Links/2007ITRS/ExecSum2007.pdf

[6] J. Ahn, M. Fiorentino, R. G. Beausoleil, N. Binkert, A. davis, D. Fattal, N. P. Jouppi, M. McLaren, C. M. Santori, R. S. Schreiber, S. M. Spillane, D. Vantrease, and Q. Xu, "Devices and architectures for photonic chip-scale integration," *Appl. Phys. A*, vol. 95, pp. 989–997, Feb. 2009.

[7] R. Dangel, R. Beyeler, N. Meier, T. Lamprecht, F. Horst, D. Jubin, J. Weiss, and B. J. Offrein, "Optical interconnects for board level applications," *Proc. SPIE*, vol. 7219, pp. 721904-1–721904-7, 2009.

[8] T. Barwicz, H. Byun, F. Gan, C. W. Holzwarth, M. A. Popović, P. T. Rakich, M. R. Watts, E. P. Ippen, F. X. Kärtner, H. I. Smith, J. S. Orcutt, R. J. Ram, V. Stojanovic, O. O. Olubuyide, J. L. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, and J. U. Yoon, "Silicon photonics for compact, energy-efficient interconnects," *J. Opt. Netw.*, vol. 6, no. 1, pp. 63–73, Jan. 2007.

[9] M. K. Smit, E. A. J. M. Bente, M. T. Hill, F. Karouta, X. J. M. Leijtens, Y. S. Oei, J. J. G. M. Van Der Tol, R. Nötzel, P. M. Koenraad, H. S. Dorren, H. de Waardt, A. M. J. Koonen, and G. D. Khoe, "Current status and prospects of photonic IC technology," presented at the IEEE 19th Int. Conf. Indium Phosphide Rel. Mater., Copenhagen, Denmark, 2007.

[10] O'Connor, "On-chip optical interconnect for low-power," in *Ultra Low-Power Electronics and Design*, E. Macii, Ed. Norwell, MA: Kluwer, 2004.

[11] S. D. Gunapala, S. V. Bandara, J. K. Liu, J. M. Mumolo, D. Z. Ting, C. J. Hill, J. Nguyen, B. Simolon, J. Woolaway, S. C. Wangc, W. Li, P. D. LeVan, and M. Z. Tidrow, "1024 $\times$ 1024 Format pixel co-located simultaneously readable dual-band QWIP focal plane," *Infrared Phys. Technol.*, vol. 52, pp. 395–398, 2009.

[12] C. R. Doerr and K. Okamoto, "Advances in silica planar lightwave circuits," *J. Lightw. Technol.*, vol. 24, no. 12, pp. 4763–4789, Dec. 2006.

[13] J. Buus and E. J. Murphy, "Tunable lasers in optical networks," *J. Lightw. Technol.*, vol. 24, no. 1, pp. 5–11, Jan. 2006.

[14] D. R. Zimmerman and L. H. Spiekman, "Amplifiers for the masses: EDFA, EDWA, and SOA amplets for metro and access applications," *J. Lightw. Technol.*, vol. 22, no. 1, pp. 63–67, Jan. 2004.

[15] H. Rong, R. Jones, A. Liu, O. Cohen, D. Hak, A. Fang, and M. Paniccia, "A continuous-wave Raman silicon laser," *Nature*, vol. 433, pp. 725–728, Feb. 2005.

[16] J. Liu, X. Sun, R. Camacho-Aguilera, L. Kimerling, and J. Michel, "Ge-on-Si laser operating at room temperature," *Opt. Lett.*, vol. 35, no. 5, pp. 679–681, Mar. 2010.

[17] A. V. Krishnamoorthy, R. Ho, X. Zheng, H. Schwetman, J. Lexau, P. Koka, G. Li, I. Shubin, and J. E. Cunningham, "The integration of silicon photonics and VLSI electronics for computing systems intra-connect," in *Proc. SPIE*, 7220, 72200V, 2009. doi:10.1117/12.813416 (Silicon Photonics IV, San Jose, CA, USA, Jan. 26, 2009).

[18] C. Gunn, "CMOS photonics for high speed interconnects," in *Proc. ECS 210th Meeting*, 2006, pp. 58–66.

[19] A. Akrout, A. Shen, R. Brenot, F. Van Dijk, O. LeGouezigou, F. Pommereau, F. Lelarge, A. Ramdane, and G.-H. Duan, "Error-free transmission of 8 WDM channels at 10 Gbit/s using comb generation in a quantum dash based mode-locked laser," in *Proc. 34th Eur. Conf. Opt. Commun. (ECOC'08)*, Brussels, Belgium, 2008.

[20] A. R. Kovsh, G. L. Wojcik, D. Yin, A. E. Gubenko, I. Krestnikov, S. S. Mikhrin, and D. A. Livshits, "Cost-effective DWDM optical interconnects enabled by quantum dot comb laser," in *Proc. SPIE Photonics West 2010*, pp. 76070W–76070W-9.

[21] G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, and J. E. Bowers, "III-V/silicon photonics for on-chip and intra-chip optical interconnects," *Laser Photon. Rev.*, vol. 9999, pp. 1–29, 2010.

[22] F. Bordas, R. Zhang, E. J. Geluk, F. Karouta, J. J. G. M. Van Der Tol, P. J. van Veldhoven, R. Nötzel, M. K. Smit, G. Roelkens, D. Van Thourhout, and R. Baets, "Compact passive devices in InP membrane on silicon," presented at the 35th Eur. Conf. Opt. Commun., Vienna, Austria, Sep. 20–24, 2009.

[23] A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, "Electrically pumped hybrid AlGaInAs-silicon evanescent laser," *Opt. Exp.*, vol. 14, no. 20, pp. 9203–9210, Oct. 2006.

[24] C. E. Zah, R. Bhat, B. N. Pathak, F. Favire, W. Lin, M. C. Wang, N. C. Andreadakis, D. M. Huang, M. A. Koza, T. P. Lee, Z. Wang, D. Darby, D. Flanders, and J. J. Hsieh, "High-performance uncooled 1.3-μm $Al_xGa_yIn_{1-x-y}As$/InP strained-layer quantum-well lasers for subscriber loop applications," *IEEE J. Quantum Electron.*, vol. 30, no. 2, pp. 511–523, Feb. 1994.

[25] X. K. Sun, A. Zadok, M. J. Shearn, K. A. Diest, A. Ghaffari, H. A. Atwater, A. Scherer, and A. Yariv, "Electrically pumped hybrid evanescent Si/InGaAsP lasers," *Opt. Lett.*, vol. 34, pp. 1345–1347, May 2009.

[26] H. Park, Y. H. Kuo, A. W. Fang, R. Jones, O. Cohen, M. J. Paniccia, and J. E. Bowers, "A hybrid AlGaInAs-silicon evanescent preamplifier and photodetector," *Opt. Exp.*, vol. 15, no. 21, pp. 13539–13546, Oct. 2007.

[27] D. Liang, J. E. Bowers, D. C. Oakley, A. Napoleone, D. C. Chapman, C. L. Chen, P. W. Juodawlkis, and O. Raday, "High-quality 150 mm InP-to-silicon epitaxial transfer for silicon photonic integrated circuits," *Electrochem. Solid-State Lett.*, vol. 12, no. 4, pp. H101–H104, Jan. 2009.

[28] G. Roelkens, J. Van Campenhout, J. Brouckaert, D. Van Thourhout, R. Baets, P. Rojo Romeo, P. Regreny, A. Kazmierczak, C. Seassal, X. Letartre, G. Hollinger, J. M. Fedeli, L. Di Cioccio, and C. Lagahe-Blanchard, "III-V/Si photonics by die-to-wafer bonding," *Mater. Today*, vol. 10, no. 7/8, pp. 36–43, Jul./Aug. 2007.

[29] A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. J. Paniccia, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," *Nature*, vol. 427, pp. 615–618, 2004.

[30] W. Bogaerts, S. K. Selvaraja, P. Dumon, J. Brouckaert, K. De Vos, D. Van Thourhout, and R. Baets, "Silicon-on-insulator spectral filters fabricated with CMOS technology," *IEEE J. Sel. Top. Quantum Electron.*, vol. 16, no. 1, pp. 33–44, Jan./Feb. 2010.

[31] K. Yamada, T. Tsuchizawa, T. Watanabe, H. Shinojima, H. Fukuda, H. Nishi, S. Park, Y. Ishikawa, K. Wada, and S. Itabashi, "Integrated photonic platform based on silicon photonic wire waveguides," in *Proc. SPIE*, 7606, 76060T, 2010, doi:10.1117/12.840889

[32] A. W. Fang, M. N. Sysak, B. R. Koch, R. Jones, E. Lively, Y.-H. Kuo, D. Liang, O. Raday, and J. E. Bowers, "Single-wavelength silicon evanescent lasers," *IEEE J. Sel. Top. Quantum Electron.*, vol. 15, no. 3, pp. 535–544, May/Jun. 2009.

[33] D. Derrickson, *Fiber Optic Test and Measurement*. Englewood Cliffs, NJ: Prentice-Hall, 1998.

[34] D. Liang, M. Fiorentino, T. Okumura, H.-H. Chang, D. T. Spencer, Y.-H. Kuo, A. W. Fang, D. Dai, R. G. Beausoleil, and J. E. Bowers, "Electrically-pumped compact hybrid silicon microring lasers for optical interconnects," *Opt. Exp.*, vol. 17, no. 22, pp. 20355–20364, Oct., 2009.

[35] A. W. Fang, B. R. Koch, R. Jones, E. Lively, D. Liang, Y.-H. Kuo, and J. E. Bowers, "A distributed bragg reflector silicon evanescent laser," *IEEE Photon. Technol. Lett.*, vol. 20, no. 20, pp. 1667–1669, Oct. 2008.

[36] H. Dorren and O. Raz, "Will photonics penetrate into inter-chip and intra-chip communications?," presented at the ECOC 2009, Vienna, Austria.

[37] B. Docter, E. J. Geluk, F. Karouta, and M. K. Smit, “Deep etched DBR gratings in InP for photonic integrated circuits,” in *Proc. Eur. Conf. Integr. Opt.*, Copenhagen, Denmark, Apr. 25–27,2007, p. ThG20.

[38] J. Van Campenhout, P. R. A. Binetti, P. Rojo Romeo, P. Regreny, Ch. Seassal, X. J. M. Leijtens, T. de Vries, Y. S. Oei, P. J. van Veldhoven, R. Nötzel, L. Di Cioccio, J.-M. Fedeli, M. K. Smit, D. Van Thourhout, and R. Baets, “Low-footprint optical interconnect on an SOI chip through heterogeneous integration of InP-based microdisk lasers and microdetectors,” *IEEE Photon. Technol. Lett.*, vol. 21, no. 8, pp. 522–524, Apr. 2009.

[39] Q. Xu, B. Schmidt, J. Shakya, and M. Lipson, “Cascaded silicon microring modulators for WDM optical interconnection,” *Opt. Exp.*, vol. 14, no. 20, pp. 9430–9435, Oct. 2006.

[40] S. Arahira, N. Mineo, K. Tachibana, and Y. Ogawa, “40-GHz hybrid modelocked laser diode module operated at ultra-low RF power with impedance-matching circuit,” *Electron. Lett.*, vol. 39, pp. 287–289, 2003.

[41] Z. G. Lu, J. R. Liu, P. J. Poole, S. Raymond, P. J. Barrios, D. Poitras, G. Pakulski, X. P. Zhang, K. Hinzer, and T. J. Hall, “Low noise InAs/InP quantum dot C-band monolithic multiwavelength lasers for WDM-PONs,” presented at the OFC 2009, San Diego, CA, Paper JWA27.

[42] A. Akrout, K. Merghem, J. P. Tourrenc, A. Martinez, A. Shen, F. Lelarge, G.-H. Duan, and A. Ramdane, “Generation of 10 GHz optical pulses with very low timing jitter using one section passively mode locked quantum dash based lasers operating at 1.55 μm,” in *Proc. OFC 2009*, Paper JThA30.

[43] B. R. Koch, A. W. Fang, O. Cohen, and J. E. Bowers, “Mode-locked silicon evanescent lasers,” *Opt. Exp.*, vol. 15, no. 18, pp. 11225–11233, Aug. 2007.

[44] A. W. Fang, B. R. Koch, K.-G. Gan, H. Park, R. Jones, O. Cohen, M. J. Paniccia, D. J. Blumenthal, and J. E. Bowers, “A racetrack mode-locked silicon evanescent laser,” *Opt. Exp.*, vol. 16, no. 2, pp. 1393–1398, Jan. 2008.

[45] J. J. Plant, J. T. Gopinath, B. Chann, D. J. Ripin, R. K. Huang, and P. W. Juodawlkis, “250 mW, 1.5 μm monolithic passively mode-locked slab-coupled optical waveguide laser,” *Opt. Lett.*, vol. 31, no. 2, pp. 223–225, 2006.

[46] H. K. Tsang, C. S. Wong, T. K. Liang, I. E. Day, S. W. Roberts, A. Harpin, J. Drake, and M. Asghari, “Optical dispersion, two-photon absorption and self-phase modulation in silicon waveguides at 1.5 μm wavelength,” *Appl. Phys. Lett.*, vol. 80, pp. 416–418, 2002.

[47] H. Fukano, T. Yamanaka, M. Tamura, and Y. Kondo, “Very-low-driving-voltage electroabsorption modulators operating at 40 Gb/s,” *J. Lightw. Technol.*, vol. 24, no. 5, pp. 2219–2224, May 2006.

[48] Y.-H. Kuo, H.-W. Chen, and J. E. Bowers, “High speed hybrid silicon evanescent electro-absorption modulator,” *Opt. Exp.*, vol. 16, no. 13, pp. 9936–9941, Jun. 2008.

[49] H.-W. Chen, Y.-H. Kuo, and J. E. Bowers, “25 Gb/s hybrid silicon switch using a capacitively loaded traveling wave electrode,” *Opt. Exp.*, vol. 18, no. 2, pp. 1070–1075, Jan. 2010.

[50] H.-H. Chang, Y.-H. Kuo, H.-W. Chen, R. Jones, A. Barkai, M. J. Paniccia, and J. E. Bowers, “Integrated triplexer on hybrid silicon platform,” in *Proc. OFC 2010*, Paper OThC4.

[51] P. Binetti, X. Leijtens, T. de Vries, Y. Oei, O. Raz, L. Di Cioccio, J.-M. Fedeli, C. Lagahe, R. Orobtchouk, J. Van Campenhout, D. Van Thourhout, P. van Veldhoven, R. Nötzel, and M. Smit, “Indiumphosphide based membrane photodetector for optical interconnects on silicon,” in *Proc. LEOS Annu. Conf.*, Newport Beach, CA, Nov. 2008, pp. 302–303, Paper TuT4.

[52] P. R. A. Binetti, X. J. M. Leijtens, A. M. Ripoll, T. de Vries, E. Smalbrugge, Y. S. Oei, L. Di Cioccio, J.-M. Fedeli, C. Lagahe, R. Orobtchouk, D. Van Thourhout, P. J. van Veldhoven, R. Nötzel, and M. K. Smit, “InP-based photodetector bonded on CMOS with Si3N4 interconnect waveguides,” presented at the IEEE LEOS Annu. Meeting Conf., Belek-Antalya, Oct. 4–8, 2009.

[53] J. J. M. Binsma, M. van Geemert, F. Heinrichsdorff, T. van Dongen, R. G. Broeke, and M. K. Smit, “MOVPE waveguide regrowth in InGaAsP/InP with extremely low butt joint loss,” in *Proc. Symp. IEEE/LEOS Benelux Chapter*, Brussels, Belgium, 2001, pp. 245–248.

[54] M. N. Sysak, J. O. Anthes, J. E. Bowers, O. Raday, and R. Jones, “Integration of hybrid silicon lasers and electroabsorption modulators,” *Opt. Exp.*, vol. 16, no. 17, pp. 12478–12486, Aug. 2008.

[55] E. J. Skogen, J. S. Barton, S. P. Denbaars, and L. A. Coldren, “A quantum-well-intermixing process for wavelength-agile photonic integrated circuits,” *J. Sel. Top. Quantum Electron.*, vol. 8, pp. 863–869, 2002.

[56] D. Nie, T. Mei, H. S. Djie, M. K. Chin, X. H. Tang, and Y. X. Wang, “Implementing multiple bandgaps using inductively coupled argon plasma enhanced quantum well intermixing,” *J. Vac. Sci. Technol. B*, vol. 23, pp. 1050–1053, 2005.

[57] SMART 2020: Enabling the Low Carbon Economy in the Information Age. (2008, Jun.). [Online]. Available: http://www.gesi.org/

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