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Coated Silicon Nanowires as Anodes in Lithium Ion Batteries

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Coated Silicon Nanowires as Anodes in Lithium Ion Batteries

A thesis submitted in partial satisfaction of the requirements for the degree Master of Science in Chemistry

by

David James Watts

2014

ABSTRACT OF THE THESIS

Coated Silicon Nanowires as Anodes in Lithium Ion Batteries

by

David James Watts

Master of Science in Chemistry
University of California, Los Angeles, 2014
Professor Sarah H. Tolbert, Chair

Even though it has the highest known theoretical specific capacity of any material (~3600 mAh/g), silicon has limited use as an anode in lithium ion batteries due to the mechanical instability caused by the large volume expansion that occurs upon Li insertion. This volume expansion not only contributes to mechanical instability in the active silicon, but it also contributes to mechanical instability in the solid electrolyte interphase (SEI), a film formed at the end of the first lithiation step. The result of this mechanical instability in the SEI is diminished cycling performance. Modifying the SEI formation by growing a SiO_2 layer on silicon nanowires (SiNW) or coating them with $Li_xAl_ySi_zO$ (LASO), we report improved cycle life and rate capability. Here we show SiNW with a thin SiO_2 layer achieved nearly 400 cycles at a capacity of 2400 mAh/g and LASO-coated SiNW cycled stably at 5.5C.

The thesis of David James Watts is approved.

Laurent G. Pilon

Xiangfeng Duan

Sarah H. Tolbert, Committee Chair

University of California, Los Angeles

2014

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CHAPTER 1: Coated Silicon Nanowires as Anodes in Lithium Ion Batteries

ACKNOWLEDGMENTS

In all honesty, I don't think I went to graduate school for the right reasons. After spending a few years at UCLA, I felt like I had to do something else with my life. On April 19, 2013, my p. i., Professor Sarah Tolbert gave me a necessary kick in the pants. I began working a lot more in lab and I began seeing promising data. Eventually, I had what I believed was a respectable amount of good data. When I decided that I needed to leave graduate school for my mental health's sake, I had to make a decision. I could do one of three things: I could take a leave of absence, I could immediately leave with a course-work Master's, or I could spend an extra quarter at UCLA writing a Master's thesis. I chose the latter option and I decided to write this Master's thesis because I felt like it was worth reporting some of the exciting cycling data that I had collected while working in the Tolbert group.

I'd like to thank Professor Sarah Tolbert. While she has supervised my research, she has also gone above and beyond to help me with some of my life challenges. I am especially grateful for her willingness to take me to counseling services at UCLA when I was going through a very rough time mentally.

I'd also like to thank my best friend, coworker, and roommate Abraham Buditama. I met Abraham my first day of graduate school in August 2010. He has been and continues to be a positive influence in my life, especially when I am struggling mentally with many of the disappointments I've experienced in graduate school and life in general.

I'd also like to thank my coworker and friend John Cook. John has been and continues to be a great asset to our lab.

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While I did not get to meet E. Joseph Nemanick and Jacob T. Cox, I do want to say thank you to them for laying the ground work for my silicon anode project and especially Dr. Nemanick for the advice he has provided to me via e-mail.

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CHAPTER 1

Coated Silicon Nanowires as Anodes in Lithium Ion Batteries

1.1 Introduction

Lithium ion batteries are widely used in small portable electronic devices.[1–3] Replacing the typical graphitic carbon anode with a silicon anode has the potential to increase power and energy density of lithium ion batteries. Silicon is an attractive anode material because it has the highest known theoretical lithium ion storage capacity of any material. At room temperature, silicon can alloy with lithium to form the $Li_{15}Si_4$ state, reaching a theoretical capacity of about 3579 mAh/g. At elevated temperatures, silicon can alloy with lithium to form the $Li_{22}Si_5$ state, reaching a theoretical capacity of 4200 mAh/g. These are both about 10 times that of the theoretical capacity of graphitic carbon (372 mAh/g).[4–6]

The main challenge with using silicon in batteries is the large volume expansion (approximately 300%) that occurs when lithium ions are repeatedly inserted into and removed out of silicon in the aforementioned alloying process. This volume expansion can crack the active material and shorten the battery's cycle life.[7–9] Many research groups have synthesized various nanostructures of silicon, which have a large surface area to volume ratio and, as a result, can better handle this volume expansion.[10–13] Of these nanostructures, silicon nanowires have shown superior cycling capabilities over bulk silicon anodes and many other silicon nanostructures. The rationale for this superior performance is silicon nanowires have short

lithium ion diffusion distances in the radial direction and fast electron charge transport in the axial direction.[3,10,14]

While nanoscale porosity is often considered to be just another form of nanostructuring, it has several distinct advantages for the work described here. Nanoporous materials combine the surface area and diffusion lengths of very small nanocrystals with a multiply-interconnected network for improved electrical conductivity. Nanoporous materials can also be much more flexible than their bulk counterparts.[15] Conventionally, high surface area porous silicon is formed by etching bulk Si in a F^- containing electrolyte at an oxidizing potential (50-100V)[16] or a high light flux. These porous films have features on the order of 50 nm and greater, and attempting to form thinner pore walls causes pore merging and collapse.[17–19] Previous work on porous Si for Li^+ anode materials has shown an improvement in the cycling of the material as the feature size, such as pore walls or particle diameter, decreases below 50 nm.[20,21] Research from our group on nanoporous cathodes with 10 – 15 nm sized pores also indicates that such porosity can increase material flexibility upon cycling.[22,23] Formation of Si with small, controlled pore sizes should thus allow for fast cycling and a retention of structural integrity during alloying/dealloying and the associated volume changes.

Recently, nanoporous SiNW have been synthesized from Ag^+/HF etched single crystal Si. The nanowire formation process is similar to other procedures for the etching of Si, with the oxidation (injection of holes) coming from the reduction of Ag^+ in solution to Ag(s) in the presence of the Si and F^- to form the $(SiF_6)^{2-}$ ion.[24–26] The Ag(s) is then redissolved in the HF solution, regenerating the Ag^+ and forming H_2. The wires maintained 2000 mAh/g, 1600 mAh/g, and 1100 mAh/g capacity when cycled at 0.5C, 1C, and 4.5C, respectively with alignate binder.[9]

Here we describe the formation of Li^+ secondary battery electrodes consisting of binder-free porous SiNW arrays from Ag^+/HF etched single crystal Si.[24] These SiNW arrays form high capacity, stable anode materials for Li^+ alloying and charge storage. Since we can cycle the porous SiNW without detaching them from the Si substrate, this technology has the potential to be integrated with other lithographically-produced devices or circuits for on-chip charge storage.[8,14] These wires are electrically conductive and attached to a conductive substrate, so they do not require the use of an inert binder and the specific capacity of electrodes can be much higher. Also, since the Si wires are intrinsically connected to a Si substrate, volume expansion does not ruin connection to current collector and hence, they have exciting potential for integrated, on chip power. Matching this high capacity anode material with a similarly high capacity cathode material could produce major strides in the field of high capacity/light weight power sources.

In addition to cycling this binder-free all Si system, we also cycled coated SiNW. Coating the wires to improve cycling performance usually involves controlling growth of the solid electrolyte interface (SEI layer). When cycling the SiNW anode at potentials close to metal lithium, the solvent and lithium salt in the electrolyte are electrochemically reduced, forming an insoluble film called the SEI layer. This layer is electrically insulating, but conducts lithium ions. Due to expansion and contraction of the SiNW during cycling, the SEI layer is not static. When the lithium ions are intercalated into silicon, the wires expand in volume and decomposition of the electrolyte causes the formation of an SEI layer. When lithium ions are removed from silicon, the wires decrease in volume. This large volume decrease can cause cracking in the SEI layer, exposing fresh silicon to the electrolyte. During the next cycle, more SEI film is formed when the electrolyte decomposes on newly-exposed, fresh silicon. This

results in an SEI layer which grows with cycling. The growing SEI layer can hurt cycle life by increasing the lithium ion diffusion distance through the SEI film, applying extra mechanical stress to the electrode, and irreversibly consuming lithium ions and electrolyte. Clearly, forming a stable SEI layer is critical for a stable cycling in silicon anodes.[6,27–29]

In order to grow an SEI layer with a constant morphology, there have been significant research efforts put into growing various silicon oxides on SiNW to extend cycle life.[3,6,27,28] For example, it was found that SiNW with a 2-5 nm thick amorphous native oxide are less likely to have electrolyte reduced to form SEI than wires which have had their native oxide stripped off by HF. The result of this is the native oxide wires have a longer cycle life than oxide-free wires.[27] It was also found that wires with an optimized surface oxide thickness can mechanically limit the volume expansion.[3] Using this and a hollow nanostructure,[30] double wall silicon nanotubes were synthesized. The outer silicon oxide wall was mechanically rigid and the inner hollow space allowed for the volume expansion upon lithiation. Upon cycling, the material showed a stable SEI, long cycle life, good capacity retention, and good rate capabilities.[28]

Some studies have focused specifically on growing SiO_2 layers on Si anodes.[3,31,32] In one of these studies, they varied the thickness of the SiO_2 and examined the cycling behavior of these structures. They found that a thin SiO_2 can suppress the volume expansion, but too thick of an SiO_2 coating can diminish the specific capacity and coulomb efficiency.[32]

In this work, we aim to build upon these previous studies, using methods developed for precise SiO_2 on Si wafer processing to grow nearly defect-free thin 0.7 to 1.4 nm thick SiO_2 layers on our silicon wires. We use methods optimized to avoid high leakage current density and to avoid the high oxidation rates that can arise as a result of thermal oxidation. We use methods

based on dipping Si samples in HNO_3, and varying temperature and time of immersion. This method produced samples with leakage current density as low as that for thermally grown SiO_2 layers and showed good reproducibility of SiO_2 thickness (± 0.05 nm), since the thickness saturates within a short time of immersion in acid.[33]

While controlled silica layer thickness may allow us to optimize coatings for Li^+ conductivity, silica is still fundamentally an ionic insulator, and so only very thin coatings can be used. By moving away from silica, more chemical functionality can be achieved. For example, there has been extensive work over the past few years using both sol-gel chemistry and atomic layer deposition (ALD) to coat electrodes and improve performance.[4,8,34–36] These coatings can provide physical support, preserve the mechanical structure of cycled material, protect electronic conduction pathways, and inhibit side reactions between the electrolyte and active silicon.[8,14,37–39] While some non-ALD coatings seem to modify the SEI layer,[14,37] ALD alumina coating applied can substitute for the SEI layer. Nguyen et. al. applied this alumina coating to SiNW and noted that the coating can act like an artificial SEI layer by forming a Li-Al-O glass film upon the first lithiation. Like the SEI layer, Li-Al-O is a lithium ion conductor and electronic insulator. Even if the ALD alumina coating cracks during cycling, it can still shield some of the active silicon material from the electrolyte. Overall, Nguyen et. al. showed that ALD alumina-coated silicon nanowires showed much better cycling stability than uncoated silicon nanowires.[8]

Despite these improvements, alumina, like silica, is still fundamentally an ionic insulator, and so only very thin coatings can be used. To address this problem, we turn to ALD coatings of $Li_xAl_ySi_zO$ (LASO), which is an intrinsic ion conductor. Lithium aluminosilicates, $Li_{4-3x}Al_xSiO_4$, are Li-ion conducting metal oxide family, with a single-phased solid solution over the range of x = 0 to 0.05.[40] Within Lithium aluminosillicates, $LiAlSiO_4$ (x=1, also known as Beta-

eucryptite) attracted a great deal of interest as a possible electrolyte in high-temperature batteries because of its high ionic conductivity above 400 °C.[41,42] It is a derivative of high quartz, with half of the SiO_4-tetrahedra of high quartz replaced by AlO_4 tetrahedra, where Li-ions are stuffed in the structural channels for charge neutrality.[43] Additionally, its ionic conductivity is known to experience increase in magnitude with a decrease in its thickness, which makes it far more advantageous than other solid oxide lithium ion conductors in applications on powering micro/nanoscale devices;[42] thereby making beta-eucryptite more favorable material to investigate for a solid electrolyte in micro lithium-ion battery applications.

Like the aforementioned ALD alumina, ALD LASO acts like an artificial SEI layer during cycling. ALD LASO is a lithium ion conductor and one benefit LASO-coated wires may have over alumina-coated wires is that a pre-lithiated anode material can be more readily paired with lithium-free cathode materials in order to make a full battery.[44]

Here, we made porous SiNW using the aforementioned well-developed electroless etching method. We immersed some samples in nitric acid to grow SiO_2 layers and we coated other samples with LASO using ALD. We present the characterization of our wires and then analyze the potentiostatic cycling data, comparing the max C-rate, initial coulomb efficiency, max coulomb efficiency, and cycle life. We found that all coated wires have similarly long cycle life. For the samples tested, there is sample-to-sample variation, but all samples are in the range from 200 – 400 cycles. The coatings differ significantly in terms of rate capability, however. For samples cycled at a capacity of 2300-2400 mAh/g, LASO-coated SiNW could accommodate the highest rate of our samples, cycling stably at 5.5C.

1.2 Experimental

Silicon Nanowire Array Preparation

Silicon nanowire arrays were etched into 500 micrometer thick prime grade p-doped (B) silicon (100) wafers (0.001 – 0.005 Ω cm).[24] These wafers were cut into approximately 1 cm^2 pieces and the back, unpolished side of the wafer pieces were marked with a small dot of nail polish. The samples were cleaned with ethanol and immersed in 5 mL of 20mM $AgNO_3$ dissolved in 10% HF at 60°C for between 10 minutes and 3 hours. Soon after immersing the samples in the etching solution, hydrogen evolution is observed and the sample becomes encased in a silver cocoon. After the nanowire arrays were etched, the sample was rinsed with 18 M Ω water, the silver cocoon was dissolved in 69% nitric acid, and the sample was rinsed again with 18 M Ω water. Then, the sample was rinsed with ethanol and air dried. Before cycling bare silicon nanowire arrays, samples were dipped in 48% HF for 30 seconds, rinsed with water, dipped in ethanol, and dried under flowing N_2.

Silicon Dioxide Coatings

Dipping the nanowire arrays in HNO_3 to remove the silver cocoon leaves a thin oxide layer on the nanowires.[45] To remove this thin oxide layer and grow new SiO_2 layers, the nanowire arrays were dipped in 48% HF for 30 seconds, rinsed with 18 M Ω water, then immersed in 69% HNO_3.[33] One set of nanowire arrays was removed from the HNO_3 bath after 30 seconds, growing a thin SiO_2 layer, and another set was removed after 26 hours, growing a thicker SiO_2 layer. Both of these samples were then rinsed with 18 M Ω water, dipped in ethanol, and air dried.

LASO Coating

$Li_xAl_ySi_zO$ (LASO) thin films were synthesized via atomic layer deposition in a hot-wall reactor where the chamber wall temperature was 290°C with a base pressure of 60 mTorr. Metalorganic precursors, lithium *tert*-butoxide (LTB, Strem Chemicals, 98%), trimethylaluminum (TMA, Sigma-Aldrich, 97%), and tetraethyl orthosilane (TEOS, Sigma-Aldrich, 99.999%) were used as the sources for Li, Al and Si, respectively, while H_2O vapor, the oxidant, was supplied by a deionized water reservoir. LTB is a solid precursor, thus the precursor host and gas line were heated to 160°C during the process to ensure sufficient vapor flux to the surface. The gas lines of TMA, TEOS and water were heated to 60°C to prevent precursor condensation. LASO thin films were deposited by alternating ALD deposition cycles of LiOH, Al_2O_3 and SiO_2 with a global cycle sequence of 10(Al-O)-6(Li-O)-4(Si-O), where a, b, c represent the local cycle number for each oxide. Five global cycles were performed to achieve a film thickness of ~10nm. Al_2O_3 was chosen to be the first layer as it is known to have excellent adhesion to silicon.[46]

SEM/TEM/SAED/XRD Characterization

TEM images were taken both before and after the nitric acid washing so that the Ag nanoparticles could be imaged. Samples were prepared by sonicating arrays in EtOH for 10 minutes to release the wires from the substrate; the resulting solution was then dropcast onto carbon TEM grids. Low resolution TEM was performed using a Philips CM120 at 120 kV and selected area diffraction (SAED) analysis was performed on a JEOL 2100 at 200 kV. For SEM, samples were imaged either after the nitric acid wash or after both acid washing and HF etching. Samples were dried under flowing nitrogen and affixed to either a 45° stage by carbon tape or mechanically broken and imaged in cross section. For imaging of individual nanowires, arrays

were sonicated in EtOH for 10 minutes and the suspensions of nanowires was dropcast onto Si. Imaging was performed using a field emission SEM (JEOL 6700F). XRD was measured using a Panalytical XPert Pro diffractometer (Cu Kα).

Electrochemical Studies

To prepare the nanowire arrays for lithium cycling studies, the nail polish on the unpolished side was removed with acetone. Wires on the unpolished side of the sample were mechanically removed with a Q-tip. Ga/In eutectic was scratched onto the exposed bulk silicon. A copper wire was attached to the sample using conductive Ag epoxy (Ted Pella Conductive Epoxy). To dry the Ag epoxy, the sample was placed in an Isotemp oven set to 80°C for 20 minutes. Then, insulating epoxy (Loctite Hysol 1C, McMaster-Carr) was applied to the entire sample, leaving only the active silicon nanowire material exposed. To dry the insulating epoxy, the sample was dried in room temperature air for 1 hour, then placed in an Isotemp oven set to 80°C for 3 hours. To remove organic compounds that are given off in the curing process, the sample was rinsed with ethanol.

For one set of samples, any surface oxide created from exposure to the air, during this preparation, was stripped away by immersing the samples into 48% HF for 30 seconds, rinsing them with water, then dunking them in ethanol. These samples were labeled as the "bare SiNW" samples. After the HF stripped off the oxide and the wires were rinsed, they were immediately placed in a pressurized N_2 filled glove box for electrochemical cycling.

The other 3 sets of samples, samples with thin SiO_2, samples with thicker SiO_2, and LASO-coated samples, were placed in the same glove box without this final exposure to HF.

To cycle the samples, an Arbin Instruments BT-2000 potentiostat was wired into the N_2 filled glove box. The electrolyte was prepared by dissolving 1.07 g lithium perchlorate ($LiClO_4$)

in 10 ml of propylene carbonate (PC) to make a 1 M solution. Samples were cycled in a flooded cell, three electrode configuration utilizing the sample as the working electrode and pieces of lithium foil as both the counter and reference electrodes. The voltage window used was between 0.05 V and 1.2 V vs. Li/Li^+. Samples were tested at cycling rates between 0.2 C to 5.8 C.

Sample Weight

To measure the active sample mass without interference from the Si substrate, samples were first alloyed to form Li_xSi_y. The sample was then removed from the glove box and immediately dunked into a 25 mL solution of 5% HNO_3 and 0.1% HF, causing the Li_xSi_y to react vigorously forming H_2 and SiF_6^{2-}. The sample was soaked for 30s and then rinsed with the acid solution. The Si content of the solution was then analyzed using ICP-AA. For 20 µm SiNW samples, the mass per unit area was approximately 116 $\mu g/cm^2$ according to ICP.

Because ICP results can be complicated by HF dissolving quartz components of the ICP machine, the reliability of this result was verified using microbalance measurements. Ten 20 µm SiNW samples were weighed on a CAHN C-31 Microbalance. Then, the SiNWs on the polished side were removed using a Q-tip and the samples were weighed again. The difference should be the mass of the active SiNWs. The area of these samples was measured and calculated using a ruler. For 20 µm SiNW samples, the mass per unit area was approximately 113 ± 6.58 $\mu g/cm^2$. Error in this measurement was calculated by propagating errors when the measurement uncertainties were set equal to the instrument limits of error. For the rest of this report, we assumed the mass of our 20 µm SiNW samples could be calculated by multiplying the active sample area in cm^2 by 116 $\mu g/cm^2$.

1.3 Results

Figure 1.1a shows nanowire arrays formed by this etching process. For a given etching condition, the nanowires had uniform lengths, with the length determined by the etch time.[24] Nanowire arrays were formed from 5 μm long to over 50 μm, and the wires formed at a rate of 13 μm/h. Figures 1.1b and 1.1c are SEM and TEM images of single nanowires, showing the secondary porous structure of the wires. The nanowires have pores of 5-10 nm inner diameter, with pore walls 5-10 nm thickness.

Figure 1.1 The structure of as-synthesized porous SiNW. a) SEM cross section view of SiNW arrays formed from the etching of p-Si in HF/Ag^{+}, b) close up SEM of a single porous SiNW showing the thin pore walls and continuous nature of the nanowires, c) TEM of a single SiNW showing pores and the 5-10 nm thick walls between the pores.

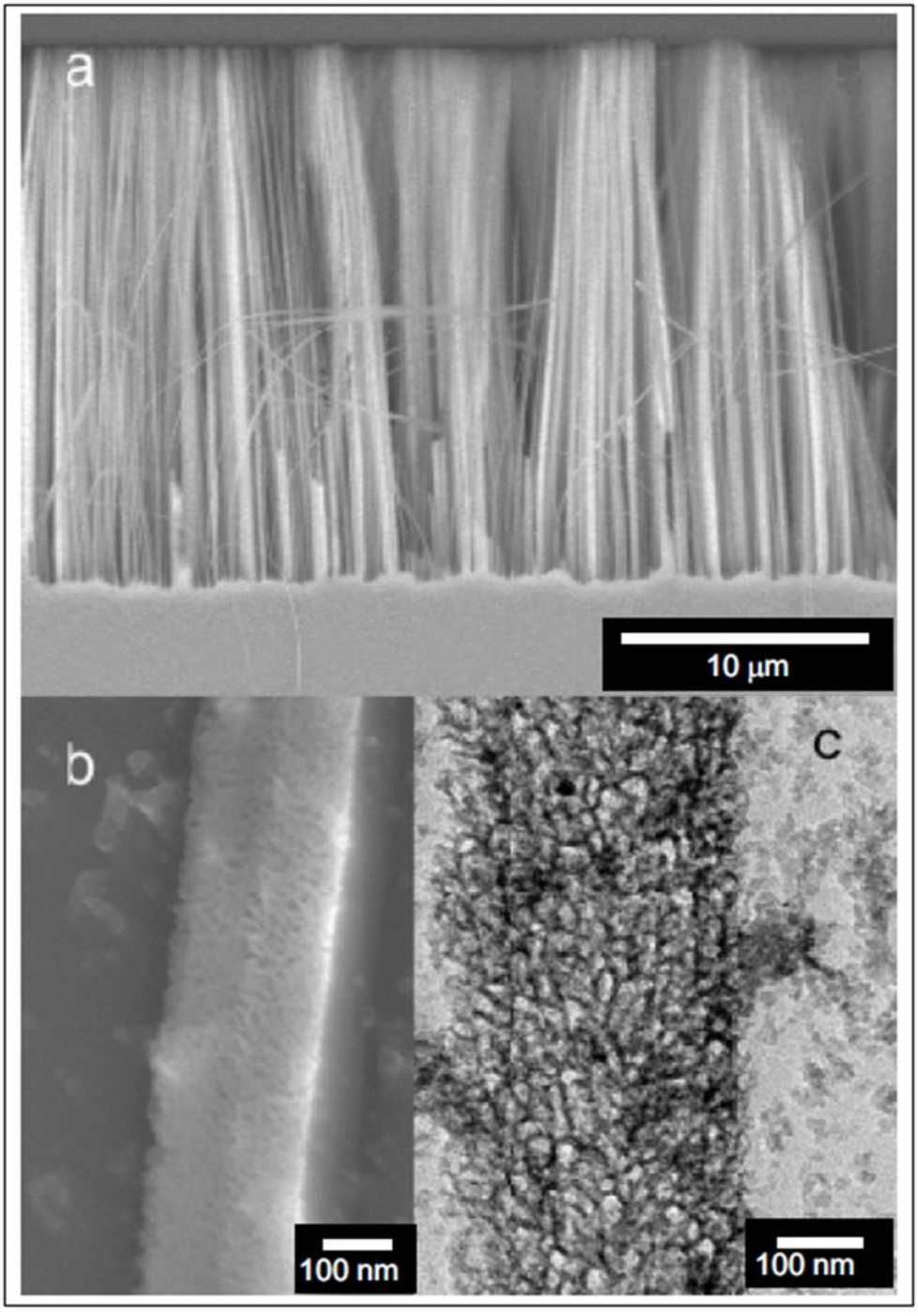
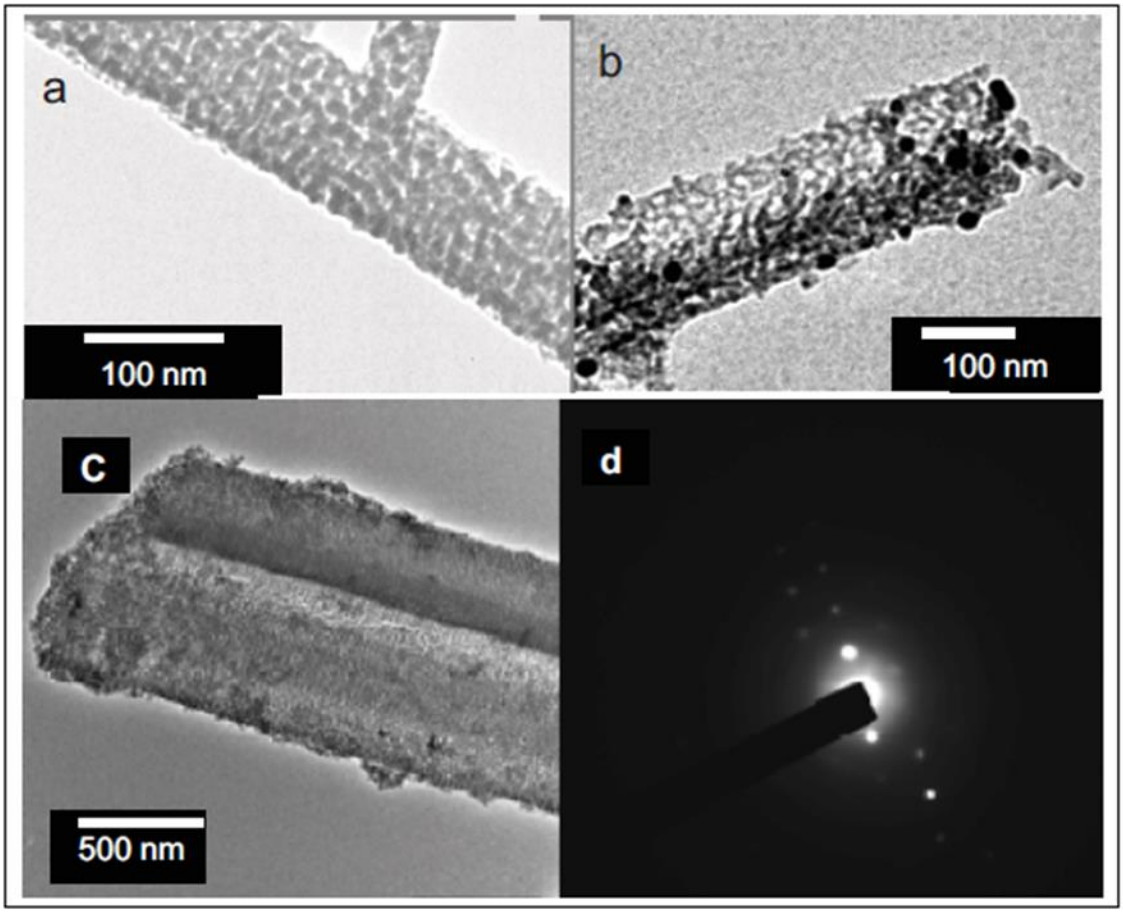


Figure 1.2 shows TEMs of SiNW freed from the substrate, with Figure 1.2a showing a fully washed SiNW. A similar wire without removal of deposited Ag nanoparticles by washing with nitric acid (Figure 1.2b) shows Ag nanoparticles on the surface as well as inside of the nanowire. These nanoparticles etched the pores in the silicon nanowires in a similar fashion to the etching seen of Si wafers by Au, Pt, and Ag.[47,48] These previous studies either used reduction of metal salts to form nanoparticles, or used direct nanoparticle deposition. The metals were placed in contact with the Si and exposed to an oxidizer such as H_2O_2; pores etched preferentially in the {100} family of directions. For the nanowires in this study, while the nanowires formed in the (100) direction, no preferential orientation of the pores within the nanowires was observed, and we believe that the relatively short distances (<100 nm) traveled within the nanowires prevented preferential orientation. We note that in this study, p-type Si was used, but other studies[49] have used n-type to form similar structures, indicating that the dopant type does influence the nanowire formation. Figures 1.2c and d show TEM of a single Si nanowire with the accompanying selected area electron diffraction (SAED) pattern indicating that the initial wires before cycling are crystalline, where only the (100) orientation is apparent.

Figure 1.2 TEM studies of SiNW before cycling. a) TEM of the SiNW after formation and etching in 10% HNO_3 showing the porous nature of the wire, b) SiNW without washing in HNO_3 showing the presence of Ag nanoparticles ranging in size from 3-15 nm on the surface. These nanoparticles cause the porosity of the wires by burrowing through them during wire formation. c) and d) Nanowire image and the corresponding SAED showing the as-formed wires to be single crystalline.



For materials such as Si, which undergo a large volume change upon Li uptake and removal, it has been seen that the smallest dimension of the material,[50,51] in this case the walls between the pores, determines the maximum rate and cyclability of the material. The thin walls between the pores of the Si nanowires allows for minimal strain upon alloying/dealloying while maintaining good conductivity. The mesoporous network also allows for short diffusion lengths, thus increasing the rate at which the arrays can be cycled.

Figure 1.3 shows the electrochemical characterization of the SiNW arrays in 1 M $LiClO_4$/PC. Figure 1.3a shows the cyclic voltammetric characterization of a 20 μm long nanowire array cycled at 5 mV/s. Cycled between 1 V and 0.05 V vs. Li(s)/Li^+, the nanowires show a strong reductive/alloying peak beginning at ~0.3 V and increasing in magnitude down to 0.05 V, where the voltage polarization was reversed. As shown by the lack of a peak in the reductive current, the Si does not completely lithiate by 0.05 V at this charge rate. The full 4200 mAh/g capacity of the SiNW in forming $Li_{22}Si_5$ cannot be reached at any potential positive enough to avoid lithium plating, so the arrays were not cycled to less than 0.05 V to avoid the electrodeposition of Li(s) rather than the lithium silicide formation. The return oxidation peak from the dealloying reaction was broader than the reductive peak, with the SiNW beginning to release their Li at ~ 0.35 V, only 50 mV positive of the onset of the reductive peak, indicating a fast, kinetically facile alloying process.

The galvanostatic alloying of a 20 μm long nanowire array is shown in Figure 1.3b, with a voltage window between 0.05V and 1.2V (versus Li/Li^+) and alloying/dealloying at ±0.4 mA/cm^2. The representative galvanostatic alloying/dealloying curves for the SiNW mirror the cyclic voltammogram, with relatively well-defined regions of alloying and dealloying for the SiNW, made even more distinct by the slower rate. The comparatively narrow reduction peak in the CV and the small potential range of the reduction plateau in the galvanostatic charge starting at ~0.2 V indicates that there was little kinetic overpotential for the lithiation of deeper sites, probably due to the high surface area of the nanowires. The hysteresis seen in the galvanostatic curves (~500 mV separation between the reductive and oxidative plateaus) indicates that the energy storage/extraction process was reasonably efficient.

One challenge of working with SiNW on a Si substrate is that that in some cases, the underlying Si substrate can also be lithiated. Indeed, when these SiNW are cycled slowly over a large potential window, the apparent capacity appeared to increase because additional Si was recruited to the active layer with each cycle. This problem can be alleviated by charging the electrode with a constant number of coulombs that is insufficient to fully alloy the Si wires. The porous wires, due to their high surface area and thin walls, are kinetically easier to alloy than the substrate, and so they will react first. When the total capacity is limited, only the wires will react. Using this capacity-limited cycling only alloys/dealloys the SiNW in the all Si system and thus is a unique binder-free way to cycle SiNW without removing them from the Si substrate.

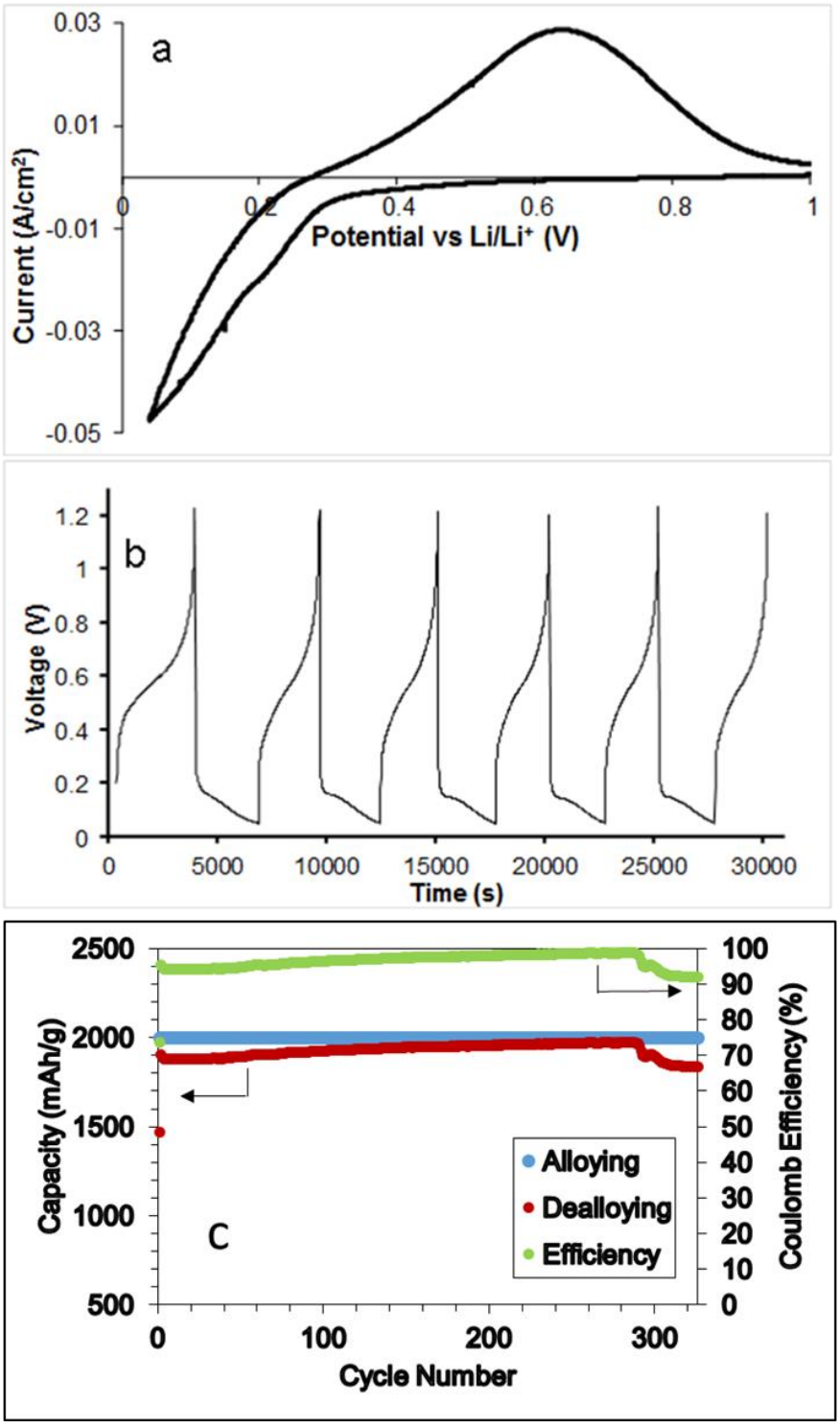
Here, samples were dealloyed at 0.2 mA/cm^2 for 5000s (1 $Coulomb/cm^2$, 0.72C), and alloyed at the same rate/time. This allows us to selectively examine the electrochemical performance of the nanowires without complication from the substrate. Figure 1.3c shows alloying/dealloying capacity as a function of cycle number for 326 cycles. During the capacity-limited lithiation process, a current is applied to alloy lithium with silicon, but some of the lithium is consumed in the formation of the SEI layer. During the capacity-limited delithiation process, the same magnitude of current is used to dealloy lithium. Because the alloying process needs extra lithium for the continuous SEI formation, it takes more Coulombs to complete. Hence, the alloying capacity starts out greater than the dealloying capacity for our wires, but the difference decreases as the SEI stabilizes.

Initially, there is an increase in dealloying capacity which we associate with our capacity-limited cycling and the irreversible conversion of slowly reacting crystalline Si to faster alloying amorphous Si.[52,53] After this initial rise, however, there is no loss of total capacity up to 292 cycles.

The data in figure 1.3c indicates a stable capacity of 2000 mAh/g. This value is lower than the theoretical 4200 mAh/g because our charge-limited technique does not allow the Si to be fully lithiated. Full lithiation requires a voltage near 0V vs. Li/Li^+, and this capacity-limited cycling stopped alloying at 0.05V. This measurement thus gives a lower bound for the specific capacity of these SiNW arrays.

Figure 1.3c also shows the coulomb efficiency, defined as delithiation capacity/lithiation capacity[14] versus cycle number, for this sample. The initial coulomb efficiency was only 74% when the majority of the SEI was forming, but the coulomb efficiency jumped up to 96% by the second cycle and then slowly climbed up to 99%. We believe this climb in coulomb efficiency upon further cycling is due to a slowly growing SEI layer. During lithiation, as less lithium is consumed in the continuous SEI formation process, more lithium is used for the alloying process. Then, during the delithiation process, more lithium can be removed, resulting in a higher dealloying capacity and therefore, a higher coulomb efficiency.

Figure 1.3 Electrochemical characterization of SiNW. (a) Cyclic voltammogram of Li^+ alloying with SiNW, cycled at 5 mV/s, (b) Representative galvanostatic alloying/dealloying curves for SiNW, cycled at 0.4 mA/cm^2, (c) Alloying Capacity, Dealloying Capacity, and Coulomb Efficiency versus Cycle Number for SiNW, cycled at 0.72C.



Analysis of the porous SiNW after Li alloying cycles allows us to understand the stable cycling observed in figure 1.3c. Figure 1.4 shows the retention of individual nanowire structure porosity after cycling 100 times at a rate of 1C. Figure 1.4a shows an SEM of a single nanowire after cycling. While the sharp edges to the porosity seen in Figure 1.1b have been rounded out, the wire still shows clearly defined nanoscale porosity with a length scale similar to that observed in the uncycled wires. Both the individual nanowires and the array in Figure 1.4b show a lack of macroscopic fracturing, in contrast to observations on bulk Si materials.[54,55] TEM analysis of the cycled wires (Figure 1.4 c and d) further confirm the retention of porosity and indicate that pores are now surrounded by a continuous network of nanosized domains, rather than by the straight walls observed in the as-synthesized nanowires. The change is consistent with the conversion of the wire from crystalline Si, which should show well-defined facets, to amorphous Si, which should prefer more spherical domains that minimize surface area. In agreement with this hypothesis, no Si diffraction could be observed in SAED. While the cycled nanowires appear somewhat more disordered than the initial pore structure, they remain porous and structurally intact after cycling, allowing for facile ion transport, good electrical conductivity, and strain minimization during cycling.

Figure 1.4 The structure of the SiNW after cycling 100x at 1C. Parts a and b are SEM, and parts c and d are TEM. Parts (a) and (b) show that both the nanoscale porosity and the nanowire array itself are stable to cycling. High resolution images (c) and (d) further show that both porosity and a connected network are retained in the cycled wires.

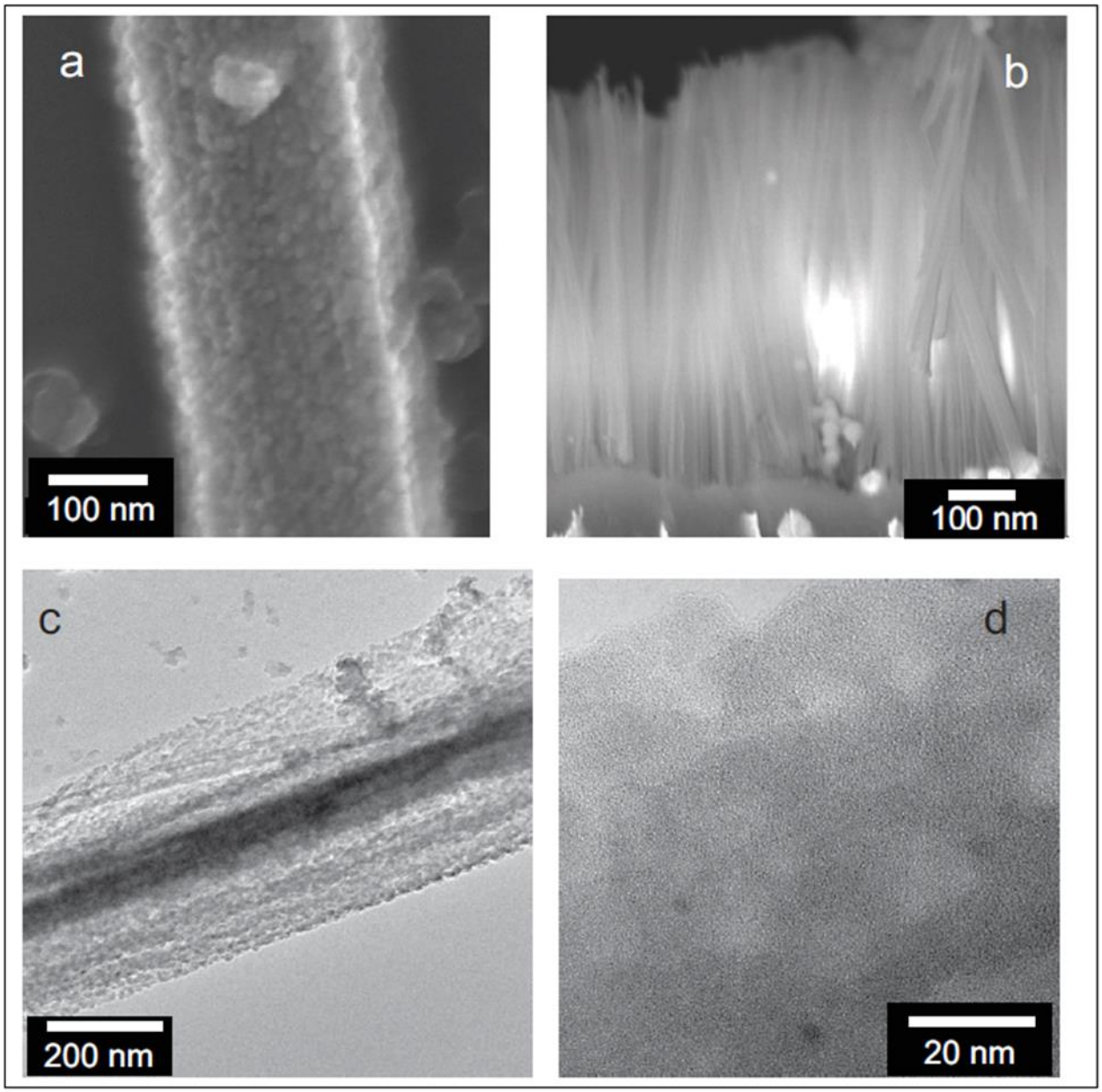
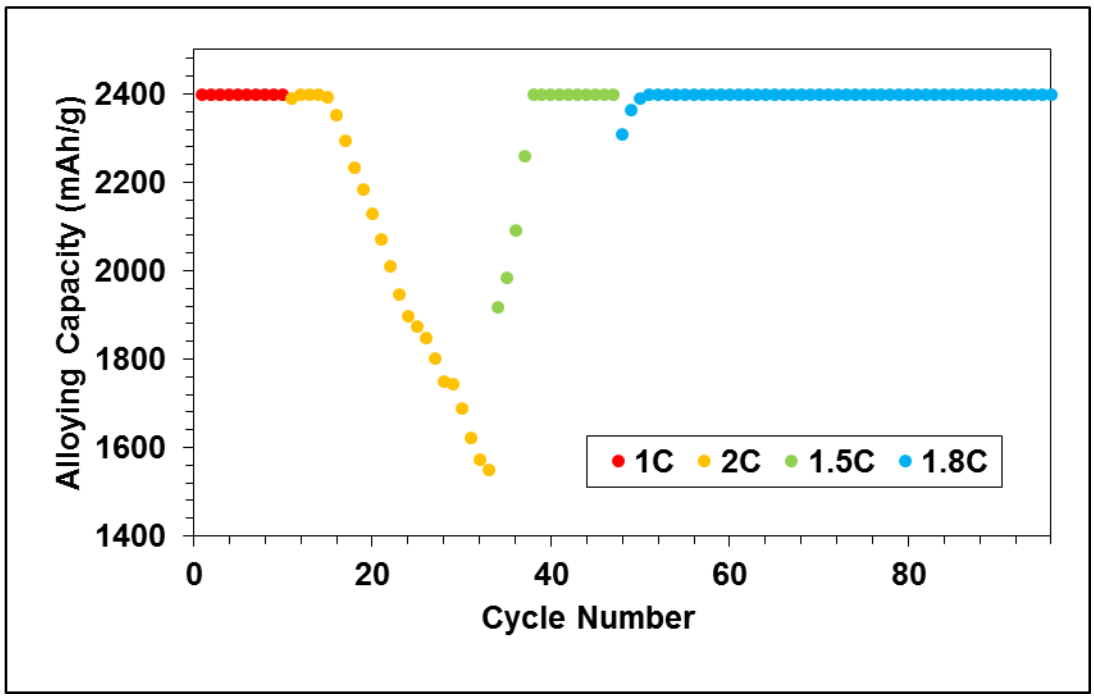


Figure 1.5 shows how we determined the maximum cycle rate for our wires. Our wires were cycled between 0.05 and 1.2V versus Li/Li^+. During stable cycling, the higher voltage limit, 1.2V was reached before the capacity limit was reached. On the other hand, the lower

voltage limit, 0.05 would not be reached before the capacity limit was reached. Only when cycling at much higher C-rates was it possible to reach 0.05V before the capacity limit was reached. We define the max C-rate as the highest rate at which the full alloying capacity cannot be reached.

To examine this, consider Figure 1.5. For the first 10 cycles, the SiNW were cycled at 1C and the alloying capacity remained stable at 2400 mAh/g. When the rate was increased to 2C for cycle 11 to cycle 33, the set capacity could not be achieved in the allowed time and the alloying capacity decreased very quickly as cycle number increased. To get back to stable cycling, the rate was decreased to 1.5C. After a few cycles at 1.5C, the alloying capacity climbed back to 2400 mAh/g and remained stable at that value. A similar trend was seen when the rate was raised to 1.8C. When the rate was increased to 1.8C from cycle 48 to cycle 96, the alloying capacity dropped but then climbed back up to 2400 mAh/g, indicating that the sample could cycle stably at 1.8C. We thus put the max rate limit for this sample between 1.8C and 2.0C.

Figure 1.5 Rate Capabilities of bare SiNW



When SiNW were dipped in concentrated HNO_3 for 30 seconds, the rate capability and cycle life of the wires were improved. We expect this treatment to produce a silica coating about 0.75 nm thick on the surface of the porous Si wires.

Figure 1.6a shows the alloying and dealloying capacity during galvanostatic cycling of a 20 μm SiNW sample with a thin SiO_2 layer, grown by dipping the sample in acid for 30 seconds, cycled at rates below 2.4 C. The sample maintained a capacity of 2400 mAh/g for 398 cycles before the dealloying capacity faded. We thus record 398 as the cycle life for our wires. Figure 1.6a also shows the coulomb efficiency for this sample. The initial coulomb efficiency was 56%. The coulomb efficiency jumped up to 78% for cycle 2 and slowly climbed up to 99%.

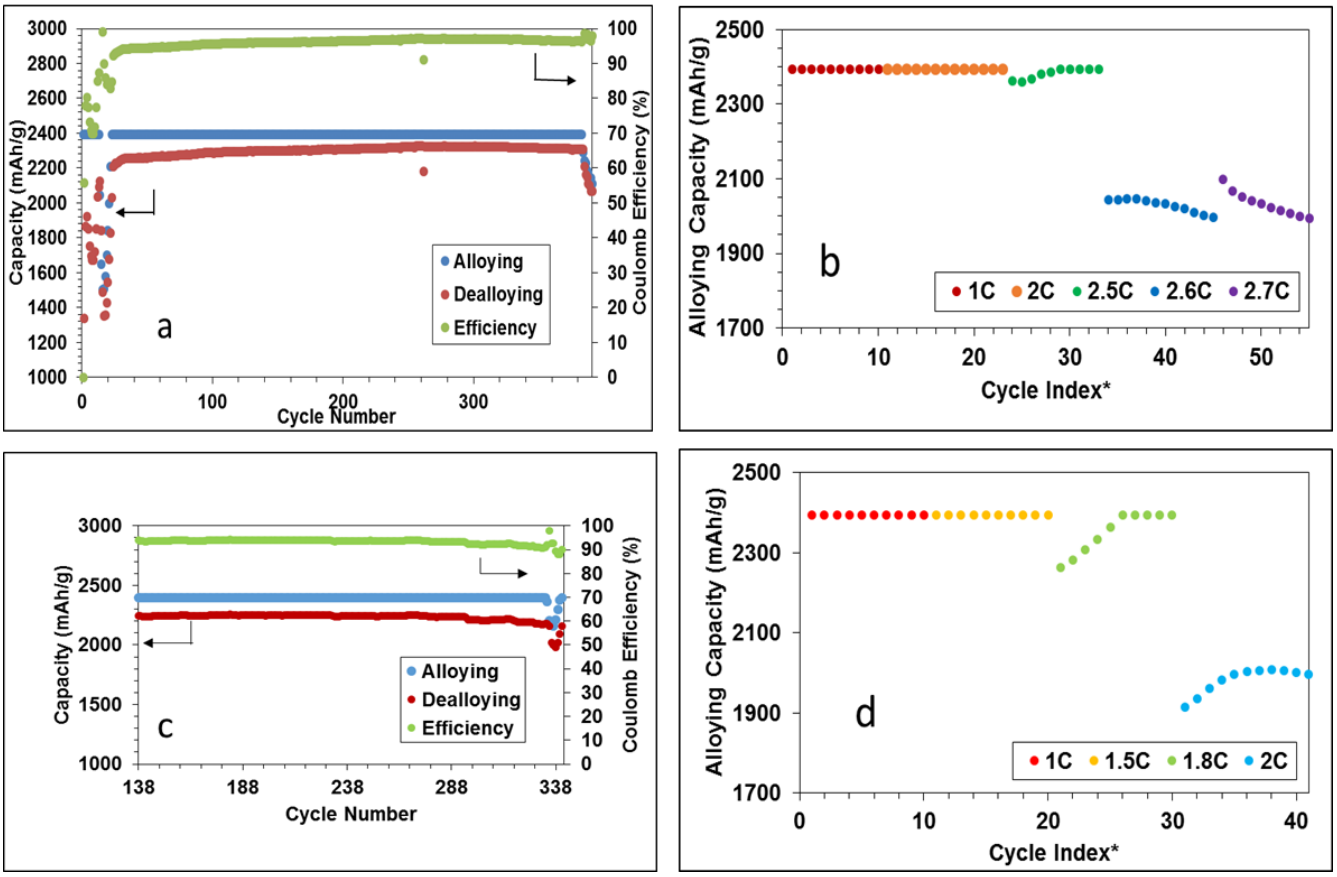
Figure 1.6b shows the rate capability of our SiNW with a thin silica layer. At 2.6C and higher C rates, the set alloying capacity could not be achieved, but at 2.4C and 2.5C, stable

cycling at 2400 mAh/g was achieved.

When SiNW were dipped in concentrated HNO_3 for 26 hours, we expect to produce a silica layer ~1 nm thick. Under these conditions, neither the rate capability nor the cycle life showed improvement. Figure 1.6c shows the alloying and dealloying capacity during galvanostatic cycling of a 20 μm SiNW sample with this thicker SiO_2 layer, grown by dipping the sample in acid for 26 hours. When cycled at 1.8C, this sample maintained a capacity of 2400 mAh/g for over 200 cycles before the dealloying capacity faded. This sample was also cycled for another 138 cycles at a range of rates. As a result, this sample showed cycle life above 300 cycles, which is in the range that is typical for these porous nanowire samples. Figure 1.6c also shows the coulomb efficiency for this sample. The initial coulomb efficiency was just 31%, but the coulomb efficiency slowly climbed up to 94%. This maximum value is significantly lower than that obtained for other samples.

Like the capacity, the rate capability is also not improved by the thick silica coating. Figure 1.6d shows that at 2C, the sample could not maintain the set alloying capacity, but at 1.8C the set capacity of 2400 mAh/g could be achieved. Thus, it appears that a thick silica coating negates all the rate advantages observed in the thin silica and results in performance very similar to uncoated wires. In other words, a thick polymer SEI layer provides similar kinetic limitations to a silica layer that is too thick.

Figure 1.6 Cycling data for silica-coated SiNW. a) Alloying Capacity, Dealloying Capacity, and Coulomb Efficiency versus Cycle Number for a SiNW sample dipped in HNO_3 for 30 seconds and cycled at rates below the max rate, b) Rate capabilities for SiNW sample dipped in HNO_3 for 30 seconds, *The cycling data was not necessarily collected chronologically in the order presented. c) Alloying Capacity, Dealloying Capacity, and Coulomb Efficiency versus Cycle Number for this 26 hour sample cycled at 1.8C. Before cycle 138, this sample was cycled at a range of rates between 1C and 2.5C. d) Rate capabilities for SiNW sample dipped in HNO_3 for 26 hours, *The cycling data was not necessarily collected chronologically in the order presented.



When SiNW were coated with 10 nm thick LASO, the rate capability of the wires was improved compared to that of bare SiNW. As indicated in figure 1.7a, at 5.6C and higher C rates, the set capacity of 2300 mAh/g could not be achieved, but at 5.5C, 2300 mAh/g was achieved.

Figure 1.7b shows the alloying and dealloying capacity during galvanostatic cycling of a 20 μm SiNW sample with a LASO layer. When cycled at rates between 1C and 5.5 C, this sample maintained a capacity of 2300 mAh/g for 176 cycles before the dealloying capacity

faded.

Figure 1.7b also shows the coulomb efficiency for this sample. In contrast to other samples where significant SEI formation was needed, the initial coulomb efficiency was 92% and this value reached a maximum of 99%. After cycle 77, where the max rate was first exceeded, the coulomb efficiency decreases noticeably, possibly indicating the LASO coating was damaged.

Figure 1.7 Cycling data for LASO-coated SiNW. a) Rate capabilities for LASO-coated sample, *The cycling data was not necessarily collected chronologically in the order presented. b) Alloying Capacity, Dealloying Capacity, and Coulomb Efficiency versus Cycle Number for this LASO-coated sample cycled at a range of rates between 1C and 5.8C. The purple asterisk (*) indicates cycle 77, where the max rate (5.5C) was first exceeded. There are breaks (//) in the Cycle Number axis where the sample did not cycle stably.

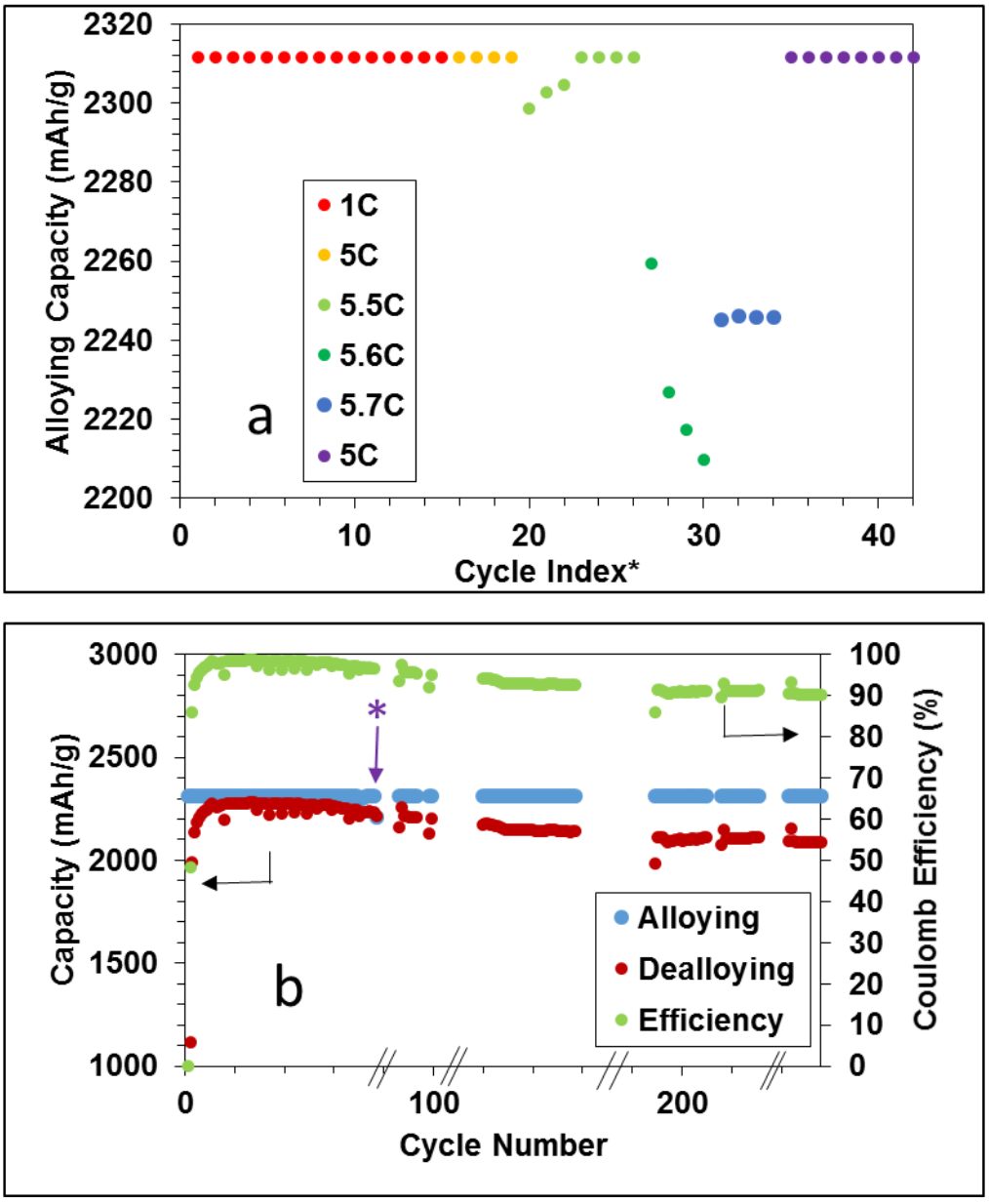


Table 1 compares the max C-rate, initial coulomb efficiency, max coulomb efficiency, and cycle life of bare, thin SiO_2, thicker SiO_2, and LASO-coated SiNW samples. Growing a thin

SiO_2 layer on our SiNW improves both the rate capability and cycle life of the sample. Growing a thicker oxide layer doesn't seem to improve the rate capability or the cycle life. A thicker oxide layer also seems to decrease the coulomb efficiency of the sample. This is consistent with other studies which indicate that when the oxide layer gets too thick, it hurts cycling performance. These studies indicate that a thin oxide layer may improve cycling performance by constraining the volume expansion and possibly limiting the extent of lithiation.[3,27,32] By contrast, coating with wires with a lithium ion conductor significantly improves the rate capability, presumably because the LASO coating prevents build-up of a thick SEI layer, and the LASO coating is a better ion conductor than either the polymeric SEI layer or the thin amorphous silica layer.

Also consistent with these studies was the effect of oxide layers on initial coulomb efficiency.[3,27] Comparing the bare SiNW with the oxide-coated NW, one can see that as the SiO_2 layer gets thicker, the initial coulomb efficiency decreases. In addition to improving the rate capability and cycle life of SiNW, LASO coating also increases the initial coulomb efficiency. Assuming a growing coulomb efficiency can be correlated with a growing SEI layer, a near unity initial coulomb efficiency for LASO-coated SiNW is a good indication that the LASO coating is acting as an artificial SEI layer.

Table 1.1 Summary of galvanostatic cycling studies of bare, thin silica, thick silica, and LASO-coated SiNW samples.

Sample	Max C-Rate	Initial CE (%)	Max CE (%)	Cycle Life
Bare	**1.8**	**74**	**99**	**292**
Thin Silica	**2.5**	**56**	**99**	**398**
Thick Silica	**1.8**	**31**	**94**	**338**
LASO	**5.5**	**92**	**99**	**260**

1.4 Conclusion

These results indicate that all-Si porous nanowire array show exciting potential as stable, high capacity anodes. Comparing specifically the max rate, max coulomb efficiency, and cycle life, the results show that SiNW with a thin SiO_2 layer and SiNW with a LASO coating cycle better than bare SiNW. Limiting the capacity to 2400 mAh/g, SiNW with a thin SiO_2 layer had the longest cycle life of our samples with nearly 400 cycles at a capacity of 2400 mAh/g. LASO-coated SiNW had the highest rate capabilities of our samples, cycling stably at 5.5C. Overall, using capacity-limited cycling to minimize the alloying of the Si substrate, we are able to cycle our SiNW arrays at around 200 to 400 cycles at rates above 1C. Stable cycling of our all-Si system indicates exciting potential on-chip energy storage applications.

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