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Engineer Nanocrystal Floating Gate Memory Scaling

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Jingjian Ren

December 2012

Dissertation Committee:

Dr. Jianlin Liu, Chairperson
Dr. Roger K. Lake
Dr. Sheldon Tan

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2012

This Dissertation of Jingjian Ren is approved:

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Committee Chairperson

University of California Riverside

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I would like to give my special thanks to my beloved parents for supporting me and encouraging me with their unconditional love. They are always there for me whenever I need them. I would also like to thank all my friends for who you are to me.

This thesis is dedicated to my parents,

to those who love me and those who I love.

ABSTRACT OF THE DISSERTATION

Engineer Nanocrystal Floating Gate Memory Scaling

by

Jingjian Ren

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, December 2012
Dr. Jianlin Liu, Chairperson

Flash memory is the dominant nonvolatile memory technology that has been experiencing fastest market growth driven by the booming of portable electronic devices. Since its invention in 1980s, it has been through aggressive scaling. Leading semiconductor memory manufacturers such as Samsung, Intel/Micron and SanDisk/Toshiba have unveiled their 19/20nm NAND flash technology in production. However, how long the fast scaling pace of flash can be maintained remains a question mark since this device using continuous polycrystalline Si floating gate faces increasing challenge brought by poor immunity to charge leakage and process difficulty due to large vertical gate stack dimension. To enable the further scaling of flash technology, change needs to be made at the cell level. Devices using discrete charge storage units have been recognized as potential alternatives to conventional flash cells, including charge trapping type device and nanocrystal floating gate device.

Nanocrystal floating gate memory is considered a promising future nonvolatile memory candidate because of its immunity to weak-point leakage in tunnel oxide and thus its superior scalability in terms of tunnel oxide thickness and power consumption. However, no scaling is easy. Problem of nano-dot density fluctuation has arisen for this type of device as scaling process proceeds. The increasing sensitivity of chip-level device performance to dot distribution in scaled cells requires that nanocrystal deposition, which is the key step for device fabrication, should be fully understood, and that this device should start evolving to incorporate material and structure innovations. This work is devoted to propelling the scaling process of nanocrystal memory through nanocrystal deposition behavior investigation and device structure engineering. In chapter 2, Si nanocrystal growth on patterned oxide substrate by chemical vapor deposition is studied both experimentally and theoretically and directed self-assembly behavior of Si nanocrystals is identified as due to the effect of substrate morphology. This deepens our understanding on nanocrystal nucleation and growth and provides a general guidance to deposition process for memory applications. Chapter 3 includes the work on a gate stack-engineered nanocrystal MOS capacitor memory device. An Al_2O_3-SiO_2 double-barrier structure is utilized for dielectric layers and process-induced oxide degradation issue is well solved, resulting in improved memory performance. Chapter 4 and chapter 5 focus on the demonstration of non-planarity concept for nanocrystal memory device. Non-planar

nanocrystal memories with multiple and single triangular-shaped Si nanowire channel are introduced. This new concept of nanocrystal memory device is aimed at alleviating dot density variation issue at the scaled technology nodes and helps extend the scaling limit of planar device.

Based on all the theoretical and experimental work in this dissertation, it is concluded that nanocrystal memory scaling lies in good understanding and control of the key process as well as continued cell architecture engineering. This work serves as a step toward the scaling limit of nanocrystal floating gate device for next generation nonvolatile memory development.

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Chapter 1 Introduction

1.1 Semiconductor memory

Semiconductor memory is one of the dominant memory technologies in people's daily life today and plays a key role in information storage. It is everywhere from personal computers, global positioning systems, automotives to portable consumer electronics such as cellular phones, digital cameras and tablets. Its applications embrace a variety of computer memories and portable storage devices for massive data storage, system code storage and other embedded solutions.

There are many ways to classify semiconductor memory based on the technology variety and the applications. As shown in Fig. 1.1, in general, it can be categorized as volatile type and nonvolatile type. The word "volatile" here refers to the fact that the stored information cannot be maintained when the power supply is cut off. In contrast, nonvolatile memory is able to keep the memory states information even when the power is turned off due to particular memory cell configuration and information storage mechanism.

Among volatile memories are SRAM (Static Random Access Memory) and DRAM (Dynamic Random Access Memory). SRAM offers the fastest write/erase speed among all memories. However, a single SRAM cell consists of 6 transistors, resulting in poor chip density, although 4-transistor SRAM cell has been developed. DRAM consists of one transistor and one capacitor. It is superior to SRAM in terms of its smaller cell size (lower cost per bit) and lower power consumption. But the writing speed is slower in the DRAM than in the SRAM. In addition, DRAM cell needs refreshing frequently to maintain its data, so from this point of view, the power

consumption is significant. As far as scaling is concerned, the size of a DRAM cell is large and scaling the DRAM cell size down would be difficult due to the large capacitor required to store data.

Nonvolatile memory is attracting tremendous interest today because of the booming market of portable electronics. Since the very first mask-programmed ROM (Read Only Memory), it has been experiencing significant evolvement from PROM (Programmable Read Only Memory), EPROM (Erasable Programmable Read Only Memory), EEPROM (Electrically Erasable Programmable Read Only Memory) to flash memory [1], with flash memory being the most prevailing technology nowadays. During the past several decades, the family of nonvolatile memory has expanded greatly. Not only have the density, speed, power consumption and cost been improved to an unprecedented level [2, 3], but more emerging memory technologies have gotten on the stage of semiconductor industry. Table 1.1 appeared in the latest update of 2011 International Technology Roadmap for Semiconductors (ITRS) [4]. It provides an overall evaluation and comparison among prototypical and emerging research memory candidates in terms of several most important industrial criteria such as scalability, multi-level cell (MLC), 3D integration, fabrication cost and endurance. The most intriguing prototypical devices demonstrated by leading semiconductor memory companies are FeRAM (Ferroelectric RAM), STT-MRAM (spin-torque transfer magnetic RAM) and PCRAM (Phase change RAM), some of which have already been patented and even utilized in hybrid products. Other emerging memories include Redox memory, which relies on cation/anion migration and reduction/oxidation reaction to realize bistable states (e.g. resistive memory with transition metal oxide), Mott memory based on Mott insulator, nanomechanical

memory with electrically controlled mechanical switch and molecular memory employing polymer molecules for high-density storage. Among all the new technologies, while some of the candidates do show very promising performance either as prototype device (i.e. PCRAM) or in research level (i.e. Redox memory), limitations within each type of memory are also becoming more realized and there yet remains a long way to go for these innovative technologies to be mature enough for the real market.

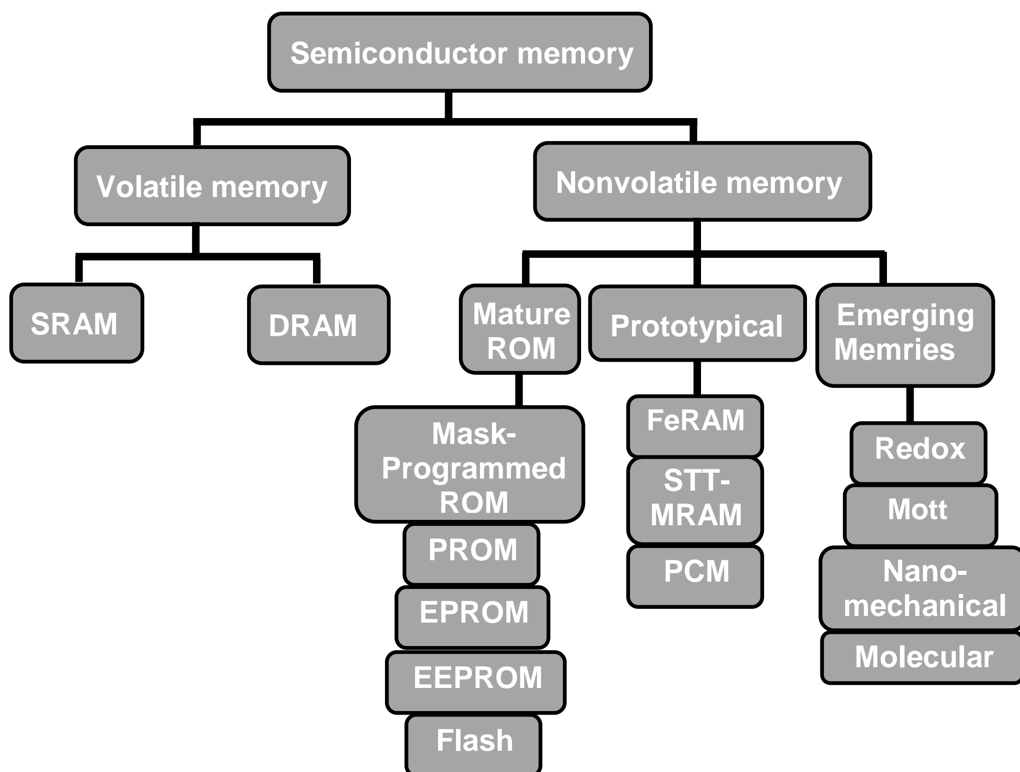

Fig. 1.1 Classification of semiconductor memory.

Within the scope of this research, scalability is the focus and the comparison of nonvolatile memory cell elements needs to be made in order to give a clear picture of this memory group. The components of one cell for each type are shown in Table 1.2 [4]. While most of the candidates require at least one transistor and one diode/resistor as well as new materials for the cell, flash memory provides supremacy in scalability through its simplified one-transistor cell structure and robust feasibility on present CMOS platform by its Si-based process. These have been the dominating features that make flash technology unmatchable and irreplaceable in the current nonvolatile memory market.

Table 1.1 Potential of Current Prototypical and Emerging Research Memory Candidates from 2011 ITRS update

	Prototypical (Table ERD3)			*Emerging (Table ERD5)*					
Parameter	**FeRAM**	**STT-MRAM**	**PCRAM**	**Emerging ferroelectric**	**Nanomechanical memory**	**Redox memory**	**Mott Memory**	**Macromolecular memory**	**Molecular Memory**
Scalability	red	yellow	green	yellow	red	green	?	?	green
MLC	red	red	green	red	red	green	?	yellow	red
3D integration	red	yellow	green	red	red	yellow	?	green	red
Fabrication cost	yellow	yellow	green	yellow	red	yellow	?	green	?
Endurance	green	green	yellow	green	red	green	yellow	red	?

	Parameter	Criterion
red	Scalability	F_{min} >45 nm
	MLC	difficult
	3D integration	difficult
	Fabrication cost	high
	Endurance	≤1E5 write cycles demonstrated
yellow	Scalability	F_{min}=10-45 nm
	MLC	feasible
	3D integration	feasible
	Fabrication cost	medium
	Endurance	≤1E10 write cycles demonstrated
green	Scalability	F_{min} <10 nm
	MLC	solutions anticipated
	3D integration	difficult
	Fabrication cost	potentially low
	Endurance	>1E10 write cycles demonstrated

Table 1.2 Cell elements of nonvolatile memories

Memory	*Flash*	*FeRAM*	*MRAM*	*PCRAM*	*Redox*	*Mott*	*Nanomechanical*	*Molecular*
Cell elements	**1T**	**1T1C**	**1(2)T1R**	**1T(D)1R**	**1T1R or 1D1R**	**1T1R or 1D1R**	**1T1R or 1D1R**	**1T1R or 1D1R**

Up to date, both academia and industry have been making every effort to explore maximum possibilities out of each device, trying to bypass those technical and practical constraints and implement those claimed advantages so as to replace all or most of the existing technologies and provide a Universal Semiconductor Memory (USM). The quest for such a USM device has long been an objective for the memory communities and a huge amount of revenue is invested by those semiconductor giants. It can be expected that the reward for achieving such a device would be extremely abundant, gaining an enormous market share from computer applications to consumer electronic products in this highly competitive global memory business.

1.2 Flash memory

1.2.1 Cell structure and working principle

Flash memory was invented by Dr. Fujio Masuoka at Toshiba in 1980. Over the decades it has been recognized as the most successful nonvolatile memory technology for both massive storage and embedded applications. The 1T cell structure enables ultra-high density integration, which is further enhanced by its MLC

capability. Furthermore, the device fabrication process compatibility with current CMOS process is what brings this technology into real application. Fig. 1.2 shows a typical cell of flash memory. Similar to a metal-oxide-semiconductor field effect transistor (MOSFET), flash cell consists of a control gate, oxide and Si substrate, with the exception that a poly-Si floating gate layer is inserted into the oxide layer as the charge storage unit. The insertion of floating gate just requires few additional masks and minor modification of the current MOSFET process flow. Consequently, it becomes an economic and practical way to fulfill this type of memory cell and array based on the already well-developed semiconductor process platform.

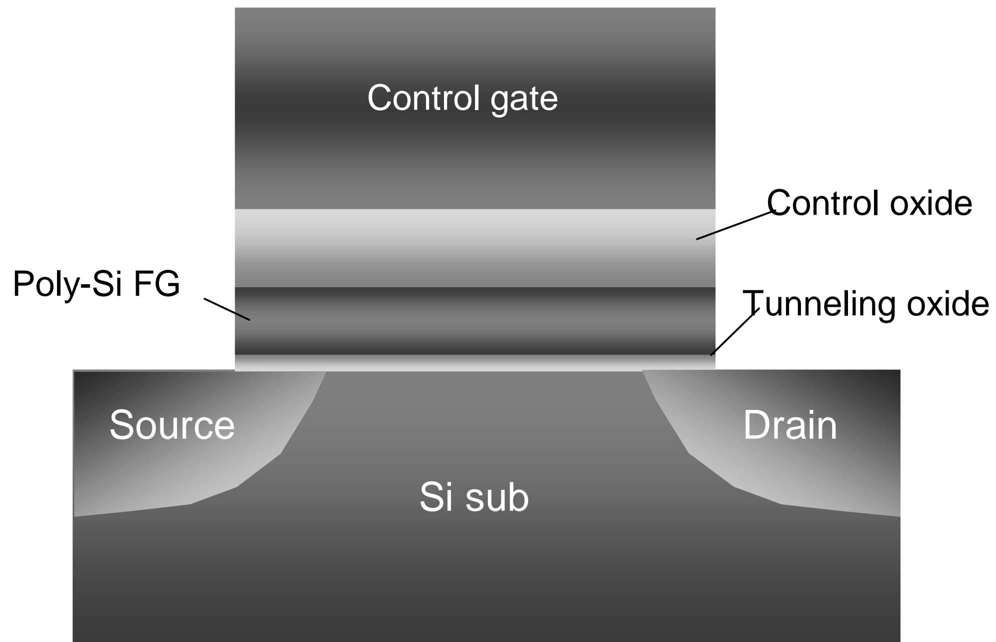

Fig. 1.2 A typical flash memory cell.

Fig 1.3 shows how flash memory works by sensing the threshold voltage shift (ΔV_T) induced by charge injection in the floating gate. The floating gate is sandwiched between two layers of oxide, namely, control oxide and tunneling oxide which serve as barriers for holding the charge injected from substrate. The stored charge imposes extra electric field on the channel, leading to ΔV_T shown by drain current-gate voltage (I_{ds}-V_{gs}) curves at neutral, programmed and erased states. The programmed and erased states are defined as logic "0" and "1" as bistable states of this memory, usually read from I_{ds} at fixed V_{gs}. ΔV_T is determined by the charge stored in the floating gate and also related to the capacitance of control oxide as: $\Delta V_T = Q/C_{control}$.

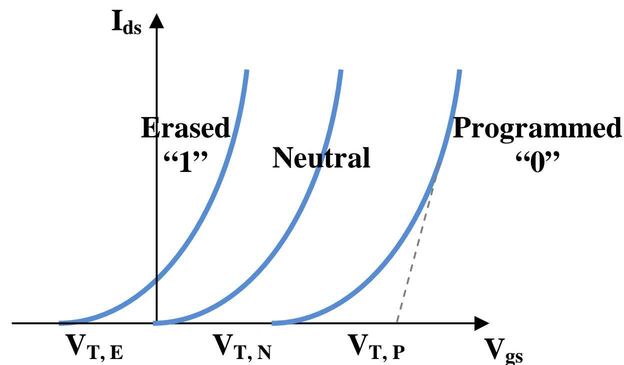

Fig. 1.3 I_{ds}-V_{gs} characteristics and V_T shift of n-type flash memory at neutral, programmed and erased states.

1.2.2 NAND vs. NOR

Based on how cells are organized as arrays, flash memory in production today can be divided into two dominant variants: NAND flash, in which cells are connected in series as a chain and packed with higher density for data-block storage; common

ground NOR flash, which consists of parallel-connected cells and is suited for high-speed read and code storage applications. The architectures of NAND and NOR array are shown in Fig. 1.4. The organization of NAND array allows the elimination of all the contact holes between wordlines (WLs) and thus reduces the occupied area by 40% compared to NOR array [5]. This is the reason the scaling of NAND flash is always ahead of NOR flash in reality.

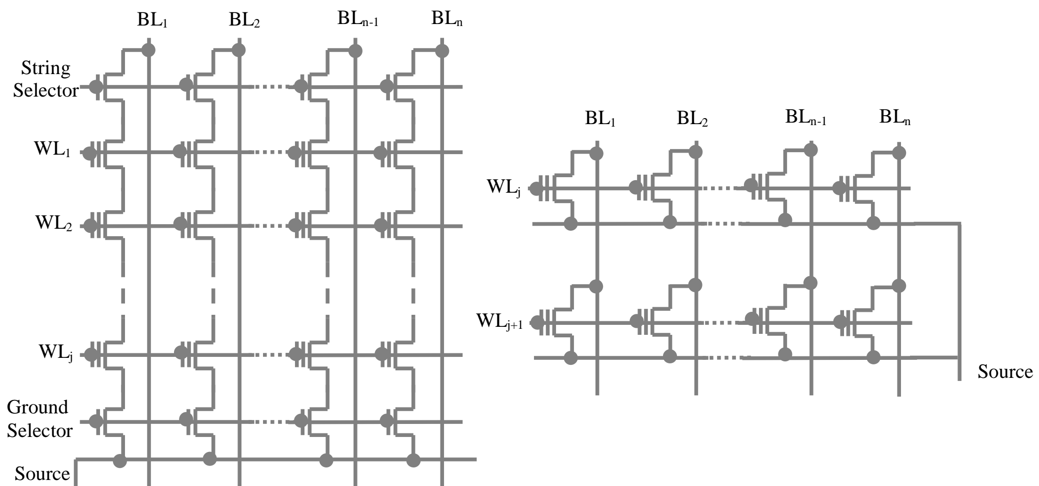

Fig. 1.4 NAND and NOR array architecture.

1.2.3 Limitations and alternatives

Charge-based nonvolatile memories require a media to hold charge for long-term storage. Hence it is critical that the media should be reliable enough and should also be small in geometries for the perspective of scaling. Conventional flash memory employs a continuous polycrystalline Si film as the floating gate for charge storage. As oxide layer gets thinner with scaling of cell dimensions both horizontally and vertically, the immunity of charge storage in poly-Si floating gate to oxide-defect

induced leakage path gets much poorer. This is primarily due to the continuous nature of the floating gate that allows charge to move freely in the film. Hence, a local leakage path (e.g. caused by stress) can drain all the stored charge. Flash device scaling, including dimension and power consumption scaling, is seriously limited by this fact and alternatives to this continuous floating gate needs to be developed to mitigate the issue. Memory cells with discrete charge storage units instead of continuous floating gate were proposed, among which are charge-trapping memory and nanocrystal floating gate memory, as illustrated in Fig. 1.5 by the dashed lines. Charge trapping memory technology was first conceptualized through the invention of the metal-nitride-oxide-semiconductor (MNOS) transistor by H. A. R. Wegener in 1967 [6] and then was developed into silicon-oxide-nitride-oxide-silicon (SONOS). This type of memory utilizes the traps in nitride layer to store charge, alleviating the problem in conventional flash up to a point. Nonetheless, the randomness of traps in nitride becomes the drawback when it comes to the controllability of charge storage. The other type of alternative with discrete charge storage nodes is nanocrystal floating gate memory, which is discussed in detail in the next part.

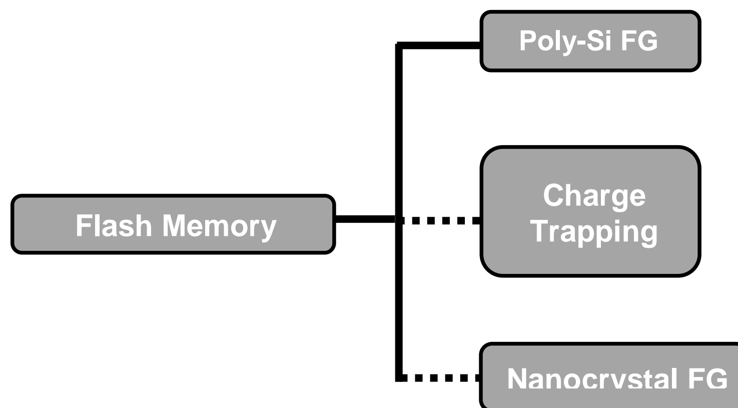

Fig. 1.5 Alternatives to poly-Si floating gate memory.

1.3 Nanocrystal floating gate memory

1.3.1 Basic device concepts

To substitute for continuous poly-Si floating gate, it was proposed that discrete nanocrystals (NCs) could be used as charge storage layer [7], as shown in Fig. 1.6. When control gate is biased, charges tunnel through the thin oxide layer and get trapped in the NCs. In this case, charges are confined within NCs of around several nanometers in size and cannot move horizontally. The amount of charge that NCs can hold is determined by density of states in the NCs as well as coulomb blockade effect [8].

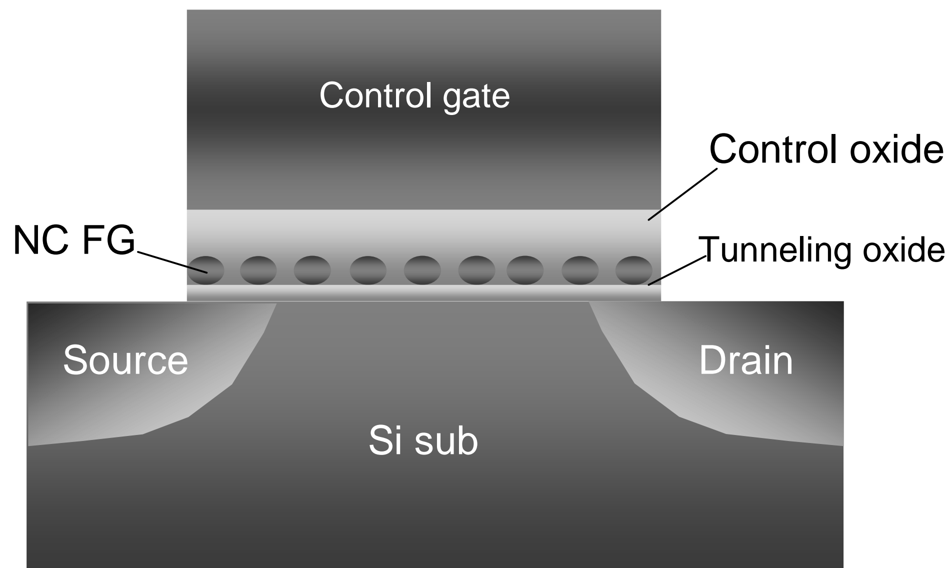

Fig. 1.6 Nanocrsytal floating gate memory cell.

As is mentioned in previous section, the immunity of charge storage to tunnel oxide leakage is severely limited by the continuous nature of poly-Si floating gate in conventional flash memory, which also puts constraints on scalability of the device. In

contrast, as shown in Fig. 1.7, localized oxide leakage path caused by process defects or stress may drain the charge kept in single NC that is touching the defects while other NCs in the same cell can still maintain the charge for cell state assurance. In this way, prolonged retention performance can be expected and thinner tunneling oxide can be adopted for this structure, leading to improved scalability and reduced power consumption. Furthermore, compared to charge-trapping type memory, it is feasible to control the ordering of charge storage sites by various NC deposition techniques, enabling further cell size scaling and enhancing reliability of the MLC features.

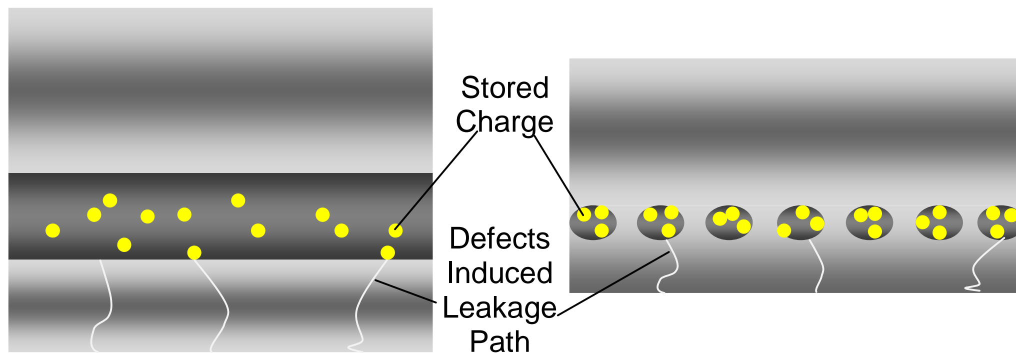

Fig. 1.7 Comparison of immunity to leakage between conventional flash cell and NC memory cell.

1.3.2 Current status

Si NC floating gate memory has been heavily explored not only in academic research but also for real-market applications by semiconductor companies. Freescale (formerly Motorola Semiconductor) successfully pioneered the use of nanocrystals in memory devices in March 2003, and discussed the demonstration of its first-of-its-

kind 4-Mbit nanocrystal memory device at the December 2003 IEEE International Electron Devices Meeting (IEDM) [9]. Later on in 2005, it started manufacturing 24-Mbit memory array based on Si NCs using their 90 nm CMOS bulk technology, aimed at automotive market [10]. Continued efforts have been invested for scaling this technology down to 65nm and further.

In the meantime, people are seeking to improve this device through various NC deposition techniques and NC material/structure engineering. NC deposition techniques such as low pressure chemical vapor deposition (LPCVD) [9, 11], molecular beam epitaxy (MBE) [12], ion implantation and subsequent high-temperature annealing [13] have been extended to the synthesis of NC floating gate. Memory devices with high nanocrystal density and good performance have been demonstrated based on these techniques. NCs of different materials such as Ge and other semiconductors [14], metal, metallic silicide and metal-like material [15-20], dielectrics [21, 22] have been adopted for device performance improvement, i.e. larger memory window, higher writing/erasing speed, longer retention and better cycling performance. Band structure engineering has also been conducted by novel NC structure development. For instance, Ge/Si hetero-nanocrystal structure was proposed for good retention while maintaining high writing/erasing efficiency [23]; Core-shell nanocrystals with metal core and high-k dielectric shell and double-layered NCs have been proven as excellent potential solutions to retention-programming/erasing trade-off [25, 26].

1.3.3 Perspective and challenges of scaling

Flash technology has been scaling aggressively. In particular, many companies dealing with NAND flash, including Samsung, Micron, Toshiba, have announced 20nm products by 2012. But if one takes a look at the 2D planar NAND flash technology requirements from ITRS 2011 updates (Table 1.3), scaling will not always be so optimistic. The slowing down pace of NAND flash scaling on cell size, tunnel oxide and inter-poly dielectric thickness and the rigorous requirements on device performance imply that this technology is also inevitably approaching the ultimate limit.

Table 1.3 2D planar NAND flash technology requirements

A. 2D Planar NAND Flash (Floating Gate (FG) or Charge Trapping (CT))								
year of production	*2011*	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*
Planar (2D) NAND Flash uncontacted poly 1/2 Pitch (nm)	22	20	18	17	15	14	13	12
Cell size – area factor a in multiples of F2 SLC/MLC [5]	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3	4.0/1.3
Tunnel oxide thickness (nm) [6]	6-7	6-7	6-7	6-7	6-7	5-6	5-6	5-6
Interpoly dielectric material [7]	ONO	ONO	ONO	ONO	ONO	ONO	High-K	High-K
Interpoly dielectric thickness (nm)	10-13	11	11	10	10	9	9	9
Gate coupling ratio (GCR) [8]	0.6	0.6	0.6	0.5-0.6	0.5-0.6	0.5-0.6	0.5-0.6	0.5-0.6
Control gate material [9]	n-poly	n-poly	n-poly	n-poly	n-poly/Metal	n-poly/Metal	Metal	Metal
Highest W/E voltage (V) [10]	17-19	15-17	15-17	15-17	15-17	15-17	15-17	15-17
Endurance (erase/write cycles) [11]	1.E+04	1.E+04	1.E+04	1.E+04	1.E+04	1.E+04	5.E+03	5.E+03
Nonvolatile data retention (years) [12]	10	10	10	10	10	10	10	10
Maximum number of bits per cell (MLC) [13]	3	3	3	3	3	3	3	3

A. 2D Planar NAND Flash (Floating Gate (FG) or Charge Trapping (CT))								
year of production	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*
Planar (2D) NAND Flash uncontacted poly 1/2 Pitch (nm)	11	10	9	8	8	8	8	8
Cell size – area factor a in multiples of F2 SLC/MLC [5]	4.0/1.3	4.0/1.3	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Tunnel oxide thickness (nm) [6]	5-6	5-6	5-6	5-6	5-6	5-6	5-6	5-6
Interpoly dielectric material [7]	High-K	High-K	High-K	High-K	High-K	High-K	High-K	High-K
Interpoly dielectric thickness (nm)	8	8	8	8	8	8	8	8
Gate coupling ratio (GCR) [8]	0.5-0.6	0.5-0.6	0.5-0.6	0.5-0.6	0.5-0.6	0.5-0.6	0.5-0.6	0.5-0.6
Control gate material [9]	Metal	Metal	Metal	Metal	Metal	Metal	Metal	Metal
Highest W/E voltage (V) [10]	15-17	15-17	15-17	15-17	15-17	15-17	15-17	15-17
Endurance (erase/write cycles) [11]	5.E+03	5.E+03	5.E+03	5.E+03	5.E+03	5.E+03	5.E+03	5.E+03
Nonvolatile data retention (years) [12]	10	10	10	10	10	10	10	10
Maximum number of bits per cell (MLC) [13]	3	3	4	4	4	4	4	4

3D non-planar technology is one of the viable ways to extend this technology to further nodes and is currently under intensive research, development and optimization. On the other hand, to explore the possibilities of NC memory as a replacement and realize the so-claimed superiorities of this device becomes more attractive.

In order for successful scaling of NC floating gate memory, the most critical part lies in obtaining NCs of high density and supreme uniformity. This can be intuitive. The device relies on NCs to store charge and fulfill its functionality. As miniaturization of device dimensions proceeds, the erasing/writing performance non-uniformity and variable memory windows of different devices on the same chip arise as an issue due to the increased sensitivity of performance to floating dot density variation. As a result, understanding towards NC growth behaviors needs to be furthered for better control over NC deposition techniques, Moreover, new materials and cell structures are a necessity for future technology nodes promotion.

1.4 Motivation of this research

The motivation of this research is to enhance the understanding on NC floating gate memory device from both material and cell point of view through theoretical and experimental efforts. It is also to investigate and demonstrate novel NC memory devices to assist the implementation of future flash candidates.

The main tasks of this research are summarized in Fig. 1.8:

1) To reveal underlying physical fundamentals of Si NCs deposition on patterned oxide substrate and cast light on robust NC layer synthesis. The effect of oxide

substrate morphology on NC self-assembly is investigated experimentally. Observation of strain-less directed self-assembly of Si NCs is addressed by building a simplified physical model and performing theoretical calculation.

2) NC layer engineering: metallic silicide NC deposition through varied deposition techniques and processes (i.e. LPCVD, gas source MBE) to achieve high density NC layer with supreme uniformity.

3) Memory cell architecture engineering: perform band structure engineering and introduce novel gate stack by using high-k material to form double-barrier structure for improved memory performance; demonstrate a proof-of-concept non-planar NC memory device by using triangular-shape Si nanowire array and single nanowire as channel for alleviating NC density fluctuation issue and extending NC memory scaling limit.

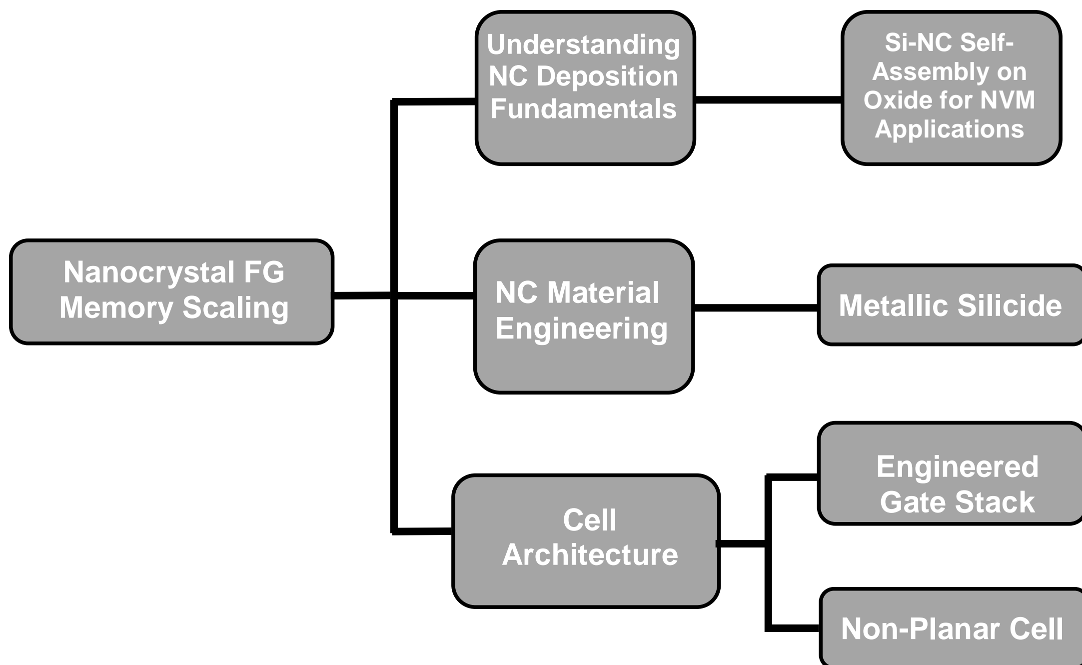

Fig. 1.8 Engineering NC floating gate memory scaling.

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Chapter 2 Strain-less Directed Self-assembly of Si Nanocrystals on Patterned SiO_2 Substrate

2.1 Introduction

As electronic devices scale down, it becomes more and more technically challenging to continue miniaturization of semiconductor nanostructures relying on lithography only. Alternatively, self-assembly is of significant interest to both academic research and industrial applications due to the potential of getting ordered nanostructures at ultra-scaled regime. Both experimental and theoretical efforts have been invested extensively into study of growth of group III-V and group IV quantum dots (QDs) or islands on single-crystalline substrates[1-5], aiming at exploring predictable and well-controlled QD growth with supreme spatial uniformity and understanding the underlying physical mechanism. Perfect self-alignment of Ge QDs on Si ridge [6-10], SiGe QDs on lithographically patterned Si substrate [11] and InAs QDs on GaAs plateau [12-13] were reported by many groups and different models were built to address the directed nucleation effect of strained islands [10-11, 14,15].

2.2 Motivation

Mediated by a substrate morphology induced strain relaxation mechanism, so far, most practices of directed self-assembly of islands have been towards strained islands on patterned substrates. However, unstrained islands growth on amorphous substrate such as SiO_2 is also of great importance because of modern electronic device demands.

Among many applications, one example is metal-oxide-semiconductor structure based nanocrystal floating gate memories [16], which require high-density ultra-uniform metallic or semiconductor NCs on oxide surface to circumvent device performance variability issue. Thus, identifying a growth mechanism that will lead to a "strain-less" directed self-assembly of NCs in V-W mode on oxide substrates is of both scientific interest and technological significance. One intriguing question is how NCs grow on patterned oxide substrate and whether the non-planar surface morphology can direct NCs self-assembly in the absence of strain.

In this work, we present our experimental observations of preferential nucleation and growth of Si NCs on patterned SiO_2 substrate, showing direct evidence of strain-less directed self-assembly. The growth condition dependence of this preferential growth effect is studied. A simple two-dimensional (2D) model is developed and calculation is performed in terms of the energetics associated with V-W island growth on the patterned substrate, to explain these interesting experimental findings.

2.3 Experiments

2.3.1 Substrate preparation

Substrates for Si NCs growth were prepared as shown in the process flow in Fig.2.1 (a). E-beam lithography was employed to pattern the resist on pre-cleaned p-type Si (100) substrates. Cr was evaporated in a high-vacuum e-beam evaporation system. This was followed by a lift-off process to form hard-mask as shown in the schematic for subsequent wet etching step. KOH anisotropic wet etching was

performed on the samples and well-defined quasi-triangular- and pit-shaped patterns were achieved. After organic contaminants and metal residue cleaning and native oxide removal, samples were immediately transferred into an oxide furnace for dry oxidation. 5nm thermal oxide on the surface of the pit-shaped substrates was formed

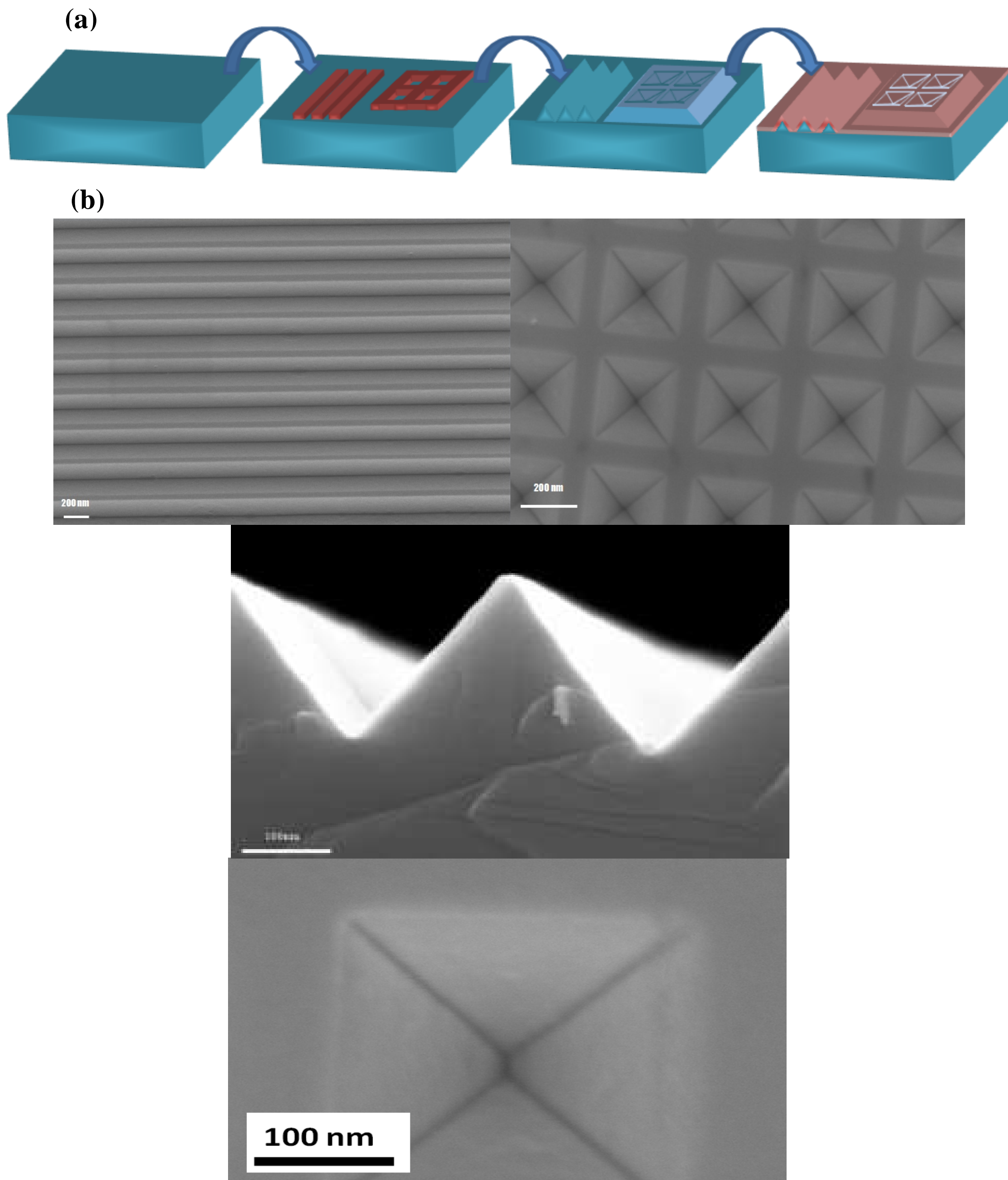

Fig. 2.1 (a) Process flow of substrate preparation; (b) SEM images of well-defined quasi-triangular- and pit-shaped patterns.

at 950°C with clean and flat surface. The large-area and magnified patterns are shown in the scanning electron microscopy (SEM) images in Fig.2.1 (b).

2.3.2 Si nanocrystal deposition

Chemical vapor Si NCs deposition technology has been explored and developed for NC memory applications and silicon crystallites with nanometer size can be reliably obtained by controlling the early stages of Si film growth [16-19]. In our experiments, Si NCs growth was performed on the patterned substrates in a low pressure chemical vapor deposition (LPCVD) system with split growth conditions. During the growth, SiH_4 was used as Si precursor and the flow rate was fixed at SiH_4:N_2=20sccm:100sccm and pressure at 0.5torr for all the samples. Growth temperature and growth time were chosen as the parameters to be tuned for condition split study of nucleation and growth behavior of NCs. Temperature is believed to be directly related to the energy gained by adatoms during growth, which is critical in determining the migration behavior and nucleation barrier. Different growth time shows the evolvement of Si dots nucleation and growth and allows one to see a clear picture of NC growth process during different stages.

2.3.2.1 Deposition temperature-dependent nucleation and growth behavior

Fig. 2.2 shows SEM images of temperature-dependent Si NCs nucleation and growth behavior on pit-shaped patterns. Samples were grown under six different temperatures from 650°C to 575°C with the same growth time of 8 sec. To monitor temperature effect on the early-stage nucleation and growth behavior of NCs, short

growth time was used and NCs with very small sizes were synthesized. Despite the tiny size of NCs (5-10nm), SEM was able to capture the morphology of NCs after growth and qualitatively show the segregation and NC density variation. From high temperature to low temperature, a clear trend of dot density and size decreasing is observed. Interestingly, while under higher temperatures of 650°C, 630°C and 615°C no obvious dot density variation between the wall (planar area) and the trench (concave area) is found, dot segregation in the trench is observed for lower-temperature samples at 600°C, 590°C and 575°C, with more NCs gathering in this concave part of the substrate than in other parts. This phenomenon is attributed to the preferential nucleation of NCs in the trench due to lower NC formation energy induced primarily by the substrate morphology. The fact of the enhanced stress of oxide substrate in this part making the chemical bonds here more reactive for nucleation also contributes to this effect [19, 20]. In the particular temperature range of 575°C-600°C, adatoms adsorbed to the sample surface move around and find most energy-favorable sites (the concave parts of the substrate) to settle down as nuclei for later NC growth. Afterwards, more adatoms segregate to the nuclei and NCs preferentially form in the trench.

Among the three temperatures, 590°C is the one under which the best preference occurs, with NCs selectively aligned along the trench and almost no dots found on other area outside the trench. This can be considered a consequence of the competition between adatoms surface migration and reaction with substrate atoms (nucleation). At lower temperature of 575°C, some NCs form on the planar surface due to insufficient energy gained by the adatoms at lower temperatures and the

limited migration. Similarly, for samples grown at temperatures below 575°C, although low NC formation energy locations (trenches) are available, the energy supplied to adatoms is not enough for them to overcome migration barrier and reach the energy-favorable sites. Therefore, no directed self assembly behavior was found. On the other hand, at higher temperature of 600°C, the nucleation and growth process is accelerated. Si NC deposition rate is so high that later-stage random nucleation starts covering the directed self-assembly effect at earlier stage. This is intuitive because as earlier-formed NCs fill in the trench, low-energy sites for nucleation are occupied and the effect of substrate morphology on the nucleation and growth of NCs becomes weaker and weaker. Preferential nucleation is then replaced by continuous

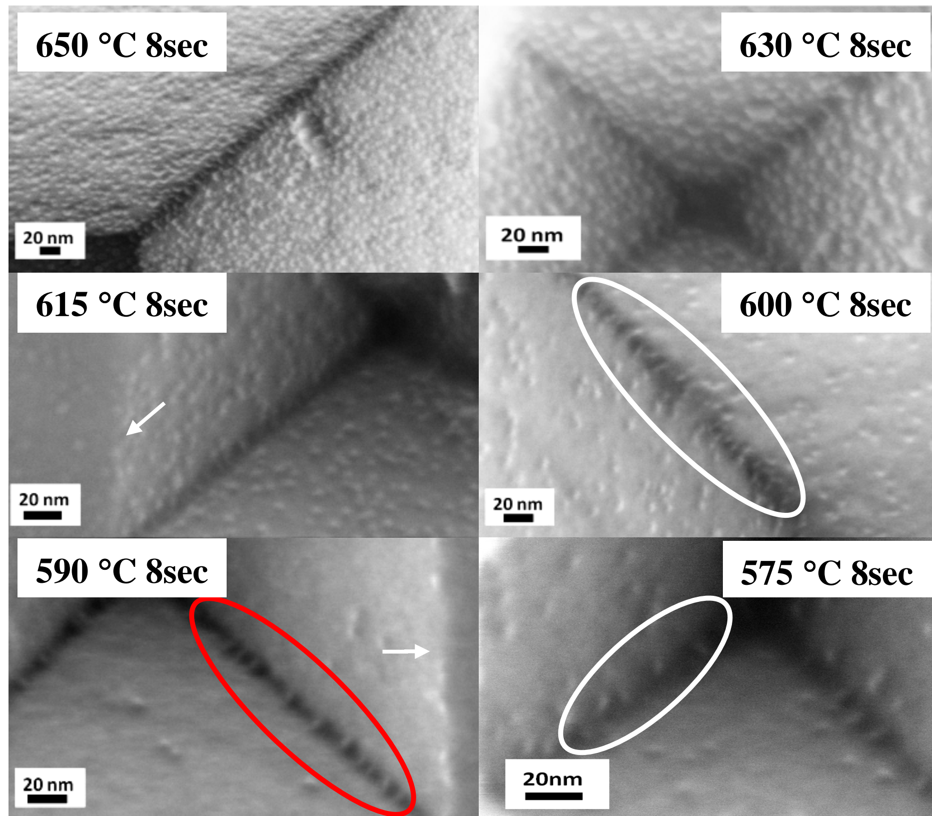

Fig. 2.2 SEM images of temperature-dependent Si NCs nucleation and growth.

random NCs deposition on the whole sample surface at later stage with no or a small limitation in the number of nucleation sites [21]. This situation is more pronounced for even higher temperatures, as mentioned above, where almost no sign of preference can be observed from the images. In fact, it is expected that even on samples where directed self-assembly is observed, with longer growth time this effect would eventually be covered by subsequent random NC formation. This is confirmed by the growth time-dependent growth experiments in this work.

It should also be mentioned that a series of NCs growth with split conditions was also carried out on substrate with quasi-triangular shaped patterns, with SEM images of selective samples shown in Fig. 2.3. Similar directed self-assembly was not observed at either convex parts (i.e. the intersection of (111) and (100) planes as marked by the white arrows) or planar parts of the substrates in our experiments.

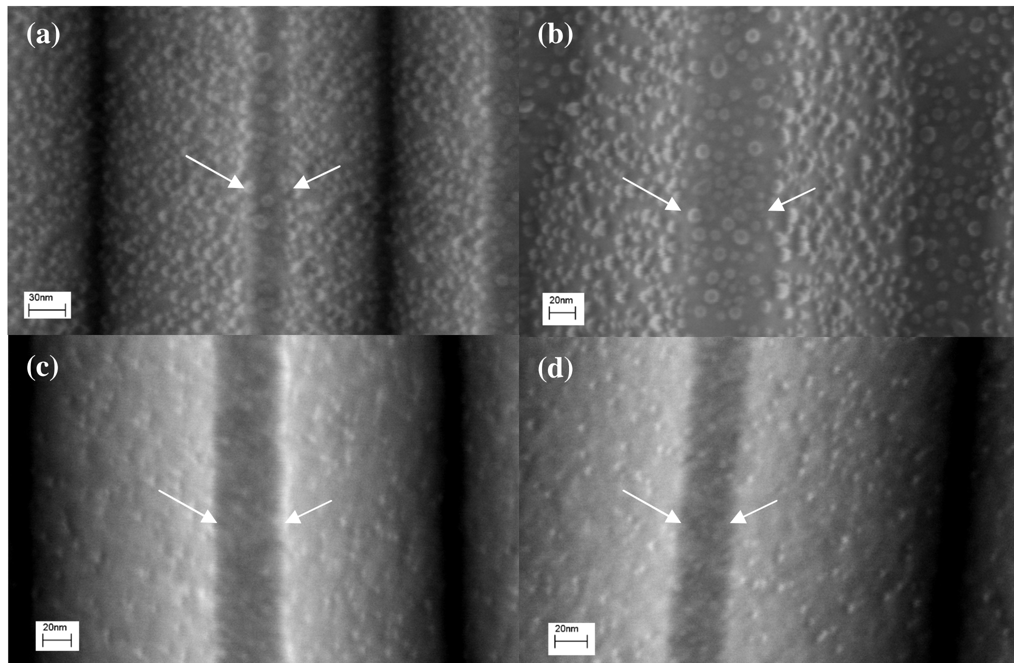

Fig. 2.3 SEM images of Si NC growth on quasi-triangular shaped patterns: (a) 650 ºC, 8sec; (b) 600 ºC, 30sec; (c) 600 ºC, 15sec; (d) 580 ºC, 60sec.

2.3.2.2 Deposition time-dependent nucleation and growth behavior

The growth time dependence of Si NCs deposition on patterned concave substrate surface is shown in Fig. 2.4. These SEM images present clear surface evolvement of NC samples with growth time at three temperatures (575°C, 590°C and 600°C). At the initial stage (with growth time of 8sec), three samples show different levels of directed self-assembly. As growth time increases, an increase of dot density and size is noticeable and directed NC formation is covered with dots showing up at locations other than the concave trench. In line with the discussion above, this is because of the occupation of energy-favorable nucleation sites by NCs that offsets the morphology-induced NC formation energy difference among concave, flat and convex areas.

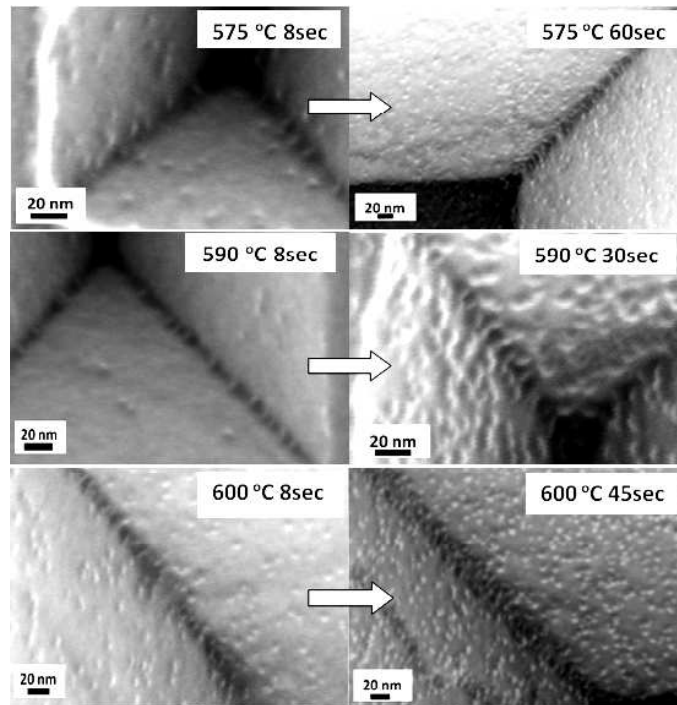

Fig. 2.4 SEM images of the growth time dependence of Si NCs growth on patterned substrate surface to show the evolvement of NC deposition process at different stages.

The growth condition splits for all the samples are summarized in Fig. 2.5, with X-axis standing for growth temperatures and Y-axis representing growth times. As highlighted in red, the temperature range of 575°C~600°C is found to be a temperature window allowing for observation of directed Si NC self-assembly on concave substrate surface, under the given experimental configurations. In other words, samples with oxide thickness of 5nm grown under pressure of 0.5torr and precursor flux of SiH_4:N_2=20sccm:100sccm show preferential nucleation behavior at these temperatures using growth duration of 8sec. This window could vary with oxide thickness, pressure and gas source flux. Note that although from an energy point of view, higher temperatures provide adatoms with higher energy to migrate on substrate and promote directed self-assembly, the whole nucleation and growth process occurs

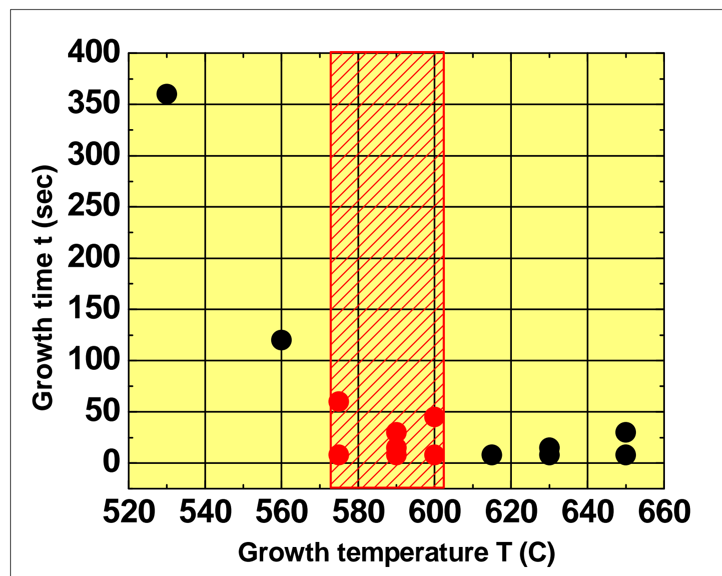

Fig. 2.5 Summary of growth condition splits and the temperature window for Si NCs preferential growth on concave oxide substrate surface with t_{ox}=5nm (temperature window: T =575°C~600°C; gas pressure P=0.5torr, gas flux= SiH_4 20sccm:N_2 100sccm)

much faster, leading to difficulty in capturing the effect of interest at earlier stage. Growth conditions need to be tuned carefully in order to reveal this behavior.

2.4 Modeling

Different from previously reported self-alignment of semiconductor islands (Ge on Si, InAs on GaAs, etc.), in this case of NC growth on amorphous substrate (e.g. Si NC on SiO_2), another growth mode, i.e. Volmer-Weber (V-W) mode, is involved, in which no wetting of the substrate happens and NC (3D island) nucleation and growth happen from the very beginning. To formulate the theory of NC nucleation on non-planar substrate in this mode, we first consider a 2D model of the NC-patterned substrate system. As shown in Fig. 2.6 (a), this model consists of saw tooth-shaped substrate (thin thermal SiO_2 layer on top of patterned Si substrate) and NCs with constant size (area). The shape of NC is assumed as surface-faceted for simplicity. Three different types of substrate surface morphology are configured, namely, planar, convex and concave, with substrate angle $\varphi=0$, $\varphi>0$, $\varphi<0$, respectively. θ denotes the surface angle of NC and $2l$ is the width of the NC covering the substrate. In this model surface and interface energy are considered to be dominant factors in determining NC nucleation and no strain relaxation energy term is introduced in the calculation [23-24]. In addition, since this growth mode normally involves material growth on foreign substrate, an interface energy term is included into the total surface energy change of the system. Consequently, the total NC formation energy can be written as:

$$E_{surf} = E_{surf-NC} + E_{int} - E_{surf-sub} = 2l\gamma_{NC}\left(\sec\theta + \frac{\gamma_{int} - \gamma_{sub}}{\gamma_{NC}}\sec\varphi\right)$$

$$= 2\gamma_{NC}\left(\sec\theta + \frac{\gamma_{int}-\gamma_{sub}}{\gamma_{NC}}\sec\varphi\right)S^{1/2}(\tan\theta - \tan\varphi)^{-1/2} \quad (1)$$

Where $E_{surf\text{-}NC}$ is the surface energy of the NC, E_{int} is the interface energy of the interface between the two materials, and $E_{surf\text{-}sub}$ is the surface energy of the substrate covered by NC; γ_{NC}, γ_{int}, γ_{sub} are the surface energy density of NC, interface and substrate, respectively; S is the NC area in 2D model.

From equation (1), it can be seen that for fixed S and θ, the total NC formation energy is a function of the non-dimensional system parameter $\gamma = (\gamma_{int}\text{-}\gamma_{sub})/\gamma_{NC}$, and substrate angle φ. To reveal how total NC formation energy varies with different substrate morphologies and γ, we examined the dependence of E_{surf} on φ and γ with θ fixed at 30° as an example, as shown in Fig. 2.6 (b). In general, the surface contact angle of QD (θ) can have a size dependence even in V-W mode due to edge effect as shown by previous theory [22] and experiments [21]. Here the value is chosen as a representative case just to show the overall trend of the effect of substrate morphology on NC nucleation behavior. γ is an intrinsic parameter related to the nature of the two materials in the system and in different growth modes it holds different value ranges. In V-W mode, $\gamma_{NC} + \gamma_{int} > \gamma_{sub}$ or $\gamma > -1$ is satisfied. Substrate angle φ is investigated within the range $-45° < \varphi \leq 28°$ to meet the restriction that $\varphi \leq \theta$. From the 3-D plot it should be noticed that E_{surf} increases with the value of γ, qualitatively indicating the fact that the larger this system parameter is, the higher NC formation energy is hence

the harder it is for NC to form. Under different γ, the changing trend of E_{surf} with φ varies. In most cases, E_{surf} decreases monotonously with φ decreasing from positive regime to negative regime, suggesting that lower NC formation energy is needed for negative substrate angle (concave) compared to zero (flat) and positive (convex) substrate angle.

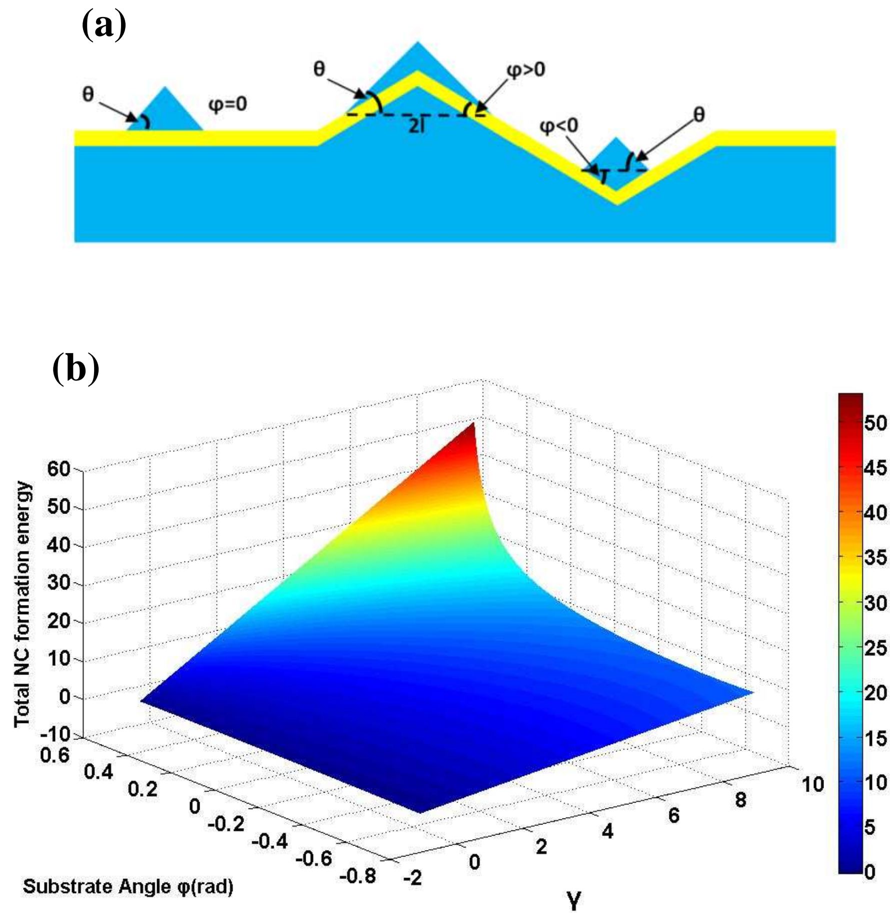

Fig. 2.6 (a) Two-dimensional model of NC-patterned oxide substrate system; (b) 3-D plot of total NC formation energy as a function of substrate angle φ and system parameter γ, with the unit of energy $2\,\gamma_{NC}\,S^{1/2}$.

To further address the experimental results observed and illustrate the morphology effect, E_{surf} as a function of γ is plotted for the three types of substrate angles for comparison. Fig. 2.7 (a) shows a schematic of the patterned substrate surface utilized in the experimental part to study NC growth behavior, with φ=-35.26° at the concave trench of the pit , φ=0 on the planar surface and φ=27.37° at the convex edge of the pit. It can be clearly seen from Fig. 2.7 (b) that within the whole range of variable γ, concave substrate requires lowest NC formation energy than that for the other two cases. This result implies that concave substrate always favors the nucleation and growth of NC in V-W mode, an effect regardless of what material system is involved (γ) and this is in very good consistency with the experimental findings above. While over a large range of γ lower energy is needed in flat case than that in convex case, the magnified region of the plots in the figure shows that in certain systems the situation could be reversed, indicating a dramatic dependence of NC formation energy on material natures and interface structures. There have been experimental reports showing NC self-alignment on convex oxide surface with very fine alignment condition window [25], a proof of more energy-favored nucleation sites on convex surface over flat surface in some systems. It is worth mentioning that the simplified 2D model developed here is aimed at semi-quantitatively describing and explaining the experimental findings, focusing on the directed self-assembly behavior observed on concave surface. The range of γ shown in Fig. 2.7 (b), (-1, 10), is chosen mainly for illustration of this concave surface effect. Although the specific value of γ could not be obtained due to the amorphous nature of thermal SiO_2 and the unknown interface atomic structure of Si-SiO_2, these calculation results provide direct

theoretical evidence to well support and address the experimental findings within the scope of this work.

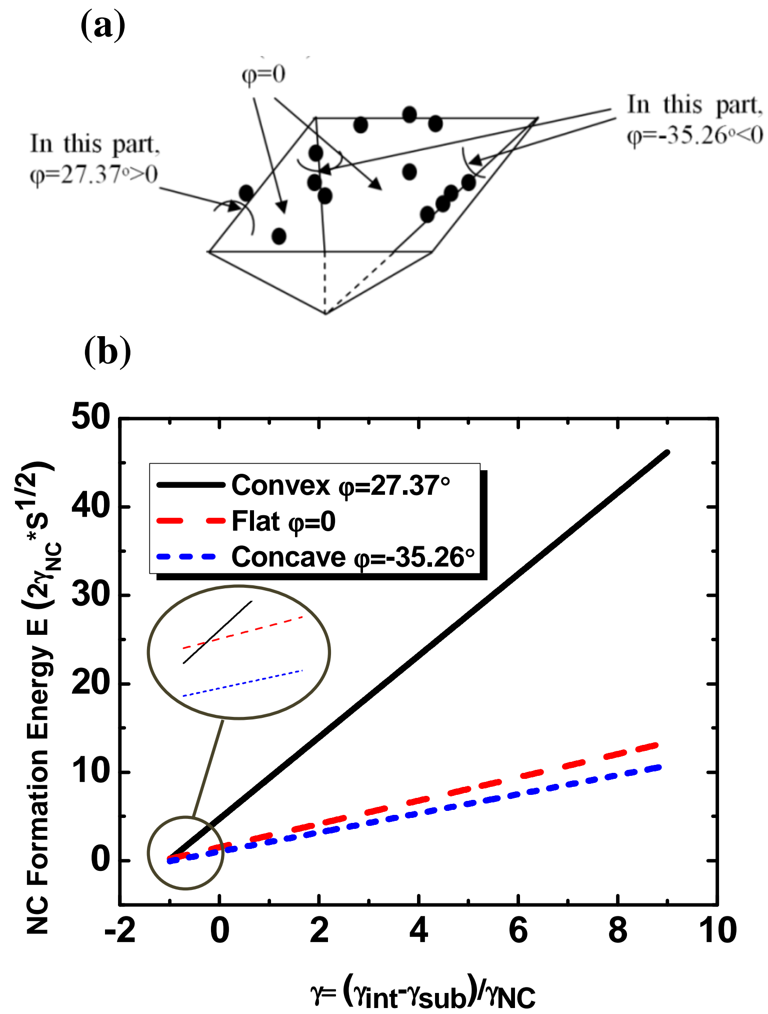

Fig. 2.7 (a) Schematic of the patterned substrate surface; (b) Calculated total NC formation energy for three different types of experimental surface morphologies.

Previous theory analysis [15] has shown that strain relaxation can favor nucleation of “strained” islands at the concave region on patterned substrates in Stranski-Krastanov (S-K) growth mode. In this study, we show that the competition between surface/interface energy without strain relaxation can also favor nucleation of “unstrained” NCs at the concave region on patterned substrates in V-W growth mode. It is also interesting to note that although the “unstrained” V-W islands have no misfit epitaxial strain, they may still experience stress effects due to surface stress discontinuity at island edges as shown before [22,26], an effect deserves further study.

2.5 Summary

Preferential growth behavior of Si NCs on patterned SiO_2 substrate is found within certain experimental condition window. Simple modeling and calculation were carried out to depict the possible dominant mechanism underlying the experimental results. Different from common strain energy directed island nucleation on patterned substrate in S-K mode, the surface/interface energy directed NCs growth on amorphous thermal oxide substrate in V-W mode is relatively a weaker effect, which requires the growth parameters to be tuned more strictly for the effect to show up. This work furthers our fundamental understanding of NC growth behavior on amorphous substrate with various morphologies.

2.6 Acknowledgement

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Chapter 3 High-density NiSi nanocrystals embedded in Al_2O_3/SiO_2 double-barrier for robust retention of nonvolatile memory

3.1. Introduction

Nonvolatile memories with discrete charge storage nodes have been investigated extensively during the past decade. Since it was pioneered by Tiwari in 1995[1], Si nanocrystal (NC) floating gate memory has been nominated as a promising replacement of conventional flash memory thanks to its immunity to defect-related charge leakage and potential to exceed flash scaling limit. Both academia and industry have also invested tremendous efforts into research of other NC memories, exploring new materials and novel gate structures for future flash memory [2-9]. Metal silicide NCs, with high density of states and robust thermal stability, have attracted much attention since they were proposed as good candidates to improve NC memory performance [10] and much work has been done to explore this material for nonvolatile memory application [11-18]. As an alternative way of improving memory performance, NC core-shell structure with additional barrier layer as floating gate has been developed and adopted by researchers. For example, metal and semiconductor NC core with oxide shell synthesized by various methods such as laser irradiation induced native oxidation [19], micelle dipping [20], chemical vapor deposition and annealing [21] and pulsed laser deposition [22] were reported.

3.2 Motivation

In this work, we report a metal-oxide-semiconductor capacitor memory device with an engineered floating gate similar to core-shell structures. The floating-gate structure consists of a layer of high-density vapor-solid-solid (VSS) [16] induced NiSi NCs by gas source molecular beam epitaxy (GSMBE) embedded in-between two Al_2O_3 thin barriers deposited by atomic layer deposition (ALD). Fig. 3.1(a) shows a schematic diagram of the device structure. The Al_2O_3/NiSi NC/Al_2O_3 floating gate is sandwiched by a control oxide layer and a tunnel oxide layer. Fig. 3.1(b) shows the flat energy band diagram of the memory device. The Fermi-level of NiSi NC with a

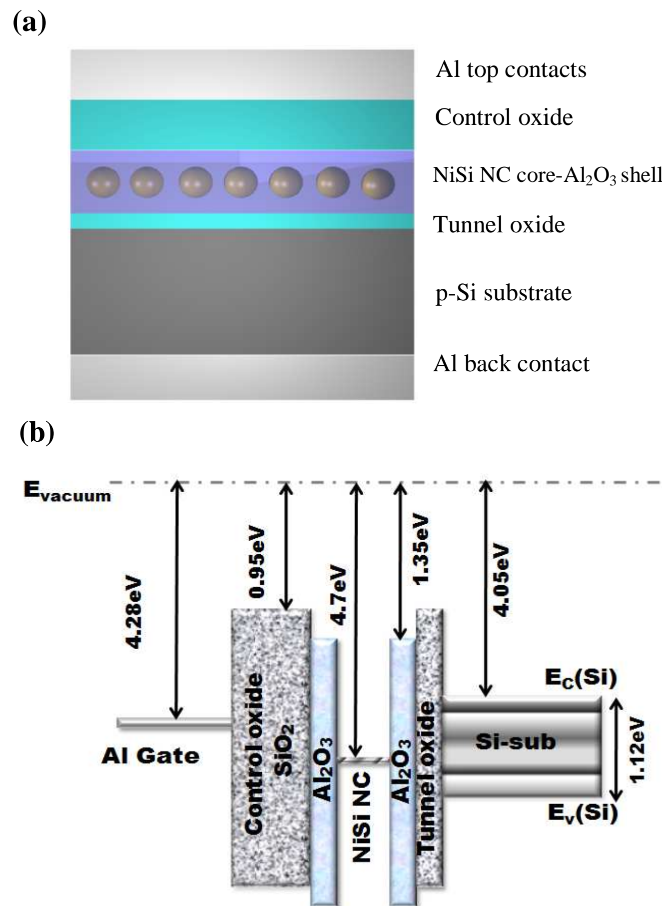

Fig. 3.1 (a) Schematic of device structure; (b) flat energy band diagram of NiSi NC-Al_2O_3 floating-gate memory.

work function of 4.7 eV [23] is aligned within the mid-gap of bulk Si. The conduction band offset between NiSi and Al_2O_3 (electron affinity 1.35eV, ref. 24) is as high as 3.35eV.

The benefit of using additional Al_2O_3 barrier layers is two folds. First, it is to minimize diffusion of Ni metal atoms into SiO_2 tunneling layer during high temperature process to reduce the charge leakage paths for prolonged retention. As shown in Fig. 3.2, during the VSS growth of metallic silicide NCs (i.e. NiSi NCs), metal catalyst is deposited onto very thin tunnel oxide layer and subsequent high temperature process may induce metal atoms diffusion, which leads to severe oxide quality degradation and increased leakage paths. The Al_2O_3 barrier plays an important role in suppressing the diffusion of metal atoms.

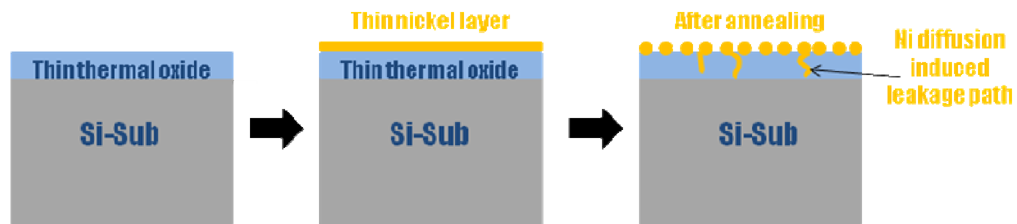

Fig. 3.2 Metal atom diffusion induced leakage paths in VSS process.

Second, it is to maintain programming efficiency and improve retention performance. Possible energy band diagrams of programming and retention states are illustrated in Fig. 3.3. During programming, positive gate bias is applied so that electrons can be pulled into NCs by Fowler-Nordheim tunneling. Because of the high-K property of Al_2O_3, electric field concentration effect [25] makes most of the voltage

drop on SiO_2 layer. In addition, since the barrier height of Al_2O_3 layer is lower than that of SiO_2, electrons do not actually have to go through the barrier of Al_2O_3 but only the thin SiO_2 tunnel barrier to reach the NC. Hence, it is believed that this structure has the ability to maintain the efficiency of programming operation compared to the structure without Al_2O_3. On the other hand, in retention state, electrons are kept in the deep quantum well formed by Al_2O_3/NiSi NC/Al_2O_3 structure. In this case, electrons see a barrier of both Al_2O_3 and SiO_2 and the total barrier thickness is increased. Therefore, robust retention characteristics are expected for this Al_2O_3/NiSi NCs/Al_2O_3 floating-gate memory device combining metallic silicide NCs with double-barrier structure.

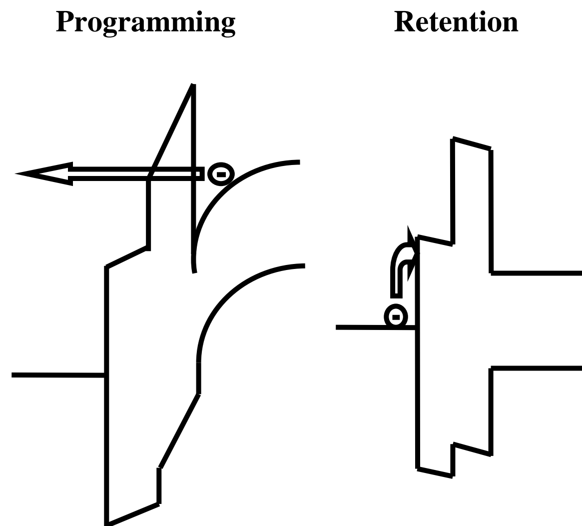

Fig. 3.3 Possible energy band diagram at programming and retention

3.3 Device fabrication

The device fabrication process flow is shown in Fig.3.4. It starts with a pre-cleaned p-type Si (100) substrate. A thin thermal oxide of 3 nm was grown on the substrate at 850ºC. This was followed by 2.5 nm Al_2O_3 deposition using ALD. A very thin layer of Ni was coated on the sample by room temperature electron-beam evaporation as catalyst and the sample was immediately transferred into a custom-built GSMBE system for subsequent silicide NC synthesis. Disilane (Si_2H_6) was used as the Si precursor to perform VSS growth at 600 ºC, which is a temperature much lower than the eutectic temperature between Ni and Si of 964 ºC [26]. Growth conditions (i.e. growth time, gas source flux) were calibrated to achieve reliable high-density ultra-uniform NCs growth over the whole sample surface. After NiSi NCs formation, another thin Al_2O_3 layer of 4.5nm was deposited on top by ALD to form the Al_2O_3/NiSi NC/Al_2O_3structure. Finally, 25nm SiO_2 was deposited as control oxide in a low pressure chemical vapor deposition (LPCVD) system and Al was evaporated onto the front and back side of the sample as contacts for the memory capacitors. Control device without NC embedded in Al_2O_3 and NC device without Al_2O_3 were fabricated simultaneously for comparison.

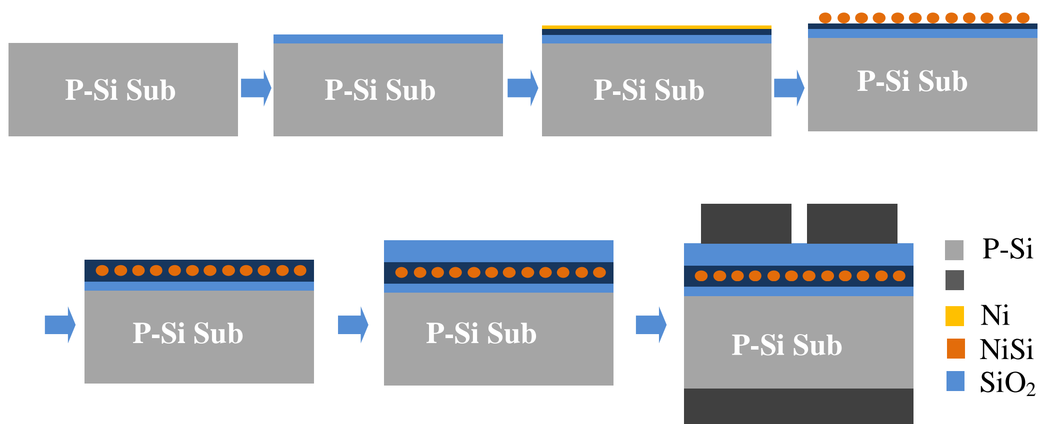

Fig. 3.4 Double barrier NC capacitor memory fabrication process flow.

3.4 Device characterization and discussion

3.4.1 Material and device structure characterizations

Fig. 3.5 (a) shows a scanning electron microscopy (SEM) image of the as-grown NCs on Al_2O_3 surface. The average size of uniformly distributed NCs over the whole sample surface is about 4.5 nm and the density is around 1.5×10^{12} cm^{-2}. X-ray photoelectron spectroscopy (XPS) was utilized to determine the chemical nature of the NCs. Fig. 3.5 (b) shows the XPS result of Ni $2p_{3/2}$ for the sample before top Al_2O_3 coverage. The binding energy peak found at 853.9 eV indicates that the nature of NC is NiSi [27]. Fig. 3.5 (c) and (d) show the cross-sectional transmission electron microscopy (TEM) images of the NC core-shell memory device and the control device without NC, respectively, where the interfaces are edge-on and the thickness of each layer in the devices could be measured directly from the images. The TEM images indicate that the interfaces are flat, and layer thicknesses are consistent with the designed ones, as mentioned above.

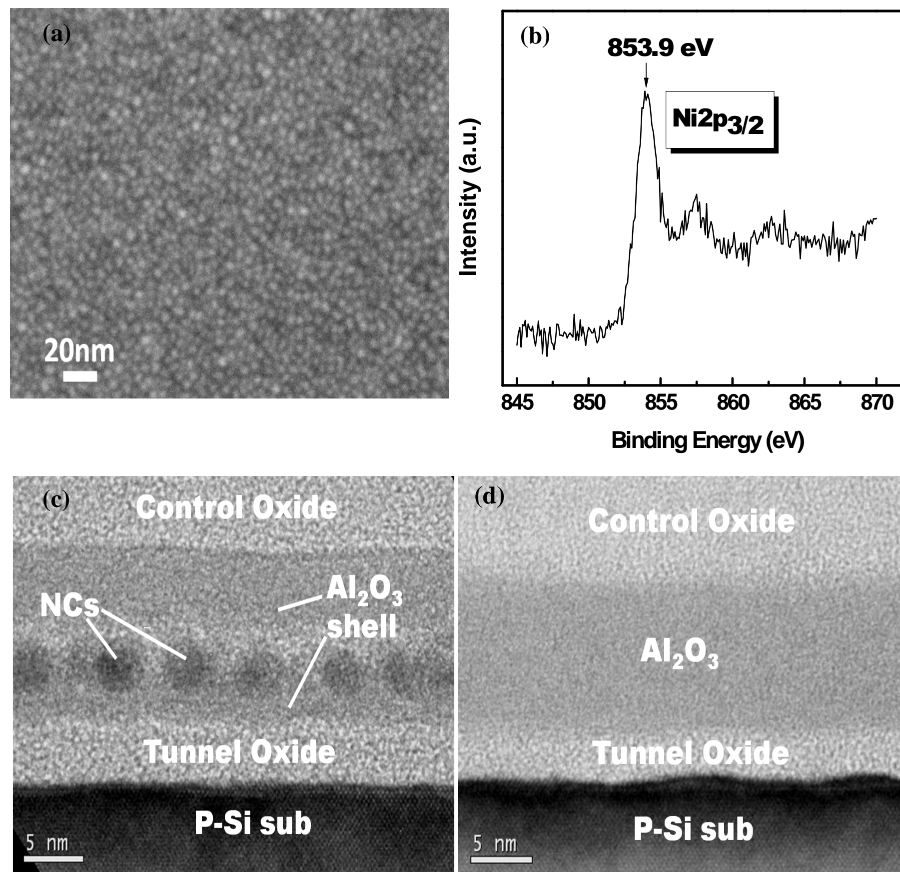

Fig. 3.5 (a) SEM image of high-density NiSi NCs; (b) XPS spectrum of NiSi NCs on $Al_2O_3/SiO_2/Si$ substrate; (c) cross-sectional TEM image of NiSi NC-Al_2O_3 floating-gate memory device, (d) cross-sectional TEM image of the control sample.

3.4.2 Memory window

Fig. 3.6 (a) and (b) show high-frequency (1MHz) capacitance-voltage (C-V) sweep characteristics of NiSi NC-Al_2O_3 floating-gate memory and its non-NC control device, respectively. With gate voltage increasing from 24V/-30V to 34V/-40V, the memory window increases from 1.4V to 15V, suggesting that the memory effect is due to the NC storage rather than defect/interface state charging. The large memory

window also suggests high charge storage capability of the NiSi NCs. In comparison, with the same gate voltage sweeping range, almost no memory window was observed in the control device without NCs, which confirms that memory window shown by the core-shell memory device is attributed to charge storage in the NCs. The high voltage required for C-V sweeping here is due to the thick control oxide layer deposited by LPCVD. With optimized device geometry, it is expected that lower gate voltage operation and shorter programming/erasing time can be achieved.

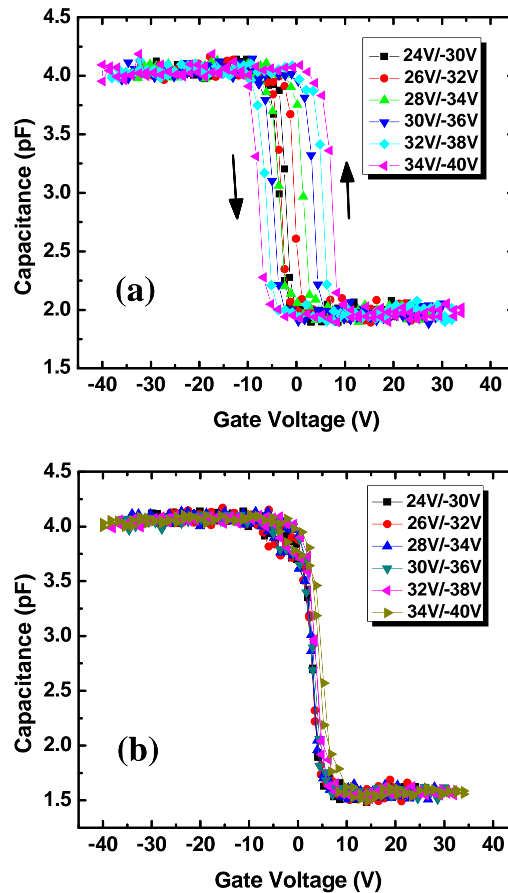

Fig. 3.6 C-V sweep of (a) NiSi NC-Al_2O_3 floating-gate memory device and (b) control device under different scanning gate voltages.

3.4.3 Transient performance

Fig. 3.7 (a) shows flat-band voltage shift (ΔV_{FB}) as a function of programming/erasing time under different gate voltages. Programming was conducted by biasing the gate with a positive voltage while a negative voltage was applied for erasing. Clear time dependence of ΔV_{FB} was observed in both programming and erasing case for gate voltage ±21V to ±24V. The lower speed of erasing than that of programming is due to the deep quantum well formed in the Al_2O_3/NiSi NC/Al_2O_3 structure, which makes electron see higher and thicker barrier in erasing. It should also be noticed from the curves that higher voltage results in larger ΔV_{FB}, suggesting a voltage-dependent programming/erasing behavior of the memory device. Fig. 3.7 (b) shows the ΔV_{FB} and number of electrons per NC as a function of writing voltage. The charge stored per unit area in a device is calculated from: $Q = (\varepsilon_{SiO2}/d_{SiO2})\Delta V_{FB}$, where ε_{SiO2} is the dielectric constant of SiO_2, d_{SiO2} is the equivalent control oxide thickness of the MOS device, which is 27nm in this work, and ΔV_{FB} is the V_{FB} shift between fresh state and programmed state. The charge number per NC is calculated from: # of electrons/dot=Q/Dq, where D is the NC density, which is 1.5×10^{12} cm^{-2} here and q is the electron charge. More than 5 electrons can be injected into each NC on average before saturation, indicating good charge holding capability of NiSi NCs similar to other metallic silicide NCs [16].

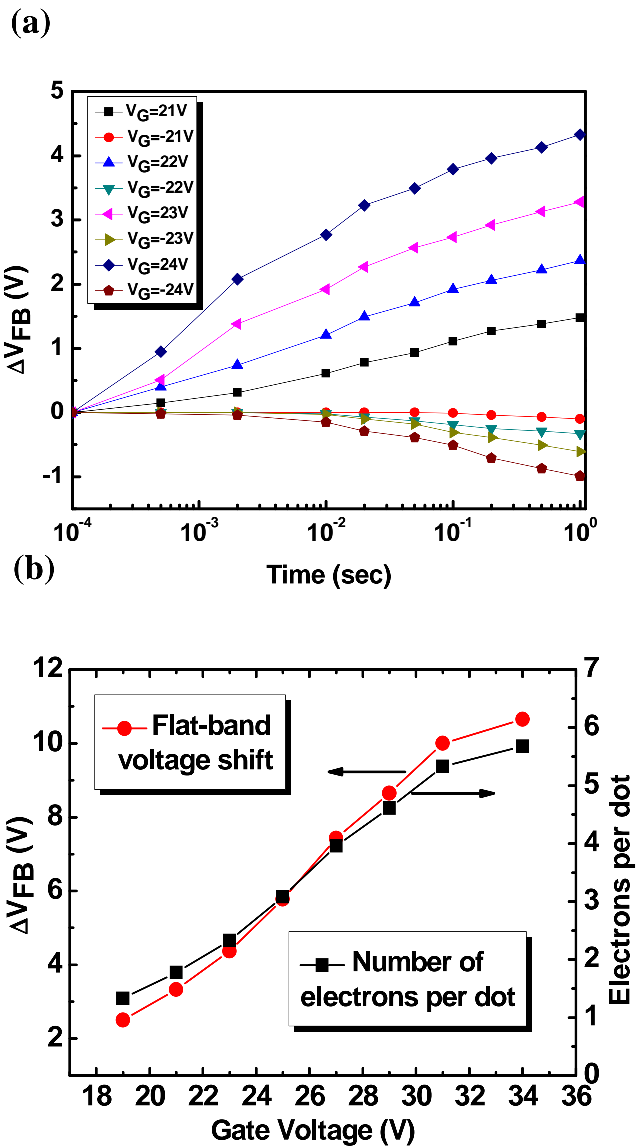

Fig. 3.7 (a) Transient characteristics of NiSi NC-Al_2O_3 floating-gate memory under different gate programming /erasing voltages,(b) flat-band voltage shift and number of electrons per dot as a function of gate bias.

3.4.4 Retention and Endurance

Fig. 3.8 (a) shows retention characteristics of NiSi NC-Al_2O_3 floating-gate memory at room temperature and 85ºC, respectively. The device was programmed at 19V/3sec and erased at -22V/3sec and ΔV_{FB} as a function of waiting time is plotted. Up to 10^5s, the charge loss ratio is only 10% for room temperature testing and 24% for high temperature testing. When extrapolated to 10 years, the curves show that there is still 80% and 60% charge maintained in the device, respectively. In contrast, 10-year charge remaining ratios between 60%-80% were observed at room temperature only in other core-shell or NC-only device structures [13, 17-19], suggesting that this NiSi NC/Al_2O_3/SiO_2 double-barrier floating-gate memory has the capability to achieve robust retention. Fig. 3.8 (b) shows room-temperature retention characteristics of control NiSi NC memory without Al_2O_3 barriers. The memory window was almost closed completely after 10^5s, indicating that the charge stored in NCs was lost at a very fast rate. As mentioned before, the diffusion and segregation of Ni metal atoms into SiO_2 tunneling layer during high-temperature NiSi synthesis process accounts for the fast leakage of charges and much worse retention properties. With an additional Al_2O_3 barrier, this problem has been effectively solved.

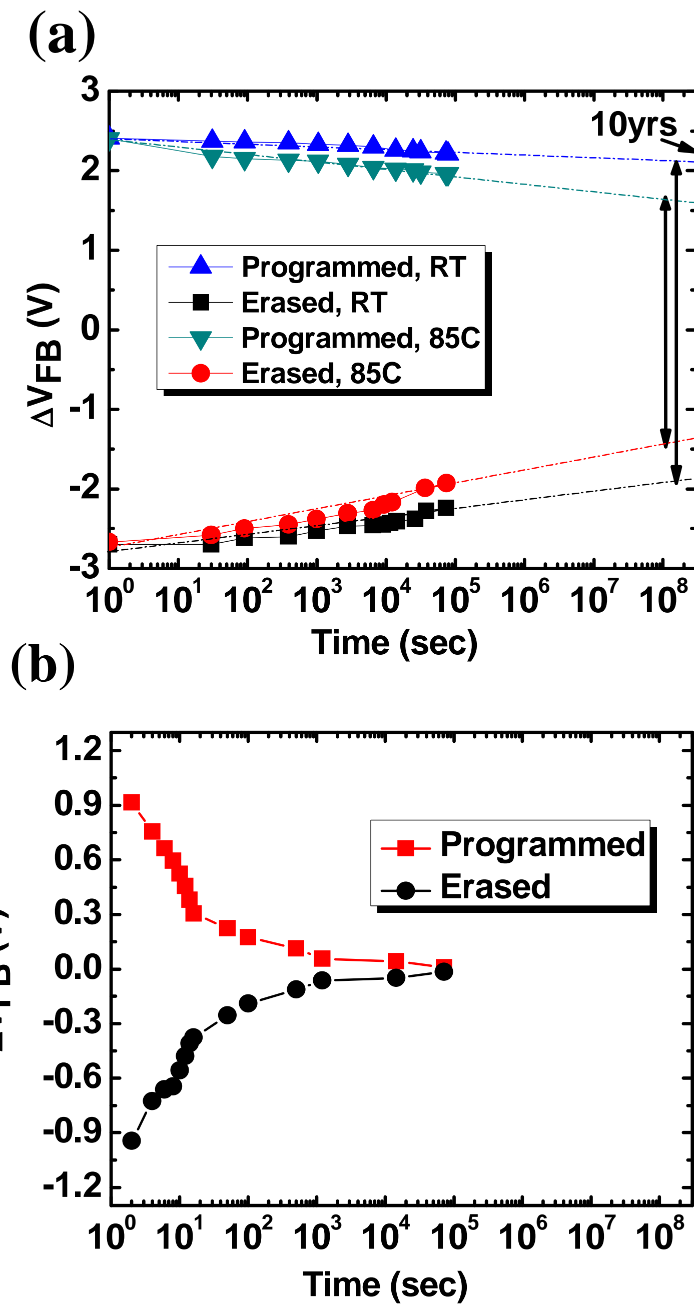

Fig. 3.8 (a) Retention characteristics of NiSi NC-Al_2O_3 floating-gate memory at room temperature and 85ºC; (b) retention characteristics of NiSi NC memory without Al_2O_3 barrier layer.

Table 3.1Comparison of retention performance among different novel NC memory work

	This work	[13]	[17]	[18]	[19]
Charge remained after 10 years at room temperature	**>80%**	**65%**	**80%**	**66%**	**68%**

Fig. 3.9 shows endurance characteristics of the device. Programming/Erasing voltage of ±20V was used to test the cycling performance. The small memory window opened is due to short pulses used in contrast to the long writing/erasing time and

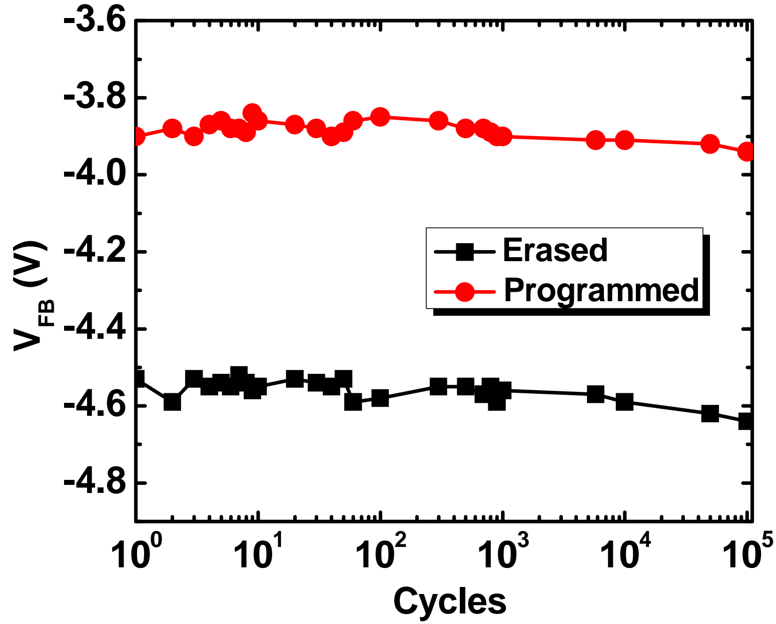

Fig. 3.9 Endurance characteristics of NiSi NC-Al_2O_3 floating-gate memory up to 10^5 cycles.

high voltage required by this device. It is evident that up to 10^5 cycles, the device stressed by such high gate bias keeps the window with almost no degradation, suggesting good endurance properties.

3.5 Summary

NiSi NCs of high density and good uniformity were synthesized by VSS growth in a GSMBE system using Si_2H_6 as Si precursor, based on which a nonvolatile memory with Al_2O_3/NiSi NC/Al_2O_3structure as floating gate was fabricated and characterized. The memory device exhibits large memory window, robust retention at both room temperature and high temperature of 85ºC, and good endurance. Further device geometry optimization of using thinner control oxide and varied Al_2O_3 thickness may be carried out to achieve low voltage operation as well as good transient performance. Memories with this structure can be a promising candidate for future flash memory application.

3.6 Acknowledgement

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Chapter 4 Non-Planar NiSi Nanocrystal Floating Gate Memory Based on A Triangular-Shaped Si Nanowire Array for Extending Nanocrystal Memory Scaling Limit

4.1 Introduction

Conventional flash memory with continuous floating gate faces increasing challenge brought by charge leakage and other scaling related issues [1]. Si nanocrystal (NC) memory was first introduced by Tiwari as an alternative to continuous floating gate memory [2] and has attracted much attention for its CMOS compatible fabrication process, immunity to oxide defect leakage together with its promising scalability thanks to the discrete charge storage nodes. Tremendous efforts have been invested into NC memory research ever since, using new cell structures and new materials [3]-[8]. Nevertheless, NC density and uniformity fluctuation have arisen as a critical concern as NC memory is unexceptionally approaching its scaling limit as other counterparts do [9]-[10]. NC number variation from cell to cell imposes serious constraints on overall device performance with respect to programming, erasing, memory window and retention. Furthermore, the reducing number of NCs in ultra-scaled memory cells severely limits the cell state controllability and reliability and may eventually lead to cell performance failure.

4.2 Motivation

The motivation behind this paper is to explore and demonstrate non-planar cell structure with high-density uniform metallic silicide NC charge storage nodes in the

same memory cell as a possible way to extend the scaling limit of NC memories without compromising the device performance. The structure of NiSi NC memory based on triangular-shaped Si nanowire (SiNW) array is shown in Fig. 4.1 (a). The internal structure of the gate stack on a single SiNW is shown in the magnified schematic; from bottom to top are SiNW, NC embedded between SiO_2/Al_2O_3 and Al gate finger. Fig. 4.1(b) shows the scanning electron microscopy (SEM) images of the as-fabricated device and the cross-sectional view of embedded triangular-shaped SiNWs. The cross-section of the SiNW is a quasiisosceles triangle with bottom edge of 140 nm and sides of 100 nm each. The advantage exhibited by this cell structure can be understood through comparison between planar NC memory cell and the proposed non-planar cell, as illustrated in Fig. 4.2. Considering the same amount of NCs in a cell, this non-planar cell only needs to occupy about half of the effective area of a planar device due to almost doubled surface area for NC accommodation (the angle between planar Si (100) plane and SiNW surface (111) is 54.7º). This will enhance the integration density of memory cells on a chip to a large extent without sacrificing the number of NCs per cell. In other words, considering the same effective cell size, the number of NCs controlling cell states is almost doubled in a non-planar device under the same NC deposition condition. In this case, the stored charge density of the whole cell is safely maintained by more NCs, leading to less dot density variation problem as compared to planar devices at the scaled technology node. In addition, the selection of silicide NCs in this work is due to the excellent thermal stability and large work function for long retention and enhanced device reliability [3], [6].

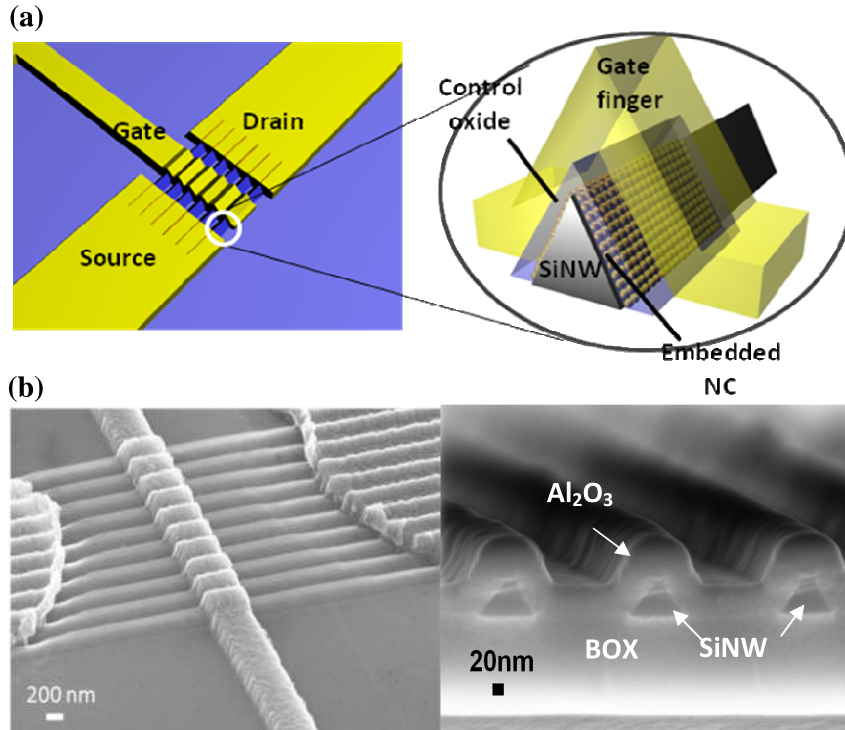

Fig. 4.1 (a) Schematic and (b) SEM images of triangular-shaped SiNW array based NiSi NC memory.

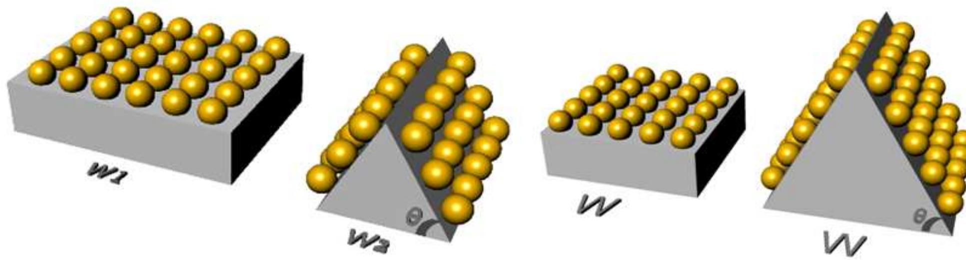

Fig. 4.2 Comparison between non-planar and planar NC memory cells: (a) cells with the same number of NCs; (b) cells with the same chip floor plan.

4.3 Device fabrication

The fabrication process is shown in Fig. 4.3. Starting with a commercially available SOI wafer (with 88nm p-type Si (100) active layer, Soitec, Inc.), phosphorous ion implantation was performed to dope the Si active layer for n-type NW device fabrication. The implant energy and dose were chosen to yield uniform doping concentration of 10^{18} atom cm^{-3} to ensure a reasonable drive current and good source and drain contacts. The sample was then annealed in nitrogen ambient at 950ºC for 60 sec to activate the doping impurities. Dry thermal oxidation at 950ºC and diluted HF etching were utilized to thin down the top Si layer to around 60nm. Line-and-space patterns along the [110] direction were created by e-beam lithography and chromium was deposited by e-beam evaporation to form hard mask for the next etching step. KOH solution was used to anisotropically etch the Si layer and etching time was carefully controlled to produce well aligned triangular-shaped SiNW array [11]. After hard mask removal and sample cleaning, 5nm tunnel oxide was formed by dry oxidation of the SiNW at 850ºC and subsequent annealing at 950ºC for oxide quality enhancement. This was followed by room temperature e-beam evaporation of a very thin layer of Ni as catalyst for silicide NC growth. NiSi NCs were synthesized by direct vapor-solid-solid (VSS) growth at 600ºC in a low pressure chemical vapor deposition (LPCVD) system, using SiH_4 as the gas source [6].

The SEM image of the top view of NC layer on a SiO_2-covered SiNW is shown in Fig. 4.4 (a). Fig. 4.4 (b) shows ultra-high-density NCs at the open area of the as-grown sample. It is determined from the images that the NCs are uniformly distributed over the whole sample surface with the average size of about 4.5nm and the density of around 1.5×10^{12} cm^{-2}. Thanks to the triangular shape of the nanowire,

such high density of nanocrystals is also ensured at the non-planar SiNW area through the same metal catalyst deposition and VSS growth processes. High resolution transmission electron microscopy (HRTEM) image of a single NC in the inset shows good crystallinity of the NC. Composition of the NCs is confirmed to be NiSi by HRTEM and X-ray photoelectron spectroscopy (XPS). By employing atomic layer deposition, 36nm Al_2O_3 was uniformly deposited as the control oxide for the device. Then the source and drain area were defined by photolithography and Ti/Au was deposited as the contacts to the highly doped SiNW array to form a junctionless transistor with no necessity of ion-implantation. This type of device bypasses the challenging junction formation steps and favors ultra-scaled device fabrication. A last e-beam lithography and e-beam evaporation step finalized the top-gated device fabrication by putting an Al gate finger over the multi-SiNW channel. The width of the gate finger defines the gate length on each SiNW to be 0.5 μm for each device. A control device without NCs was fabricated simultaneously for comparison.

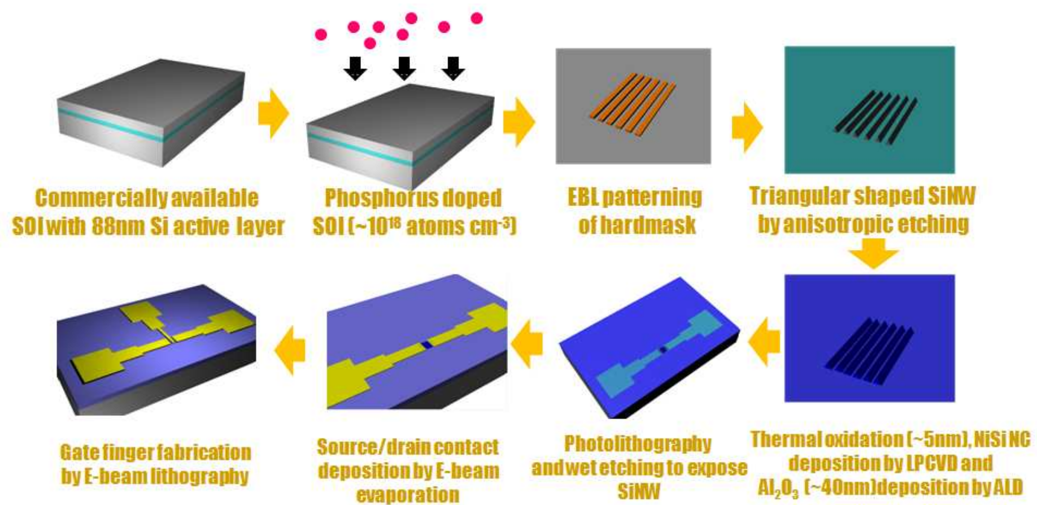

Fig. 4.3 Fabrication process flow of a SiNW array based non-planar NC memory device.

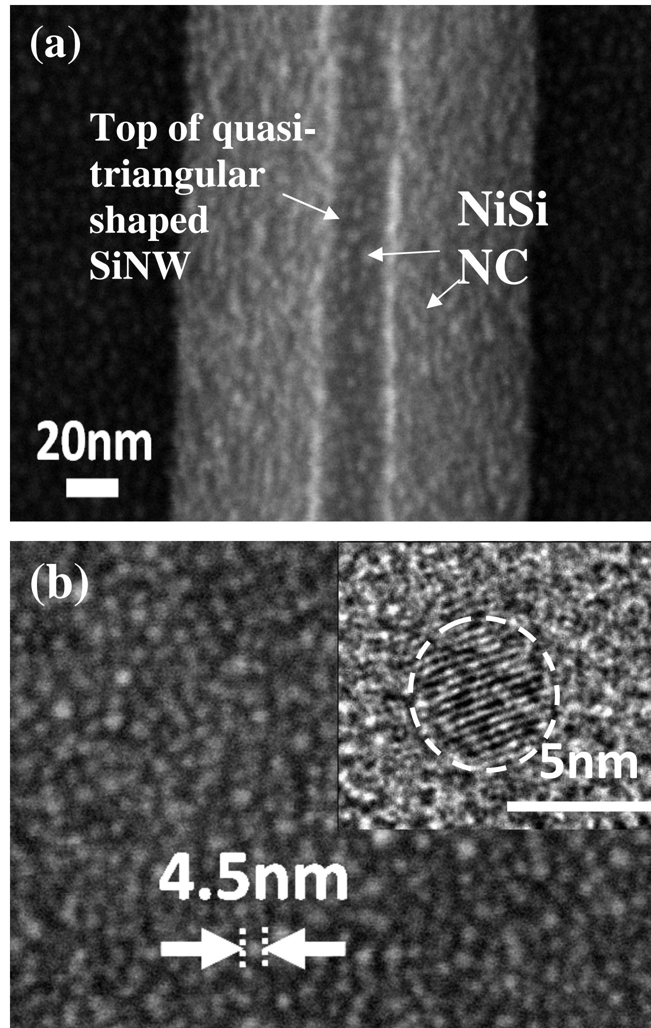

Fig. 4.4 (a) Top-view SEM image of NiSi NCs on a SiO_2-covered SiNW; (b) SEM image of NiSi NCs at open area. Inset shows an HRTEM image of single NC.

4.4 Results and discussion

4.4.1 Output characteristics

An Agilent 4155C semiconductor parameter analyzer was utilized to characterize the electrical properties of the devices. Fig. 4.5 shows the output

characteristics of the memory field effect transistor. The drain voltage was swept from 0V to 1V. Drain current increased with gate bias increasing from -1V to 1V, indicating typical I-V characteristics of an n-type enhance-mode junction-less device based upon heavily doped n-type NW channel.

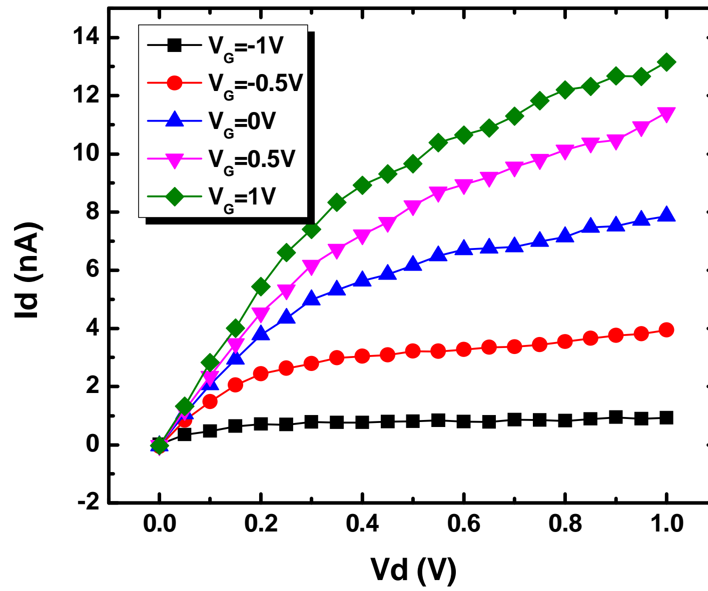

Fig. 4.5 Output characteristics of SiNW array based non-planar NC memory transistor.

4.4.2 Transfer characteristics

Fig. 4.6 shows the transfer characteristics (I_d-V_g) for this memory device at neutral, programmed and erased states. A gate bias of 7.5V and -10V was applied for programming and erasing, respectively, both for 100 milliseconds (ms). The shift of I_d-V_g curve towards higher (lower) gate voltage side indicates the charging (discharging) of NiSi NCs with electrons. In comparison, the I_d-V_g curves of the

control device shows negligible shift under the same programming condition (not shown here), which confirms that the memory effect should be attributed to the NCs.

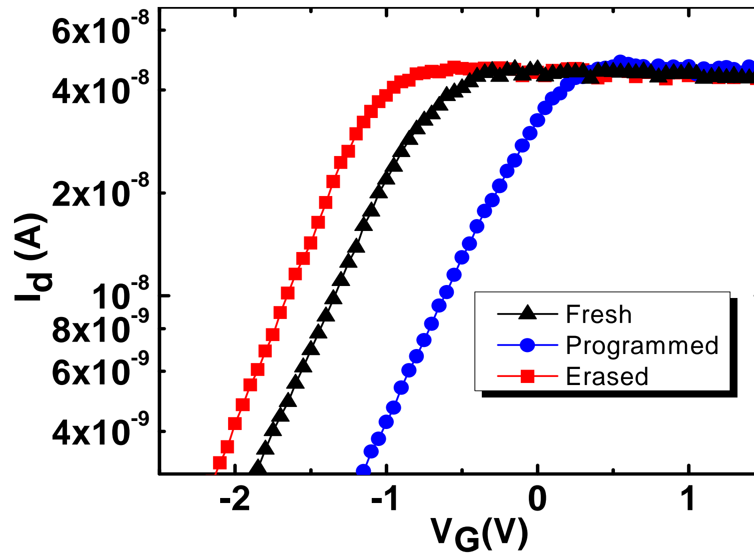

Fig. 4.6 Transfer characteristics of triangular shaped SiNW array based NiSi NC memory at the neutral, programmed and erased states.

4.4.3 Transient characteristics

Fig. 4.7 (a) and (b) show the time and gate bias-dependent programming and erasing characteristics of the device, respectively. As shown in Fig. 4.7 (a), the threshold voltage shift (ΔV_{th}) of the device increases with programming and erasing (P/E) time under gate bias of ±10V until saturation at around 10ms. The large window of 2.7V indicates good P/E performance and charge storage capability. ΔV_{th} as a function of gate bias in Fig. 4.7 (b) shows a clear voltage dependence of the P/E performance under a fixed programming/erasing time of 20ms, which is consistent with the fact that higher voltage promotes electron tunneling through the barrier between the floating gate (NCs) and the substrate. The slightly faster speed in

programming than in erasing case can be ascribed to the lower tunneling barrier height electrons see from the NW toward the NC.

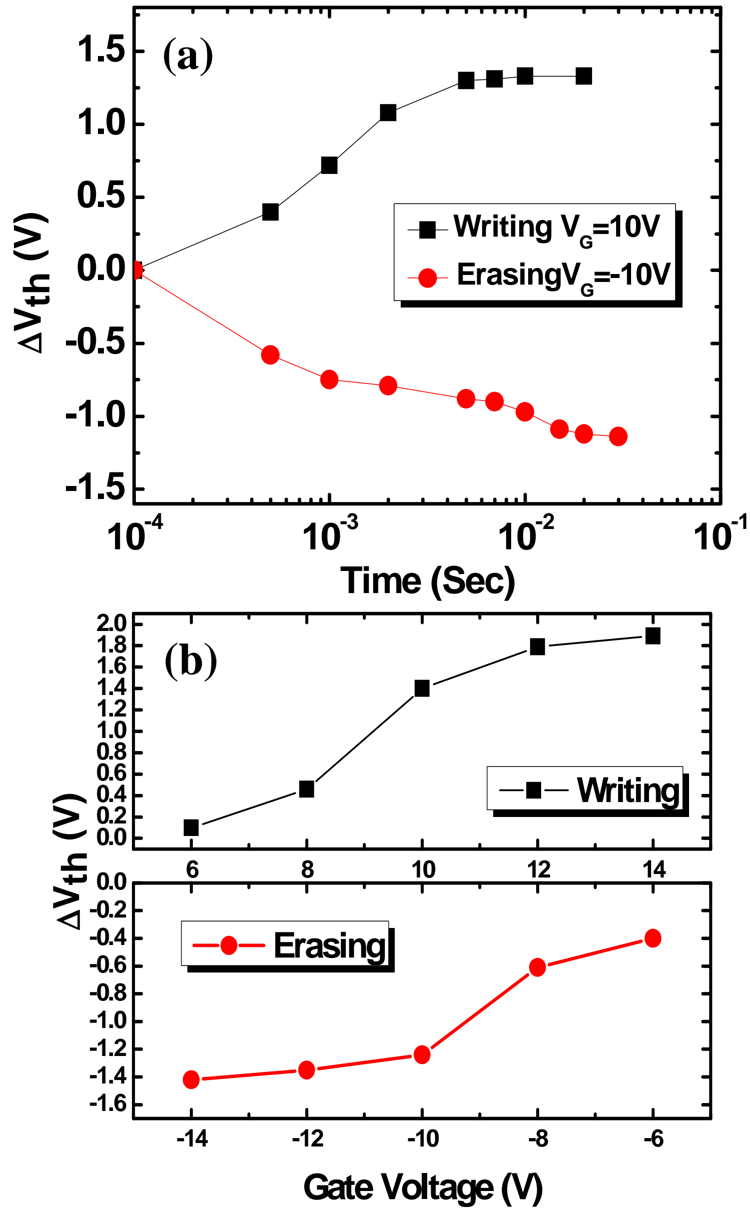

Fig. 4.7 (a) Time and (b) gate bias dependent P/E characteristics.

4.4.4 Retention and Endurance characteristics

Fig. 4.8 (a) shows the comparison between retention characteristics at room temperature and 85ºC. Programmed and erased with ±12V/200ms, the device shows a remained memory window of 2V and 1.5V for room temperature and high temperature test, respectively when extrapolated to 10 years, suggesting insignificant degradation of retention performance in high temperature environment thanks to robust thermal stability of metallic silicide NCs. Fig. 4.8 (b) shows the endurance characteristics under gate bias of ±10V. Only very slight memory window shrinkage was observed after cycling at both room temperature and 85ºC. The similarity in endurance characteristics at room temperature and high temperature again indicates that no evident performance degradation of this type of device happens under high temperature.

It should be noted that although a strict comparison of performance among reported NC memory work is impossible due to varied device structures, NC materials/density and tunneling/control oxide materials/thicknesses, rough evaluation of P/E efficiency, retention and endurance characteristics among different NC memory devices shows that the overall memory performance achieved with this device is very competent [4], [12]-[18]. This includes the relatively low operation voltages required in light of the large ΔV_{th} exhibited, which may benefit from the particular electric field distribution due to non-planar geometry [14], and the robustness of retention and endurance properties at both room and high temperature, as described above. With further process optimization, it is expected that non-planar devices like this could achieve much more enhanced performance for future memory scaling.

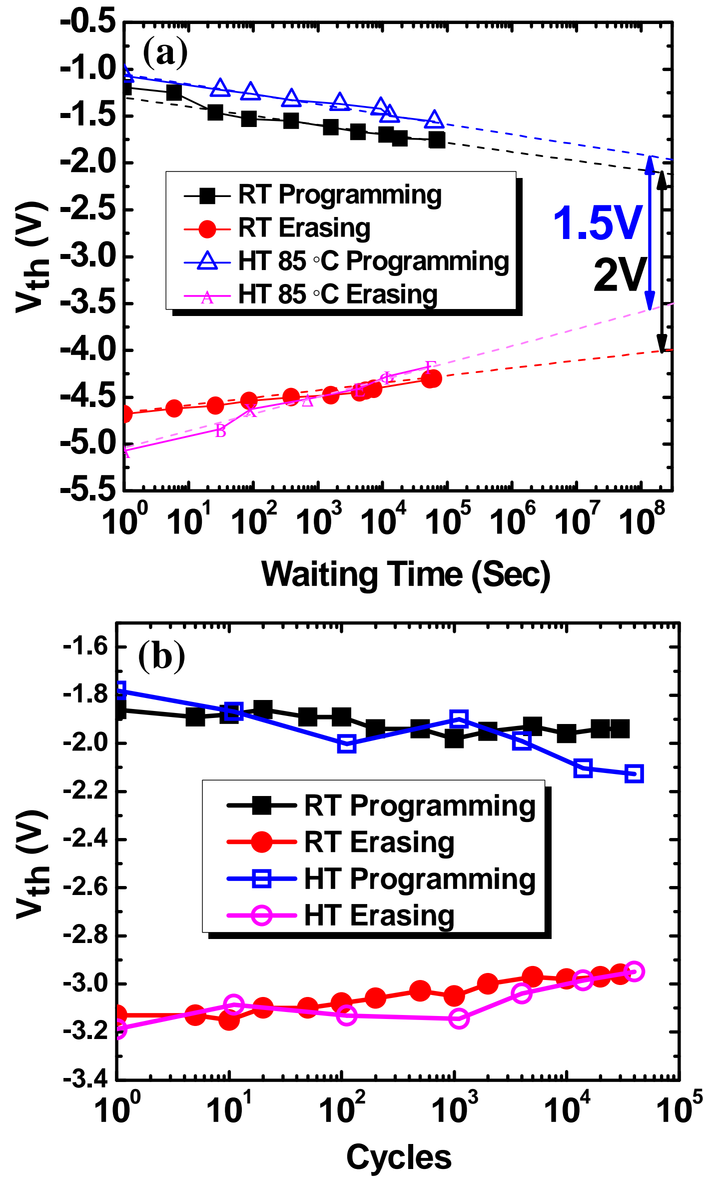

Fig. 4.8 (a) Retention characteristics and (b) Endurance characteristics of triangular-shaped SiNW array based NiSi NC memory at RT and 85ºC.

4.5 Summary

The idea of non-planarity is demonstrated for NC memory cell through fabrication and characterization of a proof-of-concept device based on triangular-shaped SiNW array. This device shows good programming, erasing, retention and endurance performance. For scaling up cell density, follow-up work on single SiNW with reduced sizes will be carried out to further prove that dot density variation effect is alleviated in three-dimensional devices and that this device architecture can be a possible way of pushing the scaling limit of NC memories further at the scaled memory technology nodes.

4.6 Acknowledgement

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Chapter 5 Non-Volatile Memory Effect of a High-Density NiSi Nano-Dots Floating Gate Transistor Memory Using Single Si Nanowire Channel

5.1 Introduction

The invention of Si nano-dot floating gate memory has stimulated broad interests among non-volatile memory community thanks to the improved reliability, CMOS compatible process, and its promise of scalability when the golden era of flash technology is approaching the limit [1]. Nano-floating gate memory employing different types of nano-dots, namely, semiconductor [2, 3], metal [4, 5], metallic silicide [6, 7, 8], core-shell dots [9, 10] and dielectrics [11, 12], have received extensive investigation. Moreover, energy band structure engineering has been widely carried out adopting varied dielectric stack [13-16] in order to enhance the memory performance for scaled technology nodes.

Nevertheless, problems of this technology have inevitably arisen as device dimensions are reduced. Despite all the efforts spent, as described in last chapter, dot density fluctuation among others remains the most serious issue in miniaturized cells [17, 18]. The number of floating dots controlling cell states becomes lower and lower in traditional planar cells as size shrinkage continues, leading to severe degradation of reliability for single cell due to less charge storage elements or poorer capability. Statistically, dot distribution shows a strong effect on the electrical characteristics of memory cells at array/chip level and random dot dispersion issue is the primary cause of significant cell-to-cell performance deviation of this particular memory family. Indeed, device performance becomes extremely dot location-sensitive and the cell with sparse and scattering dots (charge) distribution can show dramatic variance in

properties from those with better dots (charge) coverage. For instance, as one of the consequences, percolation happens where channel conduction is not well controlled by charge storage and screening effect, leading to unpredictable dot distribution-dependent memory windows and requiring. Therefore, this lack of controllability puts serious constraints on the application of nano-floating gate memory technology, hindering its steps toward manufacturing stage and requiring urgent mitigation before it goes to further scaled nodes.

5.2 Motivation

In light of the aforementioned problems, a scaled device channel covered by a floating gate layer with high density nano-dots of superior uniformity becomes an essence. In addition, increasing the number of dots per cell by non-planar channel architectures can be another possible solution due to increased cell area. Toward the goal of non-planar devices, efforts have been put into exploring various channel structures, among which the most attractive ones are FinFETs [19] and surrounding-gate vertical FETs [20]. With their nanocrystal memory variants also proposed and developed [21, 22, 23], these non-planar technologies have well extended logic and memory transistor dimensions to the third one. An alternative approach to realize scaled non-planar device channel is to adopt nanowires (NWs), which have been nominated building blocks for future electronics for their unique electronic properties and scalable dimensions. Nano-floating gate memory devices employing NW channel have been reported, aiming at maximizing both the charge storage and transport capabilities [24, 25]. However, the nano-dots used in these studies were randomly

spin-coated colloidal dots with low sheet density, leaving limited control over the size and density distribution of the nano-dots. The size of NW was also relatively large, around 90-120nm. Hence, it is hence desirable to develop more favorable methods for nano-dots synthesis to promote the advantages brought by non-planar channel, particularly when the channel size is reduced to deep-scaled regime. Recently we have reported a memory device based on multi-Si NW channel [26]. This device combines non-planar cell with high-density uniform metallic silicide NC as charge storage nodes, providing a possible way to extend the scaling limit of NC memory devices. Compared to planar device with the same floor plan, the number of NCs that controls cell states is almost doubled in this non-planar device, leading to less dot density variation problems and enhanced cell operation reliability.

In this chapter, as a piece of follow-up work, we report an ultra-scaled non-planar NiSi NC memory device with single triangular-shaped SiNW channel enclosed by one Si (100) plane and two Si (111) planes on a SOI substrate. Although similar NW fabrication process was employed as in ref. 26, single NW channel rather than multi-NW channel would reduce complexity of each cell for reliable device performance and also significantly increase data storage density in future memory array integration. Furthermore, dot density variation is an effect directly associated with device dimensions and becomes more and more evident as cell size shrinks. Therefore, it is necessary to realize a device with scaled dimensions by this non-planar technology for further clarification and future applications. In contrast to the large size of the earlier demonstrated multi-Si NW channel [26], the size (base) of the NW employed here in this work is aggressively scaled to around 40nm. This physical size could be adopted in 22 nm technology node if similar design rule demonstrated in

90 nm technology node NC memory array could be used [27]. Since the angle between Si (100) and (111) planes is 54.74º. Compared to planar device with the same floor area, the number of NCs that controls cell states is almost doubled in this non-planar device, leading to less dot density variation problems and enhanced cell operation reliability.

5.3 Device fabrication

Fig. 5.1 shows the schematic of the structure of back-gated device and its step-by-step fabrication process flow. First, phosphorus ion implantation was performed on a commercially available SOI wafer (Soitec, inc.) with 88nm p-type Si (100) active layer and 145 buried oxide layer to achieve a doping concentration of 10^{18} cm^{-3}. Then dopants were activated at 950ºC for 60sec. Stand-alone Si NWs were obtained on buried oxide surface via top-down wet chemical etching by KOH solution. After DI water rinsing, a 5nm thermal oxide was formed by dry oxidation on the surface of NWs as tunneling layer. High-density NiSi nano-dots were deposited over the whole sample surface as floating gate for charge storage by vapor-solid-solid (VSS) method. VSS has been a traditional way used for NW growth study [28]. However the initial stage of the VSS growth to form silicide nano-dots before the formation of NWs can be a reliable and reproducible way for high-density storage nodes preparation as reported in our previous work [8, 15]. To perform VSS growth, a very thin layer of Ni was deposited by e-beam evaporation on the sample surface, followed by immediate transfer of the sample into low pressure chemical vapor deposition system for NiSi nano-dots growth at 575 ºC using SiH_4 as Si precursor. 40nm Al_2O_3 was deposited by

atomic layer deposition to cover the nano-dots/NW surface as passivation. Schematics (f) through (g) in the process flow show the view of the subsequent fabrication steps from the cutting plane AA'. By using E-beam lithography, two electrode patterns were aligned onto the SiNW to create two openings for the next etching step. After removing Al_2O_3/nano-dots/SiO_2 layers by wet etching using diluted HF (1:100) for 30sec, SiNW was exposed in the opened windows. Ti/Au was deposited by room temperature e-beam evaporation as direct metal contacts to the SiNW and the two electrodes were formed by a lift-off process. Previously junction-less transistor was reported as being advantageous in terms of the simplified fabrication process and promise of scalability [30]. The benefit of this type of device can be more pronounced in scaled devices where source/drain implantation becomes extremely challenging. Here we adopt this junction-less structure for our memory with a NW channel in line with the scaling requirements of nano-floating gate memory device. Aluminum was also deposited to the back side of the wafer to make good back gate contact. A control device with no nano-dots embedded was fabricated simultaneously for comparison.

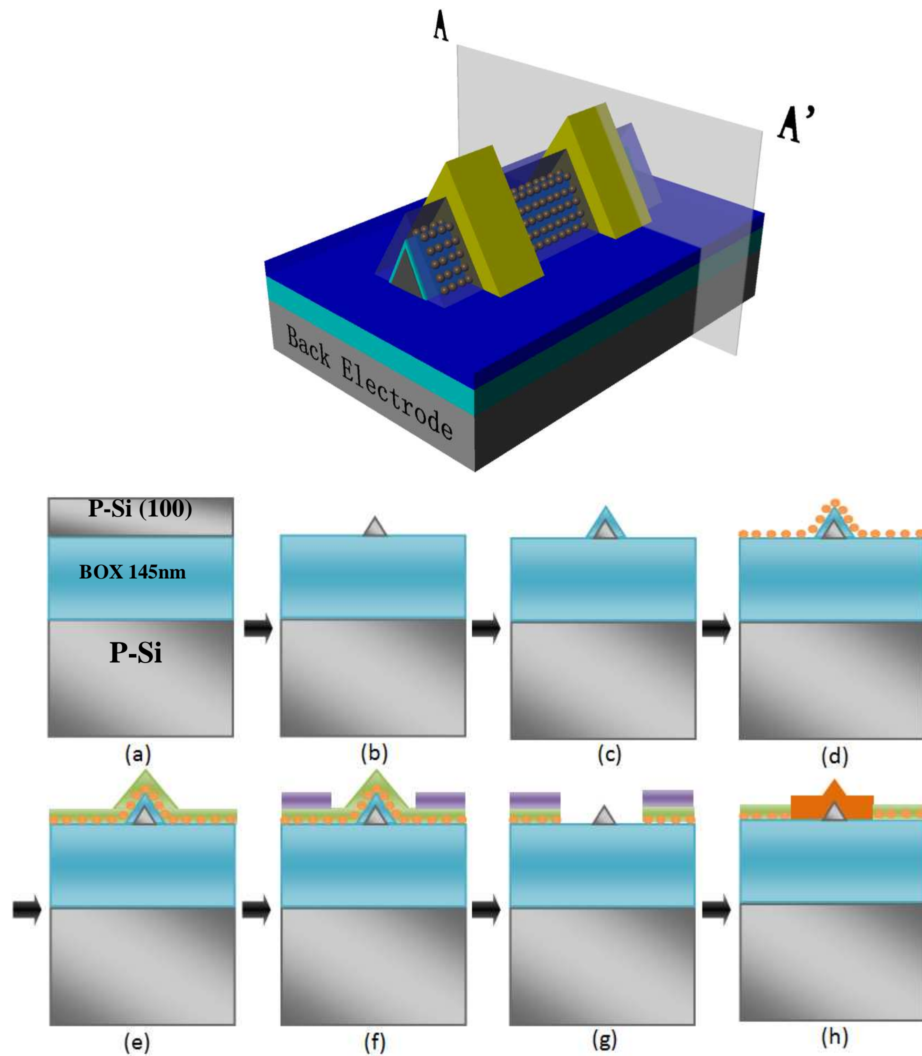

Fig. 5.1 Schematic of back-gated device structure and fabrication process flow: (a) SOI wafer; (b) SiNW after etching; (c) Tunneling oxide by dry oxidation; (d) Nano-dots deposition; (e) Al_2O_3 passivation; (f) E-beam lithography patterning of S/D; (g) Wet etching to expose SiNW channel; (h) Contact metal deposition.

5.4 Results and discussion

5.4.1 Material and device structure characterization

The device at different stages of the fabrication process flow was characterized by SEM and TEM. Fig. 5.2 (a) shows an SEM image of the triangular shaped SiNW on buried oxide at a tilted angle. Fig. 5.2 (b) and (c) show the top view of nano-dots distributed on top of a NW and at the open area of the sample right after VSS growth. A nano-dots layer with high density of 1.5×10^{12} cm^{-2} is achieved with ultra-uniform distribution and average size of around 4.5 nm. In Fig. 5.2 (d), the high-resolution XPS data obtained from the nano-dot layer for Ni $2P_{3/2}$ shows a binding energy at 853.9 eV, confirming that the nature of NCs is NiSi [30].

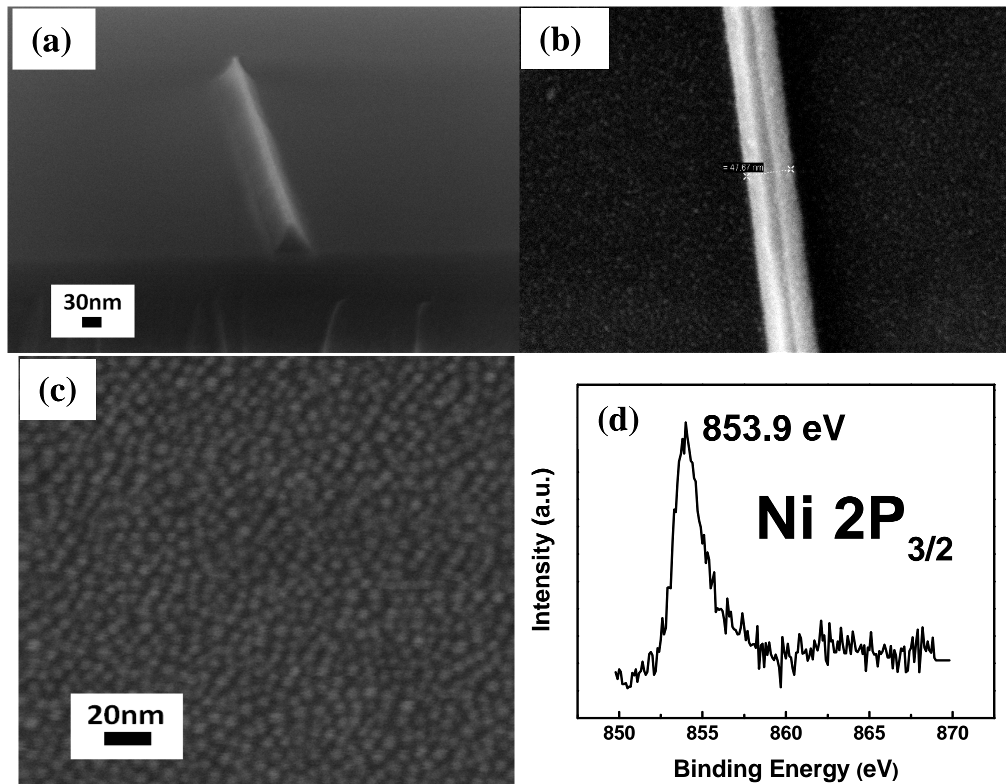

Fig. 5.2 (a) Tilted cross-sectional view of stand-alone triangular-shaped SiNW (~40nm); (b) Top view of high-density nano-dots on tunneling oxide-covered SiNW; (c) Evenly distributed nano-dots at open area; (d) XPS result of nano-dots layer.

Fig. 5.3 (a) shows an SEM image of the NW after Al_2O_3 coverage. The finalized device with two metal electrodes is shown in the inset. Fig. 5.3 (b) is the cross-sectional TEM image of the triangular-shaped NW embedded under Al_2O_3 and thin SiO_2 tunneling layer. This TEM sample was prepared by a Leo XB1540 Focus Ion Beam (FIB) system through a milling, lift-out and polishing process and an embedded layer of nano-dots can be clearly seen.

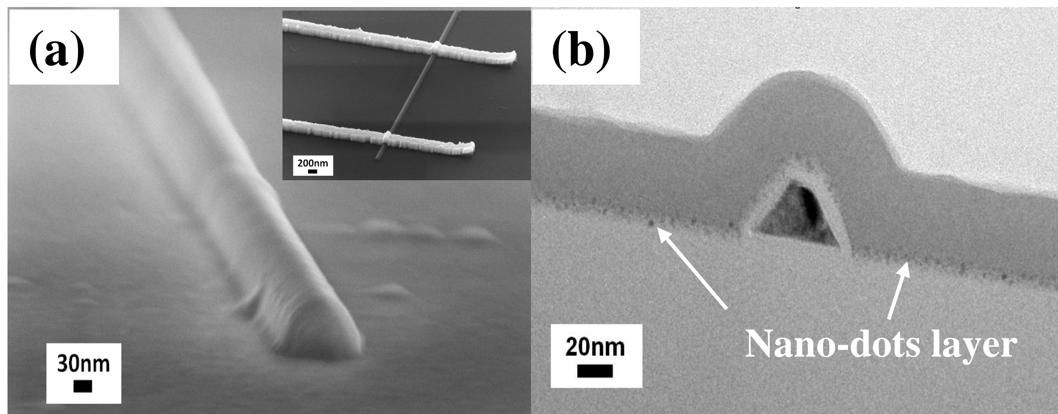

Fig. 5.3 (a) Tilted SEM view of NW covered with Al2O3; Inset: S/D contacts of as-fabricated device by E-beam lithography; (d) Cross-sectional TEM image of triangular SiNW embedded in Al_2O_3.

5.4.2 Electrical characterization

5.4.2.1 Transfer characteristics

The current-voltage characteristics of this memory device were tested by an Agilent 4155C semiconductor analyzer. Clear memory effect is shown in the transfer characteristics of the device at neutral, programmed and erased states in Fig. 5.4. As seen from the figure, the phosphorus doped NW device shows enhancement-mode n-

type characteristics and the current level in this device is very low. This is due to the schottky contacts formed between the metal electrodes and SiNW, which leads to on-state currents at nano-ampere scale. Contact resistance plays a significant role in determining the current-voltage properties of NW devices where device features shrink to nanometer scale and good ohmic contact formation becomes extremely challenging [31, 32]. Despite the low current level the memory effect of this device is the focus and of more concern in this work. Source and drain are grounded during programming/erasing. When a pulse of 60V/1sec is applied to the back gate, the I_d-V_g curve shows a large shift to the right, suggesting the charging of the floating gate (nano-dots) and the shift of threshold voltage (ΔV_{th}) is due to the excess electric field imposed by the stored charges. In contrast, when the device is erased by a negative pulse of -60V/1sec, the charges in the floating gate are pulled back to the channel and the curve shifts back to the left. The control device exhibits negligible shift in I_d-V_g curves under the same operation conditions (not shown here), which also confirms that the memory effect stems from nano-dots charging/discharging rather than defect/trap charge storage. The high gate voltage required to bias the back gate is due to the existence of thick buried oxide layer in the wafer and the inefficiency of fringing field programming/erasing mechanism.

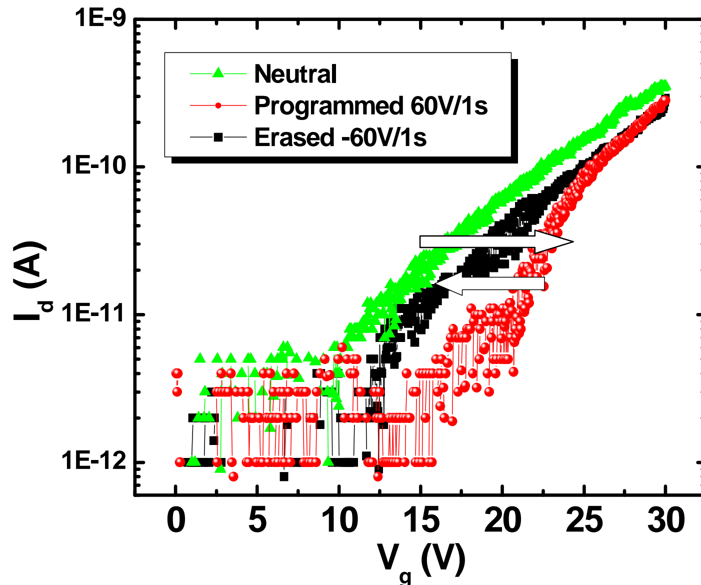

Fig. 5.4 Transfer characteristics of back-gated non-planar nano-floating gate memory at neutral, programmed and erased states.

5.4.2.2 Programming/erasing mechanism: fringing field

Due to particular geometries of the back gate and channel, this NW device relies on fringing electric field originating from the back electrode to implement the programming/erasing processes [33, 34]. Fig. 5.5 (a) shows the equivalent energy band diagram of the device. The gate and buried oxide layer are in dashed line because in real device they should be on the back side of SiNW. During programming/erasing operations, the buried oxide layer serves as part of control oxide while in retention state charges are kept in the deep quantum well formed by Al_2O_3/NiSi nano-dots/tunneling SiO_2 sandwich structure thanks to the large conduction band offset and work function of NiSi. Simulation results in Fig. 5.5 (b) and (c) from Comsol Multiphysics qualitatively show the direction of electric field

within the device around the channel at programming and erasing states, respectively. In contrast to the one-dimensional SiNW channel, the whole back side of the sample acts as the back electrode and the area of this back gate is so large that it can be considered two-dimensional. During programming process, the channel is grounded and a positive bias is pulsed on the back gate. In this case, the electrical potential of the nano-dots layer is lower than that of the back gate but higher than that of the channel, and the electric field starting from the back electrode is oriented from the nano-dots toward the channel. This field accounts for the charging of nano-dots and the right shift of the I_d-V_g curve under a positive bias. Similarly, the back gate is negative biased when the device is erased (Fig. 5.5 (c)) and electrons are pulled from the nano-dots back to the channel due to the fringing field and capacitive coupling among gate, nano-dots and NW channel. Therefore, when a negative pulse is applied, the I_d-V_g curve shifts to the left to erased state.

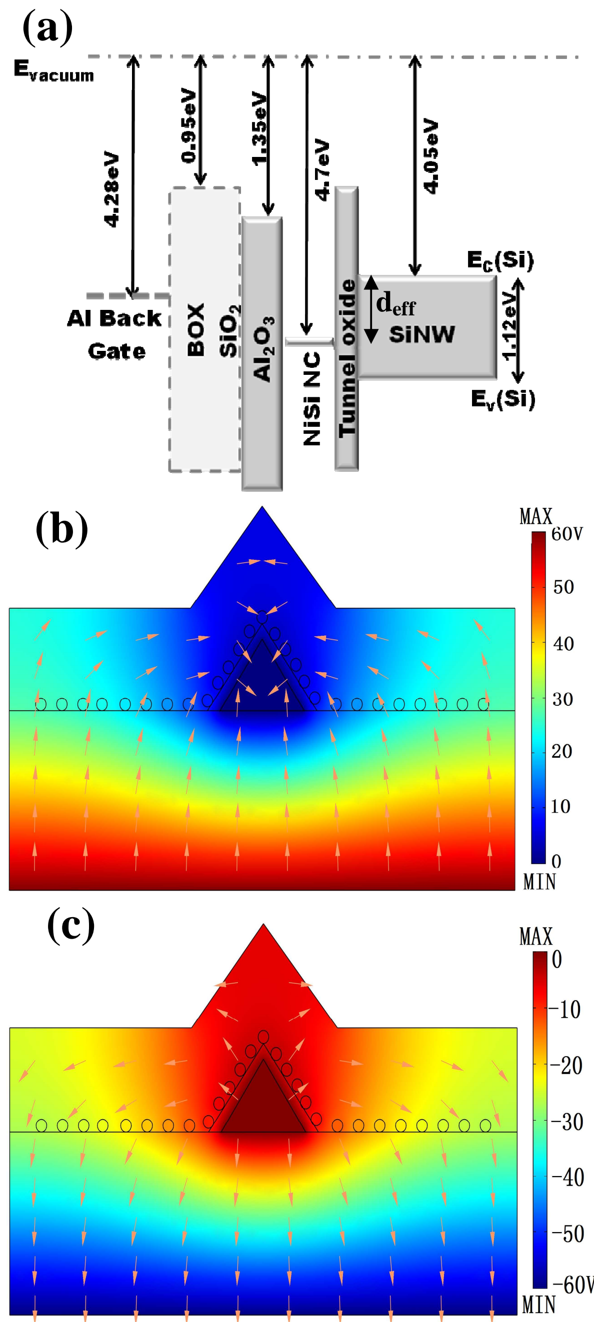

Fig. 5.5 (a) Equivalent energy band diagram of back-gated non-planar nano-floating gate memory, work function of NiSi~4.7eV; (b) Fringing electrical field direction during programming; (c) Fringing electrical field direction during erasing.

5.4.2.3 Programming/erasing characteristics

The programming/erasing behavior of this device was studied via testing the transient performance and examining ΔV_{th} under varied back gate bias. Threshold voltages (V_{th}) of the device at different states are extracted by I_d-V_g curve sweeping and linear extrapolation of the curve at the point of maximum slope to x-axis where $I_d=0$ [35]. As shown in Fig. 5.6, for each gate voltage, ΔV_{th} increases with programming/erasing time until saturation starts to occur at millisecond scale. Under gate voltage of ±50V, the device exhibits ΔV_{th} of 3.2V and 1.8V at around 30ms for programming and erasing, respectively. With a higher gate bias of ±80V, larger ΔV_{th} of 12V and 10.3V is observed under same writing/erasing time.

Threshold voltage shift caused by one electron storage in each nano-dot (ΔV_{th0}) can be estimated by rough calculation as follows: $Q_0=De=1.5\times10^{12}cm^{-2}\times1.6\times10^{-19}C=2.4\times10^{-7}C/cm^2$, where Q_0 is the charge sheet density assuming each nano-dot is charged evenly by one electron, D is the sheet density of nano-dots and e is the unit charge. Then $\Delta V_{th0}= Q_0/C_{control}$~10V is the resulted threshold voltage shift with this device geometry, with $C_{control}$ being the equivalent control oxide capacitance (consider t_{BOX}=145nm, assume a control oxide thickness of 150nm). From the programming/erasing behavior shown by Fig 5.6 (a), we observe a saturation of ΔV_{th} at around 10V for the gate bias used, which indicates that on average only one electron is injected into each nano-dot. The poor efficiency of fringing-field writing/erasing scheme and the thick buried oxide are responsible for this small shift.

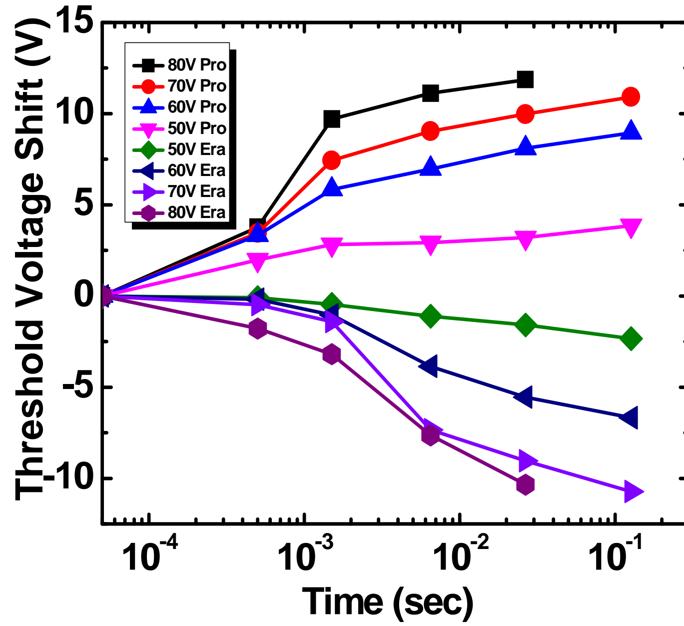

Fig. 5.6 Programming/Erasing characteristics of back-gated non-planar nano-floating gate memory under varied gate bias;

5.4.2.4 Retention

Charge retention characteristics of the device were also obtained at both room temperature and high temperature of 85 ºC, as shown in Fig. 5.7. The device at neutral state was first programmed/erased at ±60V/1sec for electron/hole injection to the nano-dots and ΔV_{th} was tracked and recorded as a function of waiting time to determine the loss of stored charge. In the beginning right after charge injection, the opening between two states, namely, programmed and erased, is around 12V. After around 10^5 sec, slight shrinkage happens and the opening decreases to 10V for room temperature case and 8.5V for high temperature case. As far as typical flash memory retention time of 10 years is concerned, extrapolated lines of ΔV_{th} change suggest an linear trend with more than 50% of the charge remained and a clear separation of the

two states for both room temperature and high temperature case. The good high-temperature retention performance of this device can be attributed to the robust thermal stability of NiSi nano-dots as reported in previous work [15]. Another possible contributing factor is the elevated energy levels in small NW channel that makes it harder for stored charge to tunnel back from nano-dots [36].

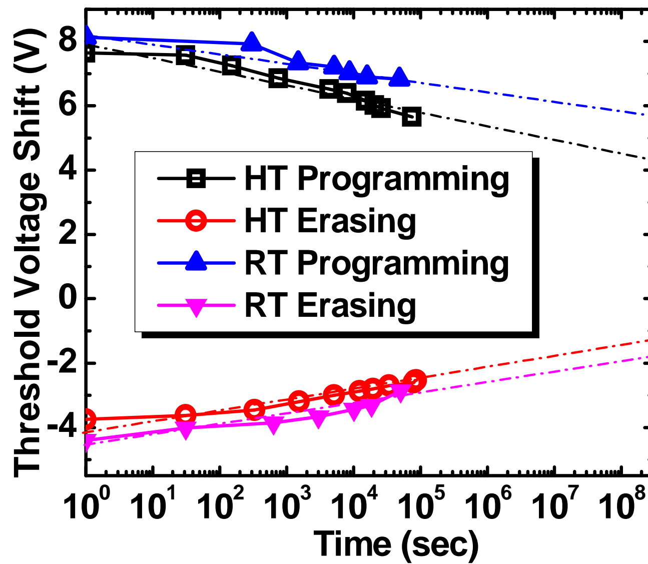

Fig. 5.7 Room-temperature and high-temperature retention properties of back-gated non-planar nano-floating gate memory showing robust high-temperature retention performance.

5.5 Summary

A combination of high-density NiSi nano-dots and scaled single SiNW is used to implement a non-planar nano-floating gate memory. The nano-dots layer with excellent size and location distribution provides a viable way to minimizing dot density variation effect while the non-planar nature of triangular-shaped Si NW

channel allows for more dots within single cell to further mitigate the issue in scaled devices. This back-gated device relies on fringing electric field to fulfill memory operations, i.e. programming and erasing, and shows good room-temperature and high-temperature retention performance. This research suggests that NC memory technology can be potentially scaled into 22 nm technology node by using non-planar device geometry. Memory properties could be further improved by optimizing device geometries and decreasing the non-planar channel size [36] in order for full exploration of the promised benefits. Large-scale statistical studies of cell performance deviation are required to extend our understanding on this hybrid device.

5.6 Acknowledgement

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Chapter 6 Conclusions and future work

1) Nanocrystal floating gate memory, as a potential replacement to traditional flash device, uses discrete charge storage nodes instead of continuous poly-Si film to improve device immunity to tunnel oxide leakage induced by process defects or stress and enhance the further scaling of flash cell; dot density fluctuation is identified as the most critical issue that limits the application of nanocrystal memory due to its influence on the device performance uniformity in array/chip level; Solutions to dot density variation problem are in great need in order to engineer the scaling process of this future flash cell candidate.

2) Si nanocrystal deposition is the key step in the process of nanocrystal floating gate memory fabrication and dot growth behavior needs to be fully understood and explored; directed self-assembly behavior of Si nanocrystals on patterned SiO_2 substrate is found within certain experimental condition window; modeling and calculation are carried out to reveal the dominant mechanism underlying the experimental results; different from common strain energy directed quantum dot nucleation on patterned substrate in S-K mode, the surface/interface energy directed strain-less nanocrystal growth on amorphous thermal oxide substrate in V-W mode is recognized, although it is relatively a weaker effect, which requires the growth parameters to be tuned more strictly for the effect to be observed.

3) NiSi nanocrystals of high density and supreme uniformity has been achieved by a gas source MBE based vapor-solid-solid process by using Disilane as Si source; Base upon the silicide nanocrystal layer, a nonvolatile memory device with engineered Al_2O_3/SiO_2 double-barrier gate stack has been fabricated and characterized; this

memory device exhibits large memory window, robust retention at both room temperature and elevated temperature of 85ºC; further device geometry optimization with thinner control oxide and varied Al_2O_3 thickness can be carried out to fully explore the advantages of double-barrier structure for nanocrystal memory applications.

4) Non-planar device has the advantage of superior scalability over planar counterparts; the idea of non-planarity is demonstrated for nanocrystal memory through fabrication and characterization of a proof-of-concept device based on triangular-shaped SiNW array; good programming, erasing, retention and endurance performance is observed; comparison of performance between planar and non-planar devices at the same technology node is required for future qualification of non-planar device; process optimization and large-scale statistical study are needed to further prove that dot density variation effect is alleviated in three-dimensional devices

5) As extended work, channel size scaling is carried out on the non-planar nanocrystal memory device; single triangular shaped nanowire channel with reduced dimension down to 40nm is obtained by anisotropic etching process and back-gated nanocrystal memory based on the nanowire channel is demonstrated; fringing electric field-based memory operation is conducted on this device with one-dimensional channel; memory effect is analyzed by both electrical characterization and qualitative simulation; For further scalability study, devices with varied channel size can be fabricated for systematic scaling trend analysis; device geometry and structure optimization (thinner buried oxide of SOI wafer; top-gated device) are a necessity for optimal memory performance.