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Formation of Porous Layers by Electrochemical Etching of Germanium and Gallium Arsenide for Cleave Engineered Layer Transfer (CELT) Application in High Efficiency Multi-Junction Solar Cells

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A thesis submitted in partial satisfaction

of the requirements for the degree of Master of Science

in Materials Science and Engineering

By

David Michael Fong

2012

ABSTRACT OF THE THESIS

Formation of Porous Layers by Electrochemical Etching of Germanium and Gallium Arsenide for Cleave Engineered Layer Transfer (CELT) Application in High Efficiency Multi-Junction Solar Cells

By

David Michael Fong

Masters of Science in Materials Science and Engineering

University of California, Los Angeles, 2012

Professor Mark S. Goorsky, Chair

This thesis investigates a method to reduce substrate costs of multi-junction solar cells by recycling handle wafers through Cleaved Engineered Layer Transfer (CELT) using porous Ge and GaAs. Multi-junction solar cells based on GaAs and Ge substrates are the most efficient photovoltaic devices with a world record efficiency of 43.5%, more than double that of common terrestrial solar cells. In order for multi-junction solar to expand to terrestrial power generation, significant reduction in device cost must be achieved; substrate costs represent up to 50% of the cell costs making substrate recycling an opportunity for significant cost reductions.

Ge and GaAs wafers are subjected to electrochemical etching with the goal of creating a porous layer that is suitable for epitaxial growth and Cleave Engineered Layer Transfer (CELT) for high efficiency III-V devices. Both n and p type Ge and GaAs were investigated with the doping concentration ranging from 10^{17}-10^{19} cm^{-3}. Electrolytes at various concentrations were tested including HCl, HF, and H_2SO_4. In addition, current profile, density, and etch time were changed to optimize porous layer formation. After electrochemical etching, samples were analyzed with a scanning electron microscope (SEM) to determine pore size, morphology, layer thickness, and substrate dissolution rate. Energy dispersive x-ray spectroscopy (EDS) was also used to find the chemical composition of the porous layer, and transmission electron microscopy (TEM) was used to determine crystallography of the porous layer. Finally, the effect of annealing on porous layer surface morphology and composition were investigated.

The results of this work showed that both n-Ge and p-GaAs yield inhomogeneous low-density pores that are not suitable for CELT. Heavily doped p-Ge (10^{18} cm^{-3} or greater) yields a uniform pore structure on the nm scale that potentially could be used in a layer transfer process. However, this porous layer includes a significant portion of germanium oxide (< 10 atomic % oxygen). Subsequent annealing in an atmospheric envi4ronment did not remove this oxide, though annealing in a reducing atmosphere such as hydrogen has not yet been investigated.

Etching of p-type GaAs in concentrated HF yielded nm sized porous layer that was completely devoid of any gallium content. This contradicts the claims made by Rojas et al.. who show a similar porous layer using the same etching parameters, but stated it was composed of stoichiometric GaAs without presenting any chemical composition data to support this assertion.

The most promising results were realized with n-GaAs doped between 1-4x10^{18} cm^{-3}. Uniform pore nucleation is achieved using 5% H_2SO_4 with a 300 mA/cm^2 current pulse for 1.4 s

followed by 20 mA/cm^2 for 1 hour. This profile creates primarily (111) oriented pores on the order of hundreds of nm in size. In addition, the electrochemical etching leaves a high density of pyramid shaped arsenic oxide structures on the surface, which are then removed by a 20 min dip in 17.5% HCl. After the HCl treatment, EDS showed the porous layer to be comprised of 3% O, 48% Ga, and 49% As by atomic percent, which could be suitable for high quality epitaxial growth to be carried out on the porous surface. Annealing of the GaAs porous layer at 450 °C for over 80 hours covered by a GaAs proximity cap showed minimal surface reorganization as well as a decrease in the layer's As content, which is due to the high vapor pressure of As as compared to Ga.

These results demonstrate that the electrochemical etching of n-GaAs can create a porous layer that could reduce the cost of high efficiency multi-junction solar cells through a CELT process. This was achieved with n^+-GaAs etched in sulfuric acid with a short duration high current pulse followed by a long duration low current pulse. Additionally a dip in hydrochloric acid is needed to remove arsenic oxide that forms on the surface. Furthermore this work shows that pores made in p-type GaAs with HF primarily consist of arsenic oxide and are not useable for a layer transfer application.

The thesis of David Michael Fong is approved.

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Suneel Kodambaka

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University of California, Los Angeles

2012

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Chapter 1: Introduction

1.1 Motivation

Multi-junction (MJ) solar cells show particular promise as a future clean renewable energy source due to their high efficiencies as compared to traditional photovoltaic technologies. Currently MJ solar cells have a world record efficiency of 43.5% as compared to about 20% for the best silicon and thin film photovoltaics [1]. This roughly doubling of efficiency means that there is less environmental impact in terms of material and land use to generate the same amount of power, as well as lower secondary costs such as installation. Currently however, the high cost to produce these cells is limiting their use to specialized space applications and is the primary barrier to widespread adoption of MJ photovoltaics.

MJ solar cells achieve higher efficiencies by stacking different band gap materials through epitaxial growth. The key to the success of this strategy is to select ideal band gaps in order to maximize the efficiency of converting the solar spectrum of photons into electricity. In the design, the top solar junction is the largest band gap material with the band gap decreasing to the smallest at the bottom junction. This structure allows low energy photons to pass through the larger band gap materials on the top of the device and be absorbed by the smaller band gap materials on the bottom of the device. This allows for the use of a greater portion of the solar spectrum and minimizes energy loss due to thermalization.

Typical MJ cells use three different active layers, or a triple-junction to absorb photons. Fabrication begins with a handle wafer that acts as the crystallographic template for epitaxial growth of the subsequent layers. In order to maximize efficiency the epitaxial layers must be high quality single crystal with minimal defects [2]. This is done by choosing materials that

have similar lattice parameters (within 1%), which minimizes the strain between the two materials and reduces the number of defects generated in the new layer. Figure 1 shows the band gaps and lattice parameters of III-V materials commonly used in MJ solar cells. One can see that Ge, GaInAs, and InGaP all have a similar lattice parameter and have different band gaps. These three materials can be grown lattice matched (LM) with minimal lattice strain to form a triple-junction photovoltaic cell starting with a Ge substrate as the initial epitaxial template. Another common triple-junction solar cell utilizes a GaAs initial substrate to grow an InGaP top layer followed by a GaAs middle layer, and finally an InGaAs bottom layer [3]. This growth scheme attempts to achieve more ideal band gap spacing by replacing the low band gap Ge cell (0.7 eV) with InGaAs (1.0 eV) at the expense of introducing strain into the final device layer. This is known as an inverted metamorphic (IMM) device since the top (high band gap) cell is grown first and the whole structure is inverted and transferred to a handle as shown in Figure 2.

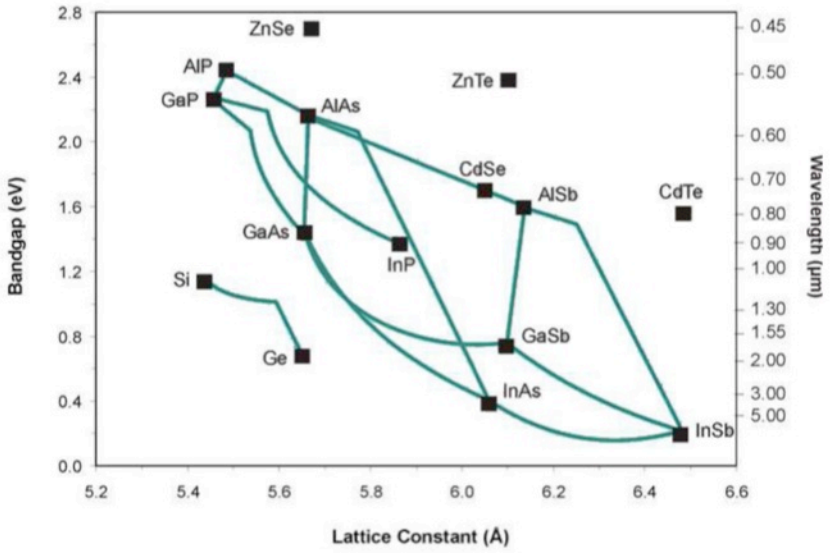


Figure 1: Lattice constant versus band gap for common materials in multi-junction solar cells. Not lattice matched materials of Ge/GaInAs/InGaP commonly used in triple junction cells. Data from Veeco. [4].

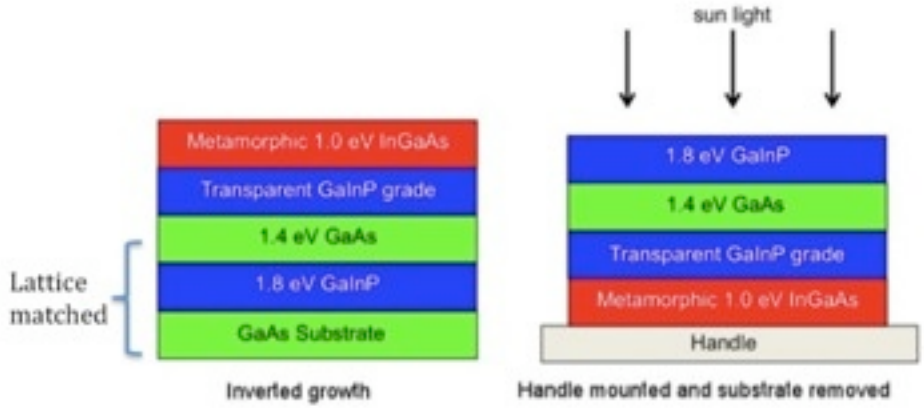


Figure 2: Left shows IMM cell grown on GaAs substrate. Right shows device transferred to handle wafer with GaAs substrate removed. Design from Spectrolab Inc. [3].

In both the LM and IMM solar cells the initial template substrate thickness range from is about 200 μm to 700 μm thick to provide mechanical stability during processing. However, in the IMM, device the initial GaAs substrate plays no role in the actual device performance and is completely removed through a polishing process. Likewise, in the LM device only 3-5 μm of Ge are needed for photo absorption with the excess Ge also removed through polishing. These initial substrate wafers represent about a third of the total device cost and provides an opportunity for significant cost reduction if these substrates can be reused rather than destroyed.

A CELT process using porous Si has been shown effective in the application of silicon on an insulator (SOI), and provides a template for how the cost of multi-junction solar cells can be reduced by the recycling template wafers [5]. To facilitate this process, electrochemical etching is used to create a mechanically weak porous layer on the substrate wafer surface. Epitaxial growth of Ge, in the case of the LM cell, and GaInP, in the case of the IMM cell, is then done on the porous substrate wafer. After this the standard cell epitaxy is performed, leaving the photovoltaic device on a porous substrate. The stack is then mounted to an inexpensive handle wafer and the device is split off at the mechanically weak the porous interface. This leaves the original substrate intact to go through the electrochemical etching again and have another device

grown on it. Figure 3 shows a hypothetical process flow for this layer transfer technique for a LM cell (IMM cell would have same process substituting GaAs for Ge and the IMM epitaxy). This layer transfer technique could allow twenty or more devices to be made from each substrate wafer versus the single device each wafer currently yields.

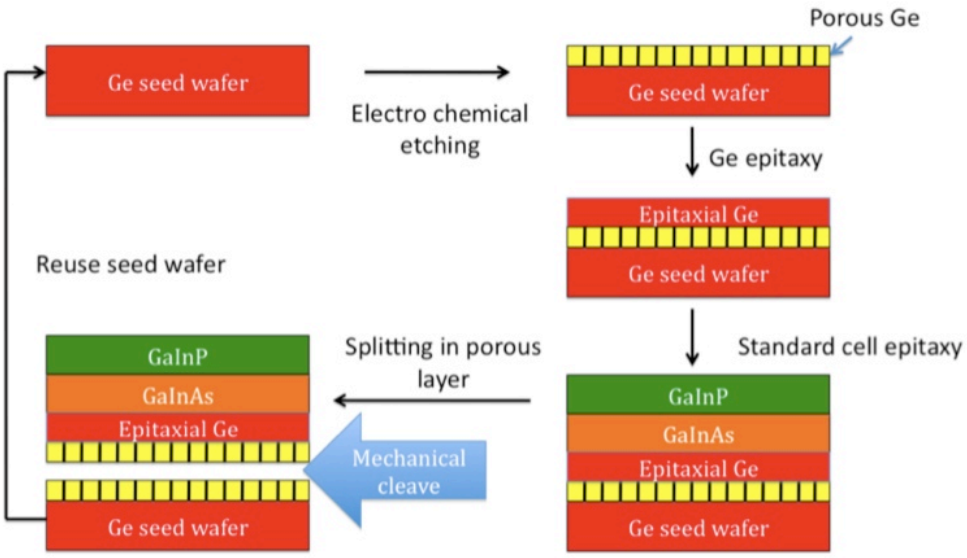


Figure 3: Schematic process flow for layer transfer technique for LM triple junction solar cell grown on porous Ge.

For this process to be successful a porous layer that is suitable for epitaxial growth and layer transfer must be generated. This means that the porous layer should be between 1-10 μm thick, have the mechanical behavior such that the layer is weak enough to split easily when the device needs to be transferred, but still strong enough to hold up to handling during subsequent epitaxial layer growth. Additionally, the surface must allow for high quality single crystal growth with minimal defect density. This requires the surface to be contaminant free, namely of oxides, and that the pore morphology be small (> 1μm) to allow the epi to coalesce into a solid surface during growth. Finally, this must be accomplished in an inexpensive way that maintains the substrate so that recycling savings can be realized.

Due to the above mentioned constraints, electrochemical etching followed by annealing is chosen as an inexpensive way to achieve the required porous layer. This thesis investigates the formation of porous layers in both Ge and GaAs by electrochemical etching as well as the effects of subsequent annealing on the layer. Previous work has been done on electrochemical etching to create porous semiconductor materials. Rojas et al., have looked at porous Ge for layer transfer application [6-9]. Additionally, Langa et al. have investigated porous semiconductors, specifically pore formation in GaAs during electrochemical etching [10]. These studies though, have been incomplete in characterizing whether those porous layers are suitable for high quality epitaxial growth. Specifically, they have not adequately investigated surface contamination and chemical composition of the porous layers. This work looks to more thoroughly characterize pore formation in Ge and GaAs with an emphasis on achieving a single crystal contaminate free porous layer.

Chapter 2: Background and Theory

2.1 Electrochemical Etching Theory

Electrochemical etching uses an acid electrolyte that acts as the cathode contact to the semiconductor surface on which the porous layer will be created. A current is then passed through the semiconductor to facilitate the etching process. Figure 4 shows the configuration of the double cell electrochemical etcher used in this work, where double cell refers to the fact that both the anode and the cathode of the semiconductor are formed by the contact with the electrolyte. In addition, a single cell etcher was used in which only the cathode contact is made with the electrolyte, while the non-etched side uses a metal contact as shown in Figure 5.

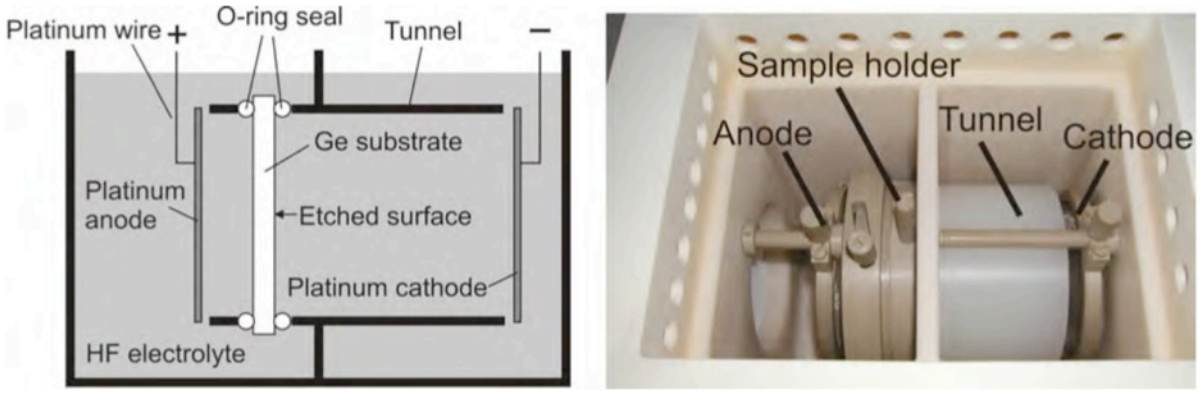


Figure 4: Schematic and picture of double cell electrochemical etcher used in this work.

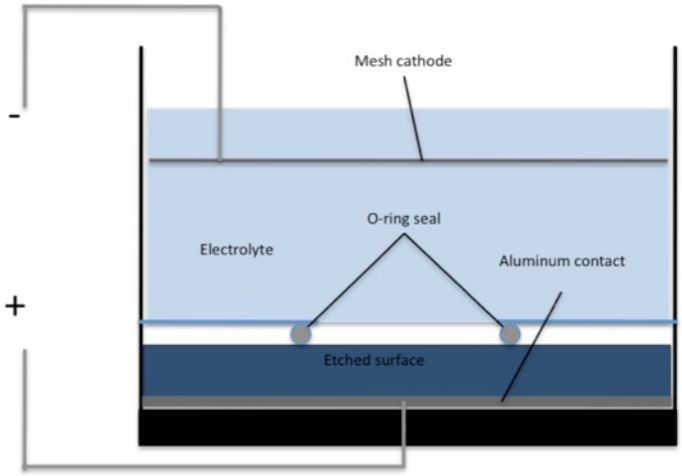


Figure 5: Schematic diagram of single cell electrochemical etcher used in this work.

During the etching process the voltage difference applied across the semiconductor generates a current in which electrons in the semiconductor migrate towards the anode, while holes diffuse towards the cathode at the etching surface. When these holes reach the surface they weaken the bonds of the surface atoms to the substrate and allow ionized electrolyte species to attack the surface atom and remove it. The specific mechanisms of the etching process are complex and depend on the substrate being etched, Ge or GaAs, as well as the electrolyte used. In addition there are numerous different pathways for atoms to be removed, as well as the possibility of oxide formation during the etching process. Figure 6 shows one of the many etching mechanisms for Ge in a HF electrolyte [11]. This six step process starts with hydrogen passivating the Ge surface due to immersion in HF. Step one begins with an HF_2^- ion in the electrolyte reacting with a Ge atom in the presence of a hole from the substrate. This enables the nucleophilic substitution of a hydrogen atom by a fluorine atom. In steps two and three, the second hydrogen atom is replaced by a fluorine atom through the ejection of an electron, producing H_2. Steps four and five show the HF_2^- ion attack the substrate bonds, removing the Ge atom from the surface. This gives an overall dissolution equation of:

$$Ge + 4HF_2^- + h^+ \Rightarrow GeF_6^{-2} + 2HF + H_2 + e^-$$

Pores then form since holes are more likely to reach sites where atoms have already been removed because of the shorter diffusion distance they must travel. There are several other pathways Ge can be removed from the surface. However, for the purpose of this paper it is sufficient to note that the electrolyte type and concentration as well as the current profile greatly affect the etching process results.

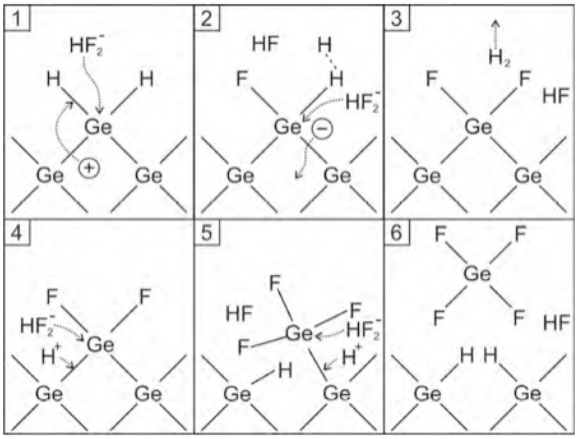


Figure 6: One possible etching mechanism for Ge in highly concentrated HF. Figure taken from [11].

2.1.2 Porous Ge Background

A review of the literature on porous Ge shows that a moderate amount of work has gone into the study of pore formation in both n and p type substrates, though not necessarily towards a CELT application. Fang et al. have studied pore formation of both p-type and n-type Ge focusing primarily on heavily doped n-type etched in HCl [12]. They found that uniform high-density pore nucleation is quite difficult, as compared to silicon, with low-density large pores being formed on the order of 10s of μm^2. An etching profile of 5% HCl, T=24 °C, 120 min ramped current 0-30 mA/cm^2 with n-type Ge yielded high density of randomly distributed pores, but the pore size was too large (roughly 20 μm^2) for use in the proposed layer transfer processes [12].

Rojas et al. has extensively studied pore formation in heavily doped p-type Ge etched in highly concentrated HF [6-9]. Rojas has created layers with nm sized pores using HF electrolytes with concentrations between 25-49%, current densities between 1-50 mA/cm^2, and both constant current profiles and alternating current pulses (positive to negative periodically while maintaining constant current amplitude). The morphology and mechanical properties of these porous layers appear to be suitable for CELT. However, Rojas does not give data for the porous layer composition or crystallography, merely stating that the layer is porous Ge. In order to use this material for a layer transfer process it must be confirmed that the porous layer is contaminant free and retains the single crystal nature of the original substrate.

2.1.3 Porous GaAs Background

Much like the literature on porous Ge, the literature on porous GaAs is incomplete in the characterization of the chemical composition and crystallography of the layer. One of the few papers to present data on chemical composition shows that, for highly doped n-type GaAs etched in a 1:4 HF:EtOH solution, there is strong tendency to generate oxide in the porous layer [13]. The oxide formation as well as the preferential etching of Ga leaves a layer that is not suitable for high quality epitaxial growth, though Ali et al. did show that optimal current profiles can somewhat minimize these negative effects. Beji et al. claim to generate nanometer sized pores in highly doped (greater than 10^{18} cm^{-3}) p-type GaAs in a 1:1 solution of HF:EtOH [14]. However, they do not present any data to show that they have avoided the oxide formation observed by Ali. Rojas et al. also claim to generate nanometer sized porous layers using p-type GaAs etched in HF and once again there is no data presented on the porous layer's chemical composition [15]. They simply state that the layer is comprised of GaAs. Langa et al. have demonstrated (111) oriented μm sized pores in n-type GaAs using a short high-current pulse followed by a long low-

current pulse in H_2SO_4 [16]. The SEM images presented in the work give a small field of view of the porous layer, making it difficult to assess the uniformity over a large region of the sample which is important for CELT technologies. In addition, there is no data presented on the chemical composition of the porous layer, making it uncertain as to whether it is suitable for a layer transfer application. In light of the fact that Ali et al. have shown that electrochemical etching of GaAs tends to generate significant oxide in the porous layer, any study of porous GaAs for CELT applications is incomplete without quantitative chemical analysis.

2.2 Annealing

In layer transfer applications using porous Si, an annealing step is often used before the device layer is grown on the porous surface [5]. This step is used to close up the pores and create a smoother and flatter surface for future growth. Figure 7 shows work done by Yonehara and Sakaguchi where porous Si is annealed in a H_2 atmosphere at 1100 °C . After annealing the top of the porous layer has coalesced into a smooth surface driven by the lower overall surface energy this configuration represents. Annealing can also have the added benefit of removing any surface contaminates such as carbon or oxide if done under a reducing atmosphere like H_2. Rojas et al. have examined annealing porous Ge under various atmospheres including H_2, but have not had success creating a layer capable of supporting high quality epitaxial growth [11]. No work appears to have been done on annealing of porous GaAs, though one would expect it could have similar results to that of porous Si.

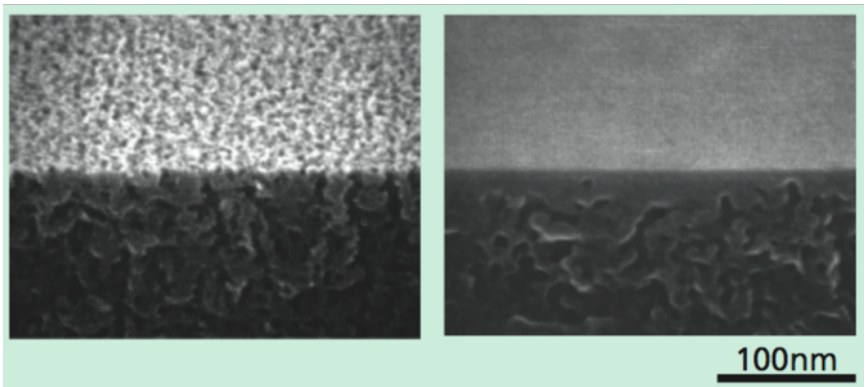


Figure 7: Left shows porous Si before anneal and right after anneal at 1100 °C. Figure taken from [5].

2.3 Characterization

2.3.1 Scanning Electron Microscopy and Energy Dispersive Spectrometry

In this study a Nova Nano SEM 230 was used to characterize pore size, surface morphology, layer thickness, and substrate dissolution. All images were taken with a 10 kV electron beam and secondary electron detector. The SEM was also used to analyze chemical composition of the porous layer via EDS. This technique uses an electron beam of a known energy to bombard the sample, generating characteristic x-rays from the material. The energy and intensity of the resulting x-ray spectrum is measured to determine the chemical composition. These x-rays are 'characteristic' because their energy is equal to the difference between electron orbital shells in the material, and are generated when an excited core shell electron relaxes to its ground state, emitting an x-ray.

When using EDS care must be taken that the x-ray signal is generated from the porous layer and not from the substrate beneath. The volume that x-ray signal is emitted from can be characterized by a production radius $R_{production}$, which can be modeled empirically by the following equation:

$$R_{production}(\mu m) = \frac{0.064\left(E_0^{1.68} - E_c^{1.68}\right)}{\rho}$$

where E_0 is the electron beam energy, E_c is the energy of the characteristic x-ray, and ρ is the density of the porous layer. A 5 kV beam is chosen to have enough energy to excited l line x-rays and to minimize the production volume. Assuming a minimum porous layer density of 10% of the original substrate, this gives an $R_{production}$ of 1.6 μm and 1.7 μm for Ge and GaAs respectively. X-ray data is automatically analyzed by the SEM software to give chemical composition.

2.3.2 Transition Electron Microcopy

A Titan 80-300 kV S/TEM was used to take higher resolution images then are achievable using SEM and to generate diffraction patters to determine the crystallinity of the porous layer. TEM samples were prepared using a focused ion beam (FIB) to mill out a cross-section of the porous layer from the plan view. A platinum cap was used to protect the TEM samples from the ion beam. Care was taken to insure that TEM data was taken far enough away from the platinum cap to avoid contamination.

Chapter 3: Experiment

3.1 Ge etching

Both n-type and p-type Ge was etched to investigate porous layer formation. All samples were (001) oriented with the p-type samples doped between 5-9x10^{18} cm^{-3} and the n-type wafers doped between 1-5x$10^{18}$$cm^{-3}$. The electrolytes used were HF, 40-49% concentration, and HCl, 5% concentration, with the experiments using HF done in a double cell etcher and those using HCl done in a single cell etcher. Prior to etching all samples were rinsed with acetone, IPA, methanol, DI water, and then dried with a N_2 gun. Following etching samples were thoroughly rinsed in DI water and then dried with a N_2 gun. Samples were then analyzed using an SEM to determine pore morphology and chemical composition of the porous layer. All EDS measurements were taken at 5 kV to insure data came only from the porous layer.

3.2 GaAs etching

For (001) GaAs, p-type and n-type wafers were etched using a single cell electrochemical etcher. P-type wafers were doped between 5-9x$10^{18}$$cm^{-3}$, while n-type wafers were doped 1-5x$10^{18}$$cm^{-3}$. Electrolytes investigated were 45% HF, 49% HF:EtOH 1:2 ratio, 5-17% HCl, and 5% H_2SO_4. All cleaning, drying, and SEM procedures matched those used for Ge. For oxide removal samples were dipped in a 17.5% HCl solution for 15 min following electrochemical etching.

3.3 GaAs Annealing

All annealing was done on a hotplate under a fume hood at 450 °C. A GaAs proximity cap was placed over each sample to minimize oxidation and out-gassing of As. Samples were annealed up to 87 hours to see the effect on surface morphology and layer composition.

Chapter 4: Results and Discussion

4.1 Ge Etching

4.1.1 P-type Ge

To generate a porous layer, p-type Ge is etched in highly concentrated HF using a double cell electrochemical etcher. Porous layers thicknesses in the range of hundreds of nanometers to up to a micron were generated using various current profiles in 49% HF. Figure 8 shows typical results for these porous layers, where the left picture shows a sample which has been etched at a constant current density of 20 mA/cm^2 for 3 hours while the right has had the current alternate from positive to negative for 18 and 6 seconds respectively at 20 mA/cm^2 for 3 hours. Both samples show nanometer sized pores and layer thickness in the micron range and, as such, appears promising for layer transfer application from a morphology standpoint. However, the EDS data in Figure 9 shows that the porous layer includes a significant portion of oxygen, which is not suitable for high quality epitaxial growth. To estimate the oxygen concentration before the porous layer is exposed to atmosphere and native oxide growth begins, the best fit line from data in Figure 9 was extrapolated to t=0. This gives an atomic percent oxygen of 17 and 10 for the constant current and alternating current samples respectively, demonstrating that oxide formation is occurring during the etching process. These results match those of Rojas et al. in terms of pore size and morphology, but show definitively that etching of p-type Ge in HF yields a porous layer that is made up of a significant portion of Ge oxide with more than 10 atomic percent oxygen [6-9].

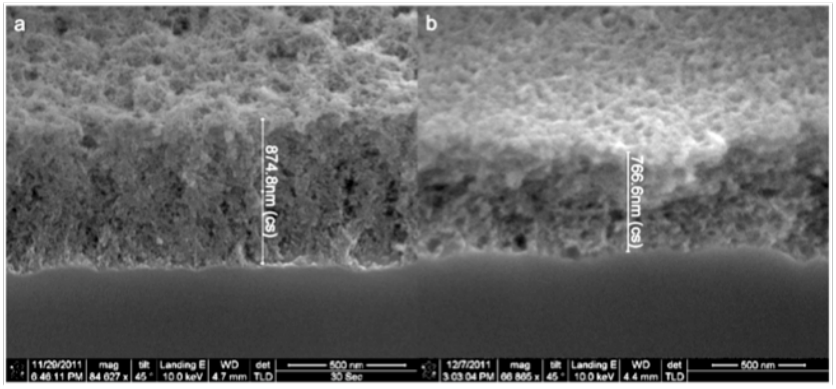


Figure 8: Cross-section view of Ge etched in 49% HF at 20 mA/cm^2 for a duration of 3 hours. Left is done at constant current, while right current alternates from the positive to the negative direction for 18 s and 6 s respectively.

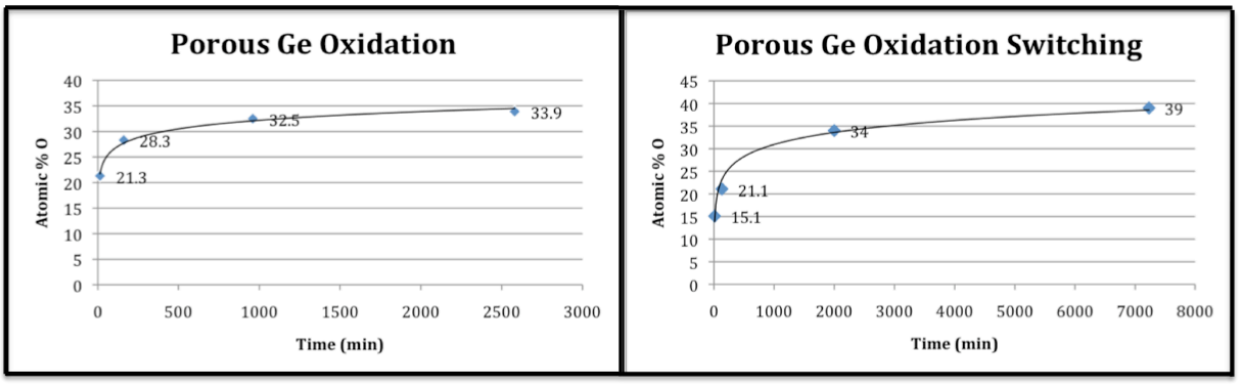


Figure 9: Oxygen concentration over time for porous Ge samples in Figure 8. Extrapolating the best fit line to t=o gives oxygen levels of 17 and 10 percent for constant current and switching current respectively. This extrapolation gives the amount of oxide generated during the etching process.

4.1.2 N-type Ge

Etching of n-type Ge was done using HCl in a single cell electrochemical etcher. The results in general gave large low density pores along with the formation of germanium oxide spheres covering the surface. Figure 10 shows the results for n-type Ge with a linearly ramped current from 0-20 mA/cm^2 over 99 min in 5% HCl. Pore size is large, between 20-30 μm^2, with a low and non-uniform density. There is also a very high electro polishing rate of 800 nm/min, which would limit the material savings of the layer transfer process even if ideal pores could be grown. Lastly, EDS data reveals that the spheres shown on the surface in Figure 9 are made up

of GeO_2. These results are typical throughout n-type Ge with variations in current density, etch time, and electrolyte concentration doing little to improve the porous layer.

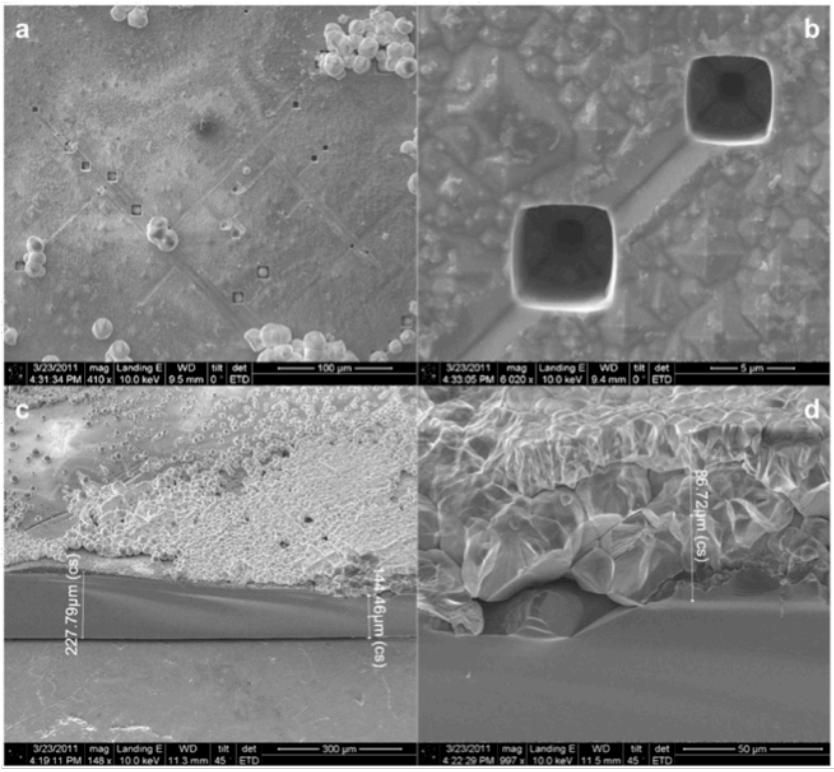


Figure 10: SEM images for n-Ge etched in 5% HCl for 99 min with current linearly ramped from 0-20 mA/cm^2. (a) shows low density of pores along with formation of oxide spheres on the surface. (b) shows large pore size of roughly 20 µm^2. (c) Shows cross-section view of high electro polishing of 87 µm. (d) shows cross-section of oxide formation.

Abrasion of the surface by 1 µm Al_2O_3 particles was used in an attempt to increase pore density. Figure 11 shows the results achieved with linearly ramped current from 0-30 mA/cm^2 over 120 min in 5% HCl. Insert (a) of Figure 11 shows that pore density does increase as compared to insert (a) of Figure 10. However, this increase is not enough for use in a layer transfer process. Pores are much too large with sizes on the order of 10s of µm^2 compared to the 10-100 nm^2 sized pores needed for layer transfer application. In addition, electro-polishing is quite high, at a rate of 1.4 µm/min as shown by insert (c) of Figure 11, which is also unsuitable for a material saving processes. Finally, the Ge oxide spheres built up on the surface would

prevent high quality epitaxial growth both as an oxide surface contaminate and from increased surface roughness. The oxide contamination can be removed through an HF dip that will preferentially etch the oxide, but the surface left behind has a high roughness that is detrimental to epitaxial growth. Figure 12 shows the results of 15% HF dip for 3 min on the Ge oxide spheres. Note that the removal of the Ge oxide spheres leaves a highly roughened surface that is undesirable for the proposed process in this paper.

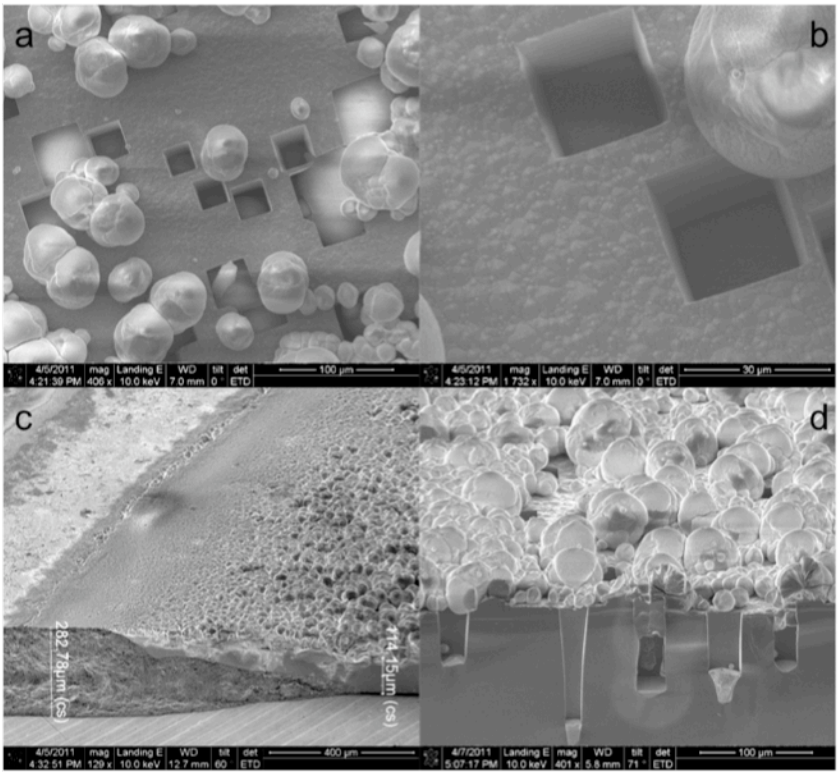


Figure 11: SEM images of n-Ge abraded by 1 µm Al_2O_3 particles etched in 5% HCl for 120 min with linearly ramped current from 0-30 mA/cm^2. (a) and (b) show plan view of large square pores along with Ge oxide spheres on the surface. (c) cross-section of high electro polishing of 169 µm. (d) shows cross-section of oxide spheres and pore structure.

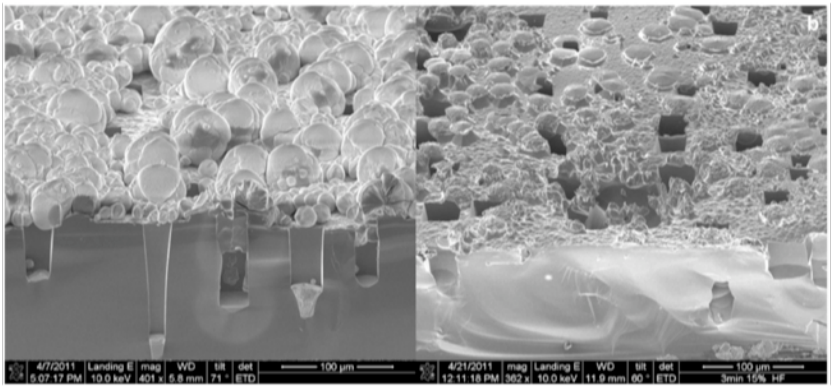


Figure 12: Cross-section SEM images of Figure 11 before (left) and after (right) 3 min dip in 15% HF. Note the increased roughness of the surface after oxide spheres are removed.

To summarize, the results for electrochemical etching of Ge are not favorable for application in a layer transfer process. P-type Ge etched in HF does yield nanometer sized pores that are uniformly nucleated at a high density as shown by Rojas et al.. However, further investigation of the layers' chemical composition reveals that it is always made up of greater than 10 atomic percent oxygen, which is detrimental to epitaxial growth. Etching of n-type Ge gives large low density pores along with a rough surface from As oxide sphere formation that is also not suitable for a layer transfer application.

4.2 GaAs Etching

4.2.1 P-type GaAs

Both Rojas et al. and Beji et al. claim to have created nanometer sized pores in p-type GaAs using electrochemical etching in a HF electrolyte [14,15]. The SEM images they show in their work support these claims in terms of layer morphology and look promising for potential application in a layer transfer process. However, neither work presents quantitative data on the chemical composition of the porous layer, so the single crystal, stoichiometric nature of the layers cannot be determined. To investigate this, p-type GaAs doped between 1.1-4.2x10^{19} cm^{-3}

was etched in a single cell etcher with parameters matching those described by Rojas and Beji. Figure 13 shows SEM images for GaAs etched at a current density of 1 mA/cm^2 for 15 min in 45% HF. These images match those shown by Rojas, specifically with the triangle features seen where the substrate and the porous layer meet. EDS data of the etched layer is given in Figure 14, which shows that layer is primarily composed of As and O with only 2 atomic percent Ga left. In addition, TEM data was taken from the cross-section of the etched layer to determine its crystallinity. Figure 15 shows the TEM diffraction pattern from the etched layer. The faint and broad rings in the left insert indicate that the layer is no longer single crystal, and has become highly disordered polycrystalline structure. The insert on the right has the GaAs substrate diffraction pattern overlaid showing that the ring spacing of the layer does not match that of the substrate. This supports the EDS data that the layer is no longer GaAs and, instead, consists of As oxide. Various combinations of current density, etch time, and HF concentration were investigated for the p-type GaAs and they all showed similar results of an etched layer composed almost exclusively of As oxide.

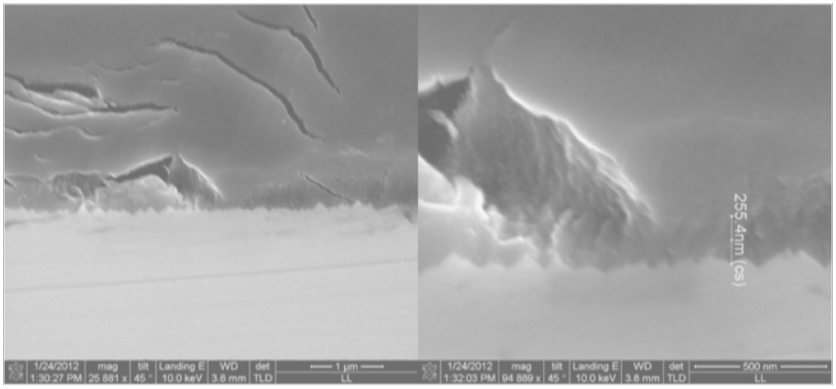
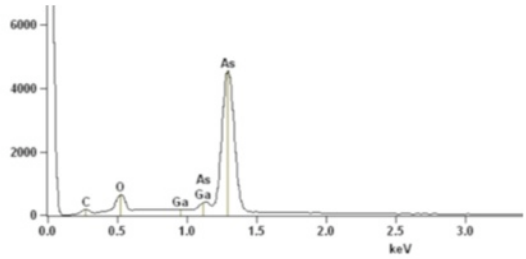


Figure 13: SEM cross-section of p-type GaAs etched in 45% HF for 1 min with a current density of 1 mA/cm^2.



Quantitative Results for: David Fong(6)

Element Line	Net Counts	Int. Cps/nA	Weight %	Weight % Error	Atom %
C K	756	39.375	1.65	+/- 0.14	8.44
O K	3848	200.417	3.60	+/- 0.11	13.80
Ga L	865	45.052	1.74	+/- 0.27	1.53
As L	45639	2377.03	93.01	+/- 0.68	76.23
Total			100.00		100.00

Figure 14: EDS data from Figure 13 showing that the etched layer is primarily made of As oxide with atomic composition of 8% C, 14% O, 2% Ga, and 76% As.

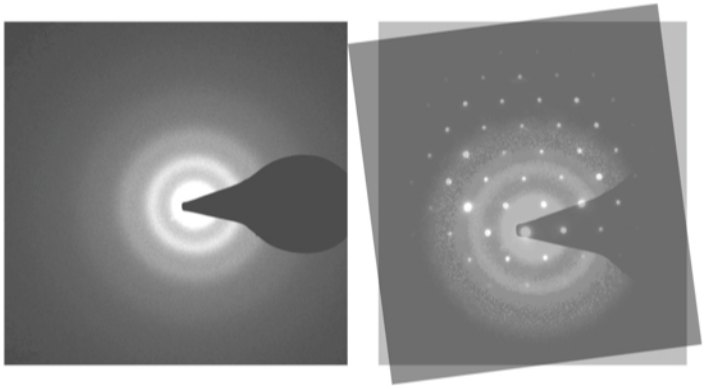


Figure 15: TEM diffraction pattern from etched layer in Figure 13. Left is layer diffraction pattern. Broad rings indicate low order polycrystalline structure. Right is layer diffraction pattern overlaid with substrate diffraction pattern. The fact that the ring spacing does not match substrate spacing indicates that etched layer is no longer Ge.

Chemical composition of the porous layer for p-type GaAs etched using parameters described by Beji et al. was also undertaken [14]. The primary difference in etching parameters from those described in the previous paragraph is a change in the electrolyte from highly concentrated HF to an HF:EtOH 1:2 by volume mixture. Figure 16 shows SEM images of p-type GaAs etched at 24 mA/cm^2 in 49% HF:EtOH 1:2 for 72 s. From a morphology standpoint, this porous layer looks very favorable for layer transfer application. Pore size is on the nanometer scale and pore distribution is high in density and uniform. However, EDS data in

Figure 17 shows that the layer is completely made up of As oxide, making it unsuitable for epitaxial growth. The results for etching p-type GaAs in HF based electrolytes shows a strong preferential etching of Ga over As leaving porous layers that are primarily comprised of As oxide. The EDS data from these experiments provide quantitative evidence that the porous layers obtained by Rojas and Beji are actually disordered polycrystalline As oxide, and not single crystal GaAs.

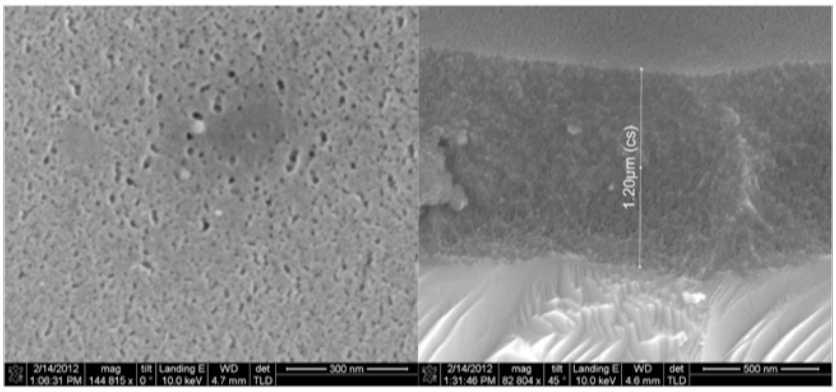
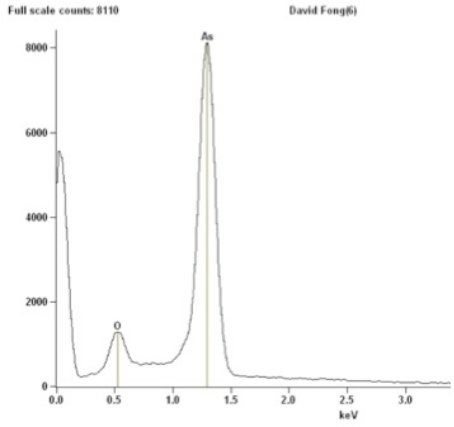


Figure 16: SEM images of p-type GaAs etched at 24 mA/cm^2 in 49% HF:EtOH 1:2 for 72s. Left image shows plan view. Right image shows cross-section.



Quantitative Results for: David Fong(6)

Element Line	Net Counts	Int. Cps/nA	Weight %	Weight % Error	Atom %
O K	13979	56.937	4.74	+/- 0.11	18.89
As L	128752	524.407	95.26	+/- 0.57	81.11
Total			100.00		100.00

Figure 17: EDS data of sample in Figure 16. Chemical composition is 19% O and 81% As

4.2.2 N-type GaAs

Etching of n-type GaAs was studied extensively based on the previous success our group had creating porous InP, another III-V semiconductor, using electrochemical etching in HCl [17,18]. Etching was done in a single cell electrochemical etcher in 5% HCl with a current density of 120 mA/cm^2 for 120 s. The result of this etching is shown in Figure 18 for a wafer doped 1.2x10^{18} cm^{-3}. Pores are randomly nucleated with a low density and are sized on the order of 100's μm^2, making it unsuitable for layer transfer application. It was found that pore density decreased as doping decreased with almost no pores found at doping levels below 10^{17} cm^{-3}. This contrasts sharply with our results for InP where a uniform high density porous layer is formed, shown in Figure 19, using the same etching parameters.

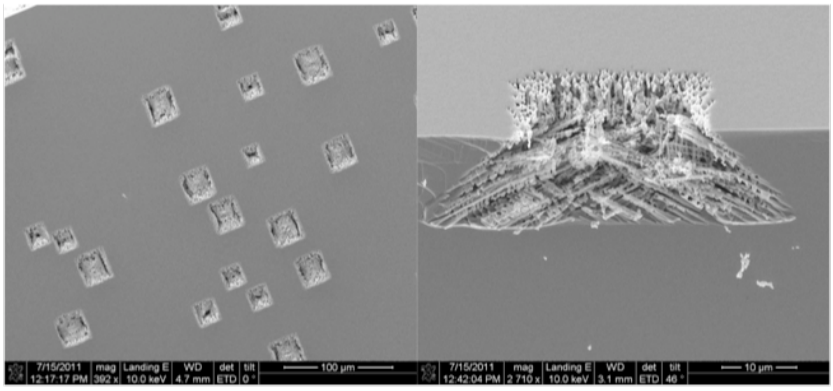


Figure 18: n-type GaAs etched in 5% HCl at 25 mA/cm^2 for 120 s. Left shows plan view and right shows cross-section.

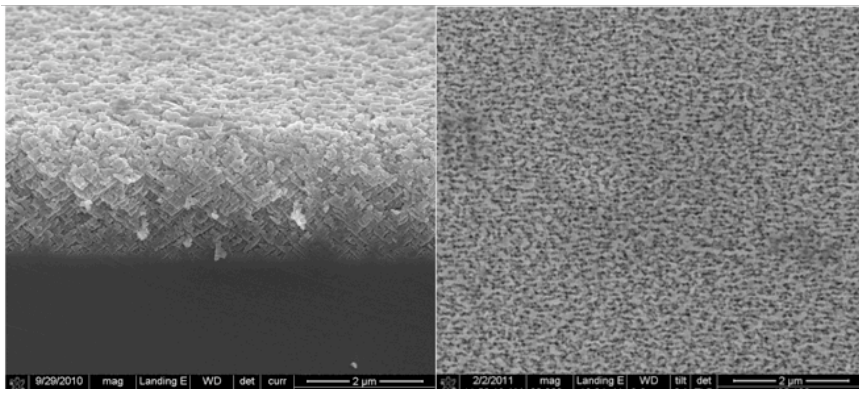


Figure 19: n-type InP etched in 5% HCl at 25 mA/cm^2 for 120 s. Left shows angled image with both plan view and cross-section components; right shows plan view [17].

Langa et al. has shown higher density pore nucleation can be achieved using sulfuric acid, H_2SO_4 with highly doped n-type wafers and an optimized current profile [10]. To investigate this n-type samples with doping between 1-5x10^{18} cm^{-3} were etched in 5% H_2SO_4 under various current profiles. Figure 20 shows the SEM images for a number of different samples. Starting with insert (a) one sees that a short high current pulse of 300 mA/cm^2 for 2 s gives low density inhomogeneous square pores with sizes on the order of 10 µm^2. These results are similar to those shown in Figure 18 using HCl as the electrolyte. To increase the density and uniformity of the pores a long low current etching period is added directly after the short high current pulse. Inserts (b), (c), and (d) show samples etched at 300 mA/cm^2 for 1.4 s followed by 20 mA/cm^2 for 225s, 60 min, and 105 min respectively. The plan view images in Figure 20 show that the low current etching step gives a uniform high density of roughly 1 µm^2 sized pores. In addition, the plan view images of (c) and (d) show pyramidal type structures that were not present when only the high current etching was used. It should be noted that insert (b) also had pyramidal structures on the surface, but was further processed to remove these features, the details of which will be explained in a later section of this paper. To summarize the results of

Figure 20, a high current pulse followed by a low current etch is necessary for uniform pore nucleation as both high and low current by themselves produce results comparable to insert (a).

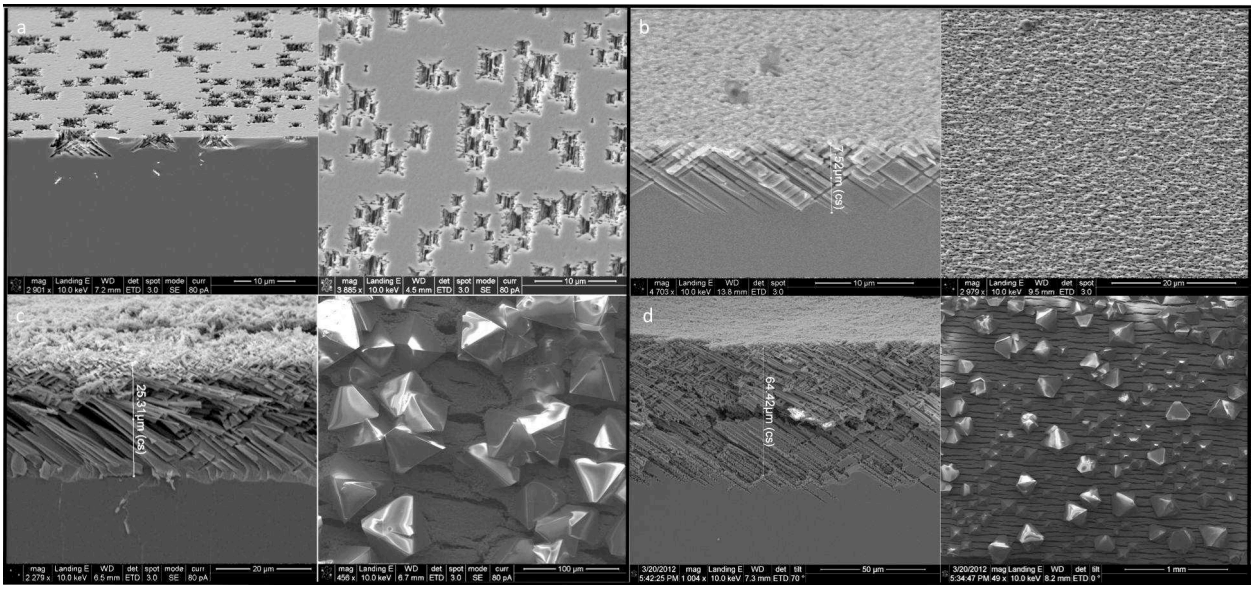


Figure 20: Etching of n-type GaAs in 5% H_2SO_4 under various current profiles and times. Images on the left show the cross-section view of the porous layer, while the images on the right show the plan view. (a) 300 mA/cm^2 for 2s. (b) 300 mA/cm^2 1.4s, 20 mA/cm^2 1 225s. (c) 300 mA/cm^2 1.4s, 20 mA/cm^2 60 min. (d) 300 mA/cm^2 1.4s, 20 mA/cm^2 105 min.

Further examination of the cross-section images in Figure 20 shows that as the duration of the low current etch increases, the porous layer thickness also increases. These pores are primarily (111) type in orientation, which can be clearly seen in the cross-section images of inserts (c) and (d). In addition to increasing the porous layer thickness, longer etching times introduces large horizontal running cracks shown in the plan view images (c) and (d). Similar cracking has been observed in the literature for highly porous silicon, above 80%, and is attributed to the surface tension force exerted by the liquid inside the pores during the drying process as it goes from a liquid to a gas phase [19,20]. These large cracks are undesirable for a layer transfer process and should be minimized. This can be accomplished through three primary means. The first means is reduction in the porosity of the layer as shown by the reduction of cracks in the plan view of insert (b) as compared to (c) or (d). The second is to use

a low surface tension liquid for drying such as pentane, which will reduce the force on the porous layer as the liquid evaporates. The third is to use a super critical dryer, which dries the porous layer at a high enough pressure so there is no longer a liquid gas interface. The success of these techniques in porous Si as well as the absence of cracking in insert (b) shows that cracking is not a significant obstacle for layer transfer in n-type GaAs.

The (111) oriented pores structure shown in Figure 20 matches the results obtained by Langa et al. [10]. However, their work only shows cross-section images with a scale and view similar to insert (c). In addition there are no reference to pyramidal structures on the surface or quantitative data on chemical composition to prove the porous layer is still stoichiometric GaAs. EDS analysis of the porous layer shows that the pyramidal structures are composed of As oxide and that the porous layer beneath does not maintain a perfect one to one ratio of Ga to As. Figure 21 shows the EDS data taken from sample (b) in Figure 20. The chemical composition presented here is representative of all the n-type GaAs samples etched in H_2SO_4 with a high current pulse followed by a longer low current etching. Insert (a) of Figure 21 shows that excluding the pyramidal structures the porous layer is primarily GaAs with a 3 atomic percent O and a slight preferential etch of Ga over As. Insert (c) clearly shows that the pyramidal structures are As oxide that appear to be forming during the low current etch by the fact that insert (a) of Figure 20 shows no surface pyramids.

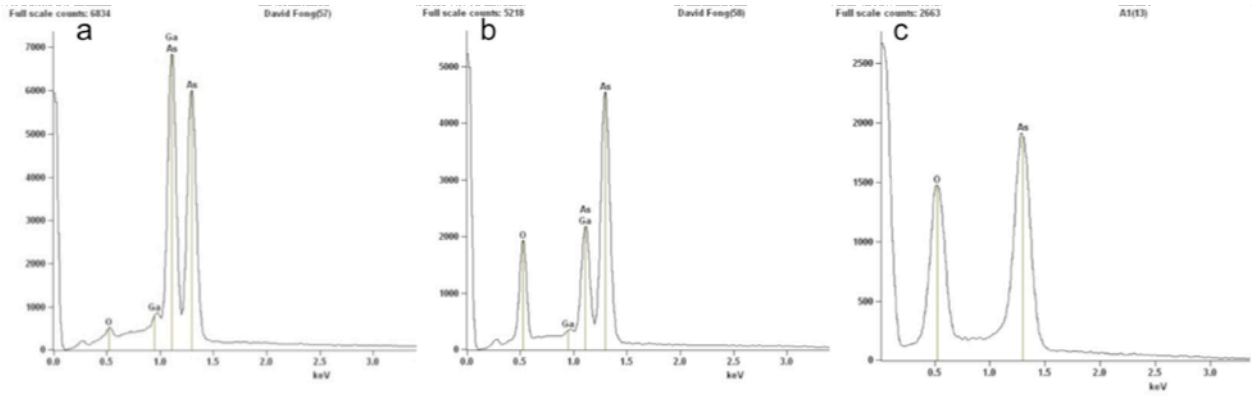


Figure 21: EDS data from sample (b) in Figure 20 giving atomic percent composition. (a) shows chemical composition of the porous layer without As oxide pyramids (3% O, 47% Ga, 50% As). (b) shows chemical composition of the average porous layer surface (29% O, 20% Ga, 51% As). (c) shows chemical composition of the As oxide pyramids (58% O, 42% As) .

The porous layers generated in Figure 20 look promising for layer transfer applications aside from the As oxide surface structures. To address this obstacle samples were dipped in 17.5% HCl, which has been shown to etch As and Ga native oxides while not etching GaAs [21]. 15 minutes was found to be sufficient to remove all pyramid structures as shown in Figure 22 and maintain the original porous layer (note insert (b) in Figure 20 was treated to the same process). EDS analysis after HCl dip confirms that the layer is stoichiometric GaAs with 3 atomic percent O, likely due to native oxide growth during the time the sample is removed from the HCl and taken to the SEM for analysis. N-type GaAs was also electrochemically etched in HCl with pulsed current in the hopes of removing the oxide pyramids without an additional processing step. Figure 23 shows the results for both 5% and 17.5% HCl. Pyramid formation is significantly less, particularly in the more highly concentrated HCl, and pore morphology matches that obtained with H_2SO_4. However, as Figure 24 shows, HCl has a stronger preferential etch of Ga than H_2SO_4 with 17.5% HCl giving almost a two to one ratio of As to Ga

in the porous layer. Based on this greater etch rate of Ga in HCl, H_2SO_4 etching shown in Figure 20 followed by an HCl dip to remove oxide is deemed to give the most favorable results.

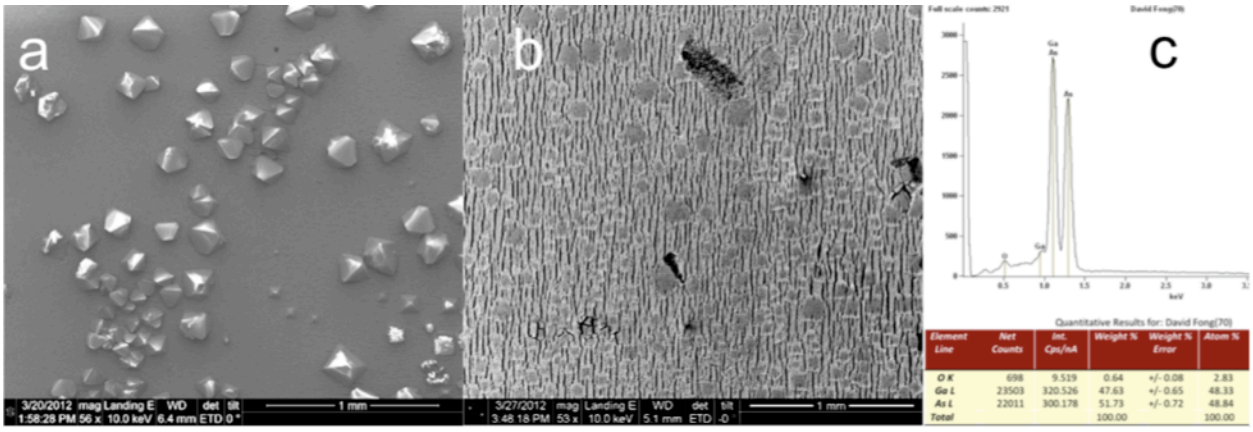


Figure 22: n-type GaAs etched in 5% H_2SO_4 300 mA/cm^2 1.4s, 20 mA/cm^2 60 min. (a) as etched. (b) 15 min dip in 17.5% HCl. (c) EDS data of (b) shows atomic composition of 3% O, 48% Ga, 49% As.

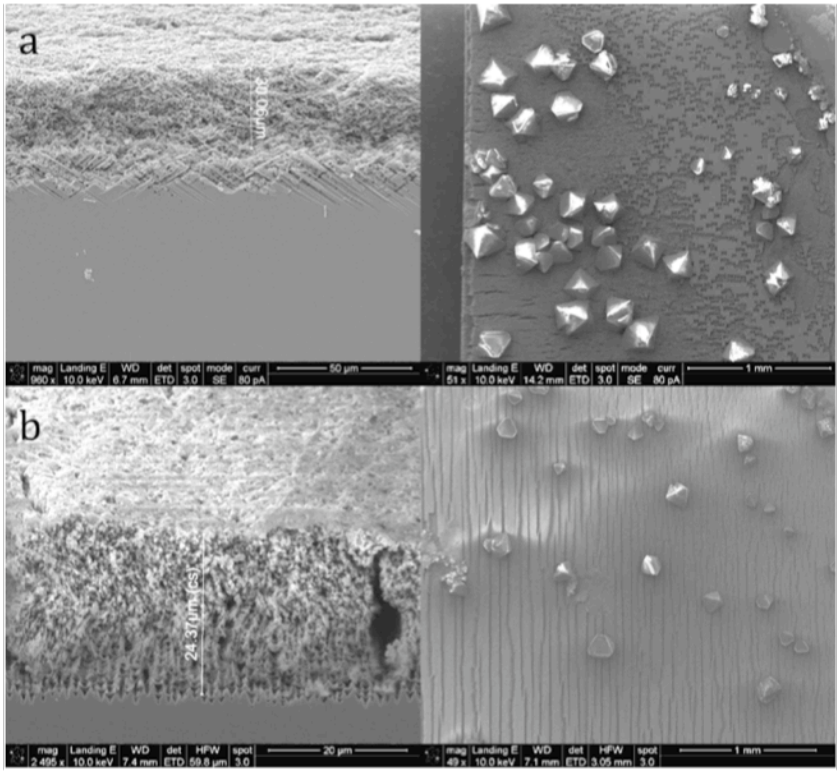
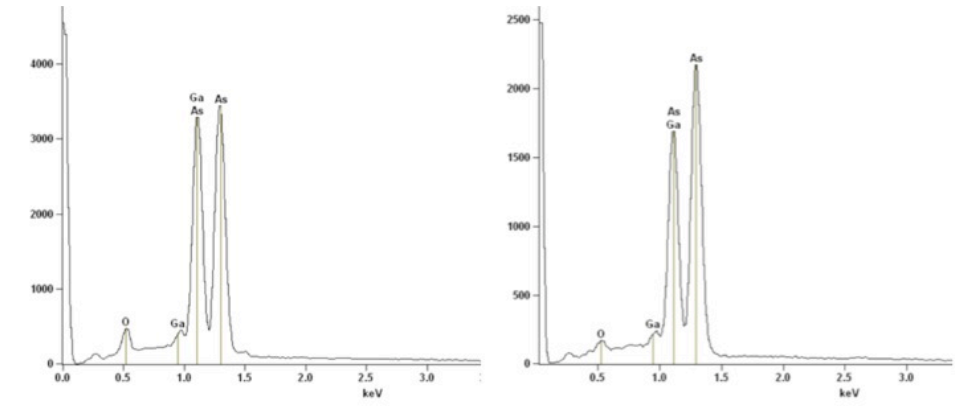


Figure 23: N-type GaAs electrochemically etched at 300 mA/cm^2 1.4s, 20 mA/cm^2 60 min. (a) in 5% H_2SO_4. (b) in 17.5% H_2SO_4. SEM images shown on left are cross-section and plan view on right.



Quantitative Results for: David Fong(29)

Element Line	Net Counts	Int. Cps/nA	Weight %	Weight % Error	Atom %
O K	2475	17.265	1.69	+/- 0.08	7.23
Ga L	27594	192.493	42.31	+/- 0.57	41.57
As L	32163	224.366	56.00	+/- 0.66	51.20
Total			100.00		100.00

Quantitative Results for: David Fong(63)

Element Line	Net Counts	Int. Cps/nA	Weight %	Weight % Error	Atom %
O K	622	10.902	0.73	+/- 0.10	3.26
Ga L	14470	253.612	37.48	+/- 0.70	38.18
As L	21190	371.392	61.79	+/- 0.84	58.57
Total			100.00		100.00

Figure 24: EDS data from Figure 23. Left is 5% H_2SO_4 and right is 17.5% H_2SO_4.

4.2.3 Annealing Porous GaAs

In order to facilitate high quality epitaxial growth, a smooth flat surface is ideal. As mentioned previously, annealing of porous Si causes the surface to coalesce, driven by surface energy minimization [5]. N-type GaAs samples shown in Figure 20 were annealed 450 °C at various times to see if similar results could be achieved. In order to prevent out gassing of As a GaAs proximity cap was put over the annealed samples to simulate an As environment. Figure 25 shows SEM images for etched sample and one annealed for 87 hours. Annealing at this temperature has no effect on the large cracks in the porous layer associated with drying. This though is expected as the cracks are much too large for coalescence through surface energy mechanisms. Figure 26 shows a more magnified image for pre and post annealed cross-sections. Comparing insert (a) to (b) and (c) reveals that a marginal amount of coalescence has taken place at the surface in the small μm sized features. EDS analysis of these layers after annealing reveals that they have become Ga rich due to the much high vapor pressure of As as compared to Ga. Figure 27 shows EDS data for annealed samples with and without a GaAs proximity cap. With

the cap the porous layer comes to an equilibrium composition of about 3% O, 45% As, and 52% Ga, essentially flipping the concentrations of As and Ga. Without the cap the porous layer oxidizes and becomes significantly more Ga rich. The results achieved from annealing porous GaAs show that 450 °C is too low a temperature to facilitate surface coalescence. For this experiment temperature was limited to 450 °C due to the constraints of the hotplate used. Further investigation at higher temperatures may provide better results based on the fact that Si requires a temperature of 1100 °C for surface reorganization.

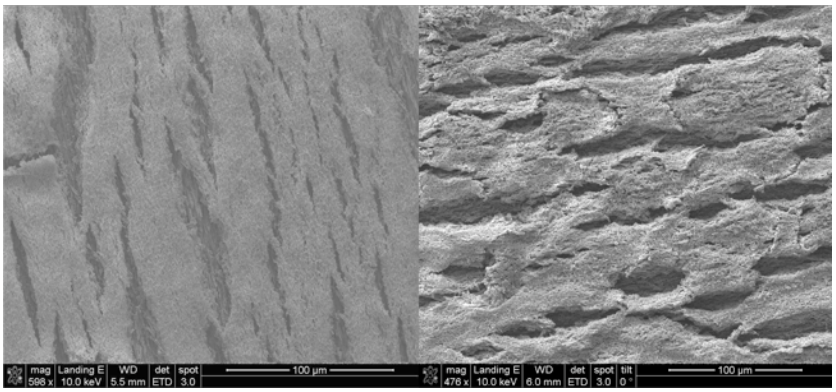


Figure 25: N-type GaAs etched in 5% H_2SO_4, 300 mA/cm^2 1.4s, 20 mA/cm^2 60 min. Left as etched and right annealed 87 hours at 450 °C. No noticeable change in large cracks.

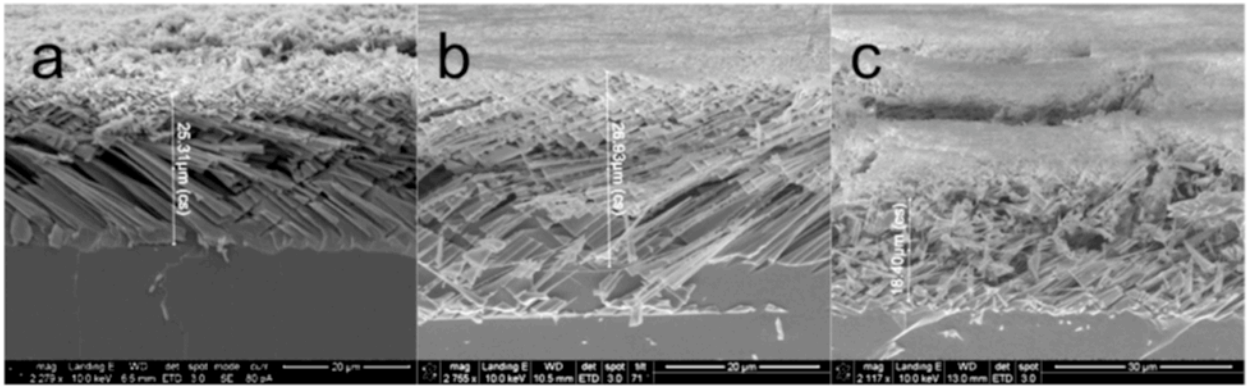
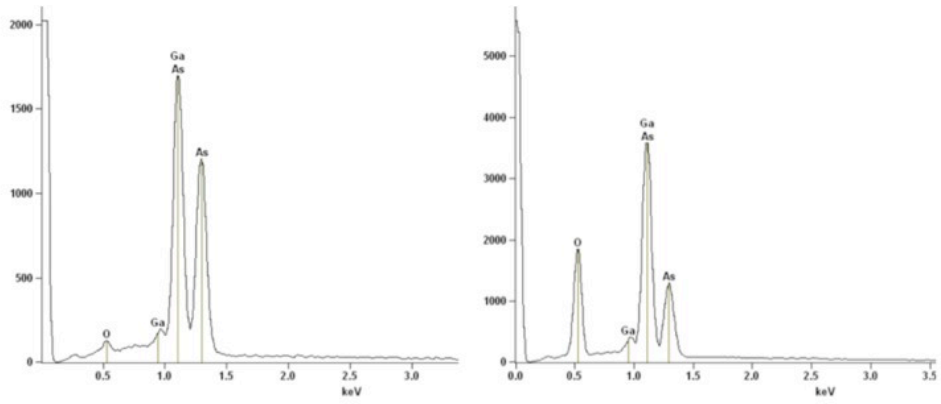


Figure 26: (a) pre annealed sample, (b) 23 hour anneal, (c) 87 hour anneal. Note images are taken from different areas of same sample. Slight coalescence seen in top µm sized pore in (b) and (c).



Quantitative Results for: David Fong(77)

Element Line	Net Counts	Int. Cps/nA	Weight %	Weight % Error	Atom %
O K	498	10.470	0.78	+/- 0.11	3.43
Ga L	14624	307.444	51.52	+/- 0.86	51.88
As L	11595	243.765	47.69	+/- 0.95	44.69
Total			100.00		100.00

Quantitative Results for: 5.12+Si 4.17.2012(15)

Element Line	Net Counts	Int. Cps/nA	Weight %	Weight % Error	Atom %
O K	12665	304.789	10.52	+/- 0.12	34.37
Ga L	31621	760.973	61.36	+/- 0.64	46.01
As L	12083	290.782	28.13	+/- 0.65	19.62
Total			100.00		100.00

Figure 27: EDS data for annealed sample with proximity cap (left) and without proximity cap (right).

Chapter 5: Conclusion and Future Work

This study investigated porous layer formation in n-type and p-type Ge and GaAs for CELT application in high efficiency multi-junction solar cells. In particular, attention was given to characterizing the chemical composition of these porous layers, which has been missing from most of the literature on this subject. The work here shows that electrochemical etching of p-type Ge and p-type GaAs in HF results in nanometer sized porous layers that look promising for CELT from a morphology standpoint. However, investigation of the chemical composition of these layers reveals that they are made up of a significant amount of oxide, contradicting claims made be Rojas et al. and Beji et al.. For p-type Ge it is found that the layer consist of 10 atomic percent oxygen or greater with an alternating current profile resulting in the lowest oxide levels. Electrochemical etching of p-type GaAs in HF gives a porous layer that is highly gallium deficient, with only a couple atomic percent Ga and As oxide making up the rest of the layer. Etching of n-type Ge gave low-density large sized (10-100's μm^2) pores that were accompanied by the formation of oxide spheres on the surface, making it unsuitable for CELT applications.

N-type GaAs gave the most promising results for CELT. A combination of electrochemical etching in 5% H_2SO_4 followed by a 15 min dip in 17.5% HCl closely maintained GaAs stoichiometry while removing pyramidal As oxide structures that form on the surface. High-density, uniformly nucleated, 1 μm^2 sized pores were created using a short duration, high current pulse followed by a long duration, low current pulse (300 mA/cm^2 1.4s, 20 mA/cm^2 225s). This two-step current profile is essential to achieving uniform high-density pore structures. H_2SO_4 was found to be a superior electrolyte than HCl for electrochemically etching n-type GaAs because of its much smaller preferential etch of Ga over As. The use of H_2SO_4

however, means that an additional HCl dip is needed to remove As oxide generated during the electrochemical etching process. Annealing of H_2SO_4 etched n-GaAs at 450 °C for over 80 hours had little to no effect on surface coalescence, and it was found that a GaAs proximity cap (or other source of an As overpressure) is needed to maintain layer stoichiometry.

Though n-GaAs etched in H_2SO_4 presents promising potential for CELT applications further work is needed to develop this technology. Foremost, the surface morphology must be optimized for epitaxial growth while maintaining a stoichiometric oxide free composition in the layer. This requires additional investigation of surface coalescence during annealing above 450 °C and potentially in an As atmosphere. After surface morphology has been addressed investigation of epitaxial growth of GaAs on the porous layer can be done with specific attention paid to generating high quality single crystal layers with minimal dislocation density.

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