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New Design Techniques for RF Receivers

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New Design Techniques for RF Receivers

A dissertation submitted in partial satisfaction
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Doctor of Philosophy in Electrical Engineering

by

Joung Won Park

2013

Abstract of the Dissertation

New Design Techniques for RF Receivers

by

Joung Won Park

Doctor of Philosophy in Electrical Engineering

University of California, Los Angeles, 2013

Professor Behzad Razavi, Chair

Despite two decades of research on RF circuits, challenges in RF design abound. The demand for a single, compact receiver that operates across different bands has led to considerable work on architecture and circuit techniques. This research addresses two critical receiver issues, namely, harmonic rejection and channel selection. It is shown that a bandwidth-programmable low-noise amplifier can suppress blockers at the local oscillator harmonics by 20 dB.

A holy grail in RF design has been to perform channel-selection filtering at RF rather than at IF or baseband. This research introduces the concept of "Miller notch filter" and demonstrates how it can provide channel selection while satisfying the exacting specifications of GSM and WCDMA. Realized in 65-nm CMOS technology, the receiver exhibits a noise figure of 2.9 dB and draws 20 mW with a 1.2-V supply at 2 GHz. The receiver can tolerate a 0-dBm blocker at 23-MHz offset and its RF channel selection devices can be readily configured to operate with WCDMA or IEEE802.11b/g as well.

The dissertation of Joung Won Park is approved.

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2013

To my beloved wife ...

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Vita

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Publications

J. W. Park and B. Razavi, "A Harmonic-Rejecting CMOS LNA for Broadband Radios," IEEE symposium of VLSI, June 2012.

J. W. Park and B. Razavi, "A Harmonic-Rejecting CMOS LNA for Broadband Radios," IEEE Journal of Solid State Circuits, vol. 48, pp. 1072-1084, Apr. 2013.

J. W. Park and B. Razavi, "A 20-mW GSM/WCDMA Receiver with RF Channel Selection," IEEE Solid State Circuits Conference, Feb. 2014.

CHAPTER 1

Introduction

1.1 Motivation

The continuous desire for a single transceiver covering the extensive frequency range from tens of megahertz to few gigahertz has led the evolution of software defined radios (SDR) and cognitive radios (CR). The biggest challenge for realizing these radios has been the existence of blockers around the desired channel and local oscillator (LO) harmonic frequencies, compelling transceivers to employ surface-acoustic-wave (SAW) filters to suppress those blockers. Since such filters are not tunable to various frequency bands, a broadband receiver itselt must reject blockers both around the desired channeland LO harmonics.

1.2 Organization

This dissertation includes two seperate solutions to reject LO harmonics and blockers around the desired channel frequency. The first part of the dissertation introduces a harmonic-rejecting low noise amplifier (LNA) to reject the third and higher LO harmonics by 20 dB. In the last part, a high-Q channel-selection receiver employing N-path filters in the feedback paths has been proposed.

Chapter 2 deals with the harmonic-rejecting LNA. Section 2.1 provides the background for the problems of LO harmonics and previous solutions, emphasiz-

ing the challenges in harmonic-reject mixers (HRMs). Section 2.2 describes the LNA design, proposing frequency response shaping technique such as feedforward and unilateral Miller capacitance multiplication. Section 2.3 deals with the calibration of the frequency response. Section 2.4 presents experimental results of the harmonic-rejecting LNA, followed by the conclusion of the harmonic-rejecting LNA in section 2.5.

Chapter 3 presents a GSM/WCDMA RF receiver with channel selection at RF. Section 3.1 discusses the background of the N-path filter and its limitation. Section 3.2 describes the employment of the N-path notch filter in the feedback path and the unilateral feedback path. Section 3.3 presents the experimental results of the proposed receiver with channel selection at RF. Section 3.4 summarizes and concludes chapter 3.

Chapter 4 concludes the dissertation.

CHAPTER 2

Harmonic-Rejecting LNA

A broadband receiver design has been a key in the implementation of a single trasceiver that covers multiple standards, i.e. from FM radio to IEEE 802.11a/g. Among the issues encountered in broadband receiver design, the problem of local oscillator (LO) harmonics has received considerable attention [1]-[3] as it leads to significant signal corruption in the presence of large blockers. Absent in conventional narrowband radios, this issue tends to raise both the power dissipation and complexity of the receiver.

This chapter introduces a 100-MHz to 10-GHz harmonic-rejecting low-noise amplifier (LNA) developed to relax the design of broadband receivers. The LNA incorporates notch and low-pass filtering techniques so as to reject by at least 20 dB input blockers at the third and higher harmonics of the LO. A calibration algorithm is also proposed that adjusts the frequency response so as to maximize the rejection. Realized in 65-nm digital CMOS technology, an experimental prototype provides tunable rejection from 300 MHz to 10 GHz while consuming 8.64 mW with a 1.2-V supply.

2.1 Background

Consider the direct-conversion receiver in Fig. 2.1, where only one downconversion mixer is shown for simplicity. If optimized for noise and gain, mixers typically

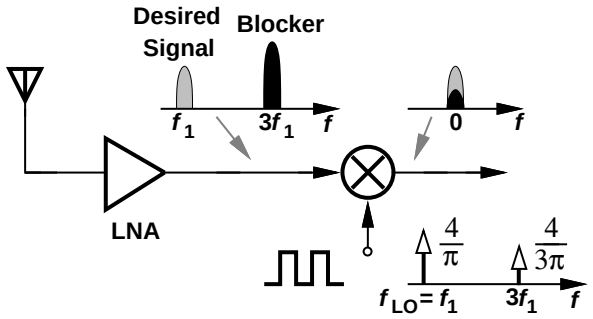


Figure 2.1: Problem of LO harmonics in a direct-conversion receiver.

perform abrupt switching, thus multiplying the RF input by a square-wave LO. As a result, input blockers coinciding with the LO harmonics are also downconverted to the baseband. With differential implementations, the odd harmonics are much more pronounced but the even harmonics may warrant attention as well [4]. In this chapter, we denote the desired input frequency by f_1 and a possible blocker at the third LO harmonic by $3f_1$. The principal challenge is that the LO harmonics decay only in proportion to $1/f$, posing severe rejection requirements on the receiver.

The effect of LO harmonics can be suppressed through the use of harmonic-reject mixers, as first realized by [5] in a transmitter and later demonstrated by [1]-[3] in receivers. Using 45° phases of the LO, HRMs can reject the third and fifth harmonics in proportion to the matchings in the LO path and in the RF path. For example, [1] attenuates these harmonics by 60 dB for $f_1 \leq 800$ MHz while consuming 17.1 mW in the LO distribution network. The design in [3], on the other hand, is insensitive to device mismatches but accommodates only $f_1 \leq 300$ MHz.

The problem of phase mismatch in HRMs becomes more serious as higher input frequencies are considered. It can be shown that a phase mismatch of ΔT

seconds between only two phases of the LO limits the rejection at the third and fifth harmonics to the following values:

$$A_{rej3} = \frac{\sin\left(\frac{3\pi\Delta T}{T_{LO}}\right)}{3\cos\left(\frac{\pi\Delta T}{T_{LO}}\right)} \tag{2.1}$$

$$A_{rej5} = \frac{\sin\left(\frac{5\pi\Delta T}{T_{LO}}\right)}{5\cos\left(\frac{\pi\Delta T}{T_{LO}}\right)}, \tag{2.2}$$

where T_{LO} denotes the LO period. If ΔT is small, we have $A_{rej3} \approx A_{rej5} \approx \pi\Delta T/T_{LO}$. For example, to obtain a rejection of 60 dB for $f_1 = 2$ GHz, a ΔT of less than 150 fs is necessary, which may not be possible even with careful layout. Of course, mismatches among the other LO phases and among the RF paths further exacerbate this issue. Note that a calibration scheme that seeks to reduce the mismatch from, say, 10 ps, to, say, 50 fs, would require 200 steps and hence substantial complexity.

We should also remark that HRMs operating with 45° LO phases do not suppress higher harmonics, e.g., the seventh or ninth, a serious drawback as the input band of interest approaches or exceeds one decade. For example, in the range of 100 MHz to 10 GHz, if $f_1 = 100$ MHz, then the blockers at LO harmonics up to the *hundredth* must be rejected.

The objective of this chapter is to demonstrate that the task of harmonic rejection can be partially shouldered by the LNA, thus relaxing the matching required of HRMs. A rejection of 20 dB is targetted to allow a tenfold increase in the mixers' mismatch budget.

2.2 Harmonic Rejection in LNA

Blockers at LO harmonics can be attenuated by means of filtering. For broadband operation, the filter must be tunable in sufficiently small steps so as to reject the blockers according to the selected LO frequency. Also, the filter *parasitics* must not degrade the LNA gain and noise figure (NF) significantly when the LNA must amplify high frequencies. These two principles govern the evolution of the LNA reported here. It is worth noting that band-pass filtering techniques based on N-path mixing [6]-[8] do not yield significant attenuation at the LO harmonics [9, 10]. Similarly, the feedforward interference cancellation techniques introduced in [11] and [12] do not provide harmonic rejection since they also use frequency mixing in the feedforward paths.

Let us contemplate an RC filter with programmable capacitors interposed between the LNA and the downconversion mixers. In order to tune the rejection from $3f_1 = 300$ MHz to 10 GHz, the capacitor value(s) must vary by about a factor of 30, e.g., from $30C_u$ to C_u. If the unit capacitor (or its switch) introduces a parasitic of, say, $0.02C_u$ in the signal path, then the circuit suffers from a total parasitic of about $0.6C_u$ when all of the units are *switched out* and the input frequency is near 10 GHz. If designed to attenuate $3f_1 = 10$ GHz by tens of decibels when one C_u is switched in, the filter unfortunately also exhibits a similar attenuation for $f_1 = 10$ GHz and a parasitic loading of $0.6C_u$. In other words, such a tunable filter inevitably produces considerable pass-band loss when programmed for high input frequencies.

The foregoing issues become even more serious for LC filter implementations due to the square-root dependence of cut-off frequencies upon the capacitor value(s). For example, the design in [13] employs an off-chip inductor to tune a band-pass filter from 65 MHz to 400 MHz.

2.2.1 Filtering by Feedforward

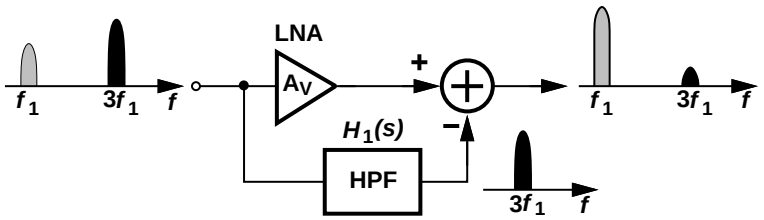


Figure 2.2: Low-pass filtering by feedforward.

Following our principle that any means of filtering must minimally load the signal path, we consider creating a low-pass response by feedforward (Fig. 2.2). If the high-pass filter (HPF) suppresses the desired component at f_1 and passes the blocker at $3f_1$ with no phase or gain error, then the output is free from the blocker. Now, the filter devices negligibly affect the signal path. Also, in contrast to HRMs, this approach attenuates *all* blockers lying within the HPF's passband, including those *not* at the LO harmonics.

The above scheme entails four issues:(1) the HPF input impedance may severely degrade the input matching; (2) the parasitics introduced by the filter devices in the feedforward path alter its gain and phase, prohibiting complete cancellation of the blocker(s) at the subtractor output; (3) the HPF must have a high enough order to reject the desired signal by a large factor, e.g., 10, while negligibly affecting the blocker(s); and (4) the feedforward path's noise at f_1 adds to the LNA output and must be minimized.

To address the first three issues, one can realize the HPF as a cascade of capacitively-degenerated common-source stages, as conceptually illustrated in Fig. 2.3. Here, the source capacitors can be programmed across a wide range and their parasitics do not attenuate the high-frequency components traveling through the feedforward path. The input capacitance of the HPF is fairly small

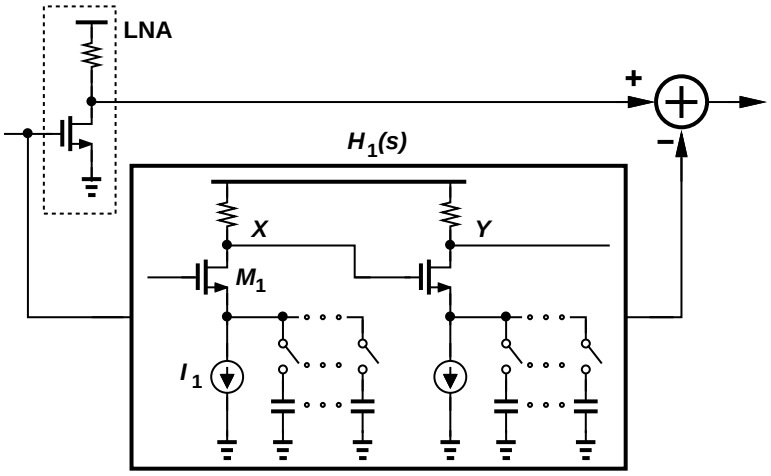


Figure 2.3: LNA using capacitively-degenerated feedforward.

and can be managed as explained below.

The fourth issue, namely, the HPF output noise at f_1 still persists. While the noise produced by the first stage, e.g., that due to M_1 and I_1, is attenuated roughly by the same factor as the input (at f_1) to $H_1(s)$, the noise of the subsequent stages experiences progressively less attenuation. Thus, a multi-stage HPF may degrade the overall noise figure considerably.

2.2.2 LNA with Embedded Feedforward

This section describes the evolution of the LNA design as various frequency response shaping techniques are applied to it so as to reject blockers at the LO harmonics. In each case, the simulated response is presented, issues are revealed, and methods are devised to resolve them. For most of the analysis. we assume a desired channel at $f_1 = 330$ MHz as an example.

This work employs the broadband feedback LNA described in [4] and embeds the frequency-selective feedforward within the LNA as shown in Fig 2.4(a). The LNA itself is designed such that $R_F/(1+A_0) = R_S$, where $-A_0$ denotes the open-

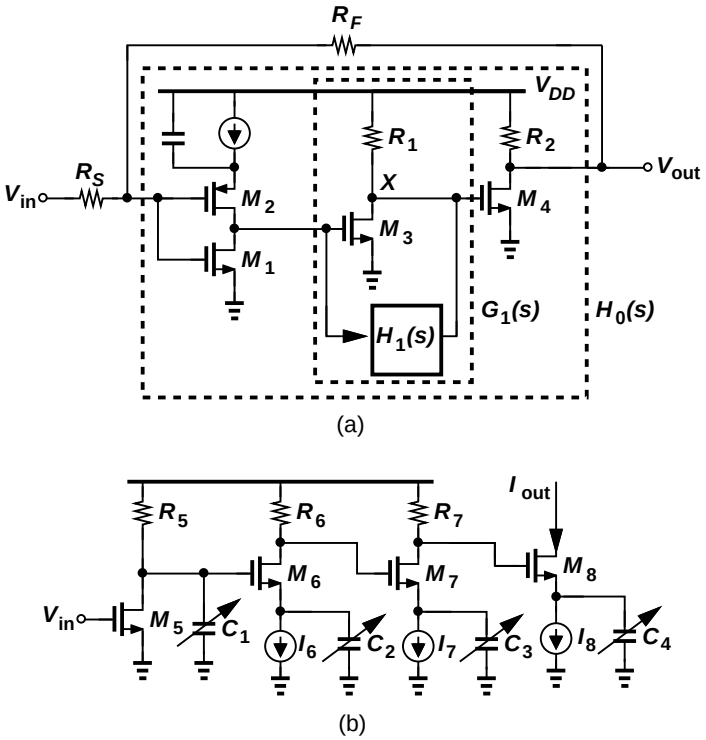


Figure 2.4: (a) Resistive-feedback LNA with embedded HPF, (b) implementation of $H_1(s)$.

loop gain. Preceded by a gain stage, the HPF now contributes negligibly to the NF. The active HPF implementation is depicted in Fig. 2.4(b), where M_5 serves as a dc interface and M_6-M_8 provide programmable high-pass filtering. Each of capacitors C_1-C_4 is formed as a 6-bit array. (The role of C_1 is described below). Ignoring C_1 for now, we can express $H_1(s) = I_{out}(s)/V_{in}(s)$ in Fig. 2.4(b) as

$$H_1(s) = -g_{m5}R_5 \cdot \frac{g_{m6}C_2 s R_6}{C_2 s + g_{m6}} \cdot \frac{g_{m7}C_3 s R_7}{C_3 s + g_{m7}} \cdot \frac{g_{m8}C_4 s}{C_4 s + g_{m8}}. \tag{2.3}$$

For feedforward cancellation, we choose the pass-band transconductance, $-g_{m5}R_5 g_{m6}R_6 g_{m7}R_7 g_{m8}$, equal to g_{m3}. Assuming $C_2 = C_3 = C_4 = C_f$ and $g_{m6} = g_{m7} = g_{m8} = g_{mf}$, we obtain the transfer function of the second stage of

the LNA, $G_1(s)$, as follows:

$$\begin{aligned} G_1(s) &= g_{m3}R_1\left[1-\left(\frac{C_f s}{C_f s+g_{mf}}\right)^3\right] \\ &= g_{m3}R_1\cdot\frac{3g_{mf}}{C_f}\cdot\frac{s^2+\frac{g_{mf}}{C_f}s+\frac{g_{mf}^2}{3C_f^2}}{\left(s+\frac{g_{mf}}{C_f}\right)^3}. \end{aligned} \tag{2.4}$$

The above transfer function applies to the second stage of the *open-loop* LNA. The closed-loop transfer function is given by

$$\frac{V_{out}}{V_{in}}(s)=\frac{R_F}{R_S+R_F}\cdot\frac{H_0(s)}{1-\frac{R_S}{R_S+R_F}H_0(s)}, \tag{2.5}$$

where $H_0(s)$ is the overall open-loop LNA transfer function. To include the feedforward action, we write from (2.4)

$$H_0(s)=-A_0\cdot\frac{3g_{mf}}{C_f}\cdot\frac{s^2+\frac{g_{mf}}{C_f}s+\frac{g_{mf}^2}{3C_f^2}}{\left(s+\frac{g_{mf}}{C_f}\right)^3}, \tag{2.6}$$

where $-A_0$ denotes the low-frequency gain. [1] Since $R_F=(1+A_0)R_S$, (2.5) emerges as

$$\frac{V_{out}}{V_{in}}(s)=-A_0\cdot\frac{3g_{mf}}{C_f}\cdot\frac{s^2+\frac{g_{mf}}{C_f}s+\frac{g_{mf}^2}{3C_f^2}}{\left(1+\frac{1}{1+A_0}\right)s^3+\frac{6g_{mf}}{C_f}s^2+\frac{6g_{mf}^2}{C_f^2}s+\frac{2g_{mf}^3}{C_f^3}}. \tag{2.7}$$

Fig. 2.5(a) plots the simulated frequency response of $H_0(s)$ with the three feedforward poles in (2.6) placed at 280 MHz for $f_1=330$ MHz. The response exhibits a peaking of about 2 dB around f_1 and an attenuation of only 6 dB at $3f_1=1$ GHz. This deficiency originates from the phase shift caused by the zeros

[1] The capacitor in parallel with the current source in the first stage of the LNA does not appear in $H_0(s)$ as it is large enough to provide an ac ground above 100 MHz.

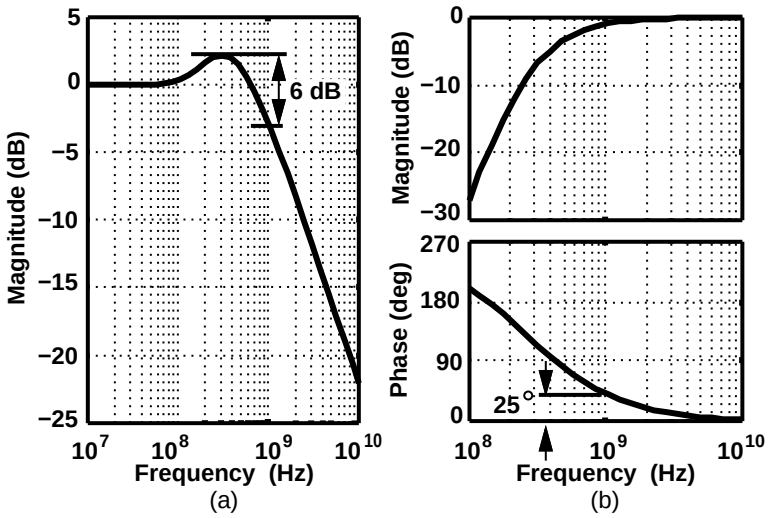
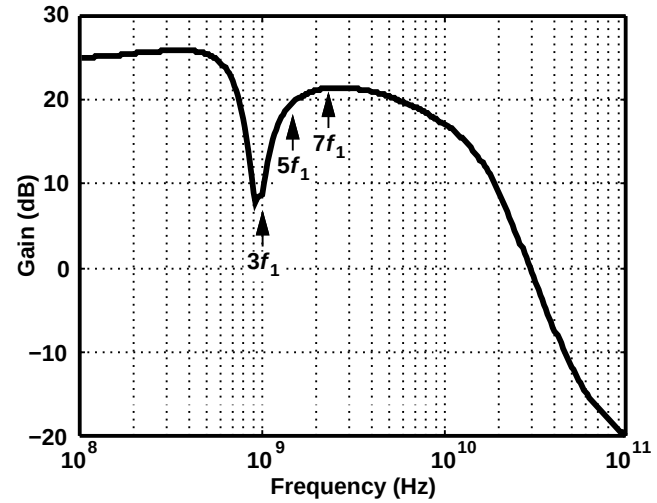


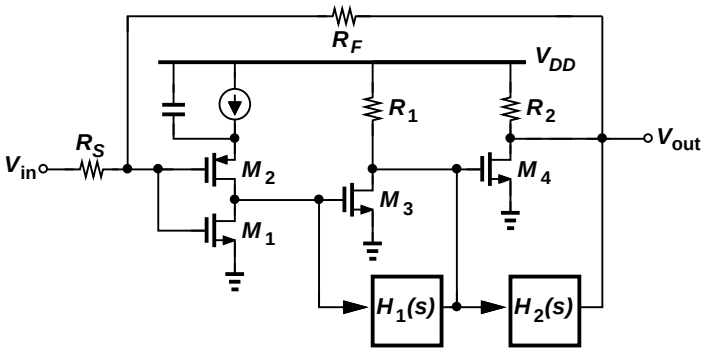
Figure 2.5: Frequency response of (a) $H_0(s)$, and (b) $H_1(s)$ ($f_1 = 330$ MHz).

in (2.6) at $3f_1$. As illustrated in Fig. 2.5(b), the magnitude of the feedforward transfer function, $|H_1(j\omega)|$, is about -0.9 dB at 1 GHz, suggesting a cancellation factor of about 10, but the phase reaches 25°, yielding a residual component with a normalized magnitude of $20\log(\sin 25°) = -7.5$ dB.

The zeros' phase lead can be compensated by a pole's phase lag, as realized by capacitor C_1 in Fig. 2.4(b). Also a 6-bit array, this capacitor is programmable in tandem with C_2-C_4. Figure 2.6(a) shows the result of this attempt: the inserted lag now allows a rejection of about 20 dB at $3f_1$, but it also alters the phase at higher LO harmonics, creating a large hump in the LNA frequency response. Fortunately, the feedforward concept can be repeated around the *third* stage of the LNA so as to introduce zeros at the higher harmonics. Depicted in Fig. 2.6(b), this path, $H_2(s)$, contains three 5-bit programmable zeros but no programmable pole, yielding the response plotted in Fig. 2.6(c). The rejection at $5f_1$ and $7f_1$ is improved but the hump at higher harmonics is still unacceptably high. This is because the intrinsic poles of $H_1(s)$ and $H_2(s)$, e.g., those at the drains M_6 and M_7 in Fig. 2.4(b), collectively contribute significant phase shift even though they



(a)



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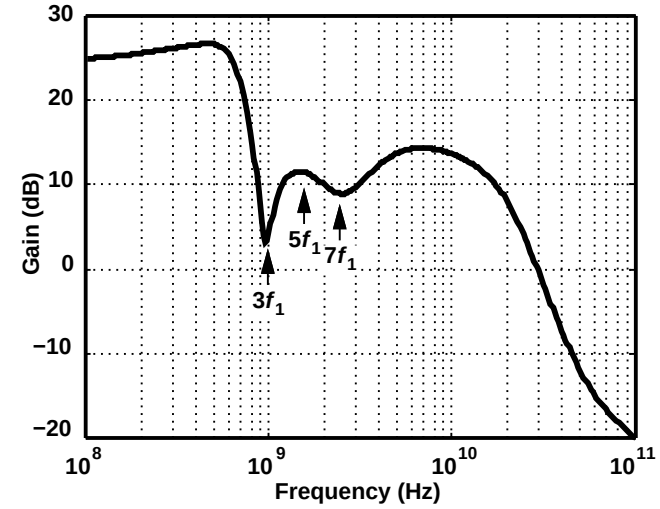


(c)

Figure 2.6: (a) LNA frequency response with pole phase lag ($f_1 = 330$ MHz), (b) LNA with two HPFs, $H_1(s)$ and $H_2(s)$, (c) LNA frequency response with $H_1(s)$ and $H_2(s)$ ($f_1 = 330$ MHz).

are located well above 10 GHz.

2.2.3 Unilateral Miller Effect

In order to further shape the LNA frequency response, we can consider the use of a Miller capacitor at the input. For example, a programmable capacitor tied between the input and output of the first stage in Fig. 2.4(a) could form an LPF with R_S, attenuating high frequencies and hence removing the hump in Fig. 2.6(c). Depicted in Fig. 2.7(a), this approach would violate one of the two principles mentioned at the beginning of Section 2.3: for the capacitor to be large enough to serve at the lowest $3f_1(= 300$ MHz), its parasitics would load the signal path so much that the LNA would not accommodate the highest $f_1(\approx 10$ GHz).

In order to isolate the output of the LNA's first stage from the parasitic loading of such a large capacitor, we can envision a *unilateral* Miller arrangement, whereby the feedback capacitor is driven by a buffer on the output side [Fig. 2.7(b)]. An ideal unity-gain buffer would yield an input pole at the frequency of $\{[1 + (g_{m1} + g_{m2})(r_{o1}||r_{o2})] R_S C_{mill}\}^{-1}$ but we can ask what happens if the buffer provides voltage gain. With a gain of B_0, the buffer lowers the pole frequency to

$$\omega_p = \frac{1}{[1 + B_0 (g_{m1} + g_{m2})(r_{o1}||r_{o2})] R_S C_{mill}} \tag{2.8}$$

thus allowing a smaller value for C_{mill}.

Let us go one step further and ask what happens if B_0 itself is frequency-dependent. In particular, if B_0 has a high-pass response, then the Miller multiplication factor of C_{mill} *rises* with frequency, making C_{mill} a "supercapacitor." This intuition can be quantified by expressing the buffer transfer function as, for example, that of a capacitively-degenerated CS stage, $B_0 C_d s/(C_d s + g_{mB})$, where C_d denotes the degeneration capacitance [Fig. 2.7(c)]. The LNA's first

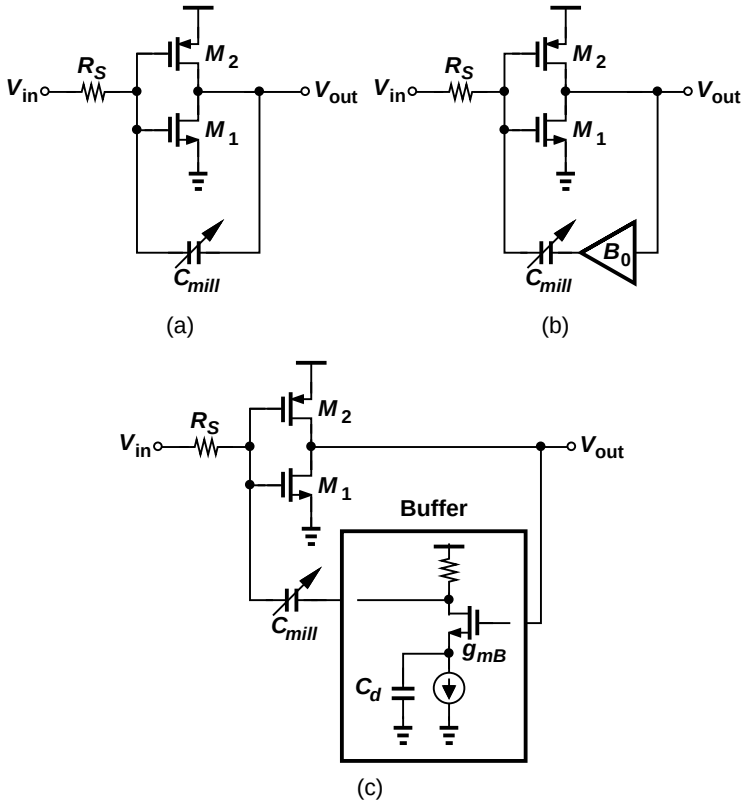


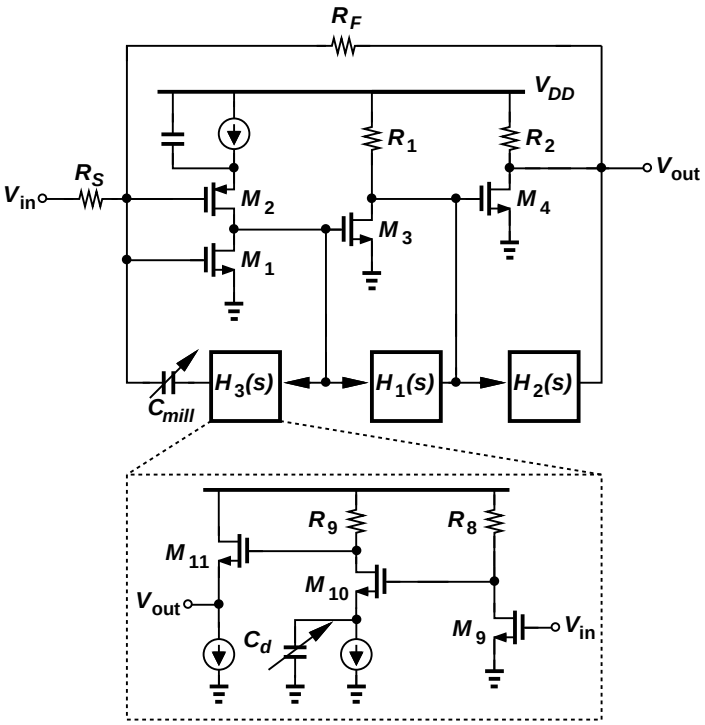
Figure 2.7: (a) Conventional Miller capacitor, (b) unilateral Miller capacitor, (c) unilateral Miller "supercapacitor."

stage response is now written as

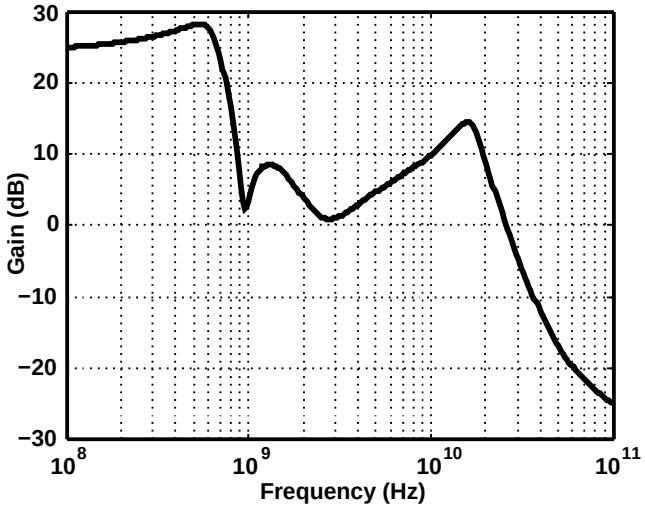
$$\frac{V_{out}}{V_{in}}(s) = \frac{-g_{mF}R_L\left(C_d s + g_{mB}\right)}{\left(1 + B_0 g_{mF} R_L\right) R_S C_d C_{mill} s^2 + \left(g_{mB} R_S C_{mill} + C_d\right) s + g_{mB}}, \qquad (2.9)$$

where $g_{mF} = g_{m1} + g_{m2}$ and $R_L = r_{o1}||r_{o2}$. In this work, the pole frequencies are chosen approximately equal to $4f_1$, so that the Miller path does not degrade the NF at f_1. The zero is located around $9f_1$.

Figure 2.8(a) shows the LNA circuit along with the unilateral Miller capacitance circuit. The corresponding response is plotted in Fig. 2.8(b), exhibiting improved rejection up to 10 GHz but still insufficient to meet the 20-dB target. The rise in the response stems from the parasitic poles within the unilateral buffer, calling for additional shaping of the frequency response.



(a)



(b)

Figure 2.8: (a) LNA with HPFs and the unilateral Miller path, (b) LNA gain with HPFs and the unilateral Miller path.

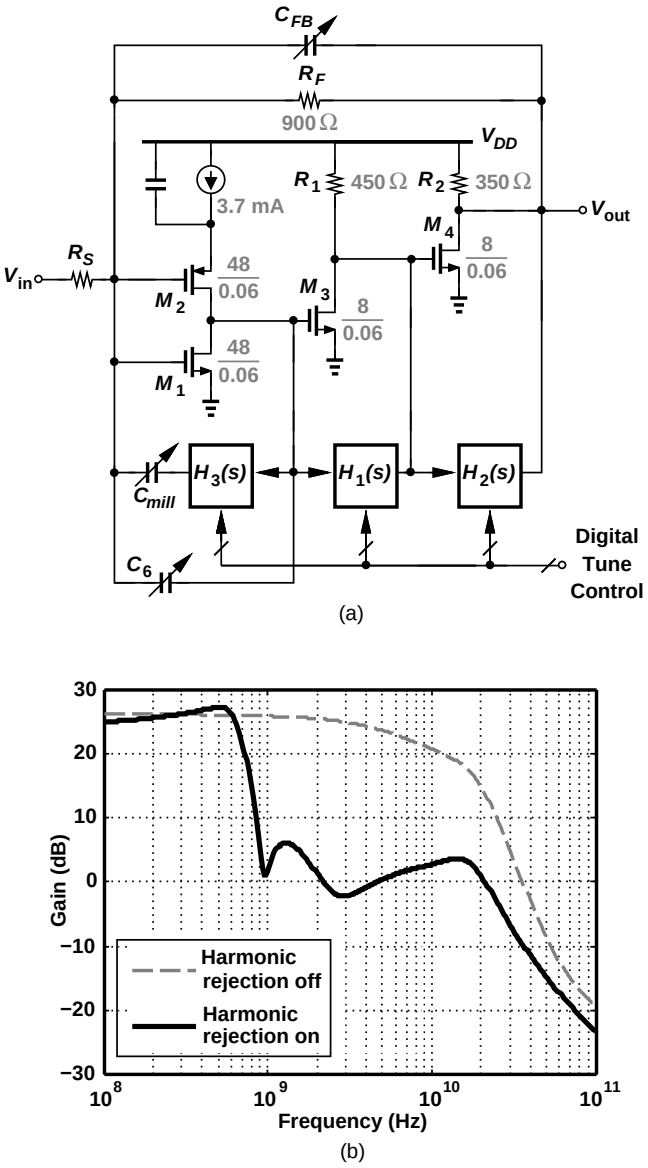


Figure 2.9: (a) Final LNA topology (transistor dimensions in microns), (b) LNA frequency response with harmonic rejection off or on.

The overall LNA incorporates two more feedback capacitors to achieve at least 20 dB of rejection at all frequencies equal to or greater than $3f_1$ for $f_1 = 100$ MHz to 3.3 GHz. As depicted in Fig. 2.9(a), capacitor C_6 dominates the Miller path at high frequencies. Capacitor C_{FB} improves both the rejection and the input matching.The black solid plot in Fig. 2.9(b) shows the final response.

The matching between the gains of the LNA main path and the feedforward paths ultimately determines the amount of blocker rejection that the overall circuit can provide. Fortunately, if the gain of the feedforward paths is *greater* than that of main paths, then it is still possible to obtain a high rejection by adjusting the amount of capacitive degeneration. Accordingly, in this design, the feedforward gains are deliberately chosen 20% *higher* than the necessary values. As verified by experimental results, this skew, along with the calibration algorithm, allows the LNA to find a rejection of at least 20 dB.

2.2.4 NF Behavior

The frequency response shaping techniques described above can potentially degrade the noise figure (and input matching) of the LNA. Indeed, many other filtering methods were tried with various LNA topologies and discarded for this reason. The NF penalty arises primarily from the noise contributed by the feedforward paths, $H_1(s)$ and $H_2(s)$, in Fig. 2.9(a). The unilateral Miller path only manifests itself at high harmonics, thus negligibly raising the NF in the channel of interest.

In order to quantify the NF penalty due to $H_1(s)$, we return to the implementation in Fig. 2.4(b) and seek the transfer functions for M_5-M_8, R_5-R_7, and I_6-I_8 to I_{out}. The sum of these contributions is then multiplied by R_1 in Fig. 2.4(a) and referred to the LNA input. Upon traveling through the high-pass filter, the

noise of M_5 and R_5 is suppressed along with the desired signal. The noise of the subsequent stages is attenuated less and merits investigation. For example, the noise of I_6, I_{n6}, reaches I_{out} according to the following transfer function:

$$\frac{I_{out}}{I_{n6}}(s) = R_6 \left(\frac{g_{mf} C_f s}{C_f s + g_{mf}} \right)^2 R_7, \tag{2.10}$$

where the notation is the same as in (2.4). With the values chosen in this design, $|I_{out}/I_{n6}|$ is about 0.6 and the contribution of $\overline{I_{n6}^2}$ is equal to one-eighth of the noise current of M_3, $\overline{I_{n3}^2}$, in Fig. 2.4(a). For the noise of I_7 and I_8 in Fig. 2.4(b), the contribution rises to one-fifth and one-third of $\overline{I_{n3}^2}$, respectively. Fortunately, the gain of the LNA's first stage (16 dB) suppresses these effects to an NF penalty of 0.4 dB. The penalty due to H_2 is an additional 0.3 dB. These penalties rise to 0.6 dB and 0.4 dB, respectively, for $f_1 = 3.33$ GHz.

2.2.5 S_{11} Behavior

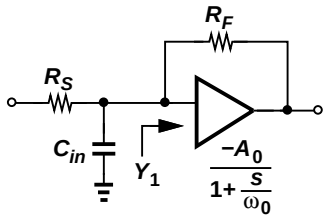


Figure 2.10: Admittance of the resistive-feedback LNA.

The input matching of the feedback LNA is primarily secured by the global feedback. As explained in [4], the admittance Y_1 in Fig. 2.10 can be expressed as follows

$$\frac{1}{Re\{Y_1\}} \approx \frac{R_F\left(\omega^2 + \omega_0^2\right)}{\left(1 + A_0\right)\omega_0^2} \tag{2.11}$$

$$Im\{Y_1\} = \frac{-A_0\omega_0}{R_F\left(\omega^2 + \omega_0^2\right)}\omega \tag{2.12}$$

If the frequency of interest, ω, is much less than the core (open-loop) amplifier's -3-dB bandwidth, ω_0, then $1/Re\{Y_1\} \approx R_F/(1+A_0)$, which must be set equal to R_S, and $Im\{Y_1\} \approx -(A_0/R_F\omega_0)\omega$, which must cancel $-C_{in}\omega$. It follows that $R_F/A_0 \approx R_S$ if $A_0 \gg 1$ and $A_0/R_F\omega_0 = C_{in}$. That is,

$$\omega_0 \cong \frac{1}{R_S C_{in}}. \tag{2.13}$$

Such a high value of ω_0 may be difficult to achieve in the LNA. For example, for $R_S = 50\ \Omega$ and $C_{in} \approx 75$ fF, ω_0 must reach $2\pi\times(42$ GHz). We therefore conclude that practical values of ω_0 degrade the S_{11} at high input frequencies. This phenomenon occurs because a low ω_0 makes the input reactance excessively inductive.

It is possible to alleviate this issue by means of a feedback capacitor [C_{FB} in Fig. 2.9(a)]. The input admittance now emerges as

$$\frac{1}{Re\{Y_1\}} \approx \frac{R_F\,(\omega^2+\omega_0^2)}{(1+A_0)\,\omega_0^2 + A_0 R_F C_{FB}\omega_0\omega^2} \tag{2.14}$$

$$Im\{Y_1\} = \frac{-A_0\omega_0 + R_F C_{FB}\,[(1+A_0)\,\omega_0^2+\omega^2]}{R_F\,(\omega^2+\omega_0^2)}\omega \tag{2.15}$$

If $\omega \ll \omega_0$ and $Im\{Y_1\}$ is to cancel $-C_{in}\omega$, then

$$\frac{A_0}{R_F\omega_0} - (1+A_0)\,C_{FB} = C_{in} \tag{2.16}$$

and hence

$$\omega_0 = \frac{1}{R_S\,[C_{in} + (1+A_0)\,C_{FB}]}. \tag{2.17}$$

Thus, a lower ω_0 can still guarantee matching if $(1+A_0)\,C_{FB}$ is large enough to satisfy the equation. Capacitor C_6 in Fig. 2.9(a) plays a similar role.

Figure 2.11(a) plots the simulated S_{11} with harmonic rejection (HR) off and on for $f_1 = 3.33$ GHz. We observe that S_{11} remains below -20 dB up to f_1. Figure 2.11(b) plots the corresponding LNA frequency response, demonstrating

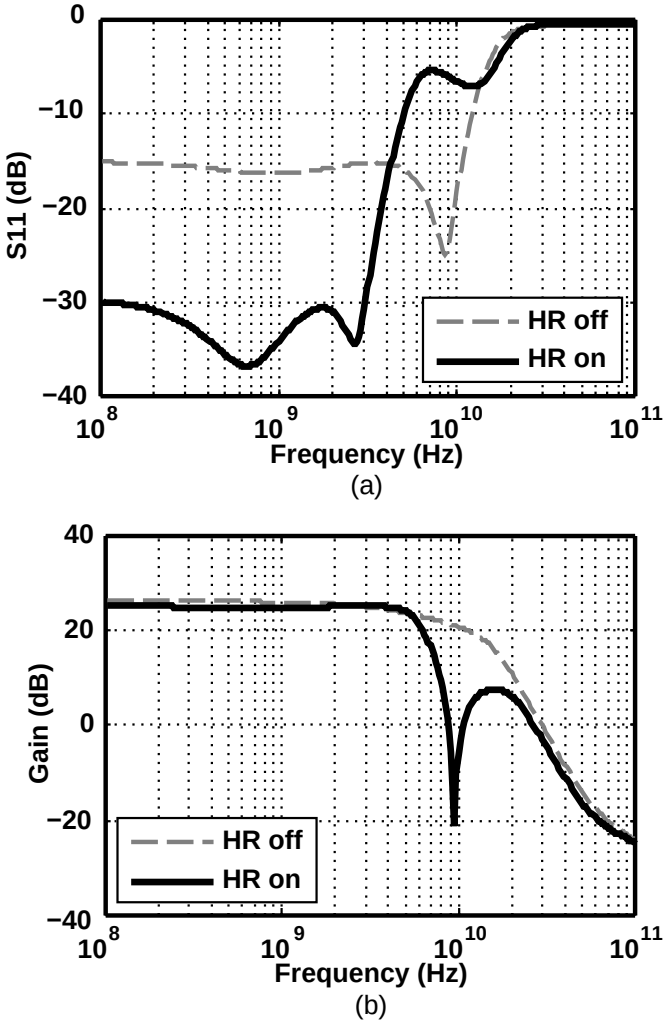


Figure 2.11: LNA performance with harmonic rejection on and off ($f_1 = 3.33$ GHz): (a) S_{11}, (b) LNA frequency response.

a rejection of about 30 dB at $3f_1$ and that the frequency response shaping devices negligibly affect the LNA performance when they are switched out.

2.2.6 Stability

In this section, we study the stability behavior of the LNA before and after harmonic-rejection frequency response shaping. In each case, a root locus is constructed with the design values shown in Fig. 2.9(a) while the feedback factor,

β, is varied from 0 to the nominal value of 0.0526. This is accomplished by varying R_F from infinity to 900 Ω.

The open-loop LNA core exhibits a transfer function, $H_0(s)$, with three poles at 8 GHz, 17 GHz, and 26 GHz:

$$H_0(s) = -\frac{A_0}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)\left(\frac{s}{p_3}+1\right)}. \tag{2.18}$$

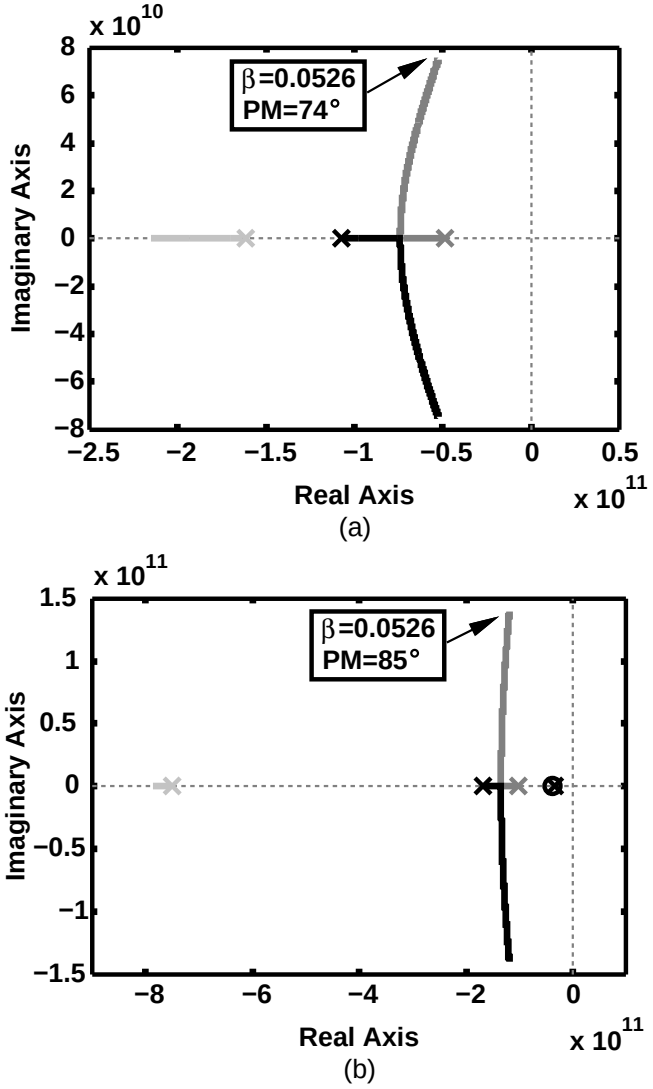


Figure 2.12: Root locus of (a) $H_0(s)$, (b) $H_0(s)$ with C_{FB}.

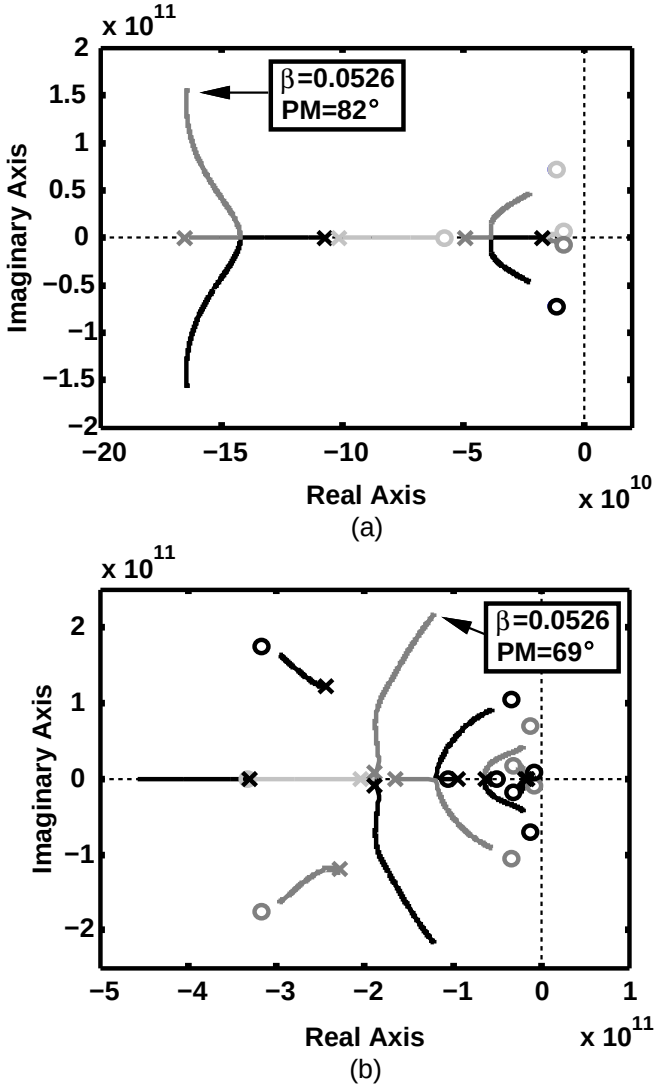


Figure 2.13: Root locus of (a) $H_0(s)$ with $H_1(s)$, (b) entire LNA.

Figure 2.12(a) plots the root locus as R_F varies, indicating a phase margin of 74° for $\beta = 0.0526$. We now consider the effect of C_{FB} in Fig. 2.9(a). Breaking the loop at the gates of M_1 and M_2, we observe that the open-loop transfer function is now multiplied by $R_S(R_F C_{FB} s + 1)/(R_S R_F C_{FB} s + R_S + R_F)$, acquiring a new zero at $-1/(R_F C_{FB})$ and a new pole at $-(R_S + R_F)/(R_S R_F C_{FB})$. For example, if $C_{FB} = 20$ fF, then the zero and the pole lie at 8.8 GHz and 160 GHz, respectively, with the former compensating the phase lag due to the poles and improving the

stability. Figure 2.12(b) plots the root locus for this case. Capacitor C_6 in Fig. 2.9 plays a similar role.

Let us next include the first feedforward stage, $H_1(s)$, in Fig. 2.9(a). The simulated root locus for $3f_1 = 1$ GHz is depicted in Fig. 2.13(a), revealing a phase margin of 82° for $\beta = 0.0526$. The phase margin changes negligibly because the overall feedback is relatively weak. For the entire harmonic-rejecting design, the simulated root locus emerges as shown in Fig. 2.13(b), still exhibiting reasonable stability.

2.3 Calibration

2.3.1 Tuning Resolution

Due to the discrete tuning of the LNA, the valley of the notch in the frequency response may not exactly coincide with $3f_1$, limiting the amount of rejection. Thus, the resolution of the capacitor arrays must be chosen according to the notch "bandwidth," i.e., the frequency range around the minimum point across which the rejection is still acceptable. We further remark that the rejection must hold within the entire RF blocker *channel* bandwidth, which, in the worst case, is that of IEEE802.11a/g and equal to 20 MHz. Figure 2.14(a) illustrates this situation, suggesting that the rejection at one edge of the channel may become problematic.

Figure 2.14(b) plots the simulated notch "half bandwidth" defined as shown in Fig. 2.14(a). A conservative choice here is to ensure that the tuning step size is *less* than the notch half bandwidth. As illustrated in Fig. 2.14(c), this choice guarantees at least one tuning code with 20 dB of rejection. In this work, the step size varies from 5 MHz at $3f_1 = 300$ MHz to 1 GHz at $3f_1 = 10$ GHz.

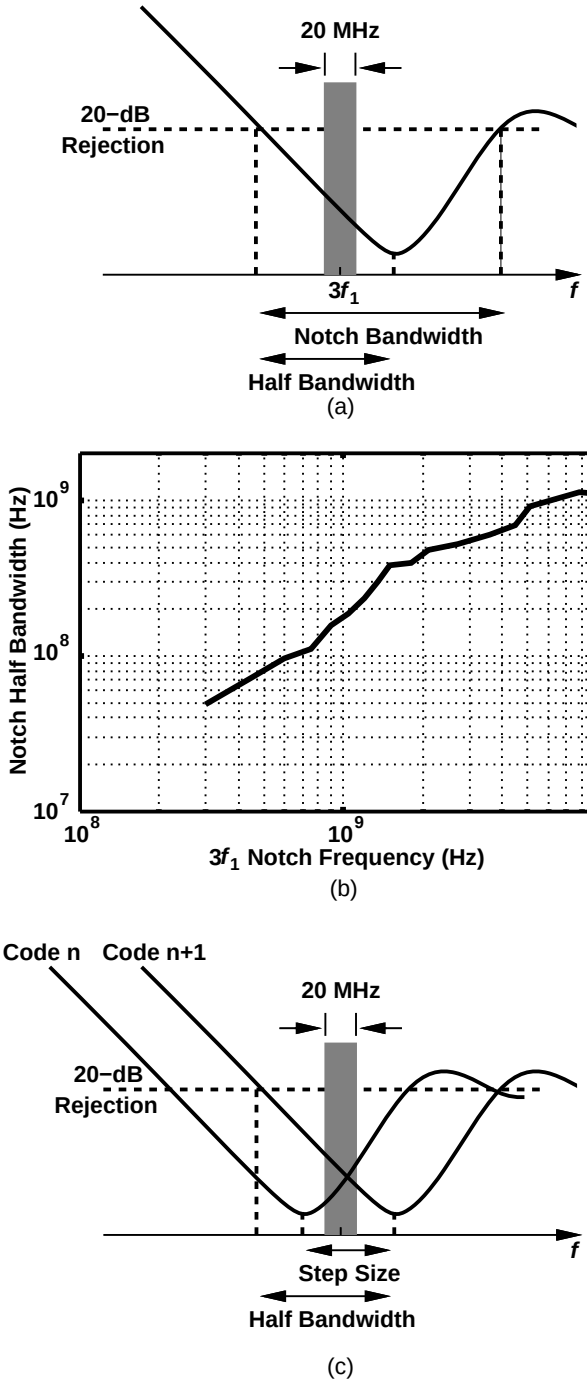


Figure 2.14: (a) Definition of notch half bandwidth, (b) notch half bandwidth as a function of $3f_1$, (c) notch step size and 20-dB rejection region.

2.3.2 Calibration Algorithm

An RF receiver utilizing the proposed LNA must automatically impose the capacitor settings according to the LO frequency. However, the frequency shaping varies with process and temperature, requiring that calibration be first performed for all LO frequencies and the results be stored in look-up tables. [2]

In order to determine the optimum capacitor tuning code for a given f_1, we can apply to the LNA input a sinusoid at $3f_1$, measure the output amplitude, and adjust the settings so as to minimize this amplitude. But this approach demands a peak detector operating from 300 MHz to 10 GHz, a complex circuit. We propose another approach that readily lends itself to a direct-conversion receiver environment and requires minimal overhead.

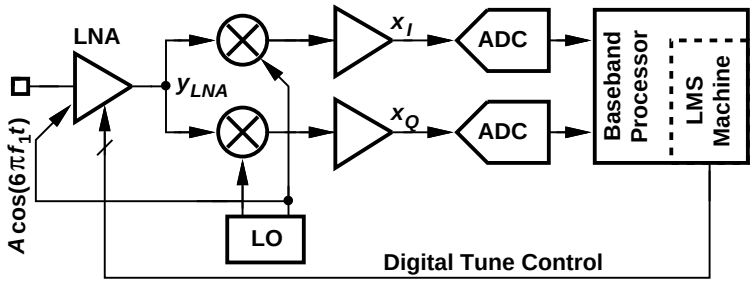


Figure 2.15: Notch frequency calibration loop.

As illustrated in Fig. 2.15, to calibrate the notch for a frequency of $3f_1$, the receiver sets the LO frequency to $3f_1$ (rather than f_1) and feeds a small fraction to the LNA. Upon traveling through the LNA and mixing with the LO, this input produces at x_I (or x_Q) a dc level proportional to the LNA output amplitude at $3f_1$. This dc value is subsequently digitized by the baseband analog-to-digital converter (ADC) and fed as an error to a least-mean-square (LMS) machine,

[2]For calibration, a single control word is applied to all of the capacitor arrays in Fig. 2.9(a) simultaneously, with $H_2(s)$ using only 5 MSBs and C_{FB} and C_6 only 3 MSBs. The resistances and transconductances remain constant.

which controls the capacitor settings. The loop now adjusts the notch frequency so as to drive the error toward zero.

This foreground calibration entails a number of issues. First, if the phase shift through the LNA at $3f_1$ happens to be around 90°, then x_I (or x_Q) falls to zero, yielding no information and prohibiting convergence of the loop. Fortunately, $x_I^2 + x_Q^2$ can be used as the error to avoid this issue. Since the calibration can be performed at low baseband clock speeds, this operation may be implemented using compact logic.

Second, the injection port for $A\cos(6\pi f_1 t)$ in Fig. 2.15 merits attention as it is undesirable to disconnect the main LNA input from the antenna (or the preselect filter). Fortunately, the signal can be injected as a current (by means of a transistor) into the output node of the first or second stage in Fig. 2.9(a). Simulations confirm that such an injection experiences the same notch frequency as does the main input. Third, the injection level must produce a sufficiently large dc value (in the baseband) that can be digitized with reasonable resolution by the ADCs. For example, a gain of 40 dB from y_{LNA} to x_I in Fig. 2.15 would require a peak amplitude of a few millivolts at the LNA output so as to produce a dc value of several hundred millivolts at the ADC input. Such an amplitude can be readily obtained.

Fourth, the dc offset due to LO self-mixing, the mismatch between the I and Q paths, and the harmonics of the input signal must also be considered. The next section deals with the receiver imperfection including the dc offset.

2.3.3 Receiver Imperfection

The dc offsets arising from LO self-mixing add to x_I and x_Q in Fig. 2.15. These offsets can be measured when the LO injection into the LNA is zero and sub-

tracted out from x_I and x_Q. This approach assumes that the LO self-mixing does not vary with the capacitor settings in the LNA, which may not be valid if all of the capacitors are first disconnected and subsequently connected one unit at a time. However, two factors ameliorate these issues. First, since simulations provide a rough knowledge of capacitor settings for a given value of $3f_1$, the calibration need not begin with all of the capacitors disconnected. Second, the baseband dc value corresponding to the LNA output amplitude is more than one order of magnitude larger than the dc offset.

Next, we study the effect of I and Q phase imbalance, $\Delta\phi$, on the calibration (The gain imbalance has little effect.) Suppose the LNA incurs a phase shift of θ at $3f_1$, producing an output given by $A_0 \cos(\omega_{LO}t + \theta)$. The error component driving the LMS machine is thus given by

$$\begin{aligned} x_I^2 + x_Q^2 &= \alpha A_0^2 \left[\cos^2\theta + \sin^2(\theta - \Delta\phi)\right] \\ &= \alpha A_0^2 \left[1 + \frac{1}{2}\cos 2\theta - \frac{1}{2}\cos(2\theta - 2\Delta\phi)\right], \end{aligned} \tag{2.19}$$

where α is related to the conversion gain of the mixers. In the ideal case, only A_0 varies with the tuning code, but in practice, θ does, too. With $\Delta\phi = 0$, the change in θ would not matter and $x_I^2 + x_Q^2$ would remain a monotonic function of the tuning code. Equation (19) suggests that the effect of $\Delta\phi$ is maximum for $\theta = 45^\circ$ (because the slope of $\cos 2\theta$ is maximum at this angle). To avoid this issue, the worst-case change in $x_I^2 + x_Q^2$ must still be monotonic. Since A_0 and θ vary by as much as 15% and 20° for consecutive codes, we have

$$\begin{aligned} &\alpha A_0^2 \left[1 + \frac{1}{2}\cos 90^\circ - \frac{1}{2}\cos(90^\circ - 2\Delta\phi)\right] \quad < \\ &\alpha (1.15A_0)^2 \left[1 + \frac{1}{2}\cos 110^\circ - \frac{1}{2}\cos(110^\circ - 2\Delta\phi)\right], \end{aligned} \tag{2.20}$$

and hence

$$\Delta\phi < 25^\circ \tag{2.21}$$

This upper bound on I and Q phase mismatch is fairly easy to guarantee.

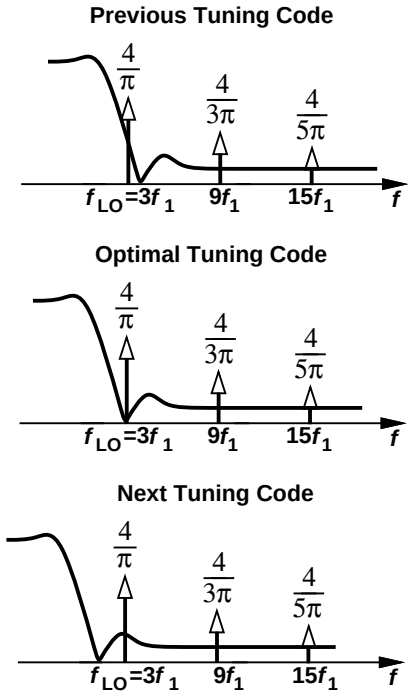


Figure 2.16: Harmonics of the test signal around the optimal tuning code.

The last issue relates to the harmonics of the the test signal. Since the LO waveform, especially at frequencies below a few gigahertz, may contain significant harmonics, we must determine their effect after they are mixed with the LO harmonics. Fortunately, as illustrated in Fig. 2.16, the harmonics of the test signal are heavily attenuated by the LNA in the vicinity of the optimal tuning code. If the tuning code is far from optimum, the sinc envelope of the harmonics still guarantees that $x_I^2 + x_Q^2$ varies monotonically with the code.

2.4 Experimental Results

The proposed harmonic-rejecting LNA has been fabricated in TSMC's 65-nm digital CMOS technology. Figure 2.17 shows the LNA core die, which measures

about 100μm×120μm. Operating with a 1.2-V supply, the main path of the circuit draws 7.54 mW and the three auxiliary paths a total of 1.1 mW. The unit capacitors in the programmable arrays vary from 18 fF to 1.68 pF. The total capacitance is 16.6 pF, occupying an area of around 70μm×70μm. The die is directly mounted on and bonded to a printed-circuit board, but the RF input and output pads are accessed by high-frequency probes. An on-chip serial bus controls the capacitor arrays.

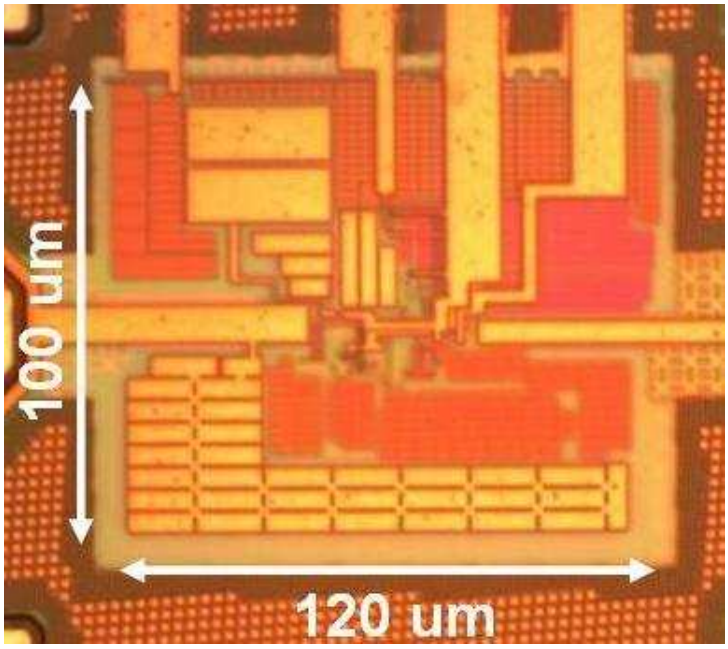


Figure 2.17: LNA die photograph.

Figure 2.18 plots the measured LNA gain as a function of frequency for various tuning codes. The harmonic rejection is at least 20 dB for all settings. The dip in the response around 700 MHz is attributed to the resonance between the supply bond wire inductance and the on-chip bypass capacitor.

Figure 2.19 plots the measured noise figure and S_{11} while harmonic rejection is off. The NF remains below 3 dB from 300 MHz to around 4 GHz. The NF rises at low frequencies due to the flicker noise of the current mirror for the 3.7-mA

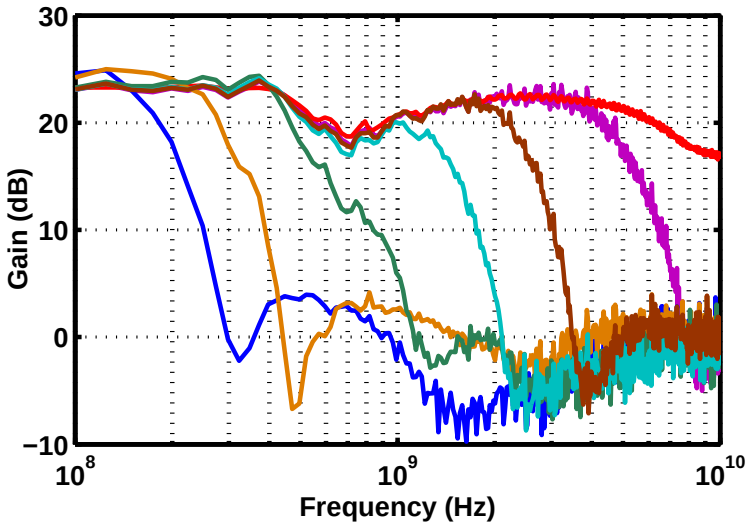


Figure 2.18: Measured LNA gain for various tuning codes.

source in Fig. 2.9(a) and at high frequencies due to the roll-off in the open-loop gain. The S_{11} is less than -12 dB across the entire band.

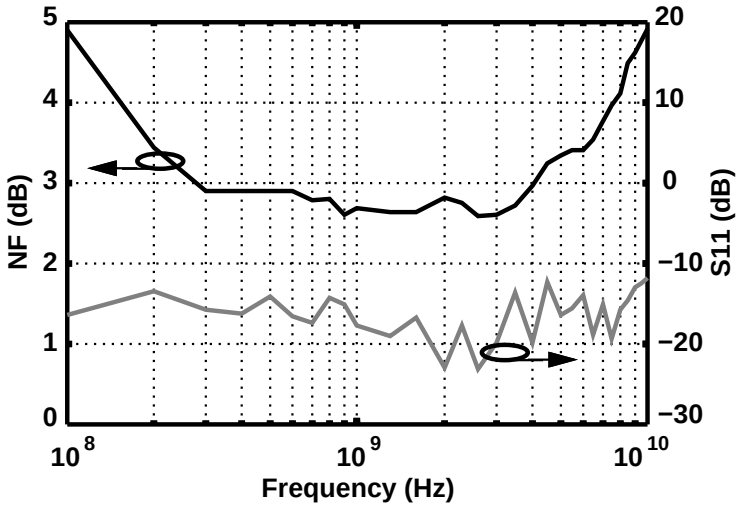


Figure 2.19: Measured NF and S_{11} with harmonic rejection off.

Figure 2.20 plots the measured noise figure when harmonic rejection is on and off. With harmonic rejection, the noise figure is measured at the input frequency of f_1 while the notch frequency, $3f_1$, varies from 300 MHz to 10 GHz. The worst-

case NF degradation due to frequency response shaping occurs for f_1 around 750 MHz. This is because for higher values of f_1, $H_2(s)$ and $H_3(s)$ in Fig. 2.9(a) are turned off, contributing no noise. Figure 2.21 plots the measured NF and S_{11} for this case, revealing about 1 dB of noise penalty at 750 MHz. According to measurements, S_{11} is less than -10 dB for all capacitor settings.

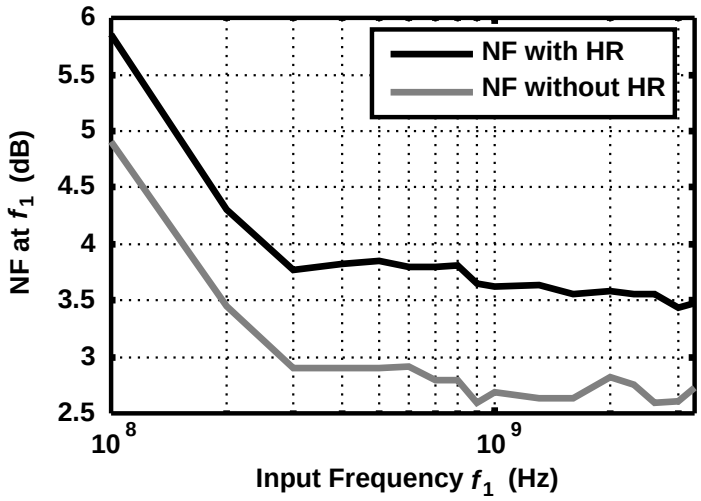


Figure 2.20: Measured NF at f_1 when harmonic rejection on and off (HR remains off for f_1 >3.3 GHz).

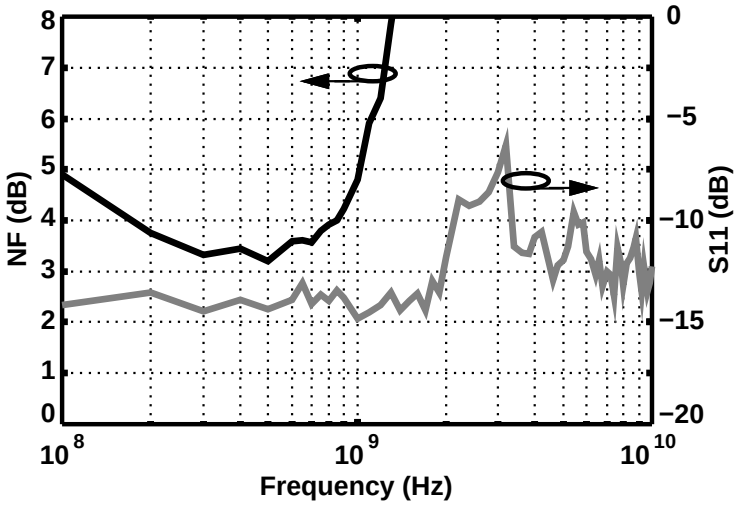


Figure 2.21: Measured NF and S_{11} with harmonic rejection on ($f_1 = 750$ MHz).

Figure 2.22 plots the measured noise figure in the presence of an out-of-band blocker at $3f_1 = 2.2$ GHz as a function of the blocker level. As expected, for blocker levels higher than the 1-dB compression point, the circuit experiences substantial non-linearity, exhibiting a higher NF. That is, as the blocker at the LO harmonic exceeds approximately -25 dBm, the receiver sensitivity begins to degrade. However, if a receiver sensing such a blocker level targets an LO harmonic rejection of, say, 60 dB, then it cannot operate properly with desired input levels below roughly -95 dBm anyway and hence does not require such a low noise figure.

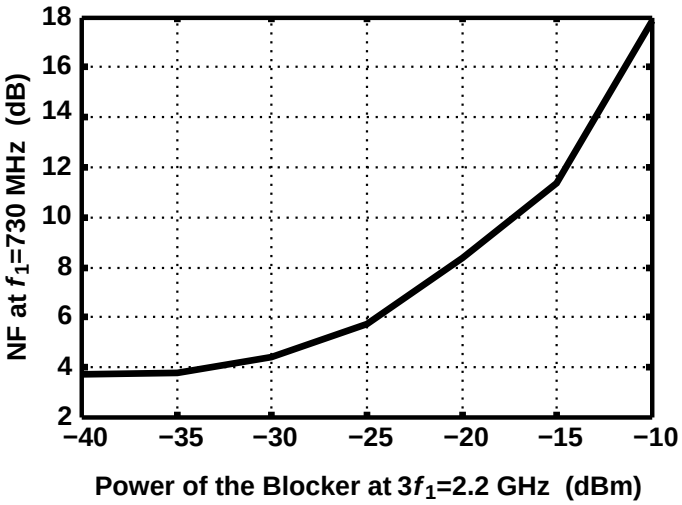


Figure 2.22: Measured NF at f_1 with blocker at $3f_1$ ($f_1 = 730$ MHz).

The calibration algorithm proposed in Section 2.4 has also been verified experimentally. In this test, the LNA input and output are connected to an RF generator and a spectrum analyzer, respectively, and the remainder of the system shown in Fig. 2.15 is realized in Matlab. The loop controls the notch frequency through the on-chip serial bus. Figure 2.23 shows how the LMS algorithm evolves for $3f_1 = 2.4$ GHz. Plotted here is $10\log(x_I^2 + x_Q^2)$ as a measure of the LNA's rejection at $3f_1$ as the calibration proceeds and the loop converges. Starting from

the smallest tuning code (the highest notch frequency), the system increases the capacitances until it finds the minimum error. In this example, the loop converges after 10 iterations. The insets show the measured LNA frequency response for some of the steps to confirm the correlation between $x_I^2 + x_Q^2$ and the amount of rejection. We observe that $x_I^2 + x_Q^2$ drops by 25 dB from the beginning to the maxima in the steady state, yielding a similar attenuation for $3f_1$. Rejection swings between 25 dB and 35 dB in the steady state.

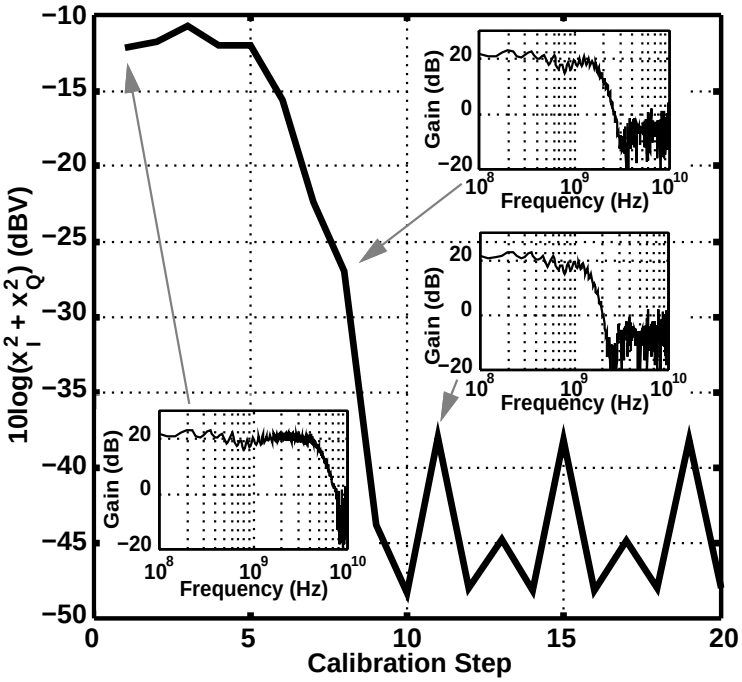


Figure 2.23: Time evolution of calibration loop with a 2.4-GHz test signal.

It is difficult to make a fair comparison between this work and prior art as LNAs typically do not provide harmonic rejection. Nevertheless, as a reference, the design in [14] is compared with our work in Table 3.1. We observe that, in addition to harmonic rejection, our LNA achieves nearly twice the bandwidth at 62% of the power consumption and with comparable noise figure while sacrificing linearity.

Table 2.1: LNA performance summary and comparison

	This Work	[14]
Frequency Band	0.1 ~ 10 GHz	0.2 ~ 5.2 GHz
Notch Frequency	0.3~10 GHz	N/A
Harmonic Rejection	> 20 dB	N/A
Supply Voltage	1.2 V	1.2 V
Power Consumption	8.64 mW	14 mW
Gain	17 ~ 24 dB	13 ~ 15.6 dB
NF (HR off, 100 MHz ~ 10 GHz)	2.59 ~ 4.92 dB	< 3.5 dB
NF (HR on, 100 MHz ~ 3.3 GHz)	3.5 ~ 5.84 dB	N/A
S_{11}	−23 ~ −11.7 dB	< −10 dB
IIP_2	1 ~ 5 dBm	> 20 dBm
IIP_3	−15 ~ −12 dBm	> 0 dBm
CMOS Technology	65 nm	65 nm

It is worth noting that the overall linearity of most RF receivers is limited by the downconversion mixers and the baseband amplifiers rather than by the LNA. For example, with an LNA gain of 24 dB and an IIP_3 of -15 dBm, the mixers must exhibit an IIP_3 of greater than $+18$ dBm if they must not degrade the receiver IP_3 by more than 0.5 dB. Such high mixer IP_3 values are extremely difficult to achieve. Thus, our LNA is unlikely to limit the receiver linearity.

2.5 Conclusion

The problem of harmonic rejection in broadband RF receivers can be greatly relaxed if the LNA attenuates blockers at the LO harmonics. This work presents a number of frequency response shaping techniques and a calibration algorithm that allow tuning the rejection frequency from 300 MHz to 10 GHz. A feedback LNA incorporates feedforward and unilateral Miller capacitor multiplication with

sufficient resolution to attenuate blockers with channel bandwidths as much as 20 MHz. The calibration algorithm utilizes a direct-conversion receiver environment to derive a dc error and force it toward zero.

CHAPTER 3

GSM/WCDMA Receiver with RF Channel Selection

One of the biggest challenges for realizing broadband radios is the existence of blockers around the desired channel compelling transceivers to employ SAW filters to suppress those blockers. Since such filters are not tunable to various frequency bands, sustaining blockers without SAW filters has been the key for SDR and CR.

Among the multiple efforts published, [15] has first suggested the N-path filter as a possible solution. Operated by the local oscillator (LO) signal, the N-path filter creates the high-Q band-pass filter (BPF) around the LO frequency and filters out blockers. However, the bandwidth of the BPF is limited by the load capacitor and the receiver requires a significant power in the LO distribution network. [16] employs N-path filter in the feedback path to increase Q of the BPF and stop-band rejection by the amount of the loop gain. However, the power consumption exceeds 60 mW, mainly consumed by the baseband amplifier. Other works[17]-[19] also have tried different architectures with the N-path filter or the mixer-first architecture to achieve high-Q filtering, but sharp channel selection with low power consumption has not been achieved.

This chapter introduces a new high-Q RF channel-selection receiver architecture operating from 50 MHz to 2.5 GHz. The receiver employs the 8-path notch

filter in the feedback network to reduce the required capacitance and the switch size, consequently, reducing the chip area and the power dissipation of the LO distribution network drastically. Also incorporating the 8-path notch filter in the unilateral feedback path, the receiver achieves 15-dB rejection at the center of the next adjacent channel at RF frequency. Fabricated in 65-nm digital CMOS technology, the receiver consumes 20 mW with a 1.2-V supply.

3.1 Background

Figure 3.1 describes a generic wideband receiver supporting various communication standards. In this scenario, blockers exist either close to or far from the desired signal frequency, f_0. The two blockers placed at f_1 and f_2, where $2f_1 - f_2 = f_0$, produce the third intermodulation distortion component at f_0 on top of the desired signal disturbing signal reception. Also, absent of filtering, these blockers themselves saturate and desensitize the receiver. Under this situation, placing a high-order filter at baseband is useless because the receiver is already saturated. To prevent the saturation, the receiver must employ a BPF at RF frequency before the LNA.

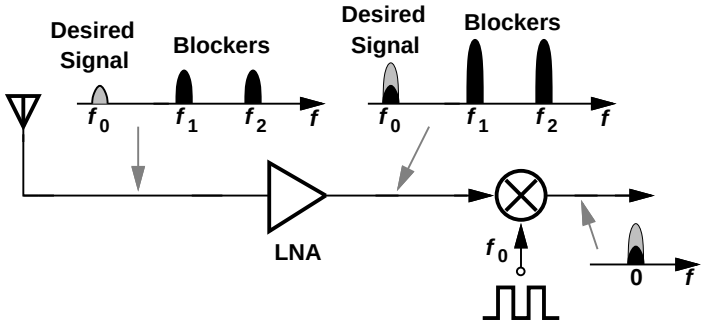


Figure 3.1: Generic broadband receiver.

The N-path filter, originally proposed in early 1970s [20] to avoid unrealis-

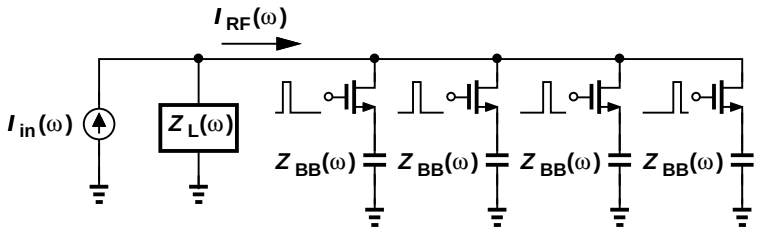


Figure 3.2: 4-path filter with capacitive loads.

tically large inductor in a BPF design at a low frequency, has been revisited to provide a sharp BPF at RF frequency [15]. [21] has analyzed the frequency response of the 4-path filter described in Fig. 3.2. The 4-path filter consists of four switches driven by a 25% duty-cycle non-overlapping LO signal and four load impedances, $Z_{BB}(\omega)$, attached to the current source and the source impedance, $R_S(\omega)$. The transfer function, $Z_{RF}(\omega)$, can be described in (3.1).

$$Z_{RF}(\omega) = \frac{V_{RF}(\omega)}{I_{in}(\omega)} = \left[R_{SW} || R_S + \frac{\left(\frac{R_S}{R_S + R_{SW}}\right)^2 \frac{2}{\pi^2} Z_{BB}(\omega - \omega_{LO})}{1 + \frac{1}{4}\frac{Z_{BB}(\omega - \omega_{LO})}{R_S + R_{SW}}} \right], \quad (3.1)$$

where R_{SW} is the on-resistance of the switch. Particularly when the load impedance is only a capacitor, C_{BB}, (3.1) becomes

$$Z_{RF}(\omega) = \frac{V_{RF}(\omega)}{I_{in}(\omega)} = \frac{R_S}{R_S + R_{SW}} \left[R_{SW} + \frac{\frac{8}{\pi^2} R_S}{1 + j4C_{BB}\left(R_S + R_{SW}\right)(\omega - \omega_{LO})} \right]. \quad (3.2)$$

The equation (3.2) implies that as the input frequency moves apart from LO frequency, the gain becomes smaller showing band-pass filtering. It also shows that C_{BB} determines the 3-dB bandwidth, while the ratio between R_S and R_{SW} decides the amount of rejection at stop band. The presented 4-path filter requires larger C_{BB} for higher-Q of the filter, and a larger switch size for greater stop-band rejection. The larger capacitor value directly increases die area, while

the larger switch size requires greater power consumption for LO distribution network. These are the main challenges that must be answered to implement a single receiver satisfying all the requirements of various standards.

[17], [18] have placed the multiple 4-path filters from the input of the LNA to the Mixers for greater stop-band rejection. For example, the 4-path filter attached at the output of the LNA experiences the output impedance of the LNA as $Z_L(\omega)$ in Fig. 3.2, which generally far exceeds 50 Ω. In this case, this 4-path filter exhibits a greater rejection than the 4-path filter with $R_S = 50\ \Omega$. Although, this attempt achieves the reasonable stop-band rejection, the switch size is still large causing a huge amount of power consumption in the LO distribution network.

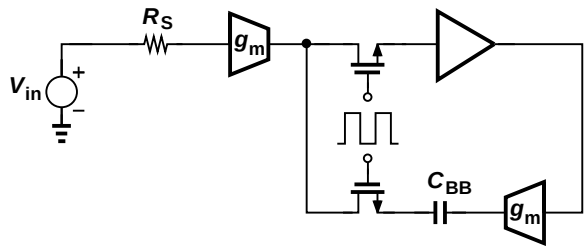


Figure 3.3: 4-path filter with capacitive loads in feedback.

[16] introduces an interesting approach to improve the stop-band rejection as shown in Fig. 3.3. It applies the 4-path filter in the feedback path. Each path of this feedback includes a baseband amplifier and a capacitor. Since the feedback has a 20-dB voltage gain, the rejection extends to 48 dB with smaller switch sizes, thus minimizing the LO power consumption. However, this approach still demands a huge amount of power for the baseband amplifiers because the baseband amplifier must drive a 15-pF load. Also, the input impedance matching cannot be easily achieved without NF degradation in this topology.

While the previous works have tried to improve the stop-band rejection, they have not provided how to deal with a large capacitor value in the 4-path filter.

Since the load capacitor value determines the 3-dB bandwidth of the filter, an unrealistically large capacitor value is necessary for a 200-kHz bandwidth. For example, if we redesign [18] to provide a 200-kHz 3-dB bandwidth, we require a total of approximately 30 nF, which is inacceptable.

3.2 High-Q Channel-Selection Receiver Design

3.2.1 N-Path Notch Filter in Feedback

An N-path notch filter [22], [23], exploiting a conventional N-path filter has been introduced to reject a blocker for different frequencies. Consider an 8-path notch filter in the feedback path around the amplifier as shown in the Fig. 3.4(a). With a notch filter in the feedback, the whole system operates as a BPF. Each path has two switches around the feedback capacitor, C_F. Simplified, Fig. 3.4(a) can be redrawn as Fig. 3.4(b), which is different from the original 8-path filter.

The original 8-path filter's input impedance is [8]

$$Z_{in}(\omega) = R_{SW} + 8 \sum_{n=-\infty}^{n=\infty} \frac{|a_n|^2}{jC_{BB}(\omega - n\omega_{LO})}, \tag{3.3}$$

where a_n is Fourier coefficient and C_{BB} a baseband impedance. For the fair comparison, we assume that the total width of two switches of each path in Fig. 3.4(b) is the same with the size of each switch in Fig. 3.2. Thus, the input impedance of the 8-path filter in feedback becomes

$$Z_{in,fb}(\omega) = \frac{4R_{SW}}{1 + A_0} + 8 \sum_{n=-\infty}^{n=\infty} \frac{|a_n|^2}{j(1 + A_0)C_F(\omega - n\omega_{LO})}, \tag{3.4}$$

where A_0 represents the gain of the amplifier in Fig. 3.4(a). Now, particularly adding the current source and the source resistor, R_S, at the input of the 8-path

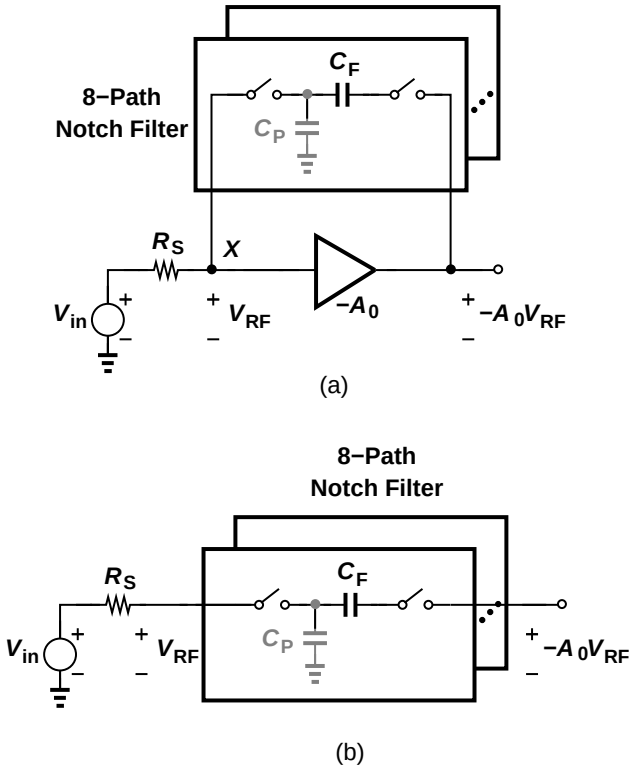


Figure 3.4: (a) 8-path filter with capacitive loads in feedback (b) Simplified circuit diagram.

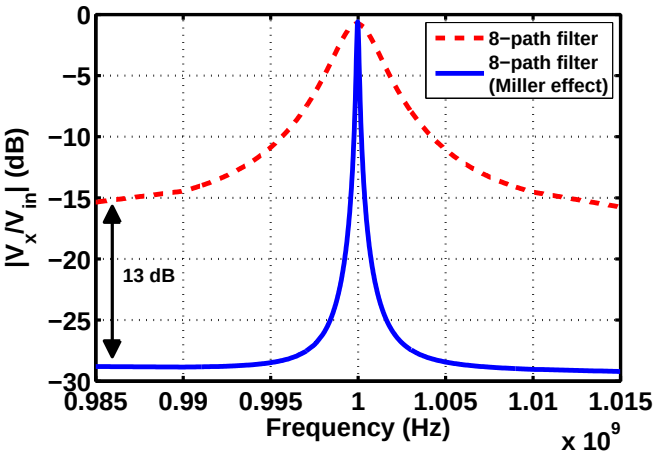
filter, the transfer function becomes

$$\frac{V_{RF}(\omega)}{I_{in}(\omega)} = \frac{R_S}{R_S + \dfrac{4R_{SW}}{1+A_0}} \left[\frac{4R_{SW}}{1+A_0} + \frac{\dfrac{16}{\pi^2}\left(2-\sqrt{2}\right) R_S}{1 + j8(1+A_0)C_F \left(R_S + \dfrac{R_{SW}}{1+A_0} \right) (\omega - \omega_{LO})} \right]. \tag{3.5}$$

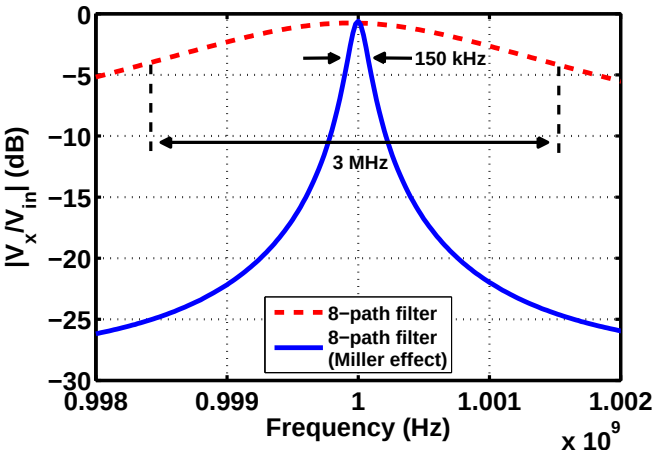
Assuming $A_0 = 20\ dB$, (3.4) and (3.5) indicate that the effective input on-resistance is reduced by around 60% and the effective baseband impedance is reduced by ten times compared to (3.2). This can be simply explained by Miller effect. If the switches are removed from Fig. 3.4(a), the circuit only consists of one amplifier and the feedback capacitor. Since the voltage across the capacitor is $1 + A_0$ times the input voltage, the effective capacitance becomes $1 + A_0$ times

larger. If we add two switches around the capacitor and turn them always on, the resistance due to switches exists in series with the capacitor. In contrast to the capacitance, the effective resistance becomes $1 + A_0$ times smaller. Now, LO signal with 12.5% duty cycle drives the switches. Although it is convenient to think that impedance of C_F has been moved to f_{LO}, it is important to note that what actually has been moved is the signal itself. After the amplifier, the signal is downconverted by one switch, experiences C_F, and is upconverted by the other switch to the original frequency. Thus, the signal sees the feedback capacitor as just a capacitor, experiencing the Miller effect.

Figure 3.5 compares the frequency response of a conventional 8-path filter and the proposed 8-path filter with Miller effect. The configuration for the conventional 8-path filter is 8-phase version of Fig. 3.2, while the proposed 8-path filter is shown in Fig. 3.4(a) with $A_0 = 26$ dB. In this simulation, for the fair comparison, $C_{BB} = C_F = 250$ pF, and the total switch sizes are equal. As indicated in Fig. 3.5, the proposed 8-path filter with Miller effect shows a 13-dB greater stop-band rejection and 20 times narrower 3-dB bandwidth. In other words, when $A_0 = 26$ dB, the 8-path filter incorporated with the feedback can save around 75% of the LO power consumption and 95% of the capacitor area. Of course, we must consider the power consumption of the feedback amplifier in the end. Nonetheless, this amount of power and area saving is significant. It is also important to note that the proposed BPF is created at the input of the LNA, much more effective in suppressing possible blockers than a BPF at the output of the LNA.



(a)



(b)

Figure 3.5: (a) Stop-band rejection for 8-path filter and 8-path filter with Miller effect (b) 3-dB bandwidth for 8-path filter and 8-path filter with Miller effect.

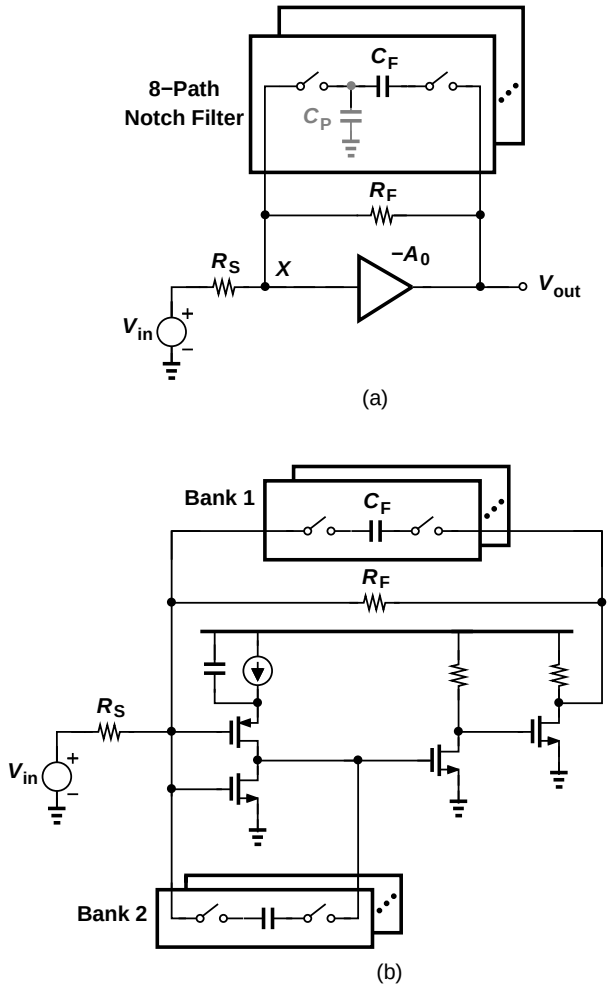


Figure 3.6: (a) 8-path filter in resistive-feedback LNA (b) three-stage resistive-feedback LNA with n-path filter.

3.2.2 LNA with N-Path Notch Filter in Feedback

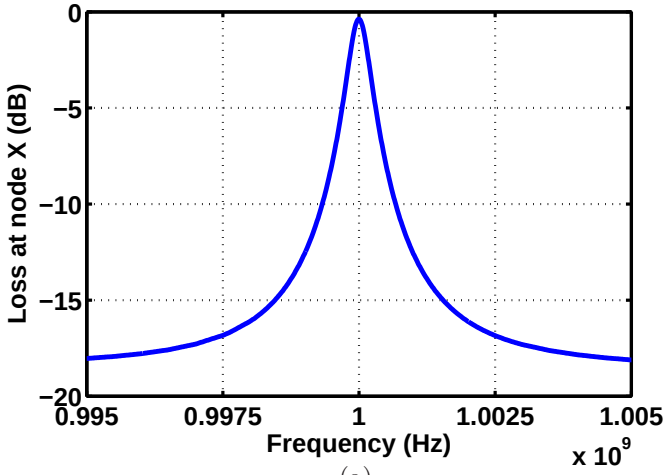
The previous section proves that placing an 8-path notch filter in the feedback path increases both the stop-band rejection and filter selectivity while consuming the same LO power and occupying the same area for the load capacitors. However, we are unable to use this circuit as an RF front end because when C_F is capacitive, the proposed circuit's input impedance becomes infinity around the LO frequency

being unable to provide 50 Ω matching as shown in (3.4). Interestingly, employing a resistor in parallel with the 8-path filter can simply solve this problem as shown in Fig. 3.6(a). The input impedance, then, becomes

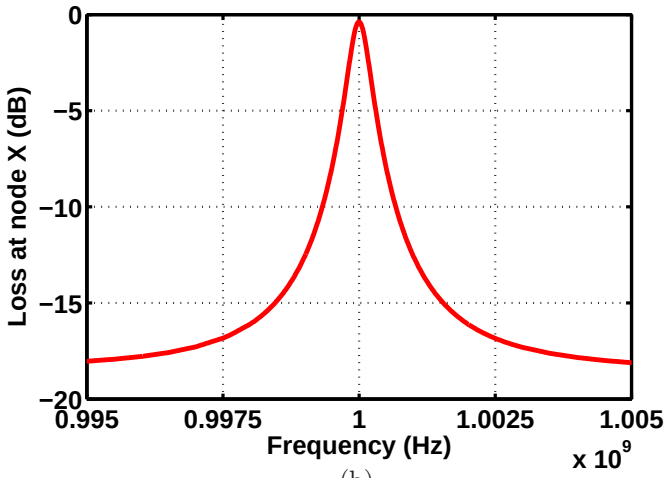
$$Z_{in,fb}(\omega) = \frac{R_F}{1+A_0} || \left[\frac{4R_{SW}}{1+A_0} + 8 \sum_{n=-\infty}^{n=\infty} \frac{|a_n|^2}{j(1+A_0)C_F(\omega - n\omega_{LO})} \right], \qquad (3.6)$$

where R_F is the feedback resistor. At $f = f_{LO}$, $Z_{in,fb}(\omega) \approx R_F/(1+A_0)$, since the capacitive impedance becomes infinity. In other words, the 8-path filter can be attached to a general resistive-feedback LNA to provide a BPF while the LNA still providing the input impedance matching around f_{LO}. Figure 3.7(a) shows the simulated frequency response of Fig. 3.4(a) with a $50-\Omega$ termination at the input, and Fig. 3.7(b) describes the frequency response of Fig. 3.6, both at the LNA output. Two frequency responses are almost identical indicating that R_F in the feedback path does provide the decent input impedance matching without degrading Q of the proposed BPF.

A three-stage resistive-feedback LNA [24] offers the good NF with the reasonable power consumption. However, this LNA suffers from the poor linearity (poor IIP_2 and IIP_3). Therefore, it is a good candidate to apply 8-path filter in parallel with R_F for the better linearity. Fig. 3.6(b) shows the combination of the three-stage resistive-feedback LNA and the 8-path notch filter in the feedback path. As a result, this configuration provides the good NF, the decent input impedance matching, and the good linearity with the low power consumption. For sharper filtering, another 8-path filter (bank 2) is introduced at the first stage of the LNA as depicted in Fig. 3.6(b). It is important to note that placing the 8-path filter at the first stage gives another benefit that it also creates a BPF at the output of the first stage of the LNA helping the blocker rejection. Despite Miller effect, the resulting bandwidth is still larger than 200 kHz.



(a)



(b)

Figure 3.7: (a) Frequency response with a $50-\Omega$ termination (b) frequency response with R_F in the feedback path.

3.2.3 Unilateral Miller Path

The larger voltage gain the signal obtains in Fig. 3.6(a), the larger Miller effect is applied to C_F. In addition to the LNA with the 8-path filters, an unilateral Miller path is introduced as shown in Fig. 3.8 to further improve Q of filtering. This path includes a switch, an amplifier, a capacitor, and another switch. The

first switch downconverts the signal to the baseband; the amplifier provides a gain to the signal; this signal passes the capacitor; and finally, the signal after the capacitor is fed back to the input after being upconverted by the other switch. The additional amplifier after the LNA further increases the gain applied to the capacitor so that this path can provide a sharper filtering around f_{LO}.

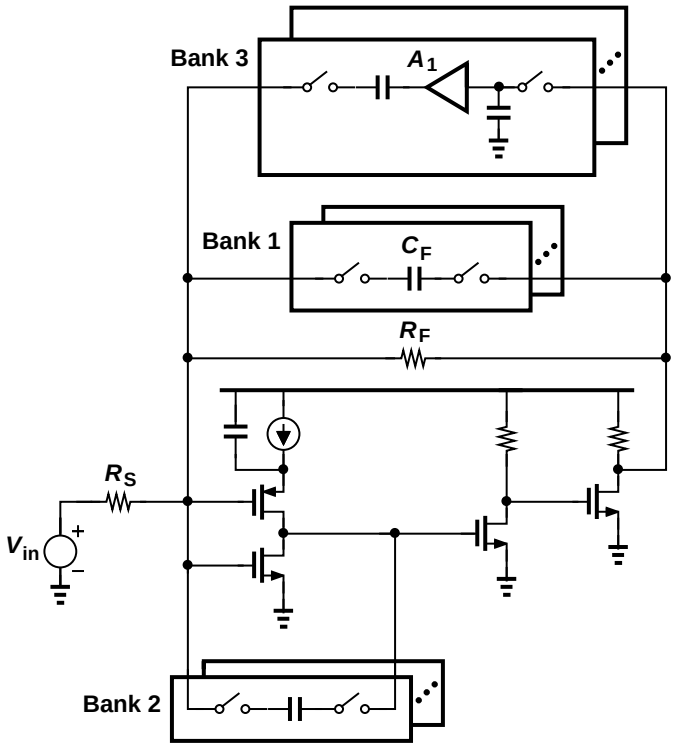


Figure 3.8: The LNA architecture with the unilateral Miller path.

Figure 3.9 plots the simulated frequency response at the LNA output. The 3-dB bandwidth of 200 kHz has been obtained with a 10-pF capacitor for each path, ten times smaller than C_F This is because the overall Miller multiplication exceeds 50 dB for bank 3, hence considerably reducing the required capacitance to earn a 200-kHz bandwidth. One interesting observation is that the center frequency of the resulting BPF is slightly shifted to the left. This issue will be discussed later in section 3.2.7.

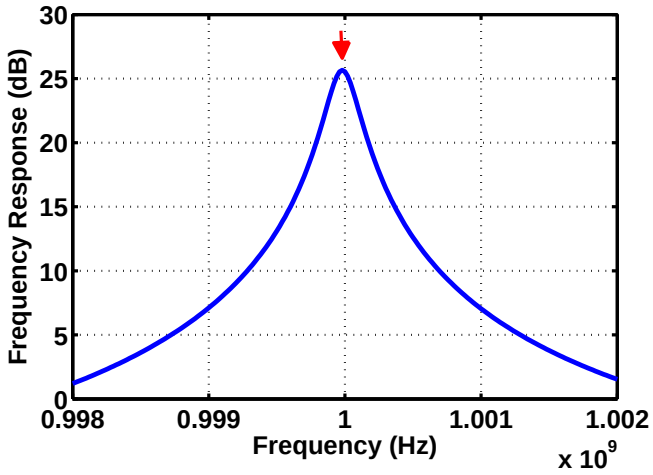


Figure 3.9: BPF around f_{LO} with unilateral Miller path.

3.2.4 Stability

Since an amplifier exists in the feedback path, the stability must be checked. The signal is downconverted by the switch after the LNA. This baseband signal is applied to the Miller amplifier whose bandwidth is limited by poles inside it, thus causing a significant phase shift at a certain frequency. Because of this phase shift, the voltage applied across the Miller capacitor has the according phase shift, so as to the current flowing through the Miller capacitor. In other words, the Miller capacitor is not a capacitor if seen at the input of the LNA. This significant phase shift even might exceeds 180° to create a positive feedback around the LNA bearing a potential stability issue. Thus, the design of the Miller amplifier is considerably important.

A simple solution is to design the Miller amplifier as one stage amplifier with a huge gain bandwidth. Because this amplifier only has one pole, a potential stability problem no more exists. However, a huge gain bandwidth impose a huge power consumption on this Miller amplifier. Fortunately, it is found that the feedback by C_F in Fig. 3.8 alleviates this issue. Because of C_F, the LNA's

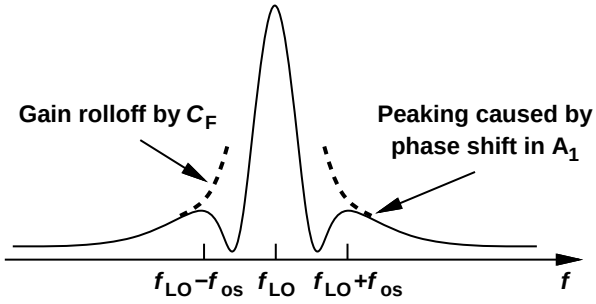


Figure 3.10: Peaking caused my A_1 and gain rolloff by C_F.

gain drops significantly at an offset frequency, $f \pm f_{OS}$ as shown in Fig. 3.10. Although the feedback by the Miller capacitor may creates a gain peaking, the circuit is stable because the loop gain is small enough. Thus, the Miller amplifier's gainbandwidth and power consumption is be determined by f_{OS}. To minimize the power consumption of the Miller amplifier, f_{OS} must be small. This can be achieved by employing a huge C_F to suppress a possible peaking at closer frequency to f_{LO}, showing a simple trade-off between the power consumption and area.

3.2.5 Noise Contribution of Miller Amplifier

Another issue in introducing the Miller amplifier is its noise contribution to the receiver. Usually, the noise in the feedback path directly appears at the output, requiring a special care in designing the circuit in the feedback path. Consider the circuit diagram described in Fig. 3.11.

Before writing the equation to find how n_i affects V_{out}, we assume the frequency conversion gain by the switches as unity. Ignoring $V_{in}(f)$, we obtain the equation as

$$-\frac{V_i(f)}{R_S} + \frac{V_{out}(f)}{R_F} = -A_1\{V_{out}(f) + n_i(f - f_{LO})\}j2\pi(f - f_{LO})C_M, \qquad (3.7)$$

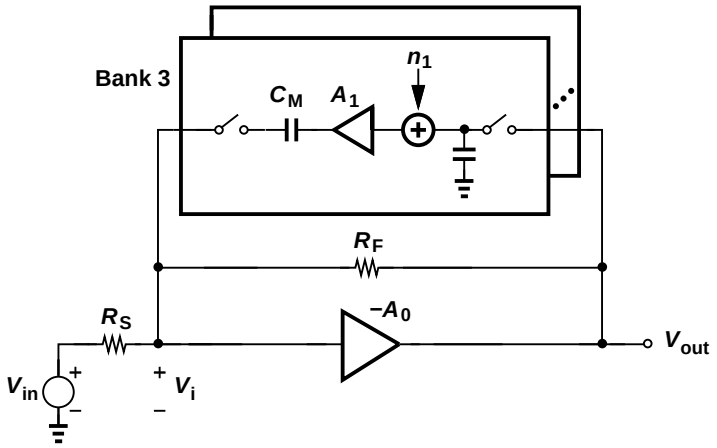


Figure 3.11: Noise contribution in the Miller amplifier.

where f_{LO} is the LO frequency driving the switches. Since $-A_0V_i(f) = V_{out}(f)$,

$$\frac{V_{out}(f)}{A_0R_S} + \frac{(1+A_0)V_{out}(f)}{A_0R_F} + \frac{1+A_0A_1}{A_0}j2\pi(f-f_{LO})C_MV_{out}(f)$$
$$+j2\pi(f-f_{LO})C_Mn_i(f-f_{LO}) = 0. \quad (3.8)$$

Finally, $V_{out}/n_i(f-f_{LO})$ can be expressed as

$$\frac{V_{out}(f)}{n_i(f-f_{LO})} = -\frac{A_0A_1R_SR_Fj2\pi(f-f_{LO})C_M}{R_F+(1+A_0)R_S+(1+A_0A_1)R_SR_Fj2\pi(f-f_{LO})C_M}. \quad (3.9)$$

As shown in (3.9), when $f = f_{LO}$, the noise cannot come out to the output. That is, the low frequency noise generated by the Miller amplifier, n_i, is blocked by C_M and does not easily affects the noise performance of the LNA around the frequency of f_{LO}. But, the flicker noise generated by the Miller amplifier still may be significant and possibly increase the NF of the LNA even after filtered by C_M. In this work, a long channel PMOS devices are chosen for the Miller amplifier to suppress the flicker noise of the Miller amplifier and prevent the possible NF degradation.

Figure 3.12 presents the noise transfer function as a function of offset frequency from f_{LO}. As the equation predicts, the noise from the Miller amplifier is high-pass filtered by C_M.

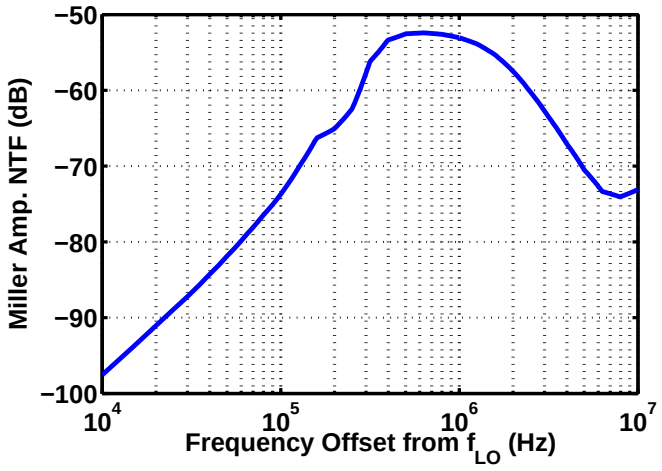


Figure 3.12: Noise transfer function V_{out}/n_i.

3.2.6 Higher-Order BPF

As discussed in section 3.2.3, the unilateral Miller path with 8-path notch filter provides sharper selectivity at RF frequency. However, this method does not increase the order of the filter, thus it is still the first-order BPF around f_{LO}. Is it possible to build a higher-order BPF at RF frequency?

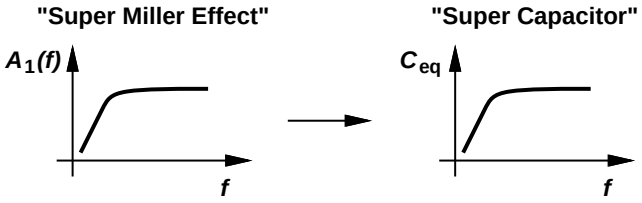


Figure 3.13: Frequency shaping and "super Miller" effect.

Consider a Miller amplifier with the frequency response of having a zero at DC and a pole at certain frequency as shown in Fig. 3.13. Since the gain of the Miller amplifier grows as frequency increases, the Miller effect also increases until the pole frequency. This growing Miller effect turns a capacitor in bank 3 in Fig. 3.8 into a "super-capacitor," enabling a sharper roll-off around f_{LO}, thus

increasing the order of the BPF.

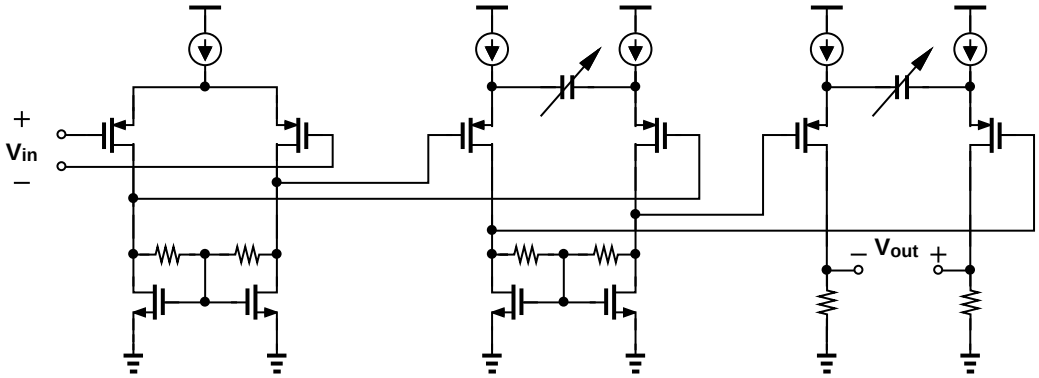


Figure 3.14: Miller amplifier in bank 3.

Now, consider a three-stage differential amplifier depicted in Fig. 3.14. The differential pairs of the second and third stages are source degenerated by a resistor and a capacitor array. This 6-bit capacitor array controls the zero frequency for the required 3-dB bandwidth of the BPF. To minimize the size of capacitor array, the differential pairs of the second and third stages consume a small amount of current providing a large impedance of the current sources. To provide a further larger impedance, the channel length of the current sources are chosen around 1 μm. The first stage's current is designed larger than the following stages to minimize noise of this amplifier. For the same reason, a zero is not inserted in the first stage. The size of the first stage's differential pair is properly chosen such that their flicker noise does not affect the overall NF. Again, although this three-stage Miller amplifier contains a number of poles degrading the phase margin, the circuit is stable with the help of C_F allowing that the Miller amplifier consumes a minimum power. Figure 3.15 plots the resulting frequency response of the Miller amplifier.

Figure 3.16 presents the higher-order BPF around f_{LO}. At around 1 GHz, Miller effect is minimum and the frequency response shows a flat response. As

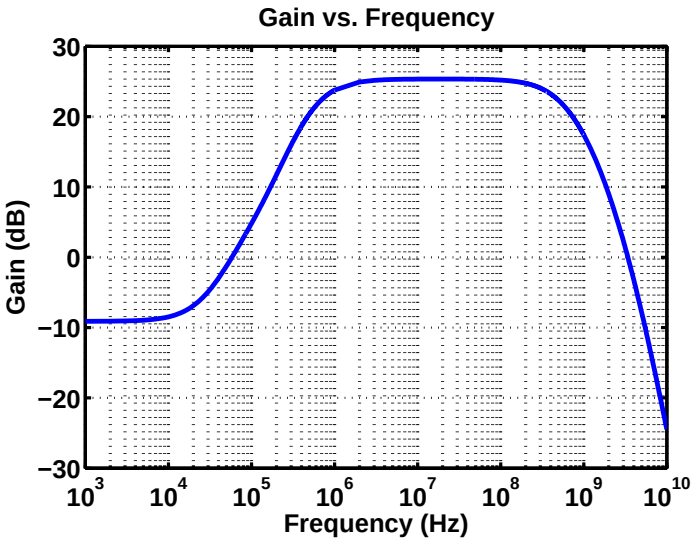


Figure 3.15: Frequency response of Miller amplifier.

the frequency departs from 1 GHz, Miller effect increases to provide sharp roll-off showing 20-dB rejection at the center of the next adjacent channel. This huge rejection at RF frequency alleviates the filter requirement of the baseband amplifier. However, the center frequency of this BPF is slightly shifted to the left showing asymmetric response.

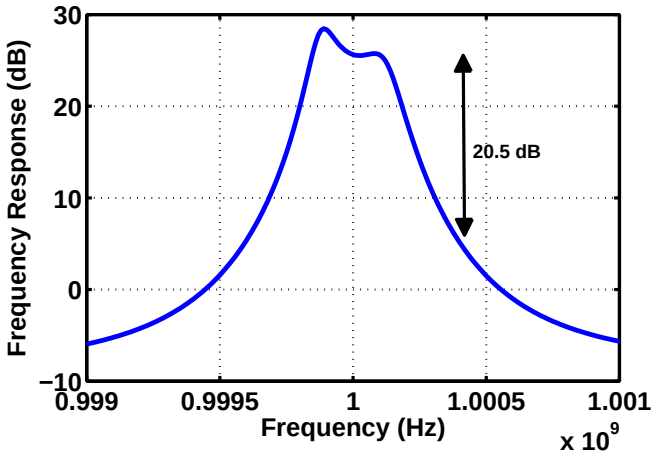


Figure 3.16: High-order BPF around f_{LO}.

3.2.7 Delay and the Center Frequency of the BPF

Employing the 8-path notch filter in feedback brings an unique problem. As shown in Fig. 3.16, the center frequency is slightly shifted to the lower frequency, which is not shown in the simulation with the ideal amplifier.

This frequency shift is caused by the native delay of the LNA and Miller amplifier. Ideally, the voltage after the Miller amplifier must be $-A_0(\omega)A_1(\omega)V_{in}(\omega)$. However, because of the delay, the voltage after the LNA and Miller amplifier becomes $-A_0(\omega)A_1(\omega)V_{in}(\omega)e^{-jt_d\omega}$, where t_d is the delay of the loop, resulting the frequency-dependent phase shift in the current flowing through the 8-path filter. Indeed, this frequency shift is minimum at 50 MHz and maximum at 2.5 GHz.

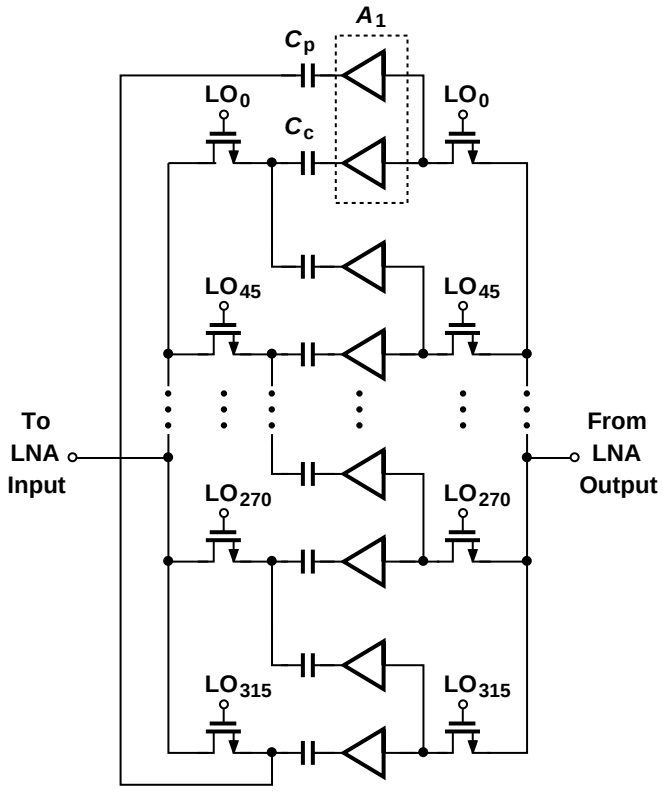


Figure 3.17: Polyphase 8-path notch filter.

Consider a polyphase 8-path notch filter in the feedback as shown in Fig. 3.17.

From the LNA output, another set of switches and capacitors is employed. Similar to the original 8-path filter, each path consists of a capacitor and two switches around it. The only difference is the LO phase that drives the two switches in each path. The switch close to the LNA output is driven by LO_{n+1} and the other switch close to the input is driven by LO_n, while the two switches in the original 8-path filter are driven by the same LO signal. This configuration feeds the output signal of the current phase back to the input signal of the previous phase, canceling the phase shift created by the delay of the LNA and Miller amplifier. In other words, when we measure the current at the input of the LNA flowing through the 8-path filter, its phase shift must not be affected by the delay of the LNA and Miller amplifier.

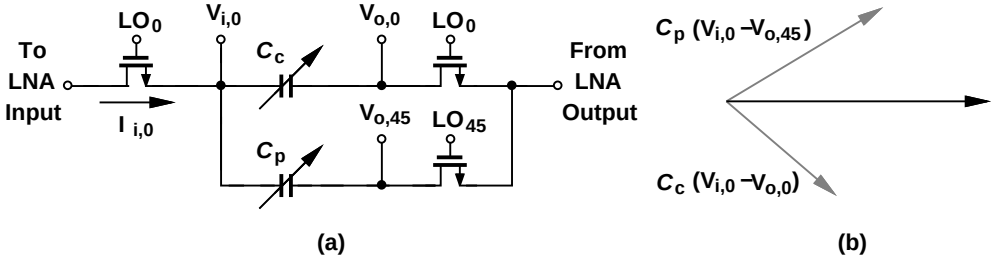


Figure 3.18: (a) Simplified circuit for modified 8-path filter (b) vector summation.

The simplified circuit is drawn in Fig. 3.18(a). The input and output signals are downconverted to become $V_{i,0}$ and $V_{o,0}$ by the switches driven by LO_0 at the left and right plate of C_c. The output signal once again downconverted by LO_{45} at the right plate of C_p. If we assume the total voltage gain and the delay from $V_{i,0}$ to $V_{o,0}$ as $-A_{BB}$ and t_d, respectively,

$$V_{o,0}(\omega) = -A_{BB}V_{i,0}(\omega)\, e^{-j2\pi\frac{t_d}{T}}, \tag{3.10}$$

where $T = 1/f_{LO}$. Since $V_{o,45}$ is a different version of $V_{o,0}$ with a phase lead,

$$V_{o,45}(\omega) = -A_{BB}V_{i,0}(\omega)\, e^{-j2\pi\left(\frac{t_d}{T}-\frac{1}{8}\right)}. \tag{3.11}$$

Now, if we calculate the net current flowing from the input of the LNA to the output of the LNA,

$$I_{i,0}(\omega) = V_{i,0}(\omega)\left[j\omega C_c\left(1 + A_{BB}e^{-j2\pi\frac{t_d}{T}}\right) + j\omega C_p\left(1 + A_{BB}e^{-j2\pi\left(\frac{t_d}{T}-\frac{1}{8}\right)}\right)\right]. \tag{3.12}$$

To make $i_{i,0}(\omega)$ purely imaginary as shown in Fig. 3.18(b),

$$C_c \sin\left(2\pi\frac{t_d}{T}\right) + C_p \sin\left(2\pi\left(\frac{t_d}{T} - \frac{1}{8}\right)\right) = 0. \tag{3.13}$$

Finally, we can derive the capacitor ratio, C_c/C_c to calibrate the frequency shift caused by the delay as

$$\frac{C_c}{C_p} = \frac{\sin\left(2\pi\left(\frac{1}{8} - \frac{t_d}{T}\right)\right)}{\sin\left(2\pi\frac{t_d}{T}\right)}. \tag{3.14}$$

The bandwidth of the BPF is function of the vector sum of the feedback capacitors, C_c and C_p. For example, the total effective capacitance is maximum as $C_c + C_p$ when $t_d = 0$, and it slightly decreases as t_d increases. Overall, this modification does not significantly affect the resulting bandwidth. Here in this work, bank 1 and bank 3 are polyphase 8-path filters. Figure 3.19 shows how the frequency shift is calibrated by adjusting the capacitor ratio, C_c/C_p. This adjustment shifts the center frequency back to 1 GHz to provide a flat response around 1 GHz.

3.2.8 Sampling Mixer in N-Path Filter

Another interesting aspect of the proposed work is that it downconverts the RF signal to the baseband in the middle of the feedback process. As shown in Fig 3.20(a), the switch in bank 1 at the LNA output downconverts the amplified signal to the baseband, operating as a sampling mixer with eight phases. Now,

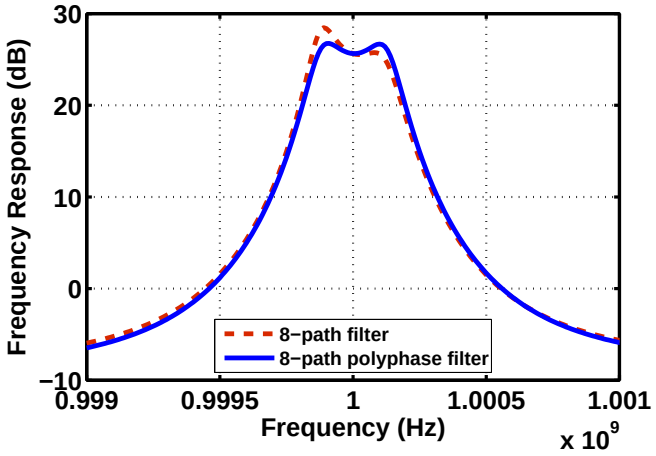


Figure 3.19: Frequency response with polyphase notch filter.

the baseband g_m stage following this sampling mixer senses the signal in each phase and converts the sensed voltage to current. As shown in Fig. 3.20(b), this current is properly ratioed and added at the output such that the baseband amplifier produces quadrature outputs rejecting $(8n-4\pm1)$th harmonics. Here, V_0, V_{45}, ..., V_{315} represent the baseband signals downconverted by LO_0, LO_{45}, ..., LO_{315}, respectively.

As [25] presents, the noise from harmonics may significantly degrades the NF of the receiver if not carefully designed. Although the 8-path filter passes only inband signal around f_{LO}, it also passes signals around harmonics at $2f_{LO}$, $3f_{LO}$, $\cdots$. Taking a differential mixer output rejects all even harmonics, but odd harmonics remain and downconvert the noise around those harmonics to the baseband degrading the NF. This noise can be rejected by harmonic rejection [5] in baseband amplifier as shown in Fig. 3.20(b). Simulation shows that the harmonic rejection improves the NF at the baseband output by 3 dB. Also for GSM, the flicker noise of the baseband amplifier must be small enough not to

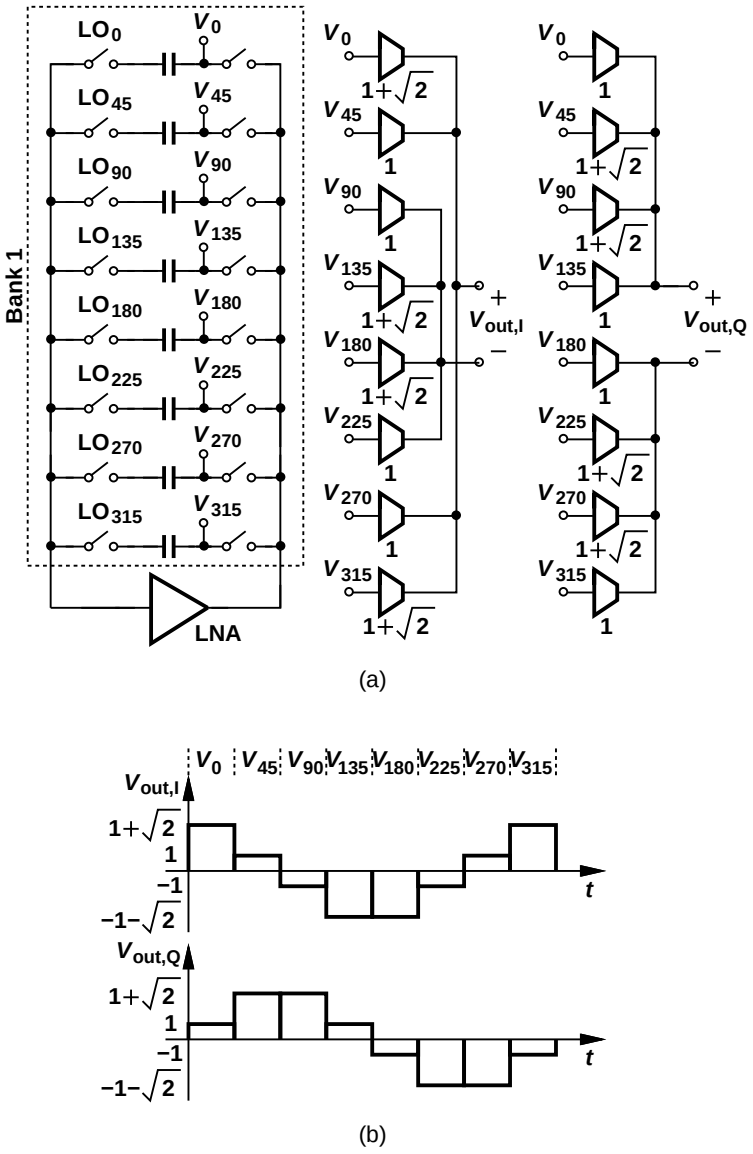
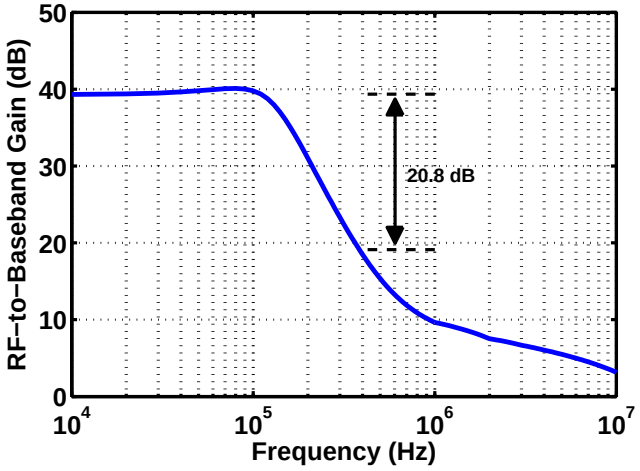


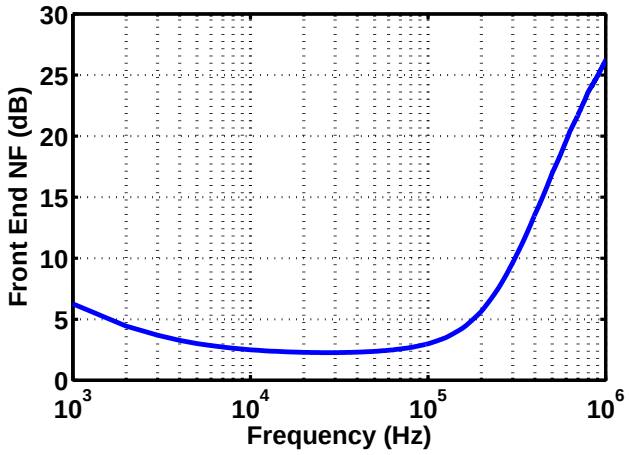
Figure 3.20: (a) Sampling mixer and baseband g_m stage (b) properly ratioed baseband output for quadrature signals with harmonic rejection.

degrade the NF at 10 kHz baseband frequency. To suppress the flicker noise, a $1.2-\mu m$ long PMOS pair is used for the input device and current source. Again, the input capacitance of the baseband amplifier do not load the LNA output since this impedance is upconverted around f_{LO}.

Figure 3.21(a) presents the simulated RF-to-baseband gain for GSM, showing over 20-dB rejection at the center of the next adjacent channel. The NF shown in Fig. 3.21(b) is higher than the simulated NF at RF frequency because the noise of the baseband amplifier has been added. The resulting NF penalty due to the baseband amplifier is 0.4 dB at 50 kHz with a 1.2-mW total power consumption



(a)



(b)

Figure 3.21: (a) RF-to-baseband gain (b) receiver NF.

3.2.9 LO Generation

One requirement for the 8-path filter is multi-phase non-overlapping clock generation with 12.5% duty cycle. To generate this clock, [8] employs eight flip-flops, reading the states of following stages and setting the stage's state to zero if one of following stages' state is one. This method, however, suffers from heavy loading in reading other stages' states, requiring a large power consumption for LO distribution network.

Figure 3.22(a). describes the proposed multi-phase clock generation. The differential $4f_{LO}$ input is divided by two to become four-phase $2f_{LO}$, and $2f_{LO}$ clock signals are fed to the quadrature divided-by-two circuit again to generate eight-phase f_{LO} signal. The quadrature divide-by-two circuit generates f_{LO} in order. This phase order must be guaranteed to properly generate the quarature outputs with harmonic rejection.

Now, an AND gate, G_1, accepts a $4f_{LO}$, a $2f_{LO}$, and a f_{LO} signal to produce a f_{LO} clock signal with 12.5% duty cycle. The detailed AND gate is shown in Fig. 3.22(b). The drain node of the transistor whose gate is driven by $4f_{LO}$ clock is shared by three other AND gates whose $4f_{LO}$ phase is the same enhancing the pulling down of the drain node. Similarly, the drain node of the transistor whose gate is driven by $2f_{LO}$ is shared by the other AND gate whose $2f_{LO}$ phase is the same. The output node of NAND gate drives an inverter that drives the switches in Fig. 3.8. Overall, LO distribution network consumes 7.2 mW at f_{LO}=2 GHz, while [8] consumes 30 mW for LO distribution circuit at 2 GHz. It is also important to note that one reason for much less power consumption for LO distribution network is that Miller effect reduces the effective resistance of switches allowing us to use smaller switches.

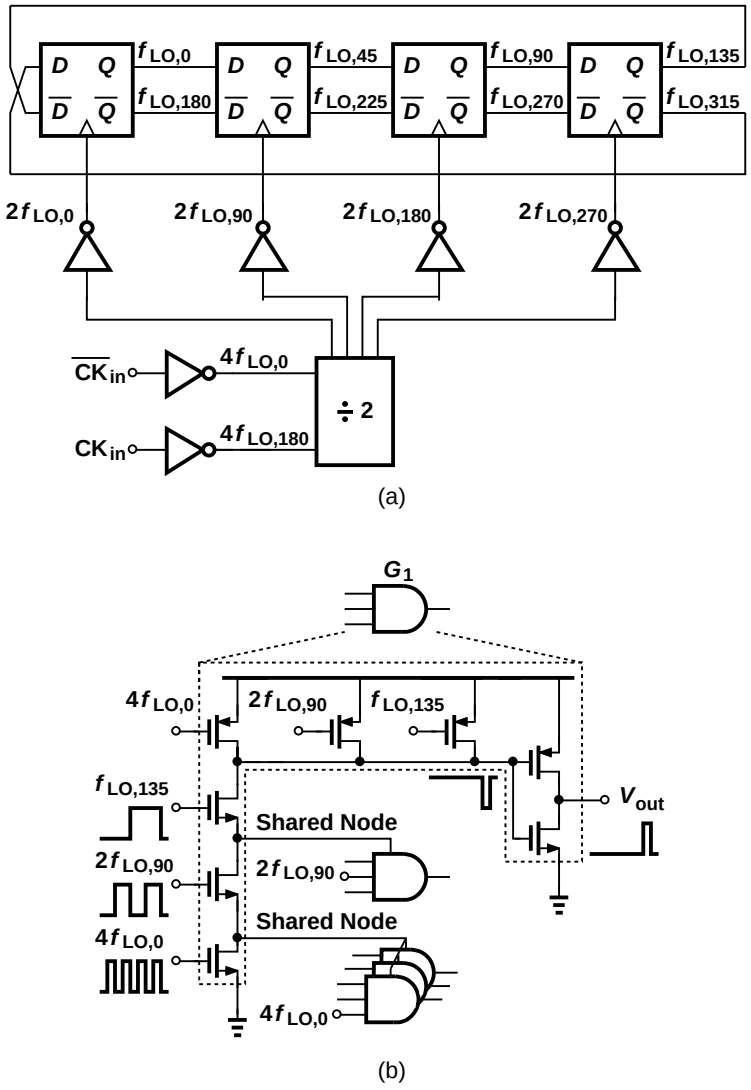


Figure 3.22: (a) $4f_{LO}$, $2f_{LO}$, and f_{LO} generation (b) AND gate design for clock generation with 12.5% duty cycle.

3.3 Experimental Results

The proposed GSM/WCDMA reciever with RF channel selection has been fabricated in TSMC's 65-nm CMOS technology. As shown in Fig. 3.23, the receiver occupies 0.82 mm^2. With a 1.2-V supply voltage, the LNA draws 8.6 mA, the

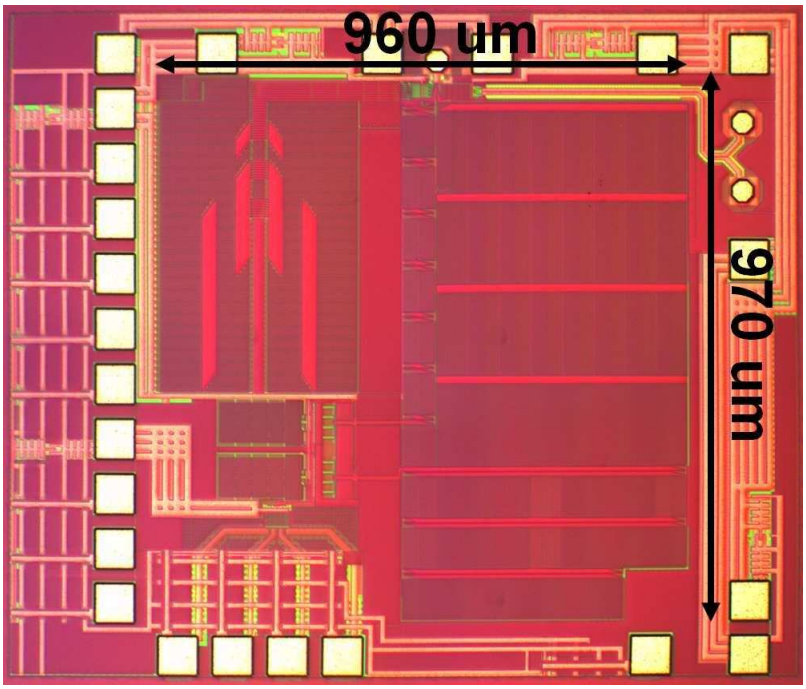


Figure 3.23: Receiver die photograph.

Miller amplifiers 1.5 mA in total, the baseband amplifier in Fig. 3.20 1 mA, and LO generation in Fig 3.22 6 mA. The feedback capacitor, C_F, in bank 1 is designed as a 6-bit programmable array with a total capacitance of 100 pF for each phase. This programmability enables the receiver to change its bandwidth from 400 kHz to 20 MHz. For the polyphase signaling as shown in Fig. 3.17, the capacitor also can be programed to be fed back either to the current phase or to the previous phase. Similarly, the feedback capacitor in bank 2 is designed as a 6-bit programmable raay with a total capacitance of 50 pF for each phase. The Miller capacitor in bank 3 is designed as a 7-bit array with a total capacitance of 70 pF for each phase. It has a higher resolution than C_F for better center-frequency calibration by polyphase signaling.

Figure 3.24 plots the measured RF-to-baseband gain as a function of baseband

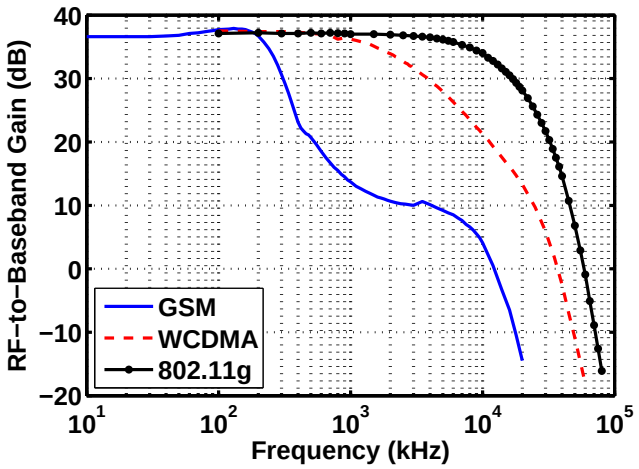


Figure 3.24: Measured RF-to-baseband gain for GSM, WCDMA, and 802.11g.

frequency for various standards. The frequency rsponse of GSM, WCDMA, and 802.11g are measrured at f_{LO}=1 GHz, 2 GHz, and 2.5 GHz, respectively. The 3-dB bandwidth changes from 400 kHz to 20 MHz with different control bits. The rejection at the center of the next adjacent channel reaches up to 15 dB for all three standards. When the receiver is tuned to GSM, the gain drops significantly after 200 kHz baseband frequency and stop decreasing around 2 MHz. Here, the feedback by Miller amplifier causes the first gain drop providing 28-dB out-of band rejection. Atfer staying flat up to around 5 MHz, bank 1 and bank 2 take over and together provide the second gain drop showing over 50-dB out-ob-band rejection at 20 MHz. On the other hand, the gain transition happens only onece for WCDMA and 802.11g because the rejection by bank 1 and bank 2 can reach down to the bandwidth for WCDMA and 802.11g helping smoother rejection.

Figure 3.25 presents the measured receiver NF as a function of baseband frequency for GSM and WCDMA. When the receiver is configured for GSM, it suffers from the flicker noise below 60 kHz. This flicker noise mainly comes from the phase noise of the clock source. When the receiver is tuned for WCDMA,

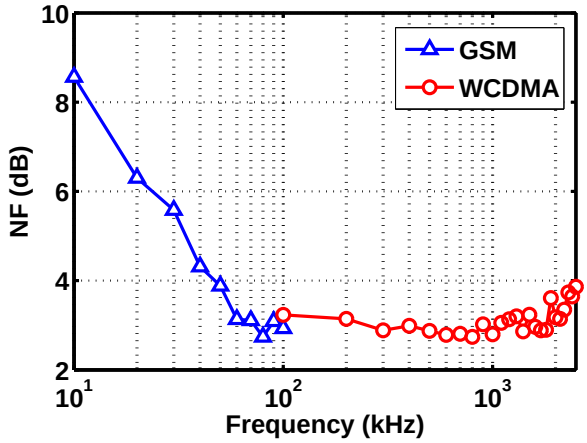


Figure 3.25: Measured NF vs. baseband frequency for GSM and WCDMA.

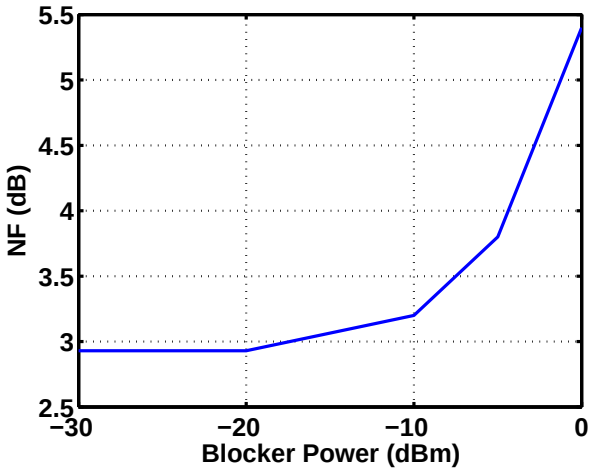


Figure 3.26: Measured NF vs. a 23-MHz offset blocker power.

the NF around 2.5 MHz rises mainly due to the gain loss as shown in Fig. 3.24. This NF rise at the edge of the bandwidth does not occur for GSM since the gain start dropping around 200 kHz.

Figure 3.26 plots the measured noise figure at 100 kHz with a blocker at 23-MHz offset. The X axis represents the blocker power, and the Y axis the measured receiver NF at 100 kHz. The problem in measuring the NF with a

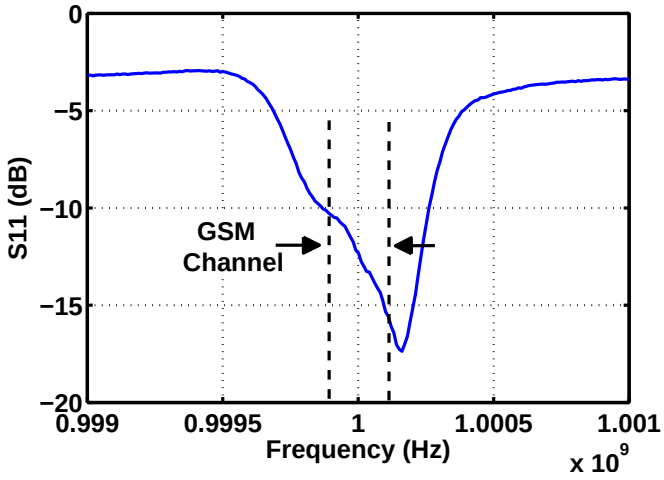
blocker is the noise from a signal generator. Since its noise floor is usually much higher than -174 dBm/Hz, it directly raises the noise floor of the receiver, so as the NF. To filter out this additional noise, a passive microstrip line filter has been built. Around 23 MHz offset frequency, this filter rejects the noise from a signal generator by 17 dB, making the noise as low as around -172 dBm/Hz. Although the worst case blocker frequency must be 20 MHz apart from the signal, we measured the receiver NF with a bloacker at 23 MHz because it is the closest frequency offset without significantly degrading the NF.

Figure 3.27(a) shows the measured S_{11} for GSM and Fig. 3.27(b) for WCDMA. For both cases, S_{11} show below -10 dB for the signal bandwidth indicating a good input impedance matching.

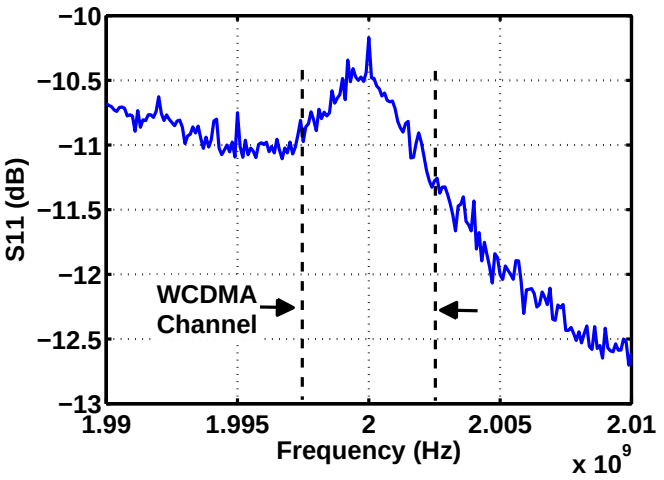
Figure 3.28 plots the measured IIP_3 and IIP_2. For IIP_3 measurement for GSM, two tones are located at $f_{LO} + \Delta f + 100$ kHz and $f_{LO} + 2\Delta f + 100$ kHz, where Δf is a frequency offset in Fig. 3.28. For WCDMA, two tones are placed at $f_{LO} + \Delta f + 1$ MHz and $f_{LO} + 2\Delta f + 1$ MHz. The measured IIP_3 reaches over 10 dBm with $\Delta f = 100$ MHz for both GSM and WCDMA and shows around -20 dBm when two tones are in band.

The location of two tones for IIP_2 measurement is $f_{LO} + \Delta f$ and $f_{LO} + \Delta f +$ 100 kHz for GSM and $f_{LO} + \Delta f$ and $f_{LO} + \Delta f + 1$ MHz for WCDMA. Applying two tones, 100 kHz and 1 MHz signals are measured at the baseband for GSM and WCDMA, respectively. As depicted in Fig. 3.28, both IIP_2s are higher than 54 dBm when $\Delta f >$150 MHz without any calibration.

Table 1 summarizes this work and compares it to previously published state-of-the-art. Comparing to other works using an N-path filter, the proposed receiver provides a unique function, a variable receiver 3-dB bandwidth from 400 kHz to 20 MHz at RF frequency. Since a high-order BPF is created at the input of the



(a)



(b)

Figure 3.27: (a) Measured S_{11} for GSM (b) measurened S_{11} for WCDMA.

receiver, it filters out a 0-dBm blocker not to degrade NF significantly. The most significant benefit the proposed work provides over other receivers is its low power consumption. This low power has been achieved mainly due to smaller switch size in the 8-path notch filters, and consequently smaller power consumption for LO distribution network.

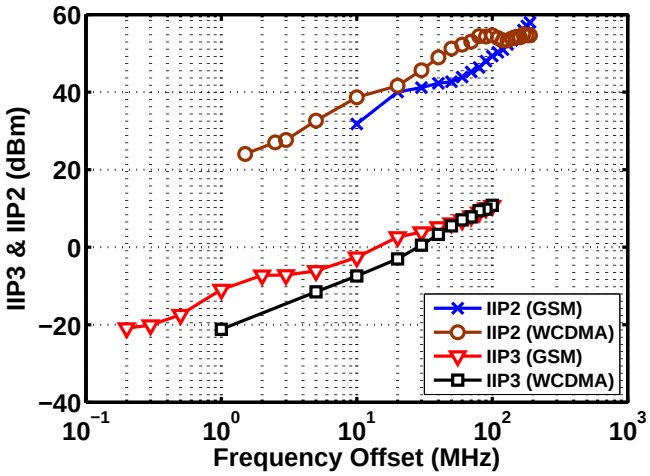


Figure 3.28: Measured IIP_3 & IIP_2 for GSM and WCDMA.

Table 3.1: Receiver performance summary and comparison

	[15]	[16]	[26]	This work
Input Frequency [MHz]	80 ~ 2700	1000 ~ 2500	1800 ~ 2400	50 ~ 2500
Channel Bandwidth [MHz]	N/A	5	N/A	0.4 ~ 20
Gain [dB]	72	30	45.5	38
NF [dB]	1.9	7.6	3.8	2.9
NF with 0−dBm Blocker [dB] (at Given Offset)	4.1 (80 MHz)	N/A	7.9 (20 MHz)	5.4 (23 MHz)
Out−of−Band−IIP3 [dBm]	13.5	12	18	10
Active Area [mm^2]	1.2	< 0.06	0.84	0.82
Supply Voltage [V]	1.3	1.2	1.2/1.8	1.2
Power Consumption [mW]	65 (2 GHz)	62[1]	35[2] (2 GHz)	20 (2 GHz)
CMOS Technology	40 nm	65 nm	40 nm	65 nm

[1]Excluding clock circuitry [2]With a 1.8 V supply for LO divider

3.4 Conclusion

The channel selection at RF frequency greatly relaxes the requirements of other suceeding blocks, such as mixers and baseband amplifiers. This paper presents the 8-path notch filters in feedback paths around the LNA utilizing Miller effect to reduce the switch sizes and the required load capacitors significantly, so as the power consumption and the die area. The 8-path notch filter in the unilateral Miller path further enhances Miller effect. Also, the frequency shaping method for Miller amplifier creates the high-order BPF at the receiver input. In conclusion, using the introduced methods, the receiver with a sharp RF channel selection of 400 kHz is achieved with low power consumption of 20 mW.

CHAPTER 4

Conclusion

This dissertation presents new design techniques for RF receivers, namely, harmonic-rejecting LNA and GSM/WCDMA receiver with sharp channel selection at RF.

Employing a notch filter and active high-order low-pass filter, the proposed harmonic-rejecting LNA rejects blockers at the third and higher order harmonics of LO frequency by over 20 dB without significant noise penalty. The resulting filter is programmable from 300 MHz to 10 GHz. A part of LO signal injected to the LNA, a direct-conversion receiver with LMS algorithm tunes the filter to the optimal frequency.

A GSM/WCDMA receiver with RF channel selection introduces methods such as N-path notch filter, unilateral N-path notch filter, "super Miller" notch filter, polyphase notch filter, and low-power multi-phase LO generation to achieve sharp channel selection at RF. This reciever provides channel bandwidth of 400-kHz to 20 MHz with over 15-dB rejection at the next adjacent channel, drawing only 20 mW at 2GHz. It is also shown that this receiver sustains 0-dBm blocker at 23-MHz offset.

References

[1] Z. Ru *et al.*, "A Software-Defined Radio Receiver Architecture Robust to Out-of-Band Interference," *ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 230-231.

[2] N. A. Moseley *et al.*, "A 400-to-900 MHz Receiver with Dual-domain Harmonic Rejection Exploiting Adaptive Interference Cancellation," *ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 232-233.

[3] A. A. Rafi *et al.*, "A Harmonic Rejection Mixer Robust to RF Device Mismatches," *ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 66-67.

[4] B. Razavi, "Cognitive Radio Design Challenges and Techniques," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1542-1553, Aug. 2010.

[5] J.A. Weldon *et al.*, "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter With Harmonic-Rejection Mixers," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2003-2015, Dec. 2001.

[6] C. Andrews and A.C. Molnar, "A Passive Mixer-First Receiver With Digitally Controlled and Widely Tunable RF Interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696-2708, Dec. 2010.

[7] A. Mirzaei *et al.*, "A Low-Power Process-Scalable Superheterodyne Receiver with Integrated High-Q Filters," *ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 60-61.

[8] D. Murphy *et al.*, "A Blocker-Tolerant Wideband Noise-Cancelling Receiver with a 2dB Noise Figure," *ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 74-75.

[9] A. Ghaffari *et al.*, "Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998-1010, May 2011.

[10] A. Mirzaei and H. Darabi, "Analysis of Imperfections on Performance of 4-Phase Passive-Mixer-Based High-Q Bandpass Filters in SAW-Less Receivers," *IEEE Trans. Circuits and Systems - Part I*, vol. 58, pp. 879-892, May 2011.

[11] H. Darabi, "A Blocker Filtering Techniques for SAW-Less Wireless Receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2766-2773, Dec. 2007.

[12] S. Ayazian, R. Gharpurey, "Feedforward Interference Cancellation in Radio Receiver Front-Ends," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 54, no. 10, pp. 902-906, Oct. 2007.

[13] D. Im *et al.*, "A Broadband CMOS RF Front-End for Universal Tuners Supporting Multi-Standard Terrestrial and Cable Broadcasts," *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 392-406, Feb. 2012.

[14] S.C. Blaakmeer *et al.*, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341-1350, Jun. 2008.

[15] A. Mirzaei *et al.*, "A frequency translation technique for SAW-Less 3G receivers," *Symposium on VLSI Circuits Dig. Tech. Papers*, June 2009, pp. 280-281.

[16] S. Youssef *et al.*, "Active Feedback Technique for RF Channel Selection in Front-End Receivers," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3130-3144, Dec. 2012.

[17] J. Borremans *et al.*, "A 40nm CMOS Highly Linear 0.4-to-6GHz Receiver Resilient to 0dBm Out-of-Band Blockers," *ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 62-63.

[18] A. Mirzaei *et al.*, "A 65 nm CMOS Quad-Band SAW-Less Receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 950-964, Apr. 2011.

[19] M. Darvishi *et al.*, "A 0.1-to-1.2GHz Tunable 6th-Order N-Path Channel-Select Filter with 0.6dB Passband Ripple and +7dBm Blocker Tolerance," *ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 172-173.

[20] E. Langer, "Impulse-Scanned N-Path Filter for Several Frequency Ranges," U.S. Patent 3 717 816, Feb. 20, 1973.

[21] A. Mirzaei *et al.*, "Architectural Evolution of Integrated M-Phase High-Q Bandpass Filters," *IEEE Trans. Circuits and Systems - Part I*, vol. 59, no. 1, pp. 52-65, Jan. 2012.

[22] M. A. Poole, "High Q Notch Filter," U.S. Patent 3 795 877, Mar. 5, 1974.

[23] A. Ghaffari *et al.*, "Tunable N-Path Notch Filters for Blocker Suppression: Modeling and Verification," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1370-1382, June 2013.

[24] J.W. Park and B. Razavi, "A Harmonic-Rejecting CMOS LNA for Broadband Radios," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1072-1084, Apr. 2013.

[25] H. Darabi and A.A. Abidi, "Noise in RF-CMOS mixers: a simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15-25, Jan. 2000.

[26] I. Fabiano *et al.*, "SAW-Less Analog Front-End Receivers for TDD and FDD," *ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 82-83.