UNIVERSITY OF CALIFORNIA, SAN DIEGO

Ultra-High Speed Data Converter Building Blocks in Si/SiGe HBT Process

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits & Systems)

by

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2005

The dissertation of Jonathan C. Jensen is approved, and it is acceptable in quality and form for publication on microfilm:

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Chair

University of California, San Diego

2005

To my lovely wife Suzanne, who supported me through years of hard work and doubt. Without her, this would not have been possible.

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ACKNOWLEDGEMENTS

The text of Chapter Two, Three, and Four, in part, is a reprint of the material as it appears in Proceedings of 2000 IEEE Custom Integrated Circuits Conference (CICC), IEEE 2002 Proceedings of the Bipolar Circuits and Technology Meeting, 2004 IEEE Custom Integrated Circuits Conference (CICC) and IEEE Journal of Solid-State Circuits. The dissertation author was the primary researcher and the first author listed in these publications. He directed and supervised the research which forms the basis for these chapters.

I began this journey in 1996 with no experience in electrical engineering. As a physics major who did not know for sure how a transistor worked, I began in earnest to complete my courses and start my research. It was a trial by fire and I certainly got a little burned along the way. I was fortunate enough to work under the direction of Professor Larson and want to thank him for giving me the opportunity to pursue state-of-the-art research. His skillful instruction and encouraging personality was instrumental during my research.

I would also like to thank professor Galton for his help and support. I had the unique opportunity to work in a shared lab with students of both Professor Larson and Professor Galton where I received countless hours of instruction and wisdom. Professor Galton's example was there for all his students and I was fortunate enough to gather some of the spill-off.

Working for many years as I did in a lab with students from both Professor Larson and Professor Galton gave me the opportunity to interact with many fine students. I actively and passively learned a lot of useful information and habits that I cannot attribute to any

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The text of Chapter Three is a reprint of the material as it appears in the 2004 IEEE Custom Integrated Circuits Conference. The original material was entitled *An 8bit 3GHz Si/SiGe HBT Sample-and-Hold*.

The text of Chapter Four is a reprint of the material as it appears in IEEE 2002 Proceedings of the Bipolar Circuits and Technology Meeting and the 2003 IEEE Journal of Solid-State Circuits. The original material was entitled *A 16GHz Ultra-High Speed HBT Si/SiGe Comparator* in both publications.

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PUBLICATIONS

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Liwei Sheng, Jonathan C. Jensen, Lawrence E. Larson, "A Wide-Bandwidth Si/SiGe HBT Direct Conversion Sub-Harmonic Mixer/Downconverter," *IEEE Journal of Solid State Circuits*,pp. 1329-1337, Sept. 2000.

Jonathan C. Jensen, Lawrence E. Larson, "A Broadband 10GHz Track-and-Hold in Si/SiGe HBT Technology," *IEEE Proceedings of the 2000 Custom Integrated Circuits Conference*,pp. 345-349, 2000.

Jonathan C. Jensen, Lawrence E. Larson, "A Broadband 10GHz Track-and-Hold in Si/SiGe HBT Technology," *IEEE Journal of Solid State Circuits*, vol. 36, no. 3, pp. 325-330, March 2001.

Jonathan C. Jensen, Lawrence E. Larson, "A 16GHz Ultra-High Speed Si/SiGe HBT Comparator," *IEEE Proceedings of the 2002 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 120-123, Oct. 2002.

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FIELDS OF STUDY

Major Field: Electrical and Computer Engineering
Studies in Radio Frequency Integrated Circuit Design.
High Frequency Data Converters
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ABSTRACT OF THE DISSERTATION

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by

Jonathan C. Jensen

Doctor of Philosophy in Electrical Engineering (Electronic Circuits & Systems)

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Professor Lawrence E. Larson, Chair

High performance multi-stage data converters and sub-sampling frequency down-converters typically require track and hold amplifiers (THA) with high sampling rates and high linearity. Following these broadband circuits, the data converter must also be able to operate at ultra-high frequencies. In this dissertation I present two THA designs and one ultra high-frequency comparator. Each achieved state-of-the-art performance implemented in a $0.5\mu m$ 45GHz BiCMOS Si/SiGe process.

The first track-and-hold amplifier was designed for sub-sampling communications applications based on a diode-bridge switching core with high-speed Schottky diodes. The THA has an input bandwidth in excess of 10GHz, consumes approximately 550mW and can accommodate input voltages up to 600mV. With an input frequency of 8.05GHz and a sampling frequency of 4GHz, the THA has an IIP3 of 26dBm and an SFDR of 30dB. The comparator consumes approximately 80mW with sampling speeds up to 16GHz.

The second was BiCMOS switched-emitter follower based THA designed to consume less current and area than the diode-bridge THA and be available in non-Schottky processes. It has an active area of $0.150mm^2$ while consuming 360mW in the THA core. In full sampling mode, the dynamic range was greater than 43.5dB for up to 4GHz clock speed.

For the comparator, an improved design approach to the traditional bipolar master-slave architecture was implemented to reduce the latch time and thus increase the overall clock speed. The result is a design with a clock speed in excess of 16GHz.

Chapter I

Introduction

The market demand for high performance wired and wireless circuits over the last two decades has been staggering. Both home entertainment and business applications demand high performance silicon integrated circuits. Practically every facet of society has incorporated some sort of wireless technology into its daily life. From satellite television, mobile phones, and Blackberries, to Wireless LAN, WiMax, and Ultra-Wideband communications infrastructures, the push for high-speed, high data rate systems has increased dramatically. Video, voice, and high volume data storage push the limits of the technology and high-speed circuit blocks are an integral piece in a myriad of system architectures [1–4].

Next-generation Internet-oriented mobile satellite systems will require low-cost, high-bandwidth receivers operating in the 12-40GHz range (See Fig. I.1 [5–9]. Often, for direct-to-digital satellite communications systems, the intermediate frequency (IF) of the receiver chain is in the neighborhood of 4-8GHz, and so a second down-conversion

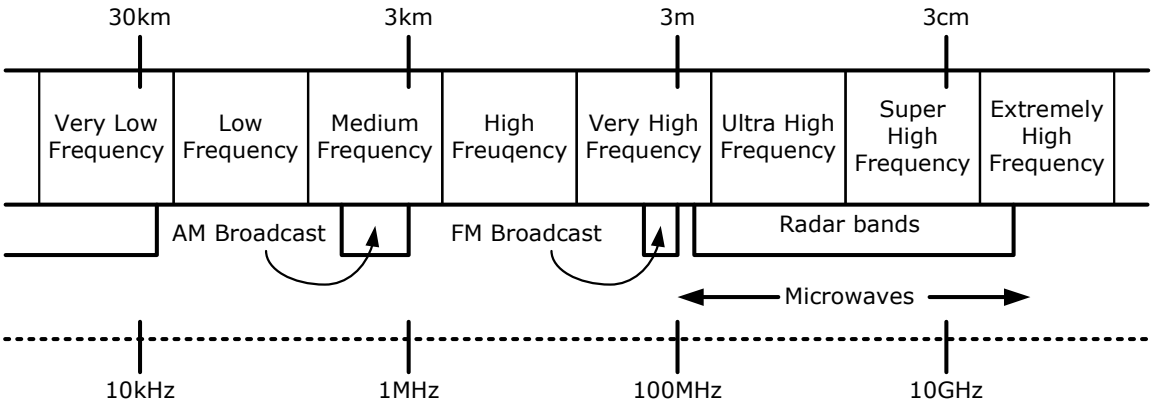

Figure I.1: Spectrum allocation.

step is usually required. Two common approaches to dealing with these Super-High and Extremely-High frequency signals are sub-sampling and Nyquist rate sampling. Each of these require ultra-wide input bandwidths and multi-gigahertz clock frequencies.

In the sub-sampling regime, see Fig. I.2 a), the center frequency of the receive signal is higher than the clocking speed of the analog-to-digital converter [1, 2, 10]. The high input frequency is the critical design focus in these low (1-4 bit) and medium (4-8 bit) resolution architectures and thus circuit architectures and technologies are chosen appropriately.

In the over-sampling architecture, see Fig. I.2 b), the input bandwidth is lower than the clocking speed of the data converter. For this configuration, noise, resolution and clock speed are the important factors in design [11, 12]. Depending on the input signal resolution and bandwidth, a mixer stage may or may not be present and the signal can be converted direct to digital.

Different architectures exist for the analog-to-digital converter (ADC) and these

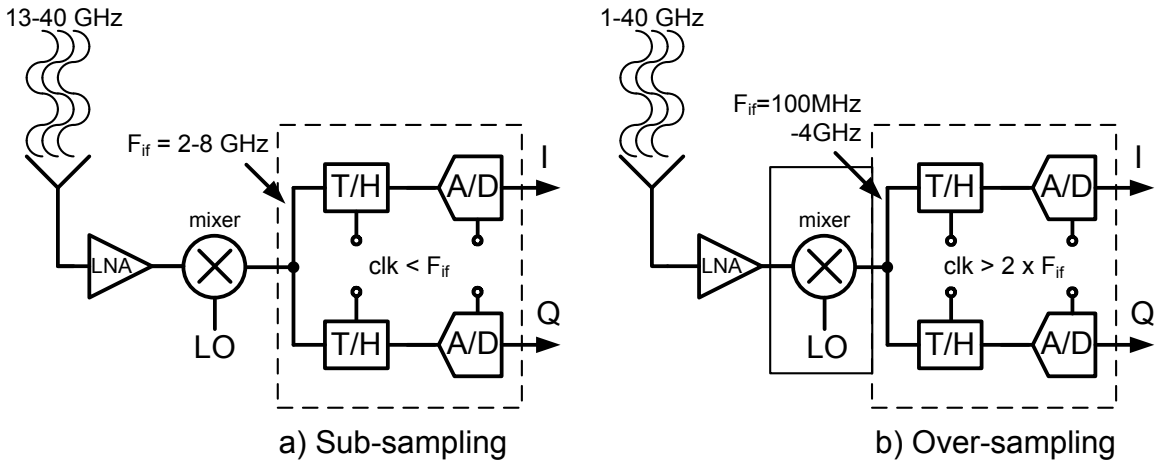

Figure I.2: a) Sub-sampling architecture b) Over-sample architecture.

differences impact the constraints we place on the building blocks. Pipeline, flash, and folding and interpolating, are the most common types of high-speed ADCs. The pipeline architecture shown in Fig. I.3 [13] usually consists of a series of low resolution converters with each stage operating at the clock frequency of the overall converter. The first stage quantizes the input signal to the particular resolution of that stage. The result from the first stage converter is then passed to a digital-to-analog converter (DAC) where the analog output of the DAC is then subtracted from the original signal. The error, or residue, is amplified and then passed to the next ADC stage, where the same process is executed. This is done until the resolution of the overall converter is reached. The measurement code from the ADC typically passes to a digital error correction block that relaxes the requirements on the comparators and helps remove errors from glitches and missed codes [14].

The pipeline converter is an excellent method of quantizing a signal, but timing constraints become extremely difficult in the gigahertz range. Some timing constraints

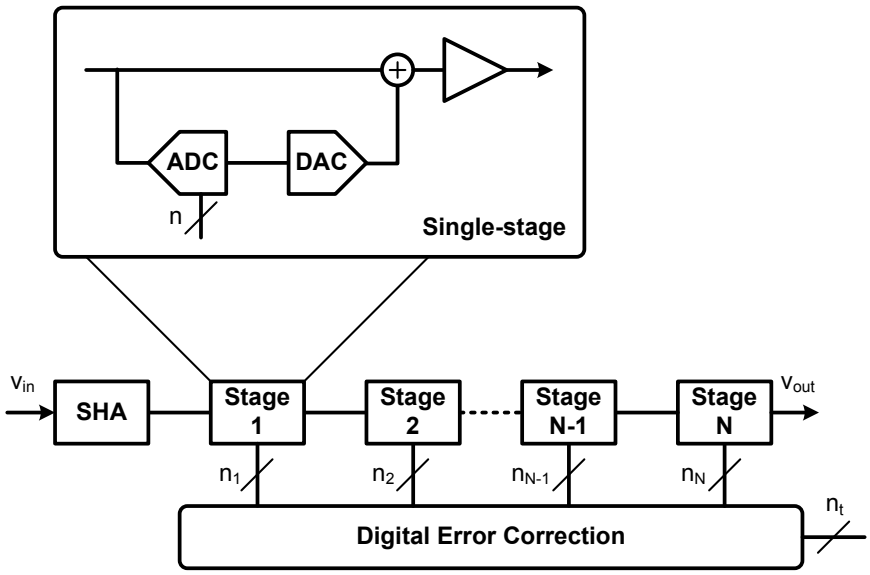

Figure I.3: Generic multi-bit pipeline analog-to-digital converter.

can be alleviated by including a sample-and-hold in the signal path, reducing distortion due to clock skew. However, the delay through the ADC-DAC loop places a limit on the maximum clock speed of the converter since the subtraction before the amplification stage must occur before the sample-and-hold clock changes. Open-loop schemes that do not employ feed-forward or feedback schemes are more successful for broadband, high frequency data conversion.

Folding and Interpolating and *Flash* architectures are similar in nature, see Fig. I.4. In an effort to reduce the current consumption of the ADC, interpolation can be used. Typically, each comparator will require its own pre-amplifier to buffer the reference level to the comparator. Instead, levels can be generated by interpolating between "known" levels before being processed by the comparators (see Fig. I.5) [15].

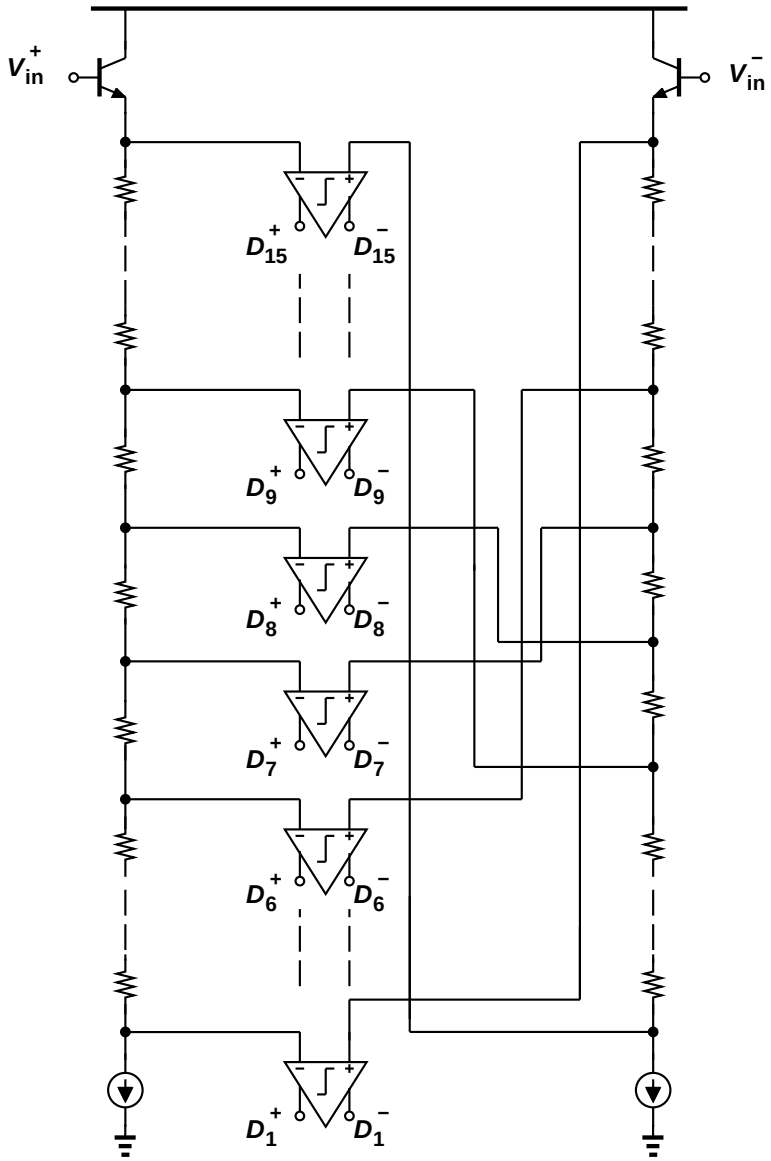

Figure I.4: Generic differential 4-bit flash analog-to-digital converter.

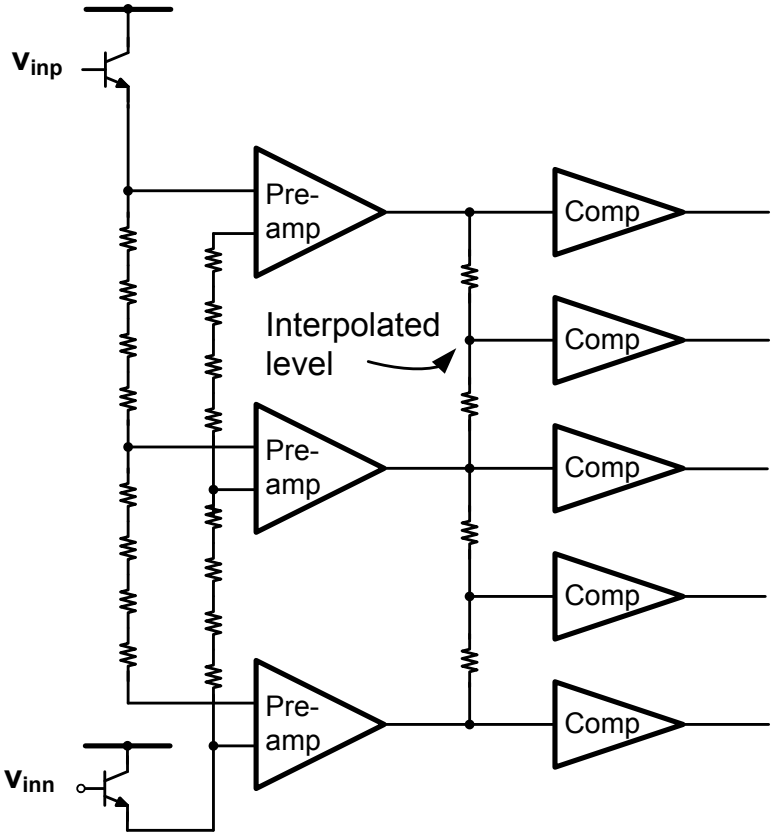

Figure I.5: Interpolating architecture.

This reduces power consumption by reducing the number of comparators. The folding process consists of an amplifier that "folds over" the input signal at quantized levels as seen in Fig. I.6 [16]. As the input voltage increases surpassing the reference levels, an opposing current is added to the output reversing the direction of the resultant signal. Thus, the signal at the output of the folding amplifier is now at n times the input frequency, where n is the number of times the signal has been "folded". Thus, the folding amplifier exchanges bandwidth for resolution, but due to the finite bandwidth of the folding amplifier, the peak of the input curve will be slightly "softened" as shown in Fig. I.6 (b). In general, when the bandwidth of the converter circuits is much greater than the bandwidth of the input signal, a folding amplifier can be a good choice.

For reasons mentioned above, the building blocks for each of the above architectures are somewhat different. Where high resolution pipeline converters need low noise and high resolution building blocks, low resolution broadband architectures require faster switching and higher input bandwidths. Three state-of-the-art converter blocks for high bandwidth sub-sampling and over-sampling architectures are designed and analyzed in this dissertation. An ultra-high-frequency track-and-hold is demonstrated for a sub-sampling system, and a sample-and-hold and a comparator are demonstrated for the over-sampling systems.

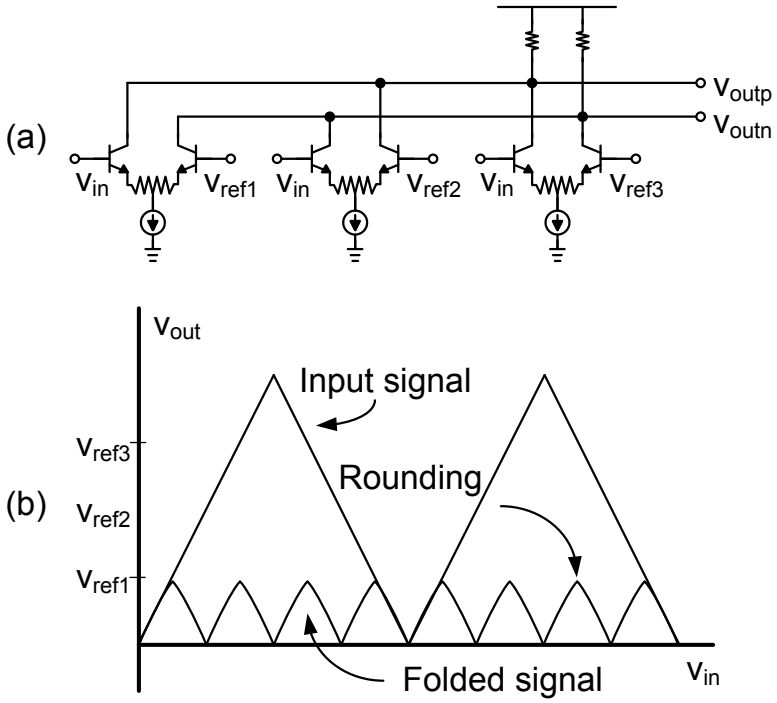

Figure I.6: Bipolar folding amplifier. a) Folding amplifier b) input and output signal waveforms of folding amplifier.

I.1 The Sample-and-Hold

I.1.1 Sub-sampling Architecture

As shown in Fig. I.2 a), a sub-sampling track-and-hold is often employed in the final stage of down-conversion prior to the analog-to-digital conversion. The sub-sampling stage has the most exacting requirements on linearity and noise, in addition to the extremely wide bandwidth requirements. Most ADC architectures require a track-and-hold (THA) or sample-and-hold amplifier (SHA) that holds the incoming signal constant for most of a clock cycle in order to reduce clock skew problems.

The THA of Fig. I.7 tracks the input signal for half a clock period and then holds the result for the remainder. The maximum speed of the THA is determined by the maximum allowable frequency of the input signal (the bandwidth), the maximum clock rate, and how quickly the THA is able to resume accurately tracking the input signal after the hold phase. Linearity and noise considerations must also be accounted for.

If a second track-and-hold amplifier, clocked on the opposite phase from the first THA, is placed at the output of the THA, we have a sample-and-hold amplifier (SHA). The SHA produces a "held" signal during the full clock period, with short transition periods at the rising clock edge. The bandwidth of the second stage must be large enough to limit the transition period between hold and track phases to a relatively small duration compared to the overall clock period.

The SHA must possess linearity and bandwidth superior to that of the overall

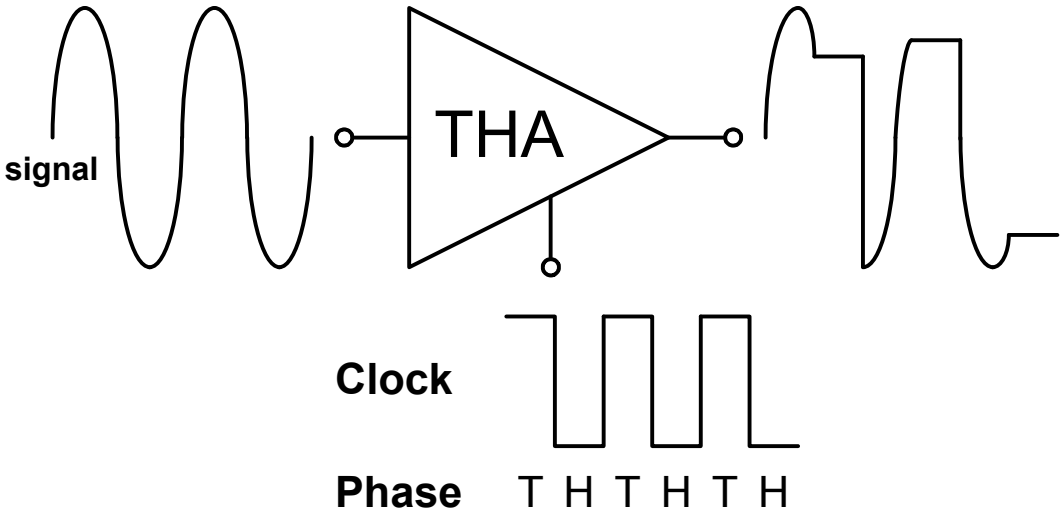

Figure I.7: Generalized operation of an ideal track-and-hold amplifier.

system, since distortion incurred in the analog portion of an ADC is difficult to remove by subsequent digital correction. Typical requirements for these systems are input bandwidths of 8-10GHz and nearly 8-bits of resolution in a 1GHz signal bandwidth.

Very high-speed track-and-hold amplifiers have been implemented in GaAs technology with results that approach these requirements [10, 17, 18]. Silicon bipolar implementations have also been demonstrated with satisfactory resolution, but with considerably lower bandwidths [19–22]. CMOS track-and-hold architectures have shown continued advances in high resolution data conversion, but the typical frequency of operation is even lower [23, 24].

It is difficult to maintain low distortion in a sampling circuit operating at these bandwidths due to frequency dependent sampling errors, which tend to grow at higher frequencies. The diode-bridge track-and-hold presented in this dissertation presents improved

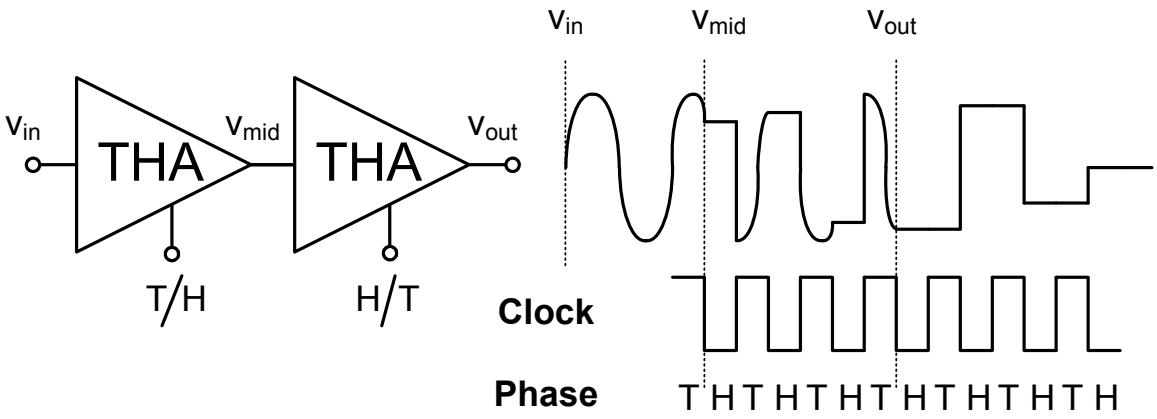

Figure I.8: Generalized operation of a sample-and-hold amplifier.

circuit design techniques to minimize these errors, and demonstrates the performance of a sub-sampling diode-bridge track-and-hold with an input bandwidth greater than 10 GHz and a IIP3 of 26dBm at 8.05GHz implemented in a production Si/SiGe BiCMOS technology. The sampling rate of this circuit at the required dynamic range is superior to other THA's in silicon technology, and is comparable to state-of-the-art GaAs-based circuits (see Fig. I.9) [10, 25].

I.1.2 Over-sampling Architecture

Over-sampling data converters have slightly different requirements on the track-and-hold amplifier. While at first glance it would appear that achieving a high clock speed is more important than a high input bandwidth, the input bandwidth must be adequately large to keep the transition period small compared to the sampling period. The transition period is the time between hold signals, $t_{sample}/2$. For lower circuit bandwidths, a larger portion of

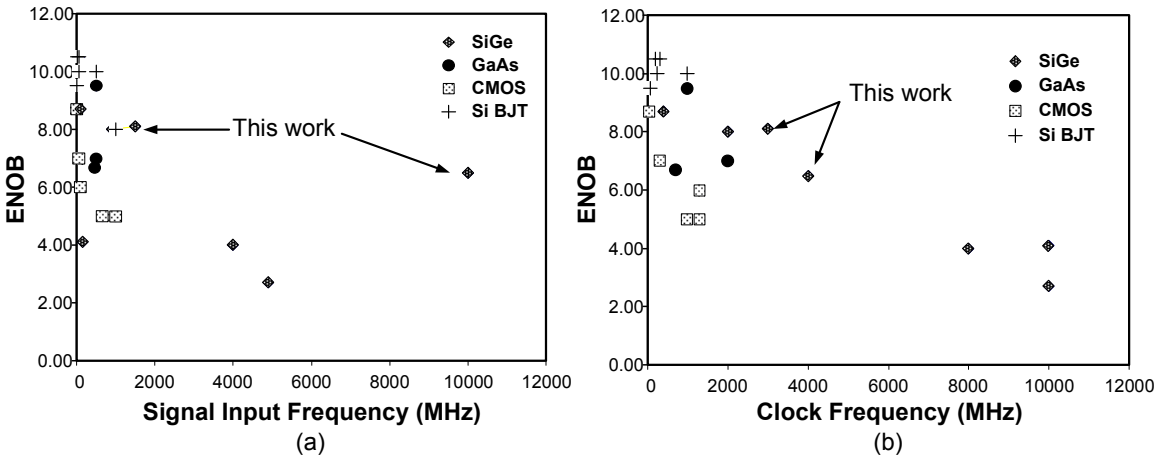

Figure I.9: Previously published SHA results: a) Effective number of bits (ENOB) versus input signal frequency. b) ENOB versus sampling frequency [12, 17, 20–22, 25–38].

the clock cycle is consumed by the transition between track and hold and less time remains for the held signal, reducing the benefit of the THA for the ADC. Over-sampling converters must be able to switch quickly *and* have a high input signal bandwidth.

Our SHA was designed to precede a moderate resolution, but high sample-rate ADC (2-6GHz and 5-6 bit). The analog-to-digital-converter (ADC) operates at a high sampling rate while still maintaining a large signal-to-noise-and-distortion ratio.

For the over-sampling SHA, a switched-emitter-follower sample-and-hold was chosen. It has inferior bandwidth to the diode bridge but has lower current consumption and reduced area compared to the diode-bridge architecture. This paper discusses the architecture along with improved circuit design techniques to minimize the high frequency sampling errors. The bandwidth and dynamic range of this circuit at the required sample rate is superior to other SHA's in silicon technology, see Fig. I.9 b).

I.2 Comparator

The A/D converters implemented in the systems described above typically have modest resolution requirements (less than 8 bit), but require extremely wide bandwidths. The comparator in these A/D converters plays a crucial role in the overall sample rate and resolution of the converter, and must be able to amplify and compare at rates greater than 10GHz. Increasing the sampling speed and bandwidth while minimizing offsets presents many challenges to the designer. For ultra-high speed analog-to-digital converters, the comparator can be the limiting factor in the overall operating speed. A failure will occur if the comparator is unable to provide a digital signal adequately before the next clock phase initiates. The amount of time depends on the systems requirements, but the minimum expectation is to have the output of the comparator to reach a maximum swing by the end of the clock period. This greatly reduces the probability of an indeterminate signal [39].

The design of a comparator that can make a decision, and then resuming tracking of the input signal within a few hundred picoseconds requires careful analysis. This dissertation presents an improved master-slave bipolar Si/SiGe HBT comparator design for ultra high-speed data converter applications. Implemented in a 0.5μm, 55GHz BiCMOS Si/SiGe process, this comparator consumes approximately 80mW with sampling speeds up to 16GHz.

This dissertation presents an improved design approach to the traditional bipolar master-slave comparator [39–44] to increase the overall clock speed of the comparator. The result is a design with a maximum clock rate that is much higher than traditional

approaches.

I.3 Si/SiGe HBT technology

Radio frequency and millimeter-wave circuits require transistor technologies whose f_T exceeds 50GHz. In the quest to accommodate ultra-high frequency signals and switching circuits, a myriad of technological processes are available. Silicon CMOS, silicon-bipolar, gallium-arsenide, indium-phosphide, and silicon-germanium each offer their own advantages and disadvantages. CMOS can be manufactured more inexpensively than the other processes, while InP and GaAs, produced on two inch and six inch wafer diameters respectively, are more expensive to fabricate but faster. For bipolar transistors, and especially the SiGe bipolar transistor, the substantial payoff in bandwidth and power savings make it an ideal candidate for high performance silicon.

In the late 1980s, the strained junction between silicon and silicon germanium was exploited for bipolar transistors yielding very positive results. The Si/SiGe heterojunction bipolar transistor (HBT) provided a device with low base resistance, high current gain, and short base charge transit times compared to a homojunction transistor [45–50]. Initial devices were aimed at high-speed digital and millimeter-wave products, but the process quickly expanded to serve analog and mixed-signal applications [51–61]. By the late 1990s, Si/SiGe HBT circuits were pushing the state-of-the-art for bulk silicon processes [62–65]. Today, products by major companies around the world use the technology to save cost, area, and achieve performance that they are unable to meet with bulk CMOS and bipolar

processes.

I.3.1 Si/SiGe HBT Physics

To design circuits operating in the 10GHz range, a silicon bipolar transistor is desired with reduced base transit time and base resistance. The f_t, or unity gain frequency, is mainly controlled by the base transit time [66], which strongly depends on the base width. Reducing the base width is effective in reducing the transit time, but it increases the base resistance, especially if the current gain is maintained by restricting the base doping concentration. The HBT allows the base doping concentration to be considerably larger than that of the emitter, yielding high current gain, low base resistance and a reduced base transit time.

First, let's look at the operation of a basic silicon bipolar transistor (BJT). The BJT relies on the coupling of two p-n diodes with a shared region called the *base* (see Fig. I.10). When biased properly, most of the current flow is from collector to emitter and very little current flows into the base. The current gain, β, is the ratio of collector current to base current and depends on the relative doping concentrations at the base-emitter junction. Using the terms shown in Fig. I.10, if the base recombination rate, $J_{rec} = 0$,

$$\beta_{bjt} = \frac{J_n}{J_p} = \frac{D_{n,b} N_e l_e}{D_{p,e} N_b w_e} \tag{I.1}$$

where $D_{n,b}$ is the electron diffusion constant in the base, $D_{p,e}$ is the hole diffusion constant in the emitter, N_e is the doping density in the emitter, N_b is the doping density in the

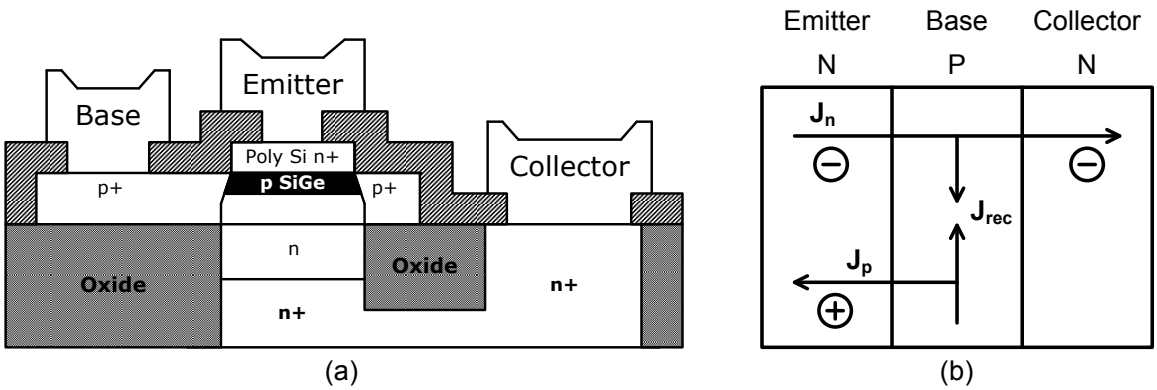

Figure I.10: a) Basic structure of a bipolar transistor. b) Schematic cross section of SiGe HBT.

base, and l_e the emitter diffusion length, w_e is the width of the quasi-neutral region in the emitter [67]. From I.1 we see that higher emitter doping density N_e will increase the current gain, β. We shall see below how the heterojunction device has current gain that is less dependant on the emitter doping density.

A schematic cross section of a Si/SiGe heterojunction bipolar transistor can be seen in Fig. I.10 a), where the SiGe base is shown between the polysilicon emitter and the highly doped collector. Germanium is graded across the base from low density at the emitter-base junction to high density at the collector-base junction [45, 68]. The extent of the grading determines the change in energy band across the base, i.e.

$$\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(x = W_b) - \Delta E_{g,Ge}(x = 0) \tag{I.2}$$

where W_b is the thickness of the base layer, and $x = 0$ is defined as the emitter-base junction [68]. Thus, the grade, $\Delta E_{g,Ge}(grade)$, is defined as the change in energy band

across the base. Due to the difference in energy bands, an electric field exists across the neutral base region that influences the base transit time. As a result

$$\beta_{hbt} = \frac{J_n}{J_p} = \frac{D_{n,b} N_e l_e}{D_{p,e} N_b w_e} e^{\frac{\Delta E_{g,Ge}(grade)}{kT}} \tag{I.3}$$

[68]

Thus, the energy barrier increases the current gain by an exponential factor and allows the base doping to be somewhat independently chosen relative to the band gap. Since the energy band gap between the base and emitter is determined to a larger degree by the germanium concentration in the base, the base can have much higher doping concentration levels to reduce the base resistance, R_b, while still maintaining the significant current gain of the device [50, 66]. The Ge doping of the base is an important "knob" to control the performance of the device.

The stronger electric field across the base due to the Ge decreases the transit time of the minority carriers across the base. If we compare the base transit time, $\tau_{b,SiGe}$, of an HBT device to that of a standard Si BJT, $\tau_{b,Si}$ we see the following relationship [68]:

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\eta} \left(\frac{kT}{\Delta E_{g,Ge}(grade)} \right) \left[1 - \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right] \tag{I.4}$$

where $\eta = D_{nb}(SiGe)/D_{nb}(Si)$, accounts for the differences between the electron and hole mobilities in the base. Equation (I.4) shows the decrease in transit time with the grade of the base doping. The increase in electric field across the base due to the graded doping, increases the electron velocity, reducing the transit time..

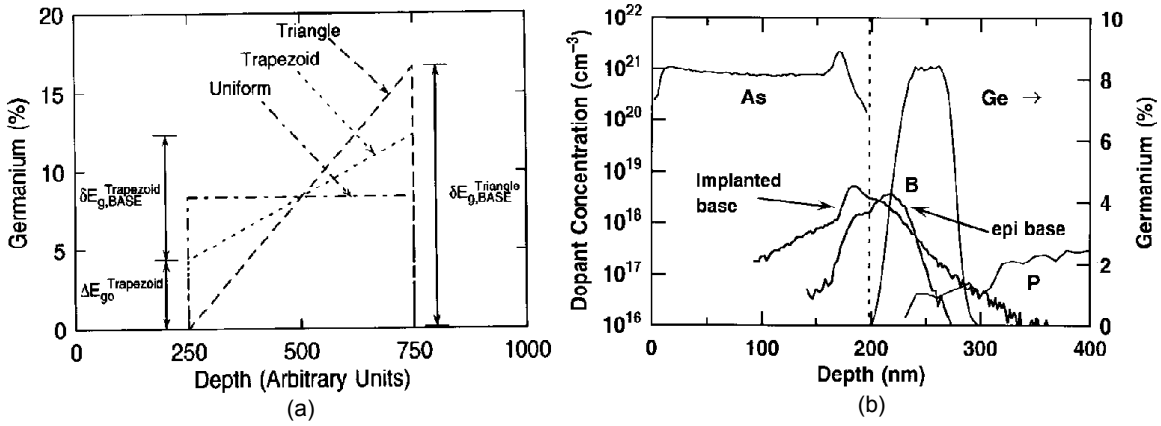

Figure I.11: a) Germanium grading profiles in the base of a SiGe transistor. The total Ge content is kept constant [68]. b) Comparison of the base profiles of a Si BJT and an SiGe HBT [51].

The unity current gain frequency, f_T, of the device is defined as

$$f_T = \left[\frac{1}{g_m}(C_{be} + C_{cb}) + \tau_b + \tau_e + \tau_c\right]^{-1} \tag{I.5}$$

where g_m is the transconductance, τ_b is the base transit time, τ_e is the emitter transit time, τ_c is the collector transit time, C_{be} is the base-emitter capacitance, and C_{cb} is the collector-base capacitance. Thus, from (I.4), the Ge profile can be adjusted to reduce $\tau_{b,SiGe}$, and maximize the f_T.

,

Another important metric of a high-frequency device is the output conductance, g_o, characterized by the Early Voltage, V_A, where $g_o = I_c/V_A$, where I_c is the collector current. Comparing the Early Voltage of a SiGe device, $V_{A,SiGe}$, to that of an identical Si

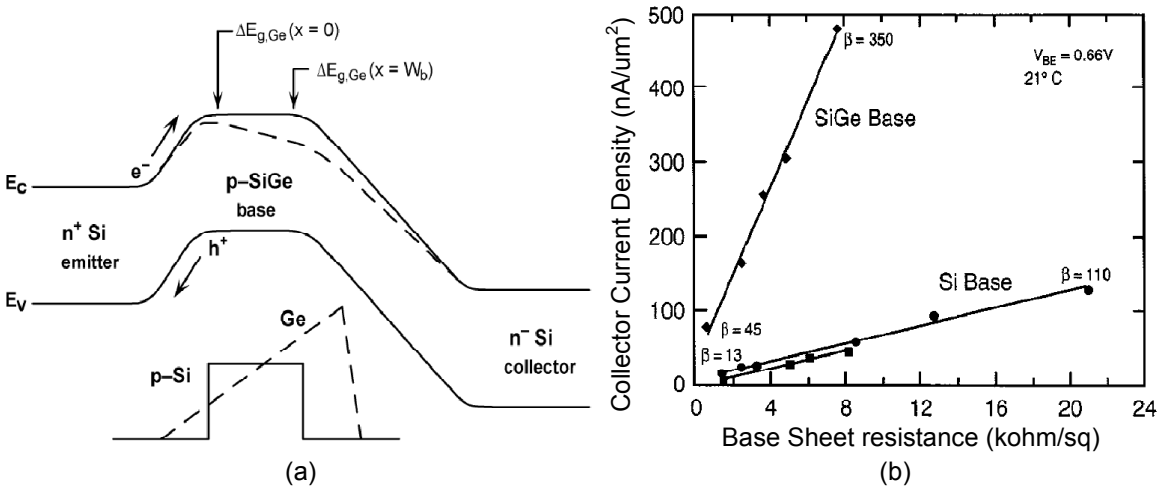

Figure I.12: a) Energy band diagram of a graded-base SiGe HBT compared to a Si BJT [68]. b) Base resistance and β relationship with base doping concentration [69].

device, $V_{A,Si}$, we get [68]:

$$\frac{V_{A,SiGe}}{V_{A,Si}} = \frac{e^{\Delta E_{g,Ge}(grade)}}{kT}\left[\frac{1-e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right] \tag{I.6}$$

From I.6 we see a similar relationship to that for the base transit time, where the bandgap grade determines the improvement in output conductance.

I.3.2 Ultra High-Speed Mixed-Signal Circuits

Front-end receiver blocks were not alone in profiting from the advantages of the silicon germanium transistor. Mixed-signal circuits also found reason to move from more expensive III-V and low performance CMOS processes to SiGe. Whether in Ultra-Wideband, direct-to-digital systems, or over-sampling IF, high-speed switching occurs.

Table I.1: IBM Si/SiGe $0.5\mu m$ Technology [63]

NPN Transistor ($0.5x2.5\mu m$ emitter)	-3σ	*Normal* Nom.	$+3\sigma$
f_T (GHz)	41	47	53
Current Gain (β)	50	100	165
β Match (%)	-10.4	0	10.4
V_{be} (mV @ $10\mu A$)	784	797	810
V_{be} match (mV)	-2.4	0	2.4
V_A (Early V)	30	65	
Resistors		Polysilicon	
R_s	187	220	253
TCR	-75		
Res. matching		.30 % ($W/L = 10/7mum$)	
Capacitors		Metal-ins.-metal	
Area Capacitance ($fF/\mu m^2$)	0.63	0.7	0.77

Even though CMOS was continually improving as a technology with more and more applications were within its reach, the forefront of high-speed, and high-volume development, made a strong shift to silicon germanium.

Early mixed-signal designs with SiGe proceeded where few other technologies succeeded. Initial circuit applications were ultra-high frequency dividers [54] and voltage controlled oscillators [56]. They were soon followed by data converter designs [27, 29, 70, 71]. All of these designs relied on the short transit times to enable switching speeds up to 23GHz.

I.4 Dissertation Objectives and Organization

This dissertation presents the analysis and circuit results for **Ultra-High Speed Data Converter Building Blocks in a Si/SiGe HBT Process**. All circuits were designed, simulated, fabricated, and tested by the author.

Chapter 2 presents the analysis and design of an extremely broad-bandwidth diode-bridge track-and-hold. The work begins with the motivation and requirements for the track-and-hold before moving onto the design of the particular circuit. The chapter concludes with analysis of the fabricated silicon and the experimental results.

Chapter 3 describes another track-and-hold architecture using a switched-emitter-follower design instead of a diode bridge. A different architecture was targeted as well as different specifications. This THA was aimed at an over-sampling analog-to-digital converter consuming less power and area than the diode-bridge design. The chapter concludes with experimental results from silicon testing.

Chapter 4 contains another ultra-high frequency analog-to-digital converter building block, the comparator. This block provides the comparison between the incoming signal and a reference signal. This chapter describes the logical evolution of this block from earlier incarnations and analysis of significant performance metrics. The chapter concludes with experimental results of the fabricated circuit.

Chapter 5 concludes the dissertation. It summarizes the goals and achievements of the circuit designs analyzed in this dissertation and describes future areas of research.

Chapter II

Diode-Bridge Track-and-Hold

II.1 Introduction

Sampling speed and signal bandwidth best describe the challenges for ultra-high speed data converters. With the advantage of a Si/SiGe HBT process and clever circuit approaches, we can help extend the bandwidth of state-of-the-art data converters. For next-generation satellite systems and millimeter-wave communications, the intermediate frequency (IF) of the receiver chain is often in the neighborhood of 8GHz, and so a second down-conversion step is usually required. One possible approach for the implementation of these systems employs a sub-sampling architecture in the final stage of down-conversion prior to the analog-to-digital conversion as shown in Figure II.1. The sub-sampling stage has the most exacting requirements on linearity and noise, in addition to the extremely wide bandwidth requirements.

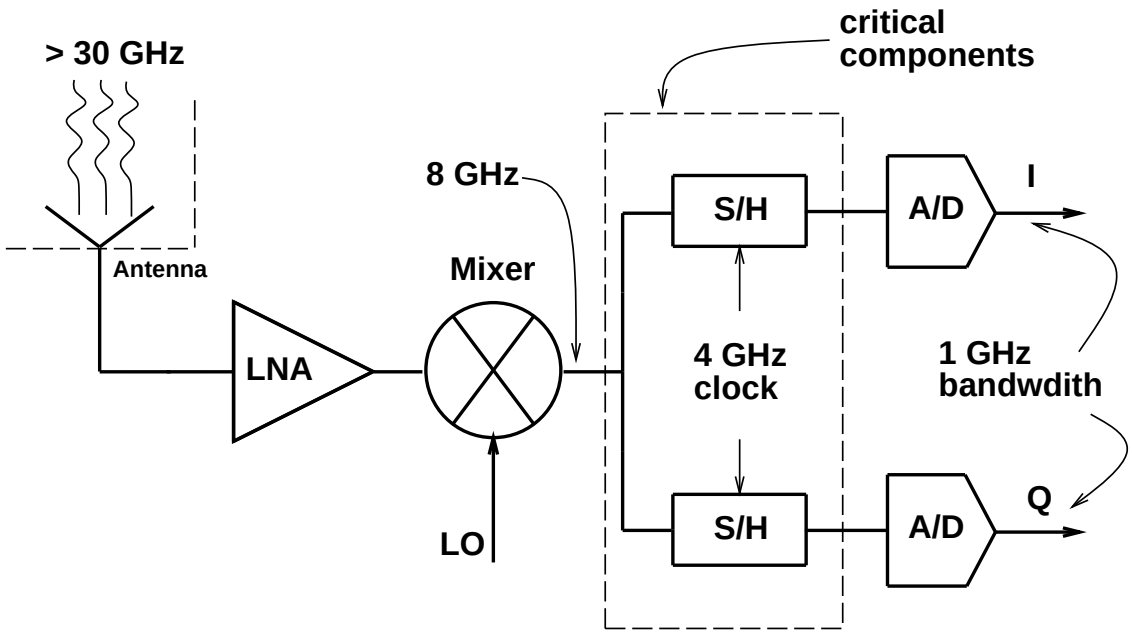

Figure II.1: Sub-sampling architecture.

At the same time, the increasing bandwidths of these systems put a greater demand on the digital conversion of the received signal; the analog-to-digital-converter (ADC) must operate at a higher sampling rate, while still maintaining a large signal-to-noise-and-distortion ratio. Single-stage, multi-bit flash ADCs can be very difficult to implement at high speeds making multi-stage designs more practical [72]. These multi-stage ADCs require a track-and-hold amplifier (THA) with linearity and bandwidth superior to that of the overall system. It is imperative that the track-and-hold be relatively free of distortion since distortion incurred in the analog portion of an ADC is difficult to remove by subsequent digital correction. Typical requirements for these systems are input bandwidths of 8GHz and nearly 8-bits of resolution in a 1GHz signal bandwidth.

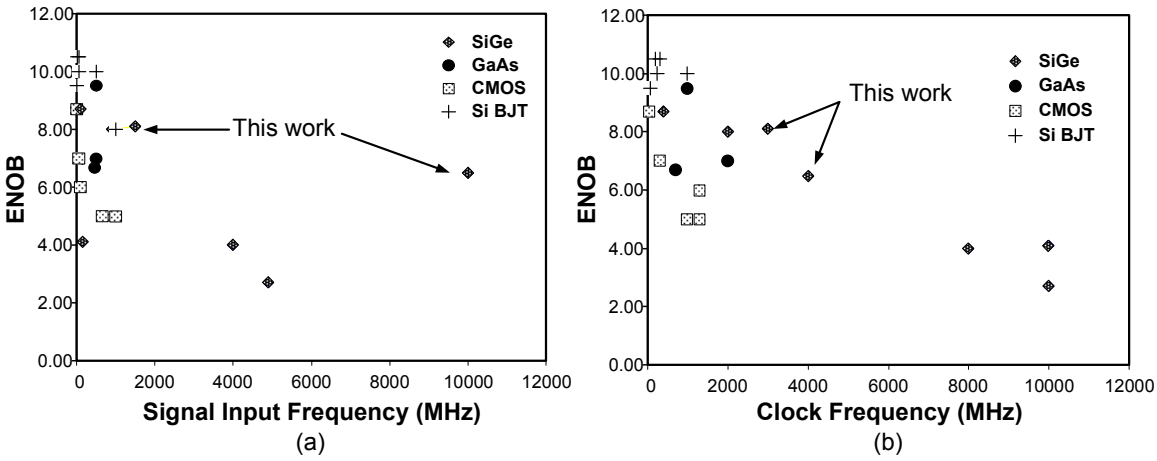

Figure II.2: Previously published SHA results: a) Effective number of bits (ENOB) versus input signal frequency. b) ENOB versus sampling rate. [12, 17, 20–22, 25–38]

Very high speed track-and-hold amplifiers have been implemented in GaAs technology with results that approach these requirements [10, 17, 18]. Silicon bipolar implementations have also been demonstrated with satisfactory resolution, but with considerably lower bandwidths [19–22, 73]. CMOS track-and-hold architectures have shown continued advances in high resolution data conversion, but the typical frequency of operation is even lower [19, 23, 38].

It is difficult to maintain low distortion in a sampling circuit operating at these bandwidths due to frequency dependent sampling errors, which tend to grow at higher frequencies. This chapter presents improved circuit design techniques to minimize these errors, and demonstrates the performance of a sub-sampling diode-bridge track-and-hold with an input bandwidth greater than 10GHz and a IIP3 of 26dBm at 8.05GHz implemented in a production Si/SiGe BiCMOS technology. The sampling rate of this circuit at the

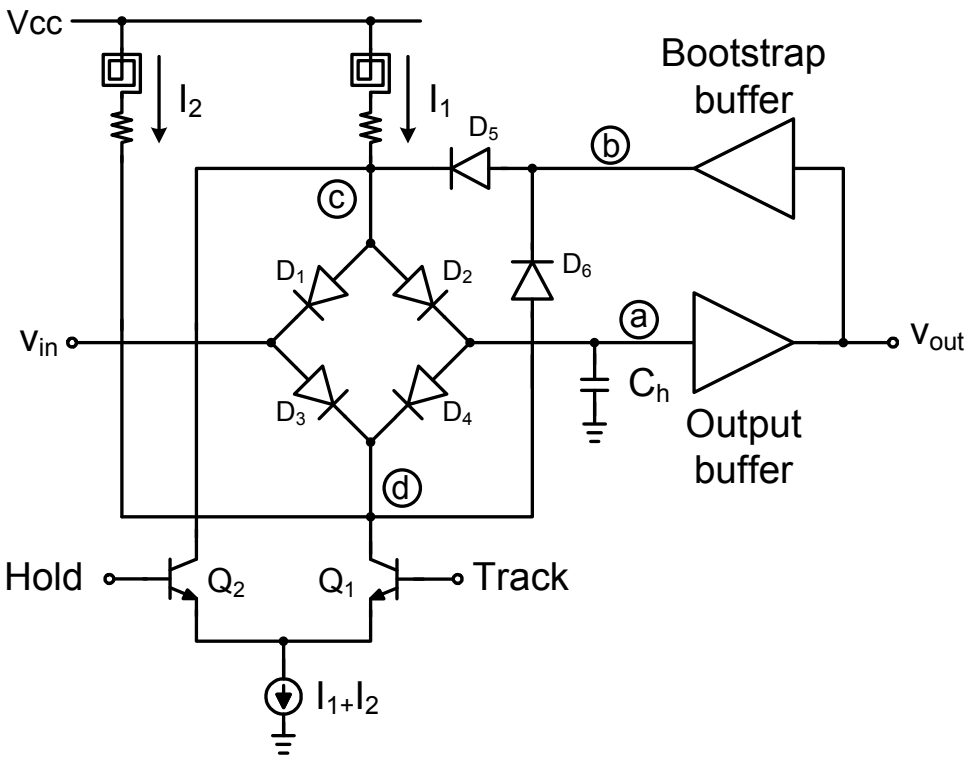

Figure II.3: Diode bridge track-and-hold with unity gain output and boot-strap buffers.

required dynamic range is superior to other THA's in silicon technology, and is comparable to state-of-the-art GaAs-based circuits (see Figure II.2).

II.2 Track-and-Hold Architecture

II.2.1 Diode Bridge Design for Wide-Bandwidth Operation

In typical applications the track-and-hold amplifier samples the input voltage prior to quantization. The track-and-hold linearity and bandwidth directly impacts the performance of subsequent blocks. This design uses a classic high-speed Schottky diode-

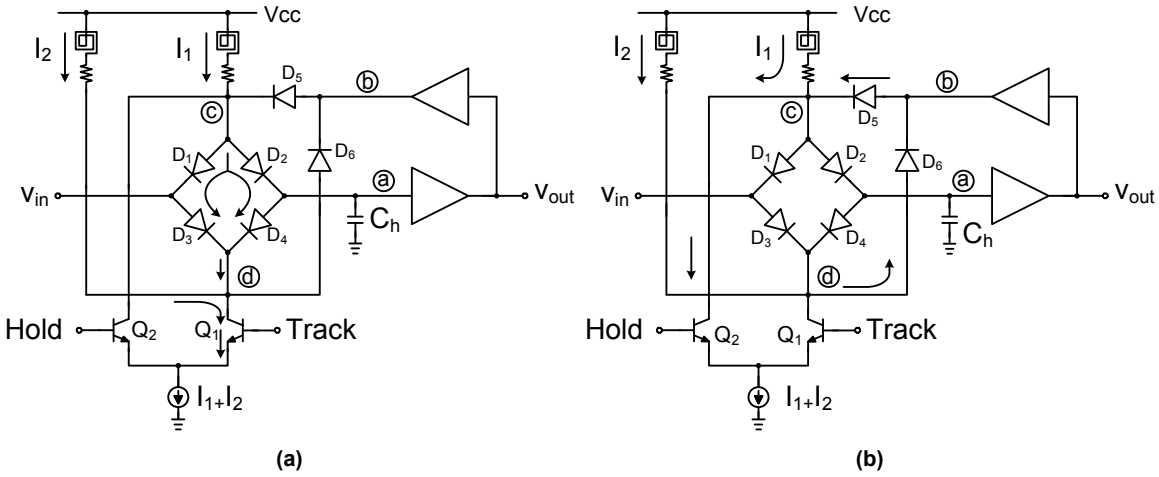

Figure II.4: a) Current flow through the diode bridge track-and-hold during the *track* phase. b) Current flow through the diode bridge track-and-hold during the *hold* phase.

bridge to disconnect the output from the input and a hold capacitor to maintain that voltage (See Figure II.3) [10, 17, 19, 25, 36]. Inductive, passive current sources instead of active sources are used to extend bandwidth.

In the track phase (see Fig. II.4 a)), transistor Q_1 is *on* and current I_1 flows through the diode bridge, D_1, D_2, D_3, and D_4, resulting in the voltage at the hold capacitor equal to the input voltage with a small delay. At this time the voltage at node *c* is higher than that at node *d*. This results in diodes D_5 and D_6 being reverse biased. All of current I_2 flows directly through Q_1 to ground. In the *hold* phase (see Fig. II.4 b)), Q_1 turns *off*, Q_2 turns *on*, and the currents from I_1 and I_2 are directed around the diode bridge, forward biasing the clamp diodes, D_5 and D_6, and reverse biasing the diode bridge. At this time, v_a is disconnected from the input and maintained on the capacitor, C_h. The speed at which this disconnection occurs contributes to the maximum operational speed of the track-and-hold.

The size of the hold capacitor, which determines the droop rate and hold-time, has a rather straightforward relationship to the bandwidth of the circuit. The 3dB bandwidth of the THA in track-mode is $I_1/(2\pi V_T C_a)$, where I_1 is the bias current through the bridge, $V_T = kT/q$, and C_a is the total capacitance at node a. The size of the diode, the output buffer, and C_{hold} are chosen such that C_{hold} makes up the majority of C_a, and thus C_{hold} largely determines the bandwidth of the THA. To maintain a wide bandwidth (greater than 10GHz), a relatively small, 325fF, hold capacitor was used.

From experimental results, the droop rate was determined to be approximately $8mV/ns$ due to the base current of the output buffer drawing charge off the hold capacitor. If the diode-bridge were operated at a lower sampling rate, the output buffer could be turned off during the hold phase, significantly decreasing the droop rate. In a differential THA design, the impact of single-ended droop rate is significantly decreased since the discharge from the capacitor is common mode and does not contribute to sampling error ([36, 74]). The sampled kT/C thermal noise from this capacitor is approximately $113\mu V$, which is 64.5dB below the maximum peak to peak input signal of 600mV and well within the design goal.

II.2.2 Current Source Design for THA Applications

The current sources, I_1 and I_2 in Figure II.3 and II.4, play an important role in the operation of the THA supplying approximately 14mA to the diode bridge. The relatively high shunt impedance of the current source extends the bandwidth of the diode-bridge and

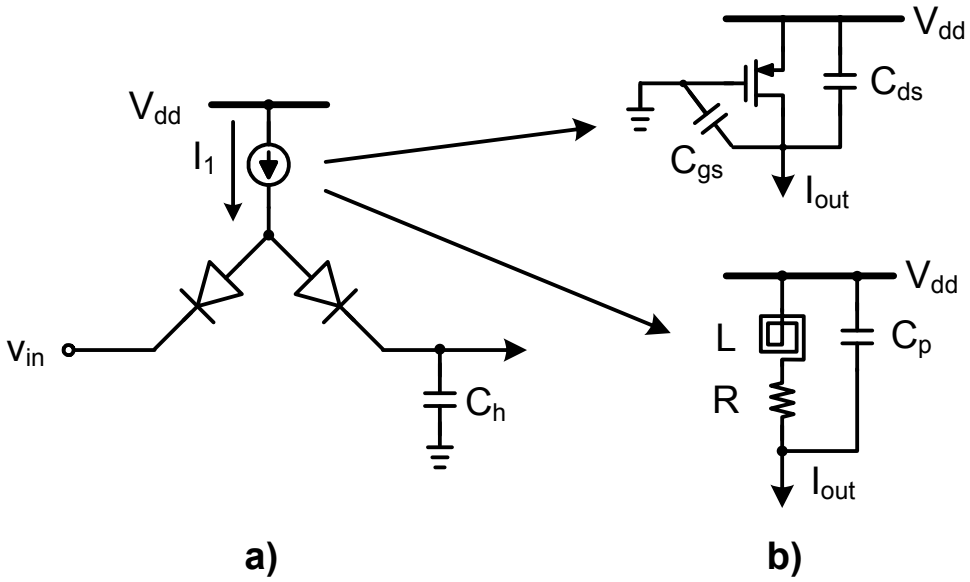

Figure II.5: a) Simplified schematic of diode bridge with current source. b) PMOS and inductively peaked current sources.

reduces some sampling distortion as we will see later in the chapter.

The inherently large drain-gate and drain-bulk capacitance associated with a PMOS current source transistor makes it difficult to maintain the high impedance of the circuit at microwave frequencies (see Fig. II.5). The current source, in shunt to the signal path, acts as a low pass network to the incoming signal (see Fig. II.6). It reduces the input bandwidth and degrades the aperture of the bridge. The aperture is the time required for the diode-bridge to disconnect the output from the input and maintain the signal on the hold capacitor. Preliminary simulations indicate that PMOS current sources would not be effective at input bandwidths much above 1 GHz (see Figure II.7). Fortunately, high-quality-factor inductors are available in a Si/SiGe HBT technology, creating the possibility of employing series

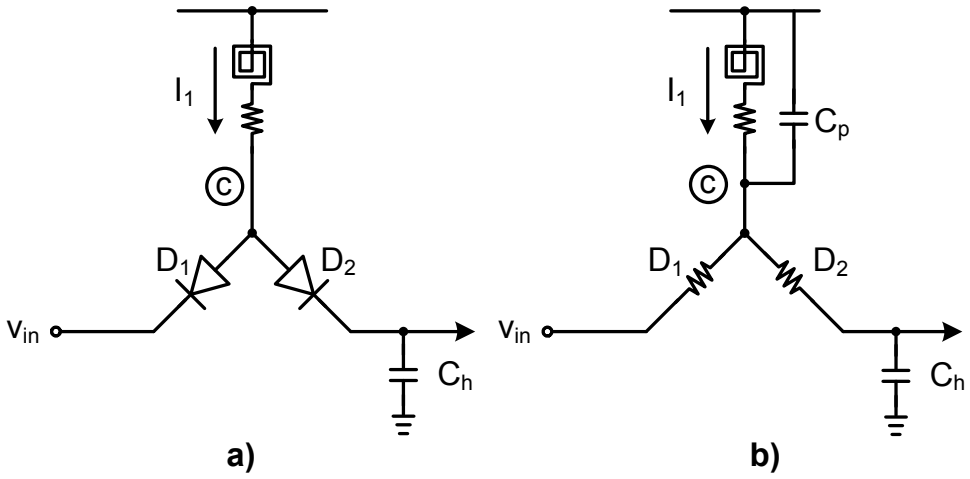

Figure II.6: a) Signal path through diode-bridge. b) RC model of current source with parasitic capacitance.

inductance to raise the impedance of the circuit at high frequencies, improving the overall performance.

For these reasons, a series L-R circuit is employed to increase the impedance at higher frequencies and simulations demonstrate that the input bandwidth, switching-speed and distortion of the diode-bridge were improved through use of this approach. Fig. II.7 shows the improvement of the simulated output impedance of a PMOS current source device compared to the L-R circuit implemented in this technology. The impedance of the PMOS current source decreases substantially after 1 GHz due to the drain capacitance, while the impedance of the inductively peaked current source increases beneficially. Fig. II.8 shows the improvement in bandwidth using the inductively peaked current source over the PMOS current source. In this simple way, the output impedance of the current sources is improved with very little penalty in dc current consumption or noise performance.

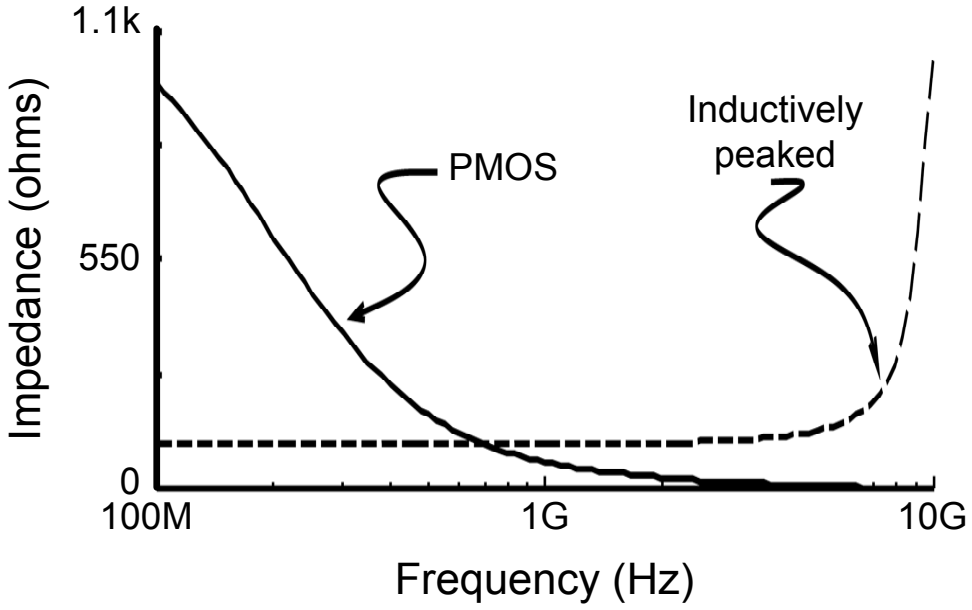

Figure II.7: Simulated output impedance of PMOS and L-R current sources.

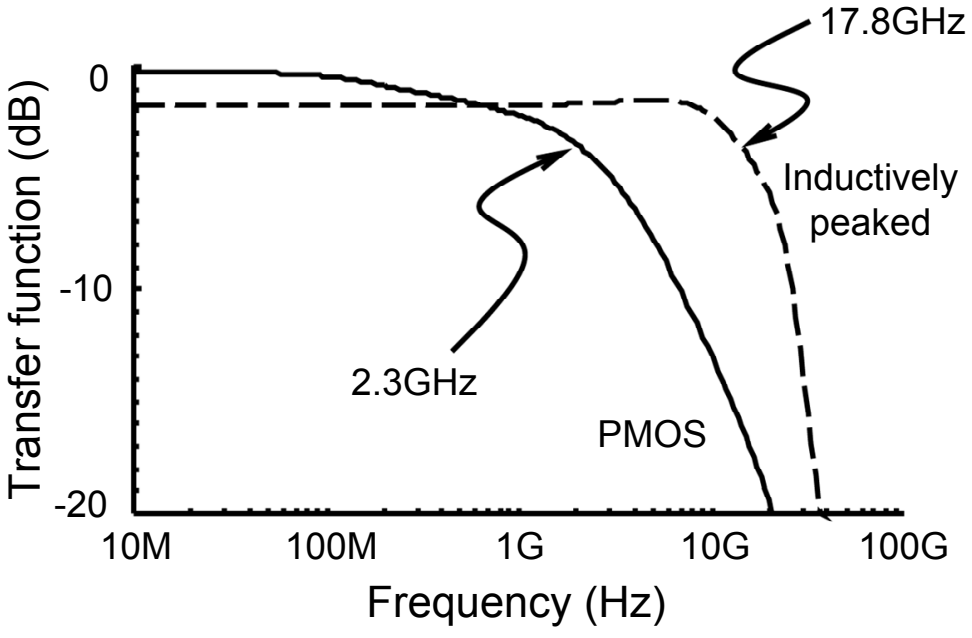

Figure II.8: Simulated bandwidth of diode-bridge.

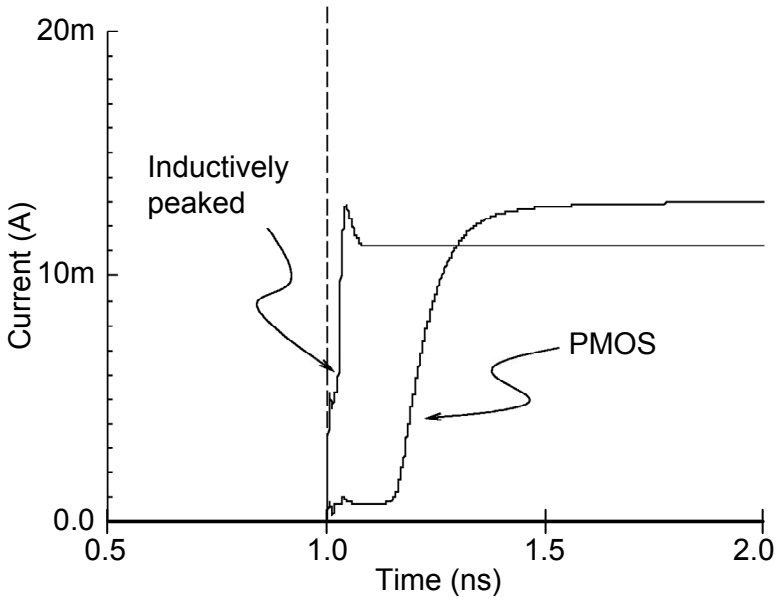

Figure II.9: Simulation of current in diode bridge at initiation of *track* phase with inductively peaked and PMOS current sources.

An unintended impact of the passive current source is that I_1 and I_2 have different values depending on whether the circuit is in the *track* or *hold* phase. The portion of the total current that is I_1 is determined by the dc voltage across the passive R-L source. The voltage at node *c* is higher in the *track* mode than the *hold* phase. Thus, the current through I_1 is less in the *track* phase than during the *hold* phase.

An improved current source will not only improve the input bandwidth, but it will also increase the peak sampling rate. As will be shown in section II.3.3, it is necessary to maintain currents I_1 and I_2 at a roughly constant level when the THA changes from the *track* to the *hold* mode and back again to reduce distortion. During the transition from *track* to *hold* mode, the voltage at node *c* should drop and the voltage at node *d* should increase

very quickly. Any capacitance at the current source will slow this transition and lengthen the aperture of the THA, limiting the sampling speed of the THA (see section II.3.2) [36]. Simulations show that the aperture is substantially decreased from approximately 600 ps with the PMOS current source to less than 100 ps with the inductively peaked current source; the peak sampling bandwidth is improved by roughly a factor of six with this approach (see Figure II.9).

II.3 Track-and-Hold Distortion Analysis

The linearity of track-and-hold circuits often degrades at higher frequencies due to the frequency-dependent errors that tend to accumulate. Signal-dependent delays, modulation of the track-hold aperture, and pedestal distortion are the main concerns. This section will analyze some of these errors, and suggest techniques for their minimization.

II.3.1 Amplitude Dependent Delay Error and Distortion

During the track mode, the current I_1 is evenly distributed through both sides of the diode bridge and the voltage at the output is a delayed version of the input voltage. The delay is partly a result of the linear RC delay through the bridge and partly a result of a complex phase term produced by higher order distortion terms. So the voltage on the hold capacitor will approximate the input voltage, except that there will be a small, signal-dependent delay term due to nonlinear distortion.

This delay error can affect the value of the held signal at the time it is sampled,

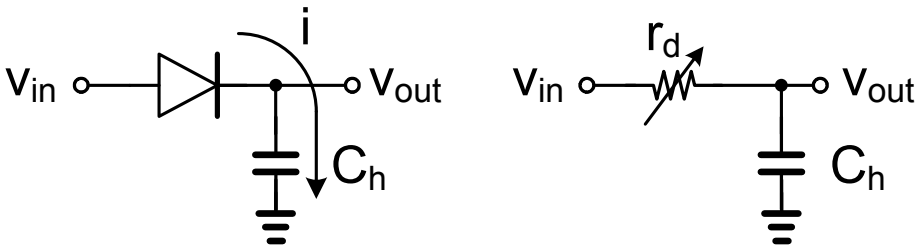

Figure II.10: Amplitude dependent delay error model.

resulting in unacceptable distortion in the sampled signal. The delay through the diode-bridge is different for the small signals than for the large signals. It can be analyzed using the simplified model seen in Figure II.10, with the input of the diode bridge filtered through a low-pass transfer function due to the hold capacitor and the diode resistance. Using Volterra series analysis, we can calculate the distortion terms [75, 76].

$$\begin{aligned} i &= C_h \frac{dv_{out}}{dt} \\ &= I_d e^{\frac{v_{in}-v_{out}}{V_t}} \\ &= I_d \left[\frac{v_{in}-v_{out}}{V_t} + \frac{(v_{in}-v_{out})^2}{2V_t^2} + \frac{(v_{in}-v_{out})^3}{6V_t^3} + ... \right] \end{aligned} \tag{II.1}$$

where I_d is the bias current through the diode and $V_t = kT/q$. For Volterra analysis, we represent the output as a Taylor series expansion with frequency-dependent coefficients as follows:

$$v_{out} = H_1(j\omega_a) \circ v_{in} + H_2(j\omega_a, j\omega_b) \circ v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3 + ... \tag{II.2}$$

Inserting (II.2) into (II.1) and looking only at the third-order or lower terms gives us:

$$
\begin{aligned}
i &= \frac{I_d}{V_t}\left[v_{in} - H_1(j\omega_a)\circ v_{in} - H_2(j\omega_a, j\omega_b)\circ v_{in}^2 - H_3(j\omega_a, j\omega_b, j\omega_c)\circ v_{in}^3\right] && \text{(II.3a)}\\
&+ \frac{I_d}{2V_t^2}\left[v_{in} - H_1(j\omega_a)\circ v_{in} - H_2(j\omega_a, j\omega_b)\circ v_{in}^2\right]^2 && \text{(II.3b)}\\
&+ \frac{I_d}{6V_t^3}\left[v_{in} - H_1(j\omega_a)\circ v_{in}\right]^3 && \text{(II.3c)}
\end{aligned}
$$

Simplifying (II.3) gives:

$$
\begin{aligned}
i &= \frac{I_d}{V_t}\left[v_{in} - H_1(j\omega_a)\circ v_{in} - H_2(j\omega_a, j\omega_b)\circ v_{in}^2 - H_3(j\omega_a, j\omega_b, j\omega_c)\circ v_{in}^3\right] && \text{(II.4a)}\\
&+ \frac{I_d}{2V_t^2}\left[\overline{(1 - H_1(j\omega_a))^2}\circ v_{in}^2 - 2\overline{(1 - H_1(j\omega_a))(H_2(j\omega_a, j\omega_b))}\circ v_{in}^3\right] && \text{(II.4b)}\\
&+ \frac{I_d}{6V_t^3}\left[\overline{1 - H_1(j\omega_a)}\right]^3\circ v_{in}^3 && \text{(II.4c)}
\end{aligned}
$$

Let us look only at the first order terms.

$$
\begin{aligned}
C_h\frac{d}{dt}H_1(j\omega_a)\circ v_{in} &= \frac{I_d}{V_t}(1 - H_1(j\omega_a)\circ v_{in}\\
j\omega_a C_h H_1(j\omega_a)\circ v_{in} &= \frac{I_d}{V_t}\circ v_{in} - \frac{I_d}{V_t}H_1(j\omega_a)\circ v_{in}\\
H_1(j\omega_a)(j\omega_a C_h + \frac{I_d}{V_t}) &= \frac{I_d}{V_t}\\
H_1(j\omega_a) &= \frac{1}{1 + j\omega_a r_d C_h} && \text{(II.5)}
\end{aligned}
$$

where $r_d = V_t/I_d$. The first-order coefficients have the same low-pass characteristic we would expect to find from a linear R-C circuit. Let us solve the second-order terms to find the second-order frequency dependent distortion.

$$
\begin{aligned}
C_h\frac{d}{dt}(H_2(j\omega_a, j\omega_b)\circ v_{in}^2) &= -g_d H_2(j\omega_a, j\omega_b)\circ v_{in}^2\\
&+ \frac{g_d}{2V_t}(1 - H_1(j\omega_a))(1 - H_1(j\omega_b))\circ v_{in}^2\\
j(\omega_a + \omega_b)C_h H_2(j\omega_a, j\omega_b) + g_d H_2(j\omega_a, j\omega_b) &= \frac{g_d}{2V_t}(1 - H_1(j\omega_a))(1 - H_1(j\omega_b)) && \text{(II.6)}
\end{aligned}
$$

where $g_d = I_d/V_t$. If we use the Volterra abbreviation $(1 - H_1(j\omega_a))(1 - H_1(j\omega_b)) = (\overline{1 - H_1(j\omega_a)})^2$ (please see Appendix II.6 for more Volterra substitutions), we can simplify into:

$$\begin{aligned} H_2(j\omega_a, j\omega_b)(j(\omega_a + \omega_b)C_h + g_d) &= \frac{g_d}{2V_t}(\overline{1 - H_1(j\omega_a)})^2 \\ H_2(j\omega_a, j\omega_b) &= \frac{(\overline{1 - H_1(j\omega_a)})^2}{2V_t(1 + j(\omega_a + \omega_b)r_dC_h)} \end{aligned} \tag{II.7}$$

HD2, the second-order harmonic distortion, is proportional to the ratio of the second-order distortion $H_2(j\omega_a, j\omega_b) \circ v_{in}^2$ to the first order term $H_1(j\omega_a) \circ v_{in}$.

$$HD2 = \frac{1}{2}\frac{|H_2(j\omega_a, j\omega_b)|}{|H_1(j\omega_a)|} \circ v_{in} \tag{II.8}$$

$$\begin{aligned} HD2 &= \left[\frac{1}{4V_t}\left(\frac{(\overline{1 - H_1(j\omega_a)})^2}{1 + j(\omega_a + \omega_b)r_dC_h}\right) \Big/ \left(\frac{1}{1 + j\omega_a r_dC_h}\right)\right] \circ v_{in} \\ &= \frac{1}{4V_t}\left|\frac{\omega_a\omega_b r_d^2 C_h^2}{(1 + j\omega_a r_dC_h)(1 + j(\omega_a + \omega_b)r_dC_h)}\right| \circ v_{in} \end{aligned} \tag{II.9}$$

To find the third-order frequency dependent distortion we collect all third-order terms from (II.4 a)-c)).

$$\begin{aligned} &C_h\frac{d}{dt}(H_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3) = -g_dH_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3 \\ &\quad -\frac{g_d}{V_t}\left[(\overline{1 - H_1(j\omega_a))H_2(j\omega_b, j\omega_c)} \circ v_{in}^3\right] + \frac{g_d}{6V_t^2}\left[(\overline{1 - H_1(j\omega_a)}^3 \circ v_{in}^3\right] \\ &C_hj(\omega_a + \omega_b + \omega_c)H_3(j\omega_a, j\omega_b, j\omega_c) + g_dH_3(j\omega_a, j\omega_b, j\omega_c) = \\ &\quad -\frac{g_d}{V_t}\left[(\overline{1 - H_1(j\omega_a))H_2(j\omega_b, j\omega_c)}\right] + \frac{g_d}{6V_t^2}\left(\overline{1 - H_1(j\omega_a)}\right])^3 \\ &H_3(j\omega_a, j\omega_b, j\omega_c)\left(j(\omega_a + \omega_b + \omega_c)C_h + g_d\right) = \\ &\quad -\frac{g_d}{V_t}\left[(\overline{1 - H_1(j\omega_a))H_2(j\omega_b, j\omega_c)}\right] + \frac{g_d}{6V_t^2}\left(\overline{\frac{j\omega_a r_dC_h}{1 + j\omega_a r_dC_h}}\right)^3 \end{aligned} \tag{II.10}$$

Dividing both sides by g_d and substituting for $\overline{(1 - H_1(j\omega_a))H_2(j\omega_b, j\omega_c)}$,

$$\begin{aligned} &H_3(j\omega_a, j\omega_b, j\omega_c)\,(1 + j(\omega_a + \omega_b + \omega_c)r_d C_h) \\ &\quad = \frac{-1}{2V_t^2}\left(\overline{\frac{j\omega_a r_d C_h}{1 + j\omega_a r_d C_h}}\right)^3 \left(\overline{\frac{1}{1 + j(\omega_a + \omega_b)r_d C_h}}\right) + \frac{1}{6V_t^2}\left(\overline{\frac{j\omega_a r_d C_h}{1 + j\omega_a r_d C_h}}\right)^3 \\ &\quad = \frac{1}{2V_t^2}\left(\overline{\frac{j\omega_a r_d C_h}{1 + j\omega_a r_d C_h}}\right)^3 \left(\overline{\frac{-1}{1 + j(\omega_a + \omega_b)r_d C_h}} + \frac{1}{3}\right) \end{aligned} \tag{II.11}$$

Dividing each side of (II.11) by $(1 + j(\omega_a + \omega_b + \omega_c)r_d C_h)$ we have:

$$\begin{aligned} &H_3(j\omega_a, j\omega_b, j\omega_c) = \\ &\frac{1}{2V_t^2(1 + j(\omega_a + \omega_b + \omega_c)r_d C_h)}\left(\overline{\frac{j\omega_a r_d C_h}{1 + j\omega_a r_d C_h}}\right)^3 \left(\overline{\frac{-1}{1 + j(\omega_a + \omega_b)r_d C_h}} + \frac{1}{3}\right) \end{aligned} \tag{II.12}$$

From this we can calculate the third-order harmonic distortion, HD3. HD3 is the ratio of the third-order distortion to the fundamental. It is defined for Volterra coefficients as:

$$HD3 = \frac{1}{4}\frac{|H_3(j\omega_a, j\omega_b, j\omega_c)|}{|H_1(j\omega_a)|} \circ v_{in}^2 \tag{II.13}$$

For our circuit the HD3 becomes:

$$\begin{aligned} &HD3 \;\; = \\ &\left|\frac{1 + j\omega_a r_d C_h}{2V_t^2(1 + j(\omega_a + \omega_b + \omega_c)r_d C_h)}\left(\overline{\frac{j\omega_a r_d C_h}{1 + j\omega_a r_d C_h}}\right)^3 \left(\overline{\frac{-1}{1 + j(\omega_a + \omega_b)r_d C_h}} + \frac{1}{3}\right)\right| \circ v_{in}^2 \end{aligned} \tag{II.14}$$

where $r_d = V_t/I_d$, I_d is the dc bias current through one side of the diode bridge, and ω is the frequency in radians per second. One must substitute ω_a, ω_b, and ω_c with the input signals of interest. For a two-tone test, $\omega_a = \omega_b$, and ω_c will be a nearby signal with negative sign

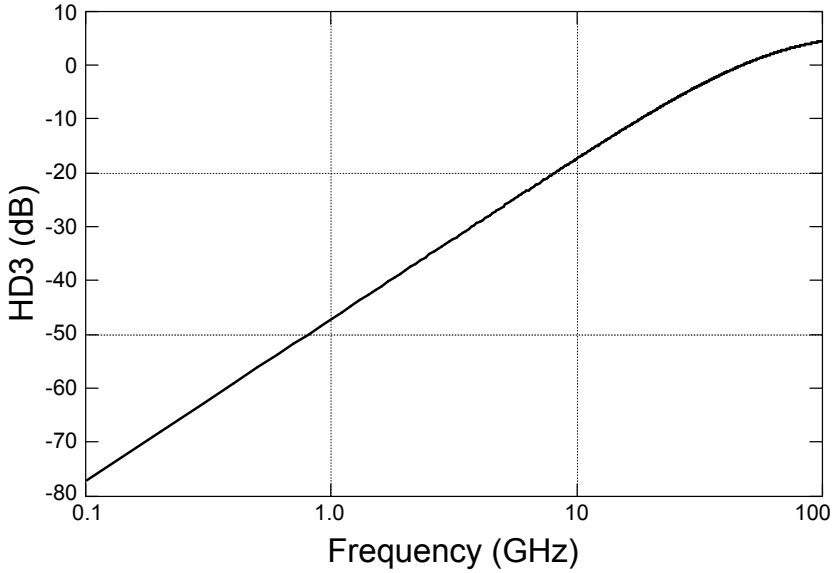

Figure II.11: Calculated third-order harmonic distortion, HD3, $v_{in} = 600mV$, $C_h = 325fF$ and $I_d = 7mA$.

such that when added together they equal $2\omega_a - \omega_c$, which would be the third-order in-band distortion term often analyzed.

Not surprisingly, higher frequency signals will produce more distortion, and increased dc current helps to minimize the distortion. These results quantify the well-known tradeoff between current and distortion and AM-PM conversion in the diode bridge. The hold capacitor and bias current were chosen using this result to minimize these effects. For our circuit (see Fig. II.11) with $C_h = 325fF$, I_d is the $7mA$ bias current through one side of the diode bridge, and v_{in} is the maximum input voltage of $600mV$, the calculated HD3 has been plotted versus input frequency.

For the voltage on the hold capacitor, if $v_{in} = A \cdot cos(\omega t)$, the output signal will

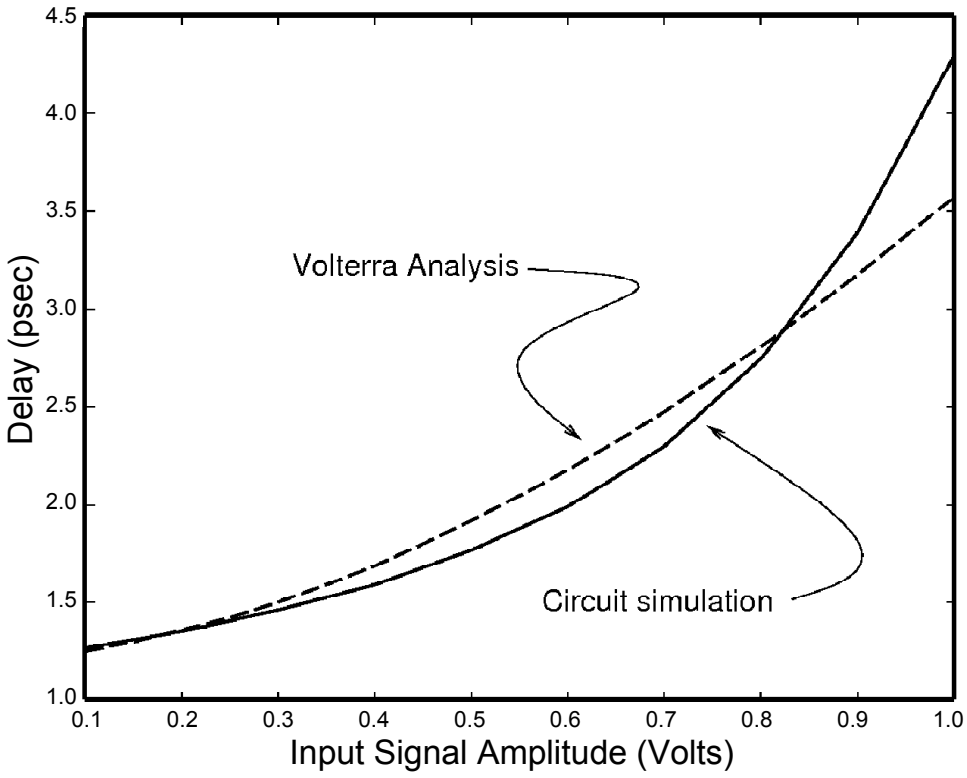

Figure II.12: Amplitude dependent delay - Volterra analysis and circuit simulated, $C_h = 325fF$ and $I_d = 7mA$.

have a cubic term that contains a complex first-order term in $A \cdot cos(\omega t)$. This complex term will alter the phase of the fundamental at the output in an amplitude dependent manner, resulting in the signal-dependent delay. In Figure II.12, this delay is plotted versus input amplitude for the above Volterra analysis and circuit simulations.

II.3.2 Aperture Error

As the THA transitions into the hold state, the current flowing through the diode-bridge will go to zero over a finite amount of time. The time from between when the *hold phase* is initiated and when the current through the bridge equals zero is known as the "aperture", labelled time t_A in Fig. II.13 [36]. Along with establishing how quickly the diode-bridge can be switched, the aperture establishes the highest allowable input frequency, since signals with a frequency equal to an integral multiple of $1/t_A$ complete full cycles during t_A and average to zero.

During the *track phase*, charge accumulates on the parasitic capacitance of the current source (c_p in Fig. II.13). When the diode-bridge is turned off, this charge drains through the diode-bridge, extending the aperture. Reducing the capacitance in the current sources contributes to a shorter aperture and a larger signal bandwidth.

The voltage is held on the hold capacitor when the current entering the hold capacitor equals the current leaving it. Positively changing signals will inject a small current proportional to dv_{in}/dt onto the hold capacitor from the current source, thereby shortening the aperture and creating non-uniform sampling and distortion. Signals with a negative

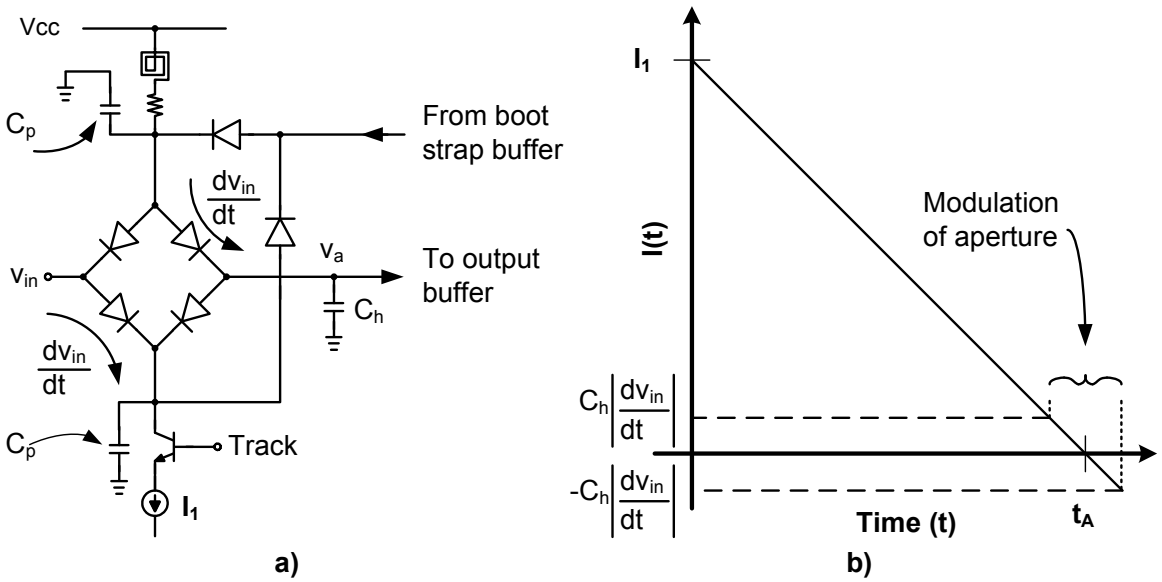

Figure II.13: a) Schematic. b) Aperture of diode-bridge, with aperture modulation error.

slope will pull current from the hold capacitor, and lengthening the time until the voltage is fixed.

Let us examine this perturbation of the aperture more closely in the presence of a linearly decreasing bias current. The current decays as shown in the equation below.

$$I(t) = -\frac{I_1}{t_A}\, t + I_1 \tag{II.15}$$

where I_1 is the bias current of the diode bridge, t is time, and t_A is the aperture time. Ignoring aperture distortion, when $t = t_A$, $I(t_A) = 0$. To determine how the sampling time is perturbed by the charge injection from the input signal, we solve (II.15) for t.

$$t = t_A \left(1 - \frac{I(t)}{I_1}\right) \tag{II.16}$$

In the presence of a time varying input signal, the sample time is perturbed by the current injected onto the hold capacitor. $I(t_A)$ is no longer equal to zero. Instead, $I(t_A) = C_h \frac{dv_{in}}{dt}$.

And (II.16) becomes:

$$t = t_A \left(1 - \frac{C_h}{I_1}\frac{dv_{in}}{dt}\right) \tag{II.17}$$

If the voltage on the hold capacitor, $v_a(t)$ is a simple sine wave, then $v_a(t) = Acos\omega t$. In the presence of a time varying input signal, inserting (II.17) into v_a at time $t = t_A$, we get:

$$v_a(t_A) = Acos\left(\omega t_A \left(1 - \frac{C_h}{I_1}\frac{dv_{in}}{dt}\right)\right) \tag{II.18}$$

If we assume that without aperture distortion $v_a = v_{in}$, then $v_{in} = Acos\omega t$. So

$$\frac{dv_{in}}{dt} = A\omega sin(\omega t) \tag{II.19}$$

And (II.18) becomes:

$$v_a(t_A) = Acos[\omega t_A(1 - \frac{AC_h\omega}{I_1}sin(\omega t_A))]$$

$$v_a(t_A) = Acos(\omega t_A + \beta sin\omega t_A) \tag{II.20}$$

where $\beta = -AC_h\omega^2 t_A/I_1$. You can see from (II.20), that the aperture modulation is analogous to phase modulation and can be analyzed identically. We can also write (II.20) in the form

$$v_a(t_A) = ARe(e^{j\omega t_A}e^{j\beta sin\omega t_A}) \tag{II.21}$$

Since $e^{j\beta sin\omega t_A}$ is periodic, it can be represented as a Fourier series. The coefficients of the Fourier series do not have a closed-form expression, but, as Bessel functions, they are well-known. With the Bessel coefficients, The Fourier series is written

$$e^{j\beta sin\omega t_A} = \sum_{n=-\infty}^{\infty} J_n(\beta)e^{jsin\omega t_A} \tag{II.22}$$

where $J_n(\beta)$ are the Bessel coefficients. The modulated waveform is now

$$v_a(t_A) = A \sum_{n=-\infty}^{\infty} J_n(\beta) cos(\omega t_A + n\omega t_A) \tag{II.23}$$

This is a Bessel function. Bessel functions have a recursive relationship of the form [77]

$$J_{-n}(\beta) = (-1)^n J_n(\beta) \tag{II.24}$$

When $\beta << 1$, the Bessel coefficients can be approximated as follows [77]

$$J_0(\beta) = 1 + 1/4\beta^2 \tag{II.25a}$$

$$J_1(\beta) = 1/2\beta \tag{II.25b}$$

$$J_2(\beta) = 0.12\beta^2 \tag{II.25c}$$

so now, (II.22) becomes

$$\begin{aligned} v_a(t_A) &= A \sum_{n=-1}^{1} J_n(\beta) cos(\omega t_A + n\omega t_A) \\ &= A[J_{-2}(\beta) cos(\omega t_A - 2\omega t_A) + J_{-1}(\beta) cos(\omega t_A - \omega t_A) + J_0(\beta) cos(\omega t_A) \\ &\quad + J_1(\beta) cos(\omega t_A + \omega t_A) + J_2(\beta) cos(\omega t_A + 2\omega t_A)] \\ &= A[J_{-2}(\beta) cos(-\omega t_A) - J_1(\beta) + J_0(\beta) cos(\omega t_A) \\ &\quad + J_1(\beta) cos(2\omega t_A) + J_2(\beta) cos(3\omega t_A)] \end{aligned} \tag{II.26}$$

Using the recursive relationship in (II.24), we can reduce further.

$$\begin{aligned} v_a(t_A) &= A\Big[[J_0(\beta) + J_2(\beta)] cos(\omega t_A) - J_1(\beta) + J_1(\beta) cos(2\omega t_A) \\ &+ J_2(\beta) cos(3\omega t_A)\Big] \end{aligned}$$

$$
\begin{aligned}
&= A\Big[-J_1(\beta) + [J_0(\beta) + J_2(\beta)]cos(\omega t_A) + J_1(\beta)[cos^2(\omega t_A) - 1] \\
&\quad + J_2(\beta)[4cos^3(\omega t_A) - 3cos(\omega t_A)]\Big] \\
&= A\Big[-2J_1(\beta) + [J_0(\beta) - 2J_2(\beta)]cos(\omega t_A) + J_1(\beta)cos^2(\omega t_A) \\
&+ \quad 4J_2(\beta)cos^3(\omega t_A)\Big]
\end{aligned}
\tag{II.27}
$$

Using (II.25 a)- c)) with (II.27), we now have

$$
v_a(t_A) = \underbrace{-A\beta}_{a_0} + \underbrace{A}_{a_1} cos\omega t_A + \underbrace{A\beta}_{a_2} cos^2\omega t_A + \underbrace{.48A\beta^2}_{a_3} cos^3\omega t_A \tag{II.28}
$$

where A is the peak input voltage and $\beta = -AC_h\omega^2 t_A/I_1$. We now have an equation for the voltage on the hold capacitor accounting for the aperture modulation from the input signal getting injected onto the hold capacitor.

The third-order distortion, HD_3, is defined as the ratio of the third-order distortion to the fundamental and can be shown to be

$$
HD_3 = \frac{1}{4}\frac{a_3}{a_1}v_{in}^2 = \frac{0.48A\beta^2}{4A}v_{in}^2 = 0.12\beta^2A^2 \tag{II.29}
$$

HD_3 is calculated when the input signal is at its peak level ($v_{in} = A$). For example, HD_3 is $-50dB$ for a peak input signal of $600mV$, 14mA bias current through the diode-bridge, a $325fF$ hold capacitor, and an input signal of 1GHz.

As mentioned at the beginning of this section, the aperture is an indication of the upper limit of the input bandwidth. We can rewrite HD_3, substituting $1/f_{3dB}$ for t_A in β. So now HD_3 becomes

$$
HD_3 = 0.12\beta^2A^2 = 0.12\left(\frac{-AC_h\omega^2}{I_1 f_{3dB}}\right)^2 A^2 = 0.12\left(\frac{\omega^2}{\omega_{3dB}}\right)^2\left(\frac{2\pi A^2 C_h}{I_1}\right)^2 \tag{II.30}
$$

Thus, a broad bandwidth will help reduce the third-order distortion, as will a small hold capacitor and increased dc current bias through the diode bridge.

II.3.3 Pedestal Distortion

Ideally, the held voltage will be flat from the moment the hold phase is initiated. However charge is often injected onto the hold capacitor at the start of the *hold* phase, creating a small pedestal on the nominally flat held voltage. If this pedestal is not signal dependent it will contribute to clock feed-through since a small voltage will be added to the input signal at every clock cycle. However, if the pedestal is signal dependent, the distortion of the resulting signal is difficult to remove by subsequent stages. To remove or reduce the distortion, one must know the transfer function of the distortion and be able to cancel it. It is often easier to reduce the distortion before it is created, rather than remove it later, especially at clocking speeds in the gigahertz range.

During the track phase while the diodes in the diode-bridge are forward biased, charge is stored across the diode junction and discharged when the circuit switches to the hold phase. If $v_b = v_a$, (see Fig. II.14), the change in charge on diodes D_2 and D_4 will be identical to the change in diodes D_5 and D_6 and no charge will be added or removed from the hold capacitor, C_h. But due to an inherent delay through the output and unity gain buffers, $v_b \neq v_a$, and the charge on the hold capacitor will change proportionally to the difference between the two voltages. Let us designate the change in voltage across D_2, D_4, D_5 and D_6 as the THA moves into the hold phase to be Δv and let v_{dx} be the

forward bias voltage of any one of the diodes, where x is the number of the diode from Fig. II.14. We will call the voltage difference between D_2 and D_5, ΔV_1 and the difference between D_4 and D_6, ΔV_2. Charge given up or accepted by diodes D_1 and D_3 is absorbed by either the current source or the input buffer and does not add charge to the hold capacitor. Relating nodes v_a and v_b we have:

$$\Delta V_1 = v_a + v_{d2} - (v_b + v_{d5}) \tag{II.31a}$$

$$\Delta V_2 = v_a - v_{d4} - (v_b - v_{d6}) \tag{II.31b}$$

Since the diodes are the same size and have identical current bias conditions, $v_{d2} = v_{d4} = v_{d5} = v_{d6}$. So

$$\Delta V_1 = v_a - v_b \tag{II.32a}$$

$$\Delta V_2 = v_a - v_b \tag{II.32b}$$

The total change in voltage during the transition from *track* to *hold* across the diodes Δv is:

$$\Delta v = \Delta V_1 + \Delta V_2 = 2(v_a - v_b) \tag{II.33}$$

If v_b is a delayed version of v_a, such that $v_b = v_a e^{-j\omega\tau}$, where τ is the delay through the bootstrap amplifier, then

$$\Delta v = 2v_a(1 - e^{-j\omega\tau}) \approx 2v_a\omega\tau \tag{II.34}$$

for small values of $\omega\tau$.

To compute Δv, we start with the small-signal diode junction capacitance model:

$$C_j = \frac{C_{jo}}{(1 - V_d/\phi_d)^n} \tag{II.35}$$

where V_d is the bias voltage across the diode, ϕ_d is built in potential of the diode, C_{jo} is the zero-bias junction capacitance (approximately $2.2fF/\mu m^2$ for this process), and *n* is $\approx 1/2$ [78]. The charge mismatch between diodes D_2 and D_5, and diodes D_4 and D_6, sum to create the total charge distortion added to the hold capacitor, ΔQ. ΔQ can be found by integrating (II.35) from $-v_d - \Delta v/2$ to $-v_d + \Delta v/2$, as described in Fig. II.14 b).

$$\begin{aligned}
\Delta Q &= \int_{-V_0-\frac{\Delta v}{2}}^{-V_0+\frac{\Delta v}{2}} \frac{C_{j0}dV}{(1 - V/\phi_d)^{1/2}} && \text{(II.36a)}\\
&= -2C_{jo}\phi_d\sqrt{1 - V/\phi_d}\,\Big|_{-V_0-\frac{\Delta v}{2}}^{-V_0+\frac{\Delta v}{2}} && \text{(II.36b)}\\
&= -2C_{jo}\phi_d\left(\sqrt{1 + \left(\frac{V_0 - \frac{\Delta v}{2}}{\phi_d}\right)} - \sqrt{1 + \left(\frac{V_0 + \frac{\Delta v}{2}}{\phi_d}\right)}\right) && \text{(II.36c)}
\end{aligned}$$

Using the series expansion $\sqrt{1+x} = 1 + \frac{x}{2} - \frac{x^2}{8} + \frac{x^3}{16} - \cdots$, (II.36) now becomes:

$$\begin{aligned}
\Delta Q = -2C_{jo}\phi_d\Bigg(1 + \frac{V_0 - \frac{\Delta v}{2}}{2\phi_d} - \frac{(V_0 - \frac{\Delta v}{2})^2}{8\phi_d^2} + \frac{(V_0 - \frac{\Delta v}{2})^3}{16\phi_d^3}\\
-1 - \frac{V_0 + \frac{\Delta v}{2}}{2\phi_d} + \frac{(V_0 + \frac{\Delta v}{2})^2}{8\phi_d^2} - \frac{(V_0 + \frac{\Delta v}{2})^3}{16\phi_d^3}\Bigg)
\end{aligned} \tag{II.37}$$

Expanding and then simplifying terms, we reduce the above equation to:

$$\Delta Q = C_{jo}\left(1 - \frac{V_0}{2\phi} + \frac{3V_0^2}{8\phi^2}\right)\Delta v + \frac{C_{jo}}{32\phi^2}\Delta v^3 \tag{II.38}$$

This is the charge distortion at the output of the diode-bridge. This charge distortion is added to the hold capacitor yielding a voltage, v_{dis} which is equal to $\Delta Q/C_h$.

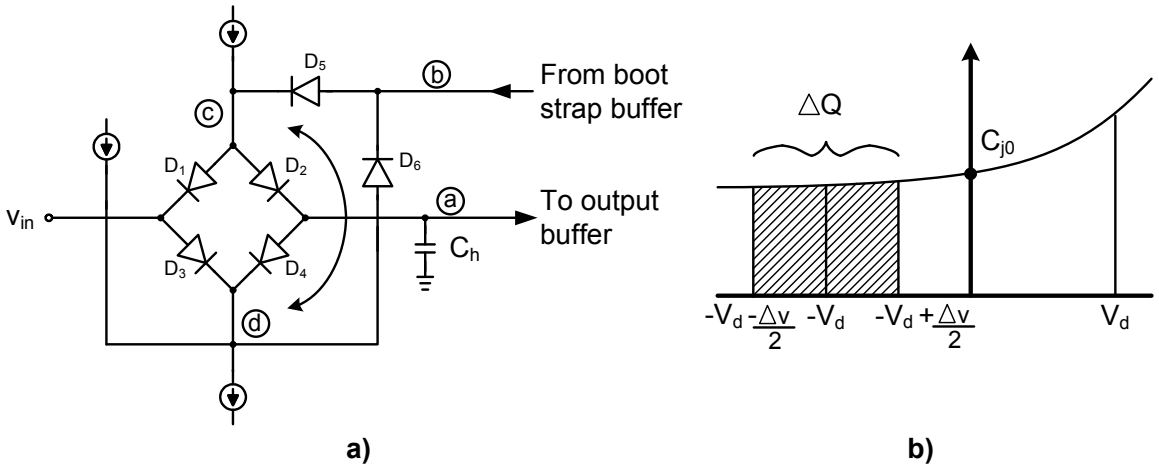

Figure II.14: Hold pedestal distortion in diode bridge. a) Schematic showing the charge path to the hold capacitor. b) Small-signal diode junction capacitance model.

Thus, the distortion on the hold capacitor is:

$$v_{dis} = \frac{C_{jo}}{C_h}\left(1 - \frac{V_0}{2\phi} + \frac{3V_0^2}{8\phi^2}\right)\Delta v + \frac{C_{jo}}{32\phi^2 C_h}\Delta v^3 \tag{II.39}$$

From (II.34) we already know $\Delta v \approx 2\omega\tau v_a$. Substituting for Δv into (II.39) we get:

$$v_{dis} = \frac{2\omega\tau C_{jo}}{C_h}\left(1 - \frac{V_0}{2\phi} + \frac{3V_0^2}{8\phi^2}\right)v_a + \frac{\omega^3\tau^3 C_{jo}}{4\phi^2 C_h}v_a^3 \tag{II.40}$$

This distortion is added to the signal on the hold capacitor, v_a making the output signal:

$$v_{out} = \underbrace{\left[1 + \frac{2\omega\tau C_{jo}}{C_h}\left(1 - \frac{V_0}{2\phi} + \frac{3V_0^2}{8\phi^2}\right)\right]}_{a_1} v_a + \underbrace{\frac{\omega^3\tau^3 C_{jo}}{4\phi^2 C_h}}_{a_3} v_a^3 \tag{II.41}$$

We see by the delay dependent term in a_1 in (II.41) a gain error exists. For this analysis, the voltage at the hold capacitor v_a is equal to v_{in}, and so the gain through the

diode-bridge is:

$$Gain = 1 + \frac{2\omega\tau C_{jo}}{C_h}\left[1 - \frac{V_0}{2\phi} + \frac{3V_0^2}{8\phi^2}\right] \tag{II.42}$$

As (II.41) and (II.42) show, if the delay through the loop, τ, is zero, the gain error is zero. The gain error shows expansion since the signal through the feedback path is in phase with the input signal. Loop stability is not a problem since this gain error does not exist during the track mode, but only at the transition between track and hold.

We can calculate the third-order harmonic distortion, HD3, from (II.41). HD3 is defined as the ratio of the third-order distortion to the fundamental tone. Specifically, it is defined as:

$$HD3 = \frac{1}{4}\frac{a_3}{a_1}v_a^2 \tag{II.43}$$

Substituting the coefficients from (II.41) into (II.43) we have:

$$\begin{aligned} HD3 &= \frac{1}{4}\frac{\frac{\omega^3\tau^3 C_{jo}}{4\phi^2 C_h}}{\left[1 + \frac{2\omega\tau C_{jo}}{C_h}\left(1 - \frac{V_0}{2\phi} + \frac{3V_0^2}{8\phi^2}\right)\right]}v_a^2 \\ &= \frac{1}{32\phi^2}\frac{\omega^2\tau^2 v_a^2}{\left(1 + \frac{C_h}{2\omega\tau C_{jo}} - \frac{V_0}{2\phi} + \frac{3V_0^2}{8\phi^2}\right)} \end{aligned} \tag{II.44}$$

Equation II.44 is plotted in Fig: II.15 versus the input frequency and the loop delay. It can be reduced by minimizing the Schottky diode junction capacitance, and by minimizing the delay through the bootstrap buffers that determines the voltage v_b. The latter was accomplished by careful design of the high-frequency feedback circuit, as described in section V, resulting in a delay of less than 15 ps.

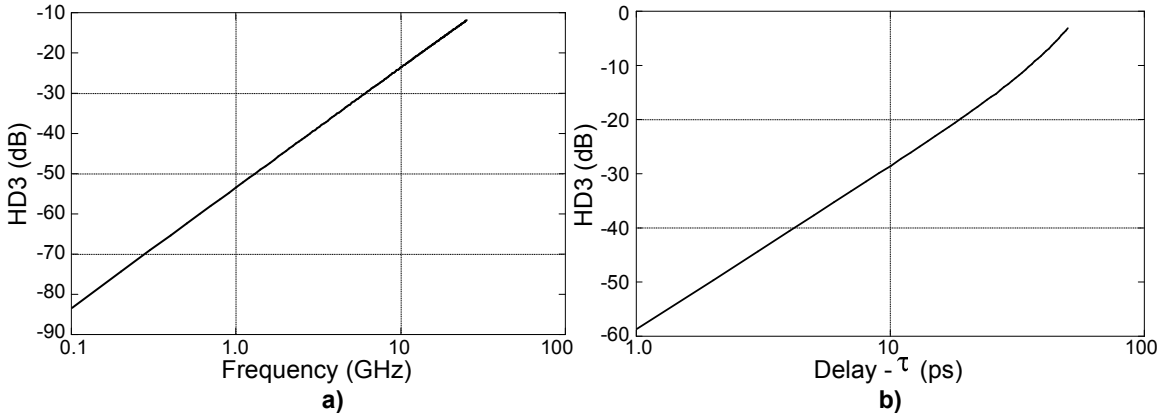

Figure II.15: (a) Calculated HD3 vs signal frequency b) Calculated HD3 versus the delay through the output buffer and boot-strap buffer. v_a equals the peak input signal of 600mV. and $C_h = 325fF$ for both plots. The input frequency was 10GHz for the delay calculation, and a 15ps loop delay was chosen for the frequency calculation.

Impact of Passive Current Source on Pedestal Distortion

As mentioned in section II.2.2, the current delivered by the passive current sources will change as the circuit changes from the track mode to the hold mode. The current through the diode bridge in the track mode is not equal to the current through the clamp diodes (D_5 and D_6 in Fig. II.16) in the hold mode. This will affect the voltage across the diodes and the charge stored on the diodes as described in (II.35).

Let us compute the change in voltage between node *a* and node *b* with the input signal equal to zero.

$$v_a = V_{dd} - I_{1t}R_1 - v_{d2} \leftarrow \textit{track mode} \tag{II.45}$$

$$v_b = V_{dd} - I_{2h}R_2 - v_{d5} \leftarrow \textit{hold mode} \tag{II.46}$$

We know v_{d2} and v_{d5} from the simple diode equations.

$$v_{d2} = V_t ln(I_{1t}/I_s) \tag{II.47}$$

$$v_{d5} = V_t ln(I_{2h}/I_s) \tag{II.48}$$

$$\Delta v = v_a - v_b = -I_{1t}R_1 - V_t ln(I_{1t}/I_s) + I_{2h}R_2 + V_t ln(I_{2h}/I_s) \tag{II.49}$$

$$\Delta v = -I_{1t}R_1 + I_{2h}R_2 + V_t ln(I_{2h}/I_{1t}) \tag{II.50}$$

Ideally, $I_1 = I_2$, but with passive current sources, when the THA goes from track to hold, the common-mode voltage at node *d* will increase and the common-mode voltage at node *c* will decrease. This will cause I_1 in the hold mode to be greater than I_2 in the track-mode. As mentioned earlier, the voltage Δv causes a mismatch in charge to build up on the diodes, and increases the pedestal error.

II.4 Experimental Results

The track-and-hold circuit was implemented in a production 0.5μm Si/SiGe BiCMOS process [63, 68]. Total power consumption was approximately 550mW, including the 50 Ω output buffer, with a power supply voltage of 5.2 Volts. A die photograph of the complete chip is shown in Figure II.21. The chip measured 2 x 1mm including probe pads.

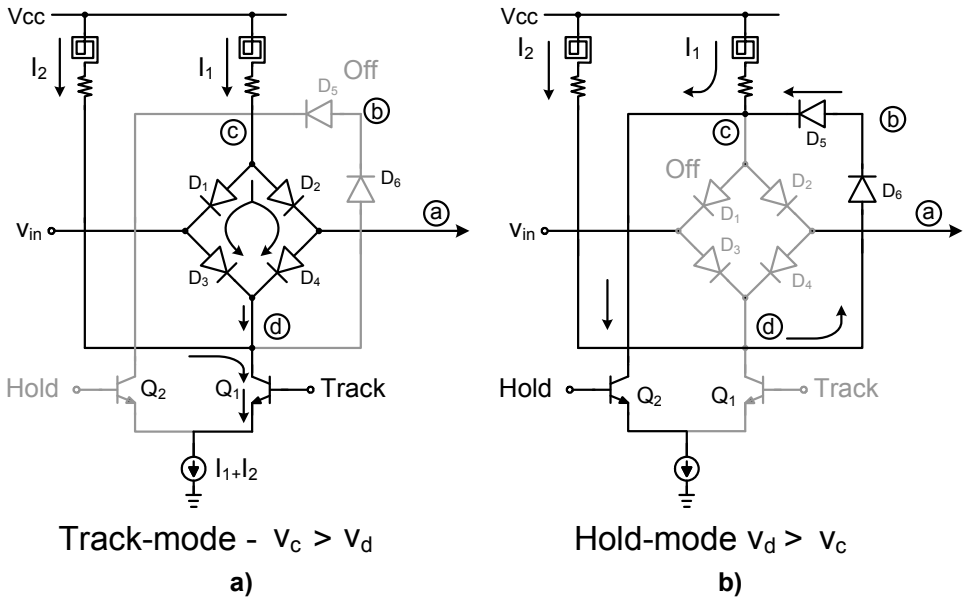

Figure II.16: The change in voltage at nodes *c* and *d* between a) *track* and b) *hold* modes will affect currents I_1 and I_2. This will increase the pedestal distortion.

The measured input 3dB bandwidth of the circuit in the track mode exceeds 10GHz. For an 8GHz input and sampling frequency of 4GHz the measured IIP3 was 26dBm and the measured IIP2 was 24dBm (see Figure II.17). The IIP2 was the major source of distortion, but can be reduced significantly at the expense of a doubling of the dc power with a differential design [25, 36]. In a 10GHz bandwidth, the maximum SFDR between the second-order distortion and the fundamental is approximately 30dB or approximately 4.7 bits. If we consider only the third-order distortion term, the SFDR between the third-order distortion and the fundamental in a 10GHz bandwidth is 41dB or ≈ 6.5 bits.

The input to the circuit is broad-band impedance matched to 50 ohms with a measured VSWR of less than 1.4:1 for frequencies up to 10 GHz. An output driver similar

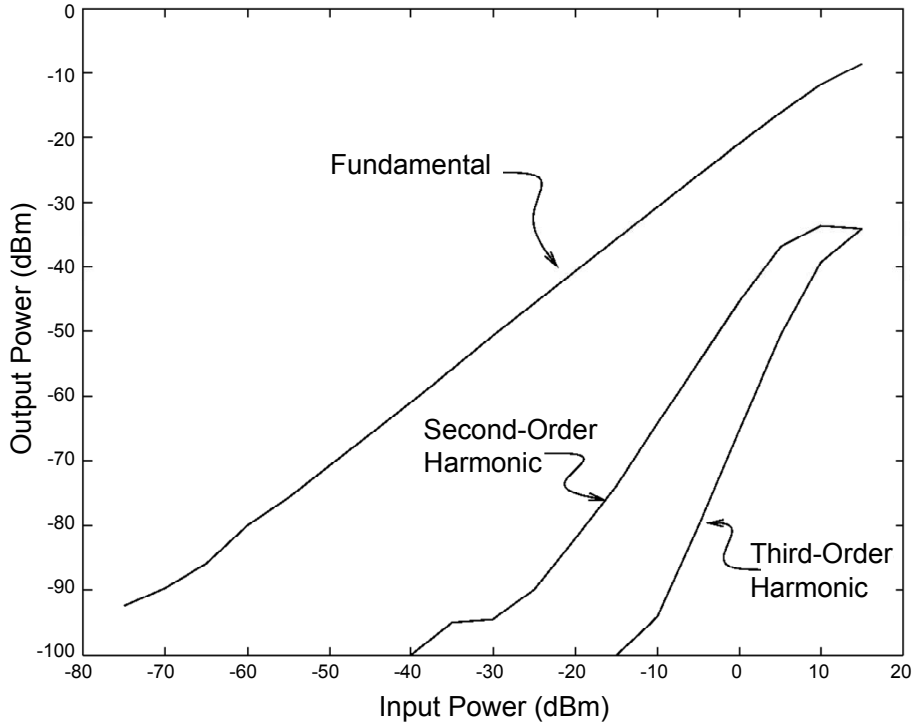

Figure II.17: (a) Measured fundamental, second-order, and third-order intermodulation curves as a function of input power.

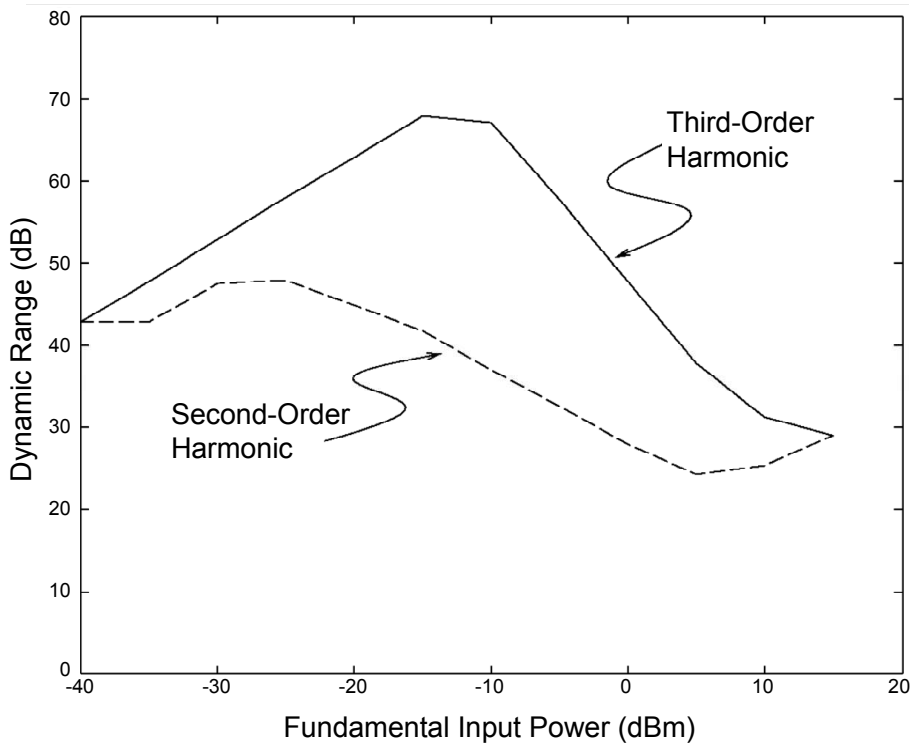

Figure II.18: Difference between fundamental and distortion terms.

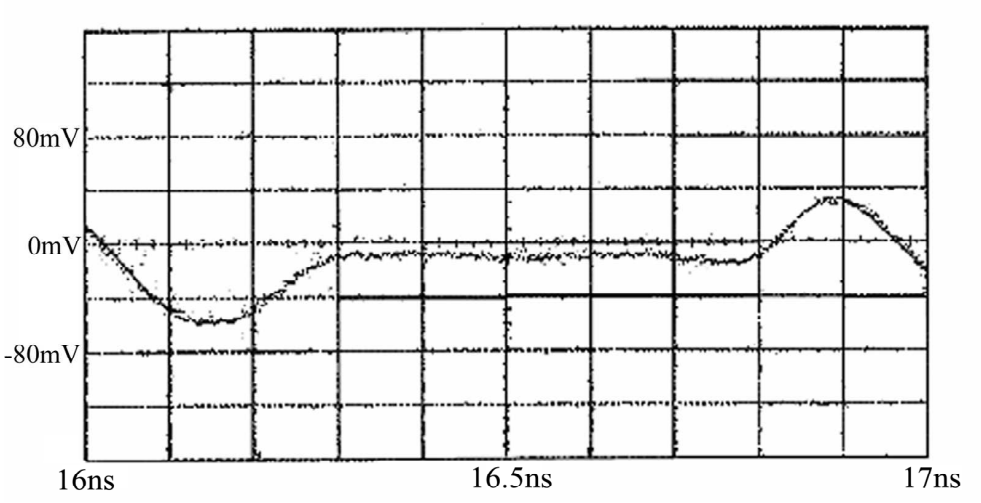

Figure II.19: Hold phase with 1 GHz clock and 2.1 GHz input signal.

to the one in [31] was used to drive a 50 Ω load impedance. The gain through the track-and-hold was -12dB; the large track mode attenuation was a product of the high series resistances in the silicon Schottky diodes.

The measured hold mode droop rate was approximately 8 mV/nS for a 2.1GHz input and 1.0GHz clock (see Figure II.19). The droop rate can be substantially reduced with a differential design.

II.5 Conclusions

An improved design has been presented for a diode-bridge track-and-hold circuit achieving wider bandwidth and lower distortion than previous circuits implemented in silicon technology, with performance comparable to the best GaAs-based track-and-holds. A standard diode-bridge design was used with an improved current source approach using series inductive loading to reduce the aperture time and lower distortion to extend performance to higher frequencies. The aspects of the track-and-hold design that lead to distortion at high frequencies were analyzed, and improvements in the circuit implemented to minimized these effects. The circuit exhibited a track-mode bandwidth in excess of 10 GHz. This circuit can be used as a building-block for next generation ultra-wide bandwidth satellite communication systems.

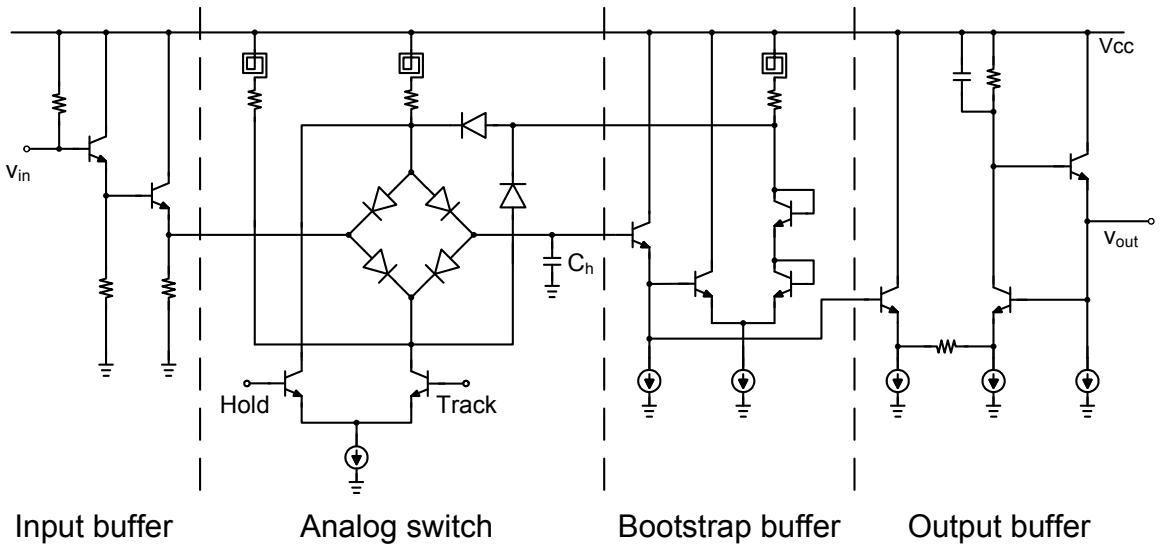

Figure II.20: Simplified schematic of diode-bridge design.

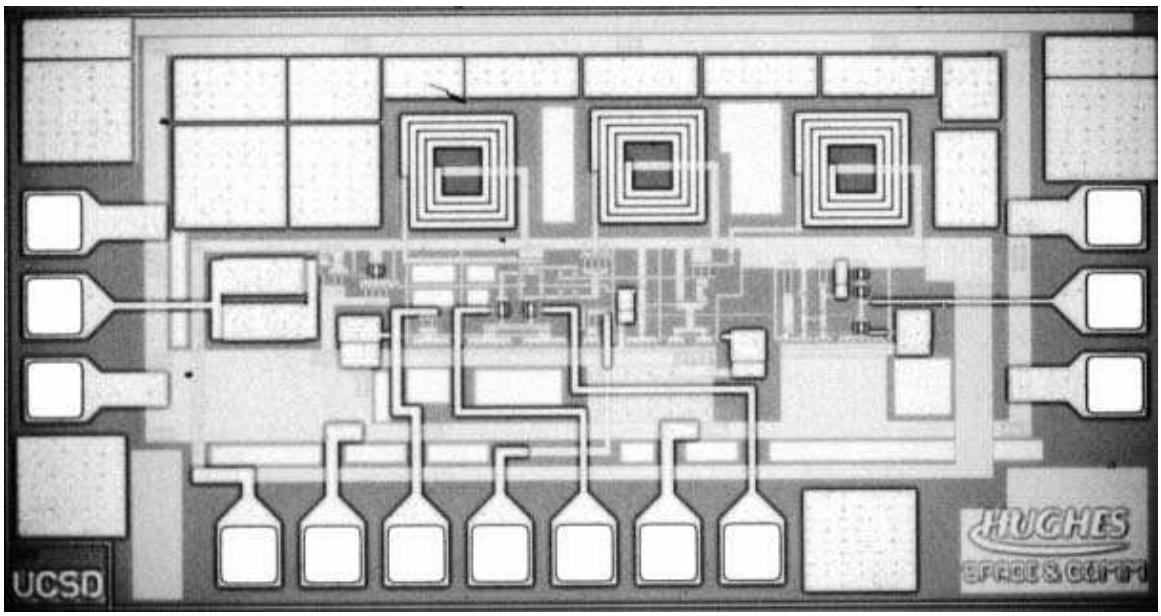

Figure II.21: Die photo of track-and-hold.

II.6 Appendix

Volterra algebra can be difficult to manage due to the complexity of the non-linear terms. Let us employ some notation to help us. Let us start with (II.10). We see $-\frac{g_d}{V_t}\left[(\overline{1-H_1(j\omega_a))H_2(j\omega_b,j\omega_c)}\circ v_{in}^3\right]$. The over-line refers to the particular frequencies we place into the equation, i.e.:

$$\overline{(1-H_1(j\omega_a))H_2(j\omega_b,j\omega_c)} =$$
$$\frac{1}{3}(1-H_1(j\omega_a))H_2(j\omega_b,j\omega_c)+\frac{1}{3}(1-H_1(j\omega_b))H_2(j\omega_a,j\omega_c)+\frac{1}{3}(1-H_1(j\omega_c))H_2(j\omega_a,j\omega_b) \tag{II.51}$$

Before we go on, we simplify $1-H_1(j\omega_b)$.

$$\begin{aligned} 1-H_1(j\omega_b) &= 1-\frac{1}{1+j\omega_a r_d C} \\ &= \frac{j\omega_a r_d C}{1+j\omega_a r_d C} \end{aligned} \tag{II.52}$$

If we go back to (II.51) and look only at the first element of the resultant.

$$\begin{aligned} \frac{1}{3}(1-H_1(j\omega_a))H_2(j\omega_b,j\omega_c) &= \frac{1}{3}\left(\frac{j\omega_a r_d C}{1+j\omega_a r_d C}\right)\left(\frac{1}{2V_t}\right)\left(\frac{(\overline{1-H_1(j\omega_b)})^2}{1+j(\omega_b+\omega_c)r_d C}\right) \\ &= \frac{1}{6V_t}\left(\frac{j\omega_a r_d C}{1+j\omega_a r_d C}\right)\left(\frac{j\omega_b r_d C}{1+j\omega_b r_d C}\right) \\ &\times \left(\frac{j\omega_c r_d C}{1+j\omega_c r_d C}\frac{1}{1+j(\omega_b+\omega_c)r_d C}\right) \end{aligned}$$

which can be simplified as:

$$\frac{1}{3}(1-H_1(j\omega_a))H_2(j\omega_b,j\omega_c) = \frac{1}{6V_t(1+j(\omega_b+\omega_c)r_d C)}\overline{\left(\frac{j\omega_a r_d C}{1+j\omega_a r_d C}\right)}^3 \tag{II.53}$$

where

$$\overline{\left(\frac{j\omega_a r_d C}{1+j\omega_a r_d C}\right)^3} = \left(\frac{j\omega_a r_d C}{1+j\omega_a r_d C}\right)\left(\frac{j\omega_b r_d C}{1+j\omega_b r_d C}\right)\overline{\left(\frac{j\omega_c r_d C}{1+j\omega_c r_d C}\right)} \tag{II.54}$$

The over-line is written over the last term to distinguish $\omega_a \times \omega_b$ from $\omega_a \times \omega_a$.

However, the second-order term, $1/(1 + j(\omega_b + \omega_c)r_d C)$, will differ. (II.51) becomes:

$$\begin{aligned}\overline{(1-H_1(j\omega_a))H_2(j\omega_b, j\omega_c)} &= \frac{1}{2V_t}\overline{\left(\frac{j\omega_a r_d C}{1+j\omega_a r_d C}\right)^3}\left[\frac{1}{3(1+j(\omega_a+\omega_b)r_d C)}\right. \\ &\left. + \frac{1}{3(1+j(\omega_b+\omega_c)r_d C)} + \frac{1}{3(1+j(\omega_c+\omega_a)r_d C)}\right]\end{aligned}$$

For the sake of brevity, I will write this above equation as:

$$\overline{(1-H_1(j\omega_a))H_2(j\omega_b, j\omega_c)} = \frac{1}{2V_t}\overline{\left(\frac{j\omega_a r_d C}{1+j\omega_a r_d C}\right)^3}\overline{\left(\frac{1}{1+j(\omega_a+\omega_b)r_d C}\right)} \tag{II.55}$$

Chapter III

High-speed SiGe Bipolar Sample-and-Hold

III.1 Introduction

In this dissertation I have stressed the requirement of next-generation millimeter-wave and optical communications systems to have low-cost, high-bandwidth receivers operating in the 20-70GHz range [5–9]. In some architectures, the intermediate frequency (IF) of the receiver chain is in the 2-4GHz range, and a second down-conversion step is usually required. Another approach employs direct digital bandpass sampling of the IF signal, as shown in Fig. III.1. In this frequency plan the sample-and-hold has the most exacting requirements on linearity for the analog-to-digital converter, in addition to the extremely wide bandwidth requirements.

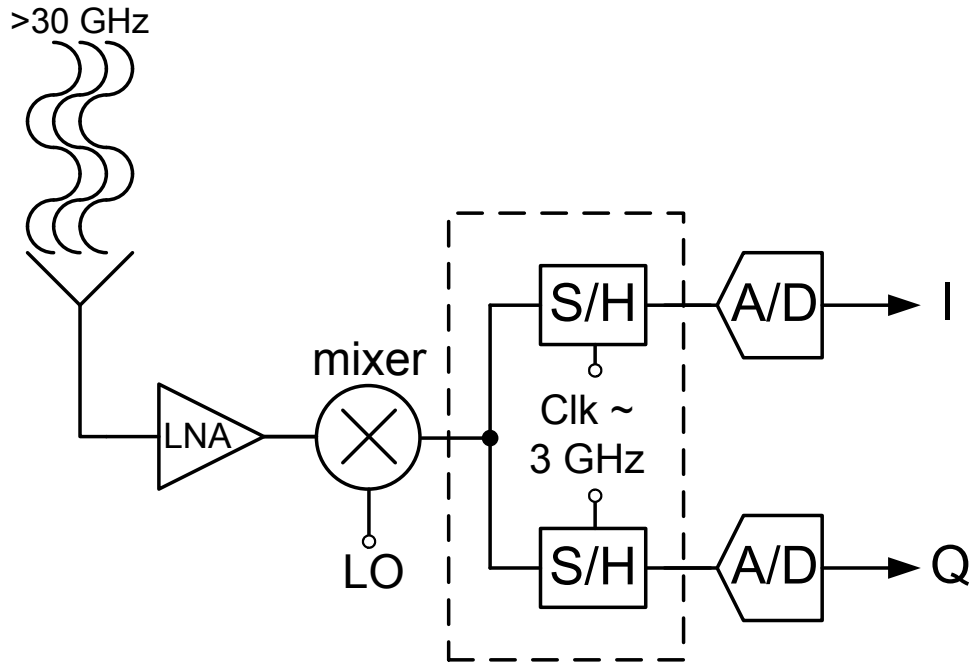

Figure III.1: High frequency receiver with digital bandpass I/Q down converter.

High-frequency, multi-stage analog-to-digital converters (ADCs) often place a sample-and-hold amplifier (SHA) before the converters. It is important that the sample-and-hold introduce very little in-band distortion, since distortion incurred in the analog portion of an ADC is difficult to remove by subsequent digital correction.

The SHA presented here was designed to consume less current and area than the SHA in the previous chapter. This chapter presents an analysis of a switched-emitter-follower based sample-and-hold, along with improved circuit design techniques to minimize the high frequency sampling errors. The bandwidth and dynamic range of this circuit at the required sample rate is superior to other SHA's in silicon technology, see Table III.1.

Table III.1: Overview of high-speed THAs performance

ref #	*Process*	*Res.*	*Fs*	*Fin*	*Power*
this work	SiGe HBT	8b	3.0GS/s	1.5GHz	0.72W
[32]	Si-HBT	8b	2.0GS/s	900MHz	0.55W
[12]	CMOS	8b	1.3GS/s	650MHz	
[11]	CMOS	6b	1.6GS/s	300MHz	
[22]	Si-Bipolar	8b	1.0GS/s	500MHz	0.44W
[35]	Si-Bipolar	10b	1.0GS/s	500MHz	0.164W
[21]	Si-Bipolar	10b	1.0GS/s	500MHz	0.30W

III.2 Track-and-Hold Architecture

The SHA must have a bandwidth greater than that of the maximum expected input signal and it must settle to the specified accuracy in a short amount of time, usually much less than half a clock cycle. Our SHA was designed to precede a moderate resolution, but high sample-rate ADC (5-6bit with 3GHz sample-rate).

Each SHA is comprised of unity-gain buffers followed by switched emitter - followers, Q_1 and Q_2 that capture the input signal onto the hold capacitor [32, 79] (see Fig. III.2). An output stage buffers the signal for the succeeding stage. Compensation capacitors, C_{comp}, are connected from the negative input node to the positive output node, and vice versa, to decrease signal feed-through during the hold phase [79]. The output buffer remains "on" during the hold phase rather than clocking them "off" in phase with with the SEF. This increased the droop rate of the signal on the hold capacitor, but greatly reduced the common-mode swing at the output. If the output buffer is turned "off" in phase with the switched-emitter-follower, SEF, negligible base current will remove charge from the hold capacitor, but the common-mode voltage with increase as the V_{be} collapses. Since the SEF

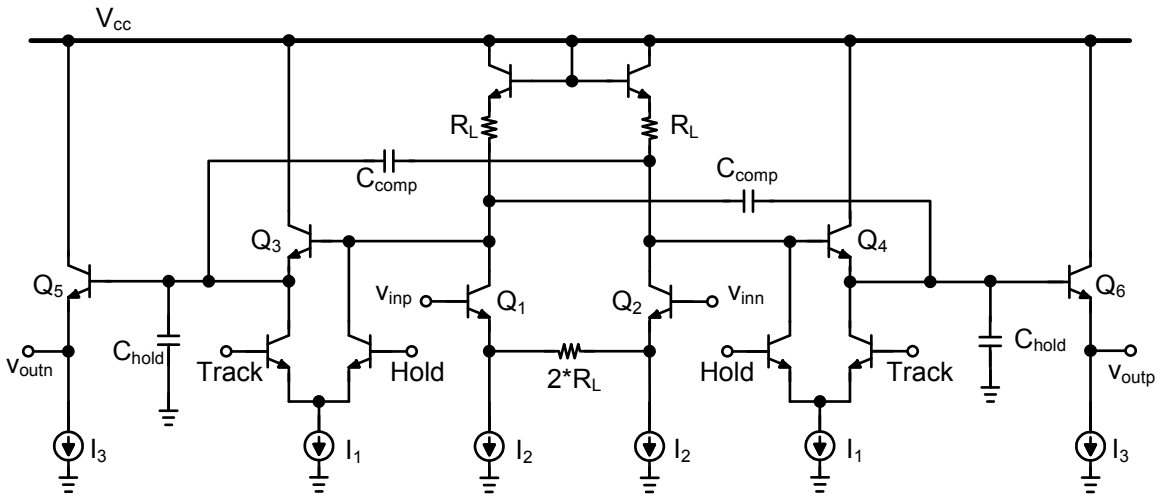

Figure III.2: Architecture of bipolar track-and-hold amplifier with switched-emitter follower and compensation capacitors.

and output buffers are dc coupled and supply referenced, the common-mode voltage at the output increases by one V_{be} when the SEF is turned *off* and two V_{be}, approximately 1.5V, when the SEF and the output stage are turned "off" at the same time. Simulations show excessive ringing in subsequent stages, the comparator buffer, when both stages are turned off at the same time. Another buffer stage could be added between the SHA and the ADC to reduce the common-mode shift during the hold-mode transition, but since the droop-rate when the output buffers "on" was not outside of specifications, the output buffer was not clocked.

Cascode devices, not shown in the simplified figure, were placed between the clock signal and the switched emitter-follower to reduce the clock injection onto the held signal. Simulations show the clock signal is reduced slightly by approximately 1dB at

3GHz. A 1dB reduction in clock feed-through is generally not large enough to warrant the addition of a cascode device and increasing the headroom of the SHA. But due to the existing input and output common-mode voltages, the cascode devices were added without increasing the headroom.

III.2.1 Switched Emitter-Follower Distortion

As mentioned above, this sample-and-hold was comprised of three parts: a highly linear, degenerated, differential input pair, Q_1 and Q_2; a pair of switched-emitter followers, Q_3 and Q_4 with a hold capacitor; and the output buffer, Q_5 and Q_6. The highly degenerated differential input pair showed very linear behavior almost to the point where all the bias current is switched to one side [80]. This occurs when the input voltage, $v_{inp} - v_{inn}$, is approximately $2I_2 * R_L$. For our circuit, the linear region extends to a peak input voltage of 2V, leaving the next stages, the SEF and output buffer, as the limiting factor in meeting the linearity requirements. Emitter-followers have inherent distortion mechanisms that must be overcome for a highly linear SHA. The SEF and the output buffer are both emitter-followers, but the output buffer drives a smaller load capacitance and will not be the limiting factor in the linearity. The switched-emitter-follower, driving the hold capacitor, will place the limit on the performance of the sample-and-hold, and Volterra analysis will provide insight into the nonlinear behavior of the circuit (see Fig. III.3).

Let us assume ideal resistance and capacitance in the small-signal model seen in

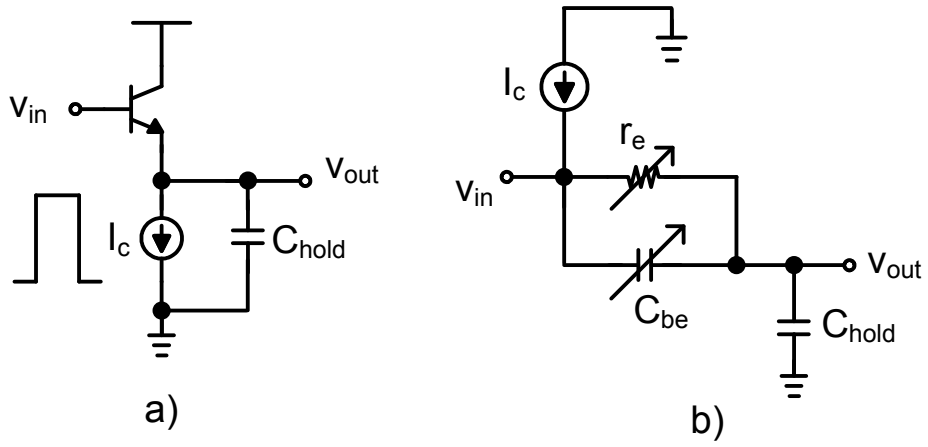

Figure III.3: (a) Simplified switched emitter-follower sample-and-hold circuit. (b) Small-signal equivalent circuit with non-linear emitter resistance and base-emitter capacitance.

Fig. III.3 b). The linear transfer function, $T_A = v_{out}/v_{in}$, can be described as:

$$T_A(\omega) = \frac{1 + j\omega r_e C_{be}}{1 + \omega r_e (C_{be} + C_{hold})} \tag{III.1}$$

At low frequencies the SEF looks like a low pass filter; but at high frequencies it tends toward a capacitive divider (see Fig. III.4). The size of the emitter-follower as well as the size of the hold capacitor determine the first-order transfer function of the SEF. Figures III.4 b) and III.5 a) and b) show T_A from (III.1) plotted against frequency, current and the load capacitance while holding the other two variables constant. As will be shown below, we want to adjust the three independent variables such that the transfer function is close to unity to reduce the total harmonic distortion.

A more accurate depiction of the SEF includes the nonlinear behavior of emitter resistance and the base-emitter capacitance. First let's look at the generalized Volterra

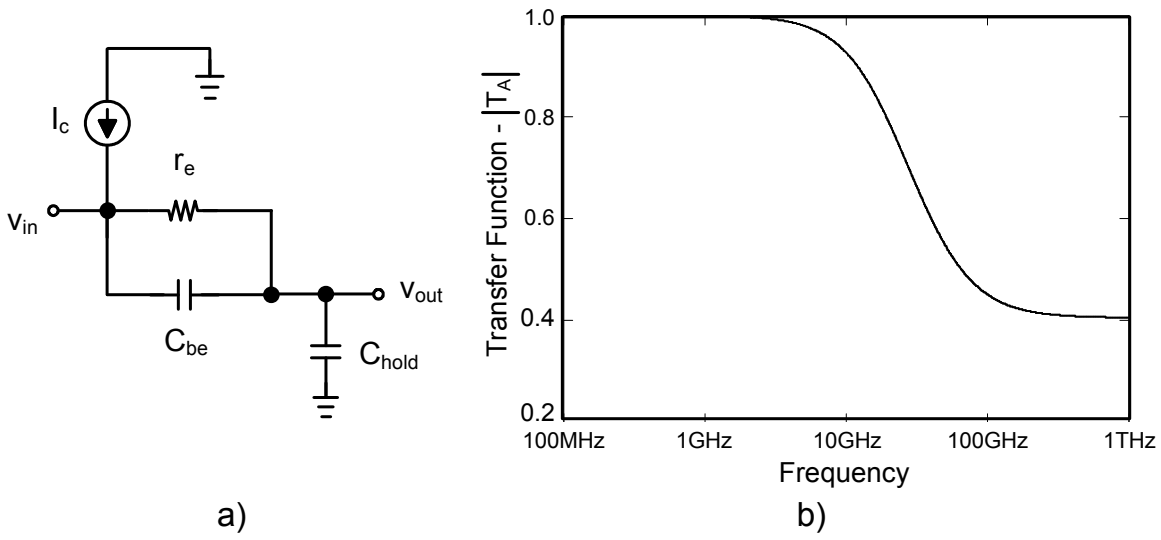

Figure III.4: (a) Linear small-signal equivalent circuit of emitter followers. (b) Linear SEF transfer function as a function of frequency current, $f_T = 55GHz$, $I_c = 6mA$, and $C_{hold} = 325fF$.

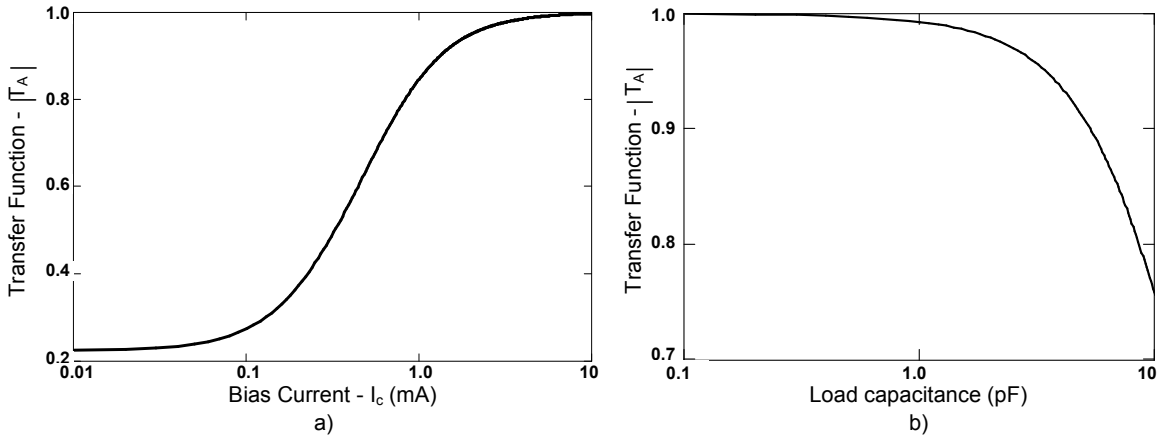

Figure III.5: Linear SEF transfer function as a function of a) bias current where $f_T = 55GHz$, $f_{in} = 3GHz$ and $C_{hold} = 325fF$ and b) hold capacitance where $f_T = 55GHz$, $f_{in} = 3Ghz$ and $I_c = 6mA$.

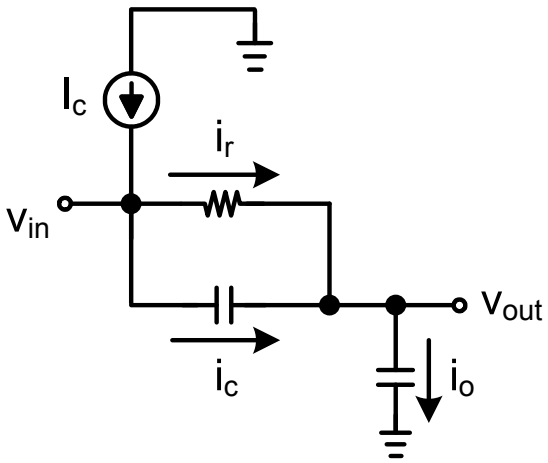

Figure III.6: Currents flowing through switched-emitter-follower used for distortion analysis.

equations. Any nonlinear transfer function can be given by:

$$v_{out} = H_1(j\omega_a) \circ v_{in} + H_2(j\omega_a, j\omega_b) \circ v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3 \tag{III.2}$$

From Fig. III.6, we sum the currents and solve for the Volterra kernels: $H_1(j\omega_a)$, $H_2(j\omega_a, j\omega_b)$ and $H_3(j\omega_a, j\omega_b, j\omega_c)$, where ω_a, ω_b and ω_c are the input frequencies to the emitter-follower. The source impedance is assumed to be zero for ease of computation. This approximation is valid where $R_L << r_b + r_\pi$, where R_L is the load resistor of the unity gain input buffer, r_b is the ohmic base resistance, and r_π is the input impedance from the base excluding the ohmic base resistance. To begin with:

$$i_r + i_c = i_o \tag{III.3}$$

Let us begin with the current through the resistor.

$$i_r = I_C e^{V_{be}/V_t} = I_C e^{(v_{in} - v_{out})/V_t} \tag{III.4}$$

where I_C is the bias current of the emitter-follower, and $V_{be} = v_{in} - v_{out}$. For clarity, we are going to include only the first through third-order distortion terms. The Taylor series representation of the natural logarithm leads to:

$$i_r = I_C \left[1 + \frac{v_{in} - v_{out}}{V_t} + \frac{(v_{in} - v_{out})^2}{2V_t^2} + \frac{(v_{in} - v_{out})^3}{6V_t^3} \right] \tag{III.5}$$

Substituting (III.2) for v_{out} we get:

$$\begin{aligned} i_r &= I_C \Bigg[1 + \frac{v_{in} - \Big(H_1(j\omega_a) \circ v_{in} + H_2(j\omega_a, j\omega_b) \circ v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3 \Big)}{V_t} \\ &+ \frac{\Big[v_{in} - \Big(H_1(j\omega_a) \circ v_{in} + H_2(j\omega_a, j\omega_b) \circ v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3 \Big) \Big]^2}{2V_t^2} \\ &+ \frac{\Big[v_{in} - \Big(H_1(j\omega_a) \circ v_{in} + H_2(j\omega_a, j\omega_b) \circ v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3 \Big) \Big]^3}{6V_t^3} \Bigg] \end{aligned} \tag{III.6}$$

If we group the first-order, second-order, and third-order terms, we have:

$$\begin{aligned} i_r &= I_C \left[1 + \frac{1 - H_1(j\omega_a)}{V_t} \right] \circ v_{in} \\ &+ I_C \left[\frac{(1 - H_1(j\omega_a))^2}{2V_t^2} - \frac{H_2(j\omega_a, j\omega_b)}{V_t} \right] \circ v_{in}^2 \\ &+ I_C \left[\frac{(1 - H_1(j\omega_a))^3}{6V_t^3} - \frac{\overline{(1 - H_1(j\omega_a)) H_2(j\omega_a, j\omega_b)}}{V_t^2} - \frac{H_3(j\omega_a, j\omega_b, j\omega_c)}{V_t} \right] \circ v_{in}^3 \end{aligned} \tag{III.7}$$

The current through the nonlinear base-emitter capacitance, i_c (see Fig. III.4), can be found by looking at the change in charge accumulated on the base-emitter capacitor with respect to time.

$$i_c = \frac{\partial}{\partial t} Q_{be} = \frac{\partial}{\partial t} \tau_F I_c = \tau_F \frac{\partial I_c}{\partial V_{be}} \frac{\partial V_{be}}{\partial t} \tag{III.8}$$

where τ_F is the forward transit time. So we can look separately at $\frac{\partial I_c}{\partial V_{be}}$ and $\frac{\partial V_{be}}{\partial t}$. We begin with $\frac{\partial I_c}{\partial V_{be}}$. As in (III.4), we have $I_c = I_C e^{V_{be}/V_t}$, and so since $V_{be} = v_{in} - v_{out}$:

$$\frac{\partial I_c}{\partial V_{be}} = \frac{I_C}{V_t} e^{(v_{in}-v_{out})/V_t} \tag{III.9}$$

Now we look at $\frac{\partial V_{be}}{\partial t}$.

$$\begin{aligned}
\frac{\partial V_{be}}{\partial t} &= \frac{\partial}{\partial t} V_{be} = \frac{\partial}{\partial t}(v_{in} - v_{out}) \\
&= \frac{\partial}{\partial t}\Big[v_{in} - [H_1(j\omega_a) \circ v_{in} + H_2(j\omega_a, j\omega_b) \circ v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3]\Big] \\
\frac{\partial V_{be}}{\partial t} &= j\omega_a(1 - H_1(j\omega_a)) \circ v_{in} - j(\omega_a + \omega_b) H_2(j\omega_a, j\omega_b) \circ v_{in}^2 \\
&\quad -j(\omega_a + \omega_b + \omega_c) H_3(j\omega_a, j\omega_b, j\omega_c) \circ v_{in}^3
\end{aligned} \tag{III.10}$$

From (III.8), the current through the base-emitter capacitance, i_c, is equal to $\tau_F \frac{\partial I_c}{\partial V_{be}} \frac{\partial V_{be}}{\partial t}$. Substituting the Taylor series for the exponential in (III.9), multiplying by (III.10) we have:

$$\begin{aligned}
i_c &= \frac{\tau_F I_C}{V_t}\Big[j\omega_a(1 - H_1(j\omega_a)) \circ v_{in} \\
&\quad +[j\omega_a(1 - H_1(j\omega_a))^2 - j(\omega_a + \omega_b) H_2(j\omega_a, j\omega_b)] \circ v_{in}^2 \\
&\quad +\Big(\frac{j\omega_a}{2V_t^2}(1 - H_1(j\omega_a))^3 - \frac{j(\omega_a + \omega_b)}{V_t}(1 - H_1(j\omega_a)) H_2(j\omega_a, j\omega_b) \\
&\quad -j(\omega_a + \omega_b + \omega_c) H_3(j\omega_a, j\omega_b, j\omega_c)\Big) \circ v_{in}^3\Big]
\end{aligned} \tag{III.11}$$

From (III.3) and Fig. III.4 , the only current remaining at the output is the current through the hold capacitor, i_o.

$$i_o = C_{hold} \frac{d}{dt} v_{out}$$

$$
\begin{aligned}
&= C_{hold}\Big[H_1(j\omega_a)\circ v_{in} + H_2(j\omega_a, j\omega_b)\circ v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c)\circ v_{in}^3\Big] \\
&= C_{hold}\Big[j\omega_a H_1(j\omega_a)\circ v_{in} + j(\omega_a+\omega_b)H_2(j\omega_a, j\omega_b)\circ v_{in}^2 \\
&\qquad + j(\omega_a+\omega_b+\omega_c)H_3(j\omega_a, j\omega_b, j\omega_c)\circ v_{in}^3\Big] \qquad \text{(III.12)}
\end{aligned}
$$

where C_{hold} is the hold capacitor. If we collect the first-order terms from i_r, i_c, and i_{out}, and solve $i_r + i_c = i_0$ (III.3) for $H_1(j\omega_a)$, we get:

$$
\begin{aligned}
\frac{I_C}{V_t}(1 - H_1(j\omega_a))\circ v_{in} + \frac{\tau_F I_C}{V_t}(j\omega_a(1 - H_1(j\omega_a))\circ v_{in} &= j\omega_a C_{hold} H_1(j\omega_a)\circ v_{in} \\
\frac{I_C}{V_t} - \frac{I_C}{V_t}H_1(j\omega_a) + \frac{\tau_F I_C j\omega_a}{V_t} + \frac{\tau_F I_C j\omega_a}{V_t}H_1(j\omega_a) &= j\omega_a C_{hold} H_1(j\omega_a) \\
H_1(j\omega_a)\left[j\omega_a C_{hold} + \frac{I_C}{V_t} + \frac{\tau_F I_C j\omega_a}{V_t}\right] &= \frac{I_C}{V_t} + \frac{\tau_F I_C j\omega_a}{V_t} \\
H_1(j\omega_a) = \frac{1 + j\omega_a\tau_F}{1 + j\omega_a(\tau_F + r_e C_{hold})} & \qquad \text{(III.13)}
\end{aligned}
$$

where $r_e = V_t/I_C$. The first order Volterra kernel below is identical to the behavior expected from the simplified model described in (III.1). Through similar analysis, we can find $H_2(\omega_a, \omega_b)$ and $H_3(j\omega_a, j\omega_b, j\omega_c)$.

$$
H_2(\omega_a, \omega_b) = \frac{[1 - H_1(j\omega_a)]^2(\frac{1}{2} + j\omega_a\tau_F)}{V_t[1 + j(\omega_a+\omega_b)(\tau_F + r_e C_{hold})]} \qquad \text{(III.14)}
$$

$$
H_3(j\omega_a, j\omega_b, j\omega_c) = \frac{(1 - H_1)^3(\frac{1}{6} + \frac{j\omega_a\tau_F}{2}) - (1 - H_1)H_2 V_t[1 + j(\omega')\tau_F]}{V_t^2(1 + j(\omega_a+\omega_b+\omega_c)(\tau_F + r_e C_{hold}))} \qquad \text{(III.15)}
$$

where $\omega' = \omega_a + \omega_b$ and $V_t = kT/q$. One cannot completely decouple the first and third-order Volterra kernels, since the third-order kernel contains the first and second-order kernel. However, we can focus our analysis on the Volterra kernels without calculating the harmonic distortion. Two very simple ideas are shown in (III.15). As $H_1(j\omega_a)$ goes

to unity, $H_3(j\omega_a, j\omega_b, j\omega_c)$ goes to zero. From (III.13), we see this will limit the size of the hold capacitor and determine the current bias of the SEF. After the current and hold capacitors are determined, it will bound the maximum frequency of operation. Graphically, we can see from Fig. III.4 and III.5 that when $H_1(j\omega_a)$ is close to unity, the third-order Volterra kernel will be minimized. The third-order intermodulation distortion is the ratio of third-order kernel to the first-order kernel described as follows:

$$IM_3 = \frac{3}{4}\frac{|H_3(\omega_a, \omega_b, \omega_c)|}{|H_1(\omega_a)|^3} \circ v_{in}^2 \tag{III.16}$$

Simple SPICE model simulations also confirm our results. An emitter-follower was simulated driving a capacitive load and the third-order intercept point was computed as a function of frequency. This is compared against the Volterra analysis and with similar results (see Fig. III.7). The Volterra analysis guided selection of appropriate values for the bias current and the hold capacitor, C_{hold}, to yield a suitable IM3 performance.

III.3 Experimental Results

The sample-and-hold was fabricated in $0.5\mu m$ SiGe/Ge BiCMOS process with an active area of $0.150mm^2$ while consuming 360mW in the THA core (see Fig. III.10). It was targeted to exist on die with a state-of-the-art ADC.

The performance was confirmed by several performance criteria. First, a single stage of the sample-and-hold was tested in track mode, to determine the track-mode distortion. Then, the sample-and-hold was tested in sub-sampling configuration to mea-

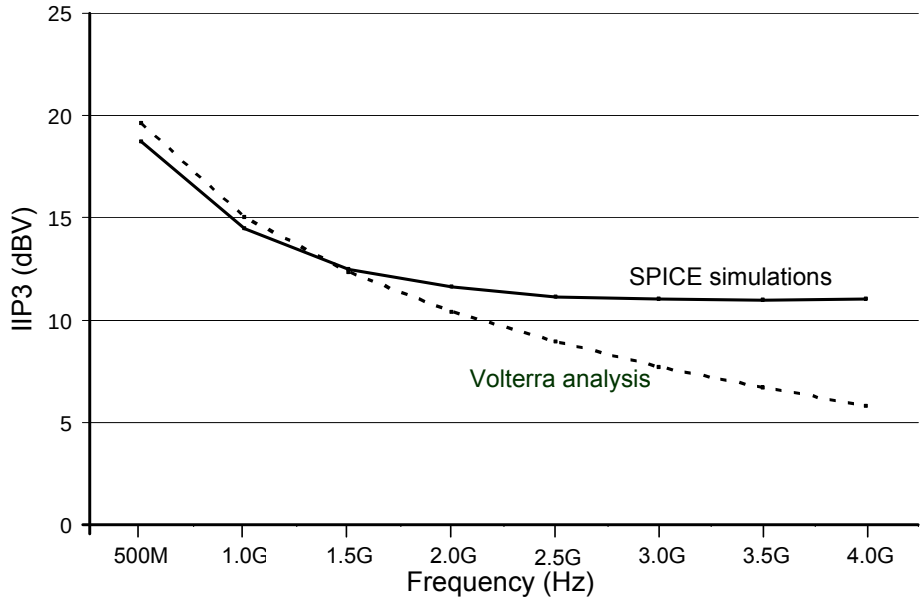

Figure III.7: Comparison of third-order intercept point using SPICE simulations and Volterra analysis ($C_{hold} = 500fF$, $I = 6mA$, and $\tau_F \approx 3.1ps$).

sure sampling distortion. Normally the SHA would be followed by an ADC that would be clocked at a short time before SHA transitions. The distortion would then be measured at discrete moments in time. Without the ability to sample the output the continuous SHA output is instead sub-sampled and feed into a spectrum analyzer. Thus, we are able to measure the performance of the SHA with the input and clock signals tested at full speed. The continuous time output signal contains more high frequency energy due to the transition times. The exact amount of extra energy in the transitions is impossible to quantify and discrete time measurement is preferred. However, an ADC with the resolution, clock speed and input bandwidth did not exist for our testing purposes, and we were limited to continuous time testing.

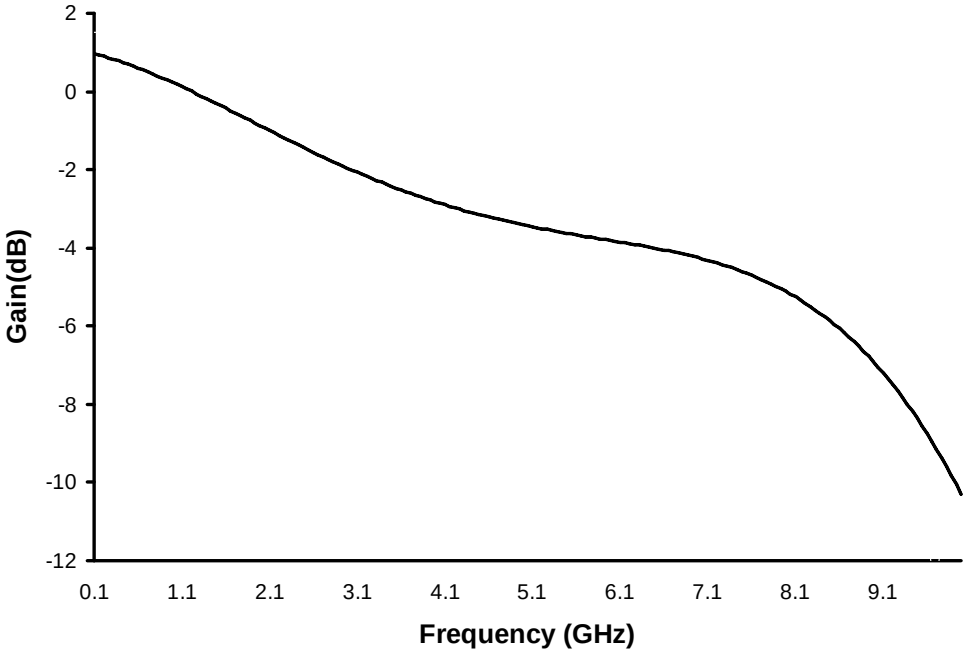

Figure III.8: Measured transfer function of single stage track and hold amplifier in the track mode.

The clock signals were buffered on chip and the output signals were also buffered to drive a 100Ω differential load. Fig. III.8 shows the transfer function of the THA in *track* mode. Imprecise matching as well as excessive ripple from the high frequency off-chip baluns used in testing contributed to ripple in the transfer function. The signal shown in III.8 has been averaged over 5 samples to observe the bandwidth more clearly.

A two-tone intermodulation test was performed first in the track-mode alone and then in the full sampling mode. The third-order intercept was computed to be greater than 26dBm with a dynamic range of greater than 46.2dB for almost all frequencies (see Fig. III.9)

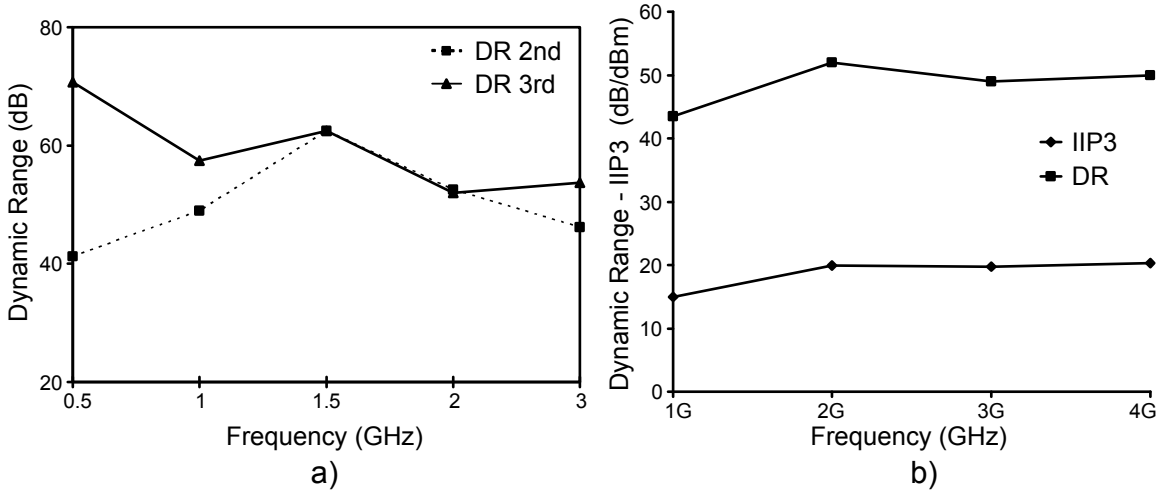

Figure III.9: a) Dynamic range of the second and third-order products during the track-mode measured as the difference between the fundamental and the second and third order distortion products. b) Measured IP_3 and dynamic range of SHA in sample-and-hold mode.

In full sampling mode, the dynamic range was greater than 43.5dB for up to 4GHz clock speed (see Fig.III.9).

III.4 Conclusions

An improved design has been presented for a sample-and-hold circuit achieving wider bandwidth and lower distortion than previous circuits implemented in silicon technology. You can see from the graph above (Fig. III.11) and the table at the beginning of this chapter (see Fig. III.1) that this sample-and-hold performed better than any other silicon bipolar, CMOS, or Si/SiGe sample-and-hold published to date. An optimized switched-emitter follower design was used to extend the performance to higher frequencies. The

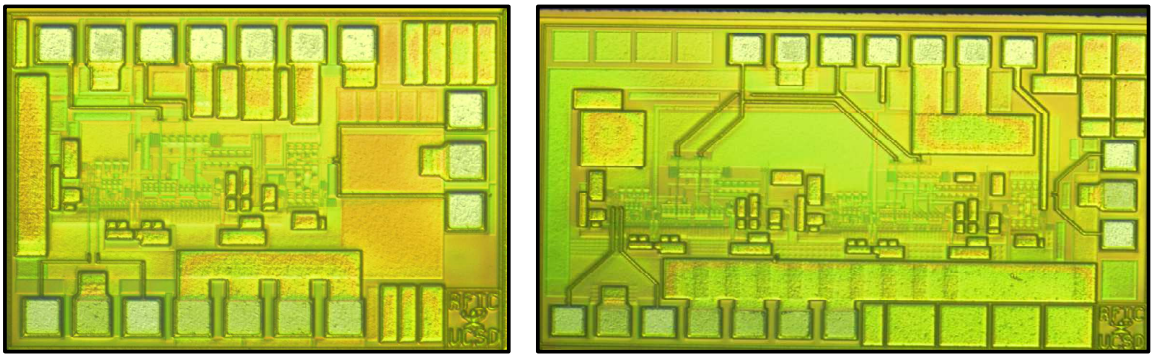

Figure III.10: a) Die-photo of single stage track-and-hold. b) Die photo of two-stage track-and-hold with anti-phase clock signals.

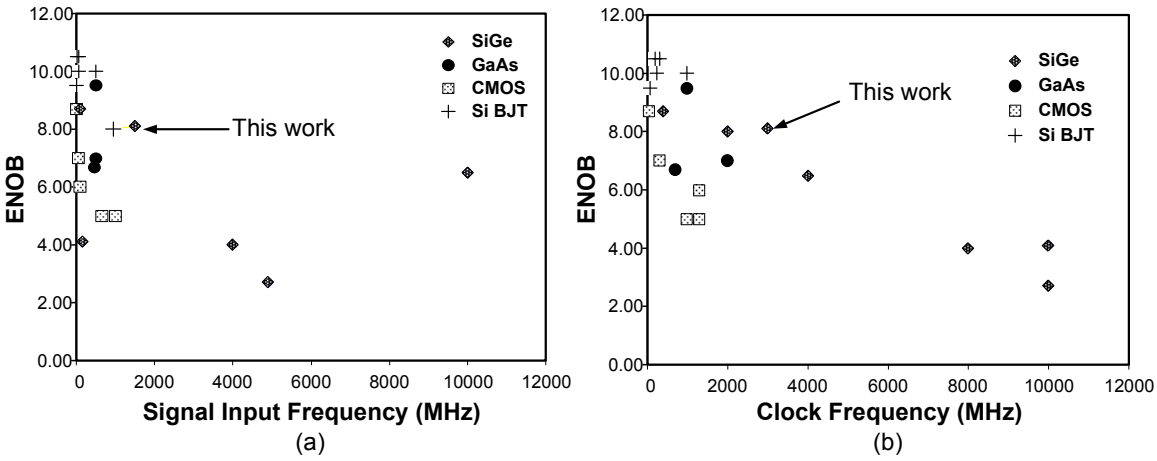

Figure III.11: Previously published SHA results: a) Effective number of bits (ENOB) versus input signal frequency. b) ENOB versus sampling frequency. [12, 17, 20–22, 25–38]

aspects of the sample-and-hold design that lead to distortion at high frequencies were analyzed, and improvements in the circuit implemented to minimized these effects. The circuit exhibited a track-mode bandwidth of 6GHz and 8bit dynamic range. It can be used as a building-block for next generation wide bandwidth communication systems.

Chapter IV

Comparator Design

IV.1 Introduction

In many converter architectures, the next step after the sample-and-hold to convert analog signals into quantized digital bits comes from the analog-to-digital converter, ADC. In the Introduction, we reviewed a few types of high speed converters [11, 12], all of which use a high-speed comparator to determine whether the input signal has surpassed or dropped below a reference voltage. In high-speed applications, the A/D converters typically have modest resolution requirements, but require extremely wide bandwidths (see Fig. IV.1). The comparator in these A/D converters plays a crucial role in the overall sample rate and resolution of the converter, and must be able to amplify and compare the incoming signal against the reference voltage at rates faster than 10GHz. Increasing the sampling speed and bandwidth while minimizing offsets presents many challenges to the designer.

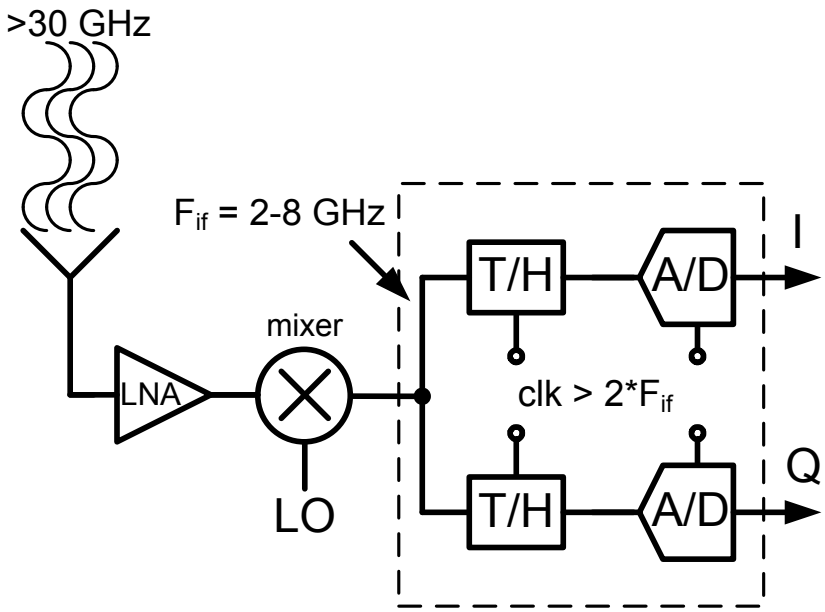

Figure IV.1: Millimeter-wave communications receivers will rely on IF sampling system architectures, requiring A/D converters operating in the multi-gigahertz frequency range.

This chapter presents an improved design approach to the traditional bipolar master-slave comparator [39–44, 81] to reduce the latch time and thus increase the overall clock speed of the comparator. The result is a design with a maximum clock rate that is much higher than traditional approaches.

IV.2 Comparator Architecture

IV.2.1 Review of Existing Comparator Approaches

A traditional latched comparator is shown in Fig. IV.2; when the *track* signal is high, the input v_{in} is amplified, and when the *latch* is high, the voltage difference at the

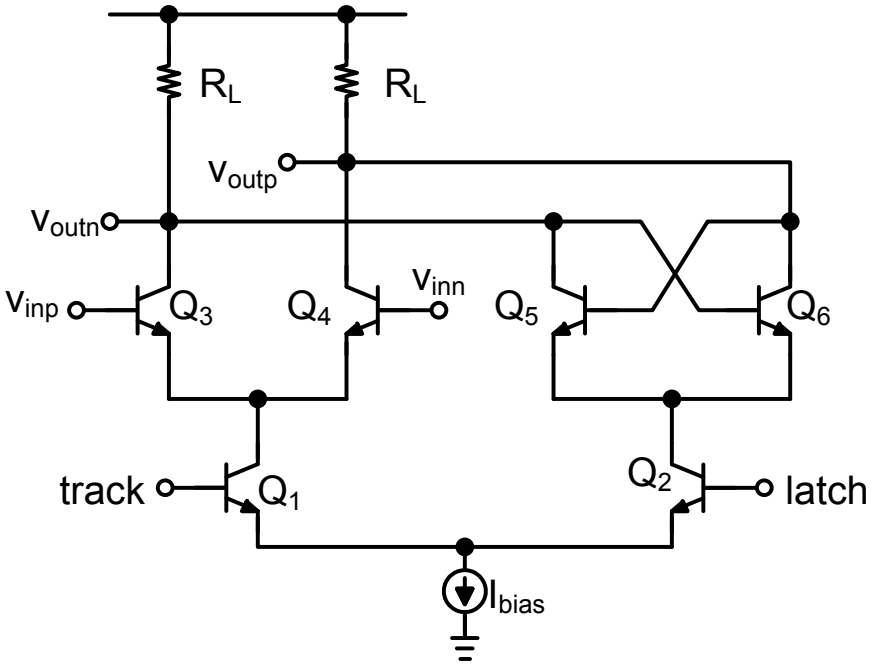

Figure IV.2: Traditional track-latch comparator design.

output will cause the positive feedback pair ($Q_5 - Q_6$) to latch, resulting in a digital output signal. One well-known limitation in this design comes at high speeds where significant "kick-back" can be detected at the input during the latch mode due to Q3-Q4 being suddenly shut-off. The kick-back, due to the back-injection of stored base-emitter charge into the base, can significantly distort the incoming signal and limit the performance of higher resolution converters.

A slight modification to this approach adds a current source in parallel with Q_1, which is always on, and will keep the input devices from turning off in the latch mode [44]. This will reduce the kick-back seen at the input. For low-power converters, this can help extend the operating frequency beyond initial limits; but further enhancements are

necessary if we wish to continue to extend the frequency of operation.

IV.2.2 Improved Comparator Design

An improvement to the previous design can be seen in Fig. IV.3, [39, 81]. Here a current-steering comparator is employed with the input devices (Q1-Q2) "always-on". The bias current, I_{bias}, is steered by the clock inputs either directly to the output in the *track* phase, or to a cross-coupled pair (Q7-Q8) in the *latch* phase. This design exhibits improved isolation between the digital output and the input compared to the standard design, at the expense of the increased headroom needed to accommodate the switching devices.

A key speed limitation of this improved design is that, when the latch phase is initiated, the base-emitter junctions of the latch, Q7-Q8, will need to turn-on and re-charge, with the re-charge current being provided by the bias current I_{bias}. At the absolute maximum clock rates, this junction charging time limits the maximum speed of the comparator.

During the track phase, with $I_1 = 0$, node @ would rise to approximately $V_{cc} - (I_{bias}/2 \cdot R_L)$. Once the comparator moves to the latch mode, this node must drop by $V_{be}|_{on}$. This $V_{be}|_{on}$ is added to the base-emitter voltage at the start of the latch phase, and extends the regeneration time of the latch. The change in voltage at node @ as a function of current is

$$\Delta V_{be} \approx V_T \cdot ln\left(\frac{I_{bias}}{I_s}\right) \tag{IV.1}$$

where I_{bias} is the bias current for the entire comparator, the thermal voltage, $V_t = 25.85mV$ and I_s is the saturation current.

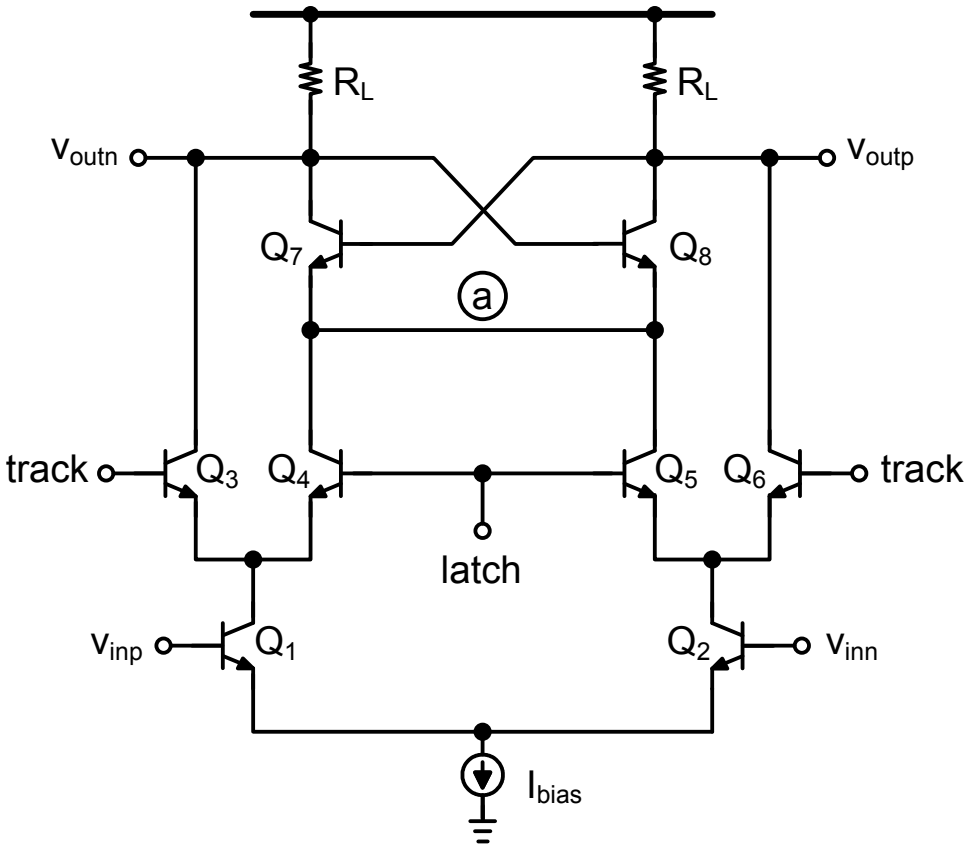

Figure IV.3: Comparator with current steering clock.

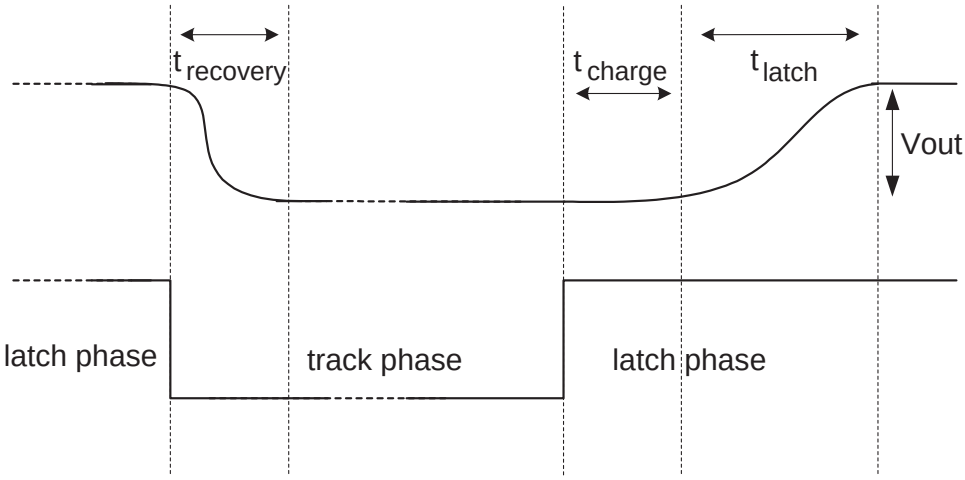

Figure IV.4: Delay times during track and latch transitions.

The total time for the latch to produce a digital signal once the latch mode is initiated is the regeneration time. As seen in Fig. IV.4, the total regeneration time of the latch is the device junction charging time plus the *latch-mode time constant* [44]. The junction charging time is the time required to charge the base-emitter junctions of the latch transistors. The latch-mode time constant is the time needed to switch the latch once the devices are *on*. For each device, the charging time can be approximated by

$$t_{charge} \approx \frac{C_{be}(V_{be})\Delta V_{be}}{I_{bias}/2} \tag{IV.2}$$

where $C_{be}(V_{be})$ is the voltage dependant base-emitter capacitance and ΔV_{be} is base-emitter voltage as described by (IV.1). The quantity t_{charge} is approximately 40 picoseconds for our latch transistor with $I_{bias} = 1.0mA$.

For the *latch-mode time constant* we start with a simplified model of the latches (see Fig. IV.5) and find a steady-state solution for the gain through the loop. Summing the

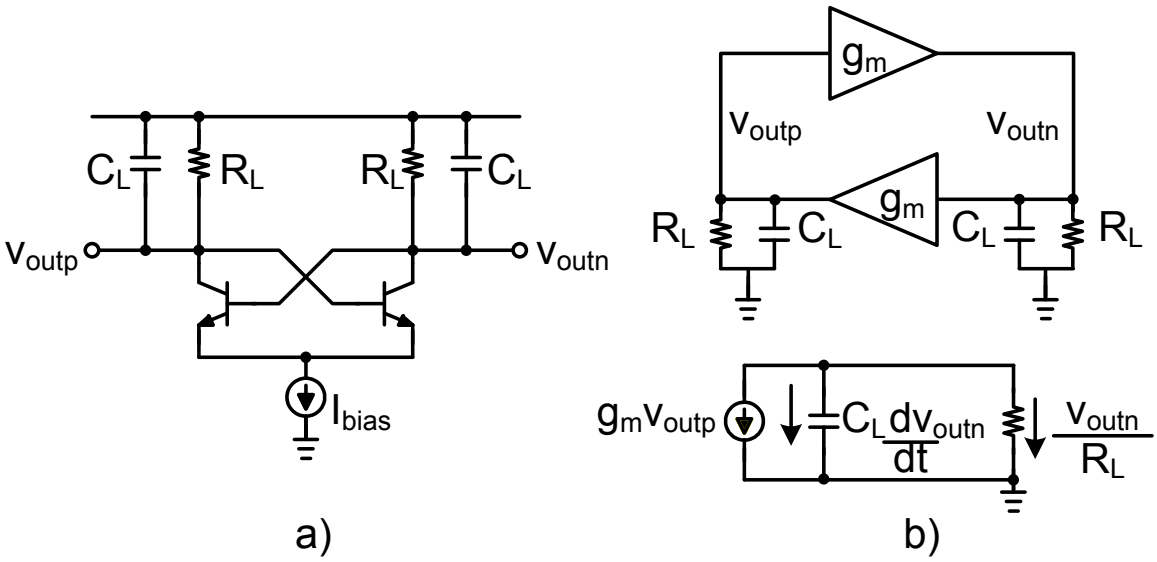

Figure IV.5: a) Comparator latch with parasitics. b) Ideal latch used for computing the *latch-mode time constant*.

currents at v_{outp} and v_{outn} and solving for the voltage difference $v_{outp} - v_{outn}$, we get

$$C_L R_L \frac{d(v_{outp} - v_{outn})}{dt} + v_{outp} - v_{outn} = A_L(v_{outp} - v_{outn}) \tag{IV.3}$$

where $A_L = g_m R_L$. If we let $v_{outp} - v_{outn} = \Delta V$ and $\tau = R_L C_L$, (IV.3) becomes

$$\begin{aligned} \tau \frac{d\Delta V}{dt} + \Delta V &= A_L \Delta V \\ \frac{d\Delta V}{dt} &= \Delta V \frac{A_L - 1}{\tau} \end{aligned} \tag{IV.4}$$

A steady-state solution for (IV.4) is

$$\Delta V = \Delta V_o e^{\frac{(A_L - 1)t_{latch}}{\tau}} \tag{IV.5}$$

where ΔV_o is the voltage difference presented to the latch at time $t = 0$. Solving (IV.5) for

the latch-mode time constant, t_{latch}, we get

$$\begin{aligned} t_{latch} &= \frac{\tau}{(A_L - 1)} \cdot ln\left(\frac{\Delta V_{final}}{\Delta V_0}\right) \\ &= \frac{C_L}{g_m} \cdot ln\left(\frac{\Delta V_{final}}{\Delta V_0}\right) \\ &\approx \frac{C_L V_T}{I_{bias}/2} \cdot ln\left(\frac{I_{bias} R_L}{\Delta V_0}\right) \end{aligned} \tag{IV.6a}$$

where ΔV_{final} is the desired final voltage of the latch. ΔV_{final} is reached when the comparator latch achieves its maximum output swing, i.e. $\Delta V_{out} = I_{bias} * R_L$. Here, t_{latch} goes to infinity when the voltage difference is zero. Thus, an extremely small input signal will lead to an extremely long latch time. However, the system requirements of the converter are usually specified to resolve only those signals greater than a half of an LSB. Only signal levels above this magnitude need concern us, and thus the worst case latch time from (IV.6) becomes

$$t_{latch}|_{lsb} = \frac{C_L V_T}{I_{bias}/2} \cdot ln\left(\frac{4V_T}{A_{pre} LSB}\right) \tag{IV.7}$$

The quantity $t_{latch}|_{lsb}$ is computed for ΔV_0 equal to $A_c A_{pre} \cdot LSB/2$, where A_c is the gain of the comparator ($R_L g_m$) and A_{pre} is the gain of any pre-amplification before the comparator. The result shows that gain before the comparator helps reduce the latch time by presenting a larger signal to the latch, at the expense of a reduction in bandwidth, increased input offset, and an increase in power consumption. The recovery time reduces linearly with bias current and logarithmically with least-significant-bit and pre-amplification. Increasing the bias current will have the largest effect on the worst case latch time of the comparator.

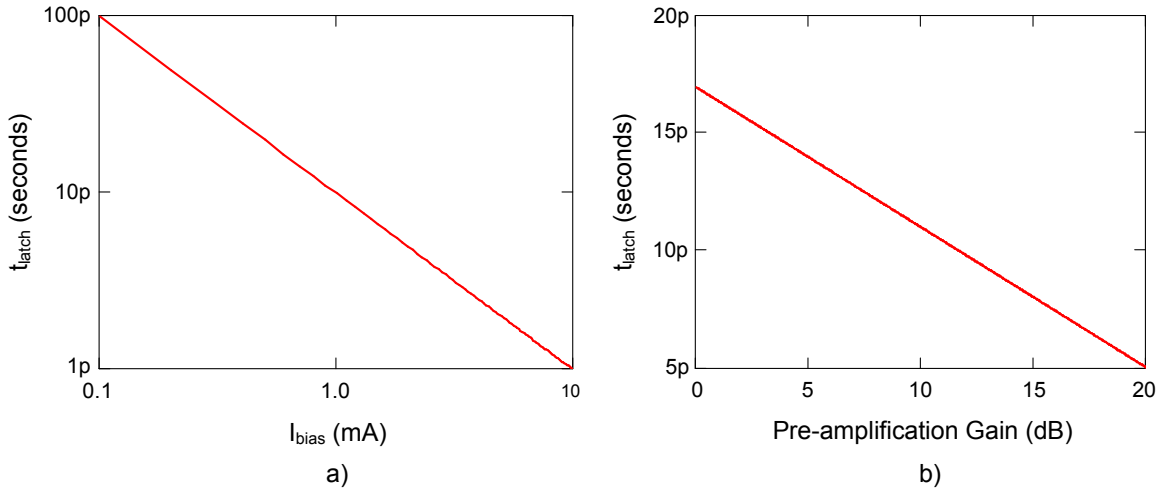

Figure IV.6: a) Worst case latch time versus bias current for 8bit resolution, where $C_L = 100fF$ and $A_{pre} = 4$. b) Worst case latch time versus pre-amplification for 8bit resolution, where $C_L = 100fF$ and $I_{bias} = 1mA$. (see (IV.7))

Figures IV.6 a) and b) show the effect of bias current and pre-amplification on the latch time constant.

Another common limitation of the comparator design is the *recovery time*. During the transition from the latch phase to the track phase, the time the differential output voltage takes to go from a full digital swing to zero when presented with an input voltage of $-LSB/2$, is the recovery time. Summing the currents at the output, the recovery time can be written as

$$t_{rec} = R_L C_L ln\left(1 + \frac{1}{tanh(\Delta V_0/2V_T)}\right) \tag{IV.8}$$

Where R_L is the load resistor and C_L is the total capacitance at the output node

of the comparator, and ΔV_0 is the voltage difference presented to the latch at time $t = 0$. For our design t_{rec} is approximately 12 picoseconds. Maintaining a large signal bandwidth is important to reducing the recovery time and improving maximum clock rate of the comparator. For low-power comparators the recovery time can be much longer than the regeneration time, due to the larger output time constants [81,82]. We were concerned with accommodating ultra-wide bandwidth input signals that lead to a short recovery time.

IV.2.3 Cascode Comparator

Another variation of the comparator that can help extend the usable bandwidth is a cascode design (see Fig.IV.7) [81]. In this topology, the comparator load is replaced with a cascode load. The currents of the input amplifier and latch are directed through the low impedance cascode devices. This helps extend the bandwidth of the comparator at the cost of more headroom. A drawback of the cascode architecture is that the latch gain is unity and must be increased for the core to latch.

One way this can be overcome is by placing resistors at the load of the latch and input devices (see Fig.IV.8). In this schematic, the gain was increased in both the track and latch phase independently. R_1 will increase the gain of both the track and latch phase and R_2 will increase the gain during the latch phase only. With the cascode design, the output digital swing can be adjusted separate from the gain of either the *track* or the *latch* phase. So the output swing can be optimized to drive the following stages while R_1 and R_2 can be adjusted for optimum signal bandwidth (t_{rec}) and latch speed (t_{latch}).

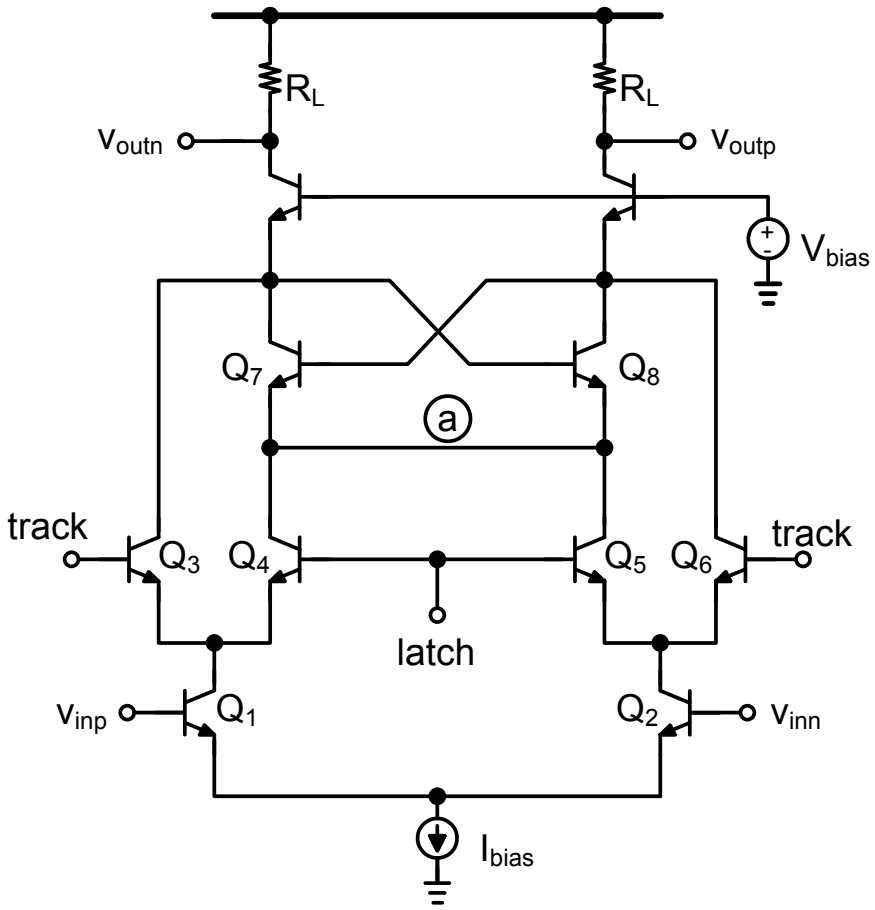

Figure IV.7: Improved Comparator design with cascode load.

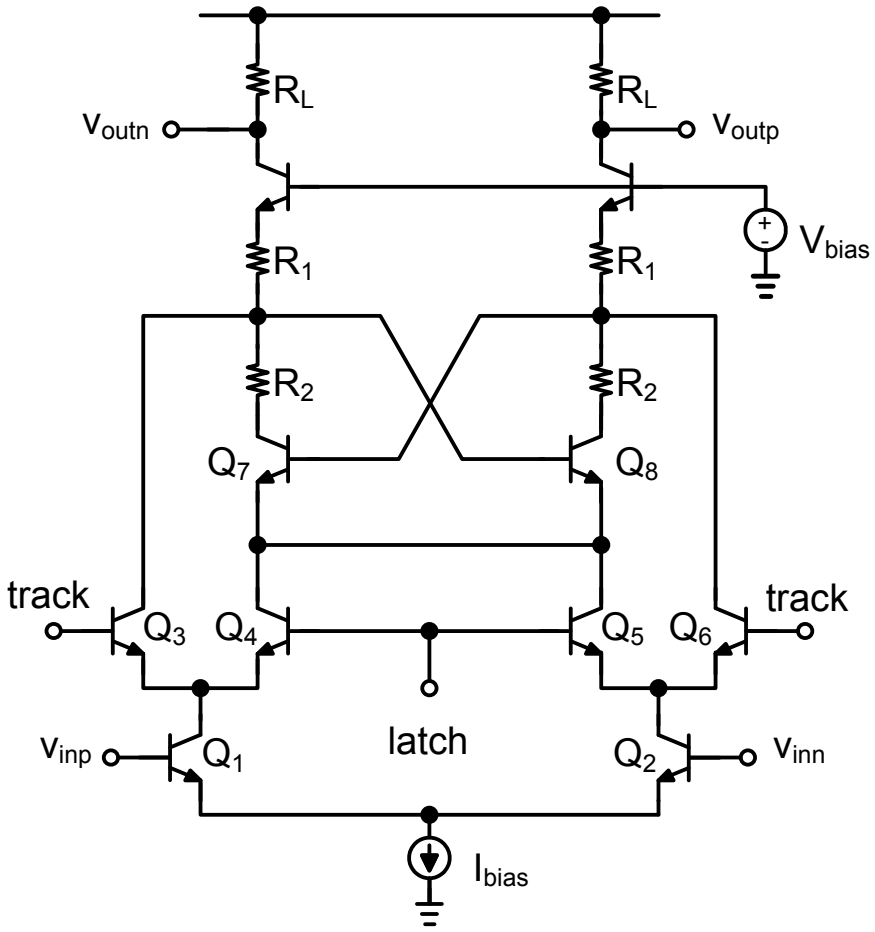

Figure IV.8: Improved comparator design with cascode load and increased track-mode and latch-mode gain.

Unfortunately, the gain-bandwidth product is constant, and as we increase the gain, the bandwidth decreases. One must consider whether the reduction of headroom is worth a marginal increase in bandwidth.

IV.2.4 Further Improvements to the Comparator

In an effort to reduce the latch-mode time constant, current source I_1 is added to keep the latch transistors from completely turning "off" (see Fig. IV.9). If Q7-Q8 remains partially "on" during the *track* phase of operation, less time is required to fully charge the base-emitter junctions during the *latch* phase, and the overall speed is improved. This small change to the master-slave latch has a profound effect on the overall speed of the comparator.

The time to charge the base-emitter junction, from (IV.2), now becomes

$$t_{charge} \approx \frac{C_{be}(V_{be})\,(V_{be,final} - V_{be,initial})}{I_{bias}/2} \tag{IV.9}$$

The results of (IV.9) are plotted in Fig. IV.10. With I_1 present, the base-emitter junction is pre-charged, significantly reducing t_{charge} to approximately 7 picoseconds from approximately 22 picoseconds.

A small current maintained through the latch devices during the track phase will be steered to the output by the voltage difference at the load. This "keep-alive" current adds a small, signal-dependent offset to the input of the latch *before* the decision is made. It is important to keep this offset small and to provide adequate gain before the comparator to limit its effect. Thus, there is a fundamental tradeoff between the hysteresis introduced by

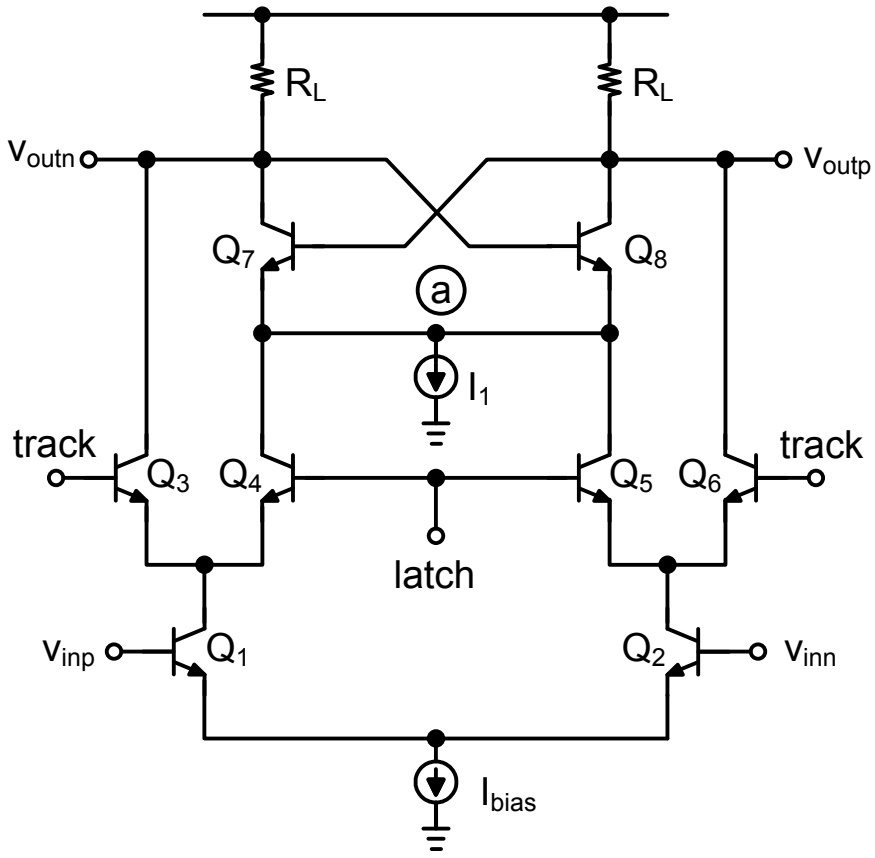

Figure IV.9: Improved comparator design with “keep-alive” current source.

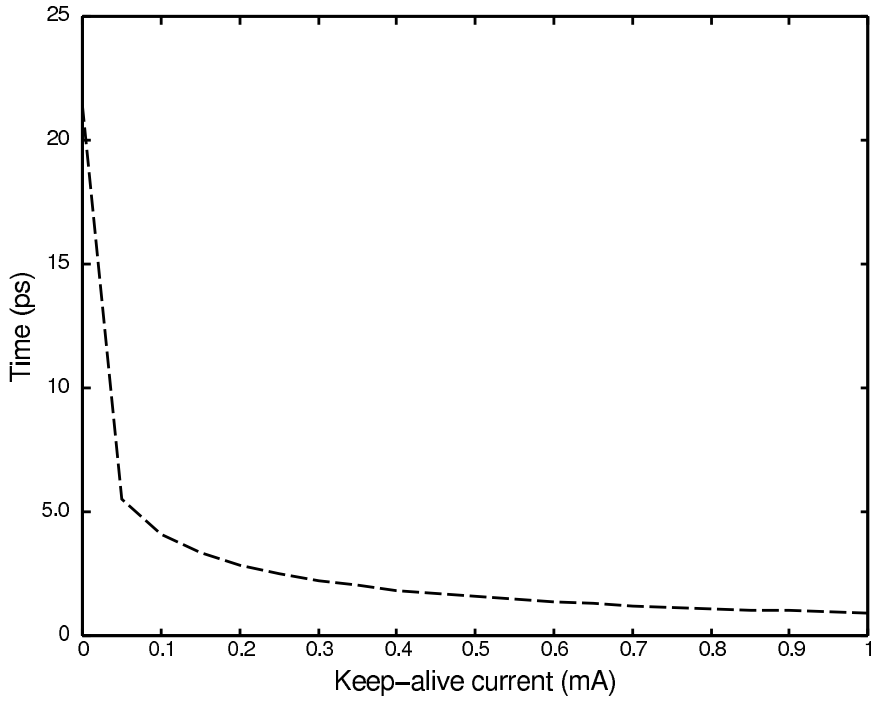

Figure IV.10: Predicted variation of t_{charge} in the latch mode with current I_1 from (IV.9) where the f_T of the device was near 50GHz and with a load resistor of 100Ω.

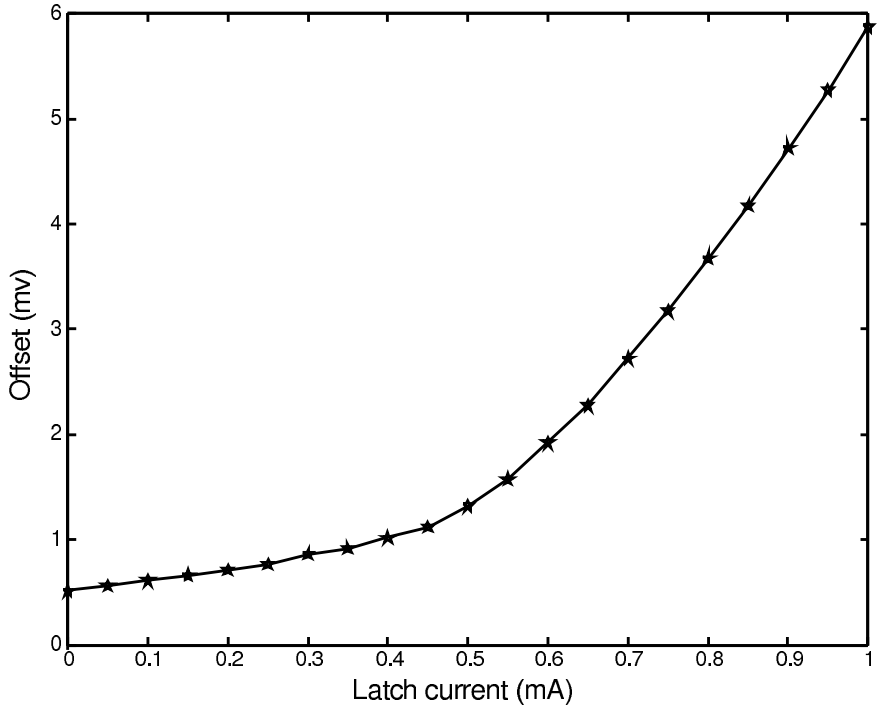

Figure IV.11: Input referred offset at comparison point with respect to keep-alive current.

the keep-alive current and the maximum switching speed and must be carefully assessed by the designer.

As long as I_1 is small during the track phase, the gain of the latch ($g_{m7} \cdot R_L$) will be less than unity and the "keep-alive current" in the latch will increase the overall small-signal gain of the comparator. The small-signal gain peaks when $g_{m7} = 1/R_L$. However, once I_1 exceeds $2V_T/R_L$ during the track phase, the negative conductance of the latch will be greater than $1/R_L$, and all of I_1 will switch to one side of the amplifier output. The maximum hysteresis of the latch will therefore be $I_1 \cdot R_L$.

In this case, $I_1 \cdot R_L$ will be added to, or subtracted from, the input during the track phase, depending on the previous decision of the latch. It might be desired to operate

the comparator in this region, and the values of R_L and I_1 should be adjusted such that the voltage offset is kept below $A_{pre}A_0 \cdot LSB/2$. The improved sampling speed may prove to be more important than the voltage offset created by the latch. This offset will increase with I_1 and eventually may grow larger than the input to the comparator. At this point the comparator will cease to function correctly and the output of the latch will remain in one logic state with the input never able to overcome the offset and trip the latch. Fig. IV.11 shows the simulated induced offset of the latch with respect to I_1.

IV.3 Analysis of Performance of the Improved Design

IV.3.1 Comparator Meta-stability

The comparator will be presented with signals so small that no decision is determined during the latch period. These signals are called "meta-stable"; they are not truly unstable, since provided enough time, the latch will eventually "trip." The probability of meta-stable occurrence must be limited or the effective number of bits will be reduced. Previous work [39, 83] has shown the probability of an occurrence of a meta-stable point after decision time t_d has elapsed, is

$$P(t > t_d) = exp\Big(-\frac{A_{latch} - 1}{\tau} t_d\Big) \tag{IV.10}$$

where τ is the RC time constant of the latch, t_d is the time allowed for a decision, and A_{latch} is the open-loop latch-gain. Normally for symmetric clocking, and ignoring the latch charging time, t_d will equal $t_s/2$ where $t_s = 1/f_s$, and f_s is the sampling speed of

the comparator. But as we saw in Fig. IV.4, part of each clock period is occupied by the charging time. The true time allowed for a decision becomes $t_d = t_s/2 - t_{charge}$. As the "keep-alive" current is increased, the charge time, t_{charge}, reduces, allowing more time for the comparator to yield a decision, reducing the occurrence of meta-stable points. For sample rate, f_s, the probable number of meta-stable states per second can be computed from (IV.10) yielding

$$M_n = f_s exp\Big(-\frac{A_{latch} - 1}{\tau}\left(t_s/2 - t_{charge}\right)\Big) \tag{IV.11}$$

As I_1 increases, the charge time reduces quickly; and thus the number of meta-stable points per second dramatically reduces.

The technique that we have employed here reduces the occurrence of meta-stable points, since the decision making time can be substantially decreased if the base-emitter junction of the latch is pre-charged. From the input buffer to the output of the comparator, there should be enough gain to minimize instability and overcome the hysteresis produced by the keep-alive current without dramatic reduction in bandwidth. The gain of the input buffer is approximately 12dB (see Fig. IV.12) and there is another 5dB of gain during the track phase of the comparator. For I_1 equal to $100\mu A$, the input referred offset would be approximately 1mV. This is less than the predicted 1σ input referred transistor mismatches of both the comparator and input buffer.

A wide signal bandwidth will help reduce the tendency for meta-stability by maintaining signal amplitude at high frequencies. (IV.11) shows that the number of meta-stable states is directly related to the unity-gain-bandwidth of the comparator [39]. To

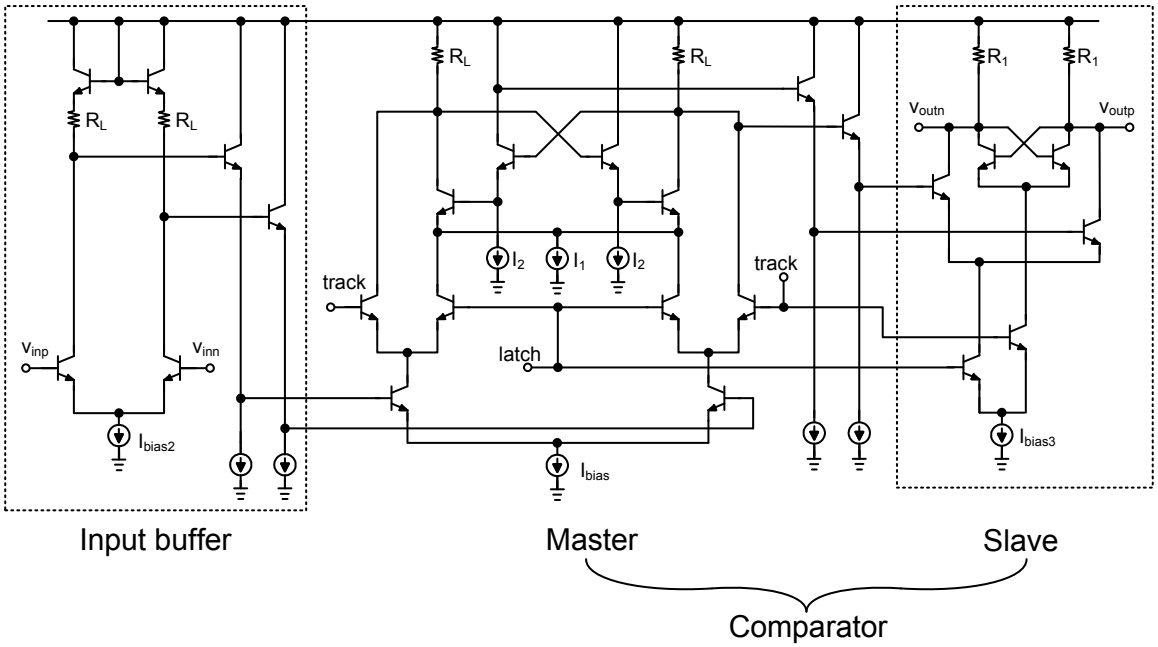

Figure IV.12: Input buffer, master and slave comparators

extend the unity-gain-bandwidth to its maximum, we used a pair of emitter-followers (Q5-Q6) within the loop to reduce the load capacitance (see Fig. IV.12).

The master comparator is followed by a similar latching core with anti-phase clock to further reduce meta-stable states (see Fig. IV.12). This second stage, the slave comparator, helps reduce meta-stable states by providing additional gain to the signal path. And, where the second stage of the sample-and-hold amplifier described in the previous chapter provides a held signal for the full clock cycle, the slave comparator provides a complete digital result for the full clock cycle.

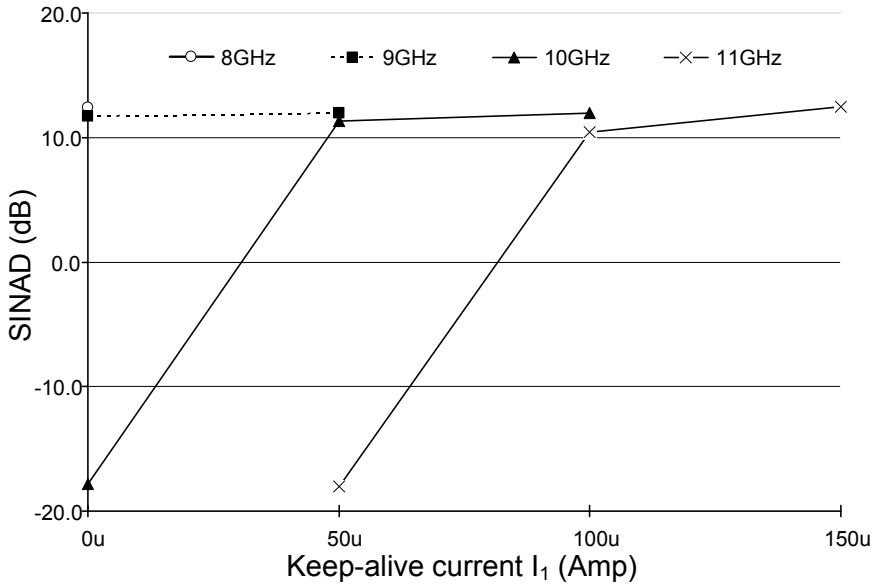

Figure IV.13: The comparator performance naturally degrades with increasing operating frequency. With a "keep-alive" device, the limit of operation is extended.

IV.4 Experimental Results

The design was fabricated in IBM's $0.5\mu m$ Si/SiGe BiCMOS process. The active area was $480\mu m$ x $200\mu m$ and the comparator consumes approximately 80mW with an additional 141mW consumed in the clock and output buffers used in the test chip. The circuit performance was confirmed using high frequency wafer probes. See Fig. IV.16 for a die photo.

Input and clock signals were both differentially matched to 50 ohms. Ultra-broadband off-chip baluns were used to bring the signals on and off chip. The input signal was sub-sampled with the input frequency 40MHz higher than the clock frequency. The digital output signal was processed with a logic analyzer state machine clocked at one and

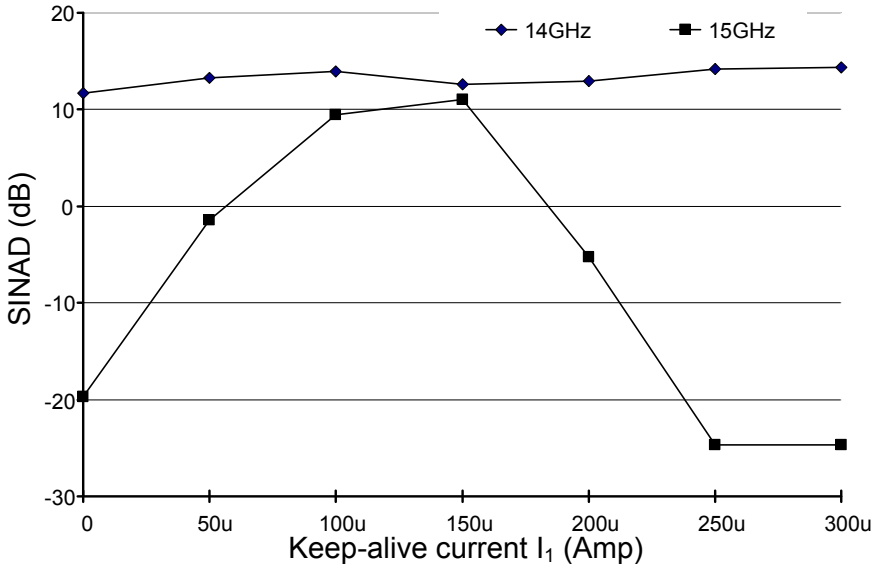

Figure IV.14: Extending the frequency of operation. With a small “keep-alive” device the comparator will function beyond existing limits until increasing offset voltage overwhelm the signal.

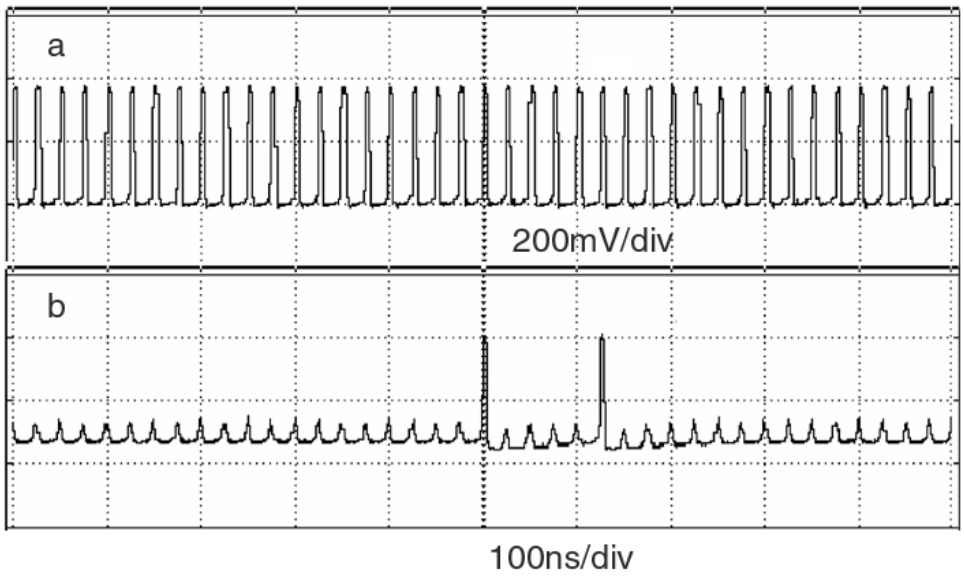

Figure IV.15: 16.04GHz sub-sampled comparator output. a)The "keep-alive" current is $100\mu A$, base-emitter diode pre-charged, and latch functions properly. b)The "keep-alive" current is turned off and the comparator is unable to operate.

a half times the Nyquist rate (just below the maximum rate of the logic analyzer.)

Fig. IV.13 shows the operating of the comparator with an input power of $-23dBm$. The comparator performance, shown as the signal-to-noise and distortion, degrades slightly at 9GHz and stops functioning completely at 10GHz when the latch remains off in the track phase. But, at 10GHz, when a small "keep-alive" current biases the latch, the comparator works again. And at 11GHz, the comparator does not function with zero or $50\mu A$ biasing the latch. But when the $100\mu A$ biases the latch, the comparator again functions as predicted. And if $150\mu A$ passed through the latch, even better performance is seem.

With a larger input signal, the comparator will operate with a clock frequency of

14GHz without the latch biased in the track phase. At 15GHz, the comparator ceases to operate, until the small "keep-alive" current biases the latch (see Fig. IV.14). You can also see that the performance degrades as the "keep-alive" current increases due to the offsets introduced to the input of the latch.

Using the timing function of the logic analyzer, the comparator is clocked at 16GHz with an input signal of 16.04GHz. With an input voltage of $20mV$ and I_1 turned off, the comparator is unable to function (see Fig. IV.15 b). By increasing the "keep-alive" current to $100\mu A$, the emitter-base junction of the latch is pre-charged and the comparator functions properly (see Fig. IV.15a). This shows the maximum operating frequency of the comparator is extended if the latch is kept partially on during the track phase.

IV.5 Conclusions

A high speed comparator has been designed and fabricated with a clock speed in excess of 16GHz. A "keep-alive" device is used to reduce the latch regeneration time and extend the frequency of operation. The nearby table shows the performance of this comparator being clearly superior to previously published work.

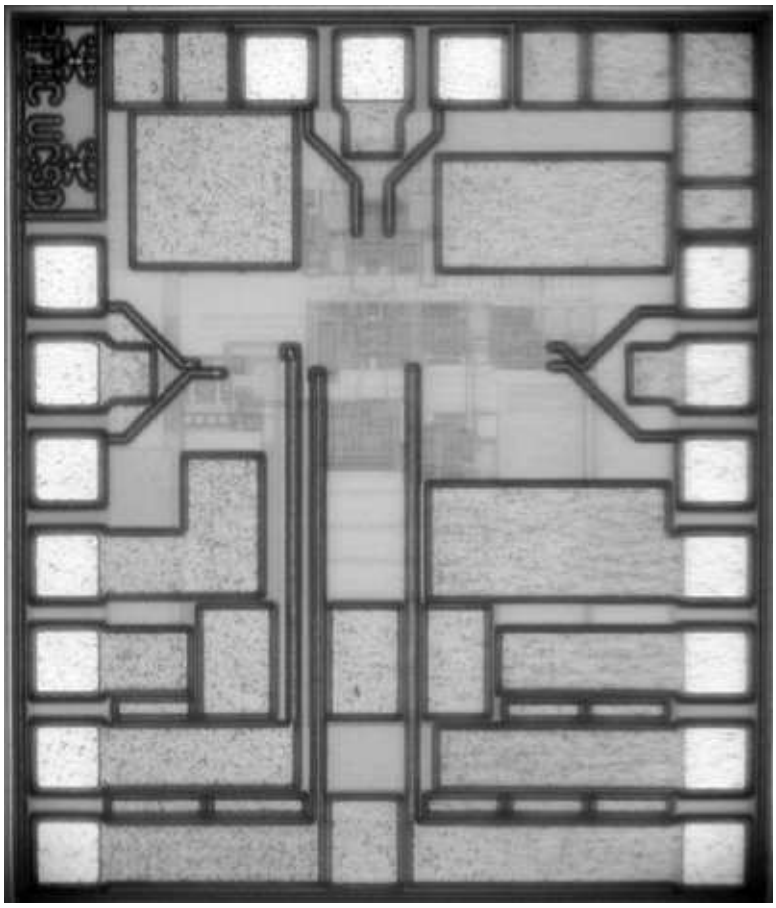

Figure IV.16: Die Photo, SiGe HBT Comparator.

Table IV.1: Overview of high-speed comparator performance

ref #	*Fs*	*Fin*	*Process*
this work	16GHz	16GHz	SiGe HBT
[84]	10GHz	4.9GHz	SiGe HBT
[85]	8GHz	8GHz	GaAs
[70]	5GHz	900MHz	SiGe HBT
[86]	4GHz	4GHz	SiGe HBT
[87]	200MHz		Si-Bipolar

Chapter V

Conclusion

The demand for mobile technology products has exploded over the last two decades. The Semiconductor Industry Association (SIA) issued a forecast in June of 2005 projecting that worldwide sales of semiconductors will grow by 6 percent in 2005 to a record $226 billion, and sales are projected to reach $309 billion by 2008. The Bureau of Labor Statistics reports that the semiconductor industry employs a domestic workforce of approximately 226,000. The number of people and the amount of sales from the semiconductor industry is truly remarkable and continues to grow.

V.1 SiGe HBT BiCMOS Process

Propelling the incredible growth in semiconductor sales over last two decades has been phenomenal advances in process technology. Radio frequency and millimeter-wave circuits require transistor technologies whose f_T exceeds 50GHz. In the quest to ac-

commodate ultra-high frequency signals and switching circuits, a myriad of technological processes are available. Silicon CMOS, silicon-bipolar, hetero-junction bipolar, gallium-arsenide, and indium-phosphide have each grown their one niche market. For bipolar transistors, and especially the hetero-junction bipolar transistor, the substantial payoff in bandwidth and power savings has produced an ideal technology for high frequency mixed-signal circuits.

V.2 Sample-and-hold architectures

High frequency sub-sampling analog-to-digital converters require SHA circuits with extremely wide signal bandwidths. This dissertation presented improved circuit design techniques to minimize errors and demonstrated the performance of a diode-bridge track-and-hold with an input bandwidth greater than 10 GHz and a IIP3 of 26 dBm at 8.05 GHz implemented in a production Si/SiGe BiCMOS technology. The sampling rate of this circuit at the required dynamic range is superior to other THA's in silicon technology, and is comparable to state-of-the-art GaAs-based circuits. The aspects of the track-and-hold design that lead to distortion at high frequencies were analyzed, and improvements in the circuit implemented to minimized these effects.

This dissertation also presented a sample-and-hold circuit for Nyquist and over-sampling analog-to-digital converters. The analysis of a switched-emitter-follower based SHA, along with improved circuit design techniques to minimize these errors was shown. The bandwidth and dynamic range of this circuit at the required sample rate was superior

to other SHA's in silicon technology. An optimized switched-emitter follower design was used, the performance of the track-and-hold was analyzed, and improvements in the circuit implemented to minimized these effects. This circuit can be used as a building-block for next generation wide bandwidth satellite communication systems.

V.3 Comparator

Advanced analog-to-digital converters typically have modest resolution requirements, but extremely wide bandwidth requirements. The comparator in these A/D converters is critical to extend the sample rate of the converter, and must be able to amplify and compare at rates greater than 10GHz. This dissertation presented an improved design approach to the traditional bipolar master-slave comparator to reduce the latch time and thus increase the overall clock speed of the comparator. A "keep-alive" device is used to reduce the latch regeneration time and extend the frequency of operation, resulting in a design with a maximum clock rate in excess of 16GHz.

V.4 Future Directions

The creation of advanced systems starts with the design of start-of-the-art building blocks. This dissertation encompasses the design of several building blocks used in ultra-high speed analog-to-digital converters and I am confident this work has done its part to advance the state of the art.

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