Proceedings of the 38th Applied Power Electronics Conference and Exposition (APEC 2023), Orlando, FL, USA, 19-23 March, 2023

A Regulated Cascaded Hybrid Switched-Capacitor Converter with Soft-Charging and Zero Voltage Switching for 48-to-12-V Applications

T. Ge
Y. Zhu
R. C. N. Pilawa-Podgurski

A Regulated Cascaded Hybrid Switched-Capacitor Converter with Soft-Charging and Zero Voltage Switching for 48-to-12-V Applications

Ting Ge, Yicheng Zhu, and Robert C.N. Pilawa-Podgurski
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Email: {gting, yczhu, pilawa}@berkeley.edu

***Abstract*—The cascaded resonant switched-capacitor converter is an energy-efficient and power-dense solution to unregulated 48-to-12-V power conversion. This work explores approaches to achieve output voltage regulation with this topology while maintaining high efficiency and high power density. The two switch nodes at the second stage are merged into one for the automatic balancing of capacitor voltages. A hybrid resonant-PWM control method is presented to realize soft charging of the middle capacitor and flying capacitors. At 12-V fixed output voltage, it achieves a power density of 3115 W/in^3, a peak efficiency of 99.0% with 48-V input and 98.6% with 54-V input (including gate drive loss), both of which are among the best in the state-of-the-art regulated 48-to-12-V solutions.**

***Keywords*—hybrid switched-capacitor converter, cascaded converter, soft charging, zero-voltage switching**

I. Introduction

Intermediate bus converters (IBC) are widely used in 48-V power distribution systems such as data centers, communication base stations, and electric vehicles. To power low-voltage devices in the system (e.g., CPU, GPU, and memory), a two-stage architecture is usually adopted, including an unregulated 48-to-12-V IBC as the first stage and a multi-phase buck converter as the second stage [1]. Note that there are also 12-V loads in the system (e.g., CPU fan, hard disk drive, automotive battery, etc.), which require the IBC to provide a regulated 12 V voltage. In this paper, a cascaded hybrid switched-capacitor (SC) converter is presented for regulated 48-to-12-V conversion with improved power density and efficiency.

The proposed regulated converter topology originates from a fixed-ratio resonant SC converter, called the cascaded resonant converter [2], [3], which features a good balance between switch stress and passive component utilization, and has achieved outstanding performance for unregulated 48-to-12-V conversion. As shown in Fig. 1(a), two 2-to-1 resonant SC converters using small inductors are cascaded to achieve an overall 4-to-1 fixed conversion ratio. An important feature of this converter is that it only requires a small middle capacitor C_{mid}, since the second stage has interleaving operation and C_{mid} sees a reduced current ripple.

When the inductance of the cascaded resonant converter in Fig. 1(a) is increased, PWM control can be used to meet the regulation requirement. Since the flying capacitor takes on the majority of the voltage step-down burden (4-to-1), the output inductor sees smaller volt-second and the inductor size can be reduced significantly, compared to more traditional topologies. Compared with the conventional buck converter with a large output inductor, this converter can achieve almost zero current ripple of the output inductor at 48-to-12-V conversion and 7× smaller volt-second at 54-to-12-V conversion. Compared with the three-level buck converter [4] and series-capacitor buck converter [5], this converter achieves 5× smaller volt-second of the output inductor.

Although the original topology Fig. 1(a) has regulation capability, some practical problems need to be addressed. The first challenge is to balance the capacitor voltage at the scenario of small duty ratio (< 0.5) and small C_{mid}. The switch-node voltages in Fig. 1(a) are not naturally balanced at heavy load due to the voltage ripple on v_{Cmid}. An active voltage-balancing control can be adopted to eliminate voltage imbalance but it comes at a cost of increased circuit complexity [4], [6]–[9]. A contribution of this work is to develop a naturally-voltage-balanced variant of the cascaded resonant converter, without adding an active voltage-balancing control. The switch nodes $sw1$ and $sw2$ are shorted together as one switch node sw in Fig. 1(b) to balance the flying-capacitor voltages as well as the switch-node voltage over the entire load range, using a small C_{mid}. The detailed operation principle is presented in Section II-A. After merging the switch nodes, the next challenge is how to realize soft charging for all capacitors. A hybrid resonant-PWM operation mode is then proposed to address the hard-charging issue in Section II-B.

II. Operation Principle

A. Merged Switch Node for Automatic Voltage Balancing

As discussed above, the inductors L_1, L_{21}, and L_{22} in Fig. 1(a) need to be increased to realize regulation capability. The switch-node voltages v_{sw1} and v_{sw2} are not naturally balanced as shown in Fig. 2, which can be seen by the inequal pulse heights in circuit states 1 and 2. This causes higher voltage stress on the switches and larger inductor current ripple than the ideal balanced condition. The main reason behind the voltage imbalance is the voltage ripple on the second-stage input v_{Cmid}, and it is a common issue for flying-capacitor multilevel converters, with relevant discussion provided in [8], [10]–[13]. When the middle capacitor C_{mid} is sufficiently

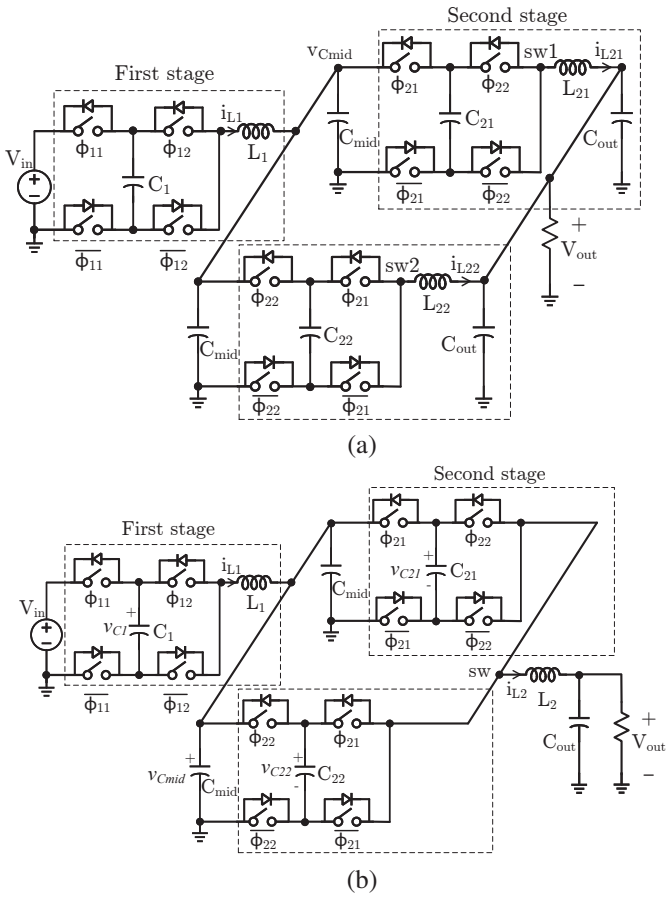

Fig. 1: (a) Conventional cascaded resonant converter and (b) proposed cascaded hybrid converter with voltage self-balancing, soft charging, and regulation capability.

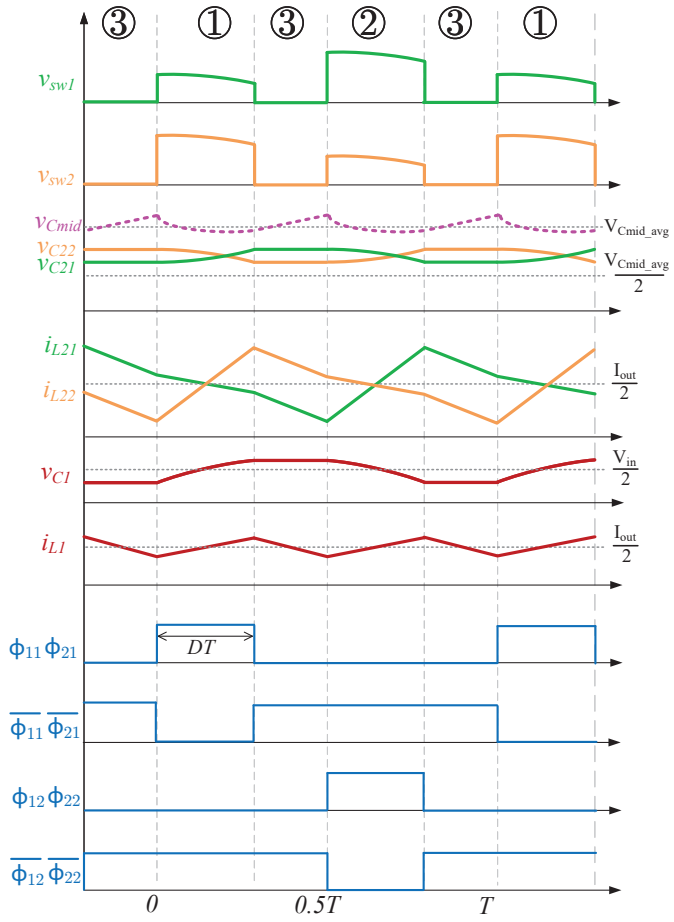

Fig. 2: Key waveform of the topology in Fig. 1(a) when both stages are operating in PWM mode.

large with a stiff v_{Cmid}, the voltages across C_{21} and C_{22} are balanced and equal to $\frac{V_{Cmid\_avg}}{2}$. However, in practice, a small C_{mid} is usually preferred for higher power density, resulting in a high voltage ripple on v_{Cmid}. The capacitors C_{21} and C_{22} then are overcharged during states 1 and 2, and their average voltages deviate from the nominal value, $\frac{V_{Cmid\_avg}}{2}$. As the capacitor C_{mid} becomes smaller and load current increases, the voltage ripple of v_{Cmid} increases, and the voltage imbalance gets worse as shown in Fig. 3. The first stage of this converter has no such balancing issue since the input capacitor is typically sufficiently large.

Fig. 1(b) shows the modified topology with the switch nodes $sw1$ and $sw2$ merged to one node. The inductors L_{21} and L_{22} are combined into one single inductor L_2. The new topology has two advantages: 1) fewer inductors and reduced size and cost; 2) lower voltage stress and current stress on the switches thanks to the automatic voltage balancing of the second stage. The equivalent circuits are presented in Fig. 4 to explain the voltage balancing mechanism. The main difference between the original topology and the new topology is that the capacitor voltages v_{C21} and v_{C22} are now constrained by the SC network. Specifically, the capacitors C_{21} and C_{22} are stacked and charged by C_{mid} in states 1 and 2, leading to

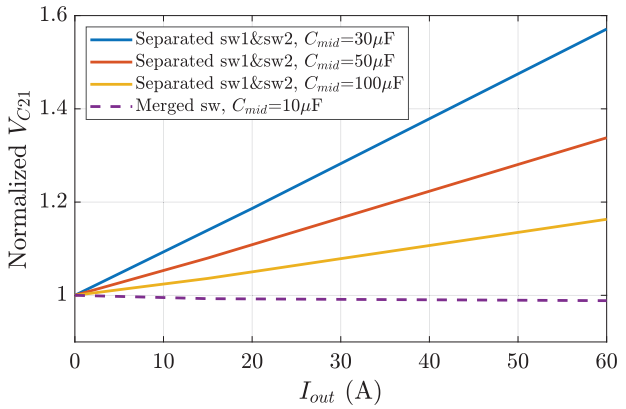

Fig. 3: Simulated average voltage of v_{C21} for the topologies with separated switch node (Fig. 1(a)) or merged switch node (Fig. 1(b)) at V_{in} = 54 V, C_1 = 40 μF, C_2 = 100 μF, and f_{sw} = 110 kHz.

v_{C21} + v_{C22} = v_{Cmid}. Since the two phases are symmetric, v_{C21} and v_{C22} have the same constrained average voltage, $\frac{V_{Cmid\_avg}}{2}$, with the waveform plotted in Fig. 5. The voltage v_{sw} is then balanced and independent of load current and capacitance C_{mid}. As seen from Fig. 3, even with only $1/10$ of the C_{mid} of the original topology, the merged-switch-

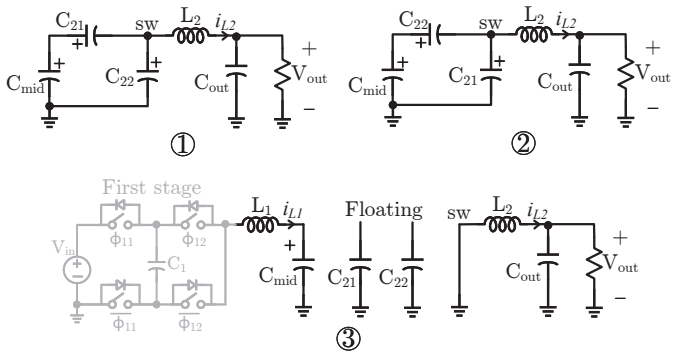

Fig. 4: Equivalent circuits of the converter in Fig. 1(b). Only the second stage is highlighted.

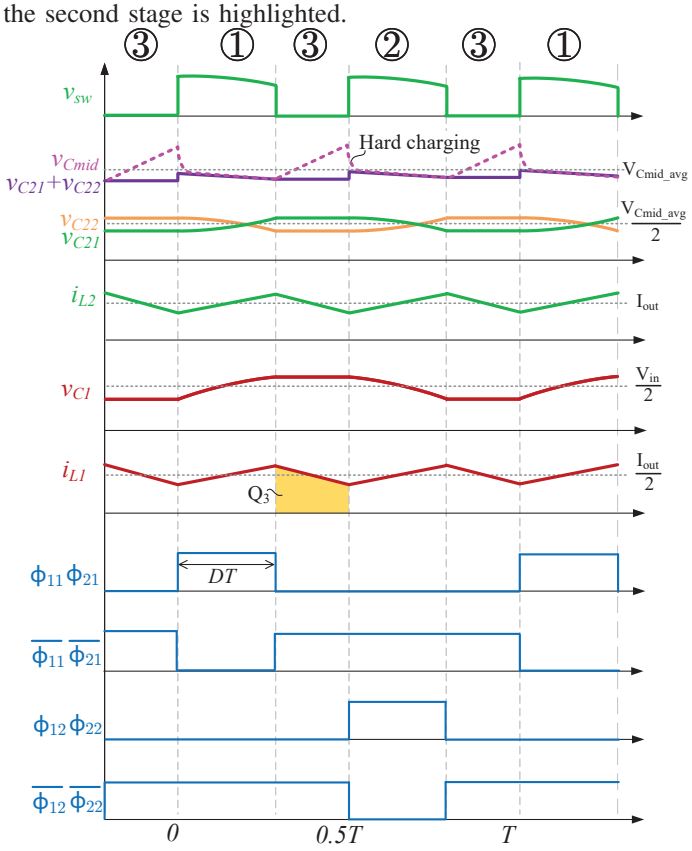

Fig. 5: Both stages operate in PWM mode. The voltage v_{sw} is balanced thanks to the merged switch node. The capacitor C_{mid} is hard charged because of an undesired charge Q_3 in state 3.

node case can achieve excellent voltage balancing over an entire load range. Since the output inductor sees a balanced switch-node voltage, the inductor current ripple is also reduced significantly compared with the unbalanced case in Fig. 2.

B. Hybrid Resonant-PWM Soft-Charging Control

A key desirable feature of hybrid SC converters is the concept of soft-charging of the capacitors, first introduced in [14], [15] to eliminate the undesirable charge sharing loss of pure switched-capacitor converters. In the proposed topology, although the voltage is balanced by merging the switch nodes, the capacitor C_{mid} may suffer from hard charging. This is

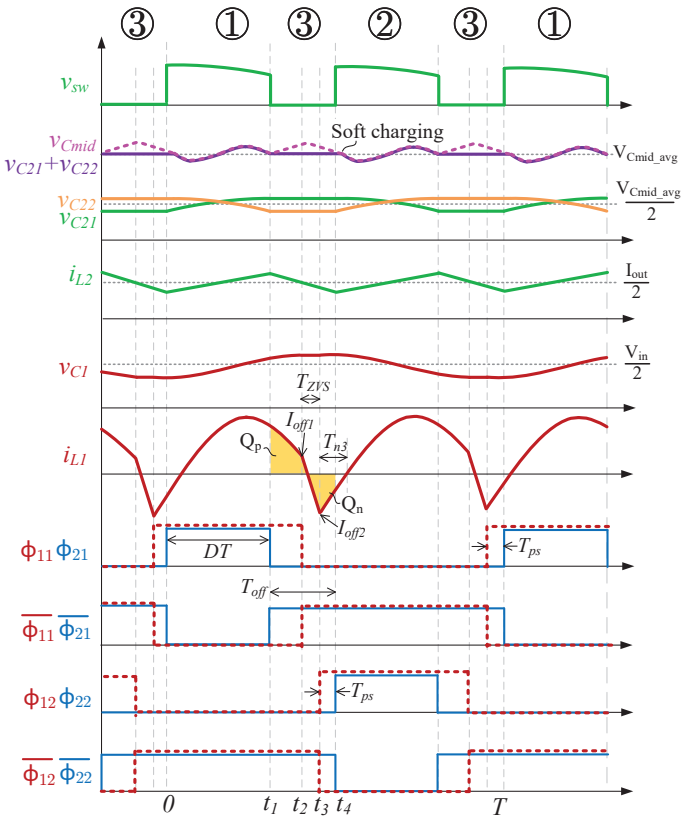

Fig. 6: The first stage operates in ZVS mode, and the second stage operates in PWM mode. The capacitor C_{mid} is soft charged because of zero net charge in state 3.

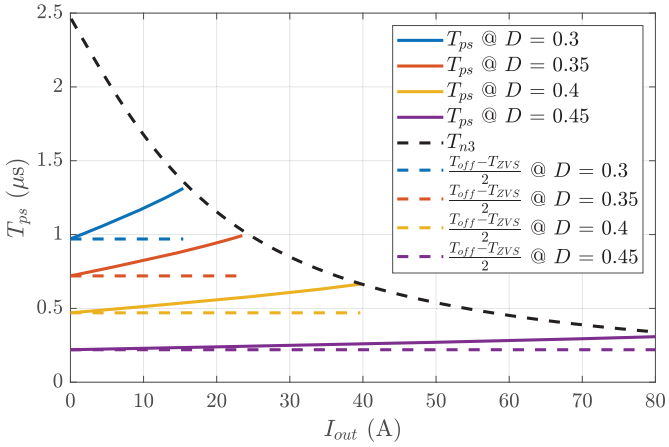

Fig. 7: Demanded phase shift T_{ps} versus I_{out} for the proposed converter operating at V_{in} = 48 V, C_1 = 50 μF, L_1 = 50 nH, $f_{sw} = f_r$ = 100 kHz, T_{ZVS} = 60 ns, and D = 0.3 - 0.45.

because C_{mid} is charged by current i_{L1} in state 3 in Fig. 4, corresponding to the undesired charge Q_3 as highlighted in Fig. 5. However, the capacitors C_{21} and C_{22} are floating during state 3 and thus $v_{C21} + v_{C22}$ is constant. The voltage difference between v_{Cmid} and $v_{C21} + v_{C22}$ causes hard charging at the end of state 3. Using a large C_{mid} can help reduce the hard-charging loss, but a small C_{mid} is often desired since it is important for improving power density.

Note that the extra charge Q_3 in Fig. 5 is the root of hard charging, so an intuitive way to realize soft charging is to ensure zero net charge of C_{mid} during state 3. The new control scheme is provided in Fig. 6, showing that the first stage operates at Zero-Voltage-Switching (ZVS) mode and the second stage operates at PWM mode. When the inductor current i_{L1} is designed to have an zero net charge during state 3, namely $Q_p = Q_n$, soft charging is achieved. The relevant ZVS control of a 2-to-1 resonant SC converter is discussed in [3], [16]. Compared with the conventional split-phase soft-charging control [17], the proposed soft-charging method does not need to sacrifice duty ratio, RMS current, or control complexity. Meanwhile, the ZVS operation of the first stage can greatly reduce switching loss and inductor size, improving system efficiency and power density.

The phase shift T_{ps} between two stages depends on the load current I_{out} and the second-stage duty ratio D. As can be seen from Fig 7, the demanded T_{ps} increases as D decreases and I_{out} increases. At light load, the slope of i_{L1} during $t_1 - t_2$ is similar to that during $t_3 - t_4$. It can also be proven that $I_{off1} = -I_{off2}$ at $f_{sw} = f_r$ [18]. Therefore, the areas Q_p and Q_n in Fig. 6 are symmetric at light load, leading to $T_{ps} = \frac{T_{off} - T_{ZVS}}{2}$, where T_{off} is defined by $T_{off} = (0.5 - D)T$. Note that the maximum negative charge Q_n is limited by the time duration T_{n3} in Fig. 6. When the converter is operating with D and I_{out} on the right side of T_{n3} curve in Fig 7, soft-charging is not achievable. Since the time T_{n3} is a decreasing function of I_{out}, and T_{ps} is an increasing function of D, the effective load range with soft-charging decreases as D decreases. In this design, the duty ratio D is in the range of $0.4 \leq D \leq 0.5$, corresponding to relatively flat T_{ps} curves in Fig 7. A simple phase-shift control with a load-independent T_{ps} is then used to realize soft-charging for a wide load range.

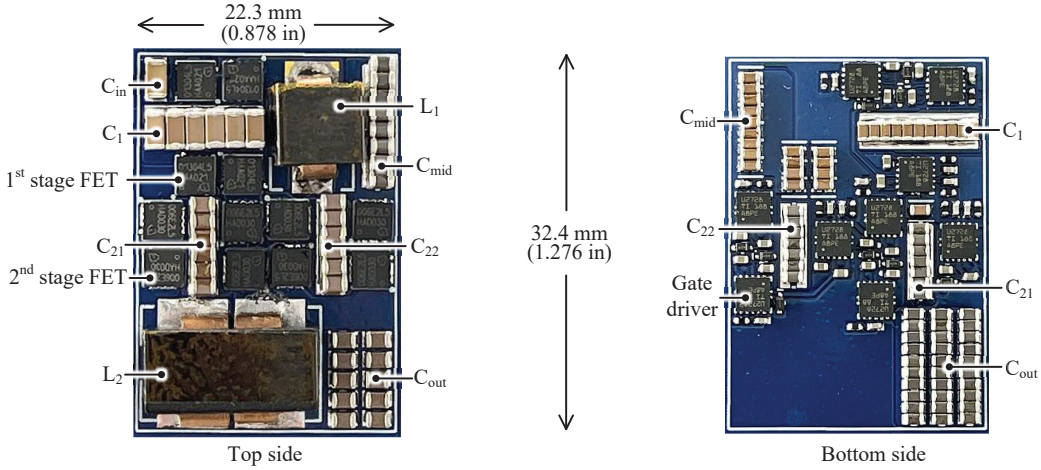

Fig. 8: Annotated photograph of the converter with the dimensions of 1.276 × 0.878 × 0.272 in (32.4 × 22.3 × 6.9 mm).

TABLE I: Main component listing of the proposed cascaded hybrid converter

Component	Manufacture and Part number	Parameters
1st-stage MOSFET	Infineon, IQE013N04LM6	40 V, 1.1 mΩ × 4
2nd-stage MOSFET	Infineon, IQE006NE2LM5	25 V, 0.65 mΩ × 8
1st-stage flying capacitor C_1	TDK, C3216X5R1H106K160AB Murata, GRM188R6YA106MA73D	10 μF*, 50 V, X5R, 1206 × 18 10 μF*, 35 V, X5R, 0603 × 11
Middle capacitor C_{mid}	TDK, C2012X5R1V226M125AC Murata, GRM188R6YA106MA73D	22 μF*, 35 V, X5R, 0805 × 24 10 μF*, 35 V, X5R, 0603 × 18
2nd-stage flying capacitor C_2	Murata, GRT21BR61E226ME13L TDK, C1608X5R1E106M080AC	22 μF*, 25 V, X5R, 0805 × 18 10 μF*, 25 V, X5R, 0603 × 7
1st-stage resonant inductor L_1	Custom powder-iron inductor	55 nH, one-turn
2nd-stage inductor L_2	Custom powder-iron inductor	180 nH, two-turn
Gate driver	TI, UCC27284DRCT	120 V, half bridge
Bootstrap diode	Onsemi, NSR0340V2T1G	40 V, Schottky

* The capacitance listed here is the nominal value before dc derating.

III. Hardware Implementation and Experimental Results

A prototype is constructed to verify the above analysis. The first-stage flying capacitor and resonant inductor are selected carefully to achieve soft charging and soft switching. The resonant inductor L_1 is a 55 nH customized one-turn inductor. The output inductor L_2 is a 180 nH customized two-turn inductor. A full component list is provided in Table I. An annotated photograph of the hardware prototype is shown in Fig. 8. All switches and inductors as well as the majority of the flying capacitors are placed on the top side of the board. The gate-drive circuits are on the bottom side of the board. The gate drive power is provided by the cascaded bootstrap method as introduced in [16]. To reduce the trace resistance, a 6-layer PCB with 2 oz. copper for each layer is used in the design.

The measured switch-node voltage is balanced as shown in Fig. 9, which verifies the analysis in Section II-A. The duty ratio of the second stage is 0.45 for 54-to-12-V conversion, and the phase shift $T_{ps} = 0.25\ \mu s$ is selected according to Fig. 7. The voltage v_{Cmid} has a small ripple (< 0.3 V) at 20 A output thanks to the soft-charging operation. The prototype is tested up to 80 A output current for V_{in} = 48 V - 60 V with a regulated 12 V output, corresponding to 3115 W/in^3 power density. Compared with the unregulated cascaded resonant converter in [3], the proposed regulated converter has 23% reduced power density due to a larger output inductor.

Very high efficiency is achieved across the entire load range as shown in Fig. 10. At 48-to-12-V conversion, the peak system efficiency is 99.0%, and full-load efficiency is 97.3%. As V_{in} increases, the duty ratio of the second stage decreases, and the inductor loss (winding loss + core loss) of L_2 increases, leading to lower efficiency. This high-density converter also has a good thermal performance. As shown in Fig. 11, the maximum temperature is 82.1^{o}C at full load with fan cooling only.

The efficiency and power density of this work and the state-of-the-art regulated 48-to-12-V IBC are listed in TABLE II. Compared with the highly integrated and highly optimized Vicor design in [19], this converter achieves 19% higher power density and 33% lower conversion loss at 60 A output. The power density is 4.6 times of that of the GaN-based LLC converter in [20]. Moreover, this converter can be fabricated using inexpensive and common components, e.g., Silicon MOSFETs and 6-layer PCB. The bottom side of the PCB in Fig. 8 has not been fully occupied by components so far. A controller circuit as well as copper pillars for power/ground terminals can be added in the spare space to construct a complete IBC module.

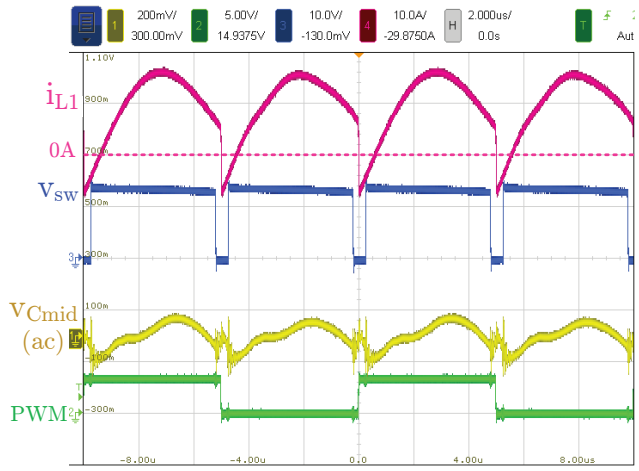

Fig. 9: Measured waveform of v_{Cmid} ripple, i_{L1}, and v_{sw} at V_{in} = 54 V, V_{out} = 12 V, $f_{sw} = 100$ kHz, and I_{out} = 20 A.

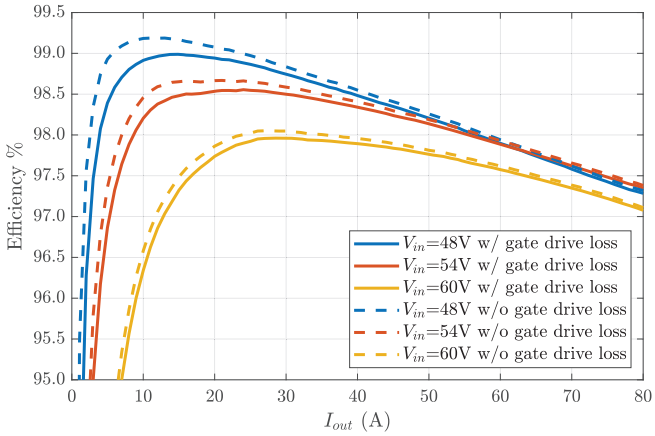

Fig. 10: Measured efficiencies at 48 – 60 V input and 12 V output with and without gate drive loss.

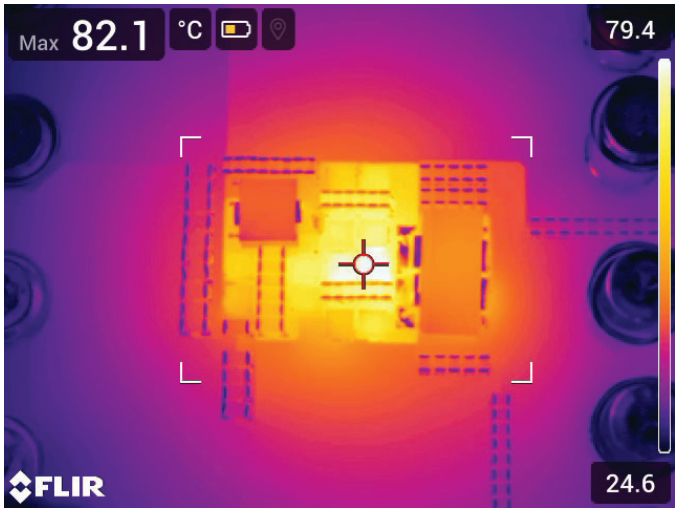

Fig. 11: Thermal performance at V_{in} = 54 V, V_{out} = 12 V, and I_{out} = 80 A with fan cooling only.

IV. Conclusions

This work proposes a novel cascaded hybrid switched-capacitor converter for regulated 48-to-12-V applications. The

TABLE II: Comparison of this work with the state-of-the-art regulated 48-to-12-V intermediate bus converters

Reference	Max. I_{out}	Power density	System Efficiency	Conversion ratio
Cascaded hybrid converter (this work)	80 A	3115 W/in^3	Full load: 97.3% Peak: 99.0%	48-to-12 V
			Full load: 97.4% Peak: 98.6%	54-to-12 V
Vicor DCM3717 [19]	62.5 A	2613 W/in^3	Full load: 96.7% Peak: 96.8%	54-to-12 V
GaN-based LLC with matrix transformer [20]	83.3 A	677 W/in^3	Full load: 97.7% Peak: 97.8%	48-to-12 V
ABB QBDS128A0B [21]	128.3 A	810 W/in^3	Full load: 97.1% Peak: 97.6%	54-to-12 V
EPC9130 Buck [22]	60 A	1000 W/in^3	Full load: 95.8% Peak: 96.2%	48-to-12 V

second-stage three-level converters have a merged switch node to achieve natural voltage balancing with a small C_{mid}. The first stage operates at a ZVS mode to realize soft charging for all capacitors. The effective load range with soft-charging capability decreases as duty ratio decreases. A hardware prototype is built and tested with input voltage ranging from 48 – 60 V and output current up to 80 A. The 3115 W/in^3 power density, 98.6% peak efficiency, and 97.4% full-load efficiency at the 54-to-12-V conversion reflect a dramatic improvement over the state-of-the-art converters from industry and academia.

V. Acknowledgment

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000906 in the CIRCUITS program monitored by Dr. Isik Kizilyalli. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

References

[1] X. Li and S. Jiang, "Google 48V Rack Adaptation and Onboard Power Technology Update," in *Open Compute Project (OCP) 2019 Summit*, 2019.

[2] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Transactions on Power Electronics*, pp. 1–1, 2019.

[3] T. Ge, Z. Ye, R. Abramson, and R. C. N. Pilawa-Podgurski, "A 48-to-12 v cascaded resonant switched-capacitor converter achieving 4068 w/in^3 power density and 99.0% peak efficienc," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021.

[4] D. Reusch, S. Biswas, and M. de Rooij, "Gan based multilevel intermediate bus converter for 48 v server applications," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2018, pp. 1–8.

[5] P. S. Shenoy, M. Amaro, J. Morroni, and D. Freeman, "Comparison of a buck converter and a series capacitor buck converter for high-frequency, high-conversion-ratio voltage regulators," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7006–7015, Oct 2016.

[6] A. Stillwell, E. Candan, and R. C. N. Pilawa-Podgurski, "Active voltage balancing in flying capacitor multi-level converters with valley current detection and constant effective duty cycle control," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11 429–11 441, 2019.

[7] J. S. Rentmeister, C. Schaef, B. X. Foo, and J. T. Stauth, "A flying capacitor multilevel converter with sampled valley-current detection for multi-mode operation and capacitor voltage balancing," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8.

[8] R. H. Wilkinson, T. A. Meynard, and H. du Toit Mouton, "Natural balance of multicell converters: The two-cell case," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1649–1657, Nov 2006.

[9] N. Vukadinović, A. Prodić, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Extended wide-load range model for multi-level dc-dc converters and a practical dual-mode digital controller," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1597–1602.

[10] Z. Ye, Y. Lei, Z. Liao, and R. C. N. Pilawa-Podgurski, "Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 2921–2935, 2022.

[11] X. Yuang, H. Stemmler, and I. Barbi, "Self-balancing of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under sub-harmonic PWM modulation," *IEEE Transactions on Power Electronics*, vol. 16, no. 2, pp. 256–263, Mar 2001.

[12] D. H. Zhou, J. Celikovic, Y. Elasser, D. Maksimovic, and M. Chen, "Balancing limits of flying capacitor voltages in coupled inductor fcml converters," in *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1–8.

[13] D. H. Zhou, A. Bendory, C. Li, and M. Chen, "Multiphase fcml converter with coupled inductors for ripple reduction and intrinsic flying capacitor voltage balancing," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 1284–1290.

[14] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*, June 2008, pp. 4008–4015.

[15] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, July 2012.

[16] Z. Ye, Y. Lei, W. c. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for gan-based flying capacitor multi-level converters," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 2925–2931.

[17] Y. Lei, R. May, and R. C. N. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 770–782, Jan 2016.

[18] J. S. Rentmeister and J. T. Stauth, "Zero voltage switching for flying capacitor multilevel converters at nominal conversion ratios," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 30–36.

[19] Vicor Inc., *48V to Point-of-Load Non-Isolated, Regulated DC Converter*, 2021. [Online]. Available: https://www.vicorpower.com/documents/datasheets/ds-DCM3717S60E14G5TN0-VICOR.pdf

[20] M. H. Ahmed, A. Nabih, F. C. Lee, and Q. Li, "High-efficiency, high-density isolated/regulated 48v bus converter with a novel planar mag-

netic structure," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 468–475.

[21] ABB, *QBDS128A0B : Barracuda DC-DC Converter*, 2022. [Online]. Available: https://www.abbpowerconversion.com/assets/pdfs/technical-documentation/datasheets/qbds128a0b_ds_v1.1_20220518.pdf?utm_source=pitching&utm_medium=newsrelease&utm_campaign=QBDS2022&utm_content=QBDS128datasheet

[22] EPC Inc., *EPC9130: 48 V-12 V, Regulated Intermediate Bus Converter*, 2018. [Online]. Available: https://epc-co.com/epc/Products/DemoBoards/EPC9130.aspx