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System on Chip Design Integrated With Visible Light Communication and Multi-Mode Multi-Band Radio-Frequency Front End

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

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by

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I was ever thinking why I came to US and pursued a PhD degree, does it matter the fame and fortune? Does it matter the career path? Does it matter changing life? All of these seem pertinent but not true. I would like to say may the God drive me here, the five academic years taught me the critical thinking and gave me the chance to touch the spiritual philosophy, and the most important, I am able to work with lots of brilliant people.

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ABSTRACT OF THE DISSERTATION

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by

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Dr. Albert Wang, Chairperson

Nowadays, the modern communication system employing the electromagnetic theory has been the mainstream in our daily life, which allows people to interact directly with people from all over the world, creating a more global society. In addition, the increasing demand for wireless data pushes the technology to move forward, the emergence of long term evolution (LTE) and LTE advanced standards already facilitate the human life greatly.

In the next a few years, the fifth generation communication system employing the massive multiple input multiple output (MIMO) and carrier aggregation techniques will further increase the data rate to enrich the application of mobile device at the price of more complex base-band (BB) modulation/demodulation method and multi-mode supported front end module (FEM), and more add-on frequency bands require a highly integrated chip to minimize the cost and size. However, consider the individual circuit performance, the power amplifier, switch, analog circuit usually will use different technology, Gallium Arsenide (GaAs), silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS), Bulk CMOS for each, therefore it will increase the cost and package complexity.

Due to the limitation of licensed bandwidth and power trade-off predicted by Shannon theory, we can forecast that the communication based on wireless radio frequency (RF) will encounter the data rate bottleneck, so that another supplementary communication method as visible light communication (VLC) is proposed. Conventional lighting using incandescent and fluorescent lamps are believed to be replaced by high efficiency lighting light-emitting diode (LED) because of the benefits of low power, long-life, inherent safety and small integrated package. At the same time, LED can be turned on/off very quickly without flickering to human eyes, so it enables the LED to modulate the signal to realize wireless communication, it's really promising to use that in the internet of things (IOT), near field communication or some radio frequency sensitive scenarios, like in hospital, airplane. Unfortunately, all reported VLC systems are assembled in PCB with discrete components and separated from RF system.

This dissertation presents a novel true single-chip, single-die, Multi-mode Multi-band (MMMB) Power Amplifier FEM and VLC designed and implemented in IBM SOI 0.18um technology. Its ultra-high efficiency and high linearity architecture offers broadband support of 3G/LTE modes. FEM integrates low-band, mid-band and high-band power amplifiers with input and output impedance matched to 50Ω, and ESD protection circuits. In addition, this chip integrated switches support more than nineteen frequency bands for all 3G and 4G modulations. It meets all specifications as stated in 3GPP 3G and LTE standards. Output power is controlled by changing the input power and VCC is adjustable to maximize PA efficiency for each power level. The VLC receiver is also integrated.

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Chapter 1 Introduction

1.1 Background

Over the decade, with continuous development in technological advancements, wireless communication has made a tremendous progress from simple to complex systems that are able to communicate across multiple networks platform. It is clear that wireless technologies will continue to play an even more critical and vital role as its proved benefits.

At present, communication using radio frequency dominates the wireless market, let's look back the history of the past tens of years, prior to 1973, mobile telephone was limited to phones installed in cars or other vehicles. Later first handheld mobile phone was produced by Motorola with 1.1Kg weight and measured with 23 cm long, 13 cm deep and 4.45 cm wide, that analogue prototype offers a talk time of just 30 minutes and took 10 hours to re-charge and works as a true "brick". Then in the 1990s, the "second generation" digital mobile phone systems emerged. Two systems competed for supremacy in the global market: the Global System for Mobile communication (GSM) and Code Division Multiple Access (CDMA), during that time, talk and text are the major features. As the use of 2G phones became more widespread and people began to utilize mobile phones in their daily lives, the demand for data was growing for sharing pictures, browsing webpages, etc. However, the 2G technology was nowhere near up to the job, so the industry began to work on the next generation of technology known as 3G Wideband Code Division Multiple Access (WCDMA) and CDMA Evolution Data Optimized (EVDO), that enables the data rate up to 2 Mbit/s maximum data rate indoors, and in the mid-2000s, WCDMA evolved to high-Speed Packet Access (HSPA) with higher data rate up to 14 Mbps. So far, the Long

LTE is most common used, which increases the capacity and speed using a different radio interface together with core network improvements. The LTE standard covers a range of many different bands, each of which is assigned with a band number. Multiple versions of the same LTE device are required to accommodate the worldwide proliferation of cellular bands-40 already and counting [1]. The problem gets even worse when people consider different band combinations required to support LTE carrier aggregation.

The demands for various standards lead to including multiple transceivers in one device, the competitive market forces the devices to be low cost to manufacture and time to market as short as possible. It became inevitable to reduce the number of components, the System on Chip (SoC) or the System in Package (SIP) approach became prevalent in this purpose [2].

With such an explosive growth of wireless communication market, the low-cost, highly-integrated wireless communication system is urgently needed. Even though most blocks in the front-end have successfully been integrated by using the CMOS technology, it is still an unbelievable challenge to integrate the entire front end. As shown in Figure 1-1, the advent of more advanced standards requires more frequency bands to achieve the needed throughput. The FEM consists of several parts, the antenna is off-chip part made in the PCB, and the RF signal will go through the Antenna tuner first to get the best matching, an antenna can efficiently cover bands with frequencies from 700 MHz to 3.5 GHz. In addition, a group of switches includes main/diversity switch, and antenna swapping switches. The antenna swap switch changes the main and diversity antenna by selecting

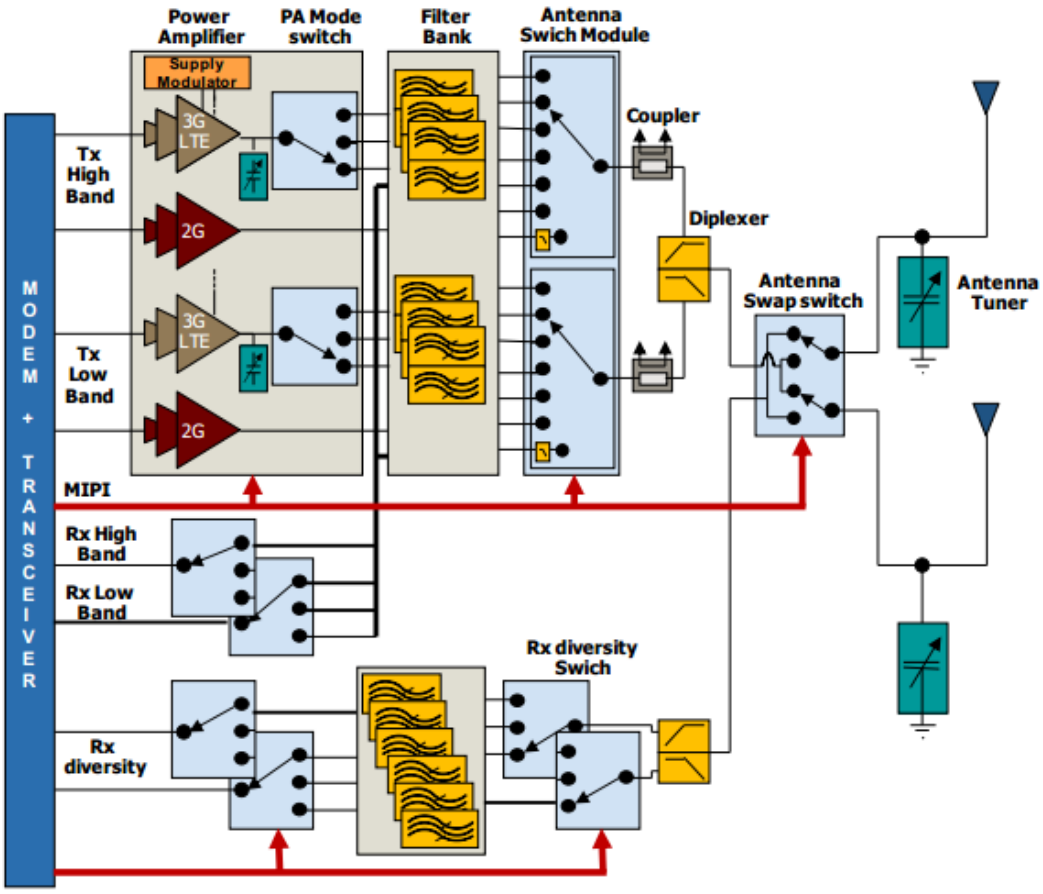


Figure 1-1 Front-end-module block diagram [3]

the stronger detected signal in base-band module as main receiving input. So far, SOI technology is the best CMOS technology to implement this kind of RF switch (SW). A three-port diplexer containing two filters in the following block will differentiate frequency signals into low pass and high pass band, which is used for band selection and potential carrier aggregation. A coupler monitors the output power at antenna port and normally requires an accurate calibration. The most important part in the FEM is the advanced architecture to achieve compact and cost efficient multi-mode, multi-band in single core broadband power amplifier (PA) [4]. In addition, an advanced power management is

required to provide the PA/SW bias voltage as well for implementing adaptive envelope tracking to make the PA more efficient. Nevertheless, the circuit blocks above can hardly achieve a single-die single-chip solution. As known to all, the CMOS technology enables the integration of the most digital and analog components in the wireless device such as digital signal processing (DSP), digital-to analog converter (DAC), analog-to-digital (ADC), DC-DC converter, etc. With the developing of technology, most of the RF components including low noise amplifier (LNA), mixers and voltage-controlled oscillators (VCOs), have successfully been integrated in the CMOS technology with competitive performance compared to other advanced technology. However, the bottleneck of the fully integrated solution relies on the power amplifiers and antenna switches. In order to get the best performance of PA in terms of power efficiency and linearity, GaAs and Silicon Germanium (SiGe) has the advantage in today's communication system whereas PA in CMOS usually suffers from low power low frequency. The today's wireless communication industry is trying to integrate more standards in a single device and integrate more components in a single chip. However, there are two concerns for this method, first, the requirement of the low cost is one of the top in the industry, as the development of scaling down of technology node, the Analog/Mixed circuit can easily achieve a fair performance as well as the low price. Secondly, the integration of multiple wireless standards necessitates the performance

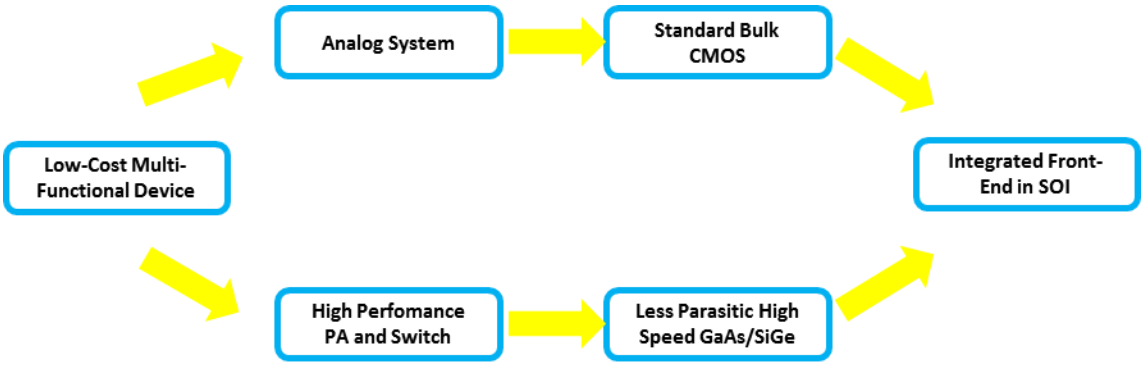


Figure 1-2 Implementation to full-integrated front-end module

comparable to separate device in the front end. In other words, the power handling capability and linearity of the RF switch should match the power signals. The linearity and efficiency of PA should be enhanced to cover the different mode modulated signals such as LTE and WCDMA. The solution to achieve these goals is shown as Figure 1-2. The demand for the low-cost, multi-functional devices leads to system integration and performance improvement. In term of the system integration, the silicon based technology is the most common option for the analog circuit. With respect to performance, fortunately, compared to bulk CMOS, SOI CMOS benefits a lot from its silicon oxide insulator layer which means the single die solution in a SOI CMOS is possible to get an overall performance with full integration.

Although wireless communication using radio frequency is prevailing featuring large coverage, invisibility advantage, however, the data rate is still not sufficient for daily use. Wireless has the limited licensed bandwidth in the air interface, and consider multi-users in a crowded cell, each user cannot experience a quick surfing. In addition, RF is not so safe or confidential considering some scenarios, like travelling in the airplane or visiting

in the hospital, so the visible light communication is good supplementary option, the receiver module is integrated in this design as well.

Designed with cost and space savings in mind, and at the same time, with competing performance, this dissertation presents a FEM and VLC design fully integrated in the IBM SOI 0.18um technology. The block diagram is depicted as Figure 1-3, Three PA cores covering LB/HB/MB are co-designed with following stage RF switch, the digital MIPI is designed to control the analog bias circuit and switch on/off. The VLC receiver is also included.

1.2 Organization of the Thesis

This dissertation is organized as follows. First, the process feature of SOI and package advantage is discussed in the Chapter 2. Then a specific design of Antenna RF switch is introduced in Chapter 3. Chapter 4 talks about another critical front end part design, diplexer. A MMMB PA has been explored in Chapter 5. Chapter 6/7/8 describe the analog/digital circuit design including Bias/VLC/MIPI Control. Electrostatic charging (ESD) protection is always important for the circuit, so Chapter 9 discusses the design methodology of that. A novel crosstalk reduction technique based on the post-fabrication has been summarized in Chapter 10. Last but not least, Chapter 11 shows the test bench and measurement result.

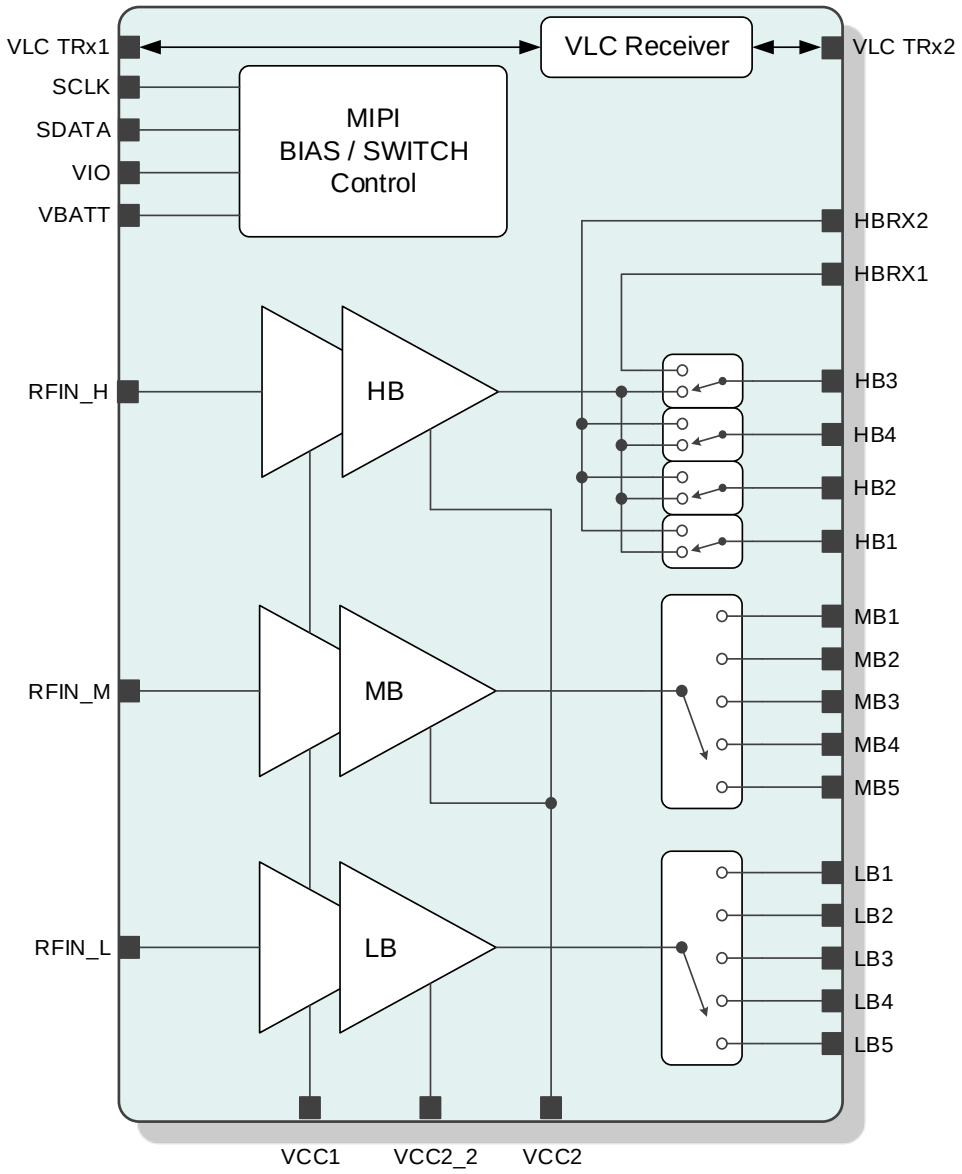


Figure 1-3 Block diagram of the Multi-Mode Multi-band FEM integrated with VLC

Chapter 2 SOI and Package Technology

2.1 SOI Technology Introduction

CMOS has been actively developed for RF applications in the low-GHz range to increase the integration level in wireless communication devices (Personal phones, Bluetooth, wireless local area network (WLAN), etc.). Full integration of the RF active and passive component in Bulk-Si, however, requires special processing, like triple well and deep trenches to control the cross-talk interaction, substrate noise, and Q-factor degradation of on-chip inductors. On the other hand, SOI and silicon on sapphire (SOS) have been recognized for their advantage in digital analog and RF applications. Over the last three decades, SOI has demonstrated as one possible method for increasing the performance of CMOS over that offered by simple scaling.

Bulk and SOI CMOS are compared in terms of speed, crosstalk, and parasitic, etc, in different circuit application [5][6][7]. In SOI, an additional BOX layer is placed between the active Si layer where is used to create MOSFET and Substrate layer as shown in Figure 2-1. The utilization of BOX is to minimize parasitic capacitances associated with junction-to-well diode, and to reduce substrate coupling. Because devices are isolated from the substrate, the transistors may be stacked to handle high power signals without requiring trip-well structures for device isolation, and the reduced parasitic capacitance enables high isolation between each circuit block.

For RF/Analog IC design, SOI shows significant advantages like improved frequency performance through reduced capacitance, higher drive current and a reduction in interconnect length. For high power application, in order to maximize the linearity,

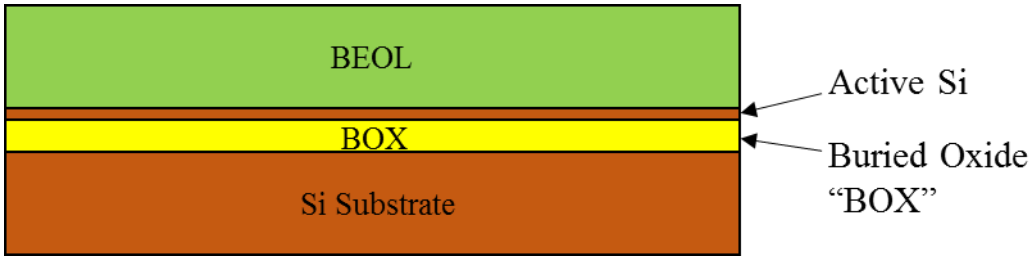


Figure 2-1 Cross section of SOI CMOS

negative voltage bias is allowed since noise and latchup are minimized through reduced substrate coupling. In addition, Inductor Q can be enhanced with very high resistivity substrates. For Digital IC design, SOI circuits exhibit better performance than bulk silicon because of the dynamic threshold voltage effect as well as the reduced junction capacitance. SOI has the advantage that junction capacitance can be scaled as supply voltage, which is difficult with bulk CMOS. This benefit offers SOI the ability to extend Moore's law to scale transistors as the channel length approaches tens of nanometers. In addition, the reduced junction capacitance of SOI implies superior SRAM performance, while translates to faster microprocessors.

As shown in Figure 2-2, SOI 180nm enables integration of RF/analog functions including multi-mode and multi-band RF switches, complex switch-biasing networks and power controllers into single-chip FEM solution. In this dissertation, with the superior RF performance, the multi-mode and multi-band power amplifier can be integrated as well. The 180nm technology node is selected for the RF switch platform as a good compromise between transistor voltage capability and feature size [8][9]. This also afford the advantage of adapting elements from IBM's existing 180nm bulk silicon RF CMOS technology, including the device spacer and silicide processes, plus the back-end-of-line (BEOL) wiring configuration. The starting wafer is 145nm SOI on a high resistivity p-silicon

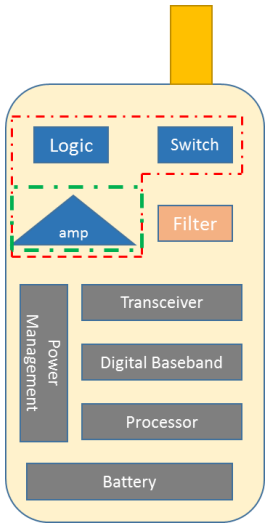


Figure 2-2 Integrated front end solution with SOI technology

substrate wafer. The thin silicon device layer permits the partially depleted SOI MOS transistors. The BOX thickness is 1um to minimize capacitive coupling to the substrate.

2.1.1 Equivalent small signal circuit

Figure 2-3 shows simplified capacitive model of SOI FET. Latch up could be avoided because transistors are completely isolated by oxide and shallow trench isolation so that there is no parasitic bipolar device between FETs. In addition, since the bottom plate of source/drain to substrate junctions is physically insulated by a thick silicon oxide layer ($\varepsilon r=3.9$), the substrate to body junction capacitance is much lower than that in Bulk CMOS ($\varepsilon r=11.9$).

2.1.2 Linearity

Linearity is another concern for the RF application, fixed charge at the oxide/silicon interface creates a weak inversion layer, also called the parasitic conduction (PSC) layer on the top of the substrate as shown in Figure 2-4. RF signals carried by wiring, bond pads,

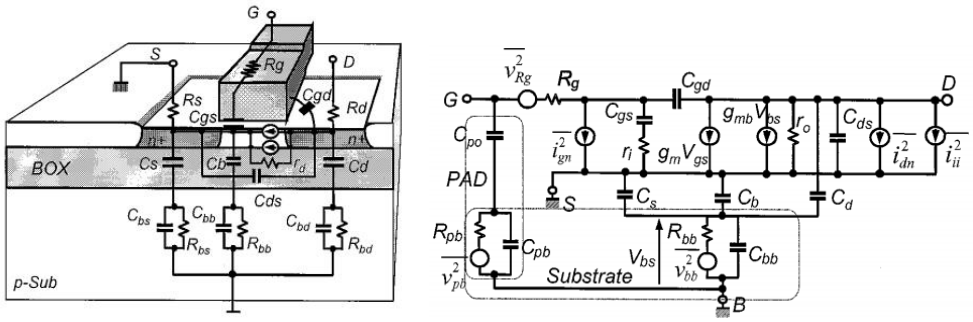


Figure 2-3 The SOI MOS transistor structure and small signal equivalent circuit elements 0

or silicon devices displace inversion electrons from the interface over the negative swing in the AC cycle. This results in a weakly varying C-V characteristic that generates harmonic power in signal lines and devices. The presence of this inversion layer also provides a mechanism to couple RF power to substrate which results in larger than expected substrate losses. It is necessary to introduce additional process steps to suppress this inversion layer [10].

TQ trench is developed for reducing harmonic distortion caused by substrate-circuit interactions and built after the FEOL devices. The trench permits a high dose damage implant to be performed, which inhibits formation of a mobile electron layer at the BOX/substrate interface, thus improve the technology linearity as shown in Figure 2-5.

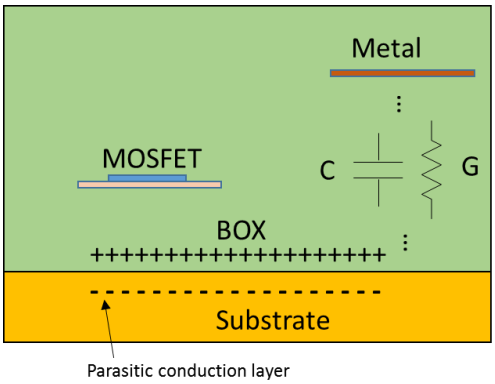
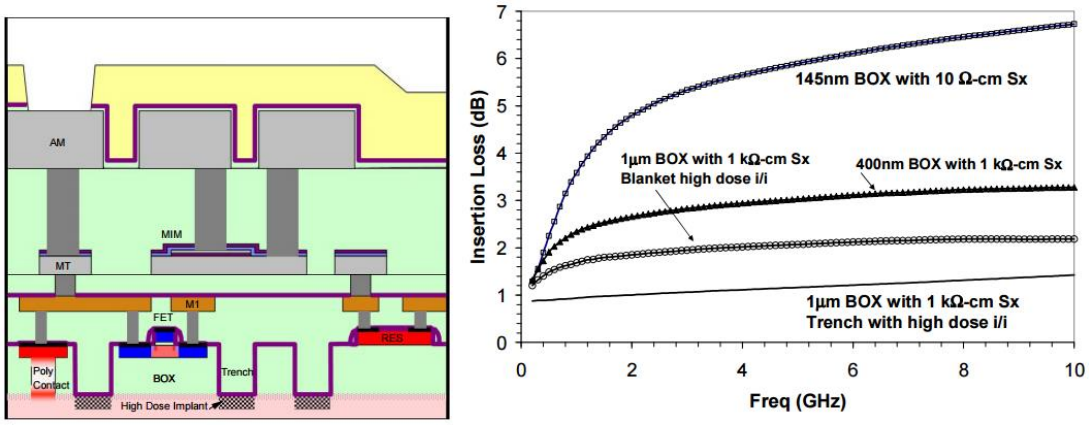


Figure 2-4 Inversion layer induced by fixed oxide charge in substrate

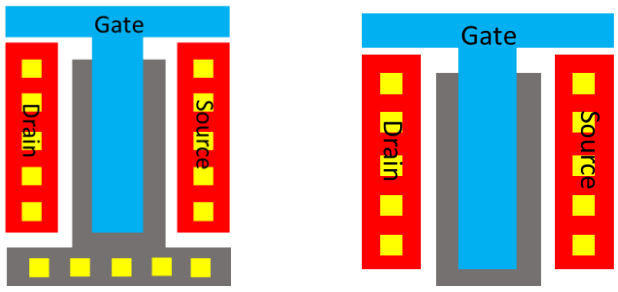


(a) (b)

Figure 2-5 (a) Process cross-section showing TQ trench in SOI (b) Insertion loss improvement with TQ trench [8]

2.1.3 Body Contacted FET and A Floating Body FET

The SOI technology used in this research was a partially-depleted SOI which provides two types of FETs, a body contacted (BC) FET and a floating body (FB) FET. The layout views of these FETs are shown in Figure 2-6. The FB FET is advantageous in terms of the size and the ease of control because that the body terminal of the FET does not need to be controlled. However, the uncertainty of the body voltage exists with large voltage swings. Moreover, the breakdown voltage of the BC FET is higher than that of the FB [11]. Thus, in this research, the BC FET was chosen to implement the antenna switch.



(a) (b)

Figure 2-6 Two types of FETs in the SOI technology: (a) body contacted and (b) floating body

2.2 Package Technology

The function of electronic packaging is to protect and cool down the microelectronic devices, and to provide electrical and mechanical connection between the devices and the outside world [12]. Packaging is an essential and integral part of semiconductor products. It is important as it affects the operating frequency, power, complexity, reliability and cost of semiconductor products. With the advance of deep sub-micron CMOS technologies, CMOS processes have been implemented in RFIC design. Because the lossy Si substrates of CMOS chips, the quality factor (Q) of on-chip inductor is usually low, typically 2~10 [13][14], this limits the design of high performance RF CMOS circuits. Although Q of the discrete inductors and embedded inductors on the package substrate is quite high [15], the parasitic of interconnects between chips and off-chip passives degrade the accuracy of inductance values. Bad tolerance of the interconnects induces large variance of parasitic from batch to batch. Compared to the traditional inductors, inductors in Wafer-level-Package (WLP) could be fabricated on a thick, low-K, low loss dielectric layer, and with wide, thick and low resistivity metal wires. As a result, Q of the inductor in WLP is much higher than that of their traditional on-chip counterparts. Regarding to front-end, high level of integration with true market value (TMV) includes Front-end in a Package (FIM), front end on chip (FOC), etc.

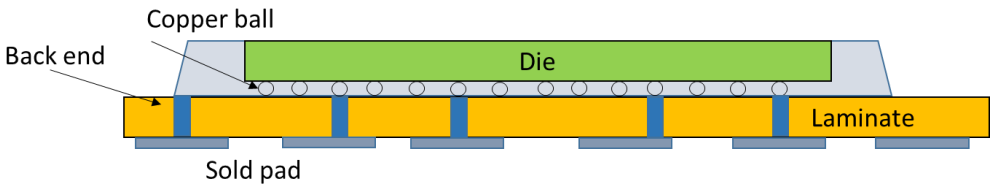


Figure 2-7 Simplified cross section of Land Grid Array (LGA) Flip-chip package using laminate

In this dissertation, a Flip-chip using laminate is proposed as the package method, which enables the embedded high Q RF passive element implementation. As shown in Figure 2-7, the die is flipped and attached on the laminate, the embedded BEOL in laminate can be used as the extra routing metal, and it provides the design capability extremely.

Table 2-1 Available process technologies comparison for front-end module

Technology	Applications in PA or front-end	Advantages	Disadvantages	notes
GaAs	PA engine	High PAE PAs, FEM	High in cost. Good for module, not for FOC/SOC	Good for FIM
SOI	Switch, control, PA	Integration for FOC/SOC	High loss in on die matching network, cost needs to come down further. No TMV.	Good for FOC with some PAE tradeoff
SiGe	WiFI PA, control, maybe switch too.	Integration for FOC/SOC, not as good as SOI for switch. TV good for thermal.	High loss in on die matching network, not cheap.	Good for WiFi FOC.
Bulk CMOS	Digital, low power PA, LNA. Baseband and SOC.	Low cost.	No TMV, High loss in on die matching network, poor device for RF. Not for switch.	Not good for FOC.

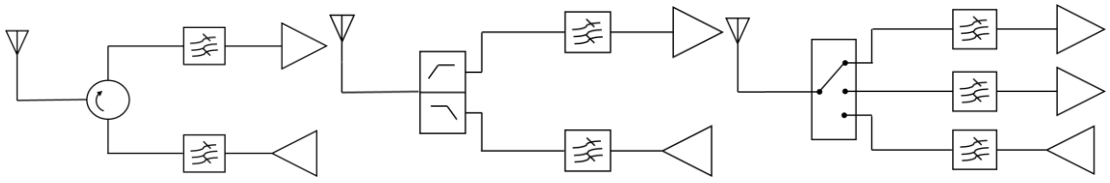
In summary, bulk CMOS is the main process technology used in RFIC area, especially in RF transceiver design, because of its low cost, low power consumption and low bias voltage. In addition, III-V technology like GaAs dominates the FEM due to its high

resistive substrate and excellent power handling capability. However, high cost, high bias voltage and difficulty in integration to CMOS make III-V group technology under high pressure. The compatibility of SOI with bulk CMOS and the high RF performance make SOI a good candidate to replace III-V technology in RF FEM design. The benefits of SOI and high performance of IC attract the interest of both academia and industry and maybe the best option for RF FEM full integration. The pros and cons of each technology are summarized in Table 2-1.

Chapter 3 SOI RF Switch

3.1 RF Switch Introduction

Basically, there are three kinds of front-end duplexing options as shown in Figure 3-1, the first one (a) illustrates a circulator approach, although it can provide load-pulling protection, it's normally bulky and heavy due to ferrite and inherent narrow band, thus it cannot support multi-band application. (b) depicts a filter-bank solution, the advantage of that is no linearity or transient concerns, but it requires very high Q resonators (LTCC/Ceramic Cavity FBAR), and high losses from multiple filters. (c) demonstrates the switching approach which benefits from high scalable ability, but it requires highly linear, low losses, high power switch and bias control signal are required as well. By making use of the advantage of SOI technology, the switching approach is the best option for the single-die, single-chip integration, as an on-die solution. SOI switch design has many advantages over traditional GaAs pHEMT designs. It can operate at much lower battery voltages and inherently has CMOS compatible control logic. The design of SOI switches, however, requires the use of extra circuitry like negative voltage, level shifters and so on to make them a complete RF switch.



(a) (b) (c)

Figure 3-1 (a) Circulator Approach (b) Filter Bank Approach (c) Switching Approach

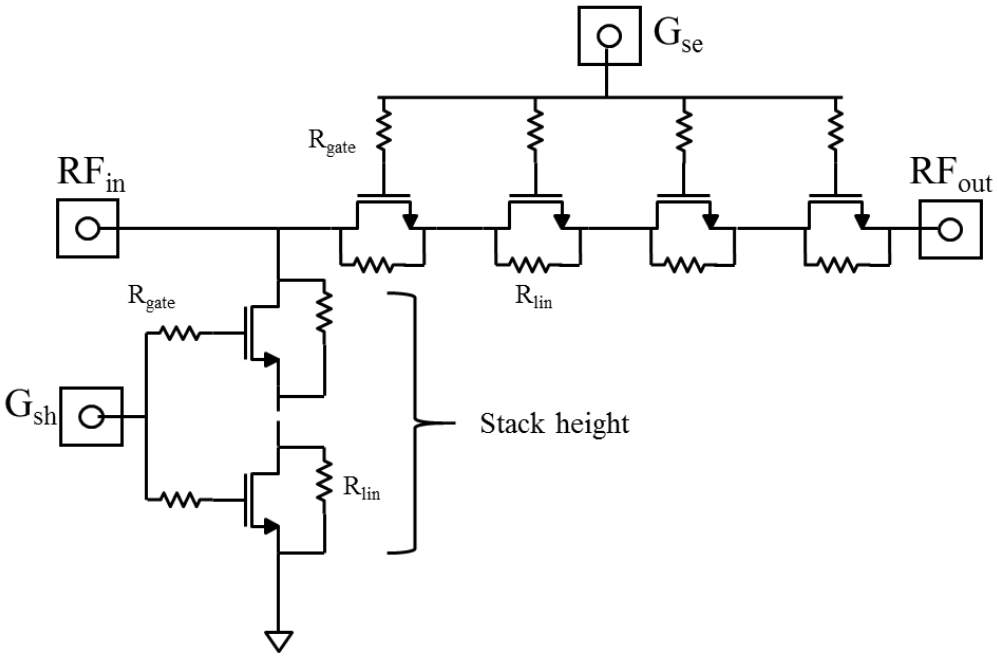


Figure 3-2 Typical SOI RF switch with series and shunt branch

A typical SOI RF switch is shown as Figure 3-2, when this switch block is turned on, RF signal will go through the series branch, the G_{se} is biased with ON state, then arrive at the RF_{out} port, the shunt branch is OFF at this time. When the switch block is turned off, the shunt branch is ON to provide additional isolation capability. A "linearizer" resistor R_{lin} is placed across the source-drain of all devices in the design to prevent any DC voltage potential from developing in the stack. This aids in equal RF voltage division across the stack height. A gate resistor R_{gate} is placed on the gate bias feed to provide RF isolation for the bias circuitry as an AC floating and reduce loss of RF energy. The stack number should be calculated based on the maximum voltage requirement taking into account the max output power and worse case voltage standing wave ration (VSWR). For example, in GSM Tx mode, the off state branches must handle strong output power up to 35 dBm, hence, as an example

$$P_{watt} = 10^{\frac{35dBm}{10}} \times 0.001 = 3.16W \quad 3.1$$

$$V_{pk} = \sqrt{2 \times P_{watt} \times Z_o} = 17.8V \quad 3.2$$

$$V_{\max} = V_{pk}(1 + \frac{VSWR - 1}{VSWR + 1}) = 30.5V \quad 3.3$$

$$Stack\ height = \frac{V_{\max}}{BV_{dss}} \quad 3.4$$

Where the P_{watt} is the power with unit W, Z_o is the characteristic impedance at antenna port, V_{pk} is the peak voltage, VSWR is the voltage standing wave ratio, and BV_{dss} is the device breakdown voltage. From Equations 3.1 to 3.4, the power in the GSM Tx paths may produce a peak AC voltage up to 30.5V at VSWR 6:1. Which requires 12 stacked NMOSFETs in the GSM Tx paths to handle the high power assuming the breakdown voltage of single MOSFET is 2.5V. The width of MOSFET determines the turn-on resistance of the switch, and it will affect the insertion loss dramatically. The device width for shunt arms can typically be 4 to 5 times smaller than the series device. The determination of R_{gate} is set by the turn on time requirement of the switch. As a rule of thumb, keep the corner frequency below the negative oscillation frequency. The design parameters follow the equations as below

$$Transient\ Rise\ Time\ (\sec) = C_{OXT}(farads) \times R_{gate}\ (ohms) \quad 3.5$$

$$R_{gate} = (\frac{1}{C_{OXT}}) \times (\frac{1}{Corner\ Freq}) \quad 3.6$$

$$C_{OXT} = Gate\ periphery \times Gate\ length \times C_{INV} \quad 3.7$$

Where the Corner Freq= 1/ Transient Rise Time, Gate periphery = gate width * number of fingers. C_{inv} is the inversion capacitance from the C-V plot. Finally the value of the linearized resistor is determined by R_{gate} over stack number. The detailed RF design metrics will be discussed in the next sections.

3.2 RF Switch metrics

RF switch is a key block in FEM. The main specifications of RF switch are IL in different paths, isolation between switched ports, power handling capability and linearity. In general, the specifications of RF T/R switch can be classified in to small signal and large signal specifications. Insertion Loss (IL) and Isolation are two main specifications for small signal while operating power and linearity are main metrics that should be taken into account for large signal part. All the specifications and their impact on transmitter and receiver should be considered. The challenges of designing an antenna switch are twofold. The antenna switch assumes very low insertion loss, and it is also expected to be linear while dealing with watt-level high power signal.

3.2.1 Insertion Loss

The insertion loss of the antenna switch directly affects the overall performance of the front-end because it deals with very high-power signal generated by PA. Most importantly, the IL is proportionally related to on-resistance of the on-state transistors. The on-resistance in series branch can be expressed as below

$$R_{on} = \frac{L}{\mu C_{ox} W (V_{GS} - V_{th})} \qquad 3.8$$

Where L and W are the gate length and gate width of a transistor, respectively, μ is the mobility, C_{OX} is the oxide capacitance, V_{GS} is the voltage difference between the gate and the source of the transistor, and V_{TH} is the threshold voltage.

For the RF switch that consists of only one series FET, when the switch is on, the FET approximates as a series resistor, and any loss which occurs in it when the RF signal passes through is characterized as IL, which is defined as the ratio between output and input RF power or a ratio of the signal level in a test configuration without the switch installed to the signal level with the switch installed. Therefore, the switch's on-state is also called its "IL state" [16]. The IL in Figure 3-3 (a) could be characterized using equation 3.9.

$$IL = -20\log\frac{2R_o}{2R_o + R_{on}} \qquad 3.9$$

Where R_o is load impedance and R_{on} is series on-resistance.

High IL could lead to impact on both transmitters and receivers. For transmitter path, critical path is the loss from power amplifier (PA) to antenna. The IL could directly degrade the effective power added efficiency (PAE) of PA. The effective PAE and loss to antenna is given by,

$$PAE' = PAE \times 10^{\frac{-IL}{10}} \qquad 3.10$$

From equation 3.10, effective PAE is reduced by approximately 1% per 0.1dB of IL. On the other hand, lower IL enables PA drive higher output impedance, which reduces the matching loss and increases the battery life. For receiver path, loss from antenna to LNA directly increases noise figure (NF) and degrades the sensitivity of the

receiver. The minimum sensitivity of LNA is a physical limit, which determines the coverage. Coverage area reduces approximately 1% per 0.1 dB of IL.

3.2.2 Isolation

Due to its intrinsic low mobility compared to the GaAs counterpart, the antenna switch in CMOS technology generally shows higher insertion loss. Even with the antenna switch in the GaAs technology, stacking multiple transistors to handle high power over 30 dBm causes higher insertion loss because the on-resistance, R_{ON}, is increased. Increasing the width of the transistor reduces the insertion loss, but it degrades the isolation performance of the antenna switch because of the increased parasitic capacitance C_{off} as shown in Figure 3-3 (b). Figure 3-4 shows the gate voltage working area as it's in on/off state, in the off regime, the FET parasitic capacitances dominate the RF behavior, FET can be well modeled as a three-terminal capacitor network when biased in deep subthreshold. C_{off} is the net drian to source capacitance with gate floating. Value are typically in the order of 250 fF/mm, generally independent of channel length for fixed D-S spacing.

The simplified AC model in Figure 3-3 (b) is comprised of the gate to source (C_{gs}) and the gate to drain (C_{gd}) overlap (depletion) capacitance as well as the source to drain body

(a) (b)

Figure 3-3 Simplified RF switch transistor model (a) on (b) off

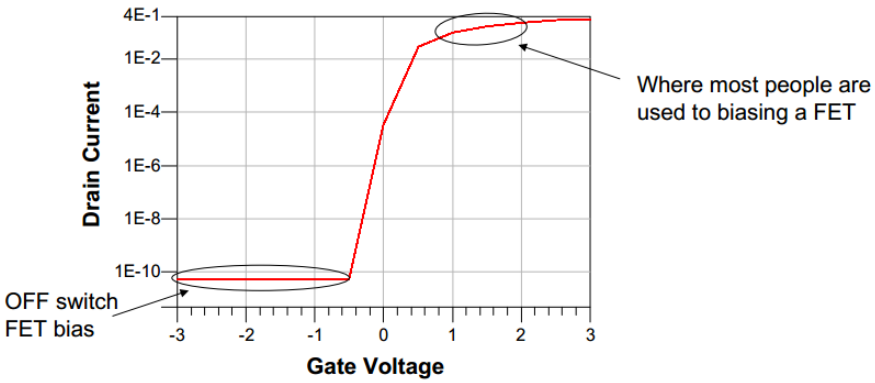


Figure 3-4 Bias voltage of on/off state RF switch

(junction) capacitance (C_{ds}). When the FET is "off", the sum of these capacitances that forms the C_{off} of the device. The large C_{off} in series will degrade the switch insertion loss, so the R_{on} and C_{off} are always the design trade-off. The isolation can expressed as below

$$Iso = -20\log\frac{2R_o}{2R_o + \frac{1}{wC_{off}}} \qquad 3.11$$

3.2.3 Figure of Merit

For the lowest IL, highest isolation and highest power handing capability, we need minimum R_{on} and C_{off} with stacking capability. SOI FETs provide excellent product of R_{on} and C_{off} and permit efficient stacking of nFETs to handle high RF voltage swing. A comparison of the figure of merit (FOM) for the CSOI7RF FETs is shown in

Table 3-1. It can be seen that the CSOI7RF FETs have excellent FOM (250 fs). In addition to the optimum of IL and isolation, 1um thickness buried oxide (BOX), 1KΩ-cm substrate impedance and high implant dosage for TQ trench are used for high linearity.

Table 3-1 Survey of Ron-Coff from several Process technologies

Technology	R_{on} (Ω-mm)	C_{off} (fF/mm)	FoM $R_{on} * C_{off}$ (fs)	Reference
0.5 um pHEMT	1.5	290	435	0
0.15 um pHEMT	1.5	240	360	0
0.18 um SOI	0.77	326	250	0

Switches have onerous power handling requirements. Unlike PAs which drive a high current into a low impedance. Switches must tolerate full power in a 50-ohm system. In many wireless communication applications, the switch is connected to an antenna which can have impedance different from 50 ohms, resulting in even higher voltage. We already discussed the design example at the beginning of this chapter. Table 3-2 summarizes the power handling requirement for different standards as design reference.

Table 3-2 Power handling requirements for different standards [19]

System Standard	Average Power[1]	Peak Power[1]	PAR	V_{PK}	Operating VSWRs	V_{PK} @ VSWR[2]
Two Tone	30	33	3	14.1	n/a	n/a
GSM	33	33	0	14.1	4:1	22.6
EDGE	27	30.2	3.2	10.2	4:1	16.4
CDMA2000	23	28.1	5.1	8.0	4:1	12.9
WCDMA	24	27	3	7.1	4:1	11.3
802.11g	15	22	6.6[3]	4.0	3:1	6.0
VHF 2-way	40	40	0	31.6	8:1	56.2

Note 1- Maximum average power at antenna in a 50-ohm system per the system specification.
Note 2- At angle which produces the highest voltage
Note 3- Assumes crest faction reduction

3.3 1P14T Antenna Switch Design

As shown in Figure 3-5, The block diagram depicts a FEM module with Quad-band GSM/GPRS/EDGE, Dual-Band TD-SCDMA- TDD LTE Band 39 and 14 TRx Switch Ports. It really a big challenge to realize a single pole multiple throw switch with good insertion loss, isolation and power handling capability. The 1P14T antenna switch design is introduced in this section.

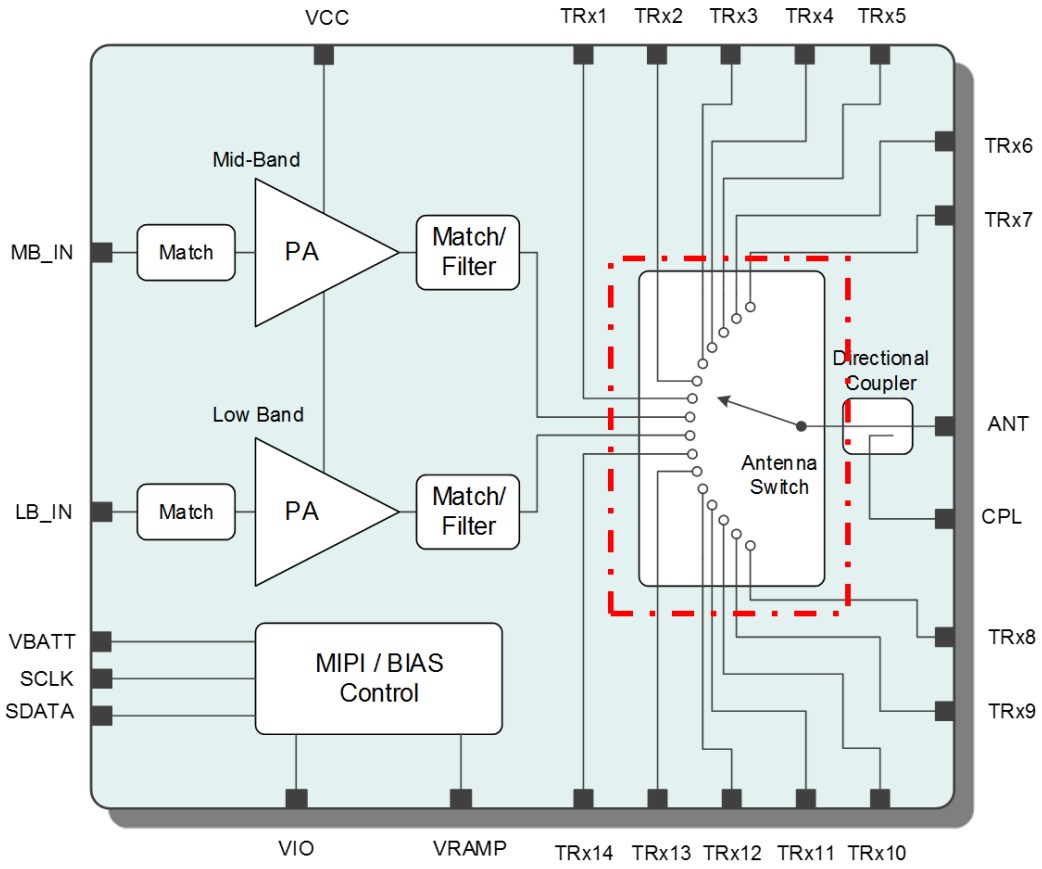


Figure 3-5 Block diagram of a FEM with Quad-band GSM/GPRS/EDGE- Dual-Band TD-SCDMA- TDD LTE Band 39 and 14 TRx Switch Ports

The switch topology is shown as Figure 3-6, it consists of 14 TRx ports, The Branch SW1/SW2 are series connected with High Band (HB) PA and Low Band (LB) PA, which has 12 stacks of series branch and shunt branch, respectively. For the common block SW3/4/19/20, they are series common branch with 9 stacks. For the following SP3T and SP4T, the stack number is 6, that means when one of the TRX branch is on, the voltage of the shunt path is over 6 transistor stacks, since TRx port power handling requirement is much lower than that in GSM Tx mode, we can design the topology like this. For the TRX part, when one of the TRx branch is on, the other branches "SW" is off and "SS" is on, the received RF power will be over 6 stacks. And the PA Tx path has 12 stacks, that's high enough to protect the Tx path. When the Tx path is on, the 12 stacks "SS1" and "SS2" should be off to endure output power, regarding to TRx path, the total off state transistor number is 15. A combos-switch using sharing stack SW3/4/19/20 are used to reduce circuit

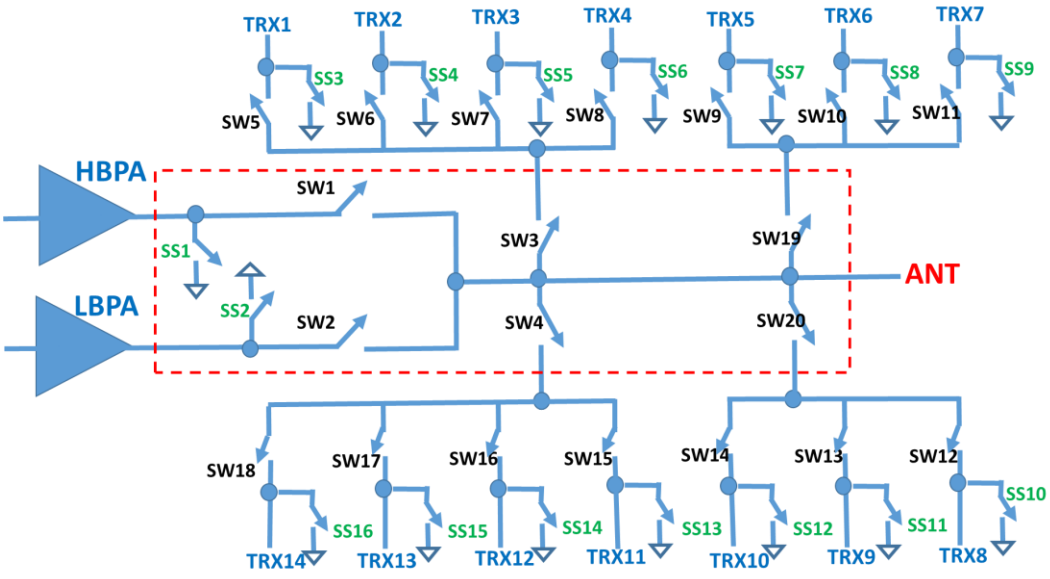


Figure 3-6 1P14T Switch topology of a FEM with Quad-band GSM/GPRS/EDGE- Dual-Band TD-SCDMA- TDD LTE Band 39 and 14 TRx Switch Ports

area and parasitic capacitance, thus improve linearity in GSM Tx modes. However, in TRx mode, the common block does degrade IL from Antenna to TRx port. A design trade-off can be found in [20].

When a 2.5V supply voltage is applied to turn on FETs in one of the series stack, another -2.5V bias is used to turn off FETs in other series stacks. The SW1/SW2 are optimized as 3.6um, while SS1 and SS2 are 1mm. The SW3/4//9/20 are with the same width as 3.6mm. Regarding to SP3T and SP4T, the series branch width is 3.2mm and shunt branch width is 1mm.

Although we can get a math analysis with respect to insertion loss and isolation by PDK models, but in the real die application, the performance is actually affected by the layout significantly. Consider the single branch layout as shown in Figure 3-7, different series and shunt branch positions are played. Figure 3-8 shows Insertion loss with different layout of single switch branch using ideal schematic, pex c+CC, pex r+c+cc respectively in cadence simulation, we can find that the version 2 layout has optimum insertion loss due to the shortest metal routing path. The 3D simulation HFSS model as shown in Figure 3-9 is further utilized to do a full EM analysis of entire switch, the extracted S parameter file from EM model can fully characterize the microwave RF switch network. Then, co-simulation with ADS as shown in Figure 3-10 is performed as a test bench to get more accurate result. The S parameter file of active MOS with on/off state of each branch is extracted as well in Figure 3-11. Since this switch is not fully designed on the die, the BEOL of laminate will be used as the interconnect for switch to antenna port routing. As shown in Figure 3-12, an LC equivalent circuit can represent such interconnect EM effect.

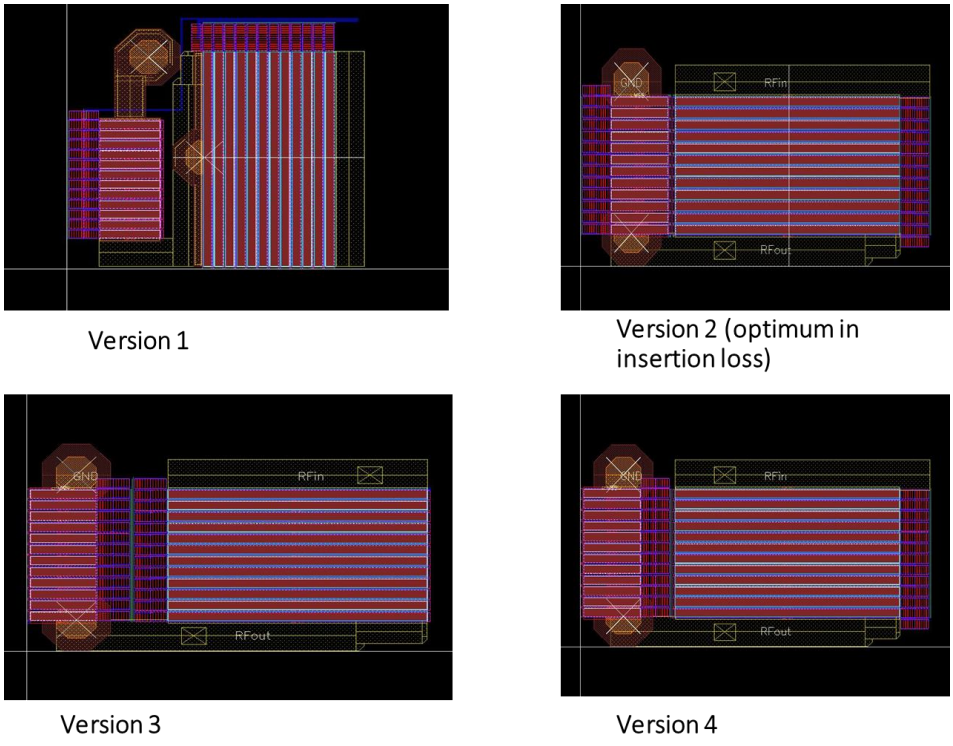


Figure 3-7 Four types of switch layout in single branch

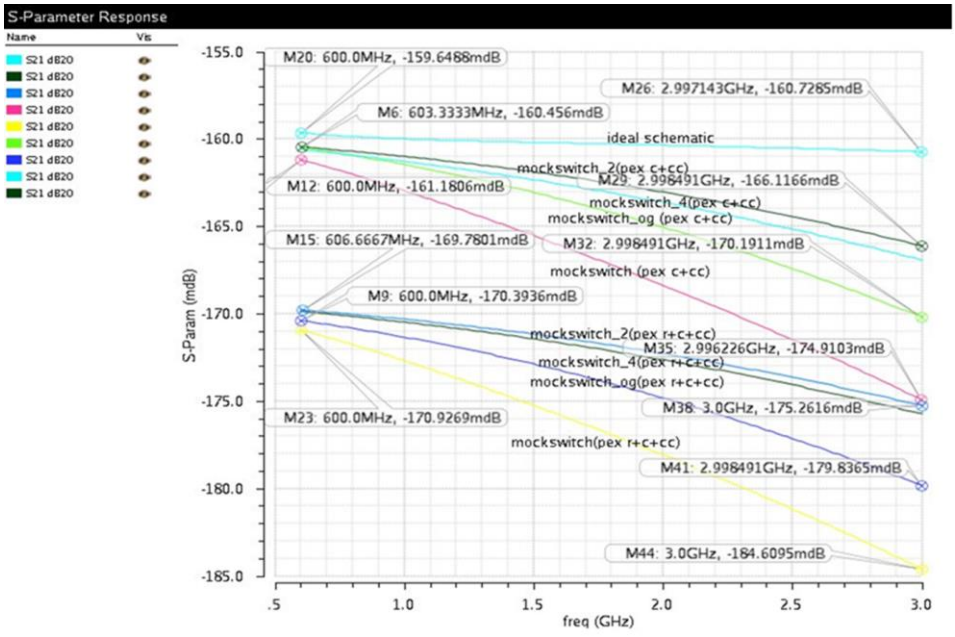


Figure 3-8 Insertion loss with different layout of single switch branch using ideal schematic, cadence pex c+CC, pex r+c+cc respectively.

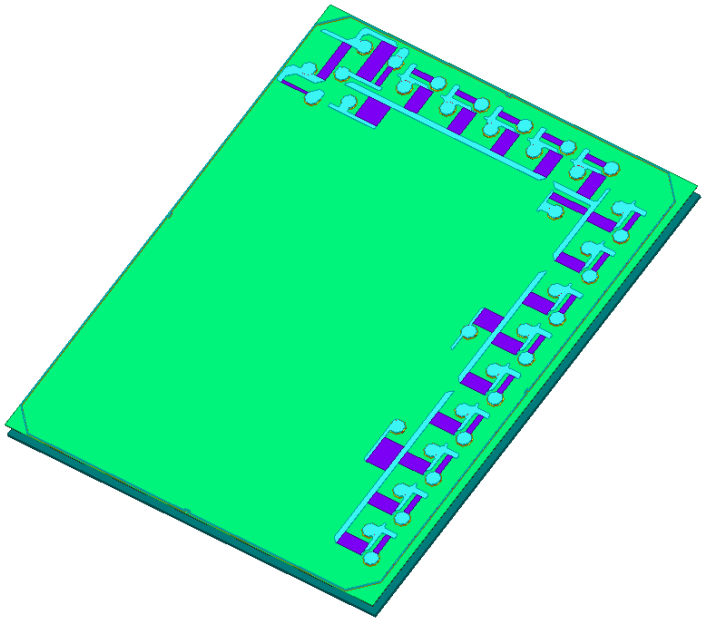


Figure 3-9 HFSS EM model of 1P14T antenna switch

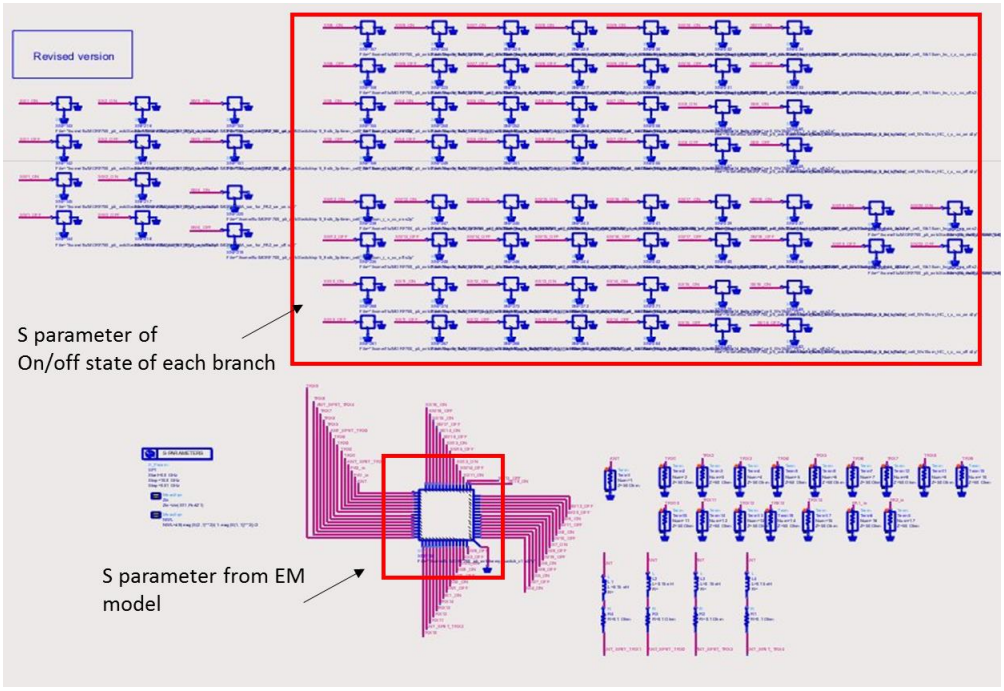


Figure 3-10 ADS co-simulation test bench with embedded EM model

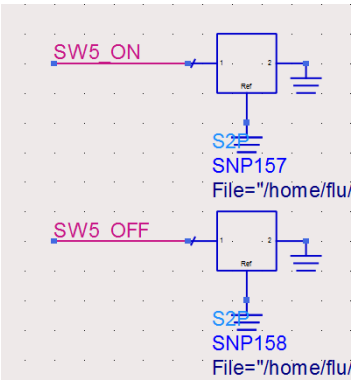


Figure 3-11 Extracted S parameter file with on/off state

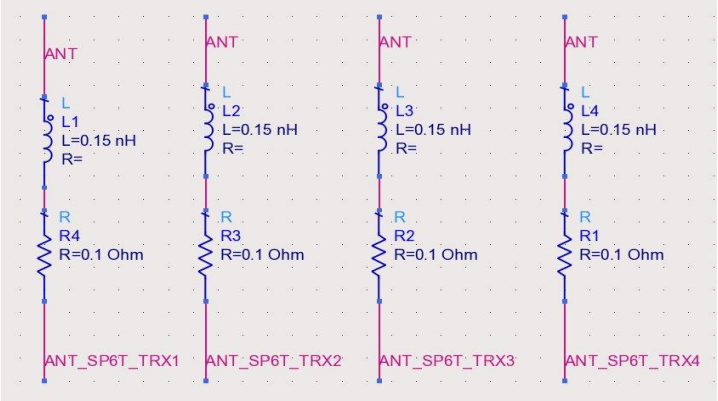
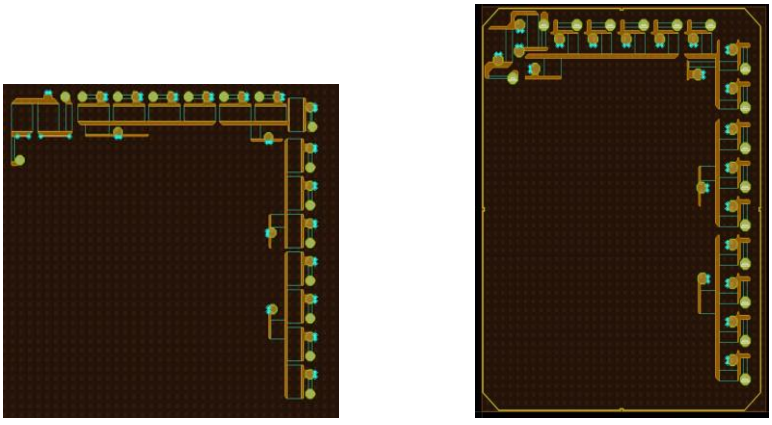


Figure 3-12 Switch port to Antenna port connection with equivalent LC circuit.



(a) (b)

Figure 3-13 1P14T switch layout design (a) old version (b) new version

In order to shown the discrepancy of different layout, Figure 3-13 shows two different layouts of entire designed 1P14T switch, although each branch has the same width and length, but compared to the old version (a), new version (b) put one branch from horizontal direction to vertical direction.

The simulation frequency is swept from 700 MHz to 2.7 GHz, covering from Low Band to High Band, We can clearly see that, with the same FET size and topology, but with different layout, somehow, there is a resonate frequency near 8 GHz which cause a notch shown in S21 curve of old version, thus drag down the insertion loss at high end. The old version is about 0.3 dB short of improved one, at the same time, with improved insertion loss, the isolation improved as well. Figure 3-14 and Figure 3-15 shows the simulation details.

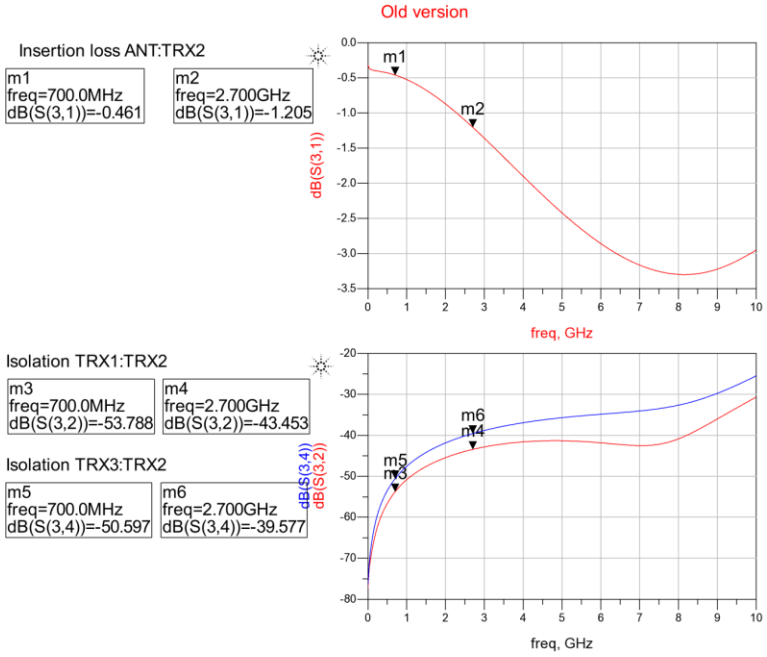


Figure 3-14 Simulated insertion loss and isolation of old version layout

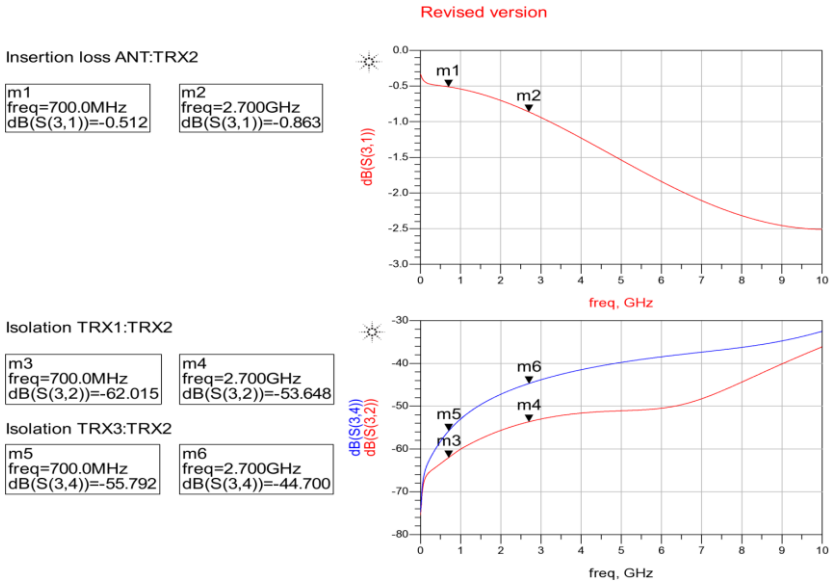


Figure 3-15 Simulated insertion loss and isolation of new version layout

3.4 HB/MB/LB Switch in MMMB FEM

Apart from antenna switch, the switches used in Figure 1-3 block diagram are shown in Figure 3-16, Figure 3-17, Figure 3-18 with detailed design topology, each with different band selection. Since this MMMB FEM targets the application of 4G LTE frequency-division duplexing (FDD), and time division duplexing (TDD), WCDMA, TD-SCDMA, the power requirement is not as stringent as GSM, each branch in LB/MB/HB features a 7 stacks FETs with 3.6mm width in series and 1mm in shunt. Since HB/MB/LB PAs are separated for each other and they not connected to antenna directly, each band are grouped into separate topology, the specific band number assignment can be checked in 3GPP Protocol. These switches follow the same design methodology, since the switch will be simulated along with PA output matching network, the performance analysis will be done together with PA.

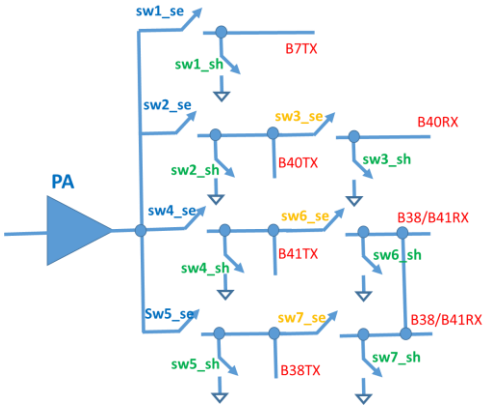


Figure 3-16 High band switch designed in the MMMB FEM

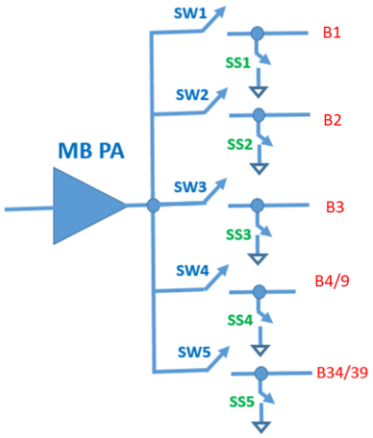


Figure 3-17 Middle band switch designed in the MMMB FEM

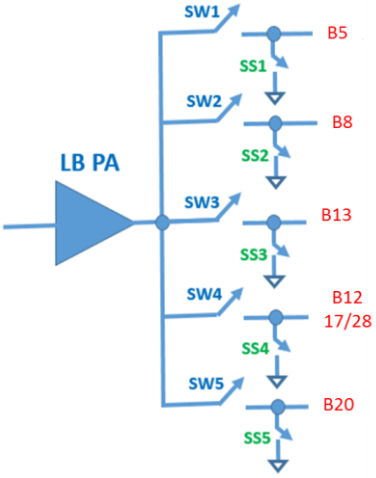


Figure 3-18 Low band switch designed in the MMMB FEM

Chapter 4 Diplexer

4.1 Diplexer motivation

Mobile operators must continuously pursue cost-effective and efficient solution to meet high data rate demands for their customers. Limited spectrum allocation and non-contiguous spectrum blocks continue to pose challenges for mobile operators supporting large data uploads and downloads across their networks. With the increase in video and social media content, the challenges have increased exponentially. Carrier Aggregation (CA) [21] is a solution that many mobile operators worldwide have begun adopting to address these challenges in the mobile ecosystem. The carrier aggregation is a technique used to combine multiple LTE component carriers across the available spectrum to 1) support wider bandwidth signals 2) Increase data rates, 3) Improve network performance. Carrier aggregation allows increased data rates and improved network performance in the uplink, downlink, or both. It also enables aggregation of FDD/TDD, as well as licensed and unlicensed carrier spectrum. In order to implement the carrier aggregation with large frequency separations between two bands (For example, one is low band, and another one is mid band) A diplexer is inserted into the block after the Antenna.

4.2 Diplexer methodology

Diplexer design is actually a filter design, and the essence to filter design by direct synthesis is the specification of transmission zeros (TZs) and understanding their influence on the filter response [22] . With the modern method refined in the 1950s, specified filter parameters include the type of approximation, such as Butterworth or Chebyshev, the

passband frequencies, the termination impedance, and the order of the filter. The TZs are fixed by the filter type.

Consider the fourth-order lowpass filter schematic in Figure 4-1 (a), also shown as open or closed switches, are the transmission characteristic of the element at DC and at the infinite frequency (Infinity). At DC, each of the inductors pass signal and each of the capacitor is open, therefore do not shunt signal to ground. At infinity, each inductor is open and each capacitor shunts signal to ground. This filter has no TZ at DC and it has four TZs at infinity. Consider the lowpass filter in Figure 4-1 (b). The anti-resonant series branch to ground produces a finite-frequency transmission zero (FTZ) at the resonant frequency. At infinity, the shunt inductor is open, and L1 and L3 can be equivalent as one inductor, therefore, this filter has no TZs at DC, two TZs at infinity and one FTZ which is placed above the passband.

The degree of a filter is the order of the transducer function polynominal, H(S). Each TZ at DC adds one degree to the filter transfer function. In addition, each TZ at infinity adds one degree to the filter. Each finite frequency TZ adds two degrees. And Each TZ adds approximately 6 dB per octave in the pass-stop band transition region.

A typical diplexer block used in FEM is demonstrated as Figure 4-2, it consists of three ports, two inputs with LB, MB/HB for each, and the output is connected to antenna. The diplexer provides the capability to separate two different frequency bands in input path and combines them in output path. In addition, diplexer is normally made by passive element, thus, it is reciprocal. The specification is as shown in Table 4-1, the LB covers from 699 MHz and 960 MHz whereas the MB/HB covers from 1427.9 MHz to 2690 MHz. We can

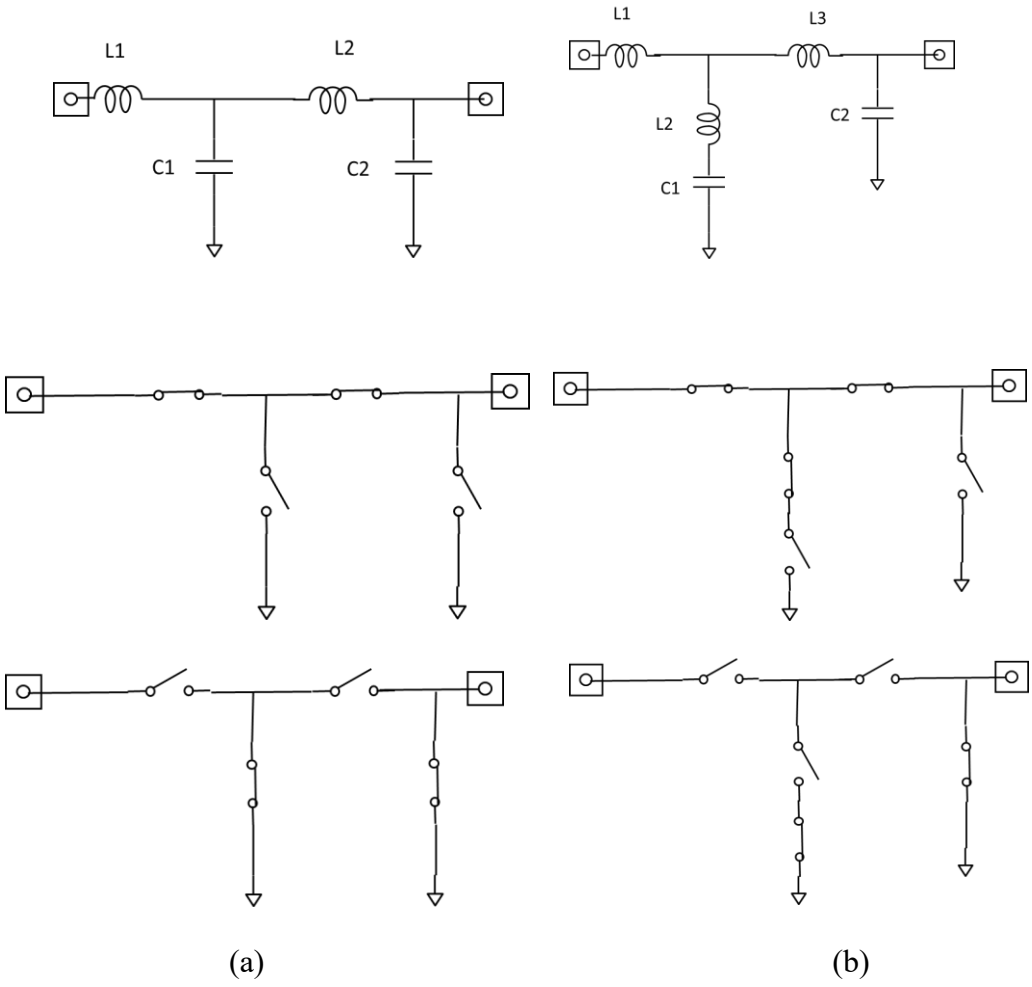


Figure 4-1 (a) All pole lowpass filter showing DC and infinite TZs and (b) a generalized lowpass with also a TZ at finite frequency.

see that the Insertion Loss spec is quite strict that requires a very high Q network, and the attenuation in each band is related to filter order. From the perspective of design principle, the higher attenuation in the stop band, the more transmission zeros, therefore, more passive elements are required, which will induce more loss. Then the insertion loss and attenuation became a design trade-off. Moreover, a high performance filter will benefit from the high Q elements.

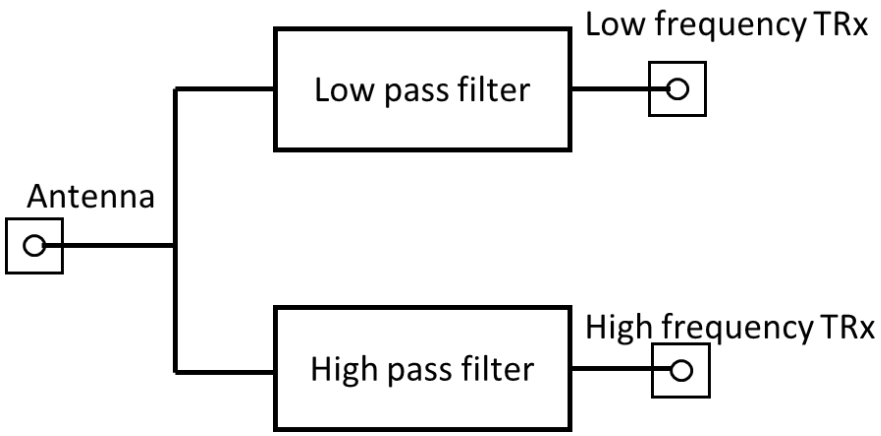


Figure 4-2 Diplexer block diagram covering FEM LB/MB/HB

Table 4-1 Diplexer design specifications

Diplexer Parameter	Specification Min	Typ	Max		Condition (25°C NTC, -20° to +85°C ETC)
Insertion Loss		0.3	0.4	dB	699-960 MHz, ETC
		0.4	0.5	dB	1710-2690MHz, ETC
		0.4	0.7	dB	1427.9-2690 MHz, ETC
Low Band Attenuation	30	35		dB	1710-2690MHz, ETC
	30	32		dB	1427.9-2690 MHz, ETC
Mid/High Band Attenuation	25	30		dB	699-960 MHz, ETC
VSWR LB		1.2:1	1.8:1		699-960 MHz, ETC
MB/HB		1.5:1	1.8:1		1427.9-2690 MHz, ETC
ESD	8000			V	HBM at ANT_RFOUT

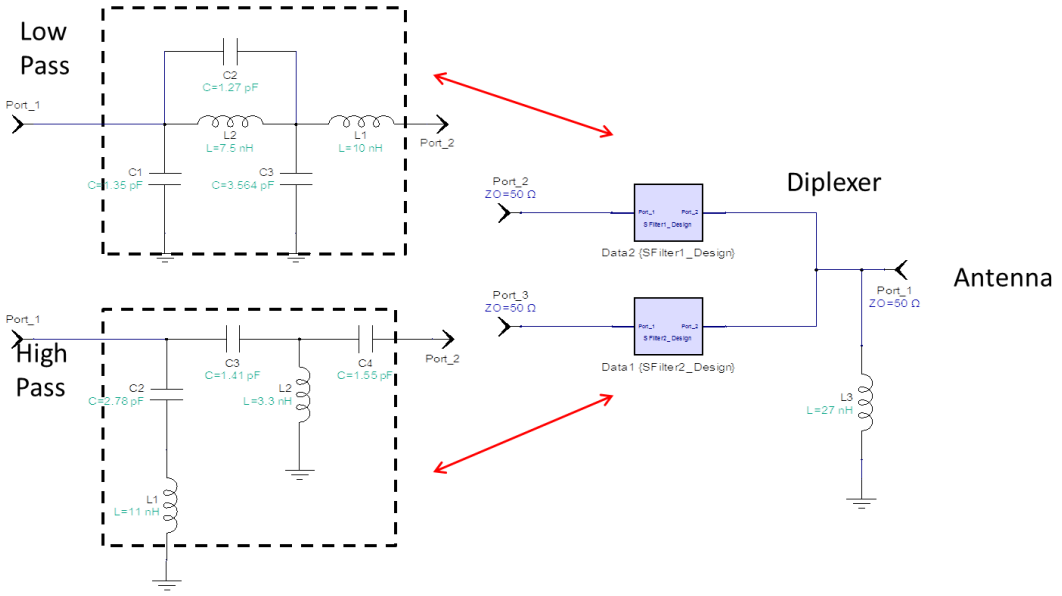
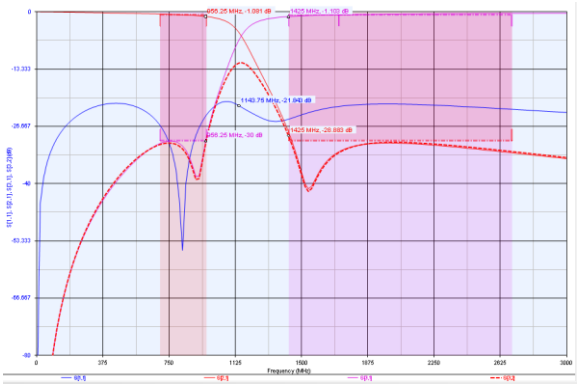


Figure 4-3 Diplexer design detailed topology

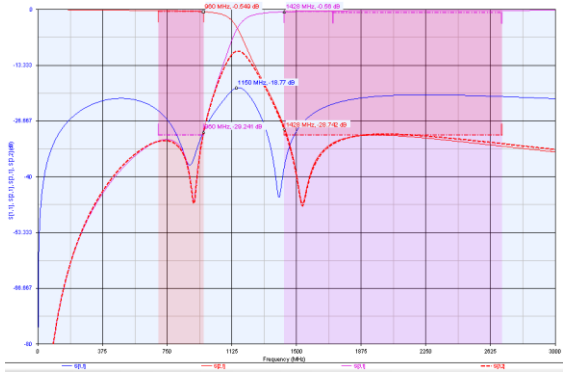
A detailed diplexer topology is designed by discrete inductors and capacitors as shown in Figure 4-3.

- For the lowpass filter, 3 capacitors and 2 inductors are used to minimize the insertion loss, 0 TZ(transmission zero) @ DC, 2 TZs @ infinity, in addition, 1 FTZ(finite transmission zero) helps to increase the out of band attenuation.
- For the highpass filter, 3 capacitors and 2 inductors are used to minimize the insertion loss, 3 TZs (transmission zero) @ DC, 0 TZ @ infinity, in addition, 1 FTZ(finite transmission zero) helps to increase the out of band attenuation.

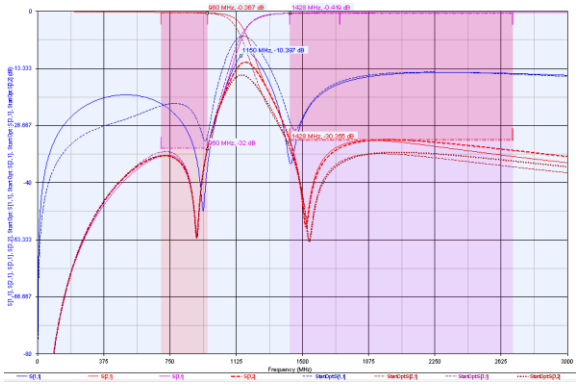
The Q value of capacitor is high enough up to few hundreds, so actually the inductor limits the network loss performance. The inductor model with Q value is included in the test bench to evaluate the insertion loss. As shown in Figure 4-4, the spec mask is displayed and the diplexer insertion loss differs from Q factor of inductor. The passive inductor is possible made in the metal layer of laminate, which has better Q factor than on-chip



(a)



(b)



(c)

Figure 4-4 S parameter curve of diplexer (a) with inductor Q value 20 (b) with inductor Q value 40 (c) with inductor Q value 60

inductor but may be worse than the discrete one. An evaluation of inductor in laminate is conducted. As depicted in Figure 4-5, the laminate features 6-layers high conductivity metal line where a spiral inductor could be produced, then 3D EM model in HFSS is simulated as illustrated in Figure 4-6, the inductor value and Q factor can be analyzed as shown Figure 4-7. The result is summarized in Table 4-2.

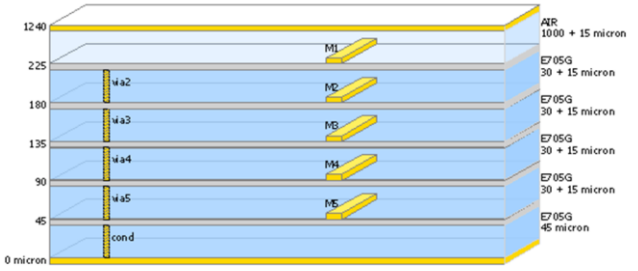


Figure 4-5 Cross-section view of back end of line in Laminate

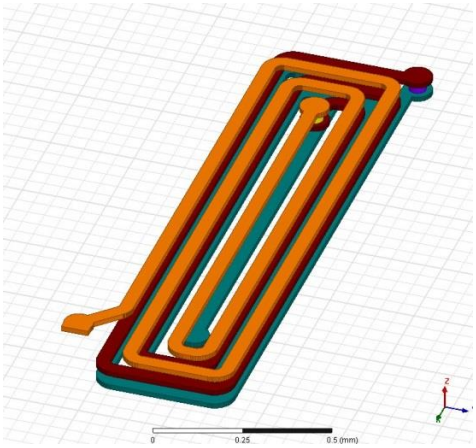
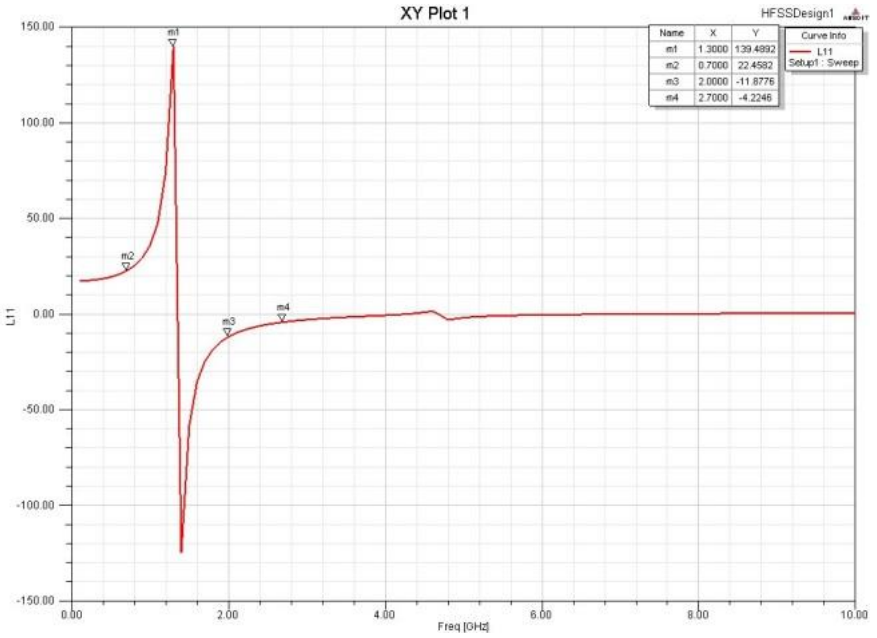
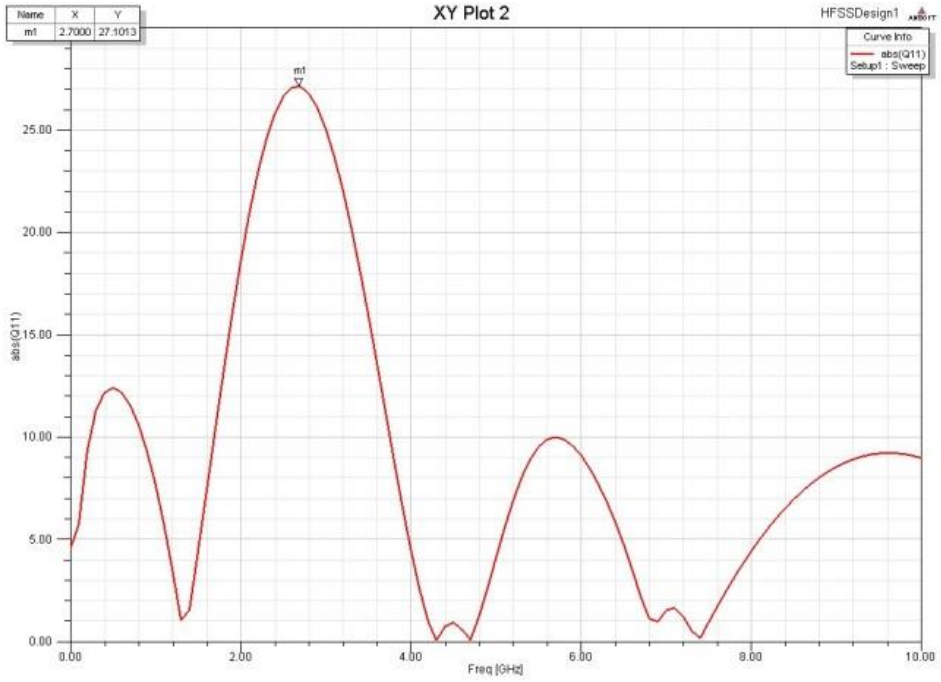


Figure 4-6 3D View of spiral inductor produced in laminate



(a)



(b)

Figure 4-7 (a) Simulated inductor value over frequency (b) Simulated Q factor over frequency

Table 4-2 Simulated laminate inductor value

	Freq (GHz)			Resonant Freq (GHz)
	0.7	2	2.7	
L (nH)	22.4	-11.8	-4.2	1.3

With respect to the simulation result from HFSS, we can see that as the inductor value goes up to 22.4 nH, the resonant frequency goes below 1.3 GHz, it's not suitable for diplexer design, moreover, the Q factor is too low to design the filter.

To meet the IL requirement, high Q inductor is preferred. A high out of band attenuation will compromise the insertion loss, e.g. if we drag the FTZ far from the pass band, the insertion loss in band will improve, but the out of band falling edge of S parameter curve will touch attenuation limit . One way to solve it is to add more TZ to increase the attenuation, however, the added components will degrade insertion loss more. In this design, Murata LQW high Q inductor has been chosen to implement design and Capacitor could use on-die one to save cost and area. The Table 4-3 and Table 4-4 summarize the inductor and capacitor value used in the topology as shown in Figure 4-3.

Table 4-3 Diplexer capacitor value table

Lowpass.C1	1.35 pF
Lowpass.C2	1.27 pF
Lowpass.C3	3.56 pF
Hihgpass.C2	2.78 pF
Hihgpass.C3	1.141 pF
Hihgpass.C4	1.55 pF

Table 4-4 Diplexer inductor value table

Lowpass.L1	LQW04AN10NH00 10nH
Lowpass.L2	LQW04AN7N5C00 7.5nH
Highpass.L1	LQW04AN11NH00 11nH
Highpass.L2	LQW04AN3N3C00 3.3nH
Antenna. L3	LQW04AN27NH00 27nH

The EM model is demonstrated as Figure 4-8, the inductor footprint layout is placed on the laminate, which occupies the most area. The S parameter could be extracted and placed in the ADS test bench as shown in Figure 4-9. The insertion loss and attenuation could be obtained from Figure 4-10, the diplexer is fine tuned to achieve a balanced performance. Compared to the commercial discrete diplexer, the IL of low pass is 0.18 dB short of spec, and IL of high pass is 0.08 dB short of spec, however, the laminate- based diplexer provides the design flexibility as a full integration.

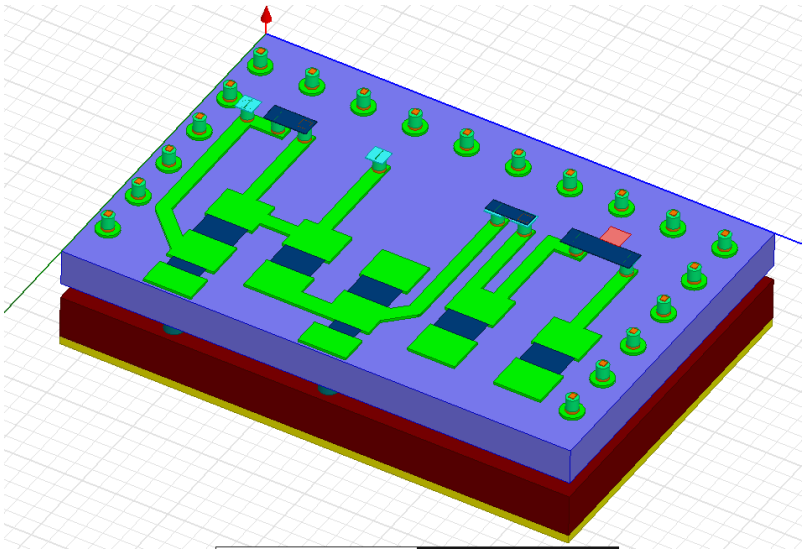


Figure 4-8 EM model of diplexer design based on the laminate

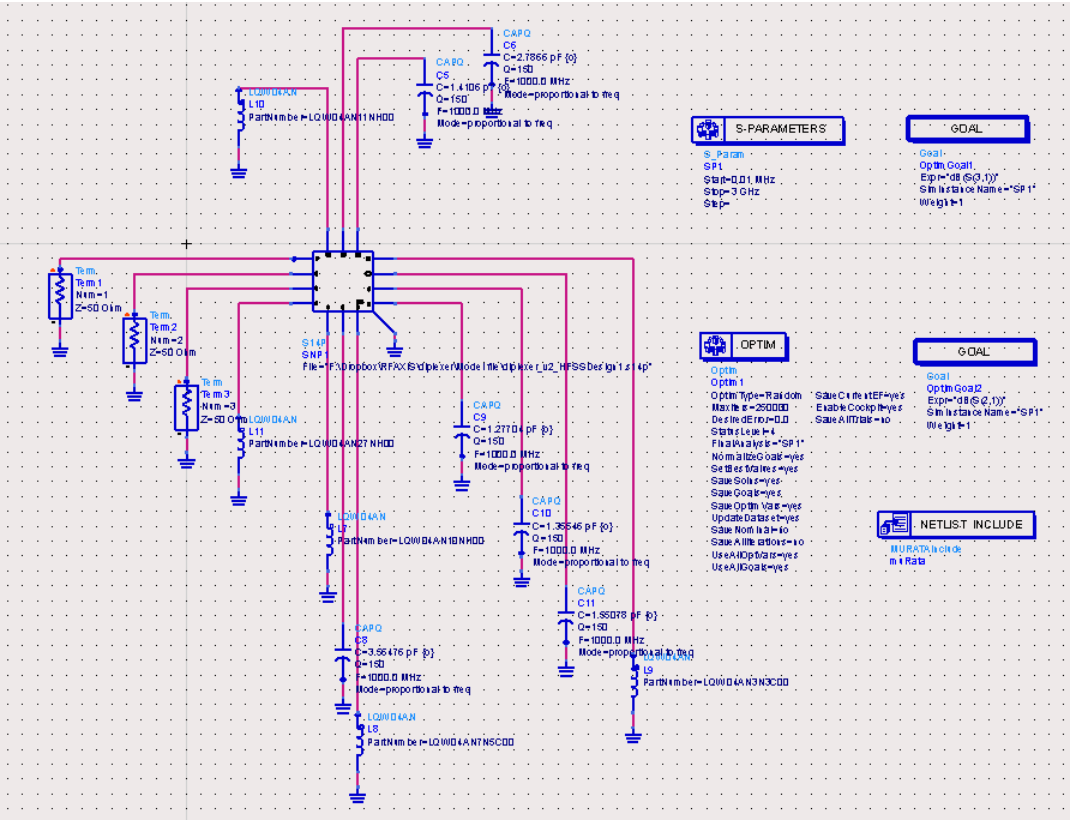


Figure 4-9 Test bench of diplexer in ADS

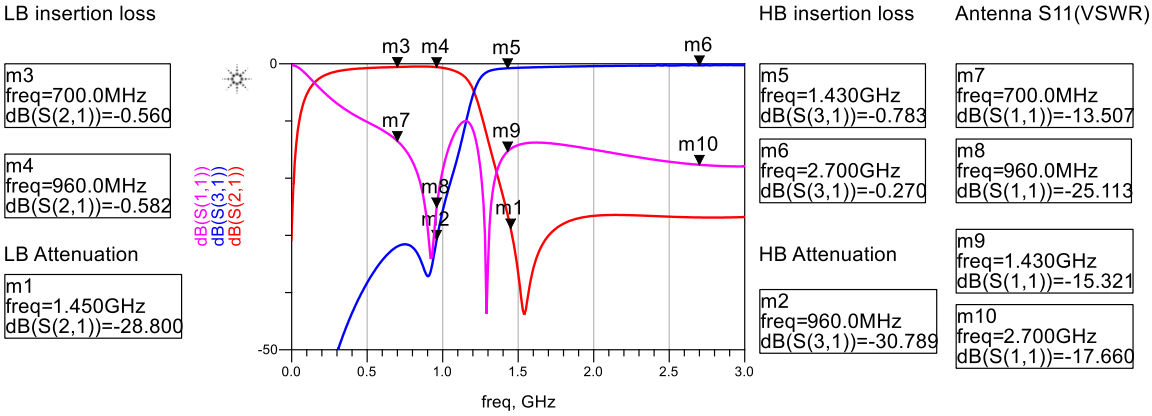


Figure 4-10Diplexer S parameter curve based on EM simulation

Chapter 5 Power Amplifier

5.1 Introduction

Power amplifier (PAs) is the key part in a front-end module, to some extent, it's most important to determine the system performance, also very difficult to design to achieve the specification trade-off. Mostly, the high performance PA is designed by HBT, BiCMOS, pHEMT which feature a high mobility and less parasitic technology. Probably PAs are the last module that has not been fully integrated on silicon. While CMOS has been implemented to many power amplifier applications such as Bluetooth, CMOS PA for wireless handsets is still limited by the technology nature. On the other hand, in high volume production, the wafer costs for CMOS are low and continually declining. There is large capacity available from foundries, providing flexibility to easily follow up and down market trends. From a design perspective, non- PA components can be readily integrated with PA, if wish. The availability of millions of transistors, and different types of transistors, allows the addition of performance enhancing functionality, including complex bias circuitry and well established ESD design procedures. Finally, CMOS allows integration of on-chip calibration and self-test circuitry that is not possible in III-V technologies [23]. However, there are shortcomings in designing CMOS PAs: Low breakdown voltage, low device gain, linearity issues, design support issues, RF model inaccuracies, lack of high voltage capacitors. At the same time, GaAs technologies have become more feature rich with the addition FETs to most commercial HBT processes, allowing III-V designers to be able to address some market requirements unattainable with bipolar only technology.

Nevertheless, because of the low cost and the potential for high-density and functionality, CMOS has long become an attractive technology for RF power amplification.

In 1997, the first CMOS RF PA that could provide 1-W of output power from a single 2.5-V DC supply to a 50-Ohm load [24]. The amplifier was designed in a standard 0.8-um CMOS technology working from 824-MHz to 849-MHz, Power Added Efficiency (PAE) of 42%. Although this PA was built not suitable for full integration, for the first time, the design demonstrated the capability of CMOS technology which is able to provide efficient RF signal power amplification at 800~900-MHz in low-voltage applications. Ever since then, there have been quite a few publications on CMOS RF PAs [25] . However, same as [24], the major obstacle that prevents them from being fully integrated in one chip is their impedance transformation networks which require off-chip components such as inductors, capacitors, or bond-wires. Driven by the demands from marketing, great efforts have been contributed to the design of low-loss, fully integrated, on-chip impedance matching networks [26][27][28][29]. Besides integration, the linearity-efficiency trade-off is another issue that the RF PA designers have been trying to solve for a long time. For transceivers in communication system with non-constant envelope modulation schemes, such as Enhanced Data rates for the GSM Evolution (EDGE), Universal Mobile Telecommunication System (UMTS), etc. the linearity of a PA is of fundamental importance. Moreover, higher efficiency always means longer battery lifetime and less heat dissipation worries. Unfortunately, a conventional PA can only achieve its peak efficiency near the maximum rated power. As the drive power is backed off from this point considering the peak to average ratio (PAR) of a specific modulation, a linear PA's

efficiency drops significantly and the heat dissipation is subject to increase [30]. Linearization as well as efficiency enhancement techniques are possible solutions to tackle this trade-off. And for applications that have stringent linearity requirements, it makes good sense to use a linear PA together with an efficiency enhancement technique such as envelope tracking and digital pre-distortion (DPD).

Multi-band phones are already in existence covering from 2G to 4G modes and bands, it increase the difficulties of integration. In current wireless market, exceptional wireless smartphone growth drives higher data rate, more frequency bands and highly integrated FEM is required. Consequently, more challenging specifications are required for handset FEM design, a MMMB PA designed in a single die single chip will help to meet the demands placed on the future smartphones.

5.2 PA fundamentals

5.2.1 Conjugate match vs Loadline match

As we talk about the RF system, we have to talk about transmission line, 50-ohm standard are sound and well proven to be a common choice. Regarding to two ports network. As shown in Figure 5-1, a transistor is represented as a two-port s-parameter matrix. The input and output impedance, or reflection coefficient, presented to the transistor, can be tuned by the matching network. Γs and Γ_L at the input and output reference plane are restricted within one in magnitude. We can characterize it with the equation as below:

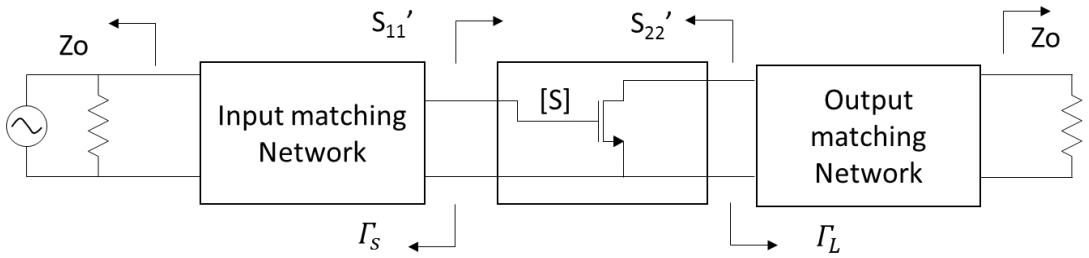


Figure 5-1 Schematic for 2 port RF network

Input match

$$S_{11}' = S_{11} + \frac{S_{21} \bullet S_{12} \bullet \Gamma_L}{1 - S_{22} \bullet \Gamma_L} \qquad 5.1$$

Output match

$$S_{22}' = S_{22} + \frac{S_{21} \bullet S_{12} \bullet \Gamma_s}{1 - S_{11} \bullet \Gamma_s} \qquad 5.2$$

$$S_{22}' = \Gamma_L^* \quad \text{and} \quad S_{11}' = \Gamma_s^* \qquad 5.3$$

Theoretically, without considering other physical limitation, one can set the equation as above for a conjugate match. To deliver the maximum power into an external load when the load resistance is set equal to the real part of generator impedance as conjugate match, but it is too ideal to be true. The basic conjugate match theory applies in a completely unrestricted case where currents and voltages at the generator terminals are unbounded by physical constraints. The loadline is a real word compromise.

For example, a case where the current generator can supply a maximum limiting current of 1A, and has an output resistance of 100 ohms as shown in Figure 5-2. Applying the conjugate match theory, a load of 100ohm would be selected for max power transfer. However, if the current generator is replaced by a transistor, it is most likely that this would exceed the voltage rating of the device. There is an additional limitation of the transistor voltage swing, that is limited by the available DC supply. With Vmax limitation, the device

will show a limiting action at a current considerably lower than its physical maximum of Imax, this is clearly undesirable situation, the full capacity of power is wasted. In order to utilize the maximum current and voltage swing of the transistor, an appropriate value of load resistance would be selected as the "loadline" match, R_{opt}. And it can be expressed as

$$R_{opt} = V_{\max} / I_{\max} \qquad 5.4$$

Figure 5-3 shows how optimum load impedance can be obtained by considering both of the device's voltage and current limitations. Where it has been assumed that $R_{gen} >> R_{opt}$, if R_{gen} is taken into account, it would be necessary to solve the equation.

$$\frac{R_{gen} \bullet R_{opt}}{R_{gen} + R_{opt}} = \frac{V_{\max}}{I_{\max}} \qquad 5.5$$

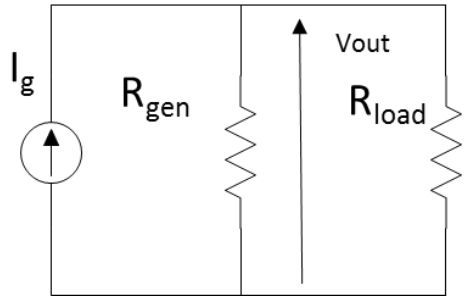


Figure 5-2 Generator equivalent circuit

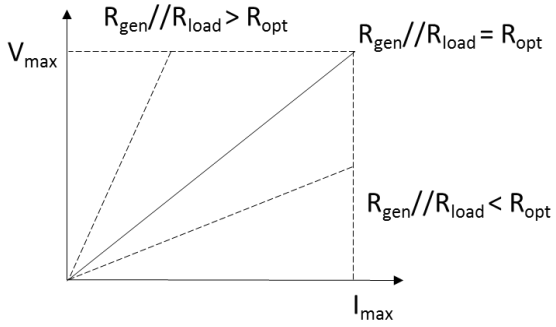


Figure 5-3 Loadline matching

5.2.2 Stability factor

The stability of an amplifier, is a very important consideration in a design and can be determined from the S parameter, the matching networks, and the terminations. In a two-port network, oscillations are possible when either the input or output port presents a negative resistance. Given a two by two scattering matrix between the input and measurement ports, The K factor or Rollett's stability factor is given by

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2 \bullet |S_{21}| \bullet |S_{12}|} \qquad 5.6$$

$$D = S_{11} \bullet S_{22} - S_{12} \bullet S_{21} \qquad 5.7$$

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |D|^2 \qquad 5.8$$

The necessary and sufficient conditions for unconditional stability factor K is greater than unity and the stability measure B is positive. It should be noted that the stability analysis based on stability factor K has some limitations. It assumes the linear behavior of the PA, whereas the PA may work in nonlinear conditions. The distinctive feature of large-signal S-parameters is that they are not only a function of frequency, but they also depend on the output power levels. Therefore, it is possible to perform a stability analysis of the PA with stability factor K at different power levels. Devices with high K-factors tend to have low gain, and some extra gain can be retrieved by allowing positive feedback around the device, while keeping the k-factor above unity.

5.2.3 Output Power

In most cases, the output power is the power from PA delivering to the 50 ohm antenna load. If a targeted in-band sinusoidal wave is considered, then the output power can be expressed as

$$P_{out} = \frac{1}{2}\frac{V_{out}^2}{R_{load}} \qquad 5.9$$

Where V_{out} is the amplitude of output signal and R_L is the load impedance. In modern communication, the output signal is normal modulated categorized into with different peak to average ratio and the signal envelop vary with time. So the average output power can be expressed as

$$\overline{P_{out}} = \int_0^\infty P \bullet \varphi(P) dP \qquad 5.10$$

Where φ(P) is the probability of the PA's output power with different level and it is determined by the probability distribution of the input signal and modulation method. To make the statistic become realistic, one way is to integrate trainsient ouput power over time. For cellphone application, the PA inside will not output power at the maximum allowable rate all the time, in a communication system, the power control algorithm will limit it, in other words, the closer handset equipment to base station, the smaller power needed. So it means the PA will not work in the best scenario with best efficiency.

5.2.4 Power Gain

The power gain of a two-port network, amplifier in this case is defined as the ratio of the output power to input power. For a two-port network, the power gain can be defined in several ways. The three commonly used definitions are transducer power gain (G_T) or

simply power gain, maximum available power gain （G_A), and available power gain (G_P). Their definitions are given as below:

$$G_T = \frac{\text{power delivered to the load}}{\text{power available from the source}} = \frac{P_L}{P_{avs}}$$
$$G_A = \frac{\text{power available from the network}}{\text{power available from the source}} = \frac{P_N}{P_{avs}} \qquad 5.11$$
$$G_P = \frac{\text{power delivered to the load}}{\text{power delivered to the network}} = \frac{P_L}{P_{in}}$$

The power available from the network is the maximum output power we can get when the output is perfect matching, and power available from the source is maximum power we can get from the source when the input matching is perfect. Normally, we will use G_T as the calculation method.

5.2.5 Input/Output VSWR

The input and output VSWR values are commonly used to characterize an amplifier's circuit match to source and load impedance (usually 50 ohm**)**. Mismatch between 50 and the amplifier's input, and the amplifier's output are measured as input and output reflection coefficients. The voltage reflection coefficient is related to VSWR as given in equation 5.12

$$R_L = -10\log\frac{P_R}{P_{in}} = -10\log(\frac{VSWR-1}{VSWR+1})^2 \qquad 5.12$$

5.2.6 Power added efficiency

For power amplifiers, power added efficiency is defined as the ratio between RF power portion that the PA adds to the input power and DC power consumed. It is usual metric to evaluate efficiency because it is a more complete metric of a PA efficiency performance.

The PAE takes into account the effect of the power gain and therefore penalizes PA designs with poor gain. Drain efficiency represents the power delivered from the drain of the active device to the power supply, and is usually used to evaluate the efficiency of the power gain stage of a PA.

$$\text{PAE}=\frac{\text{output signal power -input signal power}}{\text{DC power}}=\frac{P_o-P_{in}}{P_{DC}} \\ =\frac{P_o}{P_{DC}}(1-\frac{1}{G})=\eta_D(1-\frac{1}{G}) \qquad 5.13$$

Where G (= P_o/Pin) is the amplifier gain.

5.2.7 EVM

The signal with complex wideband modulation like quadrature amplitude modulation (QAM) signal scheme demands PAs with high linearity, due to the inherent high peak-to-average ratio, Error Vector Magnitude (EVM) is a parameter used to quantify the performance of a system with phase-shift modulation. It measures the deviation of the demodulated received symbol (I, Q), from the original transmitted data symbol (I0, Q0). A signal sent by an ideal transmitter would have all constellation points precisely at the ideal locations, however, various imperfections in the implementation (such as LO leakage, low image rejection ratio, phase noise, etc.) cause the actual constellation points to deviate from the ideal. Figure 5-4 shows the error vector magnitude concept in a 16 QAM constellation.

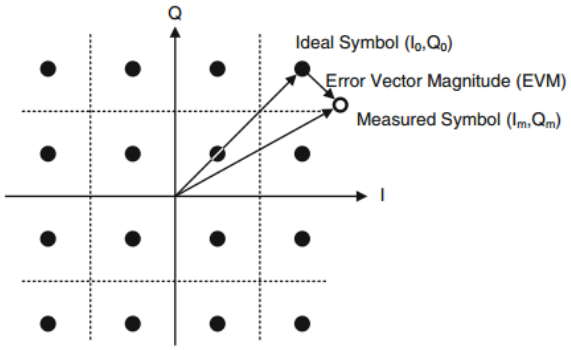


Figure 5-4 Plot of I –Q 16QAM constellation diagram showing the error vector magnitude

5.2.8 ACLR

Adjacent Channel Leakage ratio (ACLR) as shown in Figure 5-5 is a commonly used figure of merit to evaluate the intermodulation distortion performance of RF power amplifier designed for wireless communication systems. ACLR is a measure of spectral regrowth and appears in the signal sidebands and is analogous to IM3/IM5 for an RF amplifier. Take a CDMA standard as example. The ACLR is defined as:

$$\text{ACLR}=\frac{\text{power spectral density in the main channel 1}}{\text{power spectral density in the offset channel 2 or 3}} \qquad 5.14$$

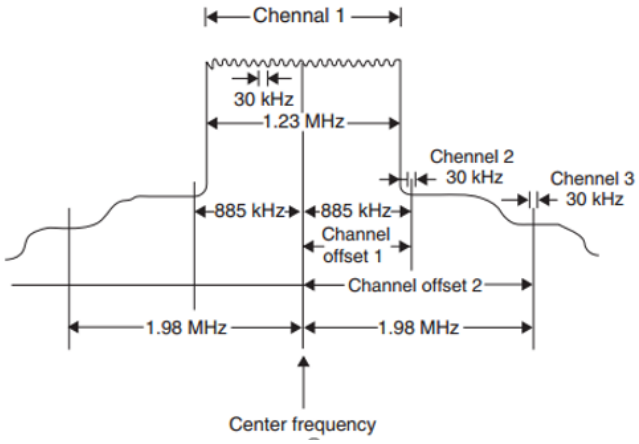


Figure 5-5 CDMA adjacent channel power measurement frequency spectrum.

5.2.9 AM-AM AM-PM Distortion

For a narrowband signal, we can partition the non-linearity into an amplitude-amplitude (AM-AM) component and an amplitude-phase (AM-PM) component. AM-AM conversion represents a Gain variation of a signal when a transistor changes from small-signal to large-signal operating conditions. AM-PM conversion represents a shift in the phase delay of a signal when a transistor changes from small-signal to large-signal operating conditions. As the input signal level applied to a transistor amplifier is increased until some degree of gain compression is produced, further increases in signal amplitude will result in a slight shift of the amplifier Gain change/phase delay. This phenomenon is known as AM-AM /AM-PM conversion and can be thought of as a result of the change of the transistor operating parameters from the small-signal to large-signal conditions. AM-AM/AM-PM conversion is the main measurement to predict the nonlinearity of ACLR.

5.2.10 Memory effect

Any RF PA will show some dynamic deviations from its static characteristics. Such deviations have become known as “memory effects.” The amplification of a modulated signal with large variation of envelope introduces distortions when the input-output characteristic is nonlinear. These distortions are particularly important when the power amplifier (PA) has non-linear memory effects with a wideband signal. These effects are very hard for the process of distortion. Memory effect normally cannot be simulated by steady state and can be traced to three main causes, dynamic thermal effects, unintentional modulation on supply rails and semiconductor trapping effects. The second of these is probably the most common cause of asymmetrical IM sidebands, in terms of ACLR, the

right hand side and left hand side channel power are not equal. Dynamic temperature effects undoubtedly play a part in PA distortion mechanisms 0, while trapping effects is another unsatisfactory generic term, which result from a low response time to switch the transistor on/off status.

5.2.11 Loadpull

In PA design, load pull is used to describe an empirical process by which the matching requirements of a PA device are determined, using some form of variable impedance tuning device. A microwave tuners are configured, and judged, based on their ability to "cover the smith chart". The purpose of load-pull is to find the optimized R_{opt} in max power and max efficiency, respectively, the procedure is quite tedious in most cases. Fortunately, nowadays, we can use simulation tool like ADS to fulfill this function.

The ADS load pull simulation is usually very useful. This setup sweeps the load reflection coefficient in a circular region of the Smith Chart and optimizes the source power level for each load reflection coefficient until the desired power is delivered to the load. The data display shows contours of constant PAE, bias current, gain, and gain compression. The input reflection coefficient is also shown for a particular load that you specify. This allows you to pick the optimal load that produces the best PAE, gain, gain compression, or bias current, or make trade-offs amongst these specifications. As shown in Figure 5-6, at the max PAE 42.217%, the delivered power is 25.162 dBm, we can get more power at the price of PAE, it depends on the designer.

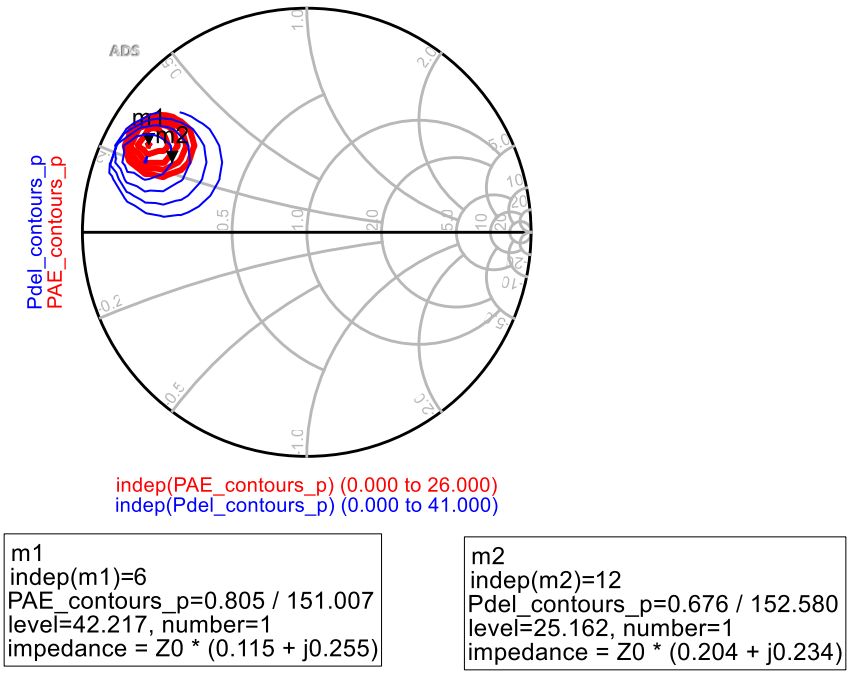


Figure 5-6 Loadpull power and efficiency contour

5.2.12 Classification of RF amplifier

The PA can be categorized into classical PAs and switching mode PAs. According to different conduction angles, the family of PA can be further grouped into four classes: Class A, Class B, Class A-B, Class C. Since the four classes mentioned above share the same circuit topology, a general equation can be derived for this group of PAs. The basic process of reducing the conduction angle is illustrated in Figure 5-7 . The device is biased to a quiescent point beyond the Class A condition, toward cutoff. It is clear that a sufficiently large amplitude of RF drive will swing the device beyond it cutoff point V_t, on the negative portion of the RF cycle. The drive level has to be increased from the Class A condition in order for the current to swing up to the maximum saturation point, I_{max}. The required signal voltage amplitude can be expressed as

$$V_s = (1 - V_q) \qquad 5.15$$

Where V_q is the normalized quiescent bias point, defined according to

$$V_t = 0, V_o = 1 \qquad 5.16$$

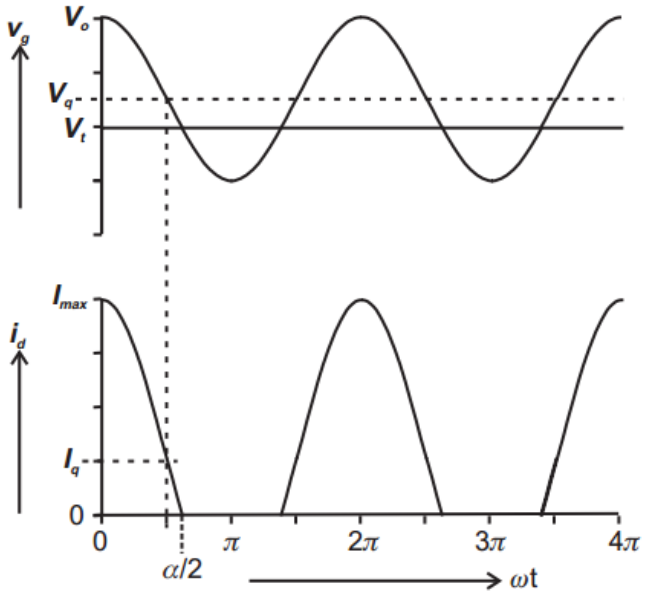


Figure 5-7 Reduced conduction angle current waveform [30]

With the derivation of Fourier analysis, the DC component of current can be given by

$$I_{dc} = \frac{I_{max}}{2\pi} \bullet \frac{2 \bullet \sin(\alpha/2) - \alpha \bullet \cos(\alpha/2)}{1 - \cos(\alpha/2)} \qquad 5.17$$

And the magnitude of the nth harmonics is

$$I_n = \frac{1}{\pi} \bullet \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} \bullet (\cos\theta - \cos(\alpha/2)) \bullet \cos(n\theta) d\theta \qquad 5.18$$

According to the Figure 5-8, it shows the harmonic components in the output current up to 5th order. The different conduction angle shows the different harmonic percentage. For simplicity, the classical PAs are assumed that all harmonics are presented with a short circuit in the load and generate no voltage; only fundamental resistor is presented at the terminal. So the drain voltage is a sinewave whose magnitude will be set by the load

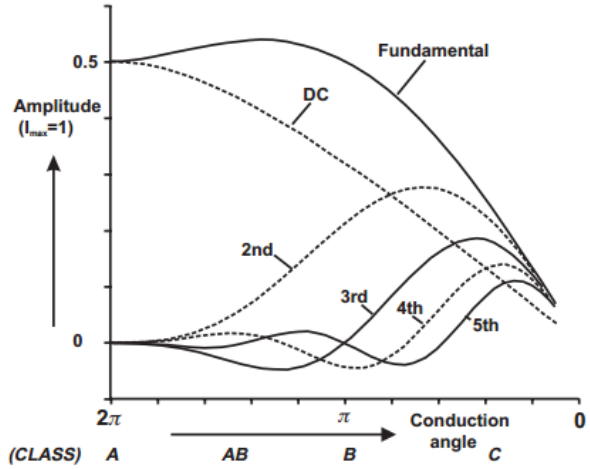


Figure 5-8 Fourier analysis of reduced conduction angle current waveforms [30]

resistor value to generate the maximum permissible voltage swing, given that the RF output voltage at the transistor will in every case be a sinewave of amplitude same as the DC operation voltage. Figure 5-9 shows the efficiency and output power curves with different conduction angle. From the perspective of efficiency, it is clear that Class C with near zero conduction angle will enjoy almost 100% efficiency, however, the corresponding output power drops close to 0, which means it is not a practical design because PA neither consumes DC power nor delivers any power to load.

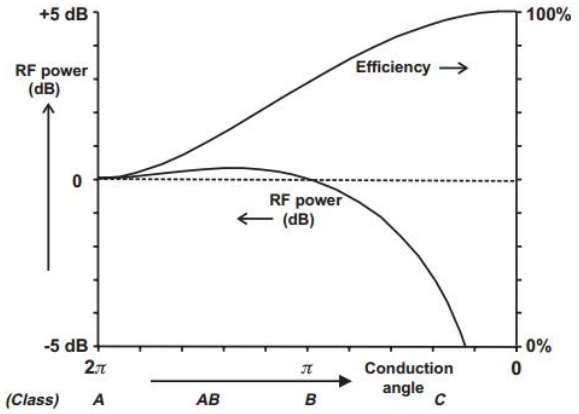


Figure 5-9 power (relative to Class A) and efficiency as a function of conduction angle, optimum load and harmonic shot assumed.

Another important PA group is switch mode PA named as Class-D, E and F. In this category, the gate driving voltage is high enough with an overdrive state so that the active device works in either linear or cut-off region (like a switch). Since there is no overlap between the voltage and drain current across the ideal switch, it means there is no power consumption over the drain, in other words, the theoretical efficiency of a switch mode PA is then given by 100%.

Class D suffers from a drain parasitic capacitance that makes the switch delay time become not ignorable, then leads to a big portion of voltage current overlap which will reduce the efficiency. Regarding to Class E, it plays a trick to absorb the active device's parasitic capacitance at the drain with a wave-shaping network. However, the peak drain voltage of a Class E PA could be as high as 3.562 times VDD[31]- [36]. Then this requires the use of high breakdown voltage transistors.

Class-F PAs offer high power capabilities and high efficiency with a limited number of controlled harmonics. In practical implementations, class-F PAs [37][38][39][40] offers high power capabilities and high efficiency with a limited number of controlled harmonics. Class F_{23} operation requires an open circuit at $3f_0$ and a short circuit at $2f_0$ so that the drain voltage waveform is shaped towards a square wave whereas the drain current is shaped as an inverse one such that it looks like a half-wave sinusoidal. As shown in Figure 5-10. A two-section low pass network is converted to a class-F_{23} PA loadline matching network by placing TZs at the controlled harmonic frequencies. At the same time, the network must create the right impedance at the device drain at f_0, $2f_0$ and $3f_0$ taking into account transistor

parasitic C_{ds} between drain and source. In practice, due to complexity of matching network, Class-F usually have no more than 5th order harmonic resonance.

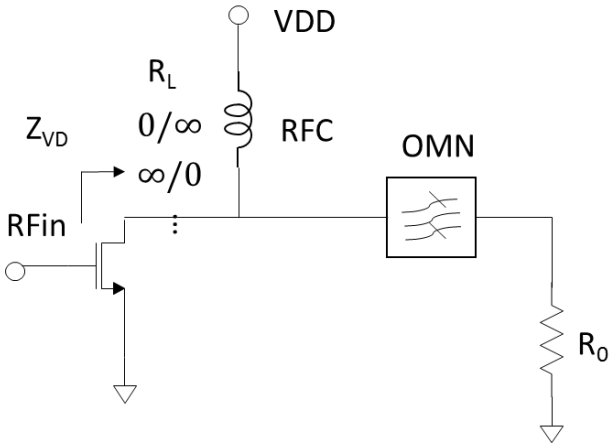


Figure 5-10 Simplified equivalent circuit of a Class F PA

Table 5-1 shows the influence of different orders of resonant networks to a Class-F PA's efficiency and output power.

Table 5-1 Influence of resonant network orders to a Class-F PA's η and Pout [41]

Resonant Network Order	Max. Efficiency	Max. Output Power
1	78.50%	$0.7860P_{out}$
3	90.69%	$0.9075P_{out}$
5	94.77%	$0.9484P_{out}$
∞	100.00%	P_{out}

As a conclusion, Table 5-2 summarizes their characteristics. In general, classical PAs have relatively higher power gain and linearity, while switch mode PAs advance in efficiency and output power. Power amplifiers efficiency is enhanced by operating the transistor in different classes, readers can pick up the interested PA topology freely with specific interest.

Table 5-2 Summary of characteristic of classical and switch mode PAs

Class	A	AB	B	C	D	E	F
Transistor Mode	Current source	Current source	Current source	Current source	Switch	Switch	Switch
Conduction Angle	2π	π~2π	π	0~π	π	π	π
Output Power	Medium	Medium	Medium	Low	High	High	High
Theoretical Efficiency	50%	50%~ 78.5%	78.5%	78.5%~ 100%	100%	100%	100%
Typical Efficiency	35%	35%~ 60%	60%	70%	75%	80%	75%
Power Gain	High	Medium	Medium	Low	Low	Low	Low
Linearity	Very high	High	high	Low	Low	Low	Low
Peak Drain Voltage	$2V_{DD}$	$2V_{DD}$	$2V_{DD}$	$2V_{DD}$	$2V_{DD}$	$3.6V_{DD}$	$2V_{DD}$

5.3 MMMB PA Design

With the growing demand of complex mobile devices that can function in multi-standard wireless communication systems for various user roaming needs, multi-mode and multi-band power amplifiers have become a critical component for future handset development because of their frequency flexibility, easy implementation, and small size. The MMMB PA adaptability enables the performance and cost constraint challenges on the RF front-end by reducing the number of the dedicated single-band power amplifiers for each additional frequency band. The MMMB PA, addressed in this dissertation, is a true single-chip, single-die, multi-mode, multi-band power amplifier designed and implemented in SOI CMOS technology. Its ultra-high efficiency and high linearity architecture offers broadband and scalable support of WCDMA, HSDPA, HSUPA, HSPA+, TD-SCDMA and FDD/TDD LTE modes. It is fully programmable through

MIPI/RFFE. Low-band, mid-band and high-band power amplifiers are integrated with input and output impedance matched to 50Ω, harmonic filters, and ESD protection circuits. The design has integrated switches to support more than nineteen frequency bands for all 3G and 4G modulations.

Figure 5-11 shows the block diagram of this design including the PA cores and band switch, band switch is following the output stage of PA. Detailed bands assignment is shown as below:

- ✓ 3G/4G only MMMB PAs to support the following bands and applications:
  - WCDMA bands: 1,2,3,4,5,8,9
  - TD-SCDMA bands: 34, 39
  - FDD LTE bands: 1,2,3,4,5,7,8,9,12,13,17,20,28
  - TD-LTE bands: 38, 39, 40, 41

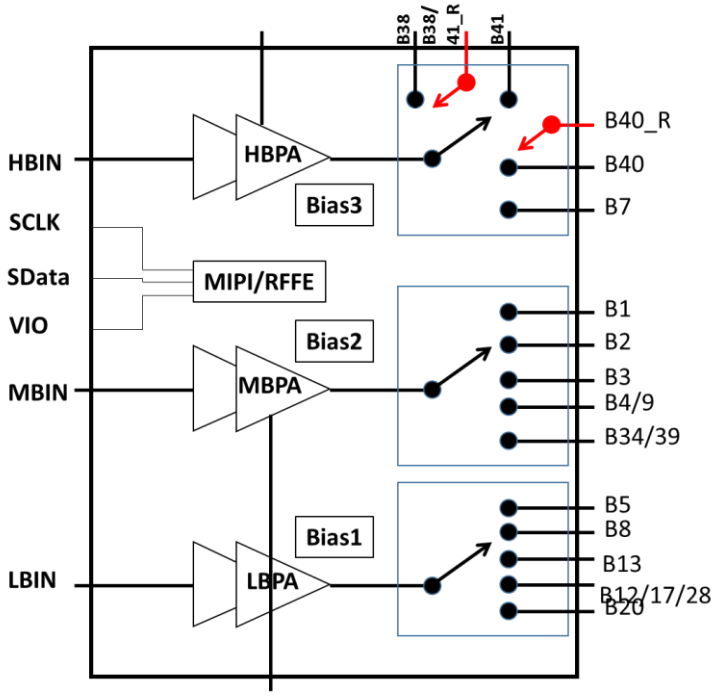


Figure 5-11Block diagram of MMMB PA including band switch

Each band PA core designed in this dissertation has the same topology as shown in Figure 5-12, but with different matching element. A HB PA will be discussed to help to understand the design methodology.

The power amplifier working into a Class F category consists of two stages to provide 30 dB gain or so. For stage number, single stage cannot provide enough gain whereas three stages PA is with sufficient gain but costs larger die area, increase the complexity of matching network and may cause potential stability issue. Stability is a major concern for any type of RF and microwave amplifier, as PAs may exhibit several types of instabilities

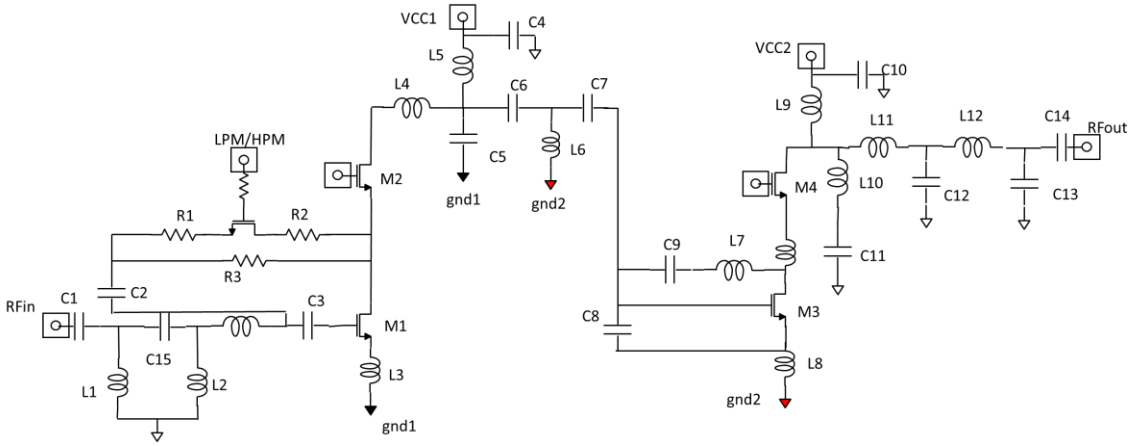


Figure 5-12 MMMB PA core schematic

simultaneously. In general, PA instabilities can be divided into two main sources. The first source comes from the instabilities caused by the transistor capacitance parasitics combined with parasitic circuit inductances. For example, the gate to drain feedback capacitor in conjunction with the drain inductor is a source of potential instability. The second source is the instability created by the combination of bypass capacitors, along with the parasitic ground and supply inductances of bonding wire or supply line connections. A simple way to solve this problem is by adding a series resistor in the gate input, thus

reducing the network quality factor, however, it may cause performance degradation, for example, noise. The first mentioned source of instability can be solved by using RC feedback networks as shown in Figure 5-12. R3 and C2 between the drain and gate of the transistor M1 are placed to improve the stability, although this produces the negative effect of gain reduction. In this way, the use of two stacks cascade transistors not only allow the PA to handle larger output power level but also improve PA stability. However, the cascade transistor itself can be a source of instability due to the insufficient AC grounding of the common-gate terminal. As shown in Figure 5-13 , the bypass capacitor C1 is used to stable DC bias from LDO, from PA's perspective, it provides the tuning capability of AC swing in the gate nodes, thus tuning the voltage distribution in each stack, and help to achieve a linearity balance.

Parasitic L3 and L8 play like a degeneration inductor, which may appear as impedance with negative real part, thus cause a stability problem. For the first stage, the RC feedback network helps to increase the stability. For the second stage, it plays a more important role to drive power. It is designed intentionally marginal stable in order to boost gain.

A partial coupling method using a feedback network comprised of L7 and C9 over gate-drain of the second stage is introduced to avoid entering the triode region. In this way, the variation in gate-drain parasitic capacitance with respect to the output power is reduced, guaranteeing a linear operation.

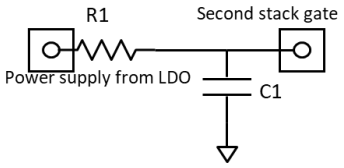


Figure 5-13 Bypass bias circuit of the second stack transistor

The bias circuit is shown as Figure 5-14, the ib1 is PTAT current from bandgap block, followed with a source follower, M3 and M4 consists of two stage source-follower, and M2 comprises the negative feedback network to make output voltage more stable. C2 with large capacitor value creates AC ground. M5 is a diode connected MOSFET, which can perform like a rectifier, in DC condition, M5 is on, then DC can be biased directly to the gate of the first stack of each PA stage. Since it's a PA design, there would be a floating AC signal in the gate node, then with the existence of R3/M5 rectifier, when there is large

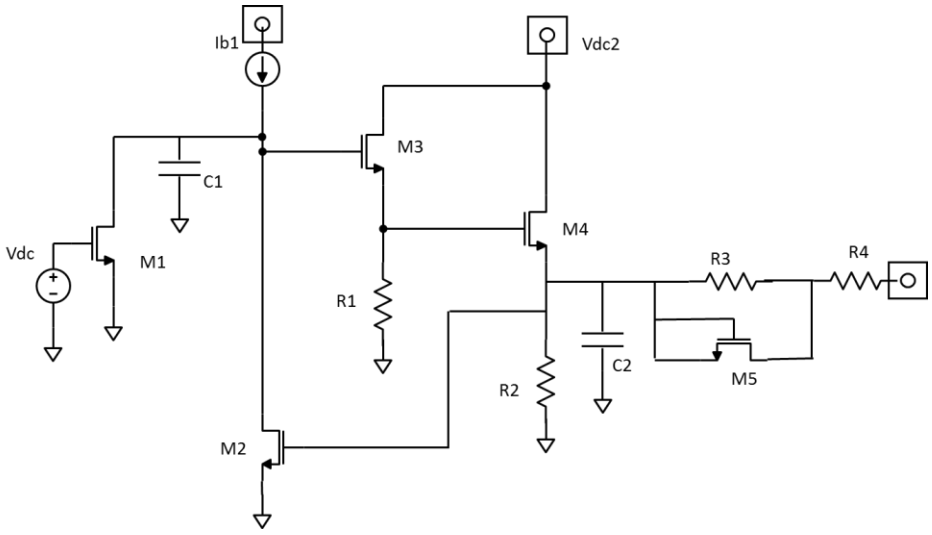


Figure 5-14 bias circuit of the first stack transistor

AC swing at high power, there would be DC component over the R3 higher than the original DC bias voltage, then at the high output power, the higher DC bias in gate will boost the gain, which is beneficial for the AM-AM flatness tuning, thus improve the linearity. However the potential shortcoming is the increasing R3 may enable more gain capability, it increases the response time in gate as well, and cause a potential baseband modulation effect, therefore degrades the overall linearity, so it's a design trade-off.

Regarding to output matching network which is following transistor M4 in Figure 5-11. It is Lowpass Lowpass network comprised of L11/C12/L13/C13. Moreover, a second order harmonic trap is implemented by L10/C11. C14 is used to be the DC block capacitor. Normally, the matching network requires a high Q inductor, so for the inductor with large value, it will be designed in the laminate, which can provide less loss.

Due to the variance of inherent CMOS parasitic capacitance nature over the voltage, the gain of each stage is not flat at high power, it will affect the linearity of PA dramatically, as shown in Figure 5-15 which displays the gain curve of each stage with three different frequencies. The gain of each stage is flat at low output power, but the AM-AM performance becomes worse, thus it will affect the linearity of power amplifier. As we can see, the AM-AM curve for each single stage is not flat as the output power is larger than 20 dBm, in other words, if only one stage is designed, the linear output can only achieve 20 dBm. However, the unflatten gain curve of each stage can be compensated at high power level. The design trick is to play the gain curve of the first stage with a notch and the gain curve of second stage with a hump in high power, then the PA presents a flat overall gain.

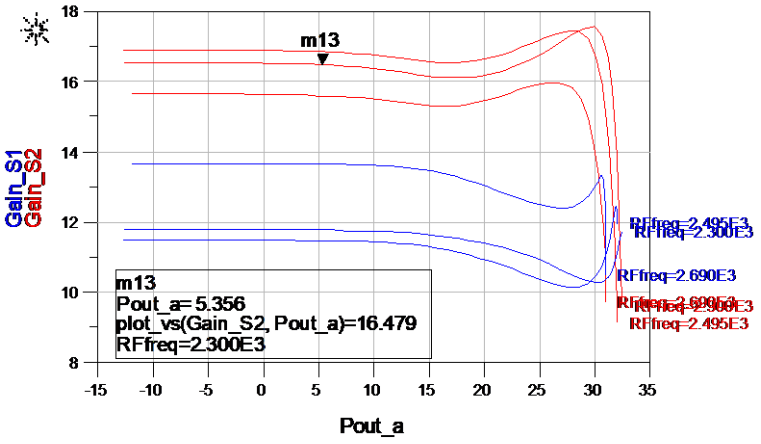


Figure 5-15 Gain over output power of PA stage one and stage two

The top level PA schematic as shown in Figure 5-16 is simulated in ADS, the DC/SP/HB engines are used to evaluate the PA performance. Single tone, WCDMA TC1 and LTE TC1 with QPSK 10M 12 RB signal are used as the PA input signal source separately.

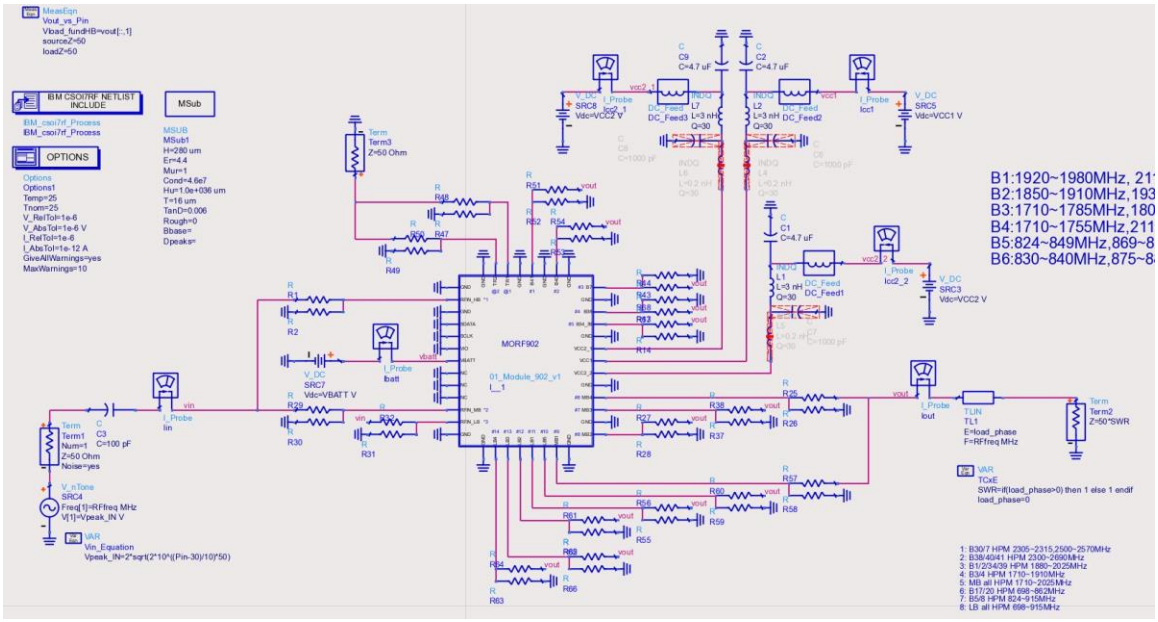


Figure 5-16 Top level schematic of Power amplifier design

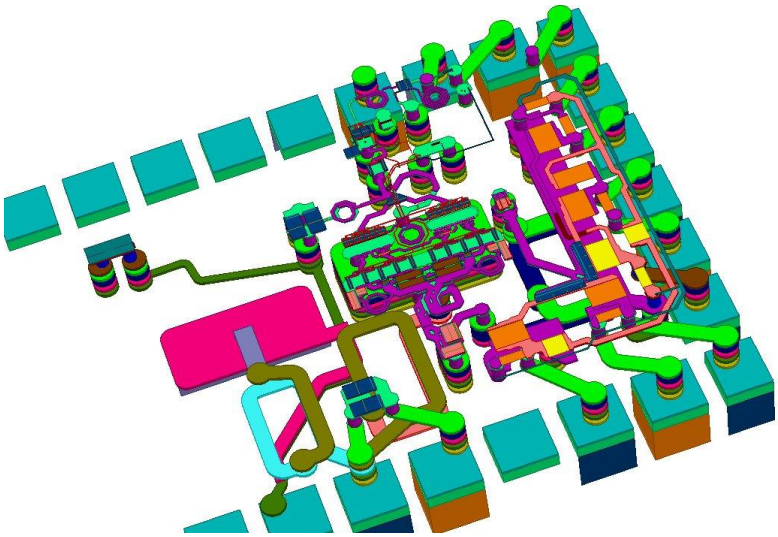


Figure 5-17 HB PA EM model in HFSS

At GHz frequencies, any interconnecting wire will have a significant electrical length in comparison to wavelength at the application frequency, and the coupling between interconnects will contribute to circuit performance as well, thus, the interconnection has to be regarded as part of the circuit design. EM effect should be considered and simulated which cannot be fulfilled in the Cadence, even though the RC parasitic was extracted by post-layout simulation tool. Several ports are set up in EM model as shown in Figure 5-17 for extracting the S parameter file or tweak purpose. The overview layout as shown in Figure 5-18, LB/MB/HB are separate in layout.

5.3.1 Simulation result

5.3.1.1 Load impedance and OMN loss

The matching network will affect the PAE and output power in terms of loss. However, the loss cannot be measured by two-port network S parameter, namely, S21 directly. Since

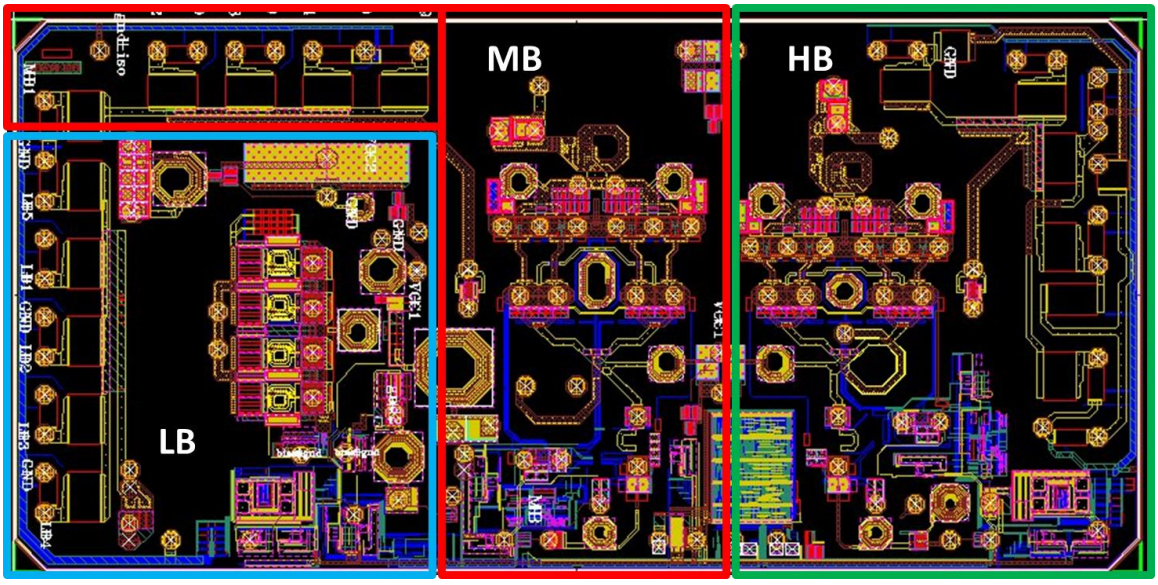


Figure 5-18 layout of MMMB PA covering LB/MB/HB

the input impedance is not matched to 50 ohm. So, considering the reflection at the input port, the actual network loss can be represented by equation 5.19.

$$\text{Network Loss} = \frac{S_{21}}{\sqrt{1-|S_{11}|^2}} \qquad 5.19$$

With respect to the four Tx branches of HB PA, loadline impedance and loss are the first concern. Figure 5-19 shows real part and imaginary part of the loadline over the frequency from 2.3GHz to 2.7 GHz, the curve should be as flat as possible to achieve a wideband performance. The loadline network loss including the matching network and switch is varying from 0.9dB to 1.15dB loss over the frequency range which is quite fair. In regards to the Rx path, it excludes the PA matching network, so the loss comes from the switch itself, as shown in Figure 5-20, Rx path insertion loss and network loss are quite close and all the branches are below 0.65 dB.

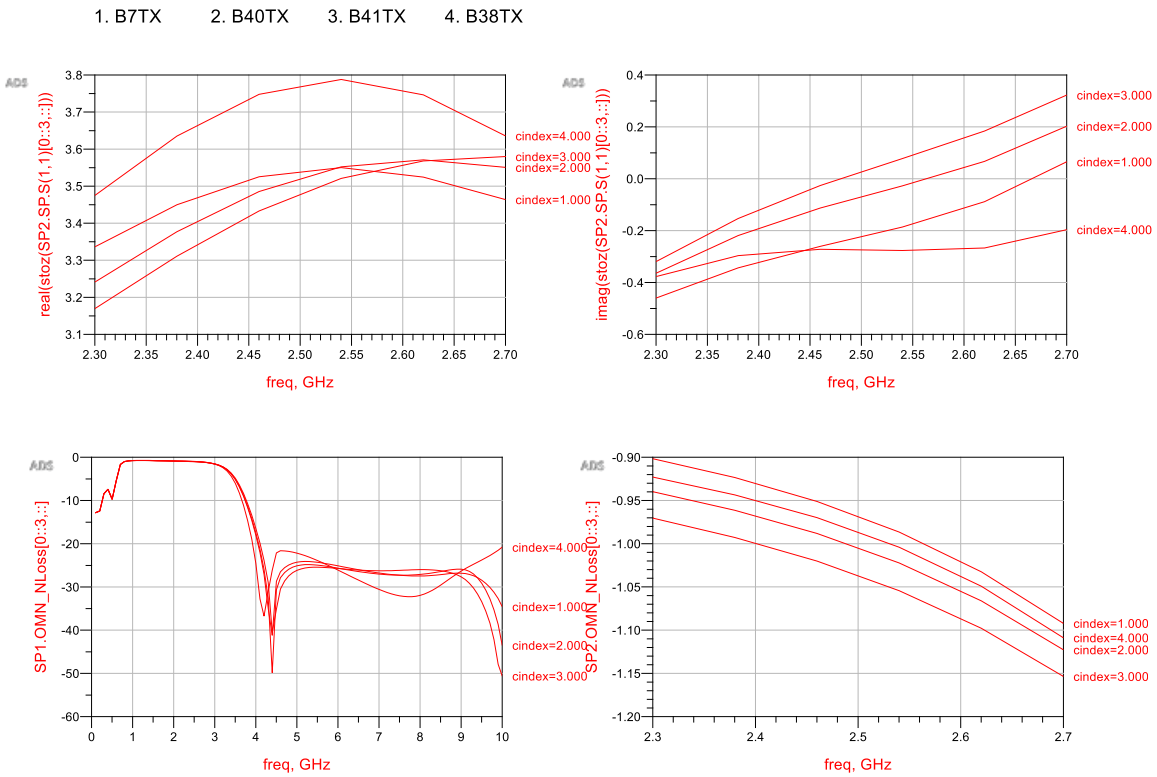


Figure 5-19 Loadline and output matching network loss over frequency for Tx path

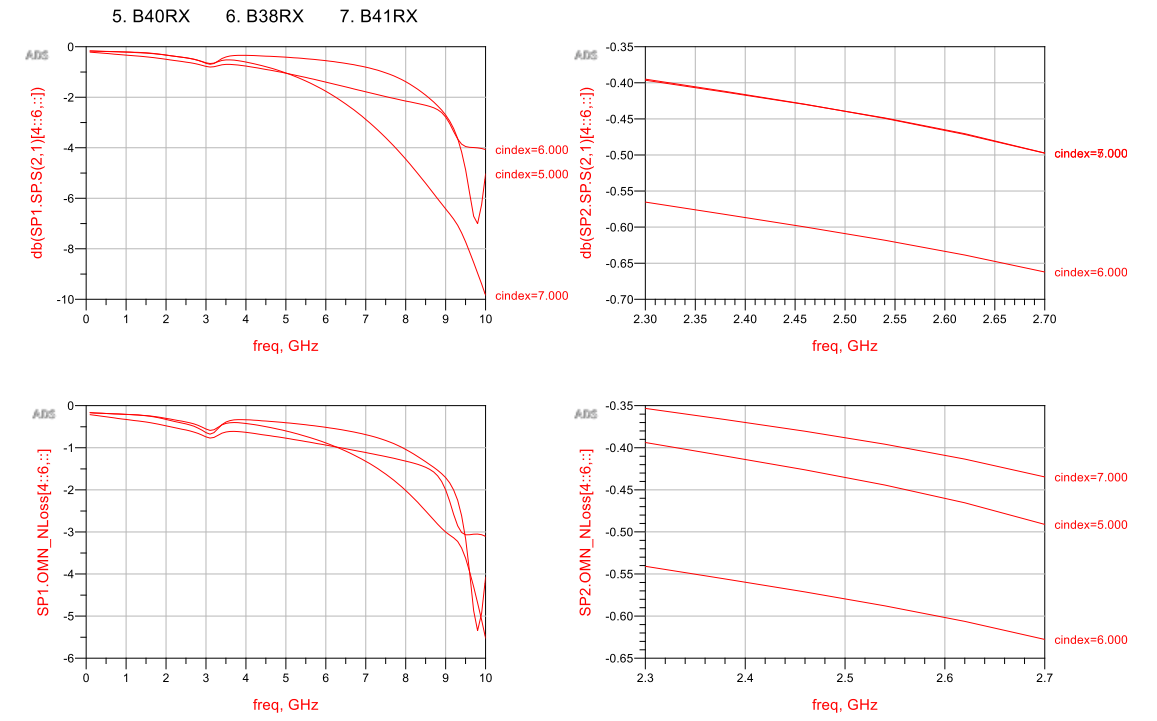


Figure 5-20 output matching S21 and network loss over frequency for Rx path

5.3.1.2 B7Tx to B41Tx and B38Tx Isolation

Another concern for the multiband is the isolation between B7 to B41 and B38, B7 is FDD LTE band from 2.5GHz to 2.57 GHz, which overlaps the TDD LTE bands 41 and 38. In this case, the isolation between these bands are extremely important since the band filter cannot suppress the in-band noise. As shown in Figure 5-21, the isolation between B7 and B41 is higher than 36 dB, and isolation between B7 and B38 is higher than 38 dB.

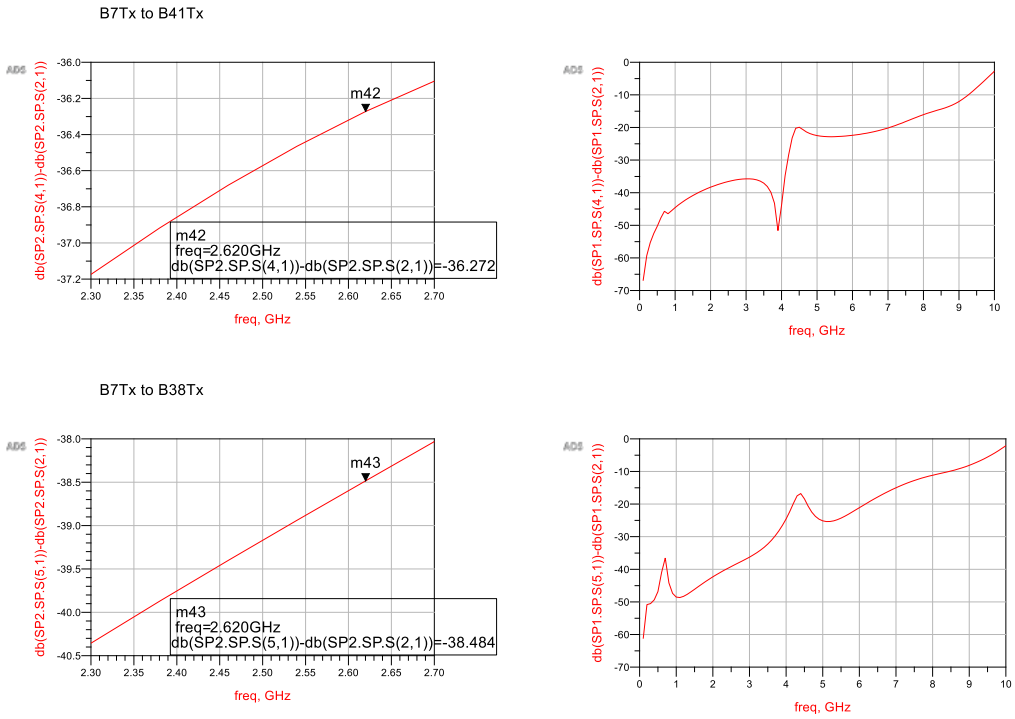


Figure 5-21 B7Tx to B41Tx and B38Tx Isolation

5.3.1.3 Small signal S parameter

For the small signal, S parameter is a good measure to look into the PA performance, the S21 parameter is presented in Figure 5-22, the green line limits the gain specs and the red lines limits the out-band harmonic suppression, prevents from leakage in GPS band as well.

A zoom in view will show more details in Figure 5-23. As we can see, the small signal gain is approximately 30 dB and quite flat in band.

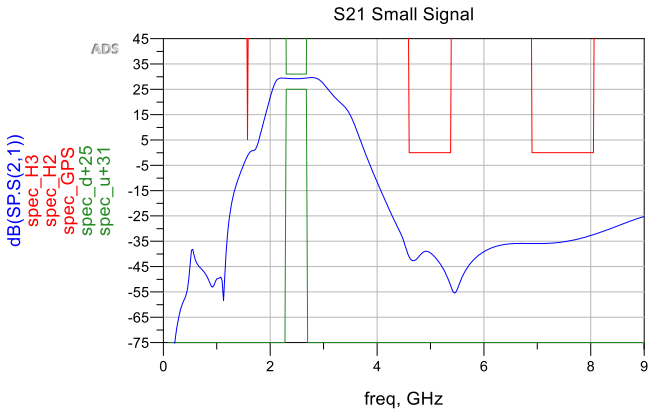


Figure 5-22 S21 parameter simulated between PA input and output

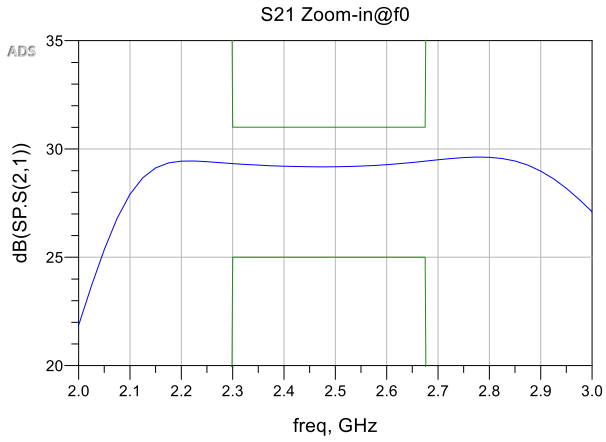


Figure 5-23 Zoom in view of S21 parameter simulated between PA input and output

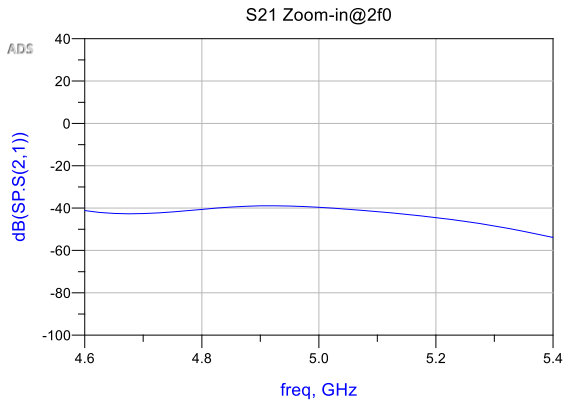


Figure 5-24 S21 parameter @ 2f0 simulated between PA input and output

Input return loss reflects the power matching in the input port of a PA, normally it matches to 50 ohm. VSWR is another parameter that can reflect the matching network. As depicted in Figure 5-25 and Figure 5-26, the curves are within the spec from the lower frequency to upper frequency.

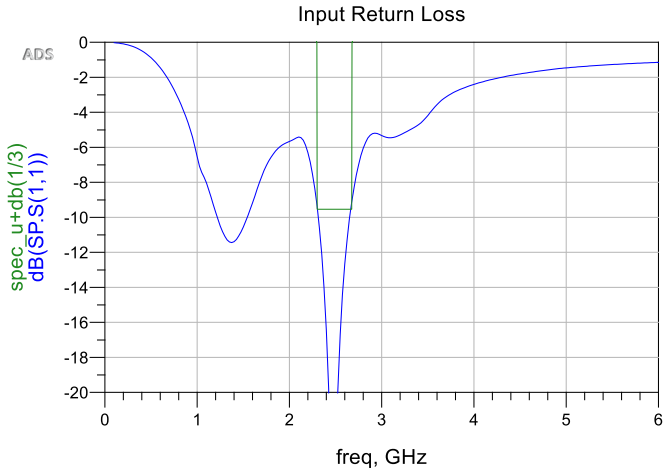


Figure 5-25 S11 parameter simulated from PA input

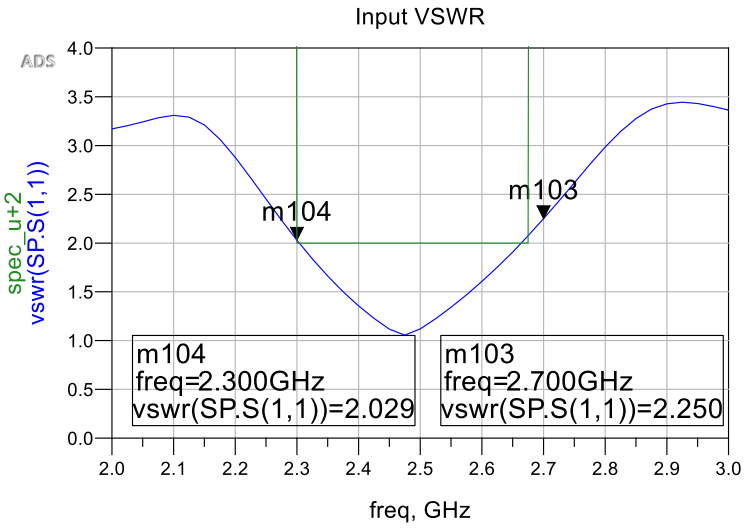


Figure 5-26 Input VSWR from PA input

The small signal S12 can be checked as well that there is no reverse gain as shown in Figure 5-27, which represents a good isolation. And the S22 curve in Figure 5-28 is flat over the frequency band with negative value which means no reflection gain at the output port.

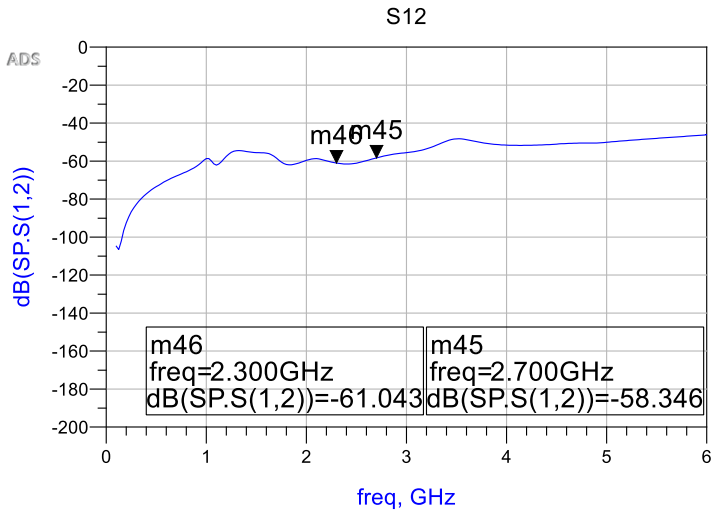


Figure 5-27 S12 parameter simulated from PA input and output

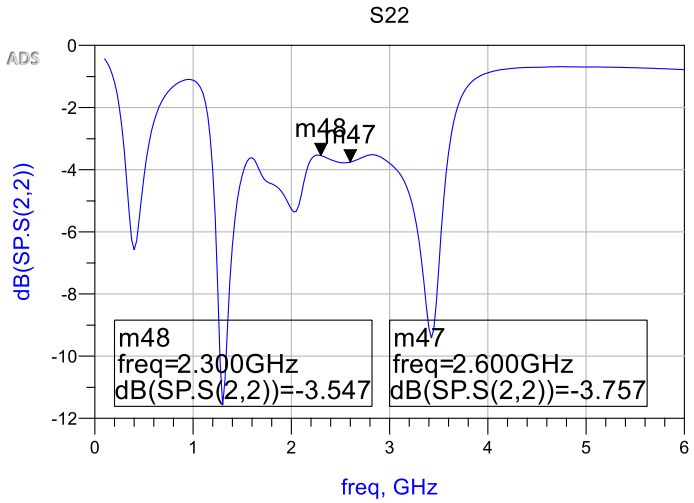


Figure 5-28 S22 parameter simulated from PA output

5.3.1.4 Stability

The overall stability can be checked by K factor and B factor measuring the two port S parameter between input and output, as depicted in Figure 5-29, K is larger than 1, and B

is larger than 0. Another potential unstable condition checkpoint is drain node of each active transistor, the adding impedance looking into the right hand side and left hand side should be with a positive real part. As depicted in Figure 5-30Figure 5-31Figure 5-32Figure 5-33, it shows the drain impedance of each stage and each transistor, it means the PA works in stable state.

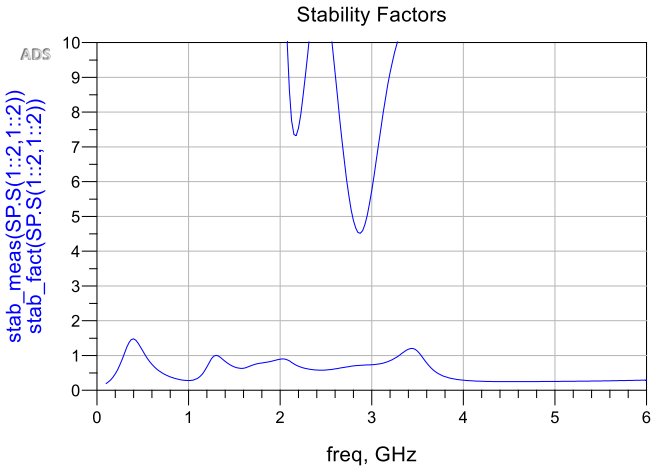


Figure 5-29 Small signal K factor and B factor

Stage 1 drain stability check

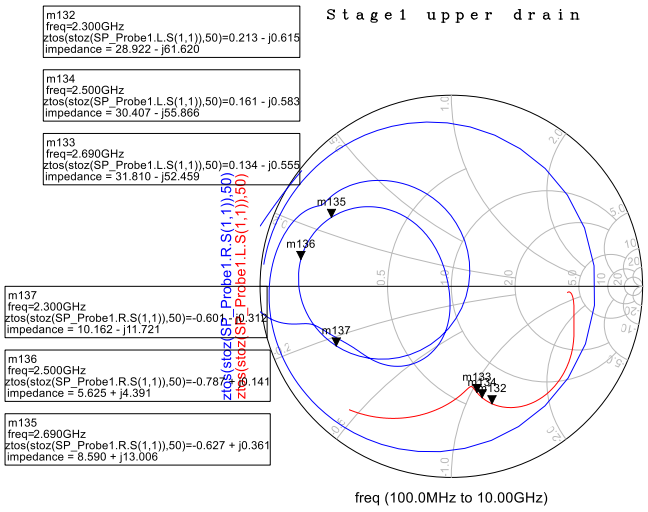


Figure 5-30 Smith chart of first stage upper transistor drain impedance

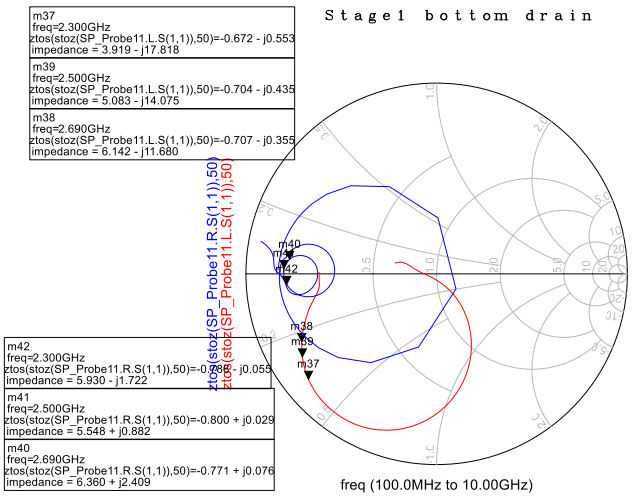


Figure 5-31 Smith chart of first stage bottom transistor drain impedance

Stage 2 drain stability check

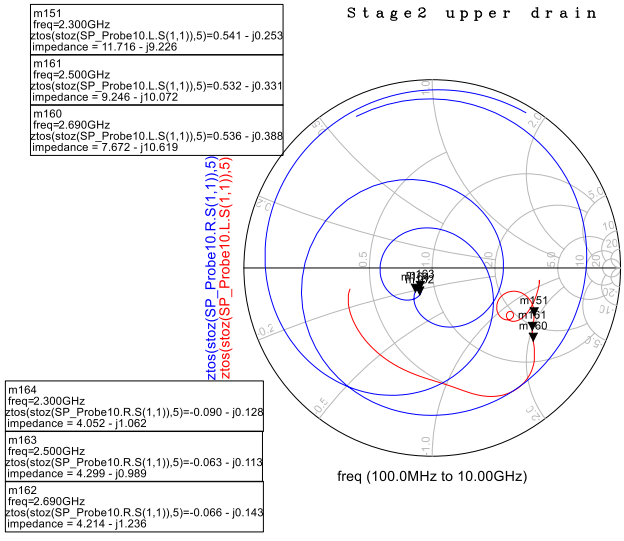


Figure 5-32 Smith chart of second stage upper transistor drain impedance

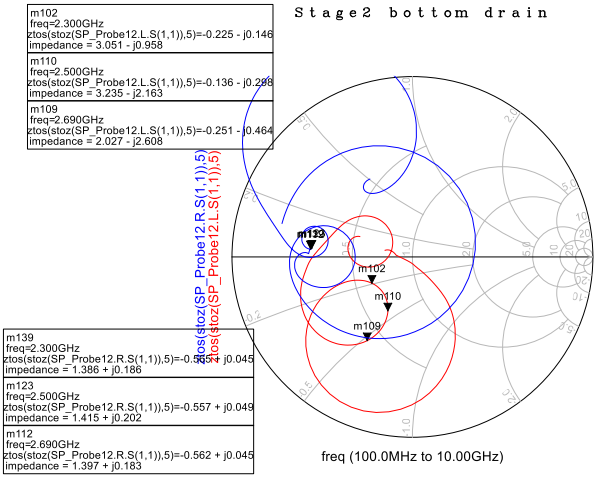


Figure 5-33 Smith chart of second stage bottom transistor drain impedance

5.3.1.5 AM-AM/AM-PM

The AM-AM and AM-PM simulation results are shown in Figure 5-34 and Figure 5-35, respectively. Using LTE TC1, the servo rated power is 27.5 dBm, around that, the AM-AM curve is quite flat and the variation is within 1 dB. The maximum output power of high band PA is 32.5 dBm or so, which should be as high as possible to improve the linearity considering the peak to average ratio. The AM-PM is not so flat and probably will contribute more to ACLR degradation.

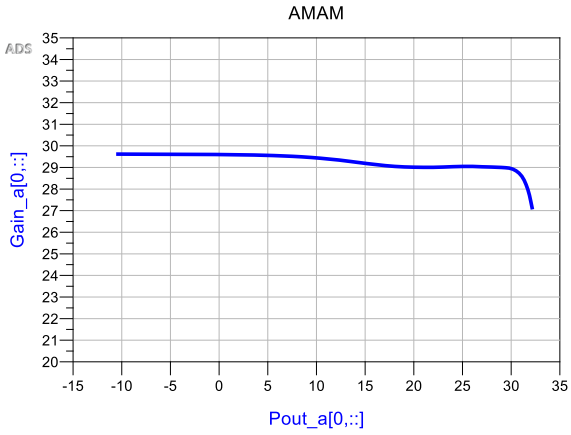


Figure 5-34 AM-AM characteristic

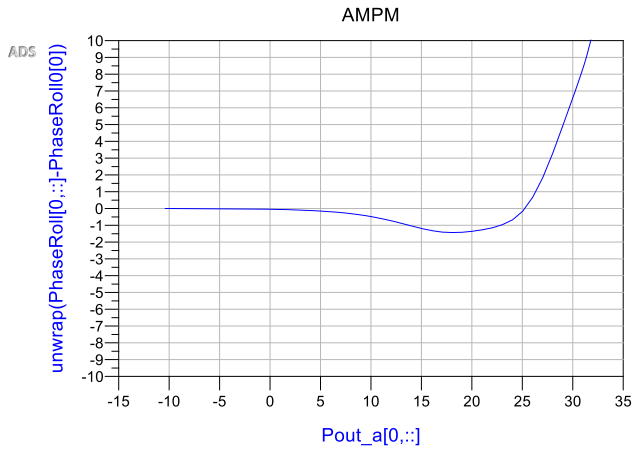


Figure 5-35 AM-PM characteristic

5.3.1.6 PAE

Figure 5-36 demonstrates the HB PA PAE when the input signal is a single tone, as linear PA, we can see that the max efficiency occurs at the maximum power, a design trade-off here is that maximum power can be pulled high to get a better linearity, but the max PAE could remain the same, thus compromise the PAE at rated power. Especially, the efficiency in high frequency can hardly achieve specs because of more loss in power transistors and matching network.

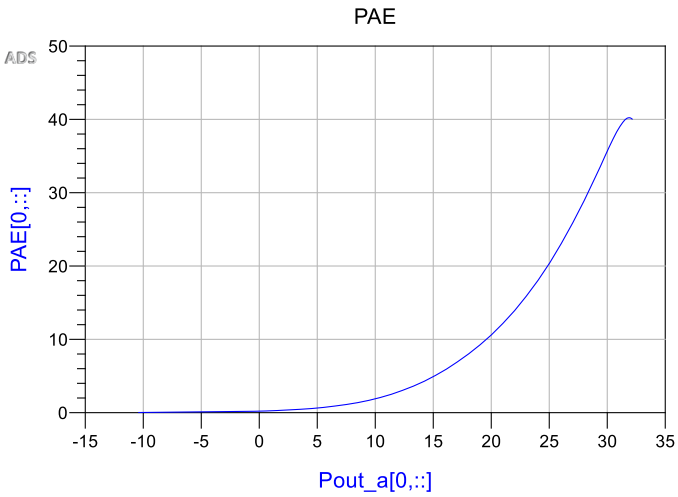


Figure 5-36 PAE characteristic

5.3.1.7 Key performance with large signal

Figure 5-37 shows the overall gain/ACLR/current/PAE over the high band frequency at servo rated power 27.5 dBm, the performance is consistent and this PA is a real wideband design.

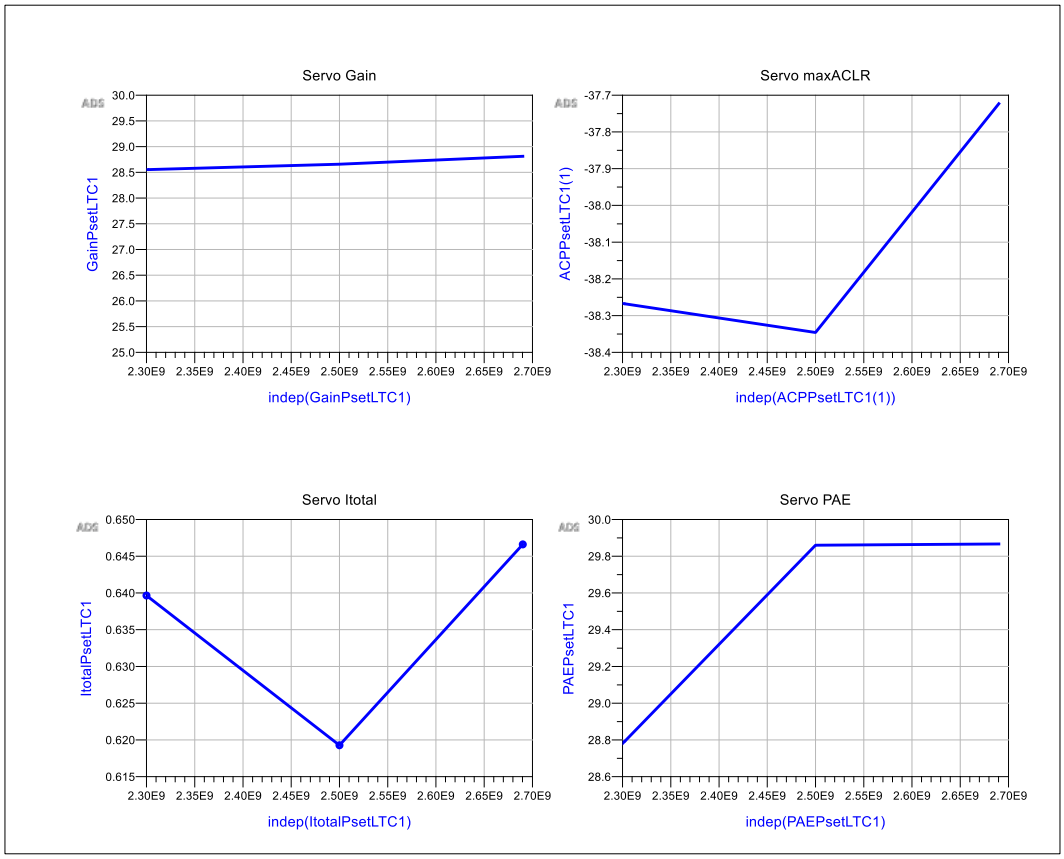


Figure 5-37 Servo Gain/ACLR/total Current/ PAE over frequency in HB

5.3.1.8 Harmonics

Harmonic simulation result is illustrated in Figure 5-38, all the harmonics up to order five are within specs. For the low-band PA, this spec is extremely important, since 2nd harmonic will drop into the Mid-band and cause an interference.

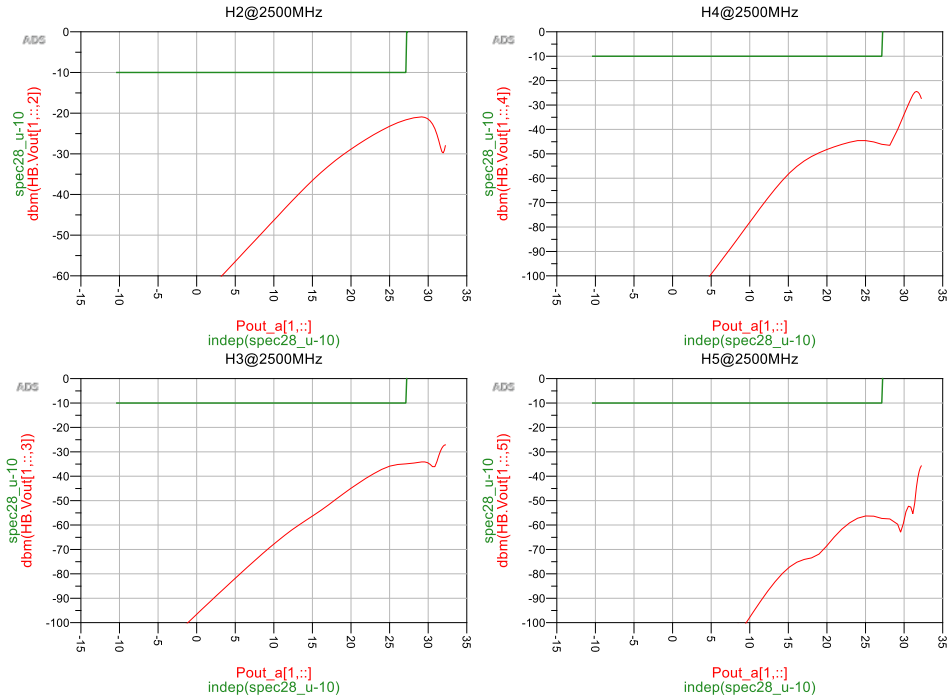


Figure 5-38 Harmonic characterization

5.3.1.9 Transient Waveform of Drain Voltage and Current

Figure 5-39 shows the voltage and current waveform, the red voltage curve can be higher than 10V, it's really a big challenge for MOSFET breakdown considering two stage PA design, the current has 180 degrees offset to voltage so that to make a Class-F type PA. The high peak voltage may not cause the transistor break down immediately, but will cause the reliability problem like hot carrier injection, the maximum output power may drop down after burning for a while, consequently, it will worsen the linearity. The safe way to avoid this is to use more stack transistors, but inevitably, it will cause the degradation of PAE and linearity due to more induced loss and more voltage-variant parasitic capacitance. Furthermore, it's harder for distributing bias voltage over the 2nd and 3rd stack transistor.

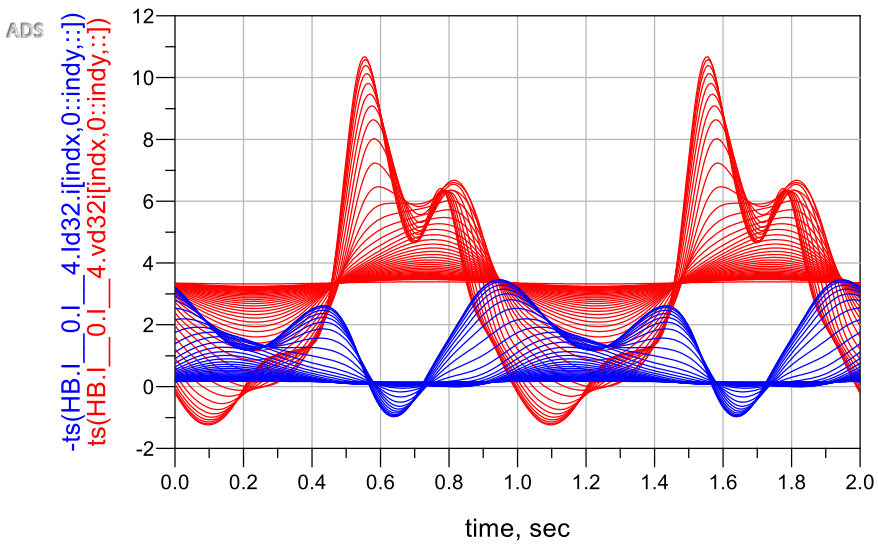


Figure 5-39 Transient waveform of voltage and current

5.3.1.10 Loadline I-V curve

The loadline can be verified in Figure 5-40 and Figure 5-41. The I-V curve of each transistor in first stage is within the cutoff and saturation region working as a class AB mode. Regarding to the second stage, we can see that the PA works in a switch mode and full maximum voltage capability are developed.

Stage1

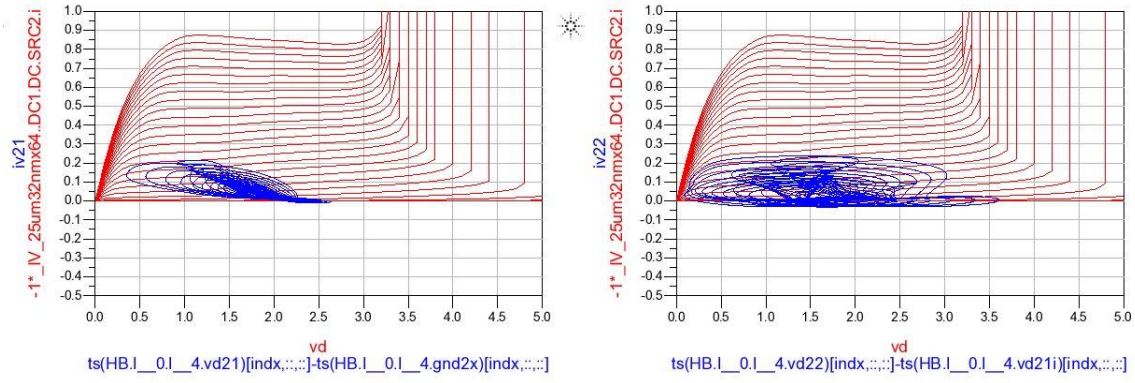


Figure 5-40 First stage loadline I-V curve for both bottom and upper transistor.

Stage2

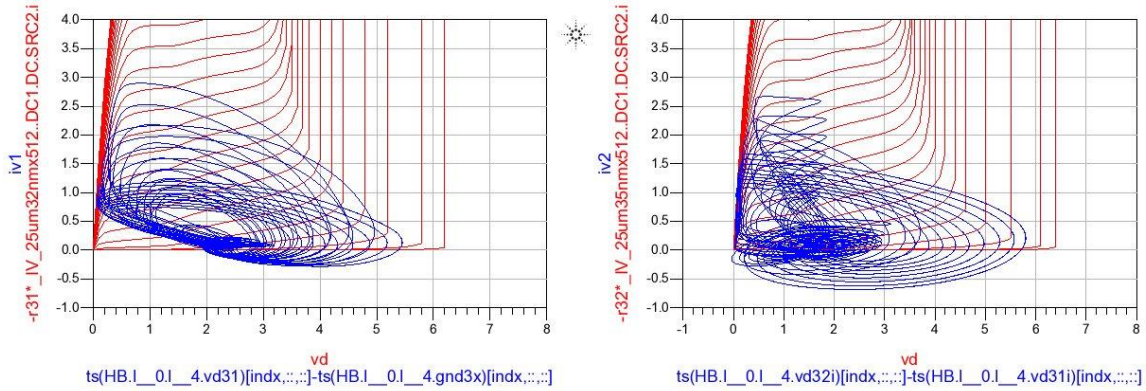


Figure 5-41 Second stage loadline I-V curve for both bottom and upper transistor.

5.3.2 Evaluation board

The schematic and layout of evaluation board is shown as Figure 5-42 and Figure 5-43. Only a few bypass capacitors are added in the periphery circuit without off-chip matching network, so this design will save cost and time for FEM PCB designer.

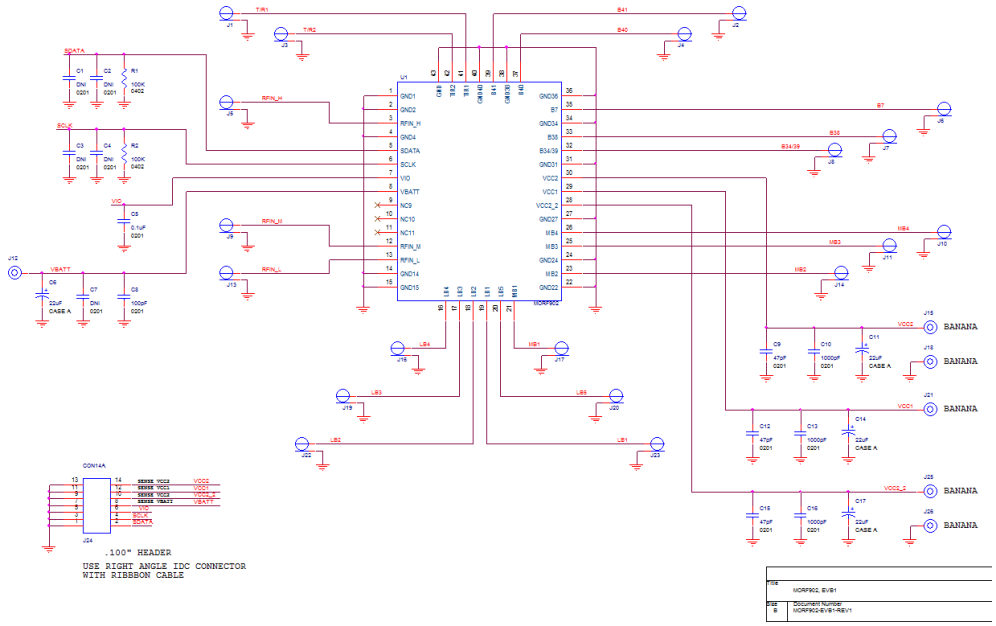


Figure 5-42 Schematic of evaluation board

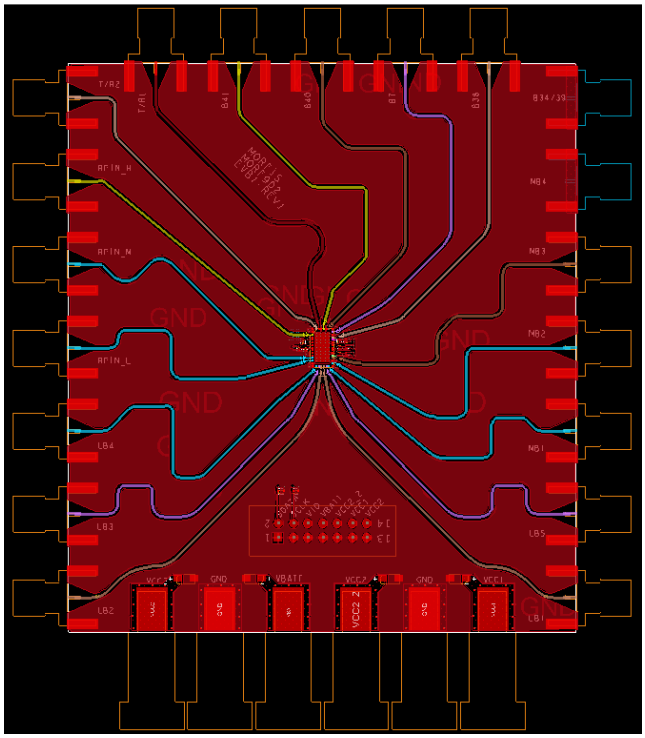


Figure 5-43 Layout of evaluation board

Chapter 6 Analog Part

6.1 Bandgap

The design of bandgap voltage reference focusing on high accuracy and low temperature coefficient is discussed in this dissertation. The novel current trimming technique is introduced to improve the accuracy. As a summary, it reports bandgap voltage reference with measured 17.1ppm temperature coefficient and 0.15% simulated 3 sigma accuracy after trim at 1.19V over temperature range -40 to 125℃.

Precision Bandgap voltage references (BGR) have been widely used in mixed-signal integrated circuits, their accuracy plays a vitally important role in determining the performance of subsequent circuits, for example, BGR circuit are utilized in the regulator and ADC/DAC which require high accuracy to provide stable power supply and high resolution data conversion. This paper introduces an ultra-high accuracy bandgap circuit with current trimming technique; meanwhile, multiple methods such as op-amp offset minimization, curvature correction are implemented to enhance the BGR performance.

The basic idea of BGR is to add a proportional to absolute temperature (PTAT) voltage to the emitter-base voltage (V_{BE}) of bipolar junction transistor (BJT) [42], so that the first-order temperature dependency of the p-n junction is compensated by the PTAT voltage, and a nearly zero temperature independent output is thus generated. The PTAT voltage is actually the thermal voltage (V_T) of the p-n junction. The simplified bandgap schematic is depicted in Figure 6-1, where V_{bg} is the Bandgap output while V_{OS} is the input offset of the Op-amp. The reference voltage output voltage V_{bg} can be expressed as:

$$V_{bg} = V_{BE} + \left(1 + \frac{R_2}{R_1}\right) * (\Delta V_{BE} - V_{os}) \qquad 6.1$$

where $\Delta V_{BE} = V_T \ln N = \frac{kT}{q} \ln N$ is the base-emitter voltage (V_{BE}) difference between Q1 and Q2 and N is their emitter area ratio. More details is described in previous published work [43].

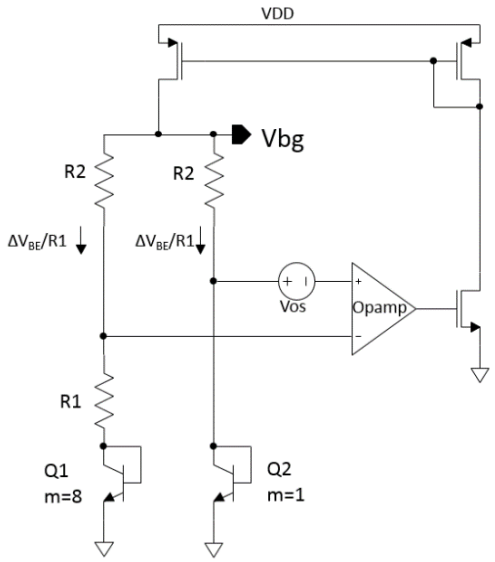


Figure 6-1 Simplified schematic of Bandgap voltage reference with NPN ratio N = Q1:Q2 = 8:1.

6.2 Low Drop Out Voltage Regulator

Industry is pushing forwards complete system on chip design solutions including power management. The study of power management techniques has increased dramatically within the last few years corresponding to the vast increase in the use of portable, handheld battery operated devices. Power management seeks to improve the device power's efficiency resulting in prolonged battery life and operating time for the device.

A power management system contains several subsystems including linear regulators, switching regulators, and control logic. The control logic changes the attributes of each

subsystem, turning the outputs on and off as well as changing the output voltage levels, to optimize the power consumption of the device. The presented research focuses on low drop-out (LDO) voltage regulators. LDO regulators are an essential part of the power management system that provides constant voltage supply rails. They fall into a class of linear voltage regulators with improved power efficiency. LDO voltage regulators have several inherent advantages over conventional linear voltage regulators making them more suitable for on-chip power management systems.

LDO voltage regulator is used in analog applications that generally require low noise, high accuracy power rails. It provides a constant voltage supply rail under wide loading conditions. These conditions include fast current transients and rapid changes in the load impedance. The LDO regulator uses a single transistor in a common-source configuration operating in saturation as shown in Figure 6-2. The output voltage is sensed through feedback resistors R_1 and R_2. An error amplifier then compares the scaled output voltage to a reference voltage. The error signal is fed to the pass transistor and forms the negative feedback path. Transistor orientation plays a major role in the operation and the stabilization of the linear voltage regulator. In this dissertation, LDO is designed to provide switch control voltage and PA bias voltage.

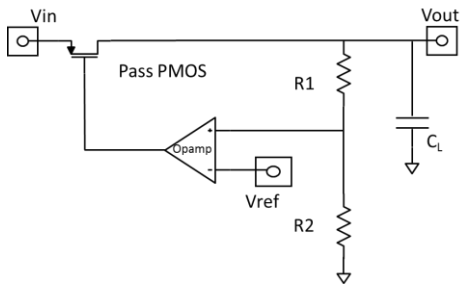


Figure 6-2 Schematic of Low drop-out voltage regulator

6.3 Level Shifter

Level shifter is a circuit which converts the signal level from one voltage to another, thus helping in the interaction of the circuit operating at different supply voltages. Since digital control block is 1.8V power domain and switch controller is 2.5V power domain in this design, then the level shifter is needed to amplify the signal so that the high voltage domain cells can read logic 1 or 0 correctly. The schematic is shown as Figure 6-3.

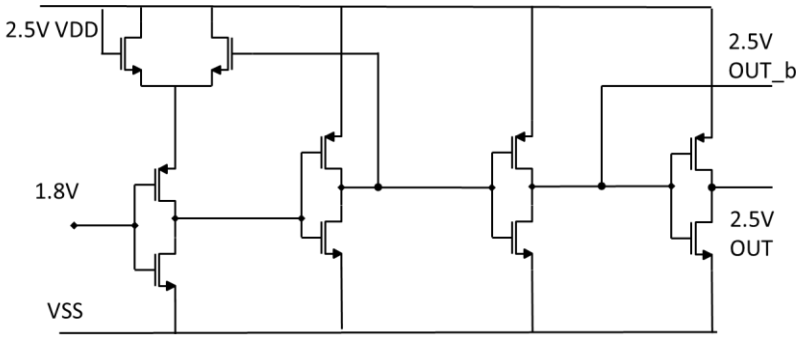


Figure 6-3 level shifter converts the voltage from 1.8V to 2.5V

6.4 Charge Pump

The charge pump is the most important block in the switch controller since it generates the desired negative bias voltage to the switch. The first charge pump introduced in [44] is to generate a voltage higher than a power supply. Figure 6-4 illustrates a schematic of charge pump, which can generate a negative voltage. It consists of eight NMOS/PMOS transistors, two charging capacitors C1 and C2, and two-stage invertor chain is used for clock waveform shaping. If *CLK* is low, $\overline{CLK}$ is high, then M1/M4/M5/M8 in the upper part are on and M2/M3/M6/M7 are off, and in the next clock cycle, the *CLK* is high, $\overline{CLK}$ is low, M1/M4/M5/M8 in the upper part are off and M2/M3/M6/M7 are on. In each period cycle, the C1 and C2 will be charged alternatively until the voltage drop is equal to VDD

across the capacitor, since C1 and C2 are series connection, and VSS is in the middle node, with appropriate load, the output voltage V_{neg} should be equal to minus VDD. In this design, V_{neg} is to provide -2.5V bias.

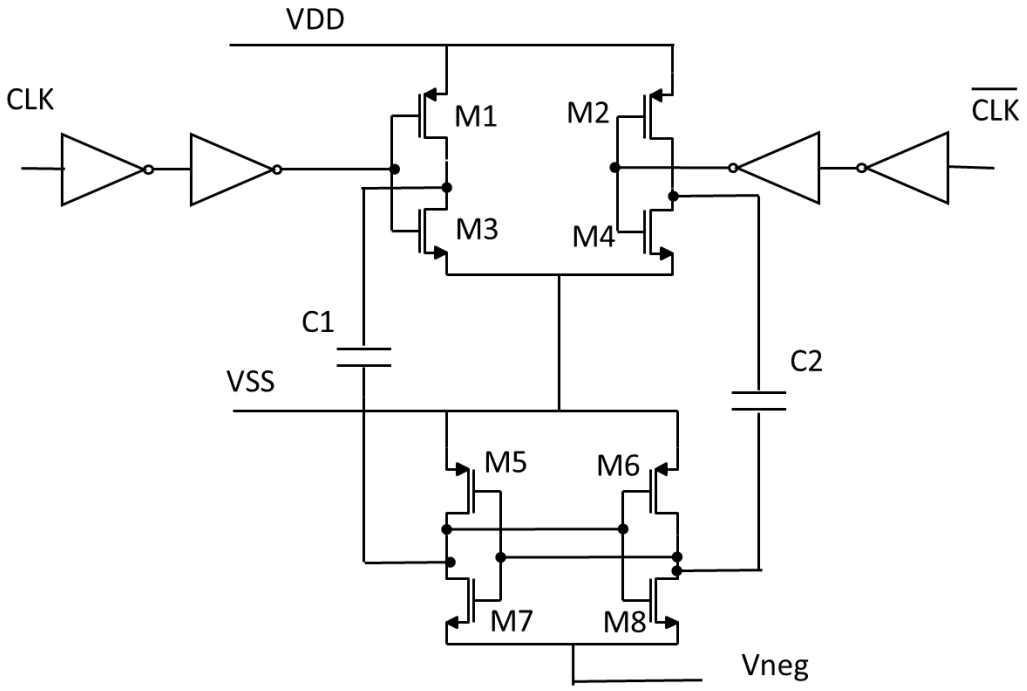


Figure 6-4 Schematic of charge pump

Chapter 7 VLC Part

It has long been known that light can be used for communications. Traditionally special lamps have been switched on and off rapidly in order to convey information and optical fibers can now carry data optically at rates of Gbits/s over long distances using coherent light from laser diode sources. However, it is also possible to modulate non-coherent light generated by lighting LED based lamps in order to carry large amounts of information over short distances without interfering with the intended function of illumination. If so, LED-based VLC systems will eventually realize the long-dreamed "communicate as you see" reality. Building into the existing LED lighting infrastructures, the novel LED-based VLC technologies will find countless application scenarios in hospitals (where RF is prohibited), airports, shopping malls, warehouses, smart traffic controls, advertisements, etc. An on chip VLC receiver is designed in this dissertation.

Optical receiver is one of the most important part in the VLC system, it enables the distorted and attenuated optical signal to be transferred into electrical signal after the optical signal propagates through the free space, followed with amplification block as shown in Figure 7-1 , then recover the digital signal from transmitter end.

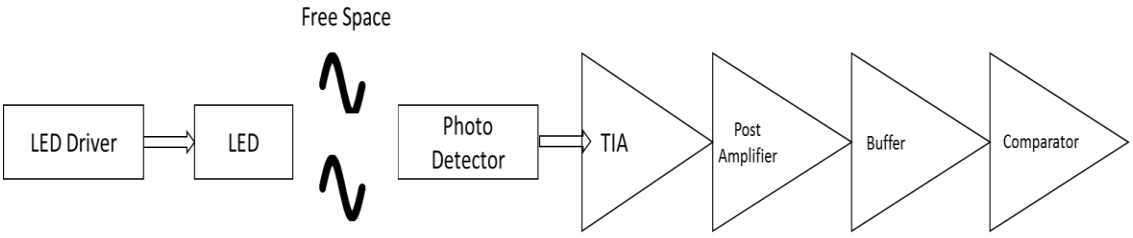


Figure 7-1 VLC transceiver block

7.1 Photodetector

Photodetector (PD) are sensors of light, which has a p-n junction that converts light photons into current. After a long propagation, the signal is already very weak when arriving at receiver end, so the detected current is normally in the order of uA. Basically, a good photodetector has the high light-electrical conversion efficiency, low noise and quick response time. The principle of photo diode is, when the diode is reverse biased, and there is no light, the weak reverse saturation current goes through the diode, and when there is light on the PD, it will generate electron-hole pair in depletion region, as these electron drift from depletion region to electrode, then the current occurs. In the IC design, the PD normally does not have a model in the PDK as a discrete off-die component, in order to get a reasonable analysis combining PD and TIA, an equivalent circuit is proposed as Figure 7-2.

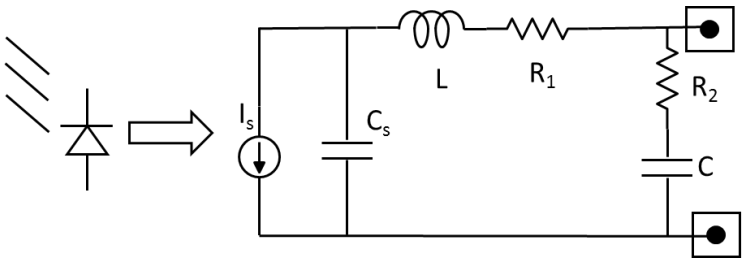


Figure 7-2 The equivalent circuit of Photo diode

Where I_s is the output current of PD with the order of uA. C_s is the parasitic capacitance which impacts the following TIA bandwidth significantly. The key design issue of receiver is to reduce the impact of C_s induced by PD as low as possible. The C_s varies from 0.1 pF to several pF which depends on the package, bias voltage and interconnects.

7.2 Transimpedance amplifier

Transimpedance amplifier (TIA) is the critical part of the VLC receiver, the function of that is to transfer the weak uA current to the voltage signal. Due to the weakness of voltage signal, it requires the characteristic of low noise. Furthermore, in order to keep the high sensitivity and reduce the Bit Error Rate (BER) of receiver, high gain is necessary for the TIA and bandwidth is another concern for the high data rate. Unfortunately, noise performance, bandwidth and gain are trade-offs in the TIA design. To some extent, TIA determines the whole performance of the VLC system, compared to normal amplifier with poor noise figure, a good TIA design should (1) reduce the input equivalent noise current to improve the sensitivity, (2) bandwidth is adaptive with the data rate, (3) high gain to make a system level low noise figure while cascading with the next stage circuit block. These three conditions are trade-offs, for example, the larger bandwidth will cause the larger noise and decrease of gain. In addition, when the temperature changes, the gain, bandwidth and sensitivity should keep stable. The input resistance should be small enough to minimize the impact of the parasitic capacitance of photodetector.

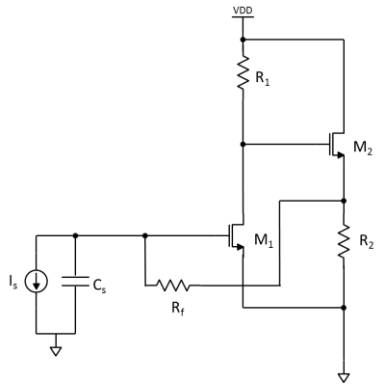


Figure 7-3 Common source TIA with source follower

The schematic of TIA is shown as Figure 7-3, I_s and C_s consist of the equivalent photodetector circuit model. The first stage is common source amplifier comprised of M1 and R1, followed by M2 and R2 acting as a source follower. The feedback resistor R_f is connected between the input and output, transfer the current into the voltage. The common source type is easy to implement and more stable at the price of low bandwidth due to its high input impedance.

The trans-impedance gain could be represented as

$$\frac{V_{out}}{i_{in}} = -\left(\frac{A}{A+1}\right) * \frac{R_f}{1+sC_T(\frac{R_f}{A+1})} \qquad 7.1$$

$$A = g_{m1}R_1 \qquad 7.2$$

Where A is the open loop gain, C_T is the input capacitance including the photodetector parasitic capacitance C_s and TIA input capacitance C_i

$$C_T = C_s + C_i = C_s + C_{gs1} + (1+g_{m1}R_1)C_{gd1} \qquad 7.3$$

From equation 7.1, the gain of this TIA is approximately R_f, and -3 dB bandwidth is

$$BW_{-3dB} = \frac{1}{2\pi R_{if} C_T} = \frac{1}{2\pi(R_f / A)C_T} = \frac{A}{2\pi R_f C_T} \qquad 7.4$$

There are three ways to enhance the bandwidth from equation 7.4. 1) Minimize the C_T, $C_T=C_s+ C_i$, and normally $C_s>>C_i$, so the C_T is determined by photodetector parasitic capacitance C_s. Therefore, as an off-chip component, picking up an appropriate photodetector is important. 2) Increase the open loop gain A, but A cannot be increased infinitely, due to the existence of miller capacitance, as the gain $A=gm_1R_1$ increases, the corresponding Ci will increase, thus decrease the bandwidth of TIA. On the other hand, a

cascade amplifier is able to increase total open loop gain, but it will introduce more poles so as to cause stability problem. 3) Minimize the feedback resistor R_f, however, the smaller R_f will induce more noise.

A improved common-source TIA is further proposed , the active load M1 and M4 replace the R1 and R2 in Figure 7-4. The final stage PMOS source follower is cascaded with middle-stage NMOS source follower to realize the voltage shift and isolation.

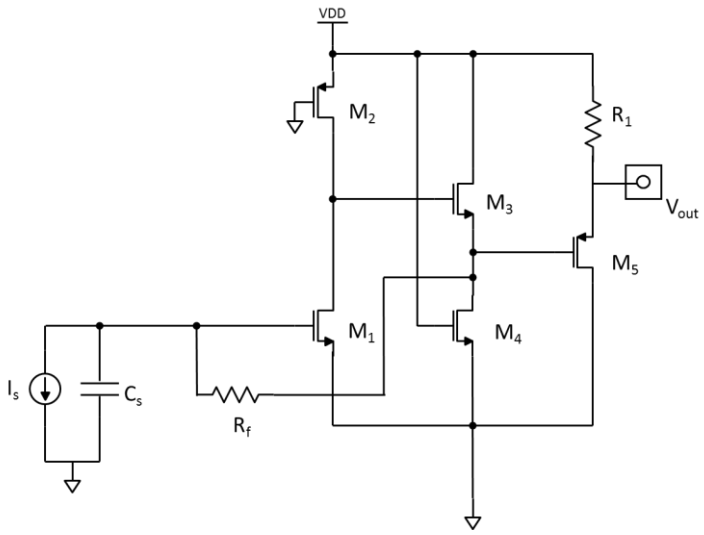


Figure 7-4 Improved common source TIA

7.3 Single to differential circuit

Due to the finite gain from TIA, the output voltage cannot achieve the design goal, therefore, a post-amplifier is needed, however, which is normally required a differential input, so a single to differential circuit (SDC) is necessary. The SDC circuit is shown as Figure 7-5, it's comprised of a MOS differential pair and a RC filter network. As it is working in the DC mode, there is no current flowing into the gate of M1 and M2, so there is no voltage drop over the R1, thus, the DC bias is the same for these two transistors.

However, as it is working in AC mode, the C_1 can be considered as a short, all the AC component is added between the M1 and M2, so as to make a single to differential transfer.

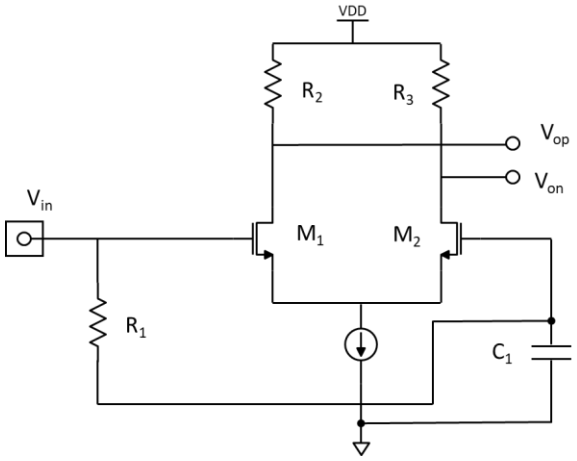


Figure 7-5 Single to differential circuit

7.4 Post-amplifier

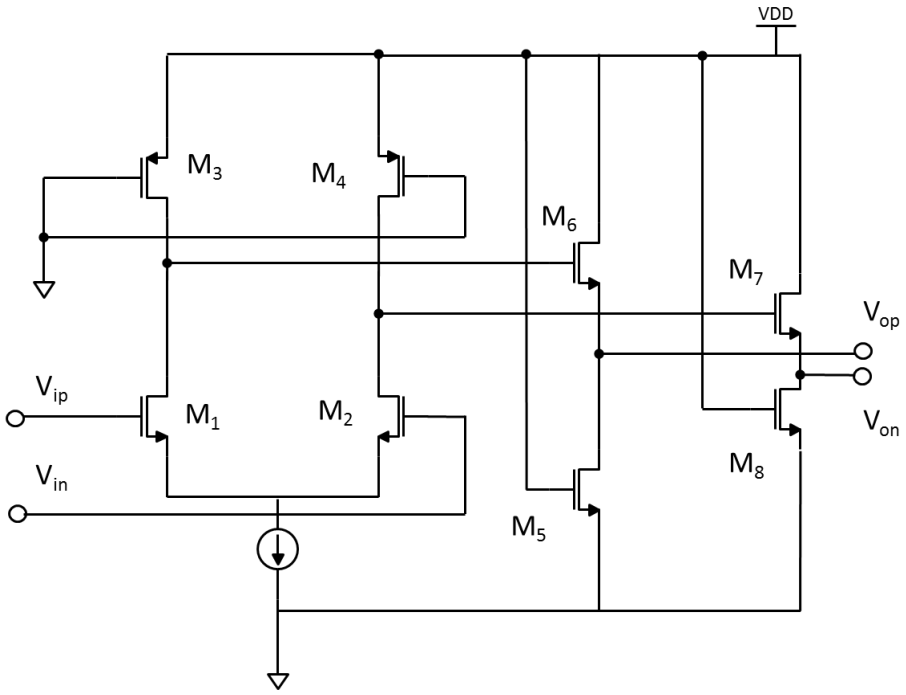


Figure 7-6 Schematic of post amplifier

The post amplifier as shown in Figure 7-6 consists of three-stage differential pairs to amplify the signal from SDC, each stage will provide 10 dB gain or so, after all, the total gain will achieve 30 dB, the gate width will be designed by balanced gain and bandwidth. Thus the post amplifier can provide strong signal to next stage.

7.5 Current mode logic (CML)

A Buffer is needed to drive the load to prevent the signal distortion. Conventionally, a CMOS inverter has a number of advantages. The static power dissipation of a CMOS inverter is negligible, as summing the leakage current to be small, and thus, is an ideal candidate for bus drivers and signal buffers in digital circuits. It shows an optimum performance with technology scaling and has a large noise margin. However, a CMOS inverter exhibits some drawbacks that prevent it from being vastly used in high-speed low-voltage circuits. First, a CMOS inverter is essentially a single-ended circuit. Recall that in high frequency range, the short on-chip wires act as coupled transmission lines. The electromagnetic coupling thus cause serious operational malfunctioning in the circuits, particularly single-ended circuits. Besides, the PMOS transistor in a static CMOS inverter will severely limit the maximum operating frequency of the circuit [45][46][47].

A CML buffer is based on the differential architecture. Figure 7-7 shows a basic differential architecture. The tail current bias provides an input independent biasing for the circuit. In the particular case of output drivers, a CML must drive a large off-chip load, the output driver must thus have a large current capability, and this means that NMOS transistor of last stage must be large. A large transistor has a large gate to channel capacitance that seriously degrades the propagation delay and the voltage swing of the

preceding pre-driver stage. To reduce the propagation delay of the pre-driver, a chain of tapered buffers is introduced. It is readily proved that the minimum delay is obtained by dividing the delay equally over all stages 0. The top layout of whole VLC receiver is depicted in Figure 7-8.

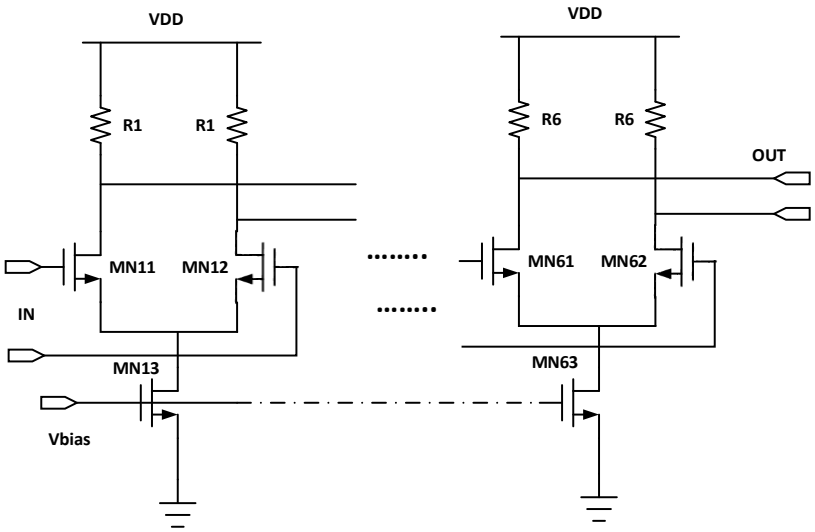


Figure 7-7 Schematic of a tapered multistage current mode logic

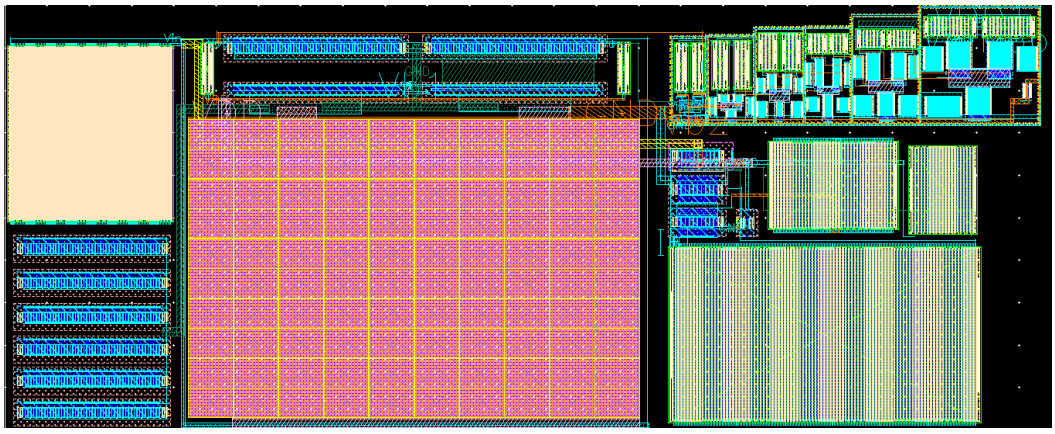


Figure 7-8 Whole layout of VLC receiver

Chapter 8 MIPI Control

8.1 MIPI Introduction

MIPI RF Front-End Control Interface (RFFE) is the specification of a bus interface specifically tailored for the needs of current and future mobile wireless systems to control the slave devices in an RF front-end. There are a variety of front-end device types, including PAs, Low-Noise Amplifiers (LNAs), filters, switches, power management modules, antenna tuners and sensors - and others may certainly appear, or already exist. The trend in mobile radio communications is towards complex multi-radio systems comprised of several parallel transceivers. This implies a leap in complexity for the RF front-end design and realization. The MIPI RFFE specification is designed to replace existing control solutions, such as SPI interfaces which suffer from a lack of standardization due to the variety of telegram structures despite the commonality afforded by similar signal structure. Dedicated analog or digital control lines also lack common definition, and consume a large number of pins and PCB area for the traces since they typically do not provide for multi-device support. Other potential candidates, such as I^2C, has never been an acceptable solution in sensitive wireless applications, since they lack some of the fundamental features desired. Thus, the RFFE bus must be able to operate efficiently from the simplest one Master and one Slave configuration to potential configurations with multiple Masters and tens of Slaves.

The key pillars of the RFFE RF Front-End Control Interface Specification include the following:

- Minimize the wiring interconnect demands in the RF front-end of a mobile terminal
- Minimize pin count for control in the RF front-end
- Optimization of control flow and ease of implementation
- Ensure minimal EMI contributions due to RFFE bus
- Minimize complexity for Slave devices
- Add flexibility and scalability, allowing use of advanced RF front-end architectures such as diversity and/or MIMO configurations
- Development of a standardized interface targeted to the needs of RF front-end control, providing a well-defined feature set, protocol, and electrical layer so as to foster interoperability and a basis for reuse, while also providing flexible options for growth.

The basic configuration of the RFFE interface and its bus structure are shown in Figure 8-1. RFFE requires two primary signaling lines - one serial bidirectional data signal (SDATA), and one clock signal (SCLK), which is controlled by the Bus Owner Master. Additional signals may be present on an RFFE device as a means for providing additional proprietary functionality, but shall not change the behavior of the RFFE interface protocol or prevent the operation of the RFFE bus as described in this specification. RFFE bus components are connected in parallel to the SCLK and SDATA lines of the bus. Power VIO can be supplied externally, or it may be sourced from the master device.

Figure 8-2 shows an example of Write Command Sequence in the Register 0, one of slave Registers. The Command Sequence starts with an sequence start condition (SSC), followed by the Register 0 Write Command Frame containing the Slave address, a logic

‘1’ (to denote the command type and address), and a seven bit word to be written into Register 0. The Command Sequence ends with a Bus Park Cycle, which is Master-initiated.

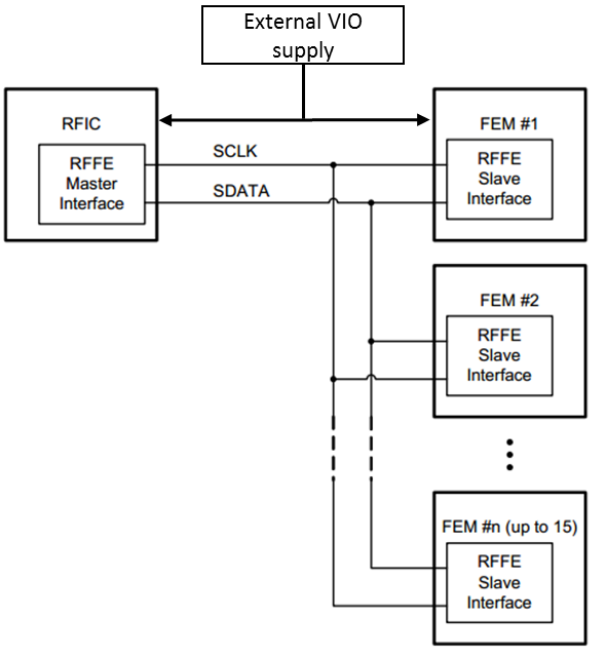


Figure 8-1 RFFE Interface and Bus Structure

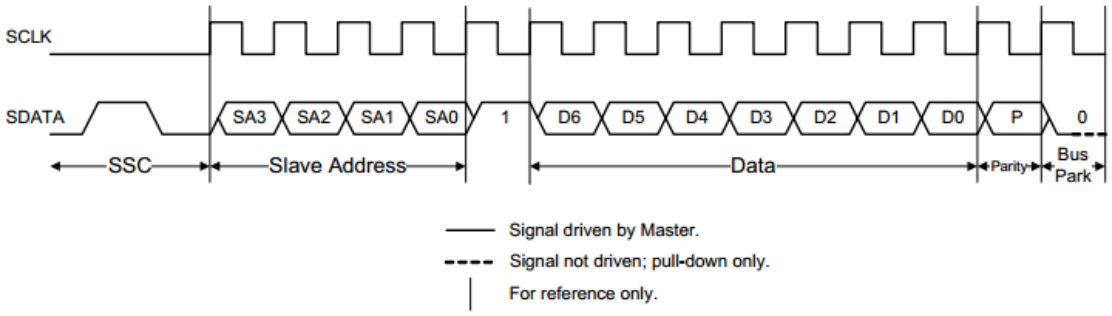


Figure 8-2 Register 0 Write Command Sequence

Follow this command definition; we can verify the MIPI circuit by simulation. A test of writing data to register# 0 (USID = 0001) in sequences has been demonstrated in Figure 8-3, 0001/0010…until 1111 was written in last four bits. The control logic of MMMB PA designed in Chapter 5 is presented in Table 8-1.

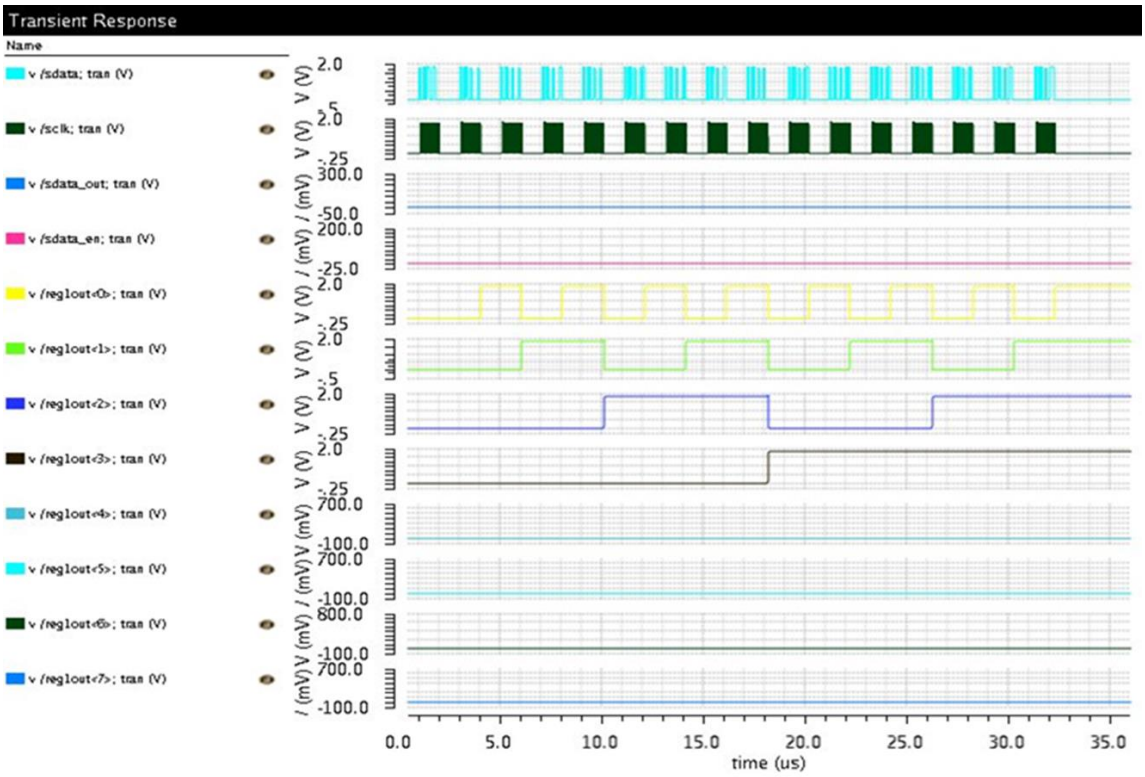


Figure 8-3 Simulation of MIPI writing sequence

Table 8-1 MIPI control logic of designed MMMB PA

Register 0	Description	Default	Notes1	Notes2
[7]	n/a	n/a		
[6:3]	PA band selection	0000		
	[6]	0	n/a	
	[5]	0	turn on/off local bg, Iptate, 4ma 2.5V ldo for LB PA	0=off, 1=on
	[4]	0	turn on/off local bg, Iptate, 4ma 2.5V ldo for MB PA	0=off, 1=on
	[3]	0	turn on/off local bg, Iptate, 4ma 2.5V ldo for HB PA	0=off, 1=on
[2]	PA disable	1	trun on/off global bg, 2.5V ldo for logics	1=All off, 0=All on
[1:0]	PA power mode	00	00: HPM, 10: LPM	0=off, 1=on
	[1]	0	trun on/off input feedback R for LPM	0=off, 1=on
	[0]	0	n/a	

Register 1	Description	Default	Notes1	Notes2
[7:4]	Iptate2 (output stage bias)	0110		
[3:0]	Iptate1 (driver stage bias)	0110		

Register 11	Description	Default	Notes1	Notes2
[7:3]	n/a	0		
[2:0]	PA_V_ctrl[2:0]	010	000~111 : 2.8V to 2.1V with 0.1V step.	010:2.6V

Register 18	Description	Default	Notes1	Notes2
[7:4]	MB/LB switch selection	0000	0000 = switch off	
			0001 = high isolation	
			0010 = LB1_TX	
			0011 = LB2_TX	
			0100 = LB3_TX	
			0101 = LB4_TX	
			0110 = LB5_TX	
			1010 = MB1_TX	
			1011 = MB2_TX	
			1100 = MB3_TX	
			1101 = MB4_TX	
			1110 = MB5_TX	
			1111= high isolation	
			rest combinations: high isolation ?	
[3:0]	HB switch selection	0000	0000 = switch off	
			0111 = B7_RX	
			1000 = B7_TX	
			1001 = B40_TX	
			1010 = B38_TX	
			1011 = B41_TX	
			1100 = B40_RX	
			1101 = B38_RX	
			1110 = B41_RX	
			1111= high isolation	
			rest combinations: high isolation ?	

Chapter 9 ESD Consideration

9.1 ESD Protection Introduction

ESD failure is a major reliability concern to integrated circuits (ICs) and electronic products (e.g. smart phones). As IC technologies continue migrating into beyond 40nm domain, ESD protection is emerging as a key IC design challenge, particularly for high-frequency operating at multi-GHz and high-speed ICs with data rates beyond multiple giga bits per second (Gbps) [48]. The ESD phenomenon originates from transfer of electrostatic charges between two objects of different electrical potential and the resulting fast and large ESD transients can damage ICs. One emerging ESD protection design challenges along with IC technology scaling-down is the ESD Design Window Shrinking Effect. As depicted in Figure 9-1, an ESD Design Window is defined by the breakdown voltage (*BV*) and power supply voltage (V_{DD}) of the core circuit under protection with a proper safe margin for practical IC designs [49][50]. An ESD protection solution requires accurate design of ESD-critical parameters including the ESD triggering voltage, current and time (V_{t1}, I_{t1}, t_1), the ESD holding voltage and current (V_h, I_h), the ESD discharging resistance (R_{ON}), and the ESD failure voltage and current (V_{t2}, I_{t2}). The rationale for setting the ESD Design Window is that the triggering of an ESD protection structure must be lower than the BV of the IC node protected ($V_{t1} < BV$) to prevent any ESD damage; meanwhile, to avoid latch-up effect, the holding voltage of an ESD protection structure has to be higher than the IC supply voltage (i.e., $V_h > V_{DD}$). Unfortunately, as IC technology scaling-down continues, BV of IC devices decreases dramatically, however, IC supply voltages only drop slightly, which results in a narrower ESD design window, i.e., ESD Design Window

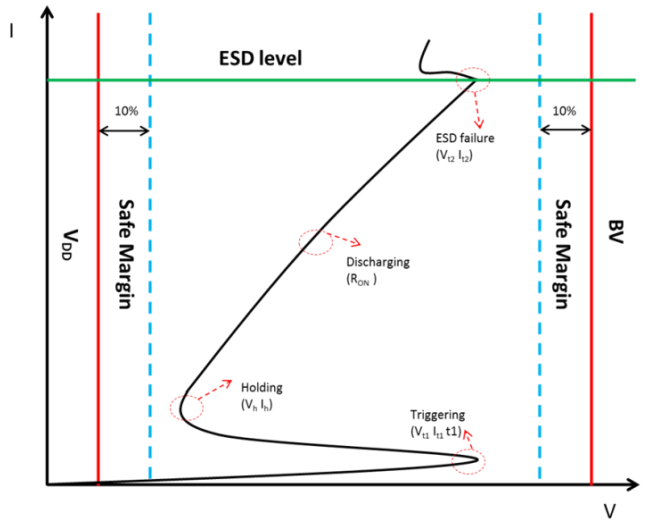


Figure 9-1 Illustration of typical ESD discharging I-C characteristics, ESD-critical parameters and the ESD design window.

Shrinking [51]. As such, a quantitative ESD protection design method is required for accurate ESD protection circuit designs in advanced IC technologies, especially for mixed-signal ICs involving multiple supply voltage domains [48]-[53].

On the other hand, ESD protection structures will inherently induce parasitic effects, such as parasitic capacitance (C_{ESD}) and noises, which will inevitably affect core IC performance, particularly for multi-GHz RF ICs and very high speed ICs with data rates above Gbps [48]-[50],[54] -[55]. Unfortunately, RF ICs used for consumer electronics, such as smart phones, typically require more robust ESD protection, which normally means larger ESD protection structures, hence, more ESD-induced parasitic parameters. Therefore, a comprehensive ESD-IC co-design technique is imperative for advanced RF and mixed-signal ICs in order to ensure simultaneous design optimization of both the core IC and the ESD protection performance at full chip level [54]-[56]. For example, without careful and quantitative ESD-IC co-design, it would be impossible to design high-speed I/O circuits for next-generation backbone communication systems of beyond 40Gbps [57].

Efforts have been made to develop advanced ultra-low parasitic ESD protection structure with minimized C_{ESD}. For extremely, a dispensable ESD design concept was reported for 40-100Gbps ICs [58]. A comprehensive ESD design methodology will be discussed in this chapter which is already verified in a CMOS 28nm technology.

There are three primary ESD models considered in the microelectronics industry: Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) as shown in Figure 9-2 [59].

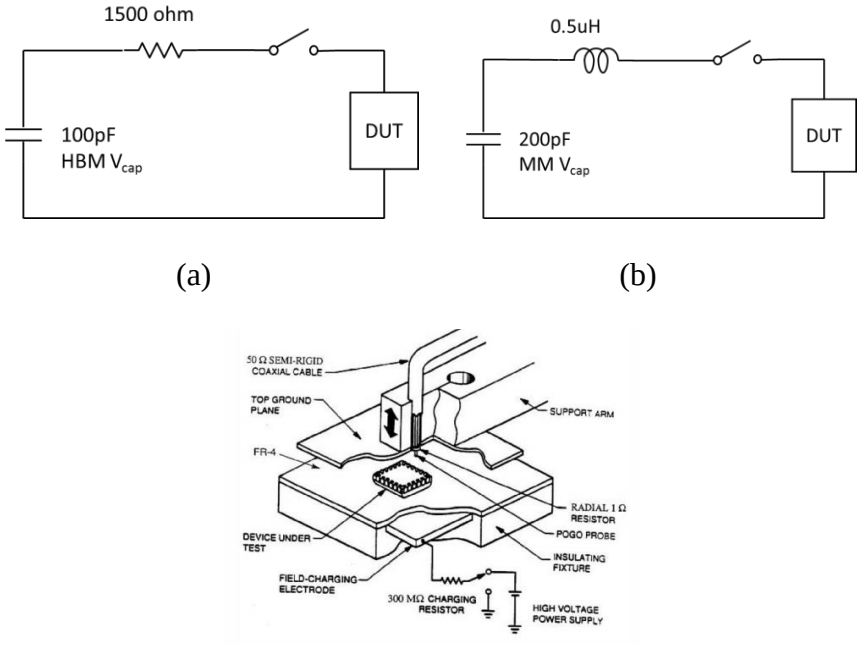


Figure 9-2 Common ESD discharge modes (a) Human Body Model (b) Machine Model (c) Charged Device Model

The human body model represents a human body discharging through the IC module to ground. The equivalent circuit for HBM is a 1.5kΩ resistor in series with a 100pF capacitor. The capacitor is charged to the specified ESD voltage, and then the switch is closed and the current flows through the Device Under Test (DUT). An HBM ESD event

occurs between any two pins on a module. HBM has the longest duration of the three primary models, but it has the lowest current for a given ESD voltage, for the 2KV HBM current waveform, it has unidirectional 1.5A peak current and 100 ns pulse width. Similar to HBM, the MM ESD event occurs across any two pins on a module. MM however, simulates a tool discharging across the two pins. This event is more rapid than HBM and has a higher current level. The waveform is also quite a bit different – the MM waveform is a bidirectional damped oscillation. For a normal 200V MM model waveform, it features a peak 3A current. Unlike HBM and MM, CDM ESD events only involve a single pin on the module. CDM is a very high current event, but occurs in a very short time interval. CDM testing is generally accomplished only on packaged chips. A field plate is used to induce a specified charge on the module, and then a probe with a low resistance path to ground is brought into contact with a single pin to discharge the module. This procedure is repeated for each pin on the module, and a functional test employed after CDM stressing is completed to determine if the module has been damaged.

Transmission Line Pulse (TLP) measurement as shown in Figure 9-3 is not ESD specifications, but rather a diagnostic tool used to understand the behavior of devices under

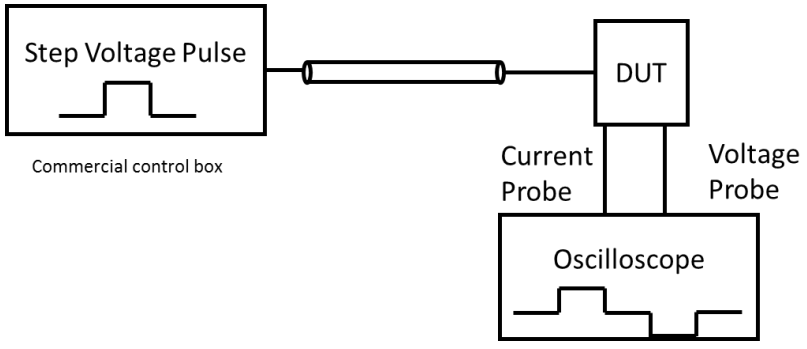


Figure 9-3 Transmission line pulse testing

the very high current conditions encountered in an ESD event. Pulsed measurements replicate the temporal behavior of the ESD event and avoid energy levels that would destroy the device in a DC measurement. Since an ESD discharge behaves like a current pulse it is reasonable to replace the charged capacitor by either a pulsed current source or a charged coaxial cable, either of which will create a rectangular current pulse. An oscilloscope is used to measure the current and voltage across the device during the discharge. The pulse width can be varied to study different types of discharge events or to gain additional understanding about the temporal dependence of device behavior at very high current levels. Transmission line pulse testing measures high current pulsed I-V characteristics using square pulse, with 100ns for HBM emulation, and 1~2 ns for CDM emulation.

ESD failures are categorized into gate oxide rupture, metal opens, or silicon electrothermal failure. CDM typically causes gate oxide rupture. HBM and MM can cause all three failure modes.

9.2 Mixed-Mode ESD Protection Design

The whole-chip ESD-IC co-design flow starts with ESD protection structure design prediction and optimization using a mixed-mode ESD protection simulation design technique, which allows designers to conduct quantitative design to define the ESD-critical parameters of ESD structures [60][61]. This mixed-mode ESD simulation design approach has several advantages: First, quantitative ESD protection design makes ESD design prediction possible before Si. Second, accurate design of ESD-critical parameters helps designers to deal with the ESD design window shrinking effect. Third, accurate design

enables ESD design optimization that delivers robust ESD protection structures with minimized parasitic effects, a critical goal for RF and high-speed ICs. Fourth, accurate ESD simulation design allows IC designers to select suitable ESD structures specific tailored for ICs under design. ESD protection design optimization in this work was conducted using the mixed-mode ESD simulation method.

9.2.1 Poly-Gated Diode ESD Structures

This study involves a large group of common ESD protection structures with different dimensions in 28nm CMOS in order to comprehensively understand the ESD impacts on core circuit performance. Figure 9-4 depicts the cross-section of a gated diode ESD

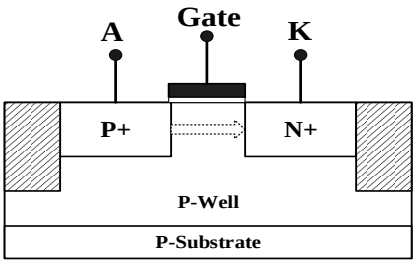


Figure 9-4 A cross-section and ESD current discharging path for a poly-gated diode ESD protection structure in 28nm CMOS.

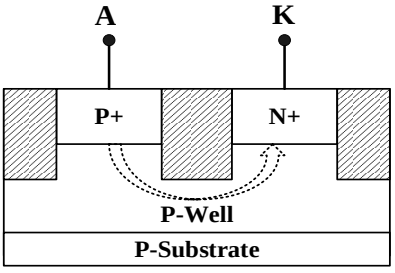


Figure 9-5 A cross-section and ESD discharging path for an N+/P-well STI diode ESD device. ESD current crowding at STI reduces ESD protection capability.

structure where a poly gate is used to isolate the cathode (K formed of N+) and anode (A formed of P+). A gated diode is used in 28nm CMOS, much like a field oxide isolated PN diode in relatively old CMOS technologies. There are two main advantages for the gated-

diode ESD device. First, the large ESD current can be conducted *directly* through the shallow *lateral* discharging path between the N+ and P+ diffusions without a sharp turning as in a STI diode, resulting in a low discharging R_{ON}. Second, ESD discharging path is very short as defined by the 28nm CMOS channel, which also ensures a low R_{ON}. Therefore, the ESD protection capability of a gated-diode ESD device shall be stronger than that of a shallow trench isolation (STI) diode ESD structure to be discussed later, which is confirmed in testing. In ESD design, the gate must be properly biased for a gated-diode ESD device in order to avoid unexpected channel turn-on in normal IC operation. The downside is its relatively high leakage current.

9.2.2 STI Core and I/O Diode ESD Structures

STI isolation is a standard feature in 28nm CMOS. STI diode can be easily designed for ESD protection. Figure 9-5 illustrates the cross-section of sample N+/P-well STI diode ESD structure designed in this work, where the N+ diffusion (K) and P+/P-well diffusion (A) are separated by a STI plug. In a typical on-chip ESD protection scheme, the STI diode ESD devices are used at I/O to discharge ESD surges in forward mode in combination of a power clamp structure. Since a STI plug has very short dimension (e.g., 150nm in one design split), STI diode ESD structures can be made very small, hence reducing ESD-induced parasitic effects and alleviating ESD layout burden. On the negative end, with a narrow STI plug between A and K terminals, the large ESD discharge current has to make sharp turns in ESD current conduction, resulting in severe current crowding at the bottom of a STI plug that affects ESD protection capability. This phenomenon is confirmed by both simulation and testing. The foundry 28nm CMOS offers both core (0.85V) and I/O

(1.8V) process modules. Accordingly, we designed STI diode ESD devices in both core and I/O process modules in this work.

9.2.3 STI and Gated Diode ESD Structure Simulation

It is essential to conduct mixed-mode ESD simulation design to fully understand the ESD discharging behaviors inside an ESD structure, to optimize ESD performance, to minimize its parasitic effects and to predict ESD performance at chip level. This ESD simulation-design method can not only ensure ESD design performance, but also reduce ESD design costs and IC design cycles, both are often affected by ESD design iterations. There exist several ESD test models including the HBM, which was used for ESD characterization [62]. Figure 9-6 illustrates the equivalent circuit of HBM ESD test model, where a human-body-induced capacitance C is charged up, then discharges into the device under test (i.e., DUT, being an ESD protection device under test) through a typical human body resistor R and a discharging inductor L. Figure 9-7 shows a typical HBM ESD discharging source current waveform used to stress an ESD protection structure under test during mixed-mode ESD simulation. Figure 9-8 depicts simulated cross-section, heat distribution and temperature contours, therefore the transient ESD discharging behaviors, for sample STI and gated diode ESD structures under the same ESD stresses. It is clearly observed that the ESD discharging current tends to crowded around the bottom of a STI plug, hence, more severe heat crowding in the STI diode than in the gated diode ESD device. This can substantially affect ESD protection capability of a STI diode ESD structure. For the given ESD protection targets, ESD device sizes were accurately selected by mixed-mode ESD simulation. Figure 9-9 shows transient ESD I-V curves for sample STI diode

ESD devices with finger width of 60µm, 100µm and 120µm that passed 2kV, 3kV and 4kV ESD stressing, respectively. All ESD-critical parameters, including V_{t1}, I_{t1}, V_{t2}, I_{t2} and R_{ON}, are obtained in ESD simulation, which allows accurate ESD protection designs for 28nm core and I/O CMOS process modules to meet the required ESD design window.

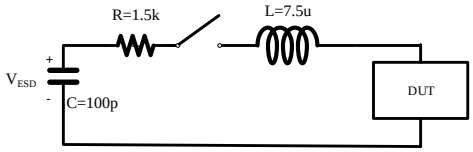


Figure 9-6 An equivalent circuit for HBM ESD discharging simulation.

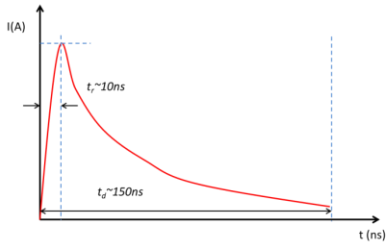


Figure 9-7 Typical HBM ESD discharging source current waveform used in mixed-mode ESD protection simulation.

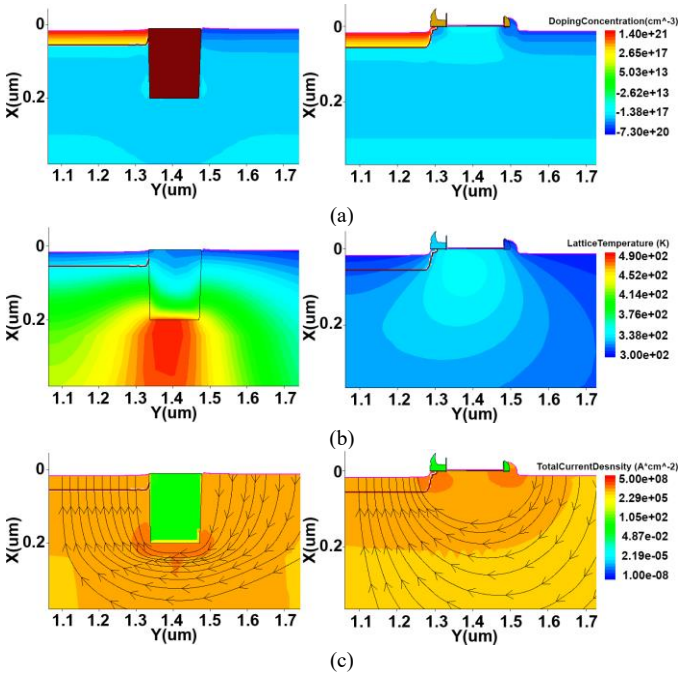


Figure 9-8 Simulated cross-section (a), temperature contours and heating effect (b), and ESD discharging current flows (c) for sample STI core diode (Left) and poly-gated diode (Right) ESD protection structures under the same ESD stressing condition.

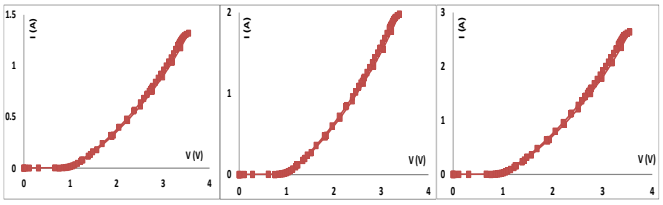


Figure 9-9 Simulated transient ESD discharging I-V curves for sample STI core diode ESD devices with different sizes: (a) 60µm, (b) 100µm and (c) 120µm.

9.2.4 DTSCR ESD Structure Simulation

Silicon-controlled rectifier (SCR) ESD structures are widely used for its excellent ESD protection capability, compact size and low ESD-induced parasitic effects. To reduce V_{t1} of an SCR ESD structure for low-voltage ICs, various trigger-assisting techniques were reported for modified SCR ESD structures [49][63]. Figure 9-10 shows a diode-triggered SCR (DTSCR) ESD protection structure suitable for low-voltage ICs in 28nm CMOS. A

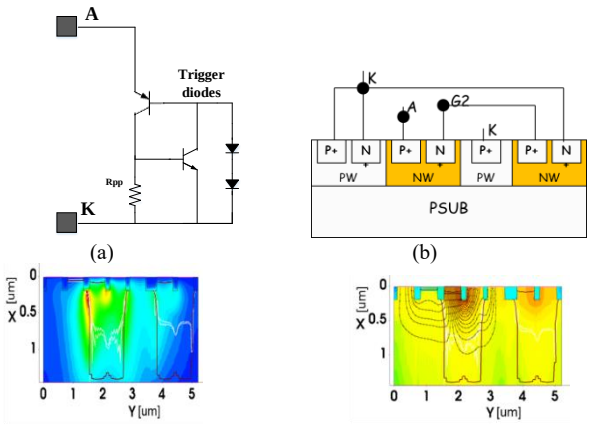


Figure 9-10 A Schematic (a), cross-section (b), ESD discharging current distribution (c) and temperature contour (d) of a sample DTSCR ESD protection structure using two diodes by ESD simulation.

DTSCR works in a way that the trigger-assisting diode is turned on first by ESD transients at low voltage, which then triggers the SCR structure to form a low-R_{ON} ESD discharging path to achieve robust ESD protection. Typically, the trigger-assisting diode can be built inside a SCR structure for a compact DTSCR layout. Figure 9-10 shows simulated transient

ESD discharging details for a sample DTCSR ESD structure by mixed-mode ESD simulation, which verifies the ESD design method again.

9.3 Scalable ESD Device Behavioral Modeling

A new accurate and scalable ESD device behavior modeling technique is developed to enable whole-chip ESD protection circuit simulation. Figure 9-11 depicts the new scalable ESD device behavior modeling flow. First, ESD protection devices are designed, fabricated and measured to obtain the ESD-critical parameters (V_{t1}, I_{t1}, V_h, I_h, R_{ON}, V_{t2} and I_{t2}) as shown in Figure 9-12. Comprehensive TLP ESD testing, featuring ESD pulse rise time t_r~10ns and duration t_d~100ns, plays a key role in this step. Extraction and analysis of the ESD-critical parameters from the TLP testing results were then

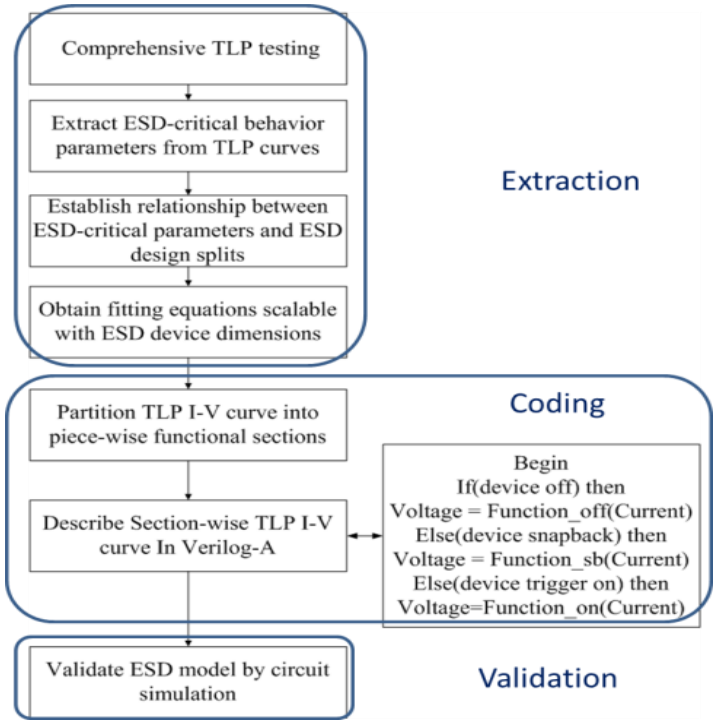


Figure 9-11 A flow chart of the new ESD behavioral modeling technique.

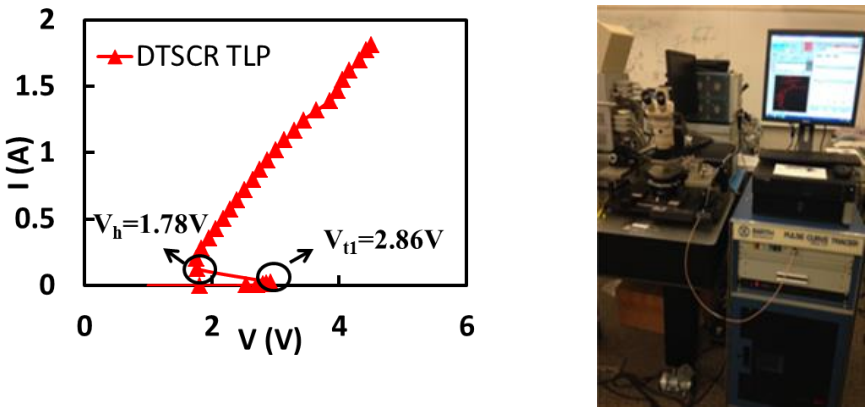


Figure 9-12 Measured ESD I-V curve for a sample DTSCR ESD structure by TLP testing (a) and the TLP tester set-up (b) used in this work.

performed. The relationship between ESD-critical parameters and ESD design splits can then be established to deliver accurate and scalable ESD device behavior models. Second, the ESD I-V curves from TLP testing are divided into several sections according to ESD discharging functions (e.g., device OFF, snapback and ON). Each section can be described by Verilog-A and the fitting parameters are extracted from the TLP I-V curve and correlating with device dimensions. Behavioral ESD modeling can accurately describe the ESD discharging I-V behaviors piece-wisely using Verilog-A for the TLP I-V curves, which were then verified by SPICE circuit simulation.

9.3.1 Poly-Gated Diode ESD Device Modeling and Verification

Developing accurate and scalable ESD device models requires carefully correlating the measured results with ESD design features, including ESD device sizes and layout patterns. Table 9-1 compares measured ESD-critical parameters I_{t2} and R_{ON} for sample poly-gated N+/PW diode ESD devices with different sizes. Figure 9-13 depicts the measured I_{t2} and R_{ON} versus the gated diode width (W) relationship. Equations 9.1 and 9.2 are extracted to

fit into the measured ESD behaviors for Verilog-A modeling. Similarly, all other ESD-critical parameters (V_{t1}, I_{t1}, V_h, I_h and V_{t2}) can be extracted from TLP testing and described by Verilog-A. An N+/PW gated diode ESD structure of W=60 and L=0.54μm is selected as an example to describe the ESD behavior modeling flow. Figure 9-14 (a) shows that the measured TLP curve is divided into multiple sections according to its measured ESD discharging behaviors, with its fitting formulas obtained for the different I-V sections. P+/NW gated diode scalable behavior models were generated similarly. Many poly-gated N+/PW and P+/NW ESD diodes with varying dimensions were used for behavior model extraction and verification. SPICE circuit simulation was then conducted to verify the extracted ESD behavior models.

$$I_{t2} = 0.0358 \times W + 0.238 \qquad 9.1$$

$$R_{ON} = -0.0251 \times W + 2.002 \qquad 9.2$$

Table 9-1 TLP results for different size N+/PW gated diodes

W(μm)	I_{t2}(A)	R_{ON}(Ω)
20	0.954	1.5
40	1.67	0.998
60	2.45	0.859

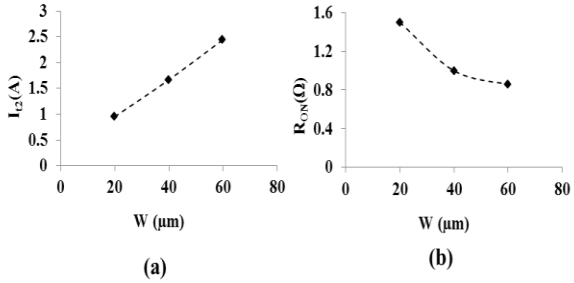


Figure 9-13 Measured I_{t2} (a) and R_{ON} (b) versus ESD device width (W) for sample N+/PW gated diode ESD devices.

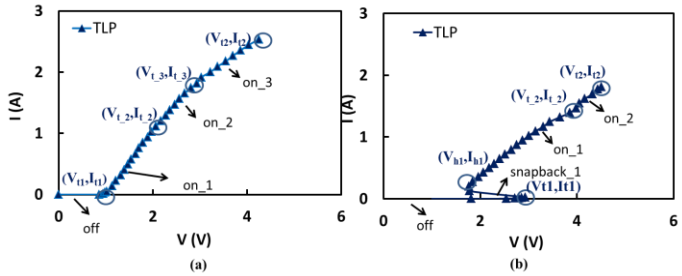


Figure 9-14 Partitioning TLP testing I-V curves for ESD behavior modeling for sample N+/PW gated diode (a) and DTSCR (b) structures.

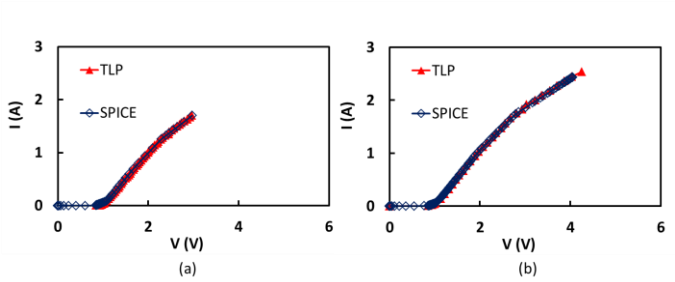


Figure 9-15 SPICE circuit simulation matches TLP testing I-V curves well for sample N+/PW gated ESD diode: (a) W=40μm and (b) W=60μm.

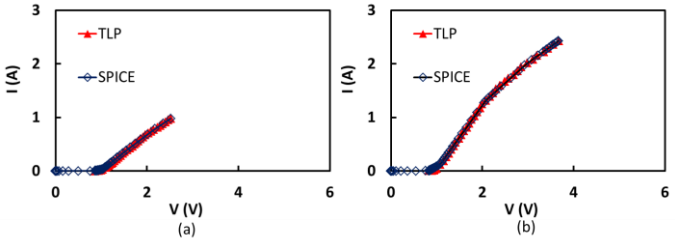


Figure 9-16 SPICE circuit simulation matches TLP testing I-V curve well for sample P+/NW gated ESD diode: (a) W=20μm and (b) W=60μm.

Figure 9-15 shows that SPICE-simulated ESD circuit function using the extracted ESD models for two samples of N+/PW gated diodes in 28nm CMOS (W/L=40/0.54μm, 60/0.54μm), which matches the measured TLP I-V curves very well, confirming that the new scalable ESD behavior modeling technique works. Figure 9-16 compares ESD I-V curves from TLP testing with those from SPICE circuit simulation using the extracted ESD behavior models for two sample P+/NW gated diode (W/L=20/0.54μm, 60/0.54μm), which again show excellent agreement and scalability of the new ESD behavior models.

9.3.2 DTSCR ESD Device Modeling and Verification

The new ESD behavior modeling technique was applied to DTSCR ESD structures. Figure 9-14 (b) shows TLP testing I-V curve partitioning and fitting for a sample DTSCR of W=50μm that uses a string of two diodes for trigger-assisting and was designed for HBM 2KV ESD protection. Figure 9-17 shows the SPICE-simulated ESD circuit function using the extracted ESD models that matches the TLP testing I-V curve very well for the two-diode DTSCR ESD structure. The excellent matching between SPICE circuit simulation using the extracted ESD models and the TLP testing I-V curves validates the new scalable ESD behavior modeling technique, which is critical to realizing full-chip ESD circuit simulation and ESD-IC co-design simulation in order to achieve chip-level ESD design prediction.

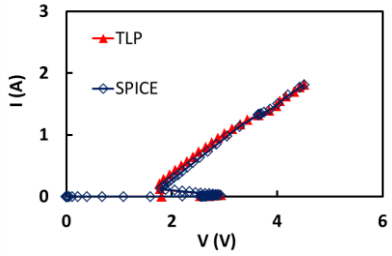


Figure 9-17 SPICE circuit simulation using the extracted ESD model matches the TLP testing I-V curve well for a sample DTSCR ESD structure (W=50μm).

9.4 Backend ESD Interconnect Characterization

Design of standalone active ESD protection devices in Si is certainly important, which reflects how well an individual Si ESD device behaves. However, without careful and quantitative design of ESD metal interconnects, whole-chip ESD protection circuit may not work as expected [64]. Hence, ESD damage to backend metal interconnects should be

considered. Figure 9-18 shows a full ESD protection block circuit consisting of an active ESD device and its metal connect (Si ESD device + metal), which shall be considered as a series circuit to meet the ESD design window requirement. It hence follows: $R_{ON} = R_{ON\text{-}Si} + R_{ON\text{-}M}$, $V_C = V_{C\text{-}Si} + V_{C\text{-}M} < BV$, $V_{C\text{-}Si} \leq V_{t2\text{-}Si}$, $V_{C\text{-}M} \leq V_{t2\text{-}M}$, $I_{ESD} = Min\{I_{ESD\text{-}Si}, I_{ESD\text{-}M}\} \leq Min\{I_{t2\text{-}Si}, I_{t2\text{-}M}\}$ where "Si" refers to Si active ESD devices, "M" refers to ESD metal interconnects, V_C is the ESD clamping voltage between the nodes to be protected, I_{ESD} is estimated chip level peak sustainable ESD current limited by either thermal melting or Si breakdown. Normally, a foundry PDK provides metal current handling specs characterized by DC and AC stressing, which are almost useless for ESD design because ESD transient are extremely fast and high surges with short duration. Historically, a PDK may suggest a universal metal width for all ESD protection level, which is oversimplified. That means the over-designed ESD metal will induce extra capacitance due to metal coupling, which is unacceptable particularly to high speed I/O circuits. In order to design ESD protection structures for a specific circuit, a metal set in term of different layers, width, length, inter-layer dielectric (ILD) was characterized by TLP testing for the standalone I_{t2} in this work.

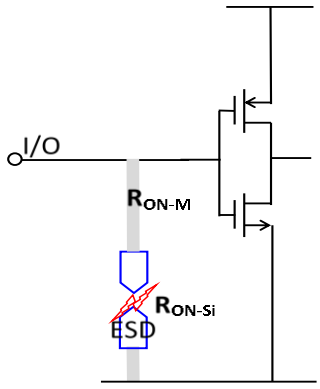


Figure 9-18 Illustration of a metal line connecting an ESD device to a pad ($R_{ON\text{-}M}$ is metal line resistance; $R_{ON\text{-}Si}$ is ESD discharging resistance of active ESD device).

Table 9-2 28nm CMOS Metal Interconnect Features

Metals[#]	*Thickness**	*Dielectrics*	*Length (μm)*	*Width (μm)*
M1	9%	ILD1	50, 150	1.5, 2.5, 4.5
Mx	9%	ILD1	50, 150	1.5, 2.5, 4.5
My	19%	ILD2	50, 150	3.0, 6.0, 9.0
Mr	125%	ILD3	50, 150	3.0, 6.0, 9.0

[#] *x=2, 3, 4, 5, 6; y=7, 8; r=9, 10 for top metals.*
** Weighting factors for thickness used for universal foundry technologies.*

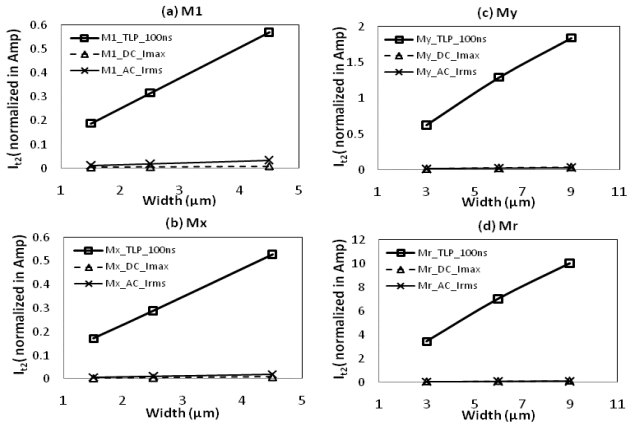


Figure 9-19 Measured I_{t2} for all metals by TLP with t_d = 100ns compares with DC and AC stressing data from PDK (data normalized to be foundry independent).

A systematic and quantitative study of backend interconnects for transient ESD protection at full chip level was performed for a 1P10M (10 Cu metals) interconnect option. The 28nm process features all-Cu 1P10M interconnects coded as M1, Mx, My and Mr with features given in Table II. Figure 9-19 presents the extracted I_{t2} data for all metals for different metal line widths measured by TLP pulse (t_d=100ns), in comparison with that by DC and AC thermal stressing data given in the PDK. Obviously, both PDK DC and AC metal stressing results are almost useless to ESD metal design, which must be evaluated by transient TLP testing. A wider metal line provides higher I_{t2}, but the trade-off is the increased ESD-metal-induced capacitance at chip level.

9.5 ESD Parasitic Parameter Extraction

Accurate ESD parasitic parameter extraction is a key to evaluating ESD impacts on high-speed ICs and realizing full-chip ESD-IC co-design. As shown in Figure 9-20, two GS-type ESD de-embedding patterns, A (full ESD structure) and B (Si ESD structure removed), were designed to accurately extract the ESD-induced capacitance by testing.

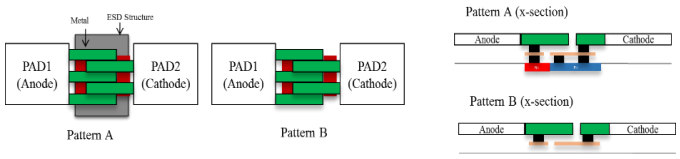


Figure 9-20 Top view and cross-section for the de-embedding ESD testing patterns A (full ESD structure) and B (Si structure removed) used in this work.

Figure 9-21 depicts the new Y-model equivalent circuit method, which are used for accurate testing and extraction of ESD capacitance associated with the ESD device in Si (C_{ESD}), ESD metal interconnects (C_{metal}) and pads (C_{pad}), respectively, hence, including all ESD-induced parasitic capacitance. Figure 9-22 shows the new test flow. Figure 9-23 depicts the extracted C_{ESD} values for sample gated diode and DTCSR ESD devices for 2kV, 3kV and 4kV targets. Such measured C_{ESD}~kV curves are critical to beyond-10Gbps and multi-GHz ICs for chip level design trade-offs to achieve both ESD and circuit performance on a chip for balanced overall performance.

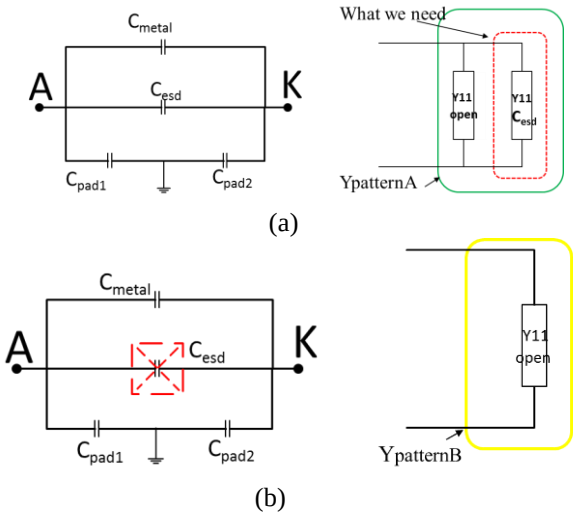


Figure 9-21 A Y-parameter circuit model for (a) ESD pattern A and (b) pattern B.

Test flow:

- ❑ Test S parameter of pattern A and pattern B separately.
- ❑ Transfer the S parameter into the Y parameter.
- ❑ $Y_{esd} = Y_{patternA} - Y_{patternB}$
- ❑ C_{esd}=IM(Y_{esd})/(2*pi*freq)

Figure 9-22. The new C_{ESD} extraction testing flow in this work.

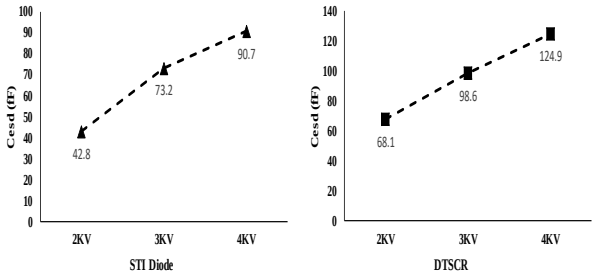


Figure 9-23 Extracted C_{ESD} for STI diode (a) and DTSCR (b) ESD devices for 2kV, 3kV & 4kV using Y-model and S-parameters measured by a VNA E8363B.

9.6 ESD Co-Design Evaluation

High-frequency and high-speed ICs can easily be affected by C_{ESD}, which can only be addressed by whole-chip ESD-IC co-design. Systematic evaluation of ESD parasitic effects on multi-GH and multi-Gbps ICs was conducted by using ring oscillator, I/O buffers, CML circuits and transmitter in this work.

9.6.1 ESD-Protected Ring Oscillator

A ring oscillator with odd number of inverters is widely used as a reference clock or for process evaluation [65]. Its beat frequency may easily be affected by ESD-induced C_{ESD}. Figure 9-24 depicts an evaluation circuit consisting of N-stage ring oscillator, ESD device and an out buffer. The impact of C_{ESD} is determined by degradation of ring oscillator beating frequency. Three ring oscillator splits of 5/7/37 stages, respectively, were designed with 2/3/4 kV ESD STI diodes in this work. Figure 9-25 shows the output transient waveform of a 37-stage ring oscillator with different ESD protection, which clearly shows that its beat frequency degrades as ESD protection level increases. Figure 9-26 summarizes the beat frequency versus ESD level matrix, clearly showing the substantially negative ESD impacts on ring oscillator circuits.

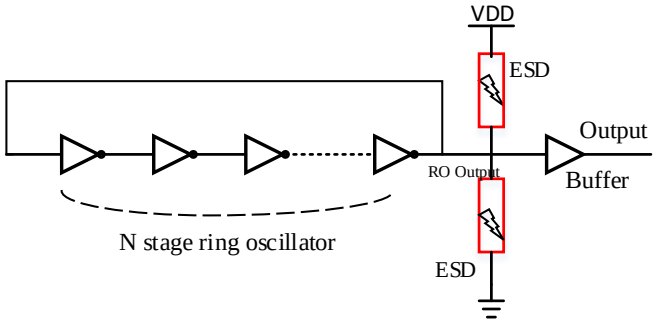


Figure 9-24 Schematic of ESD-protected ring oscillator evaluation circuit.

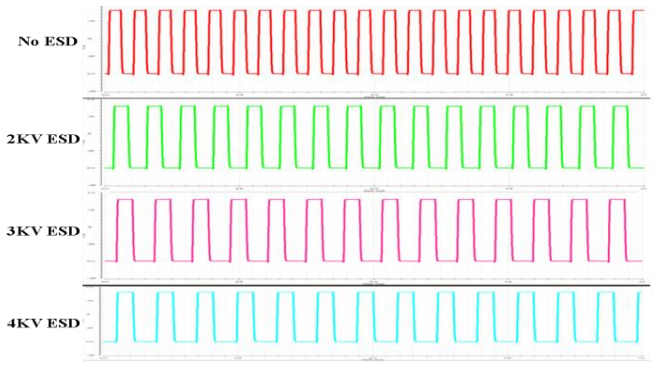
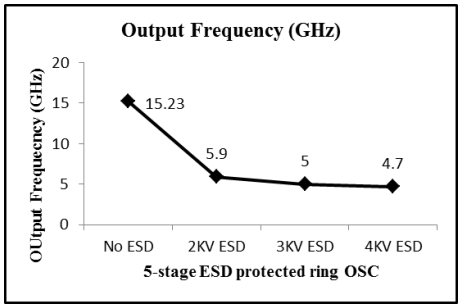
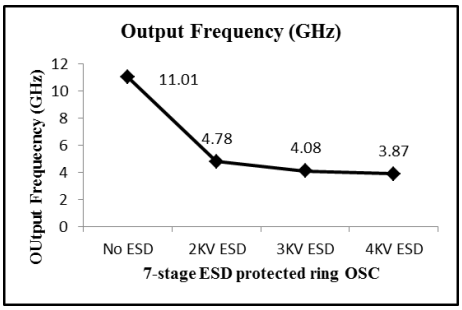


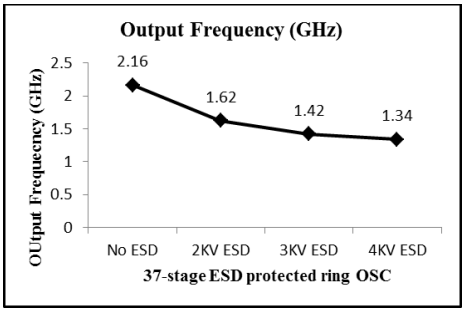
Figure 9-25 Output waveform of a 37-stage ring oscillator with different ESD protection levels using STI diode ESD structures.



(a)



(b)



(c)

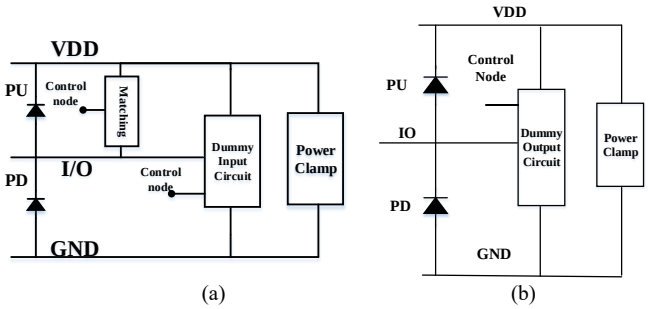
Figure 9-26 Mapping the ring oscillator beat frequency with ESD protection levels: (a) 5 stages, (b) 7 stages and (c) 37 stages.

9.6.2 ESD-Protected Dummy Input and Output Buffers

Figure 9-27 shows ESD-protected high-speed dummy I/O buffer circuits designed in 28nm CMOS for up to 40Gbps used to evaluate ESD parasitic effects on ICs. To accurately evaluate ESD impacts on IC data rates, four IC splits with various ESD devices and targets (2kV, 3kV & 4kV) are used as shown in Table 9-3: **Split-1** is core IC without ESD, **Split-3** is Split-1 with **full** ESD structure, **Split-2** is Split-3 with the **Si** ESD device removed (i.e., C_{ESD}=0), and **Split-4** is Split-3 plus BGA package-induced capacitance. Figure 9-28 is the return loss results for dummy I/O circuits with different ESD protection levels evaluated using the CEI-28G-SR standard [66], which clearly shows significant impacts of ESD (C_{ESD}, C_{metal}, C_{pad}) and package on high-speed IC throughputs. Figure 9-29 depicts the accurate mapping between IC data rates and ESD protection levels obtained for the circuit splits in 28nm CMOS, which is a critical reference for high-speed IC designs to balance the needs for robust ESD protection and beyond-10Gbps ultra high throughputs.

Table 9-3 ESD+IC co-design splits

Splits	ESD	ESD Features
Split-1	No	N/A
Split-2	Yes	Split-3 with Si ESD device removed
Split-3	Yes	Full ESD cell: Si + metal
Split-4	Yes	Split-3 + BGA package capacitance



(a) (b)

Figure 9-27 Schematic of high-speed dummy I/O circuits with different ESD protection structures: (a) Input buffer and (b) Output buffer.

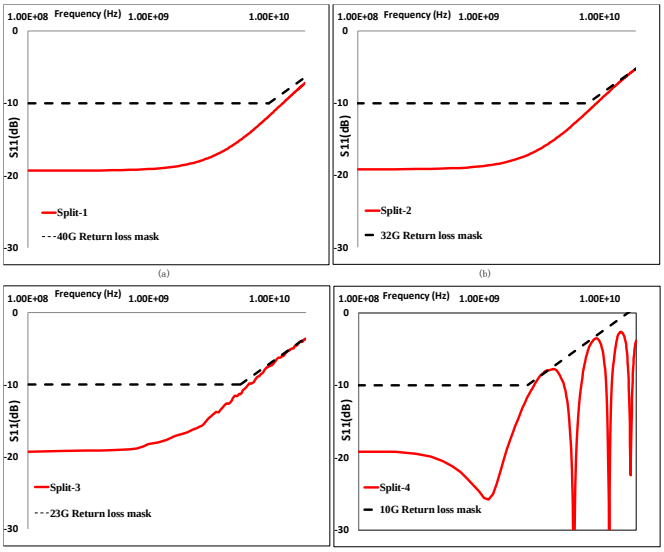


Figure 9-28 Return loss obtained per CEI-28G-SR standard for I/O circuits using STI ESD diodes show ESD impacts on data rates: (a) Split-1, 40Gbps; (b) Split-2, 32Gbps; (c) Split-3, 23Gbps; and (d) Split-4, 10Gbps.

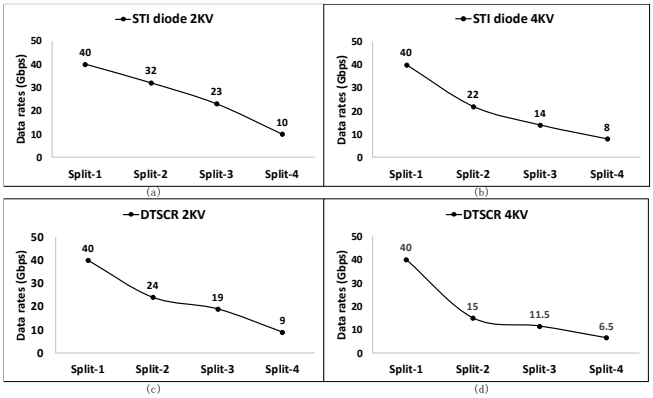


Figure 9-29 Mapping of IC data rates versus ESD protection levels for the dummy I/O circuits with 2kV/4kV STI ESD diodes (a/b) and DTCSR ESD devices (c/d) reveals significant impacts of ESD parasitic effects on ultra-high-speed ICs.

9.6.3 ESD-Protected CML Circuits and Transmitters

Figure 7-7 shows the tapered CML circuit blocks designed in this work that consist of six-stage resistively loaded differential pair with a simple current mirror and the output load of 50Ω for impedance matching. Figure 9-30 depicts a high-speed data link transmitter featuring the CML block. Different ESD protection levels were designed in this study to evaluate ESD parasitic impacts on the high-speed transmitters. The first stage ring oscillator embedded in the transmitter was designed for 14.95 GHz to provide the high frequency clock input. After the signal output from first buffer, a 7-bit peudo-random bit sequence (PRBS) generator provides a bit sequence that goes through the second buffer for waveform shaping and single-to-differential converter as the input of CML. ESD protection devices were provided for the CML output pins. Four circuit splits were designed with STI ESD diodes including No ESD, 2kV, 3kV and 4KV. Figure 9-31 illustrates the output waveform of the transmitter without ESD protection that shows correct PRBS generation. Figure 9-32 clearly shows the ESD-caused waveform distortion: as the ESD protection level increases, the slope of the rising edge decreases, which led to worse jitters as shown in Figure 9-33. The mapping for jitter degradation versus ESD protection level is depicted in Figure 9-34.

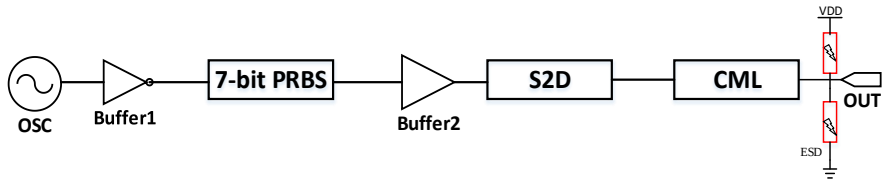


Figure 9-30. A block diagram of high-speed data link transmitter using CML.

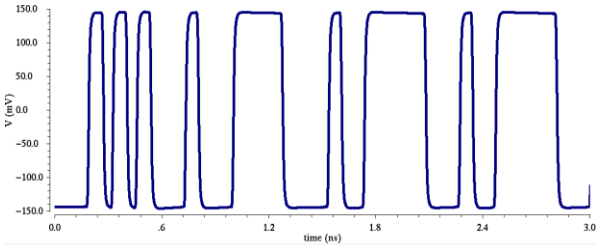


Figure 9-31 Simulated output transient waveform of a 14.95 Gbps high-speed data link transmitter without ESD protection.

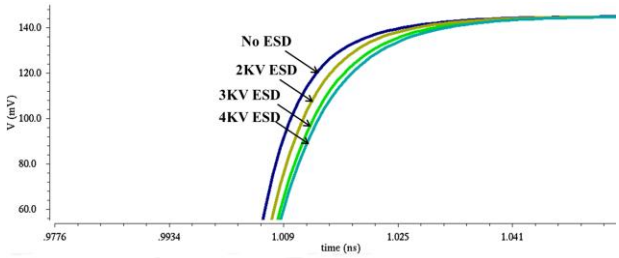


Figure 9-32 Simulation shows that rising edge of the 14.95 Gbps high-speed data link transmitter is affected by ESD protection levels.

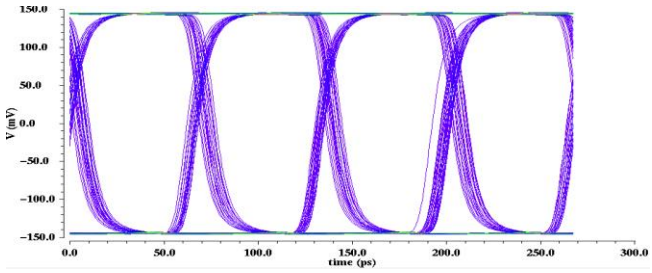


Figure 9-33 Simulation shows that eye diagram of the 14.95 Gbps high-speed data link transmitter is affected by ESD protection levels.

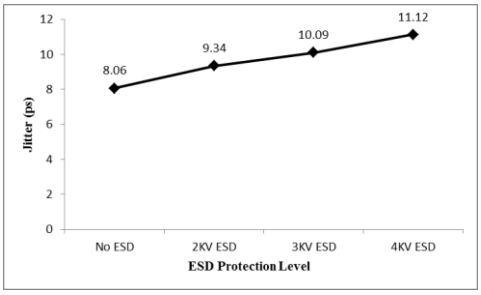


Figure 9-34 Simulation shows that jitter of the 14.95 Gbps high-speed data link transmitter is seriously affected by different ESD protection levels.

A 22Gbps data link circuit featuring a CML block with different ESD protection was also designed in 28nm CMOS to further argue the ESD impacts on ultra-high data rate ICs.

Considering the fact that any ESD protection structure will introduce parasitic C_{ESD}, no matter how well it may be optimized. In other word, to ensure ultra-high data rates, non-traditional ESD protection solution is needed. We devised a novel fuse-based *dispensable* ESD protection solution of such extremely high data rate ICs targeting for certain enterprise backbone networks where after installation, HBM ESD risk may not be a concern any more due to human accessibility. Therefore, the ESD protection structure will finish its required job after equipment installation and can be *physically* removed, therefore fully recover the ESD-induced IC performance

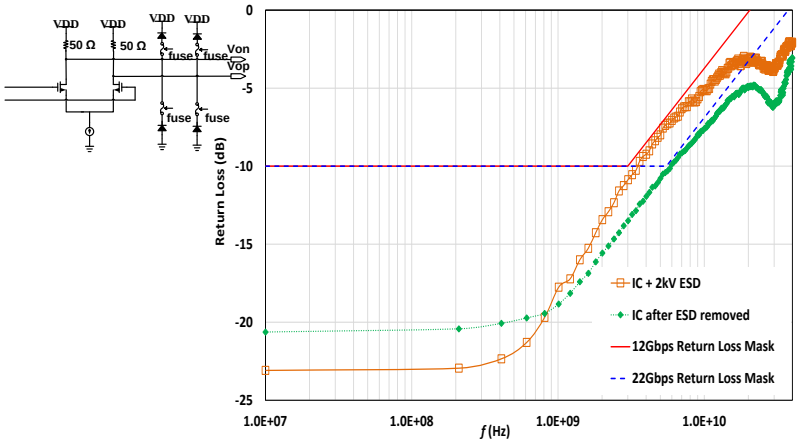


Figure 9-35 Measured output return loss for a 22Gbps circuit shows that C_{ESD} reduces the data rate to 12 Gbps (Red), which recovers back to 22Gbps (Green) after removing the dispensable ESD devices. Inset is a CML output buffer for the 22Gbps data link circuit using the new fuse-based 2kV ESD devices in 28nm CMOS.

degradation. Figure 9-35 shows 22Gbps high-speed circuit designed in 28nm CMOS and the measured return loss for different circuit splits: the data rate dropped to 12Gbps due to ESD parasitic effect and recovering back to the designed 22Gbps after removing the dispensable ESD structure.

9.6.4 ESD Co-Design Failure Analysis

Whole-chip level ESD failure analysis is a critical to debugging and optimizing ESD protection at full chip level for high-speed ICs in advanced CMOS. Figure 9-36 illustrates the complex ESD discharging current path patterns for the dummy I/O buffer circuit corresponding the required ESD stressing polarities during a practical ESD zapping test. The full-chip ESD protection uses STI diode ESD protection structures from I/O to V_{DD} (pull-up, i.e., PU, using a P+/NW diode) and GND (pull-down, i.e., PD, using an N+/PW diode) combined with a power clamp. The individual P+/NW diode, N+/PW diode and power clamp ESD structures are designed for 2kV ESD protection. However, full-chip ESD zapping test found that the IC failed at 1.5KV during an ESD zapping stress from the input to V_{DD} negatively. Emission Microscopy (EMMI) technique was used for real time ESD failure analysis where ESD zapping was conducted while the IC is biased to normal operation mode for live ESD debugging.

Figure 9-37 presents the EMMI image of ESD-protected dummy input buffer during the input-negatively-to-V_{DD} ESD stressing, where a hot spot was readily observed at P+/NW STI diode (PU) location at 1.5kV ESD zapping level. By design, ESD discharging in this ESD stressing mode should take the path-4 through the power clamp and the forward N+/PW STI diode (PD). Likely due to a larger-than-expected total ESD discharging resistance in the very long path-4, the total voltage drop in path-4 exceeds the reverse breakdown voltage of the pull-up P+/NW STI diode, which reservedly broken the PU ESD diode, resulting in early ESD failure of 1.5kV at chip level even though the standalone P+/NW STI ESD diode can handle 2kV ESD transients. This ESD failure analysis further

suggests that full-chip ESD-IC co-design and ESD failure analysis is critical to ensuring predictive ESD protection design at whole-chip level.

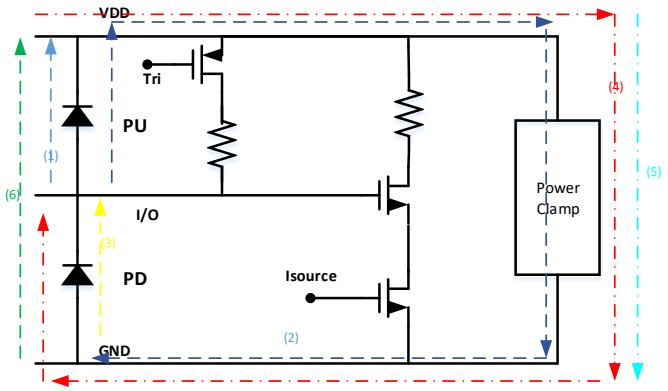


Figure 9-36 Illustration of chip-level ESD current discharge paths corresponding to different ESD stressing polarities in practical ESD zapping testing. A dummy input buffer is used for illustration. During an ESD zapping case from the input negatively to V_{DD}, the ESD transient will discharge through the path-4 consisting of the power clamp and the PD ESD device.

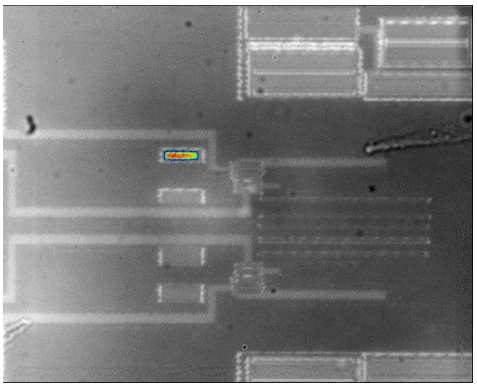


Figure 9-37 EMMI image reveals that ESD damage during the input-negatively-to- V_{DD} ESD zapping mode occurs at the P+/NW STI ESD diode (PU).

9.7 Designed ESD protection scheme

One of the most commonly used ESD protection strategies is to use two diodes on the pin, one to supply bus and other to ground bus. Figure 9-38 shows the current path in the chip for the possible discharges between the pin and its supply and ground buses. The power clamps will be discussed later in more detail, but essentially they are turn off during normal operation and turn on during an ESD even to provide a very low resistance

discharge path, because the diode appears as parasitic capacitance on the input/output node, the designer may have to balance ESD protection against circuit performance. This scheme is effective for the HBM protection, but considering CDM protection, it achieved by adding a voltage divider between the I/O pin and the MOS gates. This is implemented by a series resistor and another set of ESD diodes. The resistor should be range from 50 to 250 ohm. In normal operation, the resistor is in series with the input impedance of the circuit and does not significantly affect the speed of the gate. Consider the scenario that the module is charged to a negative voltage and discharged through the I/O pin. Again, a large voltage develops between the pin and the power supply and ground buses, but the resistor and the forward-biased "up" diode divide this voltage based on the proportion of the resistor value and the diode on-resistance. The second set of double diodes may be much smaller than first one since they don't carry as much current. For the digital IO like SDATA, SCLK, the ESD scheme is good to protect the IO pin.

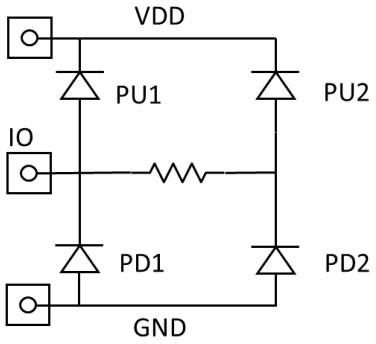


Figure 9-38 ESD protection scheme for the digital IO pin

A RC power clamp is normally connected between the power supply node and ground node, however, due to the unpredictable power start up time, the dual-direction diode is

more reliable to protect, in this design, consider the 3.4V power supply, 8 forward series diodes and 2 reverse series diodes are used as shown in Figure 9-39.

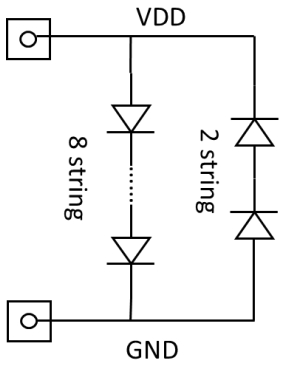


Figure 9-39 ESD protection scheme for the power pin

For the RF port, the input power is less than 0 dBm and corresponding voltage amplitude is less than 1V, considering the input matching network band-pass capability, for the ESD current, it performs like an open network, so 2 series diodes for both directions are utilized as shown in Figure 9-40.

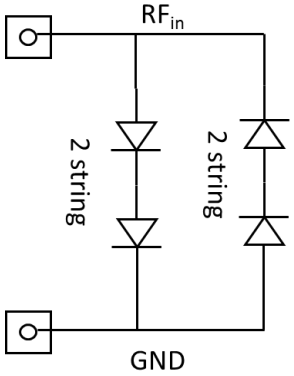


Figure 9-40 ESD protection scheme for the RF pin

9.8 Antenna ESD design

ESD protection requirement is quite harsh in the antenna port as high as 8KV HBM, with this limit, the ESD current is very high and cause a high voltage over the antenna node.

Then the normal ESD device with low trigger voltage probably is not suitable to use any more due to the large RF swing in high power working condition. Therefore, an LC type high pass filter may be a good option. The HBM waveform power spectrum analysis is shown in Figure 9-41, we can see that the main spectrum domain is within 2 MHz, it low enough to be suppressed by high pass filter. A 30V-HV capacitor and a on laminate inductor are used to implement the ESD protection as shown in Figure 9-42, the power amplifier off-state is equivalent to a 500 ohm resistor. The transient simulation result is illustrated in Figure 9-43 and Figure 9-44, almost all the HBM transient current goes through the ESD inductor to ground, and the voltage over the ESD capacitor is 11V or so which is below its dielectric breakdown voltage.

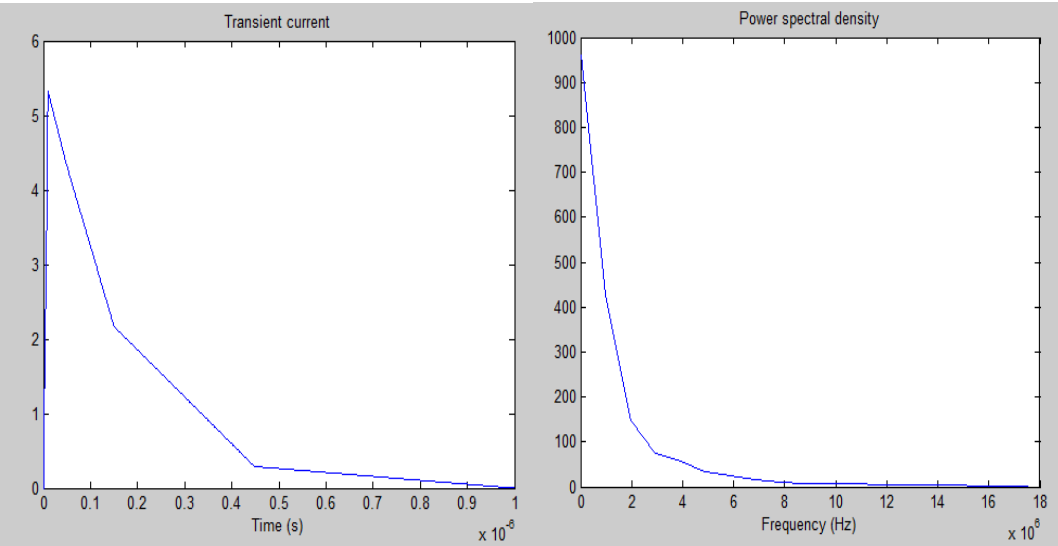


Figure 9-41 HBM transient waveform and power spectrum density

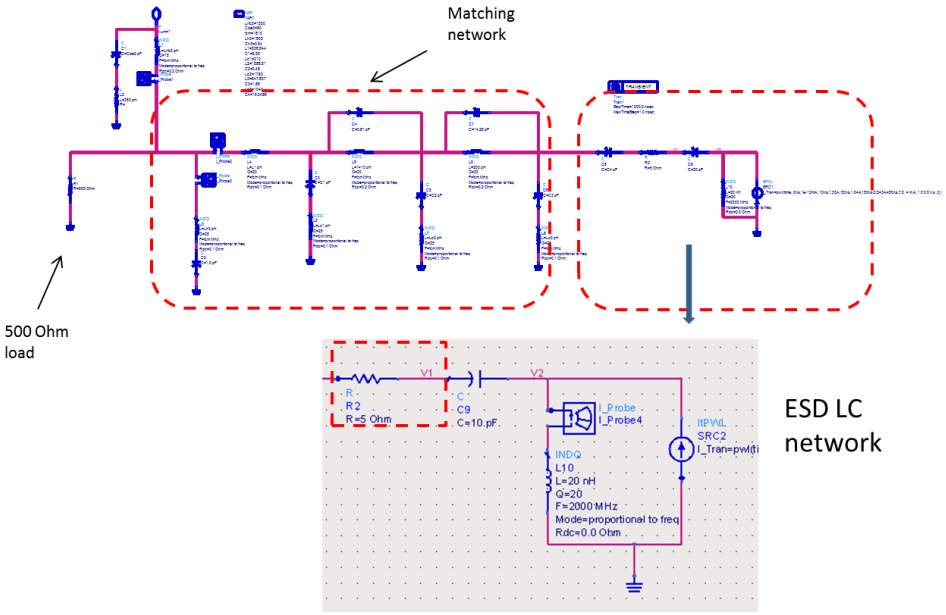


Figure 9-42 Schematic of Antenna ESD protection LC network

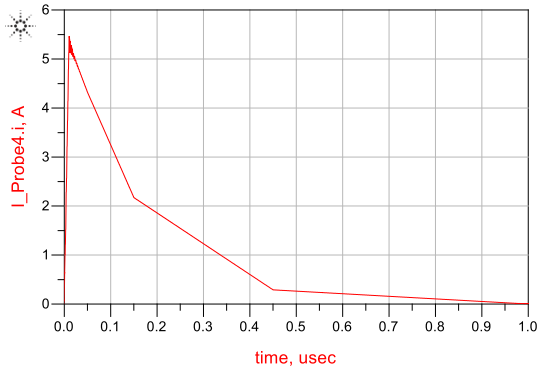


Figure 9-43 HBM transient waveform over the ESD inductor

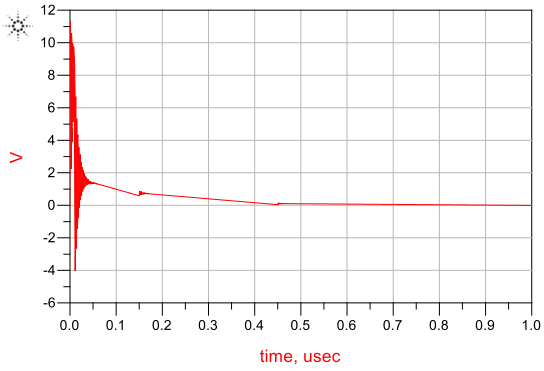


Figure 9-44 HBM transient waveform over the ESD capacitor

Chapter 10 Crosstalk Suppression

Crosstalk or noise coupling through the conductive silicon substrates has been a major technical challenge for RF, analog and mixed-signal ICs in CMOS. While CMOS scaling has generally been advantageous to IC integration and performance, noise crosstalk has been a technical barrier to implementation of systems-on-a-chip, which, nevertheless is the trend for advanced ICs, such as chipsets for the 5th-generation mobile communications. SOI technologies have many advantages over bulk CMOS processes, including less parasitic effects, smaller MOSFET size without using body contacts, and no latch-up effect. SOI also features reduced substrate noise coupling effect due to using shallow trench isolation, buried oxide layer and high-resistive Si substrate, making it a preferred technology for high-performance RF and mixed-signal ICs [67]. Substantial efforts have been devoted to Si substrate noise isolation in CMOS, leading to many design techniques to suppress global crosstalk, e.g., guard ring, oxide trench, decoupling by-pass capacitor, shielding ground [68]-[72]. In addition, trap-rich substrates are used to reduce crosstalk induced by the under-BOX parasitic surface conduction (PSC) effect [73][74]. Various Faraday cage structures were also reported to suppress Si substrate crosstalk 0-[77]. For example, 0 uses metal-filled trench by an exotic MEMS process including creating a deep local cavity in the wafer backside that is impractical for foundry CMOS. [76] reports a poly-Si filled trench in SOI that requires bonding a Si handle wafer. [77][78] depicts a dotted Cu-filled trench made of through-Si vias that also requires wafer backside etching to form a local cavity, impractical to foundry CMOS. While various substrate isolation techniques have substantially reduced the noise coupling effect due to in-Si global crosstalk

through the Si substrates, the above-Si global crosstalk through the complex BEOL stacks is becoming a noise concern for ICs in SOI, particularly for FD-SOI featuring very thin active Si layer, typically less than 150nm thin, on a BOX layer.

10.1 Crosstalk Isolation using Metal Mall

From classic electromagnetic theory, the simplest shielding configuration is that as shown in Figure 10-1, where a uniform plane wave is impinging with an angle Θ^{inc} on a single planar shield of infinite extension in the transverse y and z directions with a finite thickness d in the x direction.

Assume a plane wave propagating in a medium that is linear, homogeneous, stationary, isotropic, and assume that each material occupying the region (①, ②, ③) is characterized by it relative permittivity and permeability, in the SOI wall shielding analysis, media 1 and 3 are the same, thus, the electric and magnetic shielding effectiveness SE_E and SH_H are the same. The shielding effectiveness can be expressed as equation 10.1.

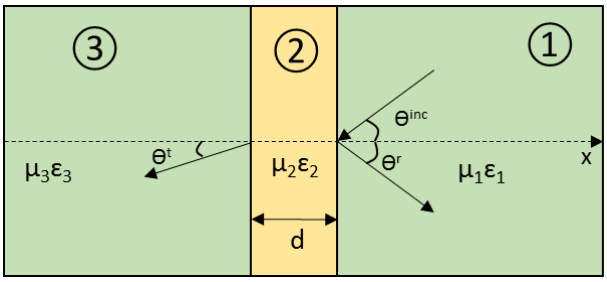


Figure 10-1 Cross section of uniform plane wave impinging on a shield of finite thickness d, an incident wave with a specific angle will generate the reflection wave and refraction wave at the medium boundary.

$$SE_E = SE_H = SE = 20\log\frac{E_3^0}{E_3^S} \qquad 10.1$$

Where E_3 indicates the electric field in the region 3, while the superscripts 0 and S indicate the absence and the presence of the shield, respectively. According the transmission line theory, the SE is readily obtained by the following equation.

$$
\begin{aligned}
SE &= -20\lg\left|\frac{4Z_0Z_S}{(Z_0+Z_S)^2}e^{-jk_{xs}d}\frac{(Z_0+Z_S)^2}{(Z_0+Z_S)^2-(Z_0-Z_S)^2e^{-2jk_{xs}d}}\right| = R+A+M \\
R &= 20\lg\left|\frac{(Z_0+Z_S)^2}{4Z_0Z_S}\right| = 20\lg\left|\frac{(\xi+1)^2}{4\xi}\right| \\
A &= 20\lg\left|e^{jk_{xs}d}\right| \\
M &= 20\lg\left|\frac{(Z_0+Z_S)^2-(Z_0-Z_S)^2e^{-2jk_{xs}d}}{(Z_0+Z_S)^2}\right| = 20\lg\left|1-\frac{(\xi-1)^2}{(\xi+1)^2}e^{-j2k_{xs}d}\right| \\
\xi &= Z_0/Z_S
\end{aligned}
\qquad 10.2
$$

The first item depends only on the free space impedance Z_0 and the impedance of the shield medium Z_s, and it accounts for the first field reflection at the two shield interfaces that is due to the mismatch between the two impedance at both the interfaces. R is called the reflection-loss term, and it is always positive or null. The second item, A, is a function of the shield characteristic only, and it accounts for the attenuation that a plane wave undergoes in travelling through an electrical depth equal to $k_{xs}d/k_0$ in the shield material, it is called absorption-loss term, and it is always positive. The last term, M, is associated with the wave that undergoes multiple reflections and consequent attenuation before passing through the shield, is called the multiple reflection loss term, and it may be positive, null or negative. M is often negligible with respect to the other terms, especially in the high frequency range. Then, we can say that with a lossy metal wall, most energy of a plane wave is blocked out by reflection loss and absorption loss, the metal wall with high conductivity metal wall is very promising. Consequently, silver is used to form a vertical

shielding wall, as deep as touching the substrate, to stop the crosstalk from transmitting to inner circuit.

10.2 Above-Si through BEOL Metal Wall

Figure 10-2 is conceptual illustration of the new above-Si through-BEOL metal wall structure based on the FD-SOI CMOS process featuring a very thin active silicon layer on BOX. The circuit block is isolated by a closed-loop metal-filled wall from the rest of the Si die. The continuous floating metal-fill wall resides inside the BEOL stacks is formed by selectively etching through the entire BEOL layers. The etching is carefully controlled to go through the thin active Si layer and the BOX layer in order to eliminate crosstalk within the conductive active Si layer. According to the EM theory, an incident EM wave to the metal wall will break into three parts: a reflection wave, an attenuation loss due to the absorption by the metal wall, and a through-wave passing through the metal wall. The crosstalk isolation efficiency is characterized by the ratio of the through-wave without the metal wall to that with the metal wall. Figure 10-3 shows a top view of the test pattern for the new through-BEOL metal wall structure, consisting of ground-signal-ground (GSG) pads, a CS amplifier test circuit located inside the metal wall and a noise input metal bar residing outside of the metal wall. The new through-BEOL metal wall structure aims to reduce the crosstalk through the above-Si coupling effect, which becomes dominant in advanced SOI technologies because the traditional through-Si-substrate noise coupling has been minimized by features such as HR substrate, STI and ultra-thin active Si layer. To ensure noise shielding effect, the width of the metal wall should be much thicker than the skin depth. This near closed-loop metal wall is different from the classic Faraday cage. In

fact, a true Faraday cage of a completely enclosed metal cage containing a top and a bottom metal planes is impossible for ICs in CMOS 0.

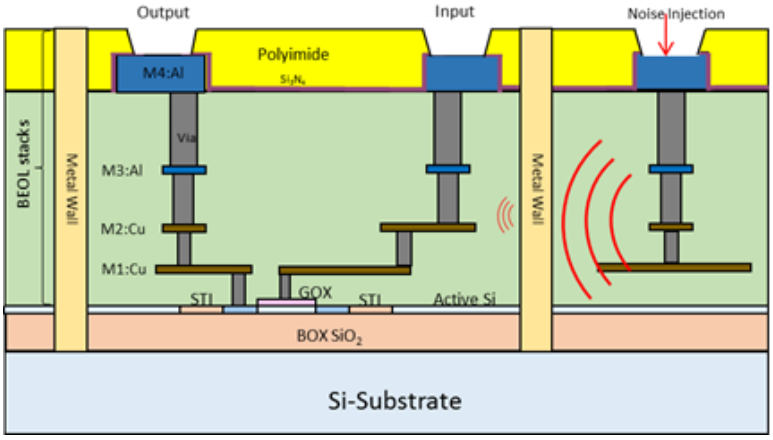


Figure 10-2 Cross section and equivalent lumped parasitic RC models in post-fab SOI CMOS. Metal wall is built to hold noise back. Powers attributed to conducting noise metal are divided into five different paths leaking to protected core where circuit metal is physical connected to active device.

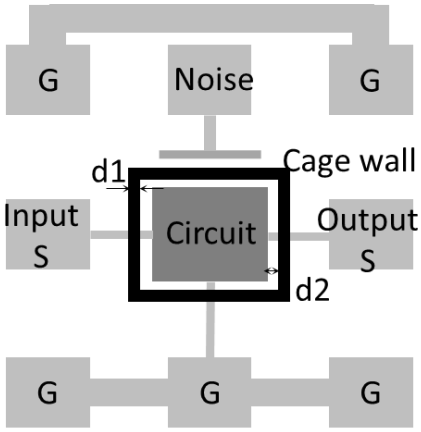


Figure 10-3 Top view of coplanar GSG testing fixture for crosstalk measurement. Inner circuit is encompassed by a metal wall with thickness d1 and distance d2.

10.3 Fabrication Process

Meatal wall is manufactured by post-fabrication process onto chips processed by foundries as shown in Figure 10-4 where a trench marker designed by top metal is already done by foundry. Focused Ion Beam (FIB), able to inject high energy ions into target materials, is used to define the surrounding metal shielding of the transistor. In the FIB

process, a mill current of 30kV/18nA is applied to bombard the targeting regions which is made of silicon and oxides, making sure the high selectivity of the aspect ratios for the wall as well as leaving the metal wall opening to routing metal as shown in Figure 10-5 (a), a sophisticated calculation regarding depth of 16um as shown in Figure 10-5 (b) guarantees that the trench will touch the substrate, at the same time, not compromise the wafer mechanic reliability. Next, silver nano-powders (99.99%, 80-100 nm) is filled manually into the surrounding trenches to achieve metal wall as shown in Figure 10-5. Specifically, under the optical microscope, first, four strips of brown tapes are used to cover all the chip areas excludes the trenches, in order to seal the chip and expose the trenches only for the filling; second, apply a bunch of silver powders by tweezers onto the exposed trenches, note that, silver nanoparticles can be crowded and accumulated by the electrostatic force; third, DC tip (tungsten) is needed to scrub the silver powders into the trenches, repeat this for several times and sonication may be used to let the powders reside into trenches more smoothly; finally, remove the brown tapes and clean the chip surfaces may contaminated by silver powders by sticking brown tapes. (And remove contamination powders adsorbed onto other chip surfaces by other brown tapes). Figure 10-5 (c) shows the image of the etched trench ring.

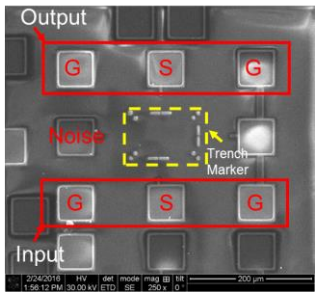
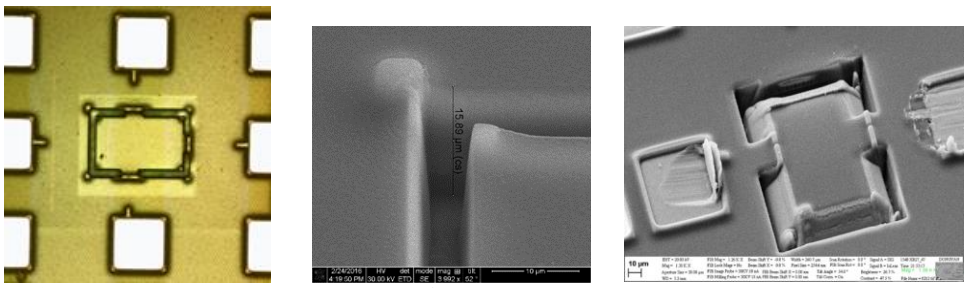


Figure 10-4 Scanning Electron Microscope (SEM) image top view of testing structure, the on-die top metal which is underneath the polyimide with the yellow line works as the post-fab alignment marker.



(a) (b) (c)

Figure 10-5 a) A top-view image of the trench ring after FIB etching, b) a zoom-in view of the trench etched (Trench dimensions: width ~ 20um and depth ~ 16um; the trench inner edge is ~10um from the inner circuit). c) SEM image of trenched die; the full enclosure is set up but the area for the circuit metal routing

10.4 Simulation and Measurement

The test structure, similar to [79], is implemented in a foundry 180nm FD-SOI technology featuring a 1kΩ-cm HR substrate and 145nm thin active Si layer on a 1Kohm-cm BOX layer to reduce the substrate crosstalk. Figure 10-6 shows the test circuit residing inside the metal wall, which is made of a 2.5V NMOSFET transistor and R1 for 50Ω impedance matching to testers.

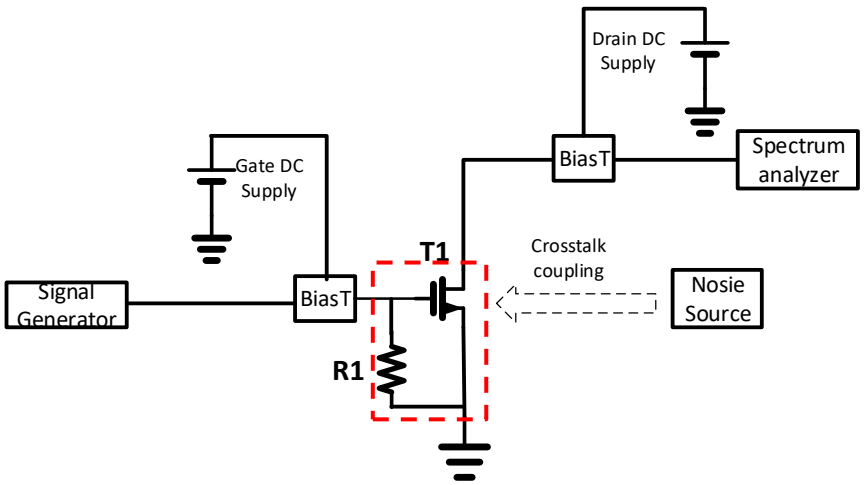
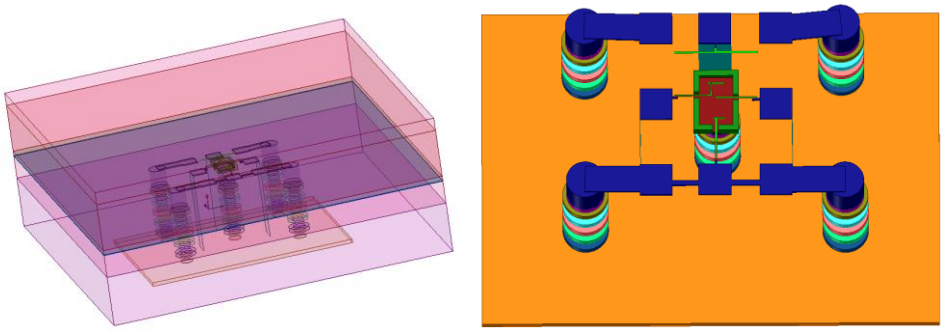


Figure 10-6 A schematic for the testing amplifier circuit where the dashed block indicating the metal wall for crosstalk isolation

Crosstalk simulation results calculated by a two-dimensional (2D) MEDICI device simulator has been reported previously 0, it can include the effects of a depletion layer

tracing a real impurity profile and simulate the device physics very well, but the drawback is that electromagnetic effect, our major concern in this metal wall concept, is unable to be solved. ADS Momentum is used as EM simulation tool obtaining the co-simulation advantage with active components, its useful for the planar EM structure and simple to set up, but not so accurate for the real 3D model. HFSS is based on Finite Element Method



(a) (b)

Figure 10-7 a) HFSS modeling of practical flip chip package, all the material layer attributes keep the real one b) Inside-view of the testing circuit, and the modeling dimension is same as the real circuit, the simulation will be performed w/ and w/o metal wall.

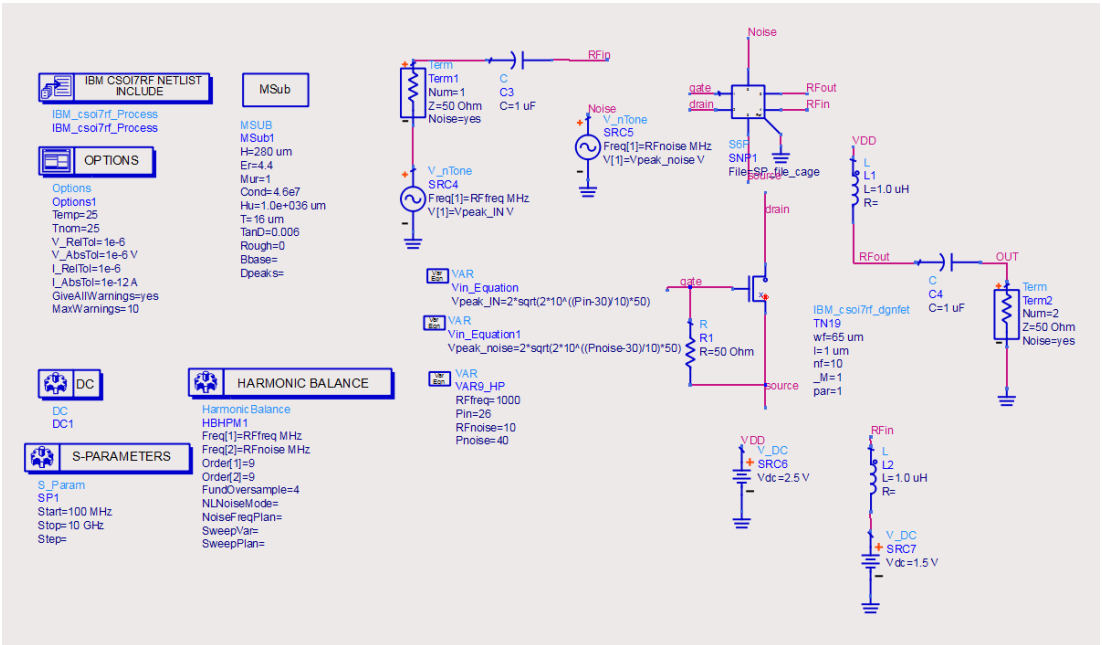


Figure 10-8 HFSS and ADS co-simulation test bench

which is more reliable for the 3D modeling, the simulation result is widely accepted to be close to experimental results with more insight into the structure, thus, an advanced HFSS/ADS co-simulation method is put forward to predict crosstalk impact. First step, assume a real Flip-chip package using 6 metal-layer laminate is simulated as shown in Figure 10-7, all the used layers with key factors such as dielectric and resistive parameters are pre-defined, only passive components are left to build the EM structure, GSG ground is tied up together through via connected to the bottom laminate metal layer. With a deliberate port setup, HFSS will provide a N-port S parameter file which can be used in the ADS co-simulation as shown in Figure 10-8. The passive EM result will combine with active MOS model in the ADS schematic to get full insight of package level. Here the harmonic balance simulator is a best option to look into the nonlinear phenomenon induced by crosstalk. In this test bench, a 1GHz signal as input and 10 MHz signal with 10 dBm

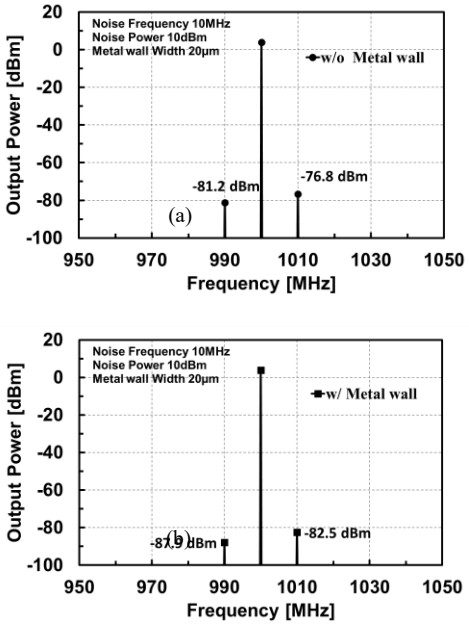


Figure 10-9 Co-simulation of the testing amplifier circuits without the metal wall (a) and with the metal wall (b) clearly show the substantial noise reduction effect due to the through-BEOL metal wall crosstalk isolation.

power as the noise are applied, after a full EM co-simulation, the 3rd order Intermodulation (IM3) result is shown as Figure 10-9 . Table 10-1 summarizes the IM3 improvement by introducing the metal wall.

Table 10-1 Summary of simulation applied by 1GHz input and 10MHz noise

IM3	Without wall	With wall	Improvement
Left	-81.19 dBm	-87.91 dBm	6.72 dB
Right	-76.76 dBm	-82.56 dBm	5.8 dB

The simulation result is further verified by the measurement. Figure 10-10 illustrates the die photo of testing fixture under microscope, and GSG probes and DC probes are stressed on the pads to feed the signal. The test bench follows the same methodology described above and the measured result in Figure 10-11 demonstrates a spectrum sweep from 950 MHz to 1050 MHz, two minor peaks can be captured as the IM3 component, it clearly shows that the linearity is greatly improved by crosstalk suppression with metal wall. Then the characterization of IM3 suppression with a group of different noise frequency was summarized in Table 10-2, we can see that, as the noise frequency increases, the improvement gets less. This issue is able to be analyzed by the equivalent lumped model,

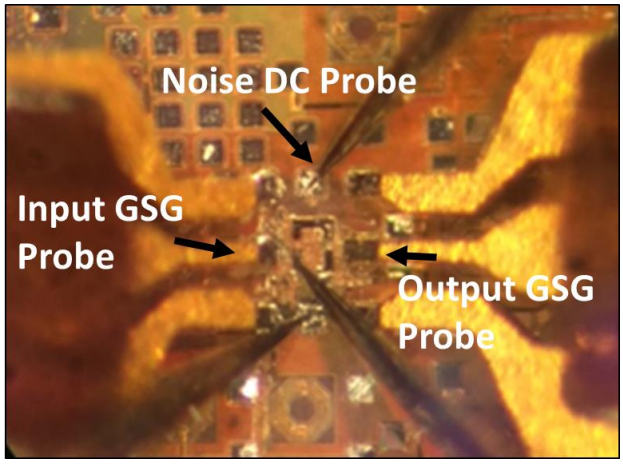


Figure 10-10 Die photo of testing structure, a metal wall can be observed obviously

though the higher frequency will undergo a larger absorption loss inside the wall due to longer electrical length compared to skin depth, but the lower impedance for high frequency signal through substrate and open slot provides a local "free-way" to unexpected crosstalk, consequently, the metal wall cannot perform as effectively as it in low frequency.

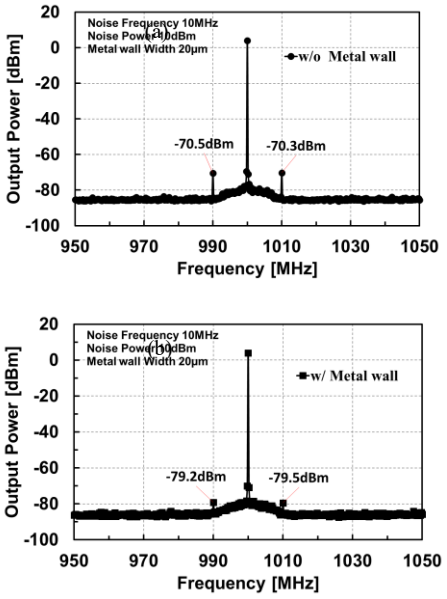


Figure 10-11 Measured output signals for the testing amplifier circuits (a) without and (b) with the new metal wall structure shows substantial crosstalk reduction due to the through-BEOL metal wall noise isolation.

Table 10-2 Intermodulation Results of circuit w/ and w/o Metal wall

Output Power (3.9 dBm)			Crosstalk Frequency		
			10 MHz	100 MHz	398 MHz
IM3 (dBm)	w/o wall	Left	-70.5	-65	-71.6
		Right	-70.3	-64	-73.6
	w/ wall	Left	-79.2	-71.7	-75
		Right	-79.5	-68	-75.4
IM3 Improvement (dB)		Left	8.7	6.7	3.4
		Right	9.2	4	1.8

Chapter 11 Program Automated Test Equipment

11.1 ATE Introduction

Computer controlled testing has helped to drive manufacturing productivity by increasing efficiency and improving quality. Automated test equipment (ATE) plays a crucial role as it enables more vigorous testing at faster rates and in a more controlled manner than was previously possible using manual procedures. ATE can involve a single measurement made continuously at very high rates or multiple measurements made by a host of different instruments. Measurements made on a DUT are typically calculated, stored and analyzed in an automated fashion by some form of computer. The process helps to remove human error and allows fault diagnosis to be performed in reproducible manner even when sophisticated measurements are involved. ATE is considered cost and time efficient testing. In this dissertation, Equipment are programmed by Visual Basic with a Graphic User Interface (GUI) and convenient to use. Figure 11-1 shows the equipment list for the FEM testing.

Figure 11-1 Equipment list for FEM testing

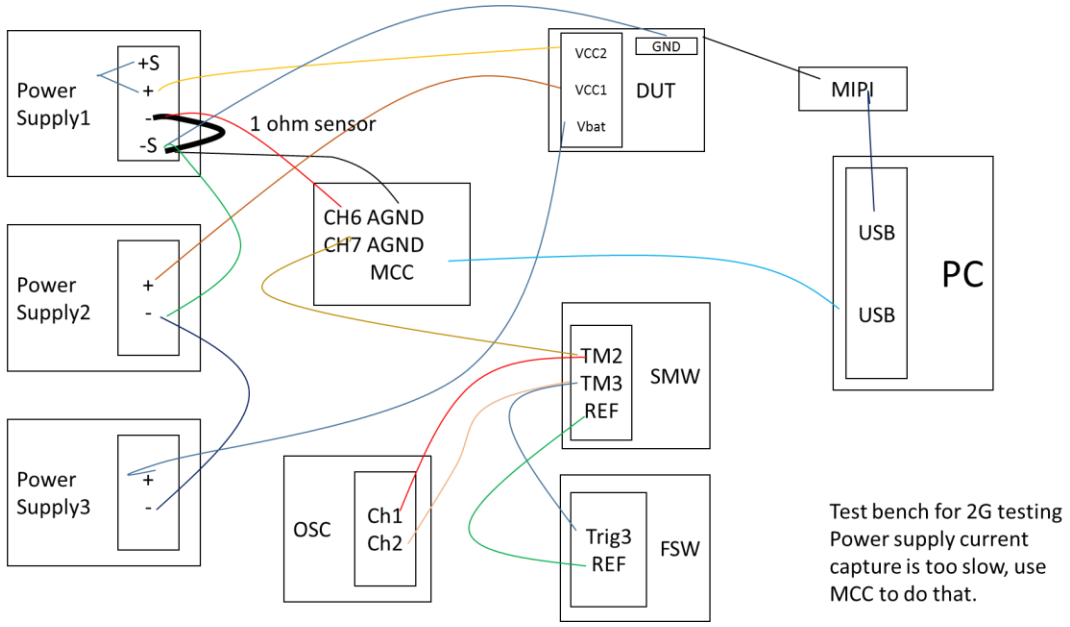


Figure 11-2 Wiring for the ATE environment

Figure 11-2 shows the equipment list and wire interconnecting, three power supplies provides voltage to the DUT separately, and normally the current can be measured by the power supply itself for the most modulation scheme, but due to slow response time, it is unable to catch the current instantly for the quick changed GSM modulation in 2G PA. A high speed AD module named as MCC is utilized to acquire accurate current. The 1 ohm resistor works as a sensor for MCC AD input. The oscilloscope is to monitor whether the trigger is sent correctly from the SMW. The reference signal of SMW should the same as FSW, all these equipment features an Ethernet interface connected to PC but MCC and MIPI Master board using USB interface.

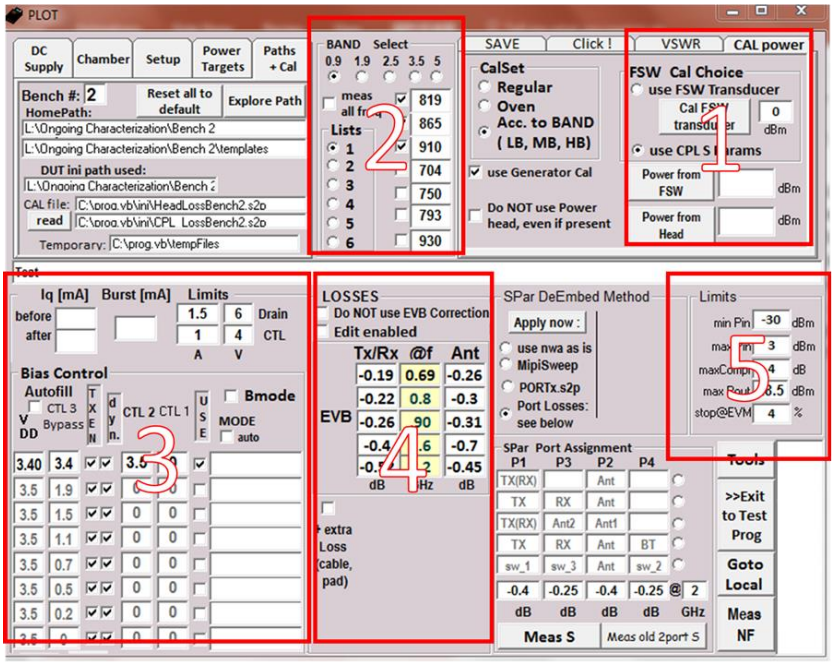
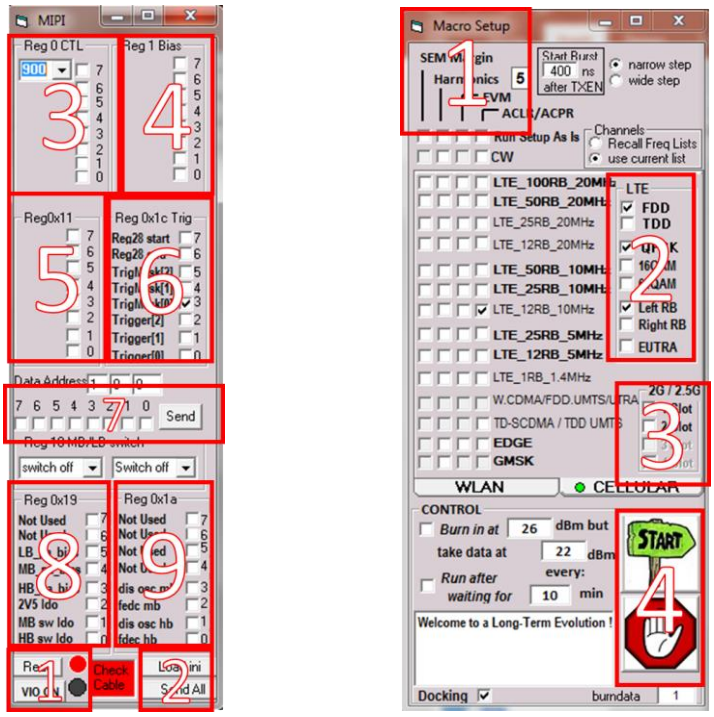


Figure 11-3 Main window of ATE for setting the testing condition

As shown in Figure 11-3, several settings must be confirmed before the testing .The calibration is first step to execute, then the specific band will be selected. The third step is to adjust the working voltage with a reasonable value. The performance of DUT itself is our concern, but inevitably, the testing fixture will induce the measurement error, in the fourth step, the evaluation board (EVB) loss is de-embedded. Regarding to PA testing, the minimum and maximum input power is controlled in step 5. Figure 11-4 shows the control panel of MIPI, The register value can be written to control PA/SW with different functionality. The aforementioned Table 8-1 shows the logic mapping for different control function. Another control functionality is selecting the testing mode, generating and analyzing LTE signals. The testing should cover all the LTE bandwidth from 1.4 MHz to

20 MHz, and the entire modulation scheme including the FDD/TDD BPSK, QPSK, 16 QAM and 64 QAM.



(a) (b)

Figure 11-4 (a) MIPI control panel (b) Waveform and testing item selection

In terms of different testing Item, the test bench is set up differently, for the basic ACLR and harmonic measurement, the test bench is shown as Figure 11-5. The signal generator works as an input followed by an isolator which can protect the signal source for reflection damage in case the DUT has a large reflection coefficient or oscillation. For the PA testing, the signal to spectrum analyzer should working in a suitable dynamic range, then a 10 dB attenuator in addition to a 10dB coupler is added. Power meter specialized in measuring power can provide a more accurate result whereas the spectrum analyzer can show the signal details in the screen. So two measurement paths either to Power meter or to spectrum analyzer are used for double check. Another concern is the stability and ruggedness, the

test bench is shown as Figure 11-6, the difference from the Figure 11-5 is that the DUT output is not connected with a 10 dB attenuator, but a load tuner instead which can change the load impedance. Then with different VSWR, the performance of PA should not be degraded. Last but not least, in band noise is another concern and the test bench is shown as Figure 11-7 , the input of in band noise signal into the PA is suppressed by a bandpass filter to guarantee a noise sanity check, then the output signal will go through a duplexer to monitor the Tx and Rx, respectively, the Rx branch will show the noise result in spectrum analyzer.

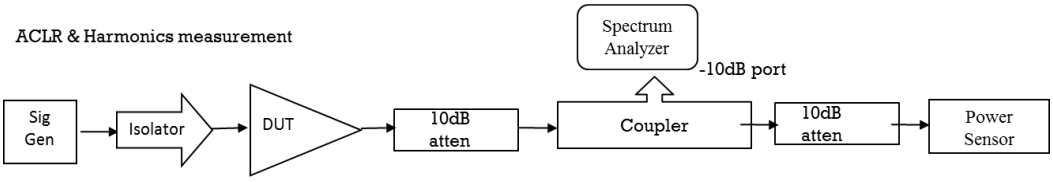


Figure 11-5 Test bench of ACLR & Harmonics measurement

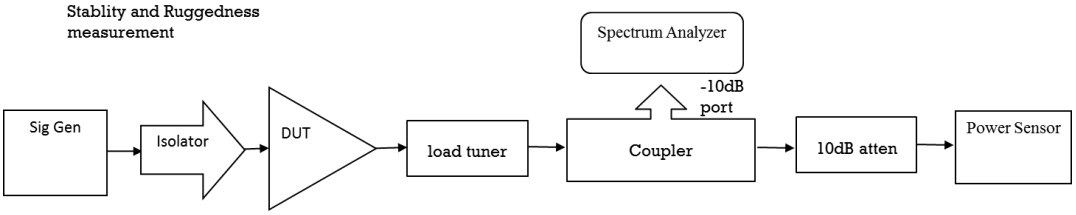


Figure 11-6 Test bench of Stability and Ruggedness measurement

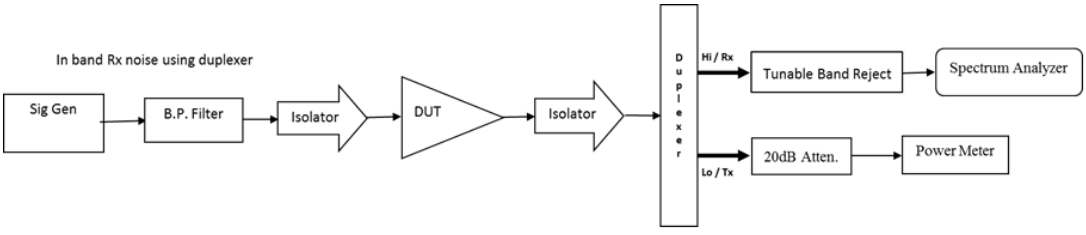
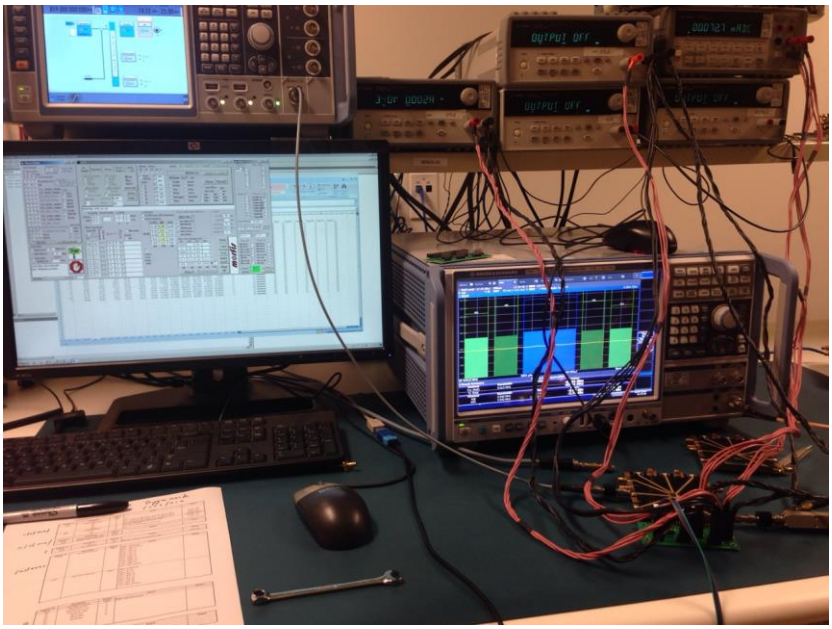
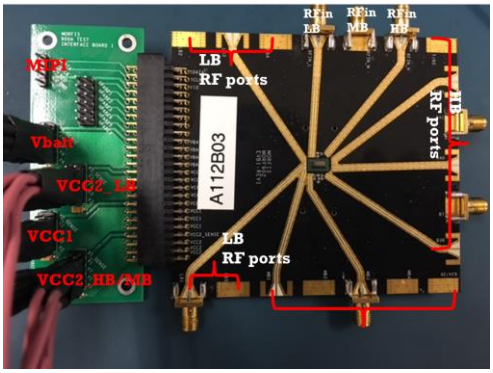


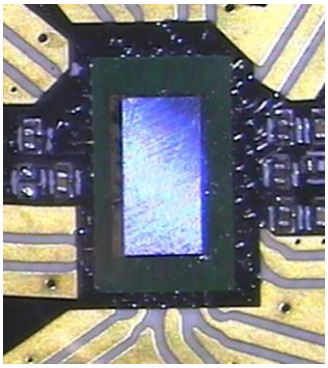
Figure 11-7 Test bench of in band noise measurement

The completely testing bench is demonstrated in Figure 11-8, the die is with flip-chip package and made on evaluation board connected with MIPI master for control.



(a)





(b) (c)

Figure 11-8 (a) Whole test bench setup (b) DUT made on evaluation board connected with MIPI Master (c) View Flip-Chip Package

11.2 Measurement result

Measurement result is presented in this section.

11.2.1 Small signal

The small signal S parameter measurement is shown in Figure 11-9 and Figure 11-10 where the Blue curve shows the simulation result and the Pink one shows the measurement result. As we can see, the curves of simulation one and the measurement one have the same trend and poles. The result is almost dead-on, which means the model from the PDK and ADS-HFSS co-simulation method is good and accurate for small signal design. All the result is within the spec limits and the testing is repeatable and shows good consistency.

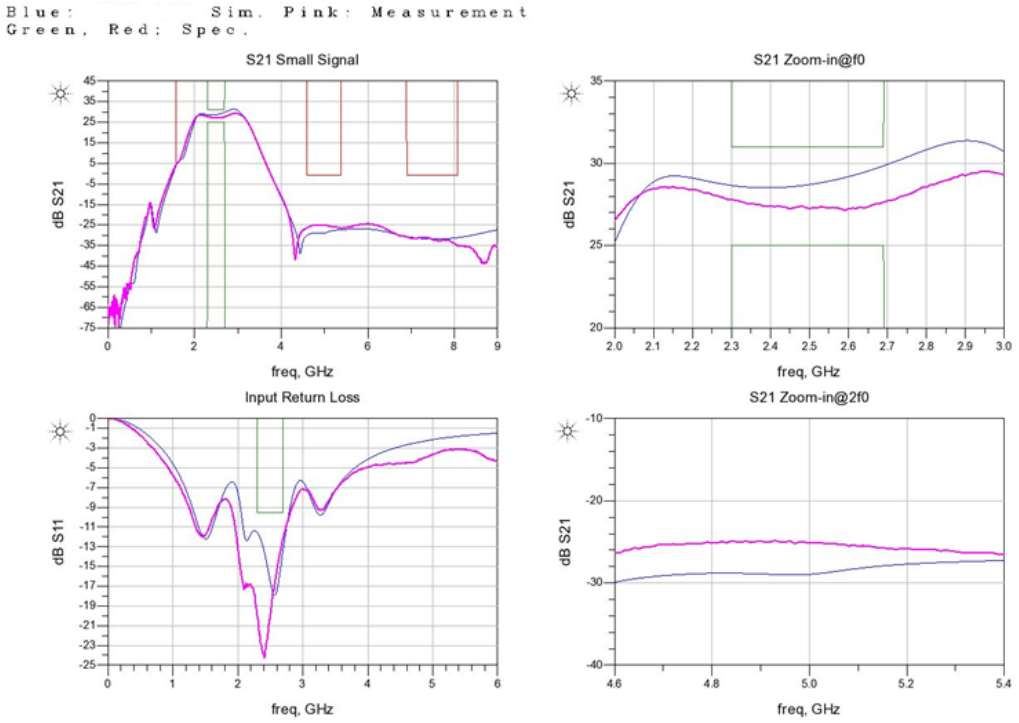


Figure 11-9 Measurement result of S21 and input return loss

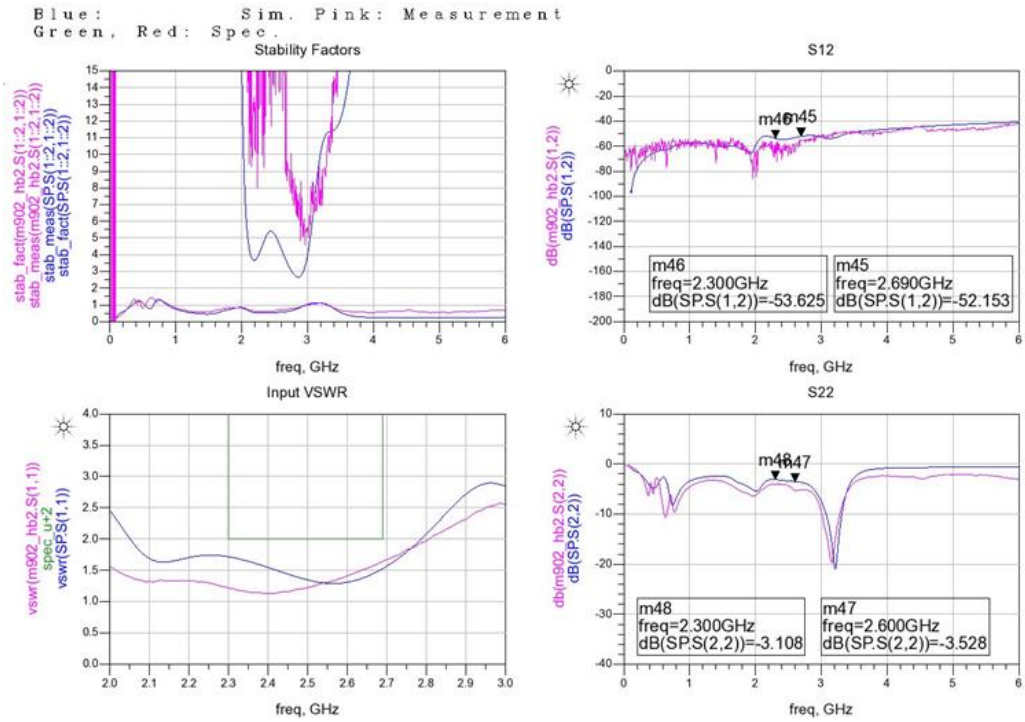


Figure 11-10 Measurement of stability factor, input VSWR and S parameter

11.2.2 Large signal

The waveform uses Band7 LTE 10 MHz 12 RB in the following measurement.

11.2.2.1 ACLR

ACLR is aforementioned in Chapter 5. In this specific design, two ACLR cases are defined.

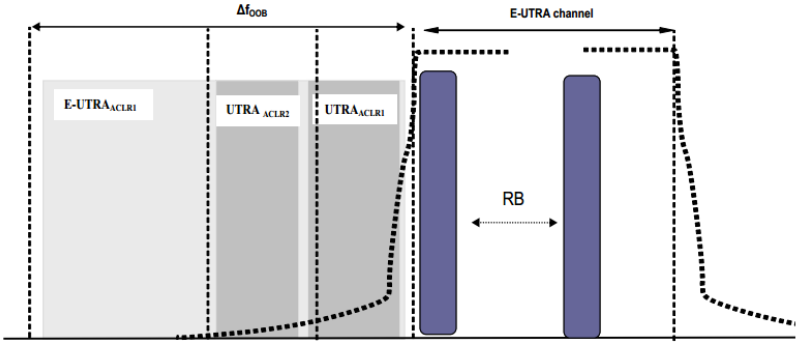


Figure 11-11 3GPP TR 36.803 v1.0.0 Adjacent Channel leakage requirements

E-UTRA (LTE) ACLR1 with rectangular measurement filter; UTRA (WCDMA) ACLR1 and ACLR 2 with 3.84 MHz RRC measurement filter with roll-off factor 0.22 as shown in Figure 11-11. The measurement results are shown from Figure 11-12 to Figure 11-14, with different test case UTRA ACLR1/ACLR2 and the EUTRA ACLR1 in room temperature.

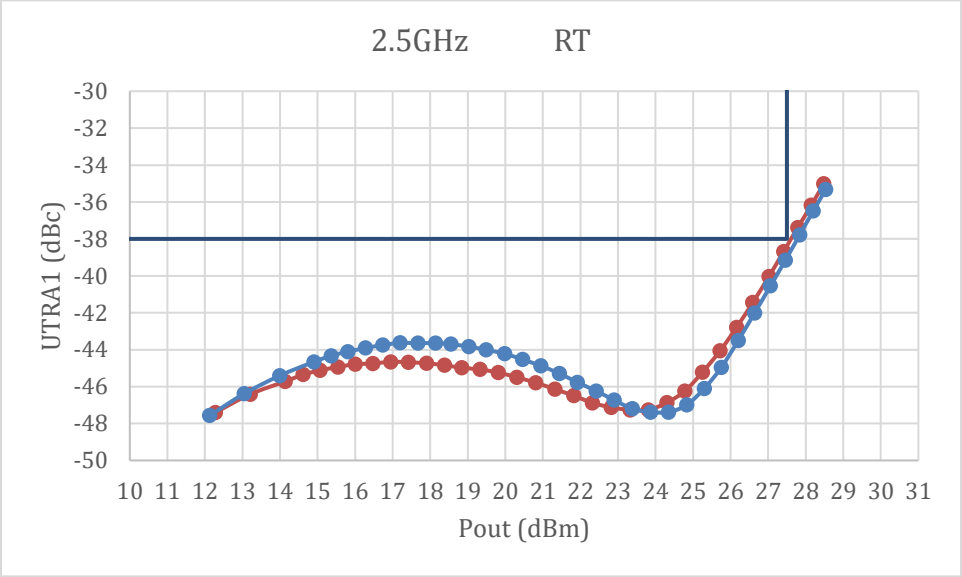


Figure 11-12 Measurement of UTRA ACLR1

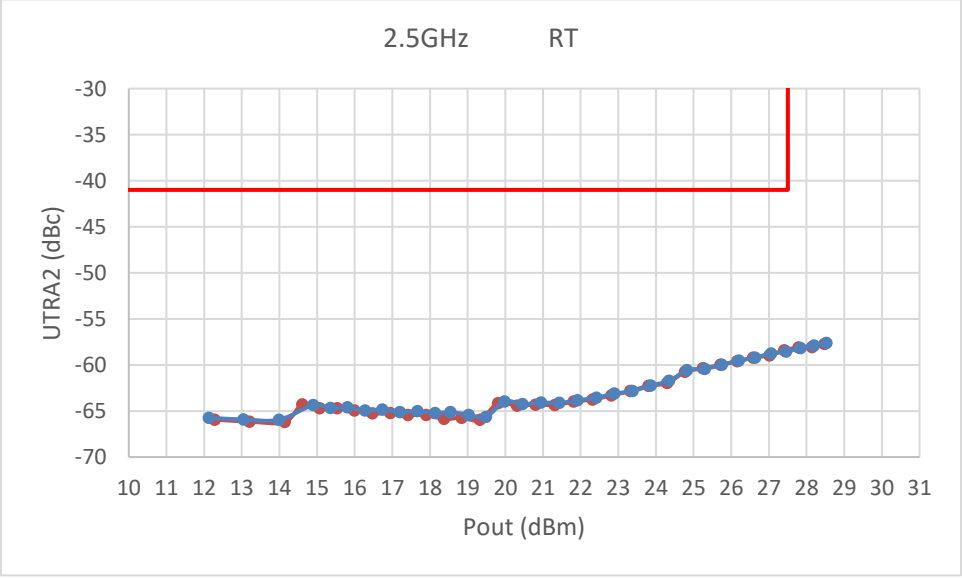


Figure 11-13 Measurement of UTRA ACLR2

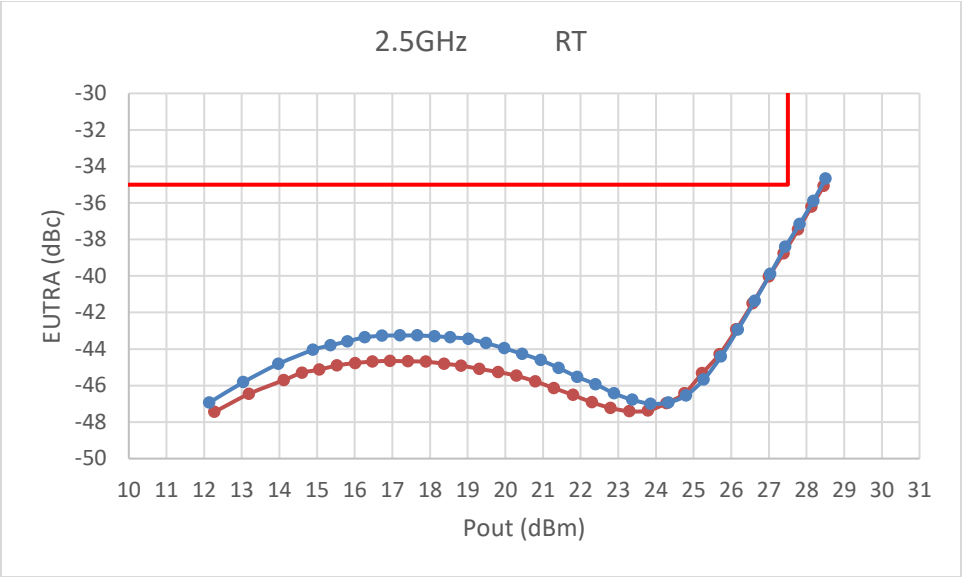


Figure 11-14 Measurement of EUTRA ACLR1 ACLR

11.2.2.2 EVM

The EVM measurement result is shown in Figure 11-15 and it is good within 5% limit.

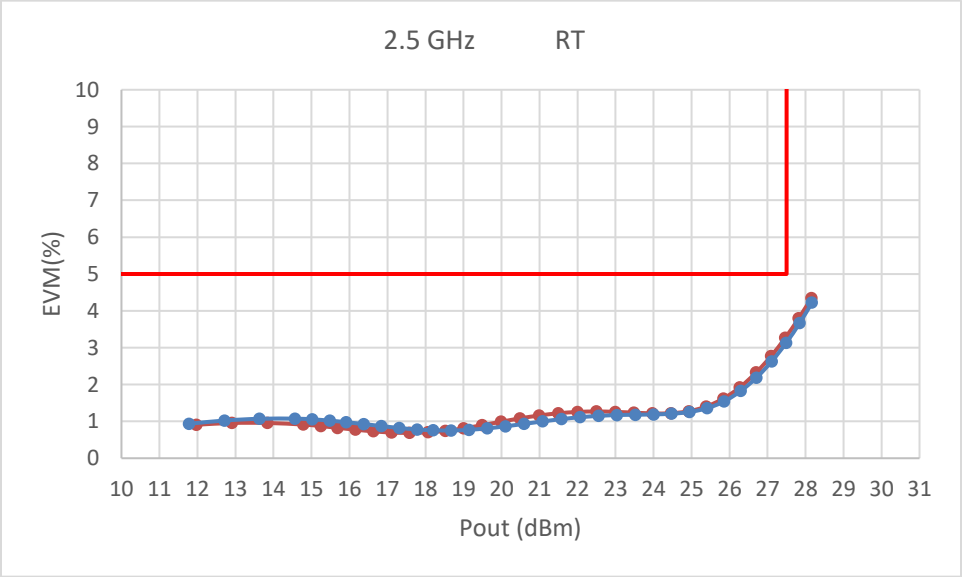


Figure 11-15 Measurement of EVM over output power

11.2.2.3 Gain

The Gain measurement result is depicted in Figure 11-16.

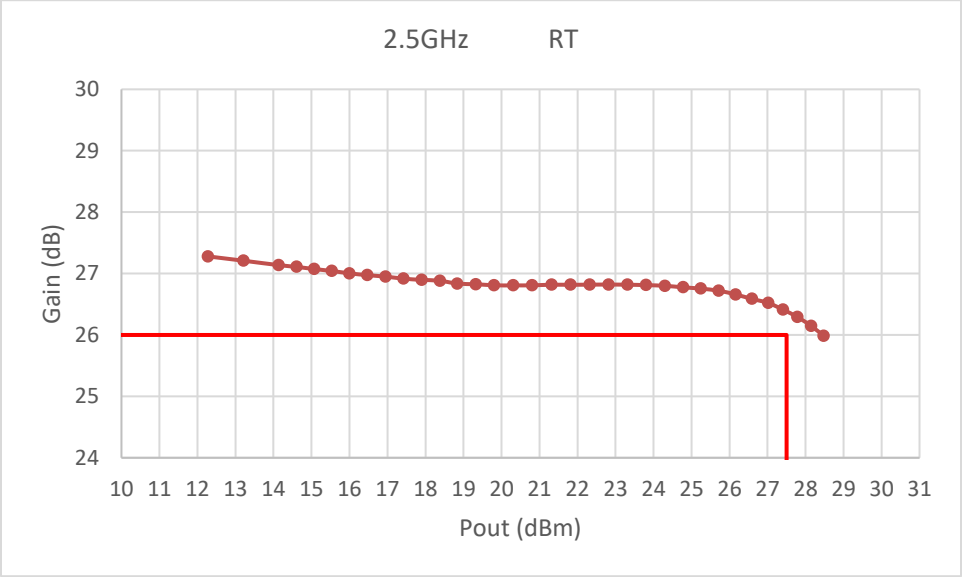


Figure 11-16 Measurement of gain over output power

11.2.2.4 PAE

The PAE measurement result is depicted in Figure 11-17.

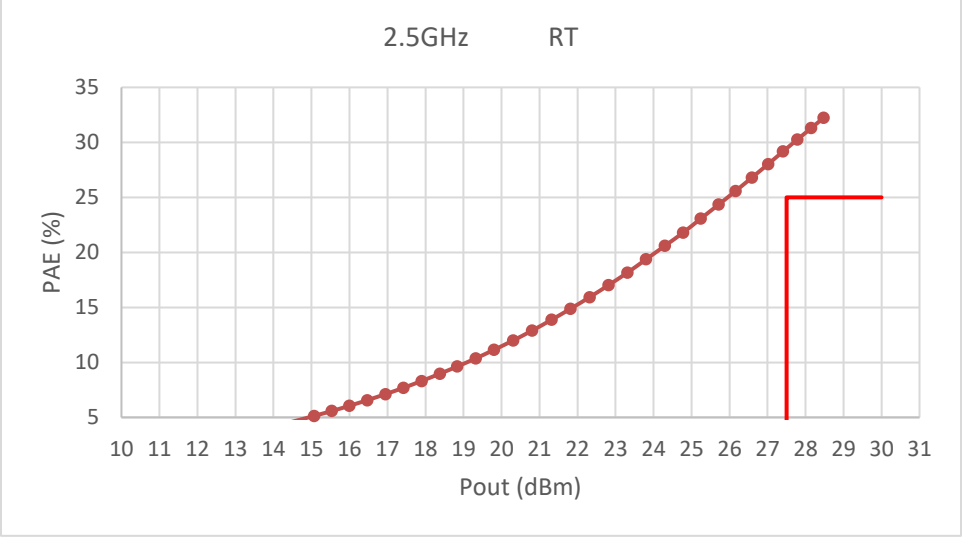


Figure 11-17 Measurement of PAE over output power

11.2.2.5 Current

The Current measurement result is depicted in Figure 11-18.

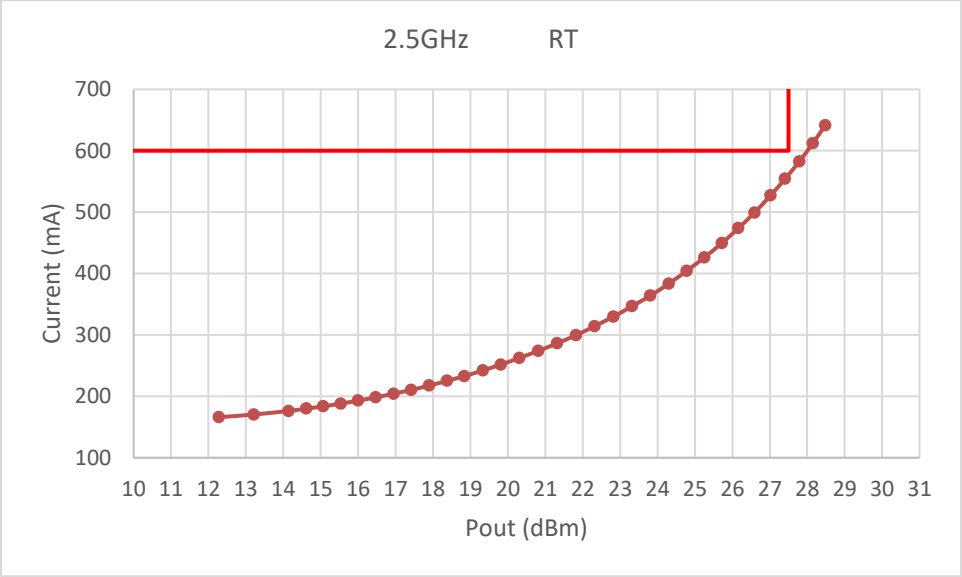


Figure 11-18 Measurement of current over the output power

11.2.2.6 Harmonics

The Harmonics measurement result is depicted in Figure 11-19 to Figure 11-22.

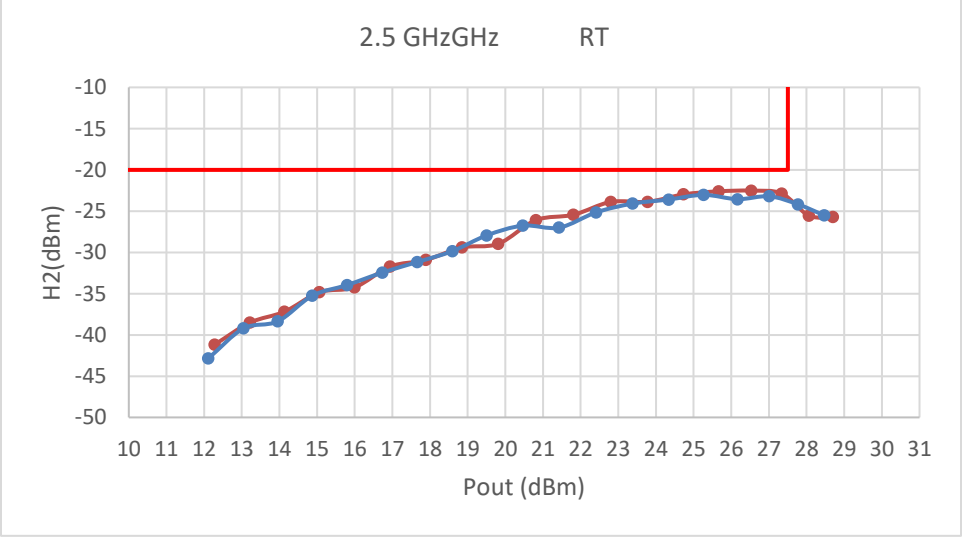


Figure 11-19 Second harmonic over output power

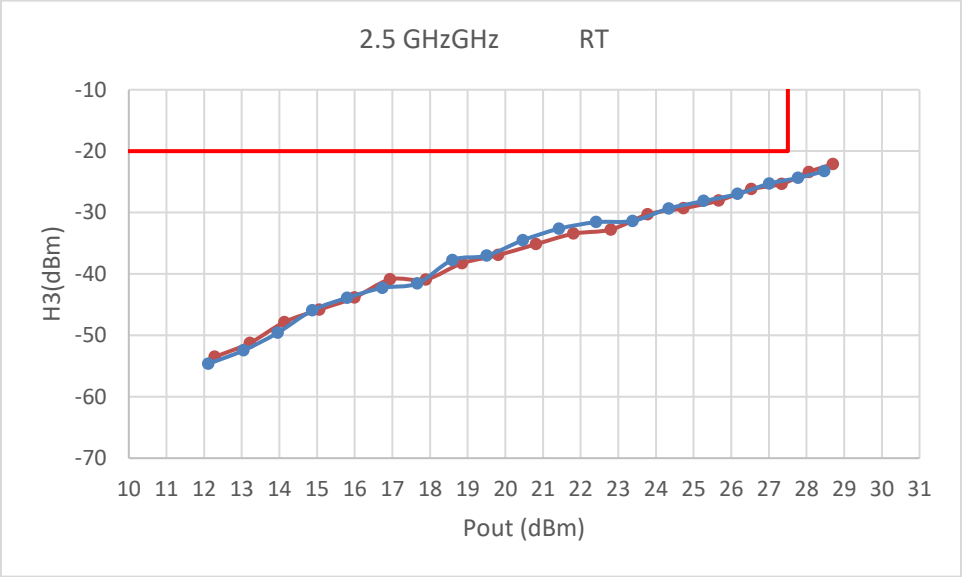


Figure 11-20 Third harmonic over output power

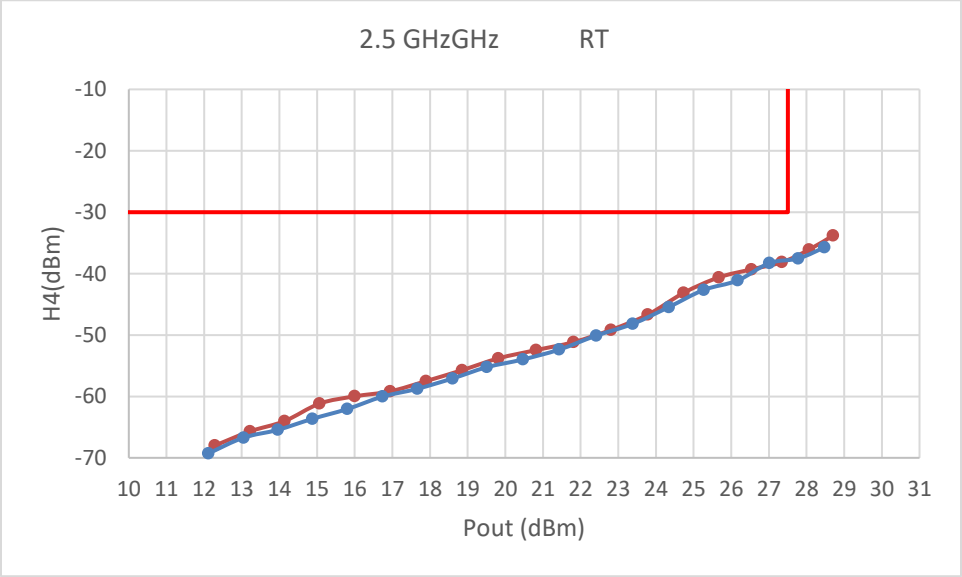


Figure 11-21 Fourth harmonic over output power

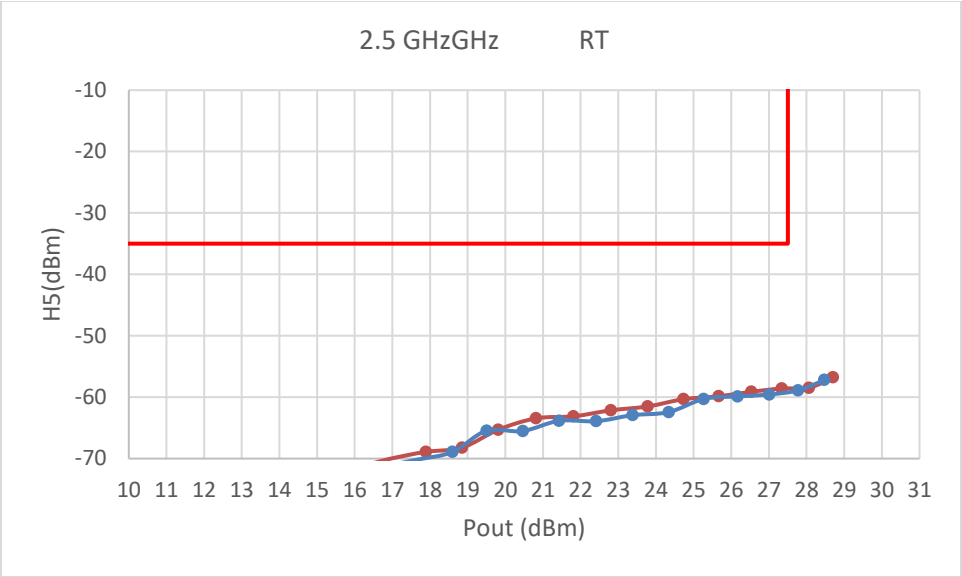


Figure 11-22 Fifth harmonic over output power

11.2.2.7 In Band Rx noise

The In band Rx noise measurement result is depicted in Figure 11-23.

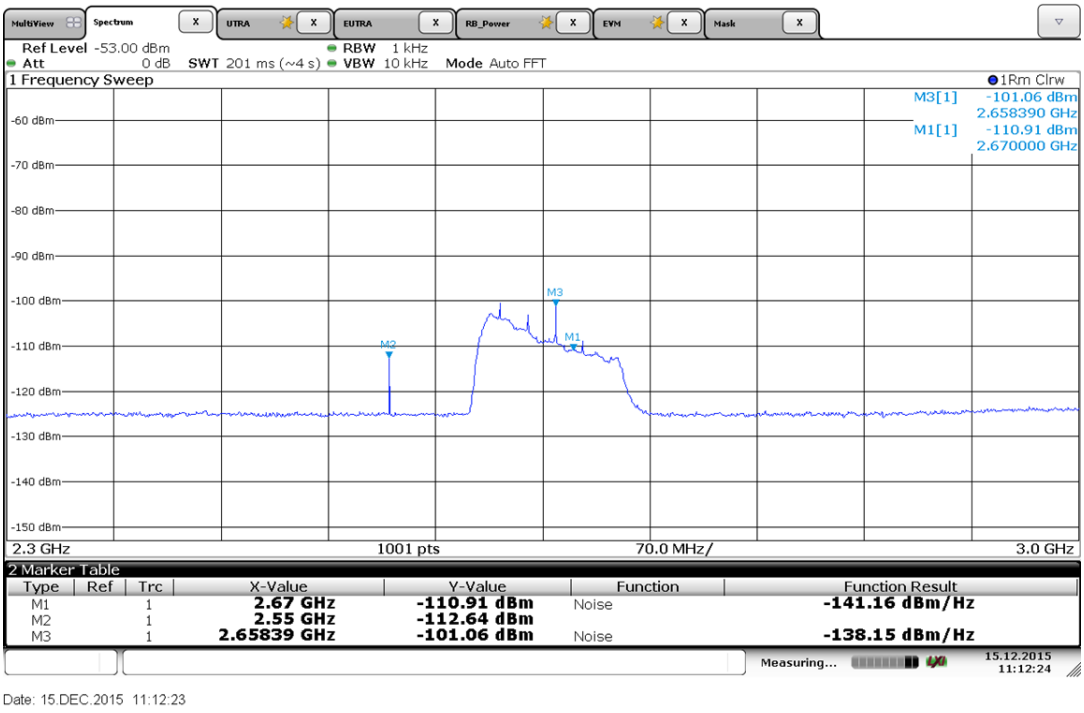


Figure 11-23 Measurement In band B7 Rx noise

11.3 VLC Simulation result

VLC measurement is not performed in this dissertation, normally it requires the random bit to measure the eye diagram. Figure 11-24 shows the simulation result of VLC output with 1 MHz data rate. It clearly shows that the waveform is good without distortion and enough V_{pp} to supply the next stage. With integration of RF FEM and VLC, it is promising to achieve the ubiquitous communication.

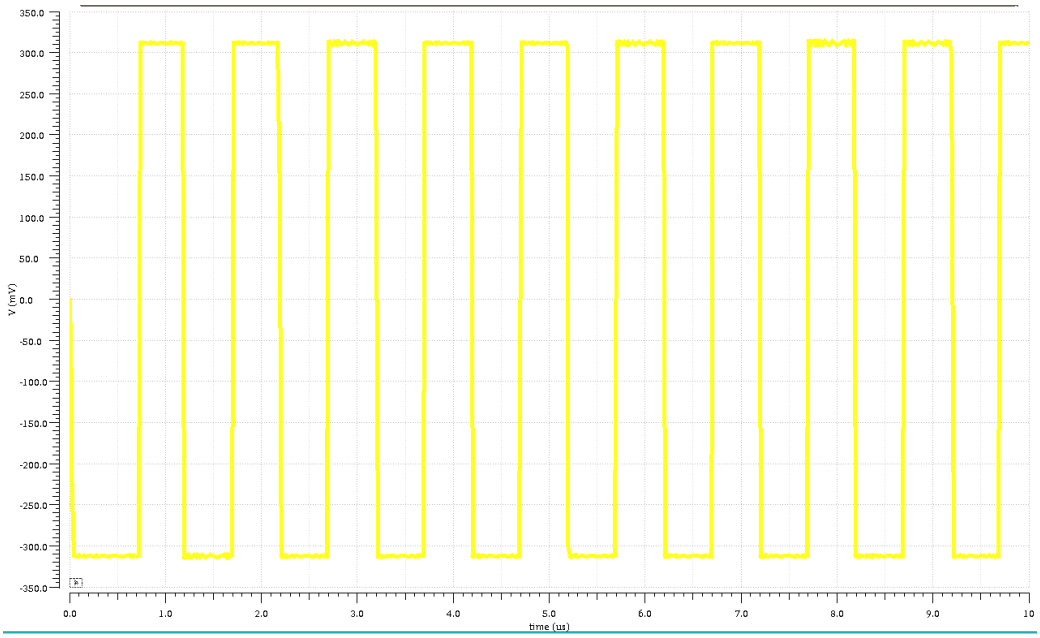


Figure 11-24 Simulation result of VLC output results with 1 MHz data output

11.4Comparison of Key performance of SKY77643-11 and this design

The overall measurement result covering LB/MB/HB is compared with SKY77643-11.

Table 11-1 Comparison of Key performance of SKY77643-11 and this design

LTE Band	Key Parameter	SKY77643-11 (Datasheet)	This design (Measured)
B7 2500 – 2570 MHz	TX Power	28.0dBm	27.5dBm
	Gain (dB)	>28.0dB	26.5dB
	UTRA_ACLR1 (dBc)	-40.0dBc typ.	-38.4dBc
	PAE (%)	29.5%	29.0%
	EVM	3.0%	2.9%
	Max. H2 H3 (dBm)	-21.0/-16.0dBm	-23.9/-25.5dBm
B1 1920 – 1980 MHz	TX Power	27.0dBm	27.5dBm
	Gain (dB)	>27.5dB	27.0dB
	UTRA_ACLR1 (dBc)	-40dBc typ.	-34.6dBc
	PAE (%)	34.7%	32.1%
	EVM	2.5%	4.5%
	Max. H2 H3 (dBm)	-12.0/-15.0dBm	-32.3/-37.4dBm
B8 880 – 915 MHz	TX Power	27.0dBm	27.5dBm
	Gain (dB)	>28.0dB	28.4dB
	UTRA_ACLR1 (dBc)	-40.0dBc typ.	-36.5dBc
	PAE (%)	37.0%	35.2%
	EVM	2.5%	3.2%
	Max. H2 H3 (dBm)	-13.0/-17.0dBm	-15.2/-23.6dBm

Band	Key Parameter	SKY77643-11 (Datasheet)	This design (Measured)
TDD B38 2570 – 2620 MHz	TX Power	27.7dBm	28.2dBm
	Gain (dB)	>29.0dB	28.8dB
	UTRA_ACLR1 (dBc) (10MHz, 12RB)	-40.0dBc typ.	-40.2dBc
	PAE (%)	29.0%	32.6%
	EVM	3.0%	1.9%
	Max. H2 H3 (dBm)	-21.0/-16.0dBm	-24.6/-15.3dBm
TDD B39 1880 – 1920 MHz	TX Power	27.0dBm	27.5dBm
	Gain (dB)	>27.5dB	29.2dB
	UTRA_ACLR1 (dBc)	-40.0dBc typ.	-43.0dBc
	PAE (%)	32%	35.9%
	EVM	3.0%	1.9%
	Max. H2 H3 (dBm)	-13.0/-15.0dBm	-19.1/-22.5dBm

Band	Key Parameter	SKY77643-11 (Datasheet)	MORF902 ES1 (Measured)
3G B1 1920 – 1980 MHz	TX Power	28.0dBm	28.0dBm
	Gain (dB)	>27.0dB	27dB
	UTRA_ACLR1 (dBc) (10MHz, 12RB)	-40.0dBc typ.	-34dBc
	PAE (%)	40.0%	34%
	EVM	2.5%	1.3%
	Max. H2 H3 (dBm)	-12.0/-15.0dBm	-36.5/-43.2dBm
3G B5 824 – 849 MHz	TX Power	27.0dBm	28.0dBm
	Gain (dB)	>28.0dB	28.6dB
	ACLR1_5M (dBc)	-40.0dBc typ.	-41.0dBc
	PAE (%)	37.0%	37.5%
	EVM	2.5%	1.5%
	Max. H2 H3 (dBm)	-7.0/-13.0dBm	-20.5/-30.5dBm

We can see from the Table 11-1, the performance of FEM SoC designed in IBM SOI is fully competitive with Skyworks which use a SIP solution. Take fully advantage of CMOS SOI, the cost and size could achieve better.

Chapter 12 Conclusion

This dissertation reports the first SoC Front end module integrated with the receiver of VLC system in CMOS SOI 0.18um. Over the past decade, the increasing demand of customers for higher data rate and more functionalities within a small chip has driven the trend of integration of multi-mode multi-band FEM along with some other communication method like VLC.

The fabrication cost is one of the most critical factors. To reduce cost, the industry has been trying to include as many components in the FEM as possible, then CMOS technology has been the star of the integration due to the advantage over other technology, for example, GaAs. The bottleneck holding up the entire integration is the PA originated from the inferior characteristics of CMOS technology to deal with large signals. In this dissertation, due to the superior linearity and transistor stack capability, CMOS SOI is the chosen one.

The switch and PA are the important parts discussed in Chapter 3 and 5, the analog bias, control circuit and VLC receiver are introduced as well. The ESD design methodology, which is critical for the whole chip reliability, is elaborated. The Measurement clearly shows the competence with the other product in the market.

As a future improvement, in order to ensure the reliability of this design further. The PA may be considered to use a three-stack topology to share the voltage drop over each stack, thus enable the longer life cycle.

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