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A Resonant Two-Switch Boosting Switched-Capacitor Converter With Full-Range Voltage Gain Regulation for MPPT Applications

THESIS

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MASTER OF SCIENCE

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by

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ABSTRACT OF THE THESIS

A Resonant Two-Switch Boosting Switched-Capacitor Converter With Full-Range Voltage Gain Regulation for MPPT Applications

By

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Master of Science in Electrical Engineering and Computer Science

University of California, Irvine, 2024

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This thesis applies a fixed ON-time switching technique to a resonant switched-capacitor converter, called the 3X RTBSC-A converter, which is studied for maximum power point tracking (MPPT) applications. The previous converter, the 3X RTBSC converter, was unable to achieve full-range voltage gain regulation for relatively light loads. However, with a new switching technique known as Switching Technique A, full-range voltage gain regulation for all loads is completely possible. In addition, the converter achieves zero-voltage switching (ZVS) to retain a high efficiency. A mathematical analysis of the ideal circuit was completed to show the conducting states, voltage gain derivation, and component stresses. Under this analysis, the prototype circuit was designed with a maximum power level of 162 W and a resonant frequency of 100 kHz. Simulations in the LTspice software proved that the circuit would not be able to achieve full-range voltage gain regulation with regular 50% duty cycle switching. In addition, details are provided in the design of the prototype's control circuit and driver circuit used to create and execute Switching Technique A. An open loop experiment demonstrates that the voltage gain of the prototype circuit closely resembles the waveforms calculated from the ideal gain formula. Also, a relatively high efficiency is recorded for each load tested with a maximum recorded efficiency of 0.9544. In addition, examination of the steady state waveforms prove that the prototype circuit is executing ZVS.

To prepare the prototype for the MPPT experiment, a sensing circuit is designed to feed data to the microcontroller. A simple perturb and observe (P&O) algorithm is programmed to find the maximum power point (MPP). The specifications of the solar panel are also presented. The results of the MPPT experiment demonstrate that the MPP found by the MPPT algorithm closely follows the actual MPP that was found manually. In addition, the prototype achieved efficiencies between 0.87 and 0.92 during the MPPT experiment. The 3X RTBSC-A converter still has the potential to achieve higher efficiencies as indicated by the report on the original circuit.

Chapter 1

Introduction

A background on three topics is given. First, the topic of switched-capacitor converters (SCCs) is reviewed. This review includes why we design SCCs, the disadvantages that must be overcome, and the circuits that preceded the converter of focus. Second, a lecture on maximum power point tracking (MPPT) is given. This lecture is necessary for insight into the science of solar panels and why we need MPPT to use their power. Last, soft switching in converters is discussed. Soft switching greatly improves the efficiency of power converters and this section reviews a method of confirming the execution of soft switching in converters that use a half-bridge topology.

1.1 Switched-Capacitor Converters

SCCs are switching converters composed primarily of capacitors and switches. Without reliance on bulky inductors or transformers, SCCs potentially have lower electromagnetic interference, lighter weight, lower cost, higher energy density, and the potential for full integration [5]. However, there are some intrinsic features related to SCCs as well as challenges

in developing SCCs that need to be recognized. First of all, SCCs produce high current spikes during transitions between switching states; and they typically have fixed gain. The efficiency of SCCs is closely related to voltage gain and circuit structure [6],[7]. Thus, when a voltage gain requirement and load range are given, it is essential to pair it with a proper topology and circuit parameters in order to achieve high efficiency.

A SCC with a symmetrical design, as shown in Fig. 1.1, is proposed in [1]. This converter, called the "Two-Switch Boosting Switched-Capacitor (TBSC) Converter," features a simple design method of adding more diode-capacitor networks to increase the voltage gain. Due to the symmetrical interleaved configuration of the circuit, ripple cancellation is achieved and the output voltage ripple is reduced. Furthermore, the TBSC converter features a low component count and high efficiency.

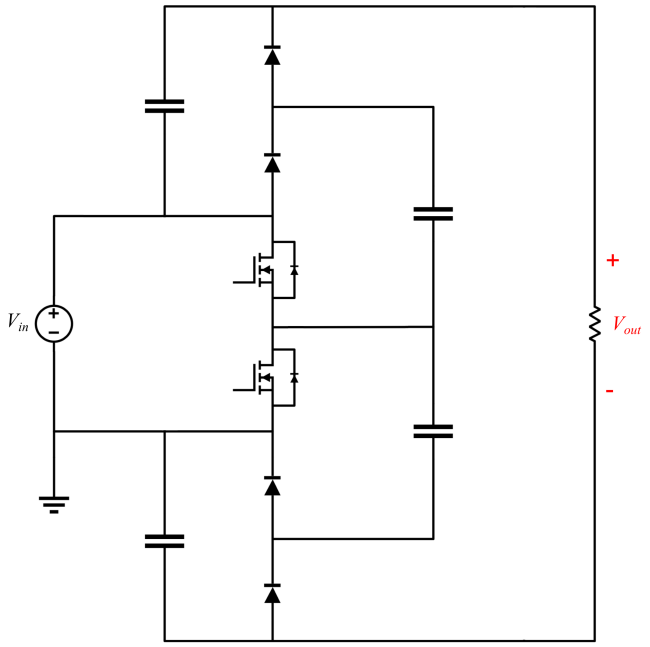
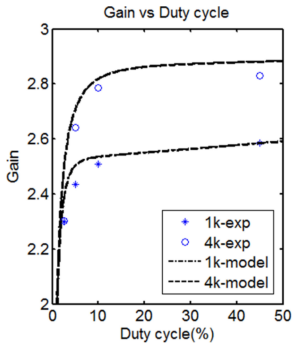


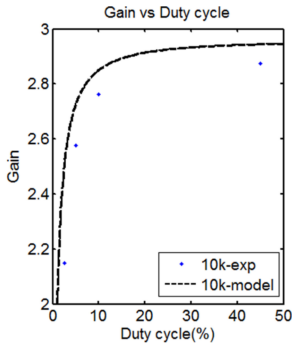
Figure 1.1: Topology of the triple-gain TBSC converter.

Like most SCCs, this converter is switched at a fixed duty cycle and fixed frequency. This is because switching signal variations achieve very little gain regulation when either the duty

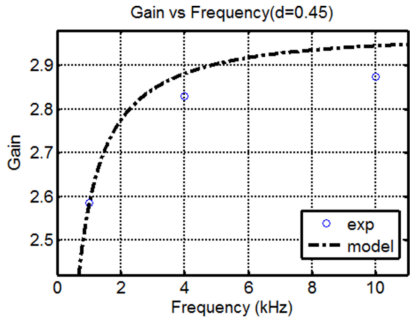
cycle or frequency is modulated as shown in Fig. 1.2.



(a) TBSC gain vs. duty cycle of 1 kHz and 4 kHz switching signals.



(b) TBSC gain vs. duty cycle of 10 kHz switching signals.



(c) TBSC gain vs. frequency.

Figure 1.2: Voltage gain modulation results of the TBSC. Figure from [1].

Also, the input current of the TBSC converter experiences a spike every switching cycle that must be calculated and monitored during design and operation respectively. An example of this current spike is shown in Fig. 1.3.

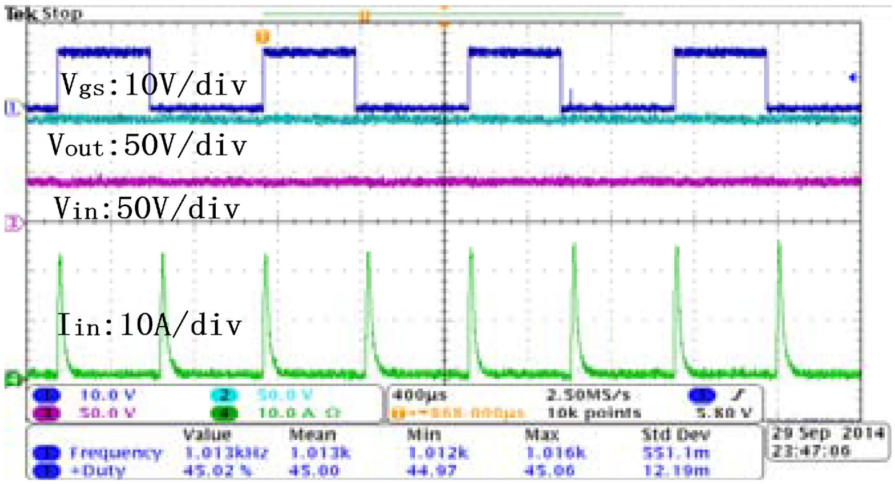


Figure 1.3: Steady state waveforms of the TBSC converter. The input current is shown in green. Figure from [1].

An improvement proposed in [2] features the addition of a resonant tank, as shown in Fig. 1.4, and simpler, frequency-modulated switching signals that achieve greater results, such as zero-voltage switching (ZVS) turned-ON transistors, zero-current switching (ZCS) turned-

ON/OFF diodes, and wider voltage gain regulation. Futhermore, the addition of a resonant tank eliminates the troublesome input current spike that the original TBSC converter experienced and also makes voltage gain regulation possible.

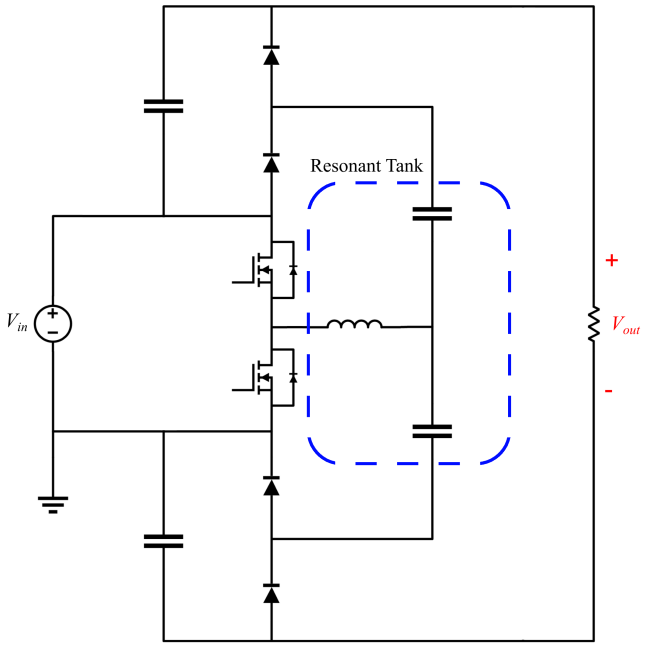


Figure 1.4: Topology of the triple-gain RTBSC converter.

However, the "Resonant Two-Switch Boosting Switched-Capacitor (RTBSC) Converter" can only achieve wide gain regulation when its quality factor (Q) is relatively large. If Q is too small, which means a very light load condition, the gain regulation range is limited, as shown in Fig. 1.5.

A converter similar to the RTBSC converter, called the "Ladder Resonant Switched-Capacitor Converter (Ladder RSCC)," was also studied as shown in Fig. 1.6.

Multiple switching techniques were proposed for achieving full-range voltage gain regulation [3]. The most promising switching techniques were known as Switching Technique A and B. These techniques use a fixed ON-time signal for one transistor while the ON-time of the

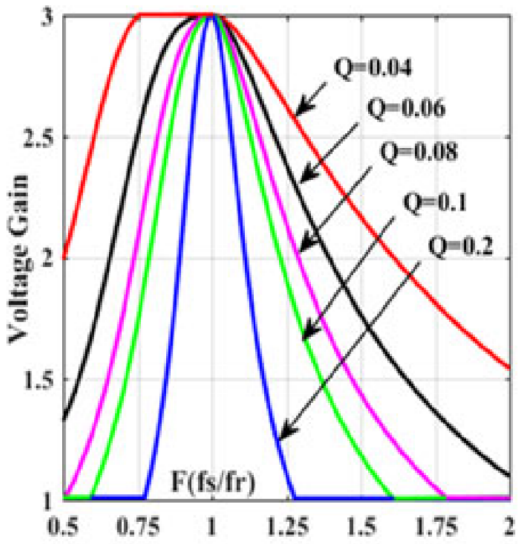


Figure 1.5: Voltage gain modulation results of the triple-gain RTBSC converter for different loads. Figure from [2].

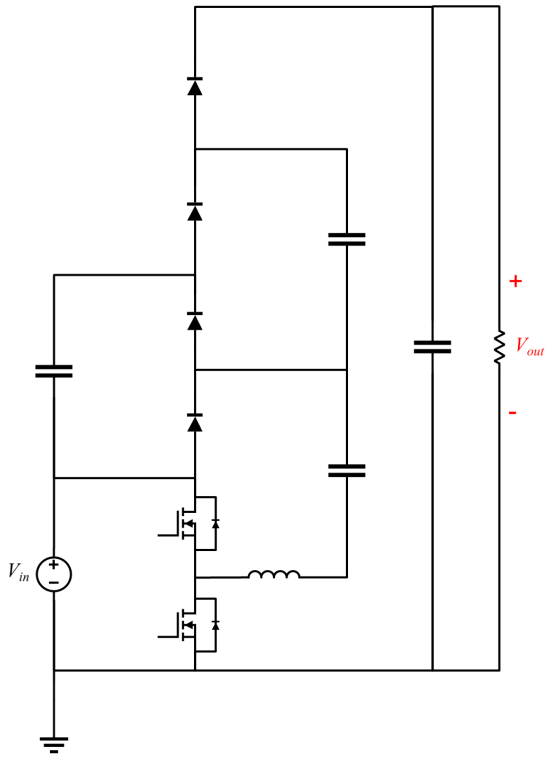
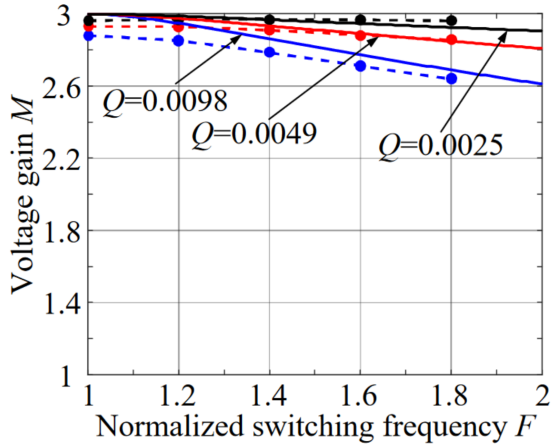
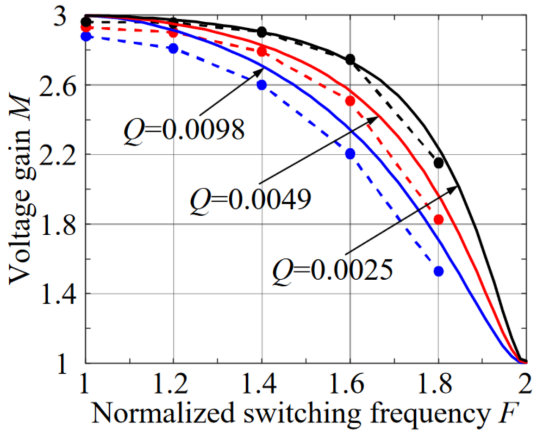


Figure 1.6: Topology of the Ladder RSCC.

other transistor was adjusted for gain regulation. Both Switching Technique A and B were shown to provide full-range voltage gain regulation to the Ladder RSCC [3],[8]. Fig. 1.7 shows a comparison of the 50% duty cycle switching technique and Switching Technique B on the Ladder RSCC voltage gain modulation. The voltage regulation techniques proposed in [3] are general enough that they can be applied to known SCCs [9].



(a) Ladder RSCC voltage gain regulation with the 50% duty cycle switching technique.



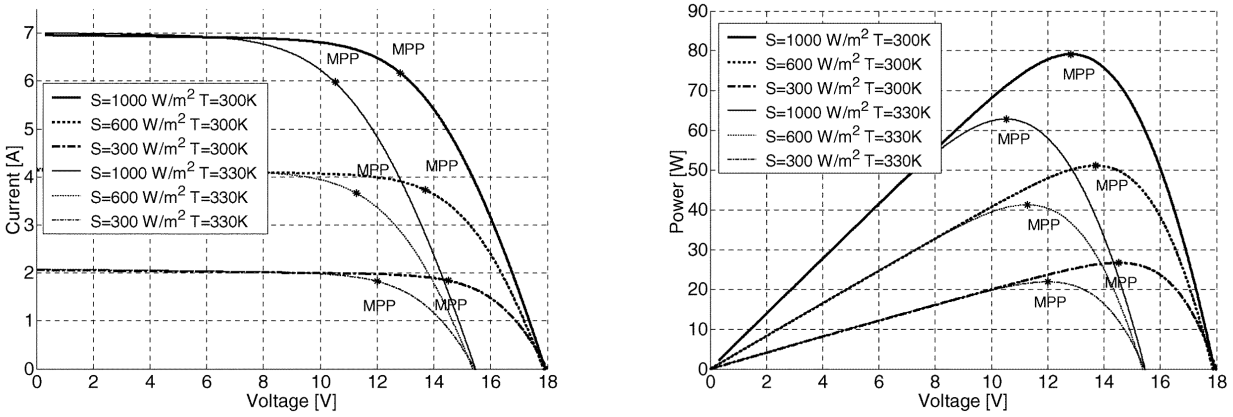
(b) Ladder RSCC voltage gain regulation with Switching Technique B.

Figure 1.7: Voltage gain modulation results of the Ladder RSCC. Figure from [3].

In the next chapter, full-range voltage gain regulation is applied to a 3X (triple gain) RTBSC converter with ZVS operation. Compared to the RTBSC converters mentioned previously, this new version will incorporate the Switching Technique A that was used to achieve full-range voltage gain regulation for the Ladder RSCC. With this new switching technique, the 3X RTBSC converter will be able to achieve full-range voltage gain with any Q. To differ from the original 3X RTBSC converter, this converter operating using Switching Technique A will be dubbed the "3X RTBSC-A" converter. Similar to the RTBSC converters, the transistors are ZVS turned-ON and the diodes are ZCS turned-ON/OFF, reducing the switching loss significantly. The main operation mode, voltage gain curves, soft-switching regions, output characteristics, and current/voltage stresses of the resonant tank of the 3X RTBSC-A converter are analyzed in detail. A 3X RTBSC-A converter prototype was built to verify the analyses.

1.2 Solar Panels and Maximum Power Point Tracking

An example of the I-V relationship of a solar panel is shown in Fig. 1.8(a). Our first observation is that the I-V relationship varies as a result of the irradiance level S and the temperature T. For each distinct case, a maximum voltage exists when the solar panel has an open circuit load, V_{oc}. This is the point where $I = 0$. A maximum current also exists when the solar panel has a short circuit load, I_{sc}. This is the point where $V = 0$. Between these two points is a very unique location called the maximum power point (MPP), where the solar panel produces maximum output power. The MPP is more evident when the P-V relationship of a solar panel is calculated as shown in Fig. 1.8(b).



(a) I-V relationship of an arbitrary solar panel. (b) P-V relationship of an arbitrary solar panel.

Figure 1.8: An example of solar panel characteristics. Figure from [4].

In power electronics, the MPP is greatly sought after because it represents the highest possible energy harvesting from a solar panel and achieves the greatest efficiency for any converters working with it. Since the MPP varies depending on S and T, it is necessary to continuously track the MPP in order to maximize the power output from a photovoltaic system for a given set of operating conditions [4]. This is called maximum power point tracking (MPPT).

The most common method to track the MPP is with the perturb and observe (P&O) tech-

nique. It is based on the following criterion: if the operating voltage of the solar panel is perturbed in a given direction and if the power drawn from the solar panel increases, this means that the operating point has moved toward the MPP and, therefore, the operating voltage must be further perturbed in the same direction. Otherwise, if the power drawn from the solar panel decreases, the operating point has moved away from the MPP and, therefore, the direction of the operating voltage perturbation must be reversed [4].

A visual example of the P&O technique can be observed in Fig. 1.9. During a change in atmospheric conditions, the MPP of the solar panel becomes a greater value. As a result, the P&O technique samples the power at regular intervals and modulates the solar panel voltage until it finds the new MPP.

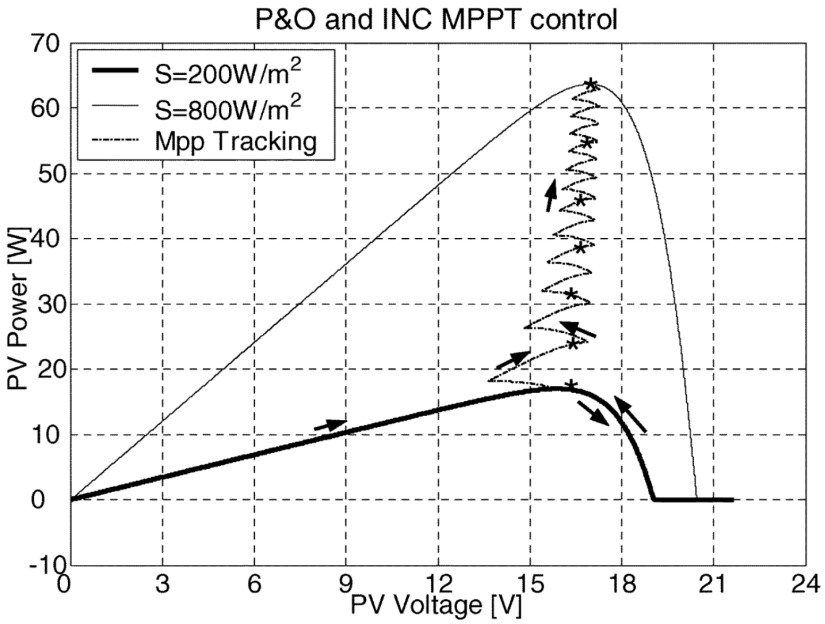


Figure 1.9: Visual example of the P&O technique finding the MPP during atmospheric changes. Figure from [4].

1.3 Soft Switching

Switching loss is one of the major sources of loss and inefficiencies in switching converters. The so-caused average power loss generated could be severe.

To reduce switching loss, a mechanism known as "soft switching" can be implemented. Soft switching occurs when a semiconductor device transitions between ON or OFF states while both the voltage across and current through its switching channel are at zero. For example, the drain-source voltage of a MOSFET goes to zero before the MOSFET turns ON. Afterwards, the drain current rises without any overlap from the drain-source voltage. This method of soft switching is known as zero-voltage switching (ZVS).

The main advantage of resonant converters over other converters is their natural ability to achieve ZVS under certain criteria. This can be observed through analysis of the half-bridge switching network seen in most resonant converters as shown in Fig. 1.10.

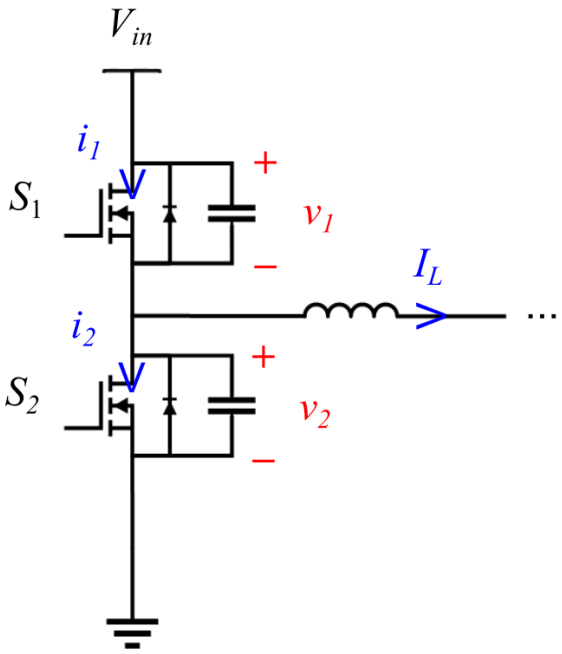


Figure 1.10: The half-bridge switching network used for analysis of soft switching.

Since the time domain we are analyzing is so small, we can assume the current through the inductor is DC.

Through analysis, we can find that during the "S_1 turn-ON/S_2 turn-OFF" transition, S_1 turns ON with ZVS and S_2 turns OFF with very little voltage-current overlap if the inductor current is negative. These waveforms are visualized in Fig. 3.5.

Likewise, the inductor current must be positive in order for S_2 to turn ON with ZVS and S_1 to turn OFF with little voltage-current overlap.

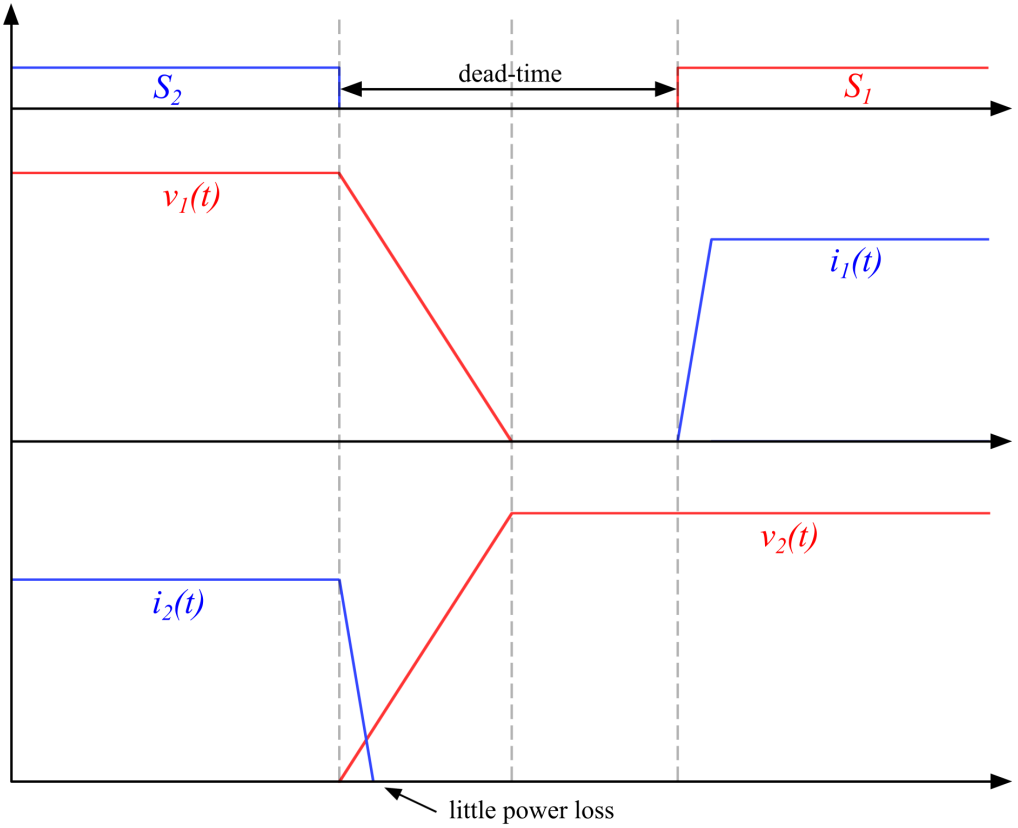


Figure 1.11: Waveforms of the half-bridge switching network indicate ZVS turn-ON of S_1 and little voltage-current overlap of S_2.

Chapter 2

Full-Range Regulation of 3X RTBSC-A Converter

The converter itself is analyzed in great detail. First, the operation of the 3X RTBSC-A converter is discussed thoroughly. This includes analysis of Switching Technique A, the conducting states of the 3X RTBSC-A converter, and why 50% duty cycle switching doesn't work. Second, a method of deriving the voltage gain equation of the 3X RTBSC-A converter is described. Last, the voltage and current stress of several components is also derived.

2.1 Operation

The topology of the 3X RTBSC-A converter is shown in Fig. 2.1. This topology features a symmetrical structure. For convenience, the upper-half is dubbed the "A-side" and the lower-half is dubbed the "B-side." $S_{A,B}$ are MOSFETs with internal anti-parallel diodes. D_{0A}, D_{1A}, D_{0B}, and D_{1B} are power diodes. An inductor L_r and two film capacitors $C_{rA,rB}$ constitute the resonant tank. The resonant capacitors have equal capacitance C_r. Capacitors

$C_{1A,1B}$ are charge banks with large capacitances. Capacitors C_{in} and C_{out} filter out voltage ripple across the input and output sides respectively. Inductor L_{in} flattens the input current into a DC waveform which will be preferred for the MPPT experiments.

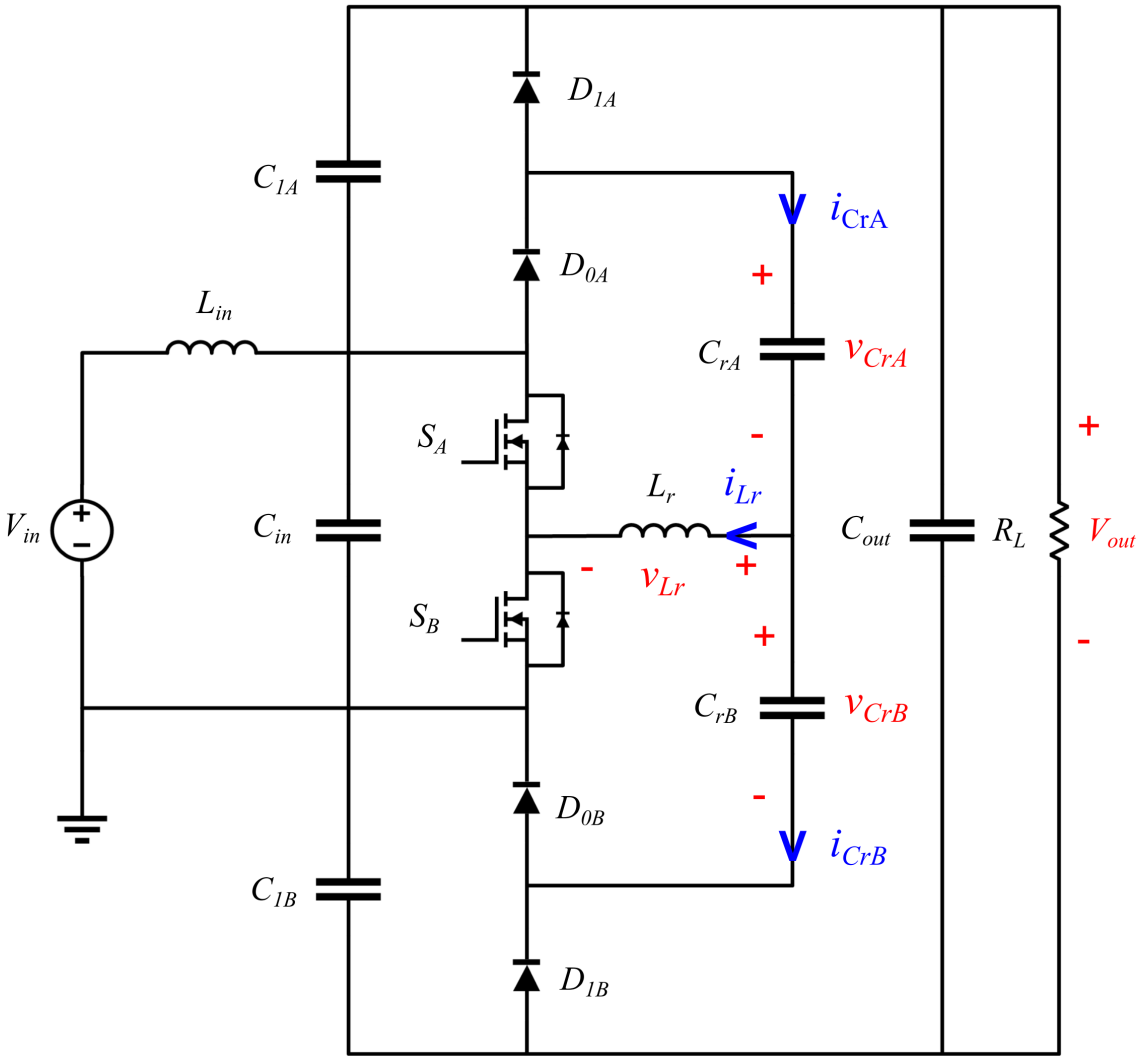


Figure 2.1: The proposed 3X RTBSC-A converter topology.

The resonant frequency, f_r, of the resonant tank can be calculated with (2.1).

$$f_r = \frac{1}{2\pi\sqrt{2C_rL_r}} \tag{2.1}$$

The normalized switching frequency, F, is defined as (2.2).

$$F = f_s/f_r \tag{2.2}$$

Accordingly, the maximum and minimum normalized switching frequencies are calculated as (2.3) and (2.4) where $f_{s,\max}$ and $f_{s,\min}$ are the maximum and minimum switching frequencies respectively.

$$F_{\max} = f_{s,\max}/f_r \tag{2.3}$$

$$F_{\min} = f_{s,\min}/f_r \tag{2.4}$$

The 3X RTBSC converter is normally operated over the frequency range $1 < F < 2$. For Switching Technique A, the ON-time of S_A must remain constant. The ON-time (t_{on}) can be calculated with (2.5).

$$t_{on} = 1/(2f_r) \tag{2.5}$$

The ON-time of S_B is varied by equivalent duty cycle d and normalized switching frequency F. The equivalent duty cycle d can be calculated with (2.6).

$$d = \frac{F_{\max} - F}{2(F_{\max} - F_{\min})} \tag{2.6}$$

For the 3X RTBSC-A converter, $F_{\max} = 2$ and $F_{\min} = 1$. So d can be calculated as (2.7).

$$d = 1 - F/2 \tag{2.7}$$

We can observe a visual representation of Switching Technique A in Fig. 2.2. The higher transistor (S_A) has a fixed ON-time while the lower transistor has a complementary and adjustable ON-time that changes the frequency of both switching signals. The time frame of each conducting state and an approximation of other important measurements are also shown. We can observe that $-i_{Lr}(t)$ is expected to be negative when S_A turns ON. This indicates that the transistors are ZVS turned-ON.

The current paths of each conducting state are shown in Fig. 2.3.

In State 1, S_A is OFF while S_B is ON. Only diodes D_{0A} and D_{1B} are ON. V_{in} charges C_{rA} and L_r while C_{rB} transfers all of its charge into C_{1B}. C_{rB} was charged from a previous state.

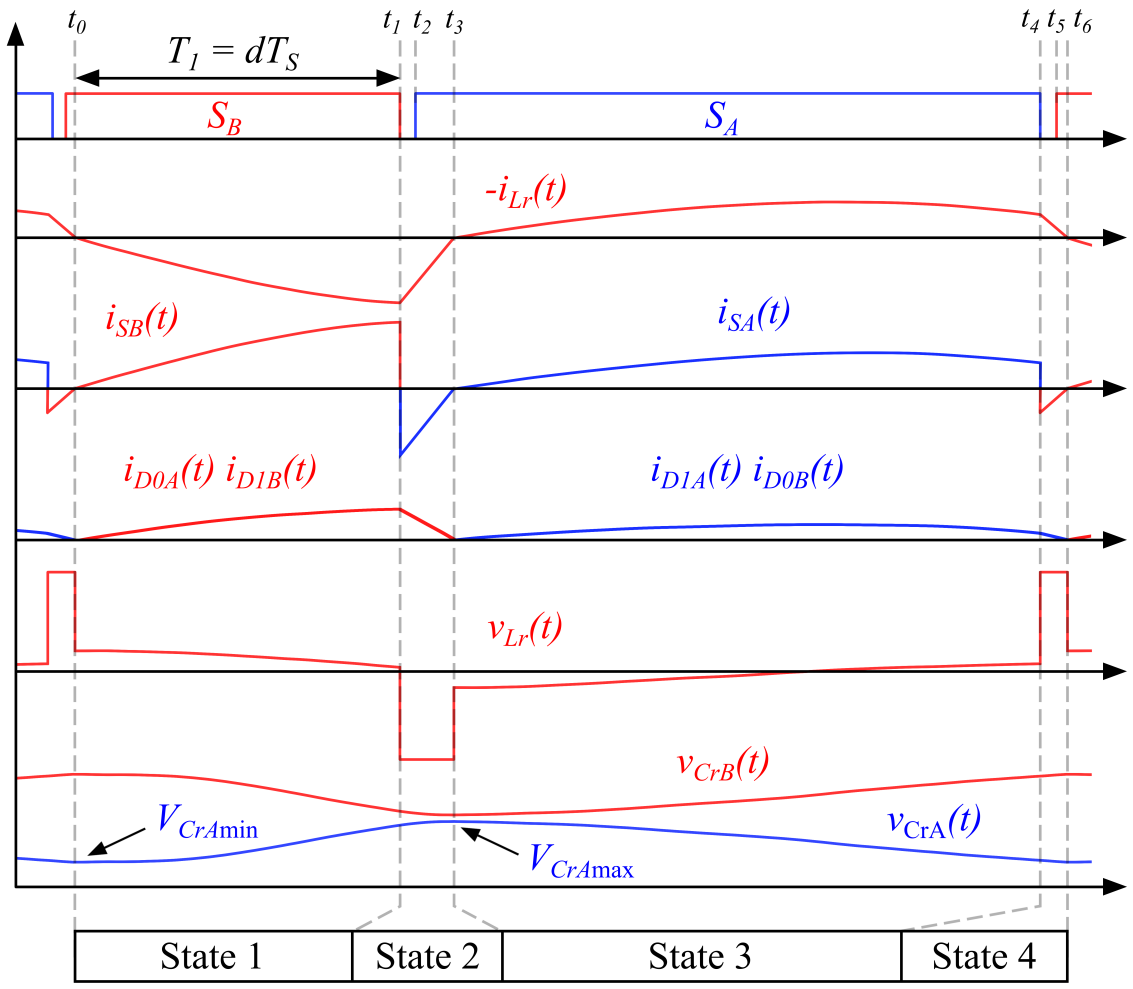
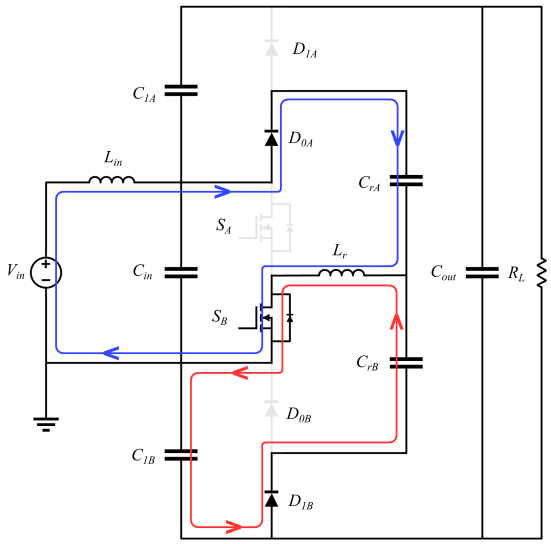


Figure 2.2: Component waveforms under operation of switching technique A.

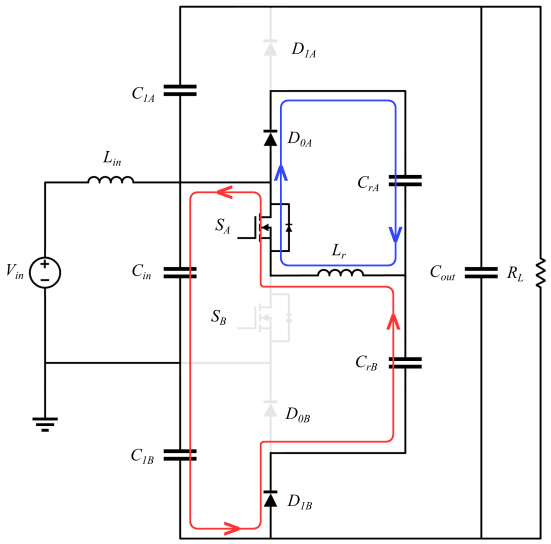
In State 2 (ignoring the dead-time), S_A is ON and S_B is OFF while the diodes keep the same state. The charged L_r continues to charge C_{rA} while C_{rB} continues to charge C_{1B}. The next state doesn't begin until L_r transfers all of its charge into C_{rA} and $i_{Lr}(t)$ reaches zero.

In State 3, the transistors keep the same state but diodes D_{1A} and D_{0B} are ON instead. C_{rA} begins transferring its charge into C_{1A} while V_{in} charges C_{rB} and L_r.

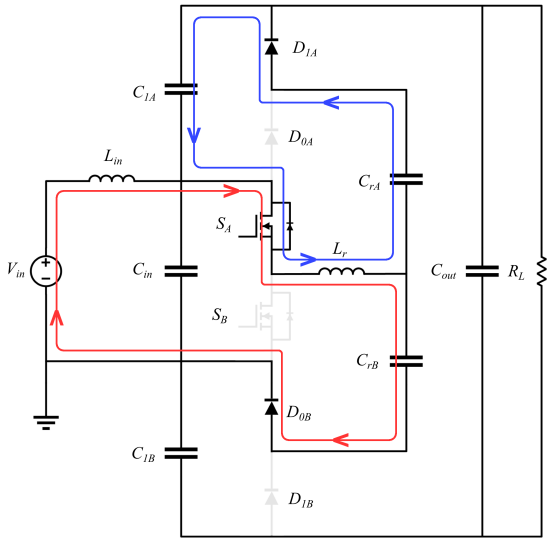
In State 4 (ignoring the dead-time), S_A is OFF, S_B is ON, and the diodes keep the same state. L_r continues to charge C_{rB} while C_{rA} continues to charge C_{1A}. This state doesn't end until L_r transfers all of its charge into C_{rB} and the whole cycle repeats from the start.



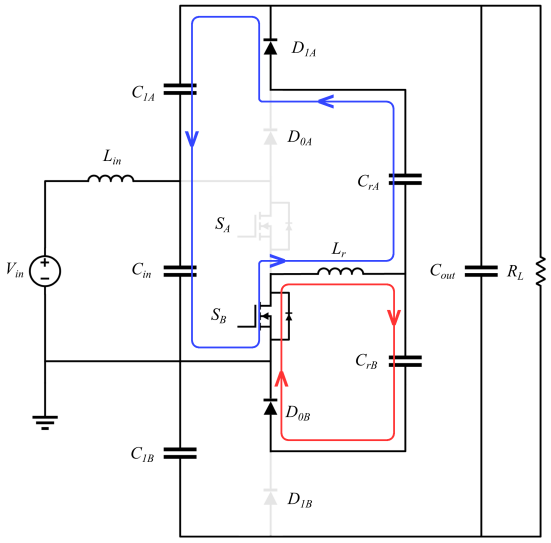
(a) State 1 [t_0-t_1].



(b) State 2 [t_1-t_3].



(c) State 3 [t_3-t_4].



(d) State 4 [t_4-t_6].

Figure 2.3: Conducting states of the 3X RTBSC-A converter.

As shown in Fig. 1.5, the 50% duty cycle switching cannot modulate the output voltage for a 3X RTBSC converter with a low Q. This is because, during the transient response, the charge bank capacitors C_{1A} and C_{1B} are not able to sufficiently discharge enough through the load resistance to sustain a lower voltage. As a result, the resonant capacitors continue to charge the charge bank capacitors near V_{in} every switching cycle and V_{out} barely changes when the frequency is modulated.

Switching Technique A adjusts the output voltage by reducing the ON-time of S_B. When the ON-time of S_B is reduced, capacitor C_{rA} will receive less charge from V_{in}. So, C_{1A} will receive less charge from C_{rA} during States 3 and 4. Capacitor C_{1B} will also receive less charge, even though capacitor C_{rB} is charged to a much higher voltage than C_{rA}. This is because the time C_{rB} discharges into C_{1B} (State 1 & 2) is relatively short. To put it simply, C_{1A} receives less charge because C_{rA} charges it with a small voltage for a long time, and C_{1B} receives less charge because C_{rB} charges it with a large voltage for a short time.

The load will have a modulated output voltage due to the partially charged charge bank capacitors C_{1A} and C_{1B}.

2.2 Gain Derivation

Before deriving the gain, several variables must be addressed. The quality factor, Q, is defined by (2.8).

$$Q = \frac{1}{R_L}\sqrt{\frac{L_r}{2C_r}} \tag{2.8}$$

A load-dependent variable, m, is defined as (2.9).

$$m = \frac{F}{2\pi Q} \tag{2.9}$$

A control variable, h, is defined as (2.10).

$$h = \cos\left(2\pi \frac{d}{F}\right) = \cos(2\pi f_r T_1) \tag{2.10}$$

The voltage across both charge-bank capacitors are observed to be approximately DC and equal to V_C as f_s varies. The equivalent series resistance (ESR) of all capacitors, ON-resistance of switches, and forward voltage of diodes are neglected. Dead-time between the switching signals is also neglected.

First, in every operating state, the following equation is always held by performing KVL around the outermost loop:

$$V_{out} = 2V_C + V_{in} \tag{2.11}$$

Second, we can observe that both C_{1A} and the load are charged by C_{rA} during T_3 and T_4. This means all of the charges delivered to the load will be first stored in C_{rA} in each switching cycle. According to the charge balance of C_{rA}:

$$C_r(V_{CrA\max} - V_{CrA\min}) = T_s \frac{V_0}{R_L} \tag{2.12}$$

After some manipulation, (2.12) can be described as (2.13).

$$V_{out} = \frac{m}{2}(V_{CrA\max} - V_{CrA\min}) \tag{2.13}$$

Next, the functions of $v_{CrA}(t)$ and $i_{Lr}(t)$ must be found in nearly all of the switching states. Two sets of boundary conditions are observed in the waveforms:

$$i_{Lr}(t_3) = 0,\ v_{CrA}(t_3) = V_{CrA\max} \tag{2.14}$$

$$i_{Lr}(t_{0/6}) = 0,\ v_{CrA}(t_{0/6}) = V_{CrA\min} \tag{2.15}$$

KCL can be performed at the junction combining all of the resonant components. (2.16) is derived, and will be used in the analysis of each switching state.

$$2C_r\frac{dv_{CrA}(t)}{dt} = i_{Lr}(t) \tag{2.16}$$

State 1 [t_0-t_1]: Differential equations (2.16) and (2.17) can be used to derive the solutions (2.18) and (2.19).

$$L\frac{di_{Lr}(t)}{dt} + v_{CrA}(t) = V_{in} \tag{2.17}$$

$$i_{Lr}(t) = -2C_r\omega_r(V_{CrA\min} - V_{in})\sin(\omega_r[t - t_0]) \tag{2.18}$$

$$v_{CrA}(t) = V_{in} + (V_{CrA\min} - V_{in})\cos(\omega_r[t - t_0]) \tag{2.19}$$

State 2 [t_1-t_3]: Differential equations (2.16) and (2.20) can be used to derive the solutions (2.21) and (2.22).

$$L\frac{di_{Lr}(t)}{dt} + v_{CrA}(t) = 0 \tag{2.20}$$

$$i_{Lr}(t) = -2C_r\omega_r V_{CrA\max}\sin(\omega_r[t - t_3]) \tag{2.21}$$

$$v_{CrA}(t) = V_{CrA\max}\cos(\omega_r[t - t_3]) \tag{2.22}$$

State 3 [t_3-t_4]: Differential equations (2.16) and (2.23) can be used to derive the solutions (2.24) and (2.25).

$$L\frac{di_{Lr}(t)}{dt} + v_{CrA}(t) = V_C \tag{2.23}$$

$$i_{Lr}(t) = -2C_r\omega_r(V_{CrA\max} - V_C)\sin(\omega_r[t - t_3]) \tag{2.24}$$

$$v_{CrA}(t) = V_C + (V_{CrA\max} - V_C)\cos(\omega_r[t - t_3]) \tag{2.25}$$

State 4 [t_4-t_6]: Since T_4 is very small compared to T_s, we can make the following approximation about $v_{CrA}(t)$:

$$v_{CrA}(t) \approx V_{CrA\min} \tag{2.26}$$

After analyzing each state, we can derive some important relationships.

Since $T_3/T_r \approx 0.5$, the following approximation can be made that:

$$\cos(\omega_r T_3) = -1 \tag{2.27}$$

$v_{CrA}(t)$ must be continuous across t_4. So (2.25) and (2.26) must be equal to each other at $t = t_4$. If we calculate this and include (2.27), we can derive (2.28).

$$2V_C = V_{CrA\min} + V_{CrA\max} \tag{2.28}$$

(2.19) and (2.22) must also be equal to each other at $t = t_1$. If we calculate this and include (2.10), we can derive (2.29).

$$\cos(\omega_r T_2) = \frac{V_{in} + (V_{CrA\min} - V_{in})h}{V_{CrA\max}} \tag{2.29}$$

$i_{Lr}(t)$ must also be continuous across t_1. So (2.18) and (2.21) must be equal to each other at $t = t_1$. If we calculate this and include (2.10), we can derive (2.30).

$$\sin(\omega_r T_2) = \frac{(V_{in} - V_{CrA\min})\sqrt{1 - h^2}}{V_{CrA\max}} \tag{2.30}$$

(2.11), (2.13), and (2.28) can be used to solve for $V_{CrA\max}$ and $V_{CrA\min}$ in terms of V_{in}, V_0, and m. The resulting equations are (2.31) and (2.32), where $M_{CrA\min} = V_{CrA\min}/V_{\text{in}}$, $M_{CrA\max} = V_{CrA\max}/V_{in}$, and $M = V_{out}/V_{in}$.

$$M_{CrA\min} = M\left(\frac{1}{2} - \frac{1}{m}\right) - \frac{1}{2} \tag{2.31}$$

$$M_{CrA\max} = M\left(\frac{1}{2} + \frac{1}{m}\right) - \frac{1}{2} \tag{2.32}$$

Finally, (2.29) and (2.30) can be combined using Euler's Identity, and (2.31) and (2.32) can be substituted into the calculated equation. The gain equation is finally calculated as (2.33). The waveforms calculated with (2.33) are shown in comparison with the open-loop experimental results in Fig. 3.9(a) in Chapter 3.

$$M = \frac{1}{4}\Big[m(-1+h) + 2(2-h)\Big] + \sqrt{\frac{1}{16}\Big[m(-1+h) + 2(2-h)\Big]^2 + \frac{3}{2}m(1-h)} \tag{2.33}$$

2.3 Component Stress

The current base parameter, I_b, is defined as follows:

$$I_b = \frac{V_{in}}{\sqrt{L_r/(2C_r)}} \tag{2.34}$$

To find the RMS current of the resonant inductor, we will have to use the inductor current equation found in each state: (2.18), (2.21), and (2.24) (State 4 can be ignored since T_4 is very small compared to T_s).

The resonant inductor current can be treated like a piecewise function and the RMS calculations can be executed. It's important to note that during these calculations, T_2 can be approximated with (2.35) according to the Taylor series expansion of a sine function.

$$T_2 \approx \frac{1}{\omega_r}\sin(\omega_r T_2) = \frac{1}{\omega_r}\frac{(V_{in} - V_{CrA\min})\sqrt{1-h^2}}{V_{CrA\max}} \tag{2.35}$$

The normalized RMS current of the inductor is obtained as (2.36).

$$\begin{aligned} J_{Lr\mathrm{rms}} = \frac{1}{2}\Bigg[& (M_{CrA\min}-1)^2\left(2d - \frac{1}{\pi}Fh\sqrt{1-h^2}\right) \\ & + \frac{F}{\pi}(1-M_{CrA\min})\Big[(M_{CrA\max}-1) + h(1-M_{CrA\min})\Big]\sqrt{1-h^2} \\ & + F(M_{CrA\max}-M_C)^2\Bigg]^{1/2} \end{aligned} \tag{2.36}$$

The voltage stress of resonant capacitor C_{rA} was calculated to be (2.32) during the gain derivation. The voltage stress of resonant capacitor C_{rB} can be derived by observing that the KVL equation (2.37) is true in all states.

$$\begin{aligned} V_{in} + V_C &= v_{CrA}(t) + v_{CrB}(t) \\ &= V_{CrA\min} + V_{CrB\max} \end{aligned} \tag{2.37}$$

If we solve (2.11) for V_C and substitute it into (2.37), we get (2.38).

$$\frac{1}{2}(V_{out} + V_{in}) = V_{CrA\min} + V_{CrB\max} \tag{2.38}$$

Dividing (2.38) by V_{in} will give us (2.39).

$$\frac{1}{2}(M+1) = M_{CrA\min} + M_{CrB\max} \tag{2.39}$$

Finally, we can substitute in (2.31) and solve for $M_{CrB\max}$ to get the voltage stress of C_{rB}, (2.40).

$$M_{CrB\max} = \frac{1}{m}M + 1 \tag{2.40}$$

Examination of the conducting states reveals that the voltage stress of both MOSFETs is V_{in}. In addition, the voltage stress of all diodes is V_C. V_C can be described in a normalized form as a function of M as shown in (2.41).

$$\begin{aligned} M_C &= V_C/V_{in} \\ &= \frac{1}{2}(M-1) \end{aligned} \tag{2.41}$$

To find the RMS current of MOSFET S_A, we can describe the drain-to-source current i_{SA} in terms of the resonant inductor current as (2.42).

$$i_{SA}(t) = \begin{cases} 0 & \text{if } t \in \text{State 1} \\ -i_{Lr}(t) & \text{if } t \in \text{State 2} \\ -i_{Lr}(t) & \text{if } t \in \text{State 3} \end{cases} \tag{2.42}$$

After executing the RMS calculations, the normalized RMS current through S_A can be described as (2.43).

$$J_{SA\text{rms}} = \frac{1}{2}\Bigg[F\Bigg(\frac{1}{\pi}\Big[1 - M_{CrA\text{min}}\Big]\sqrt{1-h^2}\Big[(M_{CrA\text{max}} - 1) + h(1 - M_{CrA\text{min}})\Big] + \Big[M_{CrA\text{max}} - M_C\Big]^2\Bigg)\Bigg]^{1/2} \tag{2.43}$$

The drain-to-source current of S_B, i_{SB}, can also be described in terms of the resonant inductor current as (2.44).

$$i_{SB}(t) = \begin{cases} i_{Lr}(t) & \text{if } t \in \text{State 1} \\ 0 & \text{if } t \in \text{State 2} \\ 0 & \text{if } t \in \text{State 3} \end{cases} \tag{2.44}$$

The normalized RMS current through S_B is calculated as (2.45).

$$J_{SB\text{rms}} = \frac{\sqrt{\pi}}{2\pi}(1 - M_{CrA\text{min}})\left[2\pi d - Fh\sqrt{1-h^2}\right]^{1/2} \tag{2.45}$$

The current through diode D_{1A}, i_{D1A}, can be described in terms of the current through C_{rA}, i_{CrA}, as shown in (2.46).

$$i_{D1A}(t) = \begin{cases} 0 & \text{if } t \in \text{State 1} \\ 0 & \text{if } t \in \text{State 2} \\ -i_{CrA}(t) & \text{if } t \in \text{State 3} \end{cases} \tag{2.46}$$

The normalized RMS current through D_{1A} is calculated as (2.47). Calculation of the RMS current through D_{0B} yields the same equation.

$$J_{D1A/D0B\text{rms}} = \frac{1}{4}(M_{CrA\text{max}} - M_C)\sqrt{F} \tag{2.47}$$

The current through diode D_{0A}, i_{D0A}, can also be described in terms of i_{CrA} as shown in (2.48).

$$i_{D0A}(t) = \begin{cases} i_{CrA}(t) & \text{if } t \in \text{State 1} \\ i_{CrA}(t) & \text{if } t \in \text{State 2} \\ 0 & \text{if } t \in \text{State 3} \end{cases} \tag{2.48}$$

The normalized RMS current through D_{0A} is calculated as (2.49). Calculation of the RMS current through D_{1B} yields the same equation.

$$J_{D0A/D1B\text{rms}} = \frac{\sqrt{\pi}}{4\pi}\Bigg[(M_{CrA\text{min}}-1)^2\Big(2\pi d - Fh\sqrt{1-h^2}\Big) + F\Big[1-M_{CrA\text{min}}\Big]\sqrt{1-h^2}\Big[(M_{CrA\text{max}}-1)+h(1-M_{CrA\text{min}})\Big]\Bigg]^{1/2} \tag{2.49}$$

Table 2.1 compiles the normalized voltage and current stresses of the most important components. The actual voltage stresses can be found by multiplying the normalized value by V_{in}. The actual current stresses can be found by multiplying the normalized value by I_b which was described as (2.34).

Table 2.1: Normalized Voltage and Current Stresses

Component	Voltage Stress	Current Stress
L_r	N/A	(2.36)
C_{rA}	(2.32)	N/A
C_{rB}	(2.40)	N/A
S_A	1	(2.43)
S_B	1	(2.45)
$D_{1A/0B}$	(2.41)	(2.47)
$D_{0A/1B}$	(2.41)	(2.49)

The component stress waveforms are calculated and visualized according to the specifications of the prototype in Fig. 3.2 in Chapter 3.

Chapter 3

Open-Loop Design of Full-Range 3X RTBSC-A Converter

This is an in-depth look into the design of the first prototype 3X RTBSC-A converter. First, the design of the power converter itself and the chosen components are analyzed. Second, an open-loop simulation in LTspice is executed and observed. This simulation will give us further analysis into the difference between Switching Technique A and 50% duty cycle switching. Third, design of the control circuit and the driver circuit is analyzed. This includes tables of the components chosen for these circuits. Last, an open-loop experiment is executed and the results are reviewed. This will include a comparison of the prototype's voltage gain with the ideal voltage gain from the formula, and a confirmation of ZVS in the converter.

3.1 Prototype Converter Design

A prototype 3X RTBSC-A converter was designed and fabricated (as shown in Fig. 3.1) with the specifications shown in Table 3.1.

A relatively high resonant frequency of 100 kHz was chosen to keep the resonant tank components small and minimize power losses. A small resonant inductance L_r means less leakage inductance, less winding resistance, and less winding capacitance.

The MOSFETs and diodes were carefully selected to handle the voltage and current stress observed in the simulations, while also having low parasitic capacitances, low ON-resistances, and low forward voltages to maintain a high efficiency.

Charge-bank capacitors $C_{1A/1B}$ were selected to be larger than the resonant capacitors $C_{rA/rB}$. Input and output capacitors $C_{in/out}$ were selected to be much larger to filter out any voltage ripple on the input and output sides.

Input inductance L_{in} was carefully selected from simulations to provide sufficient inductance in keeping the input current as close to DC as possible while also having quick response to changes in f_s.

Table 3.1: Specifications of the prototype 3X RTBSC-A converter.

V_{in}	30 V	R_L	50 Ω	$C_{rA/rB}$	2.2 μF (film capacitors)
L_{in}	5 μH	f_r	100 kHz	Power Level	$< 162\ W$
$C_{in/out}$	100 μF	$S_{A/B}$	TK30E06N1	L_r	0.57 μH
$C_{1A/1B}$	10 μF	$D_{1A/0A/0B/1B}$	10TQ045	V_{out}	$< 90\ V$

To make sure the right components were selected, the voltage and current stresses were calculated according to the specifications given in Table 3.1. These stresses were calculated using the equations given in Chapter 2. Fig. 3.2 shows the stresses plotted against F. With

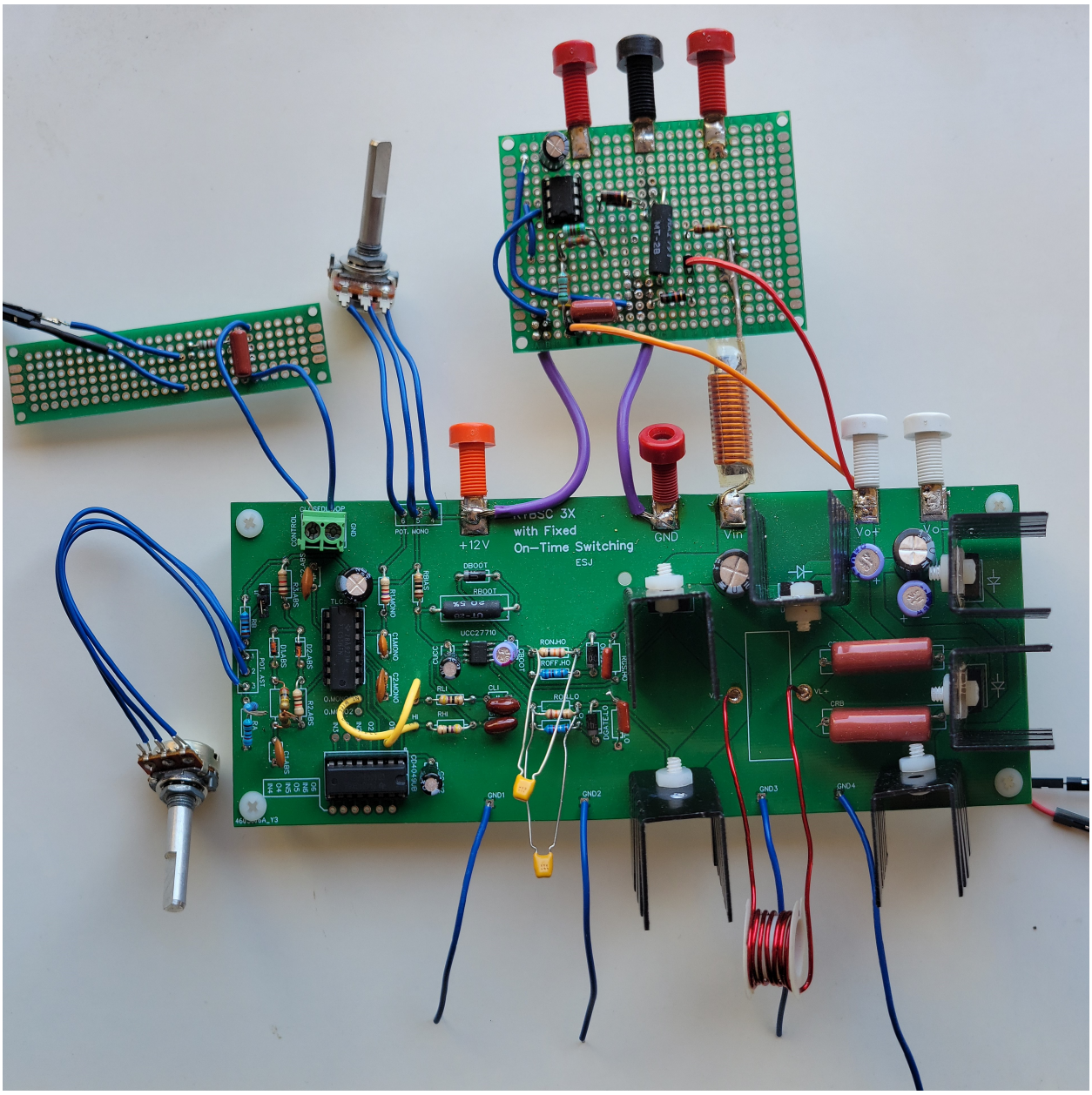


Figure 3.1: Fabricated prototype 3X RTBSC-A converter.

these stresses, we can make sure our components were selected with a large enough working voltage or current.

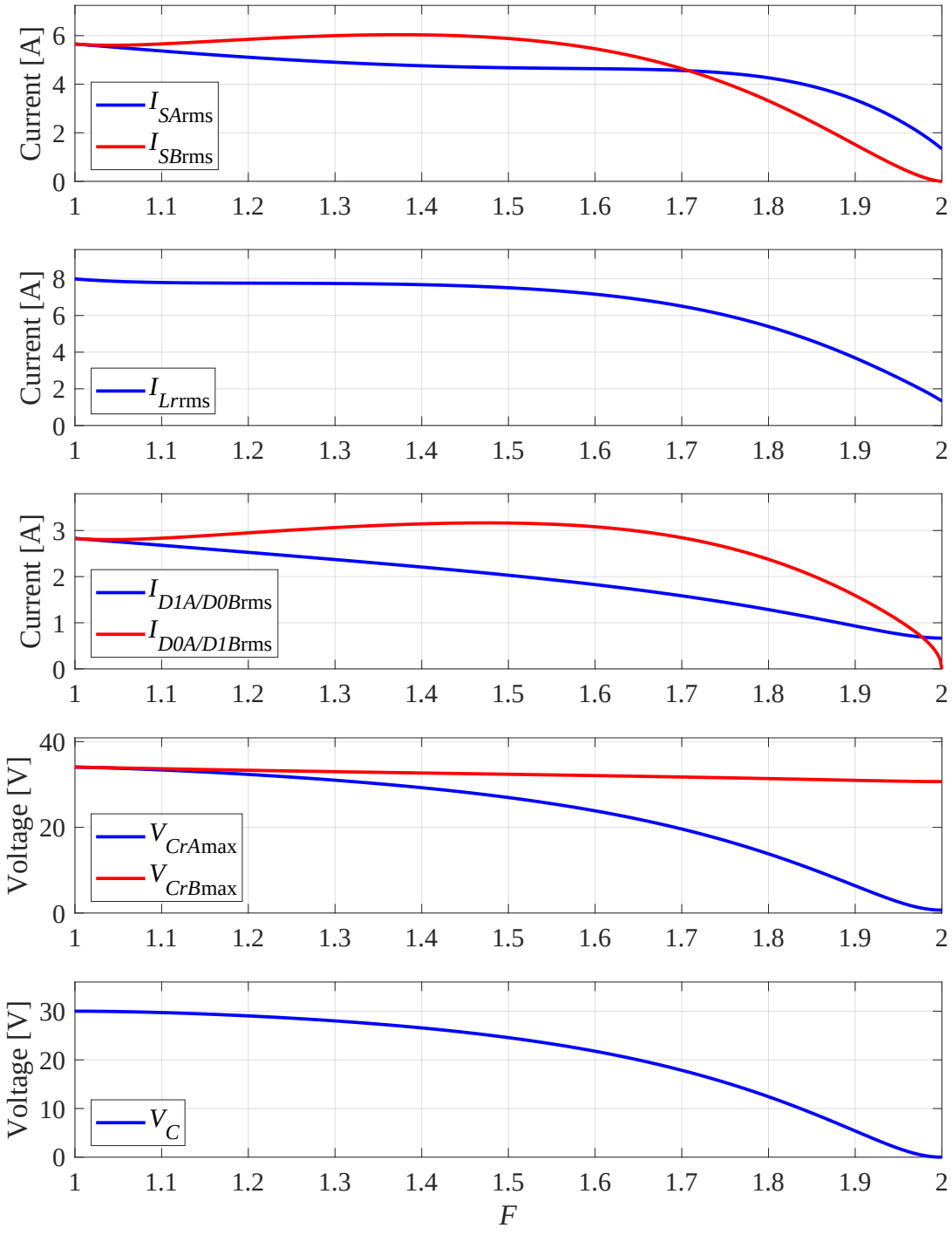


Figure 3.2: Component stresses according to the specifications given in Table 3.1.

3.2 Open-Loop Simulation Results

A frequency-sweep simulation was performed in LTspice of the 3X RTBSC-A converter as shown in Fig. 3.3. The purpose of this simulation was to compare the voltage gain range of Switching Technique A and 50% duty cycle switching.

The simulation was performed with most of the specifications shown in Table 3.1 with the exception of the MOSFETs and diodes. The simulation uses similar switches.

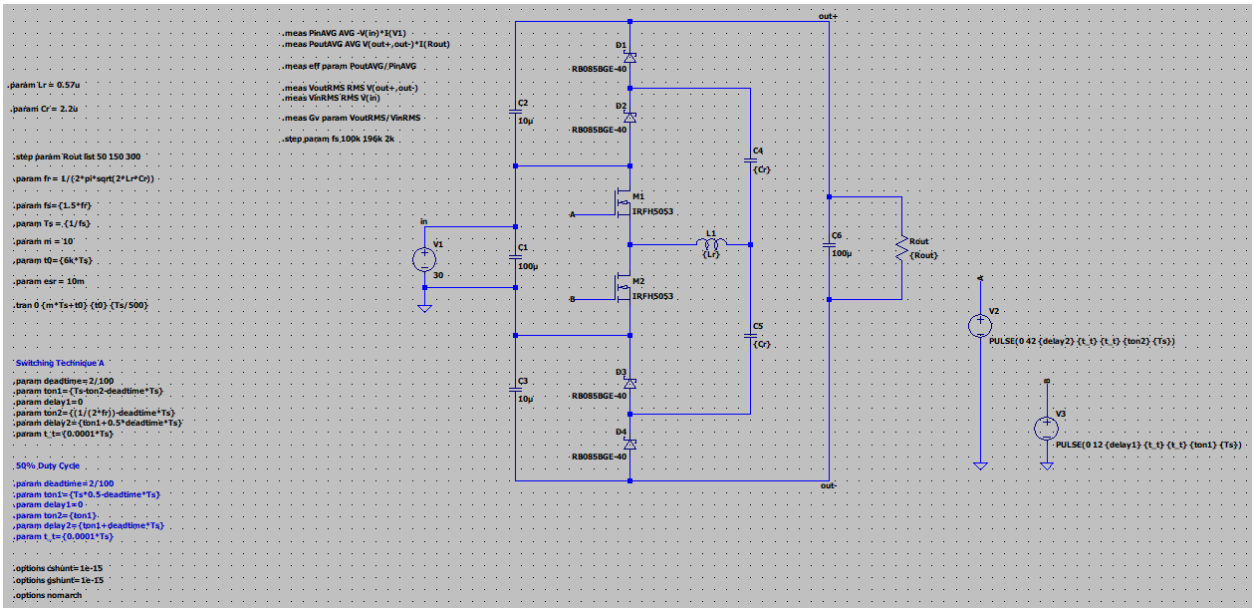


Figure 3.3: Topology of the LTspice simulation.

The simulation results are shown in Fig. 3.4. We can observe that a converter operating with Switching Technique A is able to achieve a nearly full voltage gain range. A converter operating with 50% duty cycle switching is barely able to deviate from triple voltage gain.

To give us some insight into why Switching Technique A gives us more voltage gain regulation, we can take a look at the steady-state waveforms from the simulations in Fig. 3.5.

As mentioned previously, we can observe that the charge bank capacitors are able to achieve a lower voltage with Switching Technique A because the resonant capacitors have different

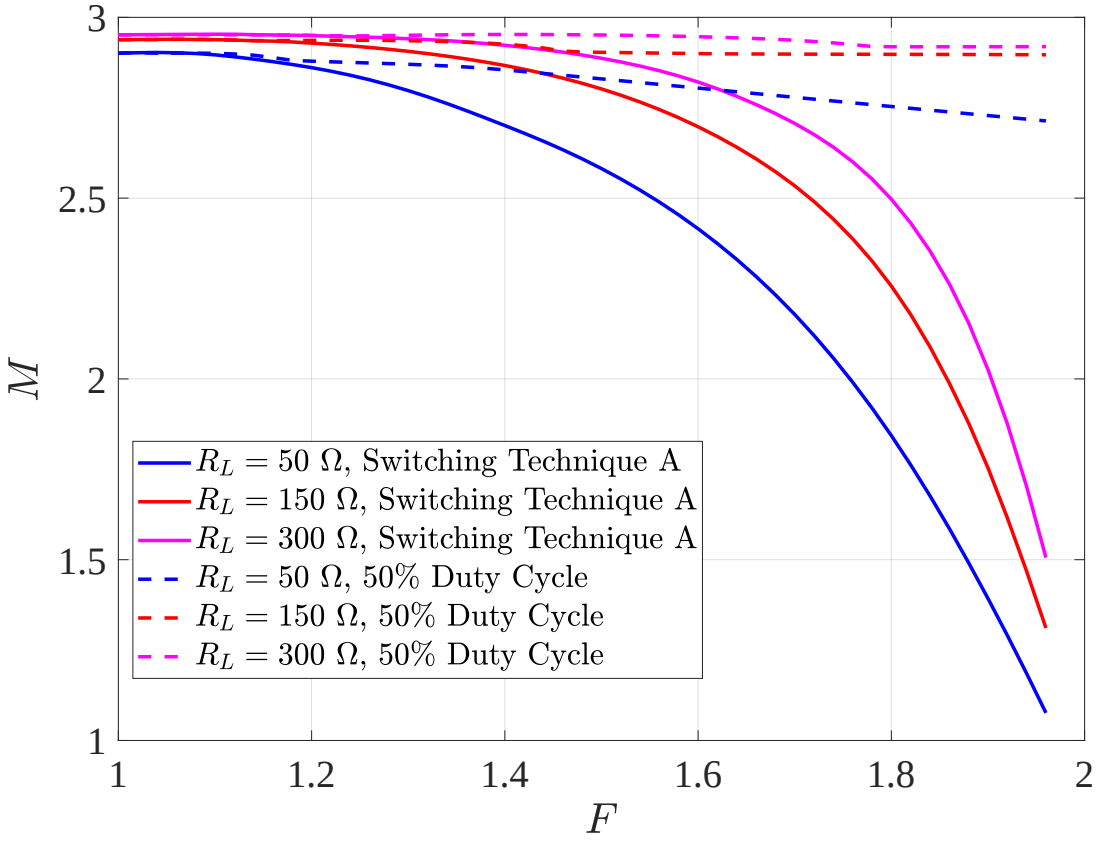


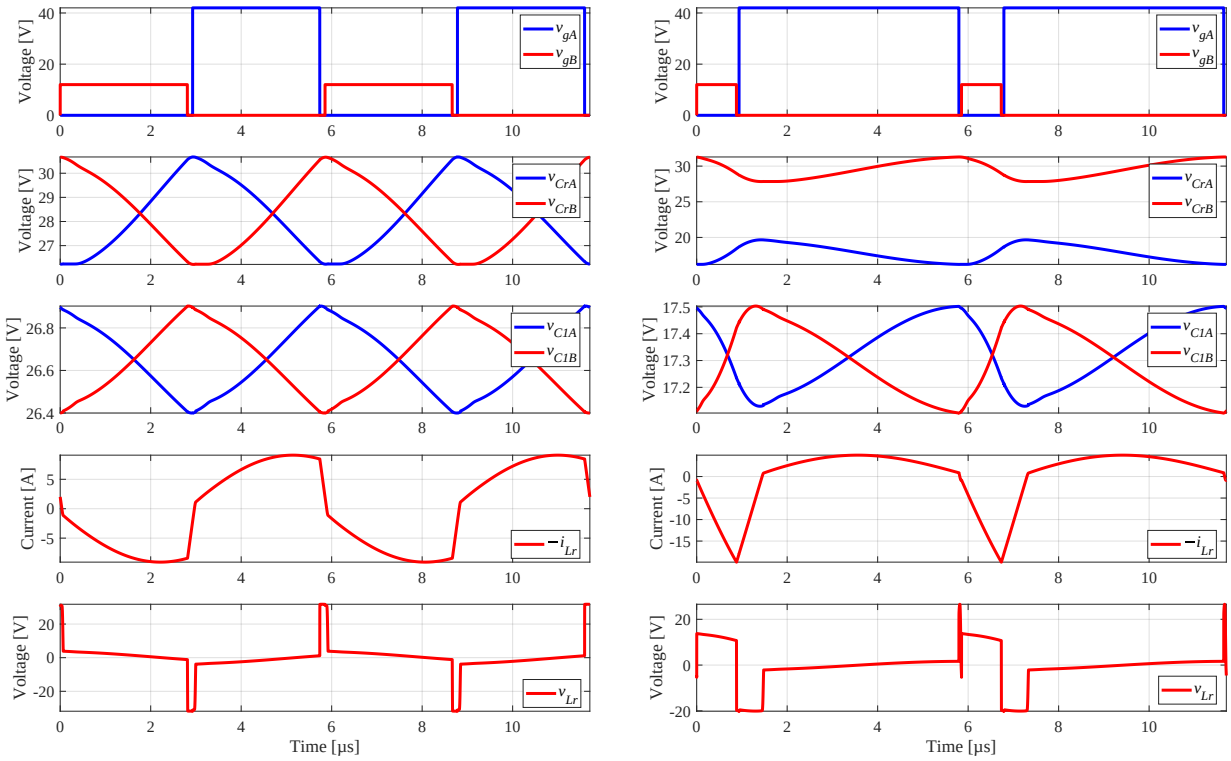
Figure 3.4: Voltage gain results of the LTspice simulation.

voltage levels and charge the charge bank capacitors at different rates. With 50% duty cycle switching, the resonant capacitors and the charge bank capacitors remain stuck at a voltage level near V_{in}.

3.3 Control Circuit Design

A control circuit to execute Switching Technique A was designed with the topology shown in Fig. 3.6.

Two series-cascaded 555 timer circuits are the main focus of the control circuit. The prototype actually uses a TLC556 IC which is simply two TLC555 ICs in one package. The first



(a) 50% duty cycle switching.

(b) Switching Technique A.

Figure 3.5: Comparison of steady-state waveforms at $F = 1.7$ with $R_L = 50\ \Omega$.

555 timer is operated in astable mode and the second one is operated in monostable mode.

The astable 555 timer is used to set the frequency of the switching signals. Its frequency is controlled by adjusting the voltage of the control pin (V_{ctrl}). The frequency can be adjusted using one of two methods (represented by the SPDT switch).

The first method is by manually adjusting a potentiometer ($R_{pot,OL}$) in a voltage divider network. The second method is by passing a PWM signal with a variable duty cycle through a low-pass filter (LPF) consisting of R_{PWM} and C_{PWM}. The PWM signal will be filtered into a distinct analog DC voltage, and will be able to adjust the frequency of the astable 555 timer. For the MPPT experiment, this PWM signal will come from GPIO pin 00 of the microcontroller. A visual respresentation of the relationship between V_{ctrl} and the switching frequency is shown in Fig. 3.7. In addition, the OFF-time of the astable 555 timer output

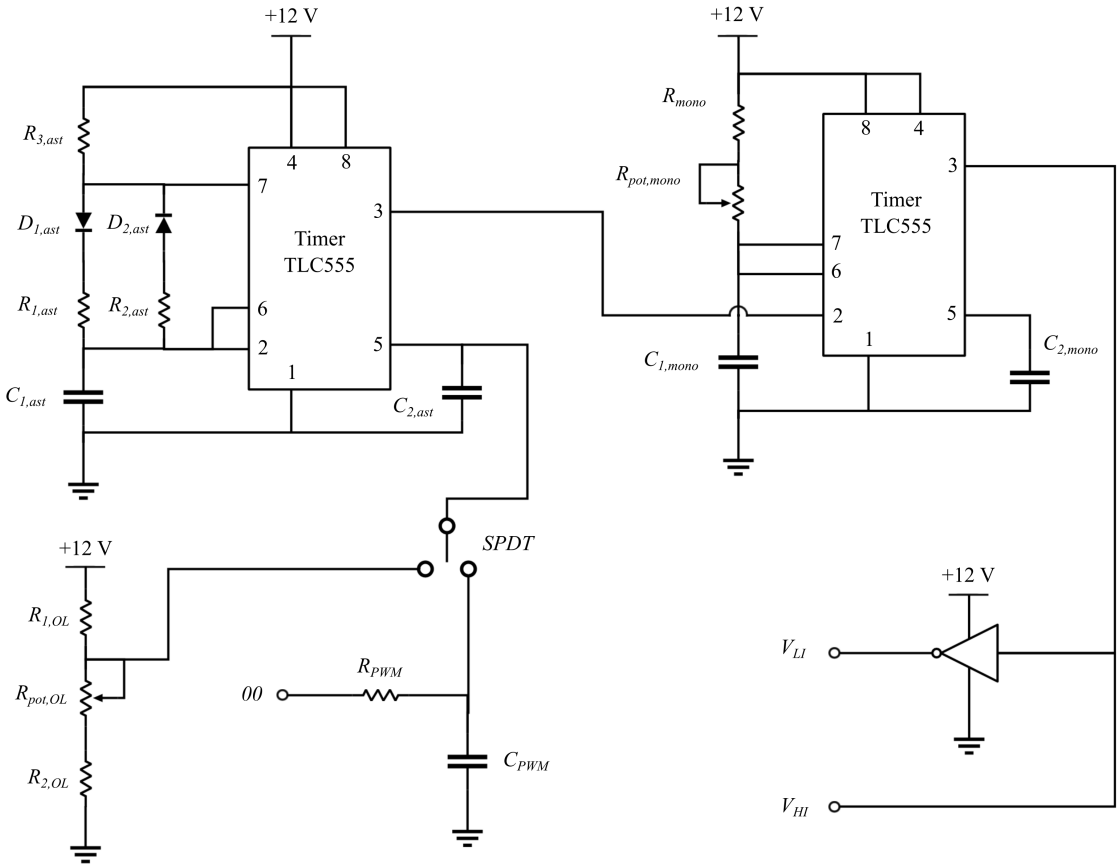


Figure 3.6: Topology of the control circuit.

is set to be very small compared to the ON-time. This is so the ON-time of the output of the monostable 555 timer doesn't extend any further passed its set value.

The output of the astable 555 timer is fed into the input of the monostable 555 timer. The purpose of this timer is to set the fixed ON-time of Switching Technique A. In our case, the resonant frequency is 100 kHz. So, the fixed ON-time of Switching Technique A must be 5 µs according to (2.5). Another potentiometer ($R_{pot,mono}$) is added to fine-tune the ON-time of the monostable 555 timer.

The output of the monostable 555 timer is a signal with a fixed ON-time of 5 µs that can be fine-tuned with $R_{pot,mono}$, and a frequency between 100 kHz and 200 kHz that can be adjusted with $R_{pot,OL}$ or with a PWM signal.

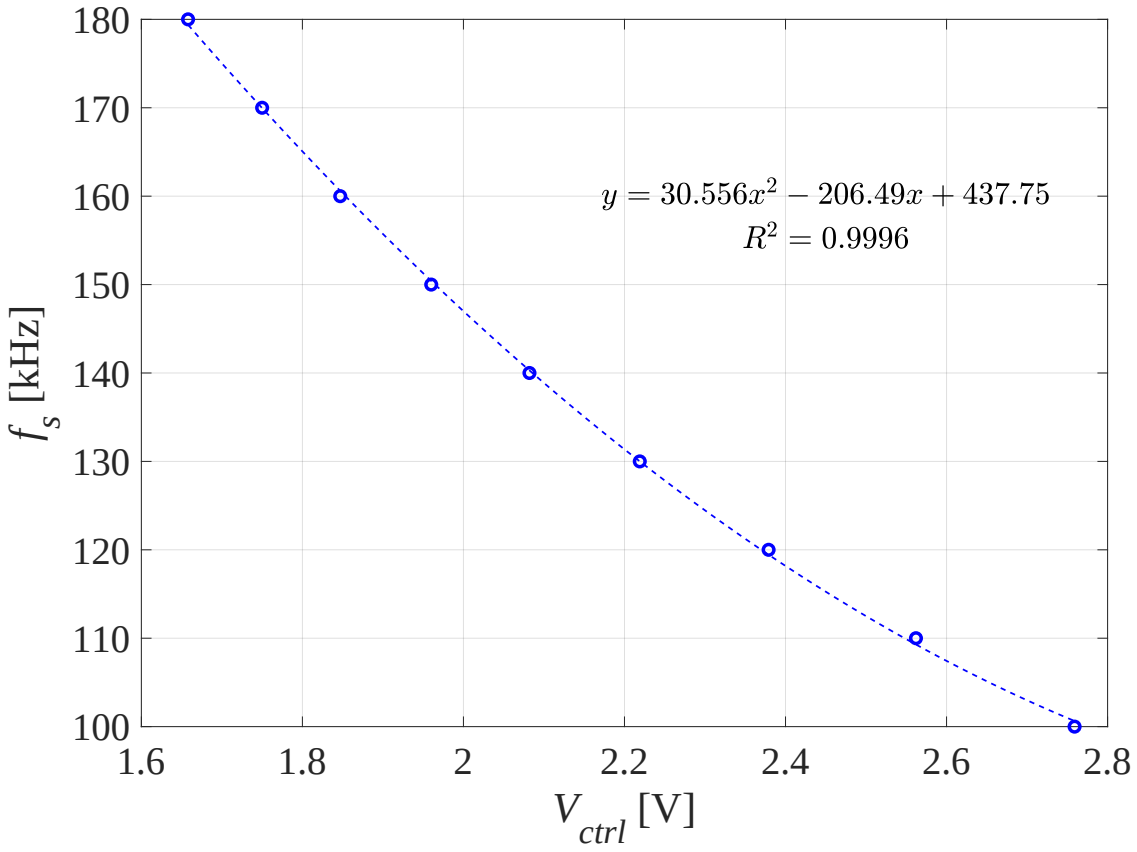


Figure 3.7: Relationship between the control voltage and the switching frequency.

Finally, the output of the monostable 555 timer is fed into a logic inverter to produce the complementary signal needed for both MOSFETs. Signals V_{LI} and V_{HI} are the input signals of the driver circuit. The slight overlap caused by the propagation delay of the logic inverter will be converted into dead-time by the driver IC.

The component values chosen for the prototype are shown in Table 3.2.

3.4 Driver Circuit Design

A driver circuit to quickly turn the MOSFETs ON and OFF was implemented in the prototype. Since the converter relies on a half bridge switching network, a bootstrap driver IC

Table 3.2: Component Values of the Control Circuit.

$R_{1,ast}$	400 kΩ	$C_{1,ast}$	100 pF	Timer IC	TLC556	$R_{1,OL}$	6.8 kΩ
$R_{2,ast}$	1 kΩ	R_{mono}	2.7 kΩ	Logic Inverter	CD4049UB	$R_{pot,OL}$	1 kΩ
$R_{3,ast}$	1 kΩ	$C_{1,mono}$	1.5 nF	$D_{1,ast/2,ast}$	1N4448	$R_{2,OL}$	950 Ω
R_{PWM}	5.1 kΩ	C_{PWM}	100 nF	$C_{2,ast/2,mono}$	10 nF	$R_{pot,mono}$	1 kΩ

was used to reliably turn the floating MOSFET ON and OFF. The topology of the driver circuit is shown in Fig. 3.8.

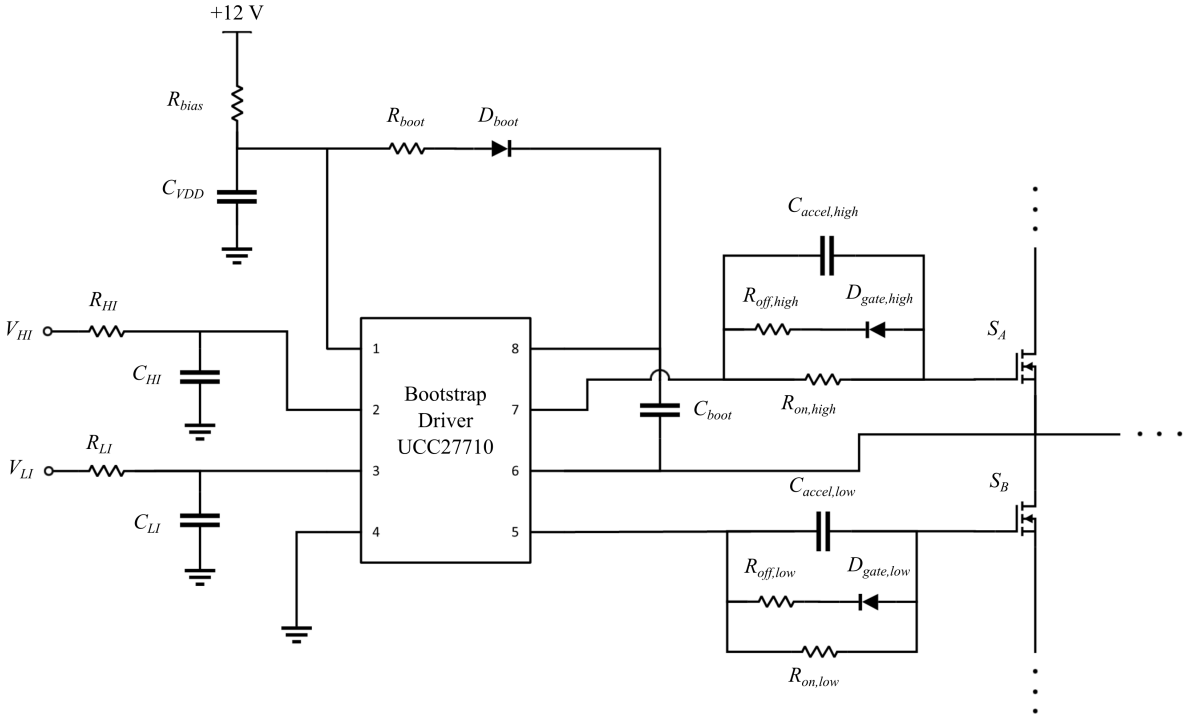


Figure 3.8: Topology of the driver circuit.

The topology of the driver circuit was derived from the example circuit given in the datasheet of the bootstrap driver, the UCC27710. The compiled components values selected are shown in Table 3.3.

$V_{HI/LI}$ are the signals leaving the control circuit and entering the driver circuit. Both signals pass through a LP filter to filter out any noise before entering the input pins of the IC.

The resistor R_{bias} is recommended to make the V_{DD} (pin 1) ramp-up time very long to minimize rising at the output pins (pins 5 and 7).

The capacitor C_{boot} was chosen to have more than enough energy to drive the floating MOSFET. The V_{DD} capacitor C_{VDD} was chosen to be at least 10 times larger than C_{boot} so there is minimal voltage drop on the V_{DD} capacitor when charging the boot capacitor.

Resistor R_{boot} is selected to limit the current in D_{boot} and avoid the same phenomenon mentioned when selecting R_{bias}.

The diode D_{boot} is necessary to prevent charge from being taken away from C_{boot}. A diode with fast recovery time, low forward voltage, and low junction capacitance was recommended.

The resistors $R_{on,high/on,low}$ and $R_{off,high/off,low}$ are implemented for three main reasons: to limit ringing caused by parasitic components and high voltage/current switching, to fine-tune gate drive strength to optimize switching loss, and to reduce EMI.

In addition, capacitors $C_{accel,high/accel,low}$ were added to further increase the switching speed of the MOSFETs.

Table 3.3: Component Values of the Driver Circuit.

$R_{HI/LI}$	47 Ω	R_{bias}	10 Ω	$R_{on,high/on,low}$	13 Ω
$C_{HI/LI}$	47 pF	C_{VDD}	10 µF	$R_{off,high/off,low}$	6.2 Ω
C_{boot}	0.47 µF	R_{boot}	2 Ω	$D_{gate,high/gate,low}$	UF4005
Bootstrap Driver	UCC27710	D_{boot}	UF4005	$C_{accel,high/accel,low}$	0.75 µF

3.5 Open-Loop Results

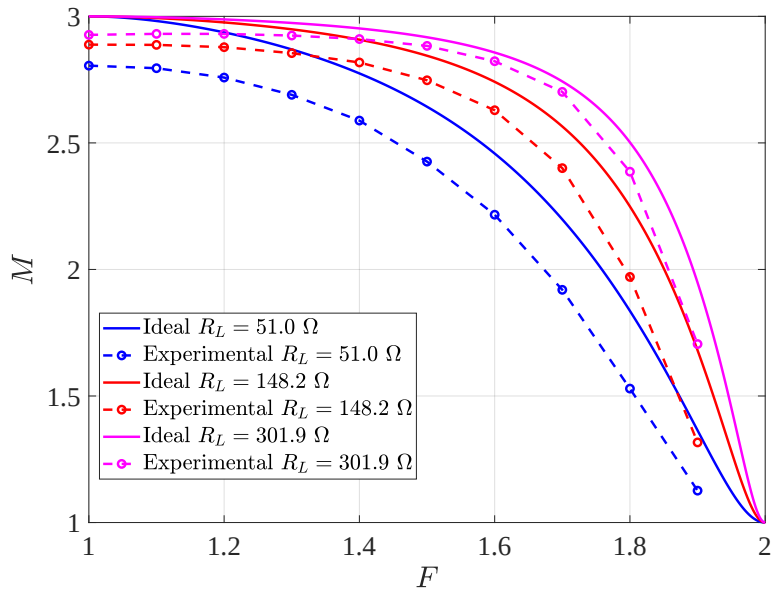
The performance of the open-loop 3X RTBSC-A converter was measured under three different load conditions: $R_L = 51\ \Omega$, $R_L = 148.2\ \Omega$, and $R_L = 301.9\ \Omega$. The theoretical values of Q are calculated to be 0.00706, 0.00243, and 0.00119 respectively.

A frequency sweep was performed with each load, and the voltage gain and efficiency were calculated from the measurements. The results are visualized in Fig. 3.9.

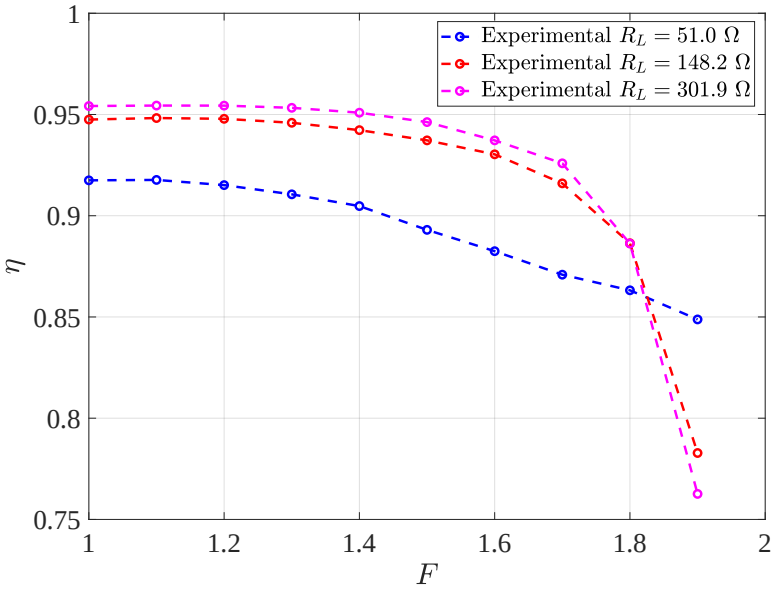
The experimental results of the voltage gain are compared with the ideal results of (2.33). We can observe that the experimental results follow the same shape as the ideal results, but are shifted slightly downwards compared to the ideal results. This is due to the combined power loss in all of our non-ideal components. We can also observe that our lightest load of $R_L = 301.9\ \Omega$ has the least difference between the experimental results and the ideal results.

As expected in many step-up converters, the efficiency is the highest when the converter is at, or close to, its largest voltage gain, and falls as the converter reaches unity voltage gain. We can observe that the difference in efficiency between loads $R_L = 148.2\ \Omega$ and $R_L = 301.9\ \Omega$ is very little, which indicates that this prototype converter has reached its peak efficiency when $R_L = 301.9\ \Omega$. The highest efficiency recorded for this load is at $F = 1.1$ where $\eta = 0.9544$.

We can examine the steady-state response of the inductor current in Fig. 3.10. The ZVS of the MOSFETs is very apparent when $F > 1$. We know the ZVS exists because $-i_{Lr}$ is negative when S_A (the higher MOSFET) turns ON and $-i_{Lr}$ is positive when S_B turns ON. The ZVS isn't apparent when $F = 1$ because $-i_{Lr}$ is near zero when either S_A or S_B turns ON.

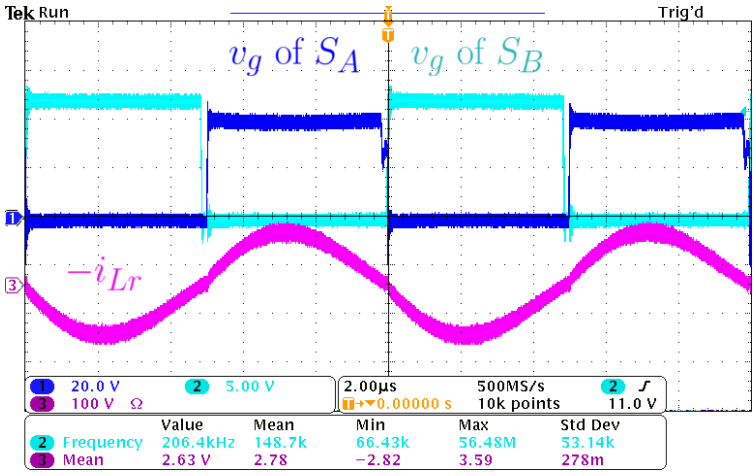


(a) Experimental voltage gain results of the prototype 3X RTBSC-A converter (dashed) compared with the ideal results from the gain formula (solid) for different loads.

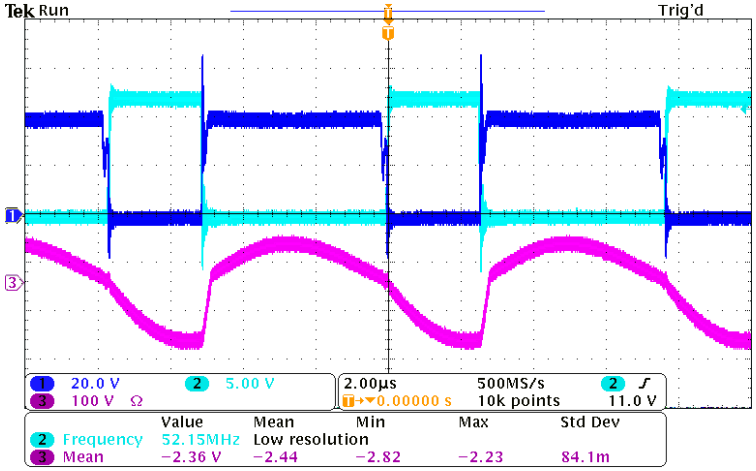


(b) Experimental efficiency results of the prototype 3X RTBSC-A converter for different loads.

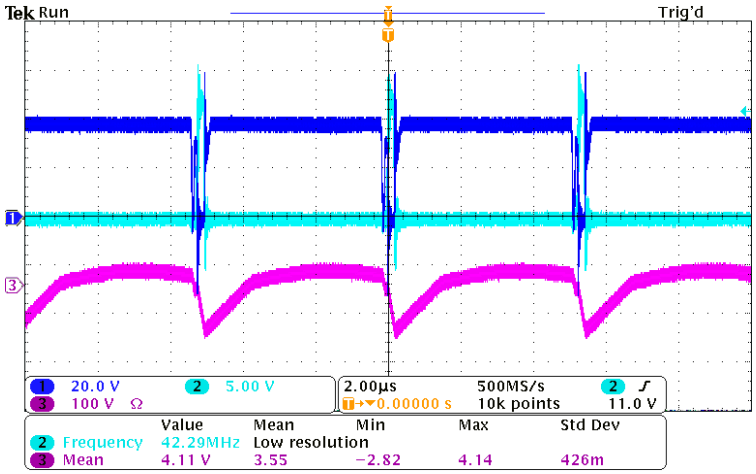
Figure 3.9: 3X RTBSC-A converter experimental results.



(a) $F = 1$.



(b) $F = 1.3$.



(c) $F = 1.9$.

Figure 3.10: Steady-state waveform shots showing proof of ZVS.

Chapter 4

Full-Range 3X RTBSC-A Converter for MPPT Applications

The MPPT experiment is described here. First, the design of a sensing circuit to feed data from the power converter to the microcontroller is described. Second, the operation of the MPPT system is reviewed. This includes review of: the entire system in the form of a block diagram, the MPPT algorithm, the microcontroller, and the solar panel used for the experiment. Third, a simulation of the MPPT experiment was executed in Simulink. The transient and steady-state results of the simulation are observed and analyzed. Last, the MPPT experiment is executed, and the results are observed and analyzed.

4.1 Sensing Circuit Design

In order to execute the MPPT experiment, a sensing circuit was designed to feed the microcontroller data about the voltage and current of the solar panel.

The topology of the sensing circuit is shown in Fig. 4.1. It is important to design the sensing

circuit appropriately so that the data fed to the microcontroller is between 0 to 3 V. The ADC pins on the microcontroller can only assign distinct digital values to analog voltages within that range. Table 4.1 shows the chosen component values for the prototype circuit.

Table 4.1: Component Values of the Sensing Circuit.

$R_{I\text{-}sens}$	30 mΩ	$R_{I\text{-}amp1}$	500 Ω
$R_{V\text{-}sens1}$	200 kΩ	$R_{I\text{-}amp2}$	6.8 kΩ
$R_{V\text{-}sens2}$	15 kΩ	$R_{I\text{-}LP}$	4.6 kΩ
Op-Amp	LM741	$C_{I\text{-}LP}$	100 nF

To read the voltage across the solar panel, a voltage divider circuit is implemented with resistors $R_{V\text{-}sens1}$ and $R_{V\text{-}sens2}$. The node between these resistors is connected to ADC pin $A0$ on the microcontroller.

To read the current through the solar panel, a small sensing resistor $R_{I\text{-}sens}$ is placed in series with the solar panel. Next, the voltage across $R_{I\text{-}sens}$ is amplified with an inverting op-amp circuit. Furthermore, the output of the op-amp circuit is fed into a LPF made up of resistor $R_{I\text{-}LP}$ and capacitor $C_{I\text{-}LP}$ to filter out noise from the signal. Finally, the output of the LPF is connected to ADC pin $A1$ on the microcontroller.

4.2 MPPT Operation

A block diagram of the complete MPPT experiment is shown in Fig. 4.2. The voltage and current of the solar panel, measured by the sensing circuit, is sent to the microcontroller. The microcontroller outputs a PWM signal to control the switching frequency of the converter through the control circuit. Finally, the switching signals are fed into a driver circuit to switch the MOSFETs of the 3X RTBSC-A converter.

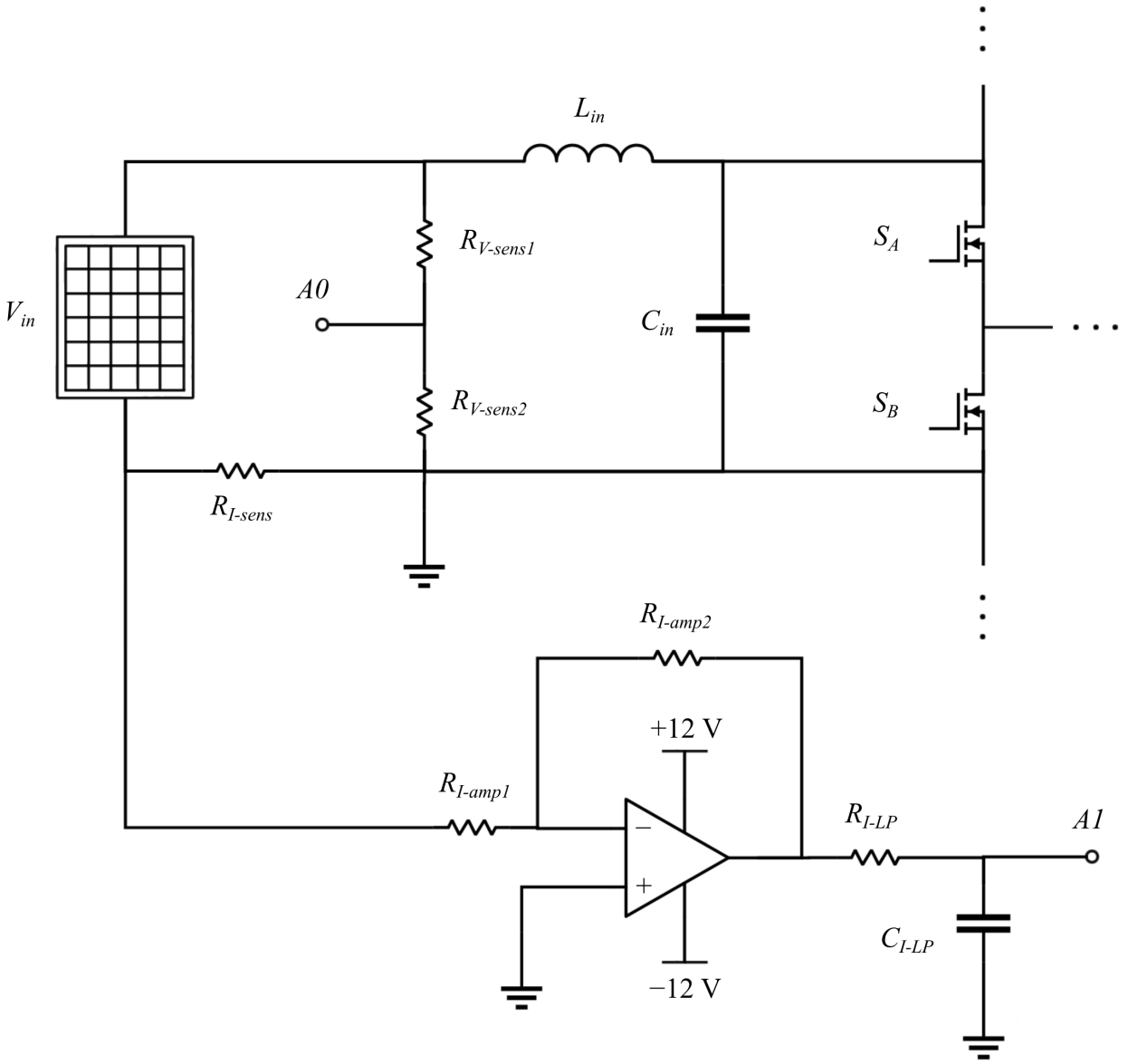


Figure 4.1: Topology of the sensing circuit.

The microcontroller used for the MPPT experiment is the Texas Instruments TMS320F28335 as shown in Fig. 4.3. This microcontroller outputs a 300 kHz PWM signal which is fed into the LPF mentioned in the control circuit. The output of this LPF is fed into the control pin (V_{ctrl}) of the astable 555 timer to adjust the frequency of the switching signals.

To modulate the voltage gain, a simple P&O MPPT algorithm was programmed. The

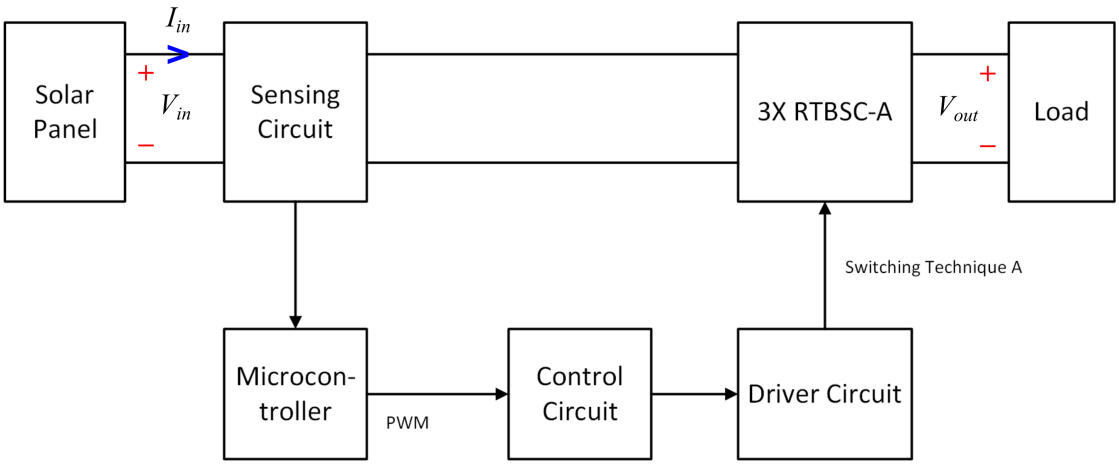


Figure 4.2: Block Diagram of the MPPT Experiment.

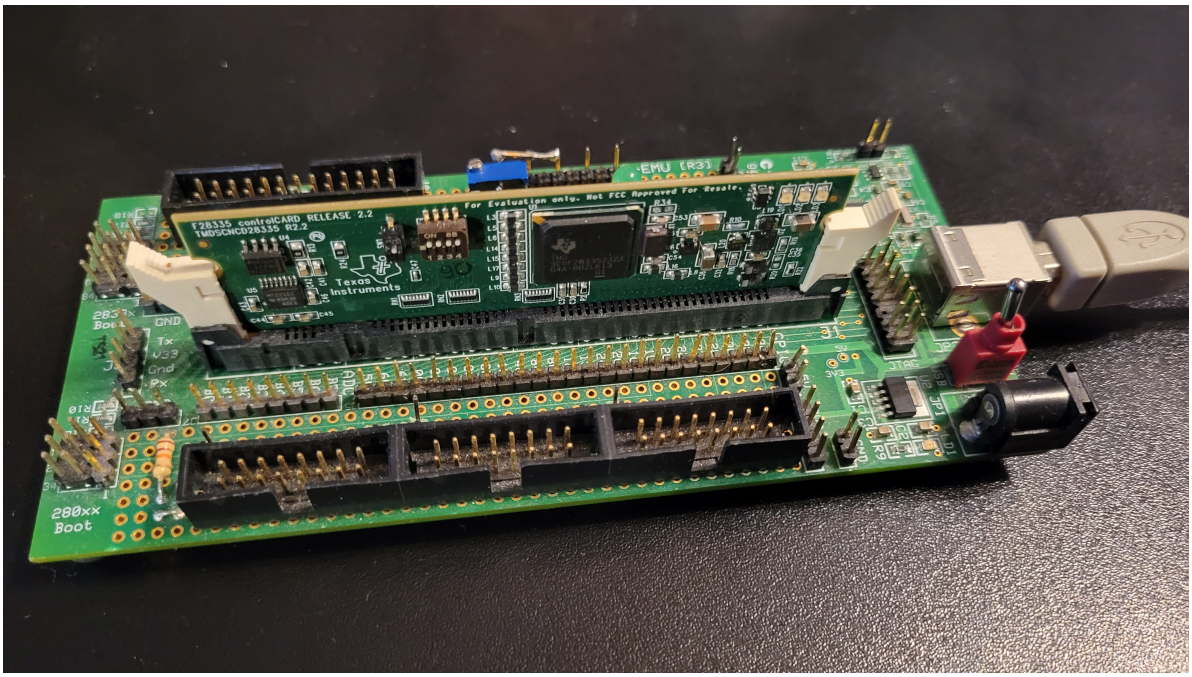


Figure 4.3: Photo of the microcontroller.

flowchart of this algorithm is shown in Fig. 4.4.

The algorithm samples the voltage and current of the solar panel using the sensing circuit and calculates the power. Next, the algorithm calculates the difference in power and the duty cycle of the PWM signal with the previous values from the last iteration. Depending

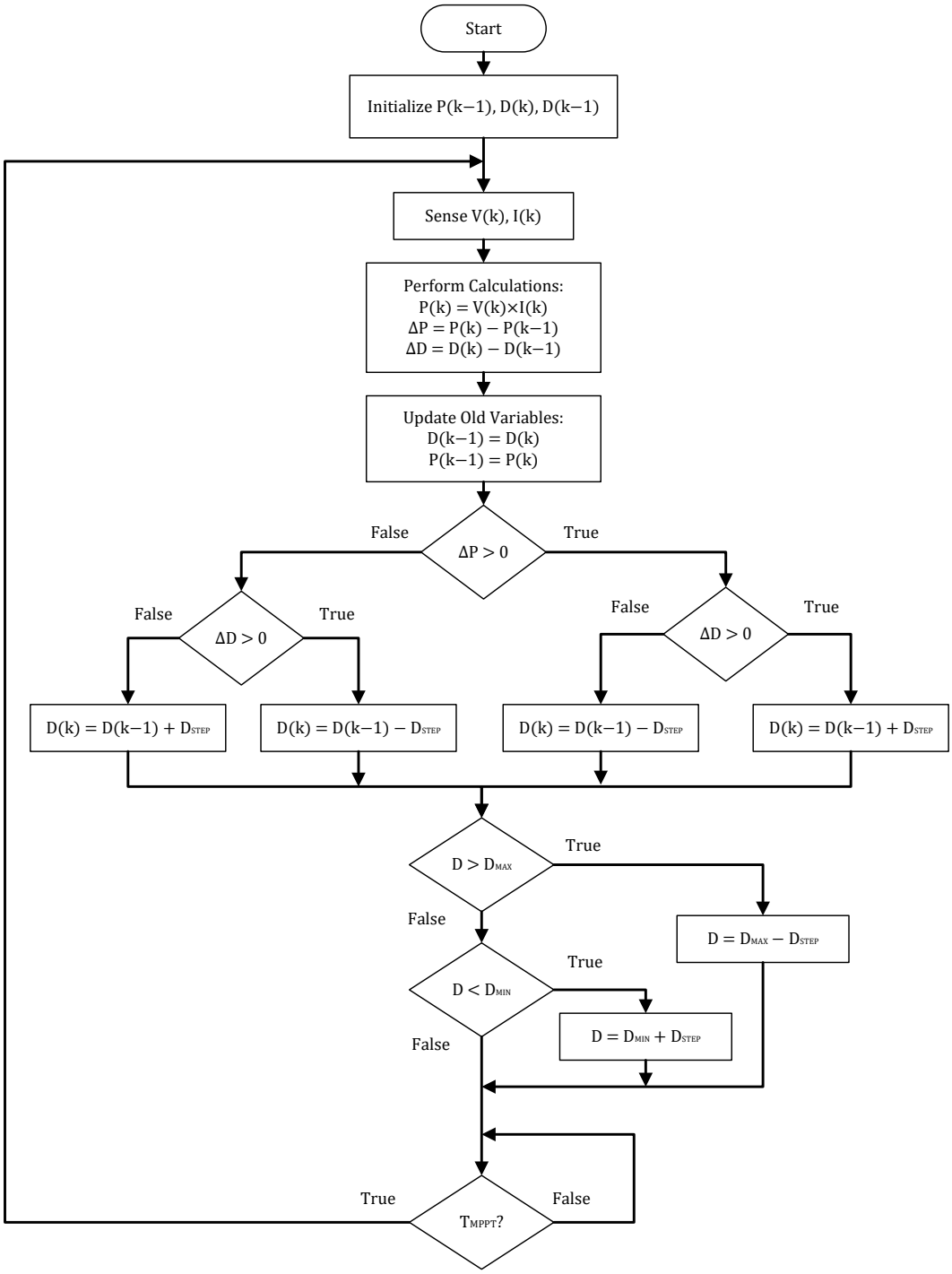


Figure 4.4: Flowchart of the MPPT algorithm.

on whether the power and duty cycle are increasing or decreasing, the algorithm moves the duty cycle in the right direction to increase the power of the solar panel. The algorithm repeats at a frequency of 50 Hz.

The solar panel used is the TDB125X125-72-P 180W shown in Fig. 4.5. Its specifications are shown in Table 4.2. The load is a 50 Ω resistor. It was actually measured to be exactly 49.8 Ω.

Figure 4.5: Photo of the solar panel used for the MPPT experiment.

Table 4.2: Specifications of the solar panel.

Parameter	**Variable**	**Value**
Maximum Power	P_{mp}	180 W
Voltage at Max. Power	V_{mp}	36.2 V
Current at Max. Power	I_{mp}	4.98 A
Open Circuit Voltage	V_{oc}	44.6 V
Short Circuit Current	I_{sc}	5.28 A

4.3 Simulation Results

A simulation of the MPPT function was performed in Simulink as shown in Fig. 4.6. A solar panel model with similar specifications to the one shown in Fig. 4.5 was used as the input. The voltage and current of the solar panel model would be sampled by a triggered subsystem at a rate of 100 Hz. The subsystem would then use a similar MPPT algorithm (compared to the one shown in Fig. 4.4) to calculate the next switching frequency for the simulation. Finally, a control system composed of Simulink blocks would execute Switching Technique A with the new switching frequency and switch the MOSFETs.

One major factor in constructing the MPPT algorithm is choosing the value of D_{STEP}. A relatively large D_{STEP} will react quickly to changes in the solar panel's input (such as irradiance or temperature) and will provide a fast response to the new power level. However, this large D_{STEP} will cause large power ripples when the system reaches steady state. A relatively small D_{STEP} will not react quickly to changes in the solar panel. However, it will provide small power ripples when the system reaches steady state.

The difference between this MPPT algorithm and the one shown in Fig. 4.4 is the additional feature of two different D_{STEP} values: a large value ($D_{\text{STEP,BIG}}$) and a small value ($D_{\text{STEP,SMALL}}$). $D_{\text{STEP,BIG}}$ is used to quickly get to new power levels whenever there is a change in the solar panel's irradiance or temperature. $D_{\text{STEP,SMALL}}$ is used to remain at steady state when changes to the solar panel are not detected. When ΔP is calculated in the algorithm, it is compared to a threshold value called P_{thres}. If $|\Delta P|$ is larger than P_{thres}, then a large change in power is detected and the algorithm will use $D_{\text{STEP,BIG}}$. This signifies that there was some change to the solar panel's input and the system needs to move to a different power level. If $|\Delta P|$ is smaller than P_{thres}, then a small change in power is detected and the algorithm will use $D_{\text{STEP,SMALL}}$. This signifies that there is barely any change to the solar panel's input and the system shouldn't move its current power level. With $D_{\text{STEP,BIG}}$

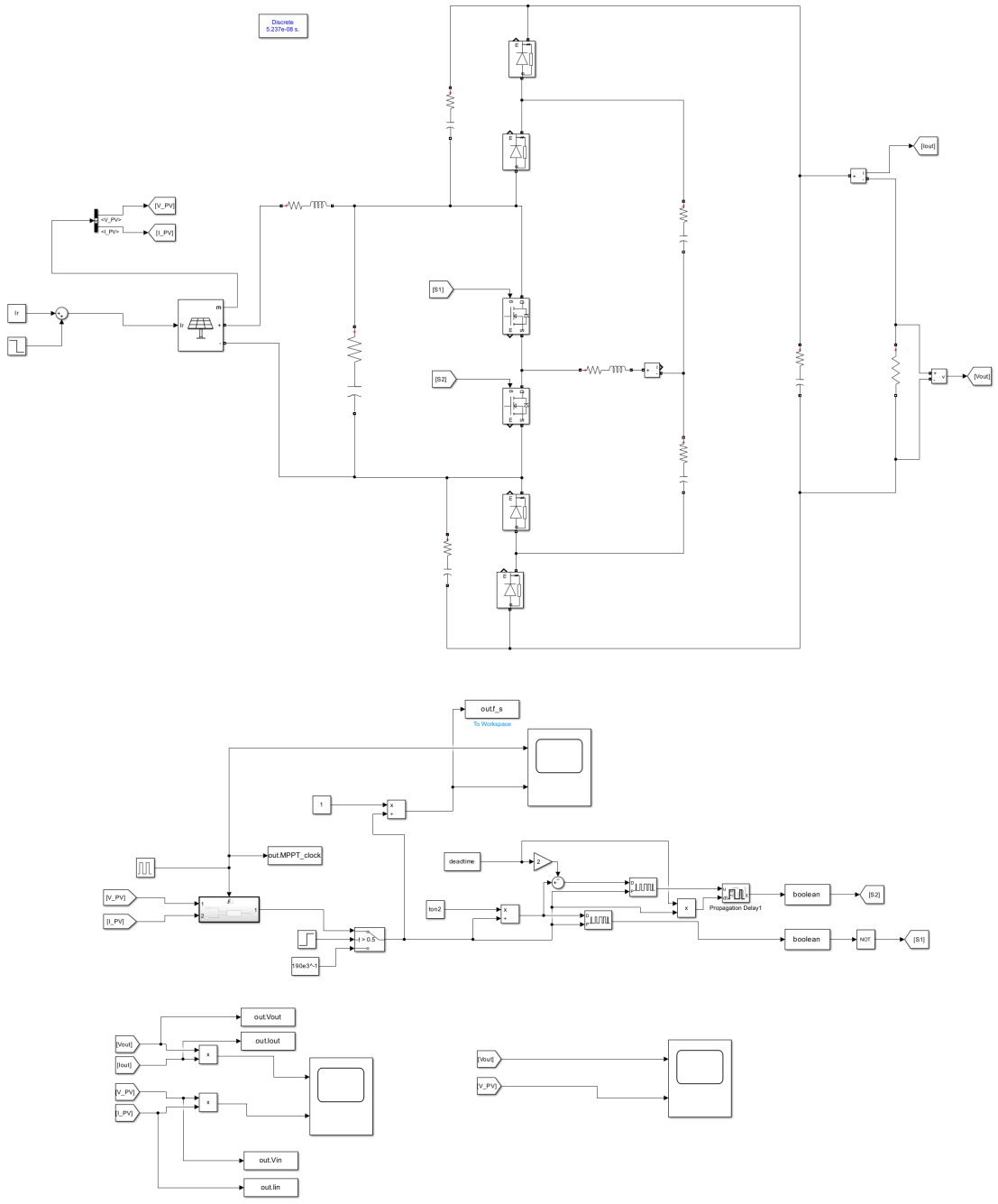


Figure 4.6: Simulation of the MPPT experiment in Simulink.

and $D_{\text{STEP,SMALL}}$, we get the fast response from a relatively large D_{STEP} and the small power ripples from a relatively small D_{STEP}.

To observe how the MPPT algorithm reacts to changes in the weather, the irradiance of the

solar panel model was initially appointed to 1000 W/m^2, but was set to instantly change to 600 W/m^2 at 0.305 seconds.

The transient and steady state waveforms of F, P_{in}, P_{out}, V_{in}, and V_{out} are shown in Fig. 4.7. As mentioned previously, two different values of D_{STEP} are used. $D_{\text{STEP,BIG}}$ is used during transient responses, such as at the beginning and when the irradiance of the solar panel changes at 0.305 seconds. $D_{\text{STEP,SMALL}}$ is used when the system approaches steady state to keep any power ripples small.

Table 4.3: Ripple values from the MPPT simulation.

Parameter	**1000 W/m^2**	**600 W/m^2**
Ripple of f_s	1.096%	1.193%
Ripple of P_{in}	0.536%	2.252%
Ripple of P_{out}	0.895%	2.809%
Ripple of V_{in}	2.378%	5.634%
Ripple of V_{out}	0.447%	1.403%

4.4 MPPT Results

The experiment took place on April 6, 2024 in Rancho Cucamonga, CA from 8:30 AM to 5:00 PM PST. Every 15 minutes, the input power of the solar panel and the output power of the load, under control of the MPPT algorithm, was recorded. Afterwards, the manual control of the converter (by adjusting $R_{pot,OL}$) would be used to adjust the switching frequency and find the approximate actual MPP. The results of the experiment are shown in Fig. 4.8.

We can observe that the input power of the solar panel closely follows the approximate actual MPP recorded. This indicates that the sensing circuits and algorithm were working together to find the MPP throughout the day.

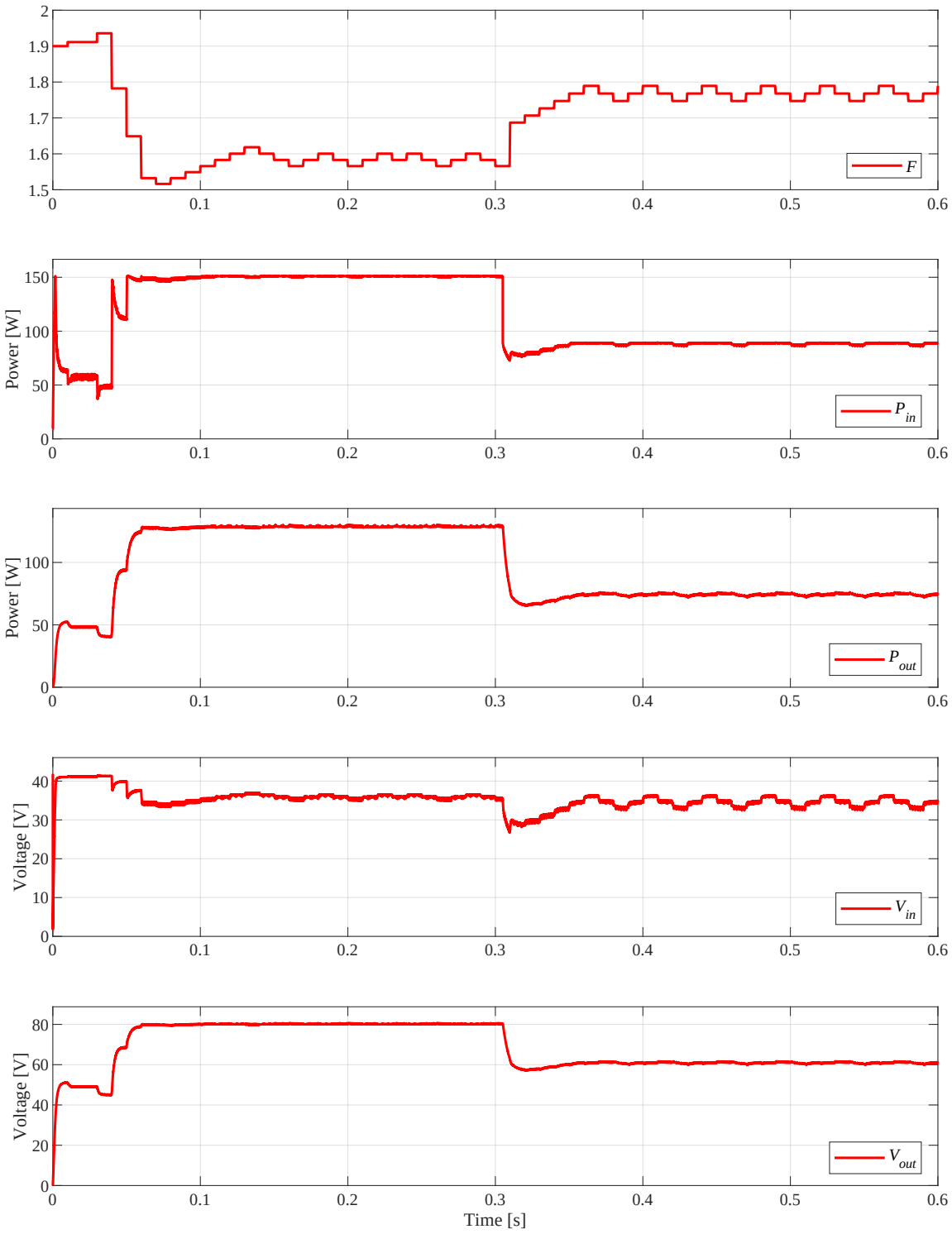
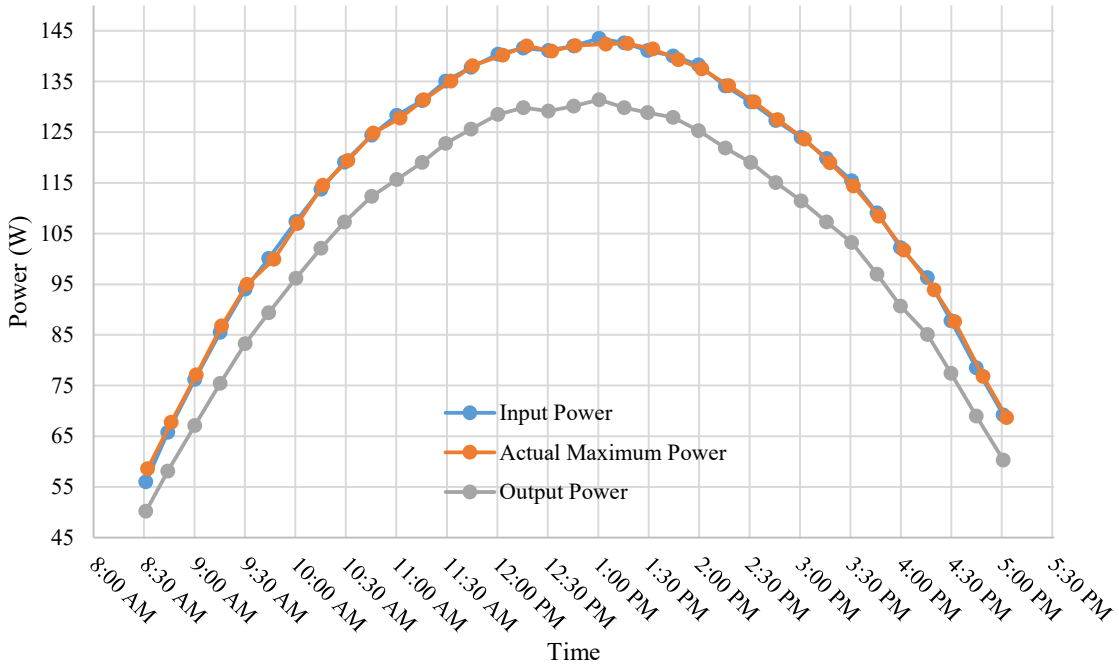
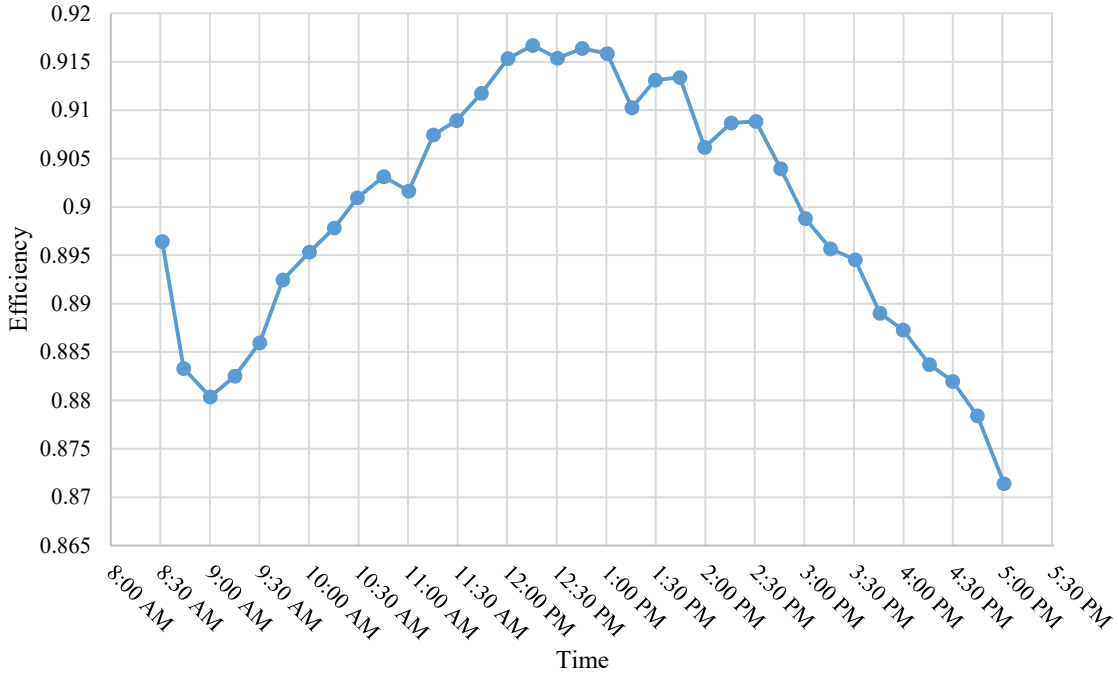


Figure 4.7: Transient and steady state waveforms from the MPPT simulation.



(a) The input power, actual maximum power, and the output power of the MPPT experiment.



(b) The calculated efficiency of the MPPT experiment.

Figure 4.8: MPPT experimental results.

Chapter 5

Summary and Discussion

The 3X RTBSC-A was employed to achieve full-range voltage gain regulation after the original 3X RTBSC proved unable to do so under relatively light loads. This achievement made MPPT of solar power possible. The work reported here has demonstrated that a SCC with the small addition of a resonant tank, operating under a fixed ON-time switching technique, is capable of achieving MPPT and retaining soft switching in the meantime. Since resonant SCCs use much smaller inductors compared to their PWM converter counterparts, the work here reveals that resonant SCCs under a fixed ON-time (or OFF-time) switching technique can replace PWM converters in this area of application.

After construction of the prototype 3X RTBSC-A, an open loop experiment was executed. We found that the voltage gain of the prototype circuit closely followed the voltage gain from the ideal formula as shown in Fig. 3.9 with a slight vertical difference due to power loss. For the 50 Ω load, the efficiency sweep was between 0.85 and 0.92. For the lighter loads, the efficiency remained above 0.9 during $1 < F < 1.8$ but quickly dropped under 0.9 when $F \geq 1.8$. The highest efficiency recorded was 0.9544 with the 301.9 Ω at $F = 1.1$. The higher efficiencies were achieved because of the converter's soft switching ability as proven

in Fig. 3.10.

There is still potential for higher efficiency. This is indicated in [2] in which the original 3X RTBSC was able to achieve efficiencies between 0.96 and 0.98 for its entire frequency sweep with a 322.8 Ω load. However, it's important to note that this load couldn't achieve full range voltage gain. A different load of 163.9 Ω was able to hold an efficiency above 0.92 at the higher end of its frequency range. In addition, the prototype for the 3X RTBSC used a smaller resonant frequency of 76 kHz. We can also find proof in [8] where a prototype 3X Ladder RSCC with $f_r = 100$ kHz had efficiences above 0.9 for its frequency sweep of $1 \leq F \leq 1.8$. This prototype converter achieved a peak efficiency of 0.9712.

One method to increase the efficiency would be to increase the converter's resonant frequency. This would make the converter's operating frequency range also increase. As a result, any conduction losses would be minimized and the efficiency would be greater than the prototype presented in this thesis. Furthermore, a higher resonant frequency means the resonant tank will use smaller components and the converter becomes smaller as well. On the downside, components for a new control and driver circuit would have to be found that can operate and handle such fast switching times. In addition, the past converters mentioned previously ([2],[8]) achieved high efficiencies with resonant frequencies equal to or lower than the prototype 3X RTBSC-A.

Another method to increase the efficiency would be to have designed and tested the converter with a higher input voltage. The prototype 3X RTBSC-A was designed for an input voltage of 30 V and a 50 Ω load for the MPPT experiments. The prototypes in [2] and [8] were designed for a 50 V input voltage. A higher input voltage would diminish the effect that the diodes' forward voltage has on the efficiency. As a result, the efficiency would increase with a higher input voltage. On the downside, the voltage and current stress of all of the converter's components would have to be examined to handle the higher power level created by a higher input voltage. This would include the width of the trace used in the PCB and

the thickness of the wire used to create the inductor.

Further optimization can be added to the MPPT algorithm. As shown in Fig. 3.7, the relationship between the control voltage and the switching frequency can be approximated with a 2nd-order polynomial. Because of this, a regular P&O algorithm would have slightly larger frequency steps at higher frequencies than at lower frequencies. To solve this, a function to "rectify" the "f_s vs. V_{ctrl}" relationship can be placed at the end of the MPPT algorithm. With this proposal, uniform frequency steps will be achieved along the entire frequency sweep for MPPT applications.

Bibliography

[1] B. Wu, S. Li, K. Ma Smedley, and S. Singer, "A family of two-switch boosting switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5413–5424, Oct. 2015. [Online]. Available: http://dx.doi.org/10.1109/TPEL.2014.2375311

[2] S. Li, Y. Zheng, B. Wu, and K. M. Smedley, "A family of resonant two-switch boosting switched-capacitor converter with zvs operation and a wide line regulation range," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 448–459, 2018. [Online]. Available: http://dx.doi.org/10.1109/TPEL.2017.2669841

[3] W. Xie and K. M. Smedley, "Seven switching techniques for the ladder resonant switched-capacitor converters with full-range voltage regulation," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 8, pp. 7897–7908, Aug. 2022. [Online]. Available: http://dx.doi.org/10.1109/TIE.2021.3106010

[4] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *IEEE Transactions on Power Electronics*, vol. 20, no. 4, pp. 963–973, 2005. [Online]. Available: http://dx.doi.org/10.1109/TPEL.2005.850975

[5] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits and Systems Magazine*, vol. 1, no. 3, pp. 37–42, 2001. [Online]. Available: http://dx.doi.org/10.1109/7384.963467

[6] C.-K. Cheung, S.-C. Tan, C. K. Tse, and A. Ioinovici, "On energy efficiency of switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 862–876, Feb. 2013. [Online]. Available: http://dx.doi.org/10.1109/TPEL.2012.2204903

[7] K. D. T. Ngo and R. Webster, "Steady-state analysis and design of a switched-capacitor dc-dc converter," in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 378–385 vol.1. [Online]. Available: http://dx.doi.org/10.1109/PESC.1992.254649

[8] W. Xie and K. Smedley, "Step-up ladder resonant switched-capacitor converter with full-range regulation," in *2020 IEEE PES/IAS PowerAfrica*, 2020, pp. 1–4. [Online]. Available: http://dx.doi.org/10.1109/PowerAfrica49420.2020.9219842

[9] ——, "General full-range regulation method for resonant switched-capacitor converters," in *2022 IEEE International Power Electronics and Application Conference and*

Exposition (PEAC), 2022, pp. 1025–1029. [Online]. Available: http://dx.doi.org/10.1109/PEAC56338.2022.9959494