Quadratic and linear optimization with analog circuits

by

Sergey Vichik

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Professor Francesco Borrelli, Chair
Professor Roberto Horowitz
Professor Ilan Adler

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Abstract

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In this work we propose and investigate a new method of solving quadratic and linear optimization problems using analog electrical circuits instead of digital computation.

We present the design of an analog circuit which solves Quadratic Programming (QP) or Linear Programming (LP) problems. In particular, the steady-state circuit voltages are the components of the QP (LP) optimal solution. The thesis shows how to construct the circuit and provides a proof of equivalence between the circuit and the QP (LP) problem.

We study the stability of the analog optimization circuit. The circuit dynamics are modeled as a switched affine system. A piece-wise quadratic Lyapunov function and the KYP lemma are used to derive the stability criterion. The stability criterion characterizes the range of critical circuit parameters for which the QP circuit is globally asymptotically stable.

The proposed method is used to build a printed circuit board (PCB) using programmable components to allow solution of various QP problems. The board supports implementation of an MPC controller for buck DC-DC converter. We conduct an experimental study to evaluate the performance of the analog optimization circuit.

We study the feasibility of very high speed implementation of the optimization circuit using Analog Very Large Scale Integration (AVLSI) technology. In AVLSI, all the required circuit components are built on top of a silicon substrate using advanced photo-lithographic technologies. AVLSI circuits are fast, small and cheap. Thus, AVLSI implementation is paramount to make the proposed technology commercially competitive.

We discuss the possible usage of the proposed method to make fast MPC controllers, image processors, communication decoders and analog co-processors. In fact, any application that requires a repeating solution of related optimization problems can benefit from this technology. Besides being faster than the digital computers, analog computers are more power efficient, may occupy smaller area on silicon and may be more resilient in harsh environments.

This dissertation is dedicated to my wife that bravely followed and supported me during those years, to my children — Adam and Eitan who may one day be inspired by this experience, and to my father whose ideas sowed a seed that started this work.

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Chapter 1

Introduction

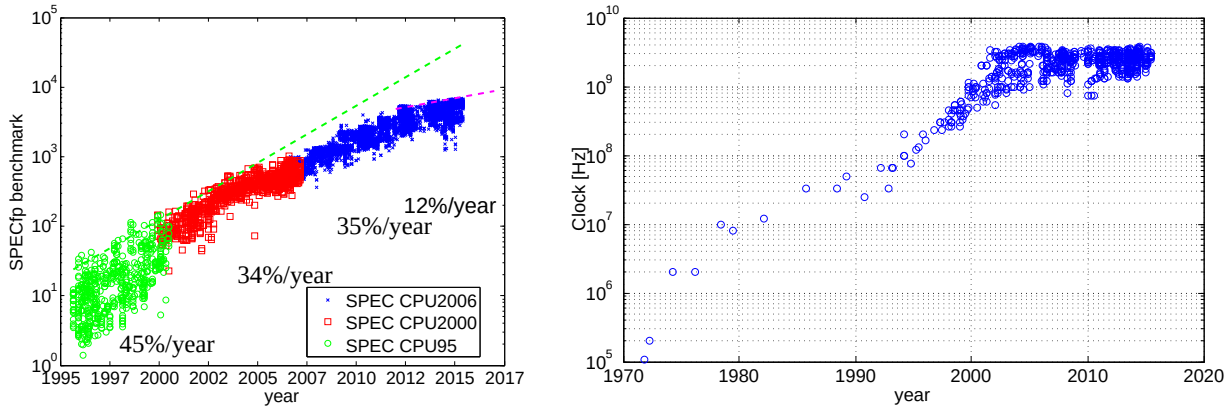
1.1 Motivation

The digital revolution has fundamentally changed technology, science and the everyday life. Our society got used to a steady and fast pace of improvement of the digital technology, embodied by the famous "Moore's law". However, there are multiple indications that this trend begins to level off. Novel and unconventional approaches will be needed to sustain the expected progress.

Standard benchmarks show the progress in computation speed. For instance, Fig. 1.1a presents the results of a floating point benchmark SPECfp from the last 20 years as published by Standard Performance Evaluation Corporation (SPEC) [86]. SPEC maintains historic and current performance results as reported by computer manufacturers. The benchmark result is the ratio between execution time of a baseline CPU to a tested CPU. Thus, benchmark result of 100 means that a tested CPU is 100 times faster then the baseline CPU. The benchmark had evolved through three versions (CPU1995, CPU2000 and CPU2006) with different baselines. In order to have smooth transition between the versions, we have scaled the results of CPU2000 and CPU2006 to match the baseline of CPU1995.

Fig. 1.1a shows a major slowdown in an improvement rate. The performance used to improve by annual 45% in 90's, but it is only 12% annually since 2012. The slowdown may be partially contributed to a stall in modern CPU clock frequency. Fig. 1.1b plots the CPU clock frequency of Intel processors from 1970 to 2015 [67, 85]. The figure clearly shows that the maximum clock speed (about 4 GHz) was reached in 2002 and remains constant ever since. Faster clock frequencies are unfeasible in practice because of an excessive heat that it produces. Therefore, the performance gain since 2002 as shown in Fig. 1.1a originates from other improvements in computer design, especially memory access optimization (cache, memory bandwidth) and deep instruction pipelines with branch prediction.

Nowadays, when the low–hanging fruits of digital computation appear to be picked, it is time to evaluate the alternatives, such as analog computation. Analog computers have radically better performance then digital computers for a certain class of computational



(a) (b)

Figure 1.1: (a) CPU floating point benchmarks from SPEC CPU95, CPU2000 and CPU2006 [86]. (b)Clock speed of Intel processors [67, 85].

problems. We demonstrate that when the analog computation is applied wisely, utilizing the progress in microelectronics, we can radically reduce computation latency comparing to digital processors. Moreover, analog computation yields lower power consumption and a smaller physical size.

The analog computers had been a formidable competitor to the digital computers at the beginning of the computer era, but were outpaced due to the rapid development of the digital computers. However, today thanks to the gigantic investment and progress made in microelectronics, we can build analog computers with the same tools utilized for the production of digital electronics. Therefore, analog computers can successfully compete in speed, price, power requirements and robustness with the digital computers.

Straightforward computation tasks can be done quickly with digital hardware, but as the complexity builds up, certain tasks demand long computing time. Digital computers are based on a sequential computation paradigm, which assumes that every computation is a sequence of operations. The sequential computation paradigm leads to iterative algorithms, which are major contributors to high latency and power consumption. Analog computers do not necessarily follow the sequential computation paradigm. For example, the optimization circuit proposed in this thesis reaches an equilibrium using a simultaneous bidirectional interaction between all parts of the problem and the solution is obtained in a single "iteration", unlike digital computers that require multiple iterations.

Analog circuits for solving optimization problems have been extensively studied in the past [26, 91, 48]. Our renewed interest in analog optimization stems from Model Predictive Control (MPC) [33, 65]. In MPC at each sampling time, starting at the current state, an open-loop optimal control problem is solved over a finite horizon. The optimal command signal is applied to the process only during the following sampling interval. At the next time

step, a new optimal control problem based on new measurements of the state is solved over a shifted horizon. The optimal solution relies on a dynamic model of the process, respects input and output constraints, and minimizes a performance index. When the model is linear and the performance index is based on two-norm, one-norm or ∞-norm, the resulting optimization problem can be cast as a linear program (LP) or a quadratic program (QP), where the state enters the right hand side (rhs) of the constraints.

This thesis proposes an analog circuit which can solve MPC problems faster and using less power then any digital method. The proposed circuit can be applied to a wide range of problems. Everything that requires repeated low-latency solution of similar problems is a potential application for analog optimization technology. Examples of possible application are (1) a MIMO receiver for mobile network, where the analog circuit recovers source signal from multiple antenna measurements; (2) image processing (e.g. edge detection, optical flow) implemented on the focal plane of CMOS sensor, where the processing is performed in an analog domain prior to image sampling; (3) error correcting decoder that recovers a valid code word from a corrupted one.

1.2 Outline and Contribution

This thesis presents an analog circuit which can solve LP or QP problems with varying r.h.s. (right hand side). In particular, the steady state voltages are the LP/QP optimizers. This thesis presents the circuit design, studies the steady state and the dynamical properties of the circuit, and demonstrates the method with hardware prototypes and simulations.

The thesis is structured as follows.

Previous work in analog optimization is reviewed in Chapter 2. One of the earliest attempts to use analog circuits for solving optimization problems was made by J. Dennis in his Ph.D. work published in 1959 [26]. More recent works by L. Chua [48] and J. Hopfield [91] proposed to build an analog solver that solves the optimization problem. The chapter discusses similarities and differences between the new circuit and the circuits proposed in previous works.

In Chapter 3 we present the design of the optimization circuit. The circuit proposed in this work is built out of resistors and diodes. A novel way of combining positive and negative resistances yields a linear equality constraint on voltage of the connected nodes. By introducing a diode, an inequality constraint is created. Resistors and a voltage source make linear and quadratic cost functions. Chapter 3 details the basic elements and their interconnection that creates an analog optimization circuit.

In Chapter 4 we show that the steady state of the optimization circuit is equivalent to a solution of the associated optimization problem. We use Karush-Kuhn-Tucker (KKT) conditions and properties of the dual optimization problem to prove the equivalence. This analysis reveals the role of voltages as the primal variables, currents as the dual variables, and the diodes as the enforcers of the complimentary slackness.

Chapter 5 studies the dynamical properties of the circuit when ideal components are replaced by devices with real properties, such as parasitic capacitances and finite gain and feedback of operational amplifiers. In particular, we study the circuit stability and find bounds on circuit critical parameters that guarantee stability of the circuit.

The theory developed in the Chapters 3 through 5 is put to the test with a hardware prototype described in Chapter 6. The prototype is a programmable printed circuit board (PCB) that can be calibrated to solve a QP as required. The PCB is based on digital potentiometers (programmable resistors). Thus, the QP problem to solve is set by a software which calibrates the potentiometers to the required values. After the board is calibrated, it receives analog input and after a transient time of few microseconds it returns an analog output that is a solution to the required QP. The PCB yields good solution accuracy and demonstrates the feasibility of the method. Simultaneously, this works highlights the challenges of building high speed analog optimization devices such as parasitic capacitance and non-linear effects.

We demonstrate the feasibility of nano-second soluion latency by carrying out a high speed design of an analog Very Large Scale Integration (VLSI) chip in Chapter 7. The first section of Chapter 7 shows how an LP/QP optimization circuit can be made out of capacitors instead of resistors. When the optimizing circuit is built using a modern 65nm CMOS technology the transient latency is as low as few nano-seconds. For the VLSI design a new formulation of the circuit using capacitors instead of resistors is developed. A variant of the proofs of Chapter 4 is used to show equivalence between the new circuit with capacitance technology and the LP/QP problem. We create a detailed layout of a solver for a QP problem using switched-capacitors technology. This design occupies just $0.08mm^2$ and yields a solution in $50ns$.

Even though the original motivation for this work stems from MPC applications, the proposed method has a much bigger potential. Chapter 8 is a speculates on additional applications. The analog optimization circuit can be used as a co-processor for fast solution of linear systems, it can decode error correcting codes faster than any digital circuit, it can be used in highly parallel image processing device.

1.3 Outlook

In this thesis we highlight the benefits of using analog optimization circuits over the digital computers. Those include radically lower latency, lower power consumption and smaller physical size. The experiments demonstrate that the developed theory correctly predicts performance of the analog optimization circuit and it is possible to design to a very short latency, in the order of nanoseconds.

However, the experimental part of the work has also illuminates the challenges that should be overcome before the analog circuits can be successfully used in real life applications. Perhaps expectedly, those challenges include the common issues with analog designs — including non-linearity of components, manufacturing tolerances, and oscillatory or unstable

behavior. The required accuracy is achievable using current technology, as shown using the PCB and VLSI designs. Yet, the design process requires an effort that is substantially larger than the one required for modern digital design. This larger effort is translated to longer design cycles and a higher design cost, that is an important limiting factor in today's very competitive technology market.

We believe that a combination of two factors will remove the obstacles for wider adoption of a modern analog computation. The first factor is an increasing demand for advanced low latency computation that digital computers would not be able to meet. The second factor is an advanced design methodology and tools that should lower the barrier for introducing analog computing elements to products. While the former factor is inevitable, since it stems from the inherent limitation of digital computers, the later factor totally depends on the will of the scientific and the engineering communities to invest in an analog computing research.

1.4 Publications

Large parts of this thesis build on results that were previously published in collaboration with colleagues and faculty advisors. These publications are listed below.

Chapters 3 and 4 are partially based on the following two publications

- Sergey Vichik and Francesco Borrelli, *"Solving linear and quadratic programs with an analog circuit"*, Computers & Chemical Engineering, 2014.
- Sergey Vichik and Francesco Borrelli, *"Fast solution of linear and Quadratic Programs with an analog circuit"* in American Control Conference (ACC), 2014, pp. 2954-2959.

Chapter 5 is based on an

- Sergey Vichik, Murat Arcak, Francesco Borrelli, *"Stability of an Analog Optimization Circuit for Quadratic Programming"*, Systems & Control Letters, 2015 (accepted).

The section 7.3 in Chapter 7 is based on Master thesis by Kristel Deems where I have guided and collaborated

- Kristel Deems, *"High Speed Analog Circuit for Solving Optimization Problems"*. M.Sc. thesis. University of California in Berkeley, 2015.

Chapter 2

Literature Review

This thesis can be viewed as an old and recently rediscovered effort to move beyond the digital computation [82, 84, 50, 27]. In this chapter we present the historical perspective of analog computation/optimization and the recent advances in this area.

2.1 "Classical" Analog Computers

Analog computers are an ancient idea and they preceded digital computers by millennia. Any physical system that converts continuous input information to continuous output information is an analog computer.

One of the earliest known analog computers is the *astrolabe* shown in Fig. 2.1a, which is an astronomical device used to compute the position of celestial objects on the sphere as function of time. The first astrolabes are mentioned in the Ptolemey's books *Almagest* and *Geography* from 150 AD, but is thought by some to date back to Hipparchus around 130 BC [55]. Another prominent example is a similar device shown in Fig. 2.1b — the *Antikythera Mechanism* dated to 150-100 BC that can predict, for many years ahead, not only eclipses but also a remarkable array of their characteristics, such as directions of obscuration, magnitude, colour, angular diameter of the Moon, relationship with the Moon's node and eclipse time [30, 31].

Fast forward to two millennia later and we find an array of conceptually similar mechanical analog computers up to the middle of the twentieth century. Those include a tide-predicting machine from 1872 and the Norden bombsight used in World War II.

Starting from the 1950s, electronic analog computers began to dominate due to a faster speed, smaller size and simpler reconfiguration. A traditional electronic analog computer is built out of resistors, capacitors, inductions and operational amplifiers. Most standard mathematical functions, including polynomials, exponents, logarithm and divisions can be implemented using the basic electronic elements [44]. Capacitors are used to store the state of a system, therefore, an analog computer can integrate linear and non-linear ordinary

(a) (b)

Figure 2.1: (a) A planispheric astrolabe from the workshop of Jean Fusoris in Paris circa 1400, on display at the Putnam Gallery in the Harvard Science Center. Sage Ross, Wikimedia Commons. (b) Exploded computer reconstruction of the Antikythera Mechanism, from [31].

differential equations. Even partial differential equations can be solved using analog computers [47].

Electronic analog computers have been used with great success for scientific, industrial and military needs. Non-linear dynamical systems, such as bridge under aerodynamic load, nuclear reactions, problems in astronomy and trajectory tracking and flight control can be studied with analog computers [51]. In fact, the veteran PID controller is a special case of an analog computer since it used to be implemented using analog electronics.

The aforementioned analog computers perform computation by sequential evaluation of mathematical functions, like a chain of linked dials (in Astrolabe, Antikythera, bombsight) or a serial connection of electronic basic blocks. For this reason, this type of analog computers are no match for the digital computers that can perform the same operations faster and with greater precision. However, analog computers can perform operations based on simultaneous interaction between all parts of the problem. One example is mathematical optimization, where the goal is to minimize a function subject to constraints. When sequential computers, digital or analog, solve an optimization problem, they need to use an iterative process to converge to the solution. However, a certain class of analog computers can achieve this goal with no iterations required. In the next section we review iterative and non-iterative analog optimization circuits from the literature.

2.2 Previous Work on Analog Optimization

2.2.1 Mathematically exact analog circuit

Analog circuits for solving optimization problems have been extensively studied in the past [26, 91, 48].

The monograph by J. Dennis [26] presents an analog electrical network for solving an QP

$$\min_{i_V, i_D, i_R} \frac{1}{2} i_R^T Q i_R + c^T i_V \tag{2.1a}$$

$$\text{s.t.} \, [N_V \; N_D \; N_R] \begin{bmatrix} i_V \\ i_D \\ i_R \end{bmatrix} = N_C i_C \tag{2.1b}$$

$$i_D \geq 0 \tag{2.1c}$$

where i_V, i_D, i_R are the optimization variables, $N_V,\ N_D,\ N_R, N_C$ are directed graph incidence matrices, $Q \succ 0$ is a diagonal matrix, and c and i_C are column vectors. The equality and inequality operators are element-wise operators. In Dennis's work, the primal and dual optimization variables are represented by the circuit currents and voltages, respectively. A basic version of Dennis's circuit consists of resistors, current sources, voltage sources, and diodes. In this circuit each element value of matrices $N_V,\ N_D,\ N_R, N_C$ is equal to 1, 0 or -1, since those are directed graph incidence matrices. Therefore, this circuit is limited to problems where the coefficients are in $\{1, 0, -1\}$. An extended version of the circuit includes a multiport DC-DC transformer and can represent arbitrary matrix. Current distribution laws in electrical networks (also known as minimum dissipation of energy principle or Kirchhoff's laws) are used to prove that the circuit equilibrium is governed by the same equations as the Lagrangian Problem that yields the optimizer of the problem [26].

The circuit of Dennis does not implement an iterative algorithm that solves an optimization problem, rather he design the circuit so that the circuit currents and voltages at steady state are the optimizer of the original problem. This is also the approach we took in this thesis. Moreover, nor Denis's circuit neither the circuit proposed in this thesis include, by design, dynamical elements that yield a transient response. Ideally, the circuits reach instantly the equilibrium state. A similar more recent work explores the behavior of resistor-transformer-diode networks as a projection operator [69].

Denis's intention was to use the circuit analogy to develop optimization algorithms. Indeed, while widely cited, this work had limited practical impact due to difficulties in implementing the actual circuit, and especially in implementing the multiport DC-DC transformer.

In later work, Chua [16] showed a different and more practical way to realize the multiport DC-DC transformer using operational amplifiers. In subsequent works, Chua [48, 15] and

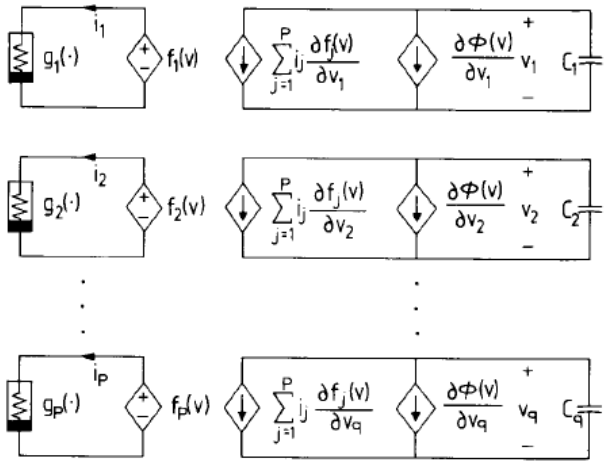


Figure 2.2: Canonical nonlinear programming circuit-dynamic model, from [48]. The circuits on the left generate currents i_j that represent dual variables, circuits on the right implement Lagrangian for KKT optimality conditions.

Hopfield [91] proposed circuits to solve non-linear optimization problems of the form

$$\begin{aligned} &\min_x \ \Phi(x) \\ &\text{s.t. } f_j(x) \leq 0, \ j = 1 \dots m, \end{aligned} \tag{2.2}$$

where $x \in \mathbb{R}^n$ is the vector of optimization variables, $\Phi(x)$ is the cost function, and $f_j(x)$ are the m constraint functions.

The circuits proposed by Chua, Hopfield, and coauthors model the Karush-Kuhn-Tucker (KKT) conditions by representing primal variables as capacitor voltages and dual variables as currents. The dual variables are driven by the inequality constraint violations using high gain amplifiers. The circuit proposed in [48] is shown in Fig. 2.2. The circuit comprises of controlled current sources, each implementing partial derivative $\frac{\partial \Phi(x)}{\partial x_i}$ or $\frac{\partial f_i(x)}{\partial x_i}$, voltage sources implementing $f_j(x)$ and variable nonlinear resistors $g_j(\cdot)$ used to impose the constraints in the circuit realization. The circuit capacitors are charged with a current proportional to the gradient of the Lagrangian of problem (2.2)

$$\frac{\partial x_i}{\partial t} = -\left[\frac{\partial \Phi(x)}{\partial x_i} + \sum_{j=1}^{m} I_j \frac{\partial f_j(x)}{\partial x_i}\right], \tag{2.3}$$

where $\frac{\partial x_i}{\partial t}$ is the capacitor voltage derivative and I_j is the current corresponding to the j-th dual variable. The derivatives $\frac{\partial f}{\partial x_i}$ and $\frac{\partial g_j}{\partial x_i}$ are implemented by using combinations of analog electrical devices [44]. When the circuit reaches an equilibrium, the capacitor charge is constant ($\frac{\partial x_i}{\partial t} = 0$) and Eq. (2.3) becomes one of the KKT conditions.

The circuit in Fig. 2.2 computes violations of the KKT conditions (currents in the right hand circuits) and a feedback loop alters the state variables until an equilibrium is reached.

Therefore, it exhibits the features of an iterative type of analog computers that implement a known mathematical functions and require iterations to converge. The authors prove that their circuit always reaches an equilibrium point that satisfies the KKT conditions. This is an elegant approach since the circuit can be intuitively mapped to the KKT equations. However, the time required for the capacitors to reach an equilibrium is non-negligible. This might be the reason for the relatively large settling time reported to be "tens of milliseconds" for those circuits in [48] for QP and LP problems implemented as a special case of problem (2.2).

2.2.2 Artificial neural network for optimization

Artificial neural network (ANN) are a powerful tool and are applied to various tasks. ANN can be implemented as analog computers [96, 66, 90, 52], or more commonly the networks are digitally simulated.

ANN can be designed and trained to solve linear and nonlinear optimization problems [19, 89]. J. Hopfield proposed a new class of ANN (called later Hopfield Neural Network) that is used to solve the traveling salesman problem [42], LP [91] and more.

The digital simulation of ANN is very computationally intensive and cannot compete with dedicated optimization algorithms and the analog implementations although demonstrate a steady progress over the last two decades but not yet competitive with digital implementations either due to scale or speed [68, 97, 74].

We believe that the analog optimization method proposed in this thesis is simpler, faster and easier to build than the one based on ANN.

2.3 Applications of analog optimization

2.3.1 Image processing

Image processing traditionally requires substantial computing power. Many of the image processing algorithms can be formulated as an optimization problem and solved using an analog circuit. There are many published results in this field [12].

Stocker has successfully used an analog optimization circuit in an analog optical flow sensor [88]. Stocker solves a QP that represents an optical flow problem using analog electronic circuit integrated in a CMOS image sensor. The approach is based on a circuit constructed of transistor and resistors originally proposed by Poggio and Koch [76, 75]. In addition, Poggio and Koch propose to perform edge detection operation using a similar circuit. Harris built an analog VLSI chip to perform Gaussian smoothing, or interpolation and optical flow estimation [37, 38]. A more recent work [18] presents an analog image processing in the focal-plane that is able to compute image convolution with predefined kernels to implement algorithms such as edge detection, smoothing and motion detection.

In 2012 DARPA driven by the realization that *"The digital processors used for ISR data analysis are limited by power requirements, potentially limiting the speed and type of data*

analysis that can be done. A new, ultra-low power processing method may enable faster, mission critical analysis of ISR data" announced the Unconventional Processing of Signals for Intelligent Data Exploitation (UPSIDE) program to *"break the status quo of digital processing with methods of video and imagery analysis based on the physics of nanoscale devices"* [95].

2.3.2 Applying analog circuits to MPC problems

The analog computing era declined before the widespread use of Model Predictive Control. Quero, Camacho and Franquelo [77] have been the first to study the implementation of analog MPC. They use the Hopfield circuit proposed in [91] to implement an MPC controller. The approach they propose is validated with an experimental circuit which reaches the equilibrium after a transient of 1.8 msec.

More recently in [71], fast analog PI controllers are implemented on an Anadigm's Field Programmable Analog Array (FPAA) device [5] for an application involving a fast chemical microreactor. An FPAA is an integrated device containing configurable analog blocks and configurable block interconnections. The analog circuit designed in [71] has a computation time that is faster than that of a digital controller implementing the PI controller. The article briefly proposes to use an FPAA for MPC without specifying details. To the best of the authors knowledge, no further work has been published in this direction.

2.3.3 Analog optimization co-processors

Multiple works have studied an offloading of computing tasks to an analog co-processor. There seems to be a growing consensus in the research community that an analog computation is capable to provide the much needed speed and power efficiency gains. In this thesis we propose to use the analog LP/QP circuit for this purpose, whereas an overwhelming majority of publications studies analog neural networks as an analog co-processor.

S. Koziol studied path planning [53], that is a special case of optimization, with resistive grid or neural network using a family of Field Programmable Analog Arrays (FPAAs) [7, 81, 11]. Those analog devices require tens of microseconds to find a solution, that was shown to be faster than a software solution and comparable to a digital hardware, FPGA, solution. The same family of FPAA devices was used to solve an optimal Bayesian inference and least squares problems using a programmable analog network of 18 neurons with speed 1000 times faster then the digital [83].

A general purpose analog VLSI accelerator and a complete tool chain was developed using hardware neural processing units (NPUs) in a large effort by multiple institutions [87]. In [22], G. Cowan studied solution of ODE,PDE and SDE (stochastic differential equations) using an analog VLSI co-processor and reported computation speed and power consumption substantially better than the digital computers.

The emerging memristor technology [17] may support the analog computation trend, since it provides the way to make compact and configurable resistors. In [79] a configurable memristor network is proposed to accelerate the solution of linear equations to achieve 1500×

reduction in time and 8.5× reduction in energy consumption. An analog neural network configurable using memristors is proposed in [56].

Chapter 3

The novel QP/LP optimization circuit

3.1 Problem statement

This thesis deals with a solution of a quadratic programming (QP) problem

$$\min_{V=[V_1,\ldots,V_n]^T} V^T Q V + cV \tag{3.1a}$$

$$\text{s.t.} \quad A_{\text{eq}} V = b_{\text{eq}} \tag{3.1b}$$

$$A_{\text{ineq}} V \leq b_{\text{ineq}}, \tag{3.1c}$$

where $V_1, \ldots, V_n$ are the optimization variables, b_{eq} and b_{ineq} are column vectors, c is a row vector ,$Q \succ 0$, and A_{ineq} and A_{eq} are matrices. We assume that the matrix Q is positive definite, but will explain also the case where positive semi-definite Q is allowed. A linear programming (LP) problem and solution of a linear system are treated as a special case of the QP problem.

In this chapter we present the basic building blocks which will be later combined to create a circuit that solves problem (3.1). The first basic block enforces equality constraints of the form (3.1b). The second building block enforces inequality constraints of the form (3.1c). Two more basic blocks implement the linear and quadratic cost functions.

3.2 Analog QP Circuit

Proposition 1. *Any QP* (3.1) *can be written in a QP form where all the coefficients of the constraint matrices* A_{eq}, A_{ineq} *are non-negative.*

Proof. We prove it by constructing a QP with non-negative matrices. Consider the QP

$$\min_{\tilde{V}=[\tilde{V}_1,\ldots,\tilde{V}_n]^T} \tilde{V}^T\tilde{Q}\tilde{V} \tag{3.2a}$$

$$\text{s.t.} \quad \tilde{A}_{\text{eq}}\tilde{V} = \tilde{b}_{\text{eq}} \tag{3.2b}$$

$$\tilde{A}_{\text{ineq}}\tilde{V} \leq \tilde{b}_{\text{ineq}} \tag{3.2c}$$

where $\tilde{A}_{\text{eq}}$ and $\tilde{A}_{\text{ineq}}$ are not necessarily non-negative. We introduce an auxiliary vector

$$V \triangleq \begin{bmatrix} V^+ \\ V^- \end{bmatrix} \tag{3.3}$$

and rewrite the QP (3.2) as

$$\min_{V} \quad V^TQV \tag{3.4a}$$

$$\text{s.t.} \quad A^+_{\text{eq}}V^+ + A^-_{\text{eq}}V^- = \tilde{b}_{\text{eq}},\ A^+_{\text{ineq}}V^+ + A^-_{\text{ineq}}V^- \leq \tilde{b}_{\text{ineq}} \tag{3.4b}$$

$$V^+ + V^- = 0, \tag{3.4c}$$

where A_{ineq} and A_{eq} are split into positive and negative parts ($A_{\text{ineq}} = A^+_{\text{ineq}} - A^-_{\text{ineq}}$ and $A_{\text{eq}} = A^+_{\text{eq}} - A^-_{\text{eq}}$). The cost matrix Q in (3.4) satisfies $M^TQM = \tilde{Q}$, where the matrix M is the transformation from $\tilde{V}$ to V

$$V = M\tilde{V} \tag{3.5}$$

$$M = \begin{bmatrix} \mathbb{I} \\ -\mathbb{I} \end{bmatrix}, \tag{3.6}$$

and $\mathbb{I}$ is the identity matrix.

The QP (3.4) can be written in the same form as the original problem (3.1).

$$\min_{V=[V_1,\ldots,V_n]^T} V^TQV \tag{3.7a}$$

$$\text{s.t.} \quad A_{\text{eq}}V = b_{\text{eq}} \tag{3.7b}$$

$$A_{\text{ineq}}V \leq b_{\text{ineq}} \tag{3.7c}$$

where

$$A_{\text{eq}} = \begin{bmatrix} A^+_{\text{eq}} & A^-_{\text{eq}} \\ \mathbb{I} & \mathbb{I} \end{bmatrix} \tag{3.8}$$

$$A_{\text{ineq}} = \begin{bmatrix} A^+_{\text{ineq}} & A^-_{\text{ineq}} \end{bmatrix} \tag{3.9}$$

$$b_{\text{eq}} = \begin{bmatrix} \tilde{b}_{\text{eq}} \\ 0 \end{bmatrix} \tag{3.10}$$

$$b_{\text{ineq}} = \tilde{b}_{\text{ineq}}, \tag{3.11}$$

with A_{eq} and A_{ineq} non-negative by construction. □

3.2.1 Equality constraint

Consider the circuit depicted in Fig. 3.1. V_k is the potential of node k, R_k is the resistance between node k and the common node α with potential U, $-\frac{1}{\sum_k \frac{1}{R_k}}$ is a negative resistance, and $\frac{b}{\sum_k \frac{1}{R_k}}$ is a constant voltage source.

Proposition 2 (Equality constraint circuit)**.** *The circuit in Fig. 3.1 enforces the equality constraint*

$$\begin{bmatrix} \frac{1}{R_1} & \dots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = b. \tag{3.12}$$

Proof. Consider the circuit depicted in Fig. 3.2. In this circuit, n wires are connected to a common node. We call this common node α, its potential U, and the current that exits this node I. Kirchhoff's current law (KCL) implies

$$\sum_{k=1}^{n} I_k = \sum_{k=1}^{n} \frac{V_k - U}{R_k} = I, \tag{3.13}$$

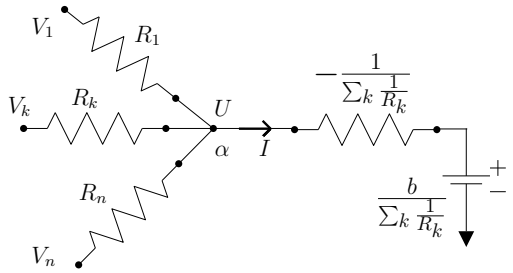


Figure 3.1: Equality enforcing circuit consisting of n resistors ($R_1 \dots R_n$), a negative resistance, and a reference voltage.

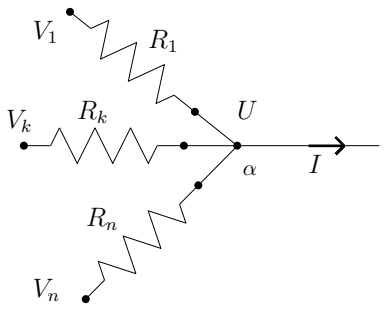


Figure 3.2: A node with n connected wires.

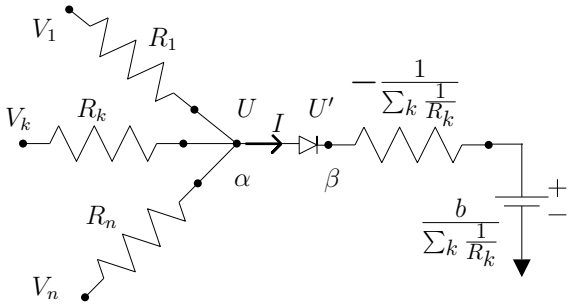


Figure 3.3: Inequality enforcing circuit.

where I_k is the current through branch k, and R_k is the resistance between node k and node α. Eq. (3.13) can be written as an equality constraint on potentials V_k,

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = I + U \sum_{k=1}^{n} \frac{1}{R_k}. \tag{3.14}$$

If the right hand side (rhs) of (3.14) is set to any desired value b, then (3.14) enforces an equality constraint on a linear combination of V_k. The voltage U is set to

$$U = -\frac{I}{\sum_{k=1}^{n} \frac{1}{R_k}} + \frac{b}{\sum_{k=1}^{n} \frac{1}{R_k}}. \tag{3.15}$$

The rhs in (3.15) is implemented by a negative resistance of $-\frac{1}{\sum_{k=1}^{n} \frac{1}{R_k}}$ and a constant voltage source of $\frac{b}{\sum_{k=1}^{n} \frac{1}{R_k}}$. Eq. (3.15) together with (3.14) yield the desired (3.12). Therefore, the circuit shown in Fig. 3.1 enforces (3.12). □

Note that the negative resistance $-\frac{1}{\sum_k \frac{1}{R_k}}$ in the circuit in Fig. 3.1 can be realized by using an operational amplifier [13, pp. 395-397].

3.2.2 Inequality constraint

Consider the circuit shown in Fig. 3.3. Similarly to the equality constraint circuit, n wires are connected to a common node α. α's potential is U and the current exiting this node is I. An ideal diode connects node α to node β. The potential of node β is U'.

Proposition 3 (Inequality constraint circuit)**.** *The circuit in Fig. 3.3 enforces the inequality constraint*

$$\begin{bmatrix} \frac{1}{R_1} & \cdots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \leq b. \tag{3.16}$$

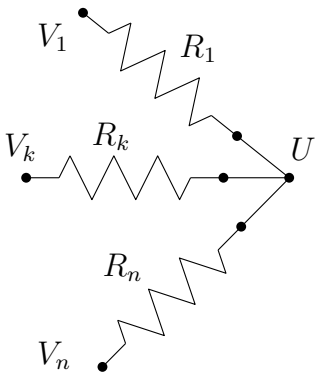


Figure 3.4: Quadratic cost circuit.

Proof. Kirchhoff's current law (KCL) implies (3.13) as in the previous case. The diode enforces $U' \geq U$. In Fig. 3.3, the voltage U' can be computed as follows

$$U' = \frac{b - I}{\sum_{k=1}^{n} \frac{1}{R_k}} \geq U. \tag{3.17}$$

Eq. (3.13) and $U \leq U'$ yield

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = I + U \sum_{k=1}^{n} \frac{1}{R_k} \leq I + U' \sum_{k=1}^{n} \frac{1}{R_k} = b, \tag{3.18}$$

which can be compactly rewritten as (3.16). Therefore, the circuit shown in Fig. 3.3 enforces (3.16).

□

The diode in Fig. 3.3 enforces

$$I \geq 0, \tag{3.19a}$$
$$I(U - U') = 0. \tag{3.19b}$$

By using (3.17) and rearranging its terms, (3.19b) can be rewritten as:

$$I \left(\left(\sum_{k=1}^{n} \frac{1}{R_k} \right) U - b + I \right) = 0. \tag{3.20}$$

Eq. (3.20) will be used later in Section 4.1 to characterize the QP circuit.

3.2.3 Quadratic cost function

Let $A = \begin{bmatrix} A_{\text{eq}} \\ A_{\text{ineq}} \end{bmatrix}$ be the matrix of constraint coefficients. By composing the elementary circuits of the previous sections we can design an analog circuit which implements the constraints $A_{\text{eq}}\, V = b_{\text{eq}}$ and $A_{\text{ineq}}\, V \leq b_{\text{ineq}}$. In section 4.2 it will be shown that such circuit

would minimize a cost function $V^T Q_A V$ where

$$Q_A = \text{diag}(\mathbf{1}^T A) - A^T \,\text{diag}\left(\mathbf{1}^T A^T\right)^{-1} A. \tag{3.21}$$

In general, this cost function is different from the desired cost Q. However, it is possible to add redundant constraints of the form $A_{\texttt{augm}} V < \infty$, which are always inactive and have no effect on a feasible set of the problem (3.1). By doing so the cost matrix can be shaped in a way that $Q_{A'} = kQ$, where $A' = \begin{bmatrix} A \\ A_{\texttt{augm}} \end{bmatrix}$, $k > 0$ is a scalar, and $Q_{A'} = \text{diag}(\mathbf{1}^T A') - A'^T \,\text{diag}\left(\mathbf{1}^T A'^T\right)^{-1} A'$ (see section 4.2 for additional details). The redundant constraints are implemented using a simple circuit depicted in Fig. 3.4, i.e, a special case of the inequality circuit, without the diode and the negative resistor.

3.2.4 Connecting the basic circuits to form a QP circuit

This section presents how to construct the circuit that solves a general QP. We construct the conductance matrix $A \in \mathbb{R}^{m \times n}$ as

$$A \triangleq \begin{bmatrix} A_{\text{eq}} \\ A_{\text{ineq}} \end{bmatrix} \tag{3.22}$$

and denote A_{ij} the i, j element of A. For a given QP (3.1) the R_{ij} resistor is defined as

$$R_{ij} = \frac{1}{A_{ij}}, \; i = 1, \ldots m, \quad j = 1, \ldots, n. \tag{3.23}$$

Consider the circuit shown in Fig. 3.5. The circuit is shown using a compact notation where each resistor R_{ij} is represented by a dot, vertical wires represent variable nodes with potentials $V_1 \ldots V_n$ and horizontal wires represent *constraint nodes*. The compact representation of a resistor through the dot symbol is clarified in Fig. 3.6. If $A_{ij} = 0$ then no resistor is present in the corresponding dot.

The QP circuit is constructed by connecting the nodes associated with the variables $V_1 \ldots V_n$ to three types of the basic circuits: equality, inequality and quadratic cost. We will refer to such nodes as *variable nodes*. Each row of the circuit in Fig. 3.5 is one of the basic circuits presented in Sections 3.2.1, 3.2.2 and 3.2.3.

3.3 Analog LP circuit

The LP circuit includes the same equality and inequality circuits as in Sections 3.2.1 and 3.2.2 and a linear cost circuit described in the next section.

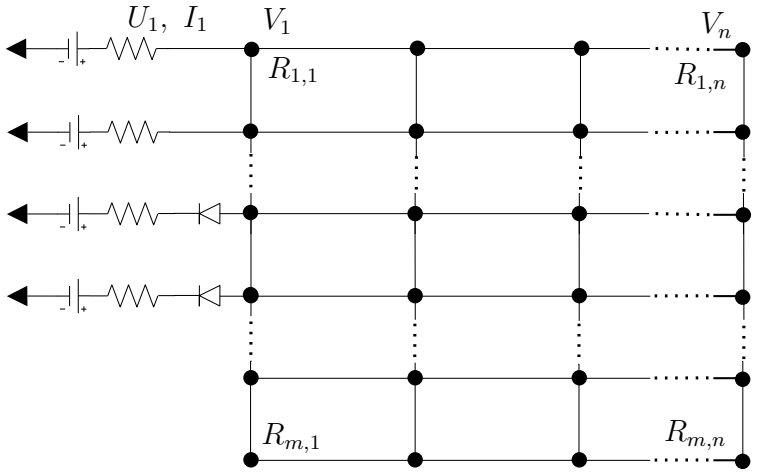


Figure 3.5: Analog circuit solving a QP. Vertical wires are variable nodes with potentials $V_1 \dots V_n$. Black dots represent resistances that connects vertical and horizontal wires. Horizontal wires are cost or constraint nodes. Some of the horizontal wires are connected to a ground via a negative resistance $R_i = -\left(\sum_j {}^1/_{R_{ij}}\right)^{-1}$, a constant voltage source and a diode for inequality nodes.

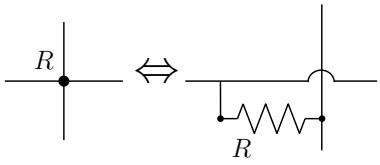


Figure 3.6: Compact representation of a resistor.

3.3.1 Linear cost function

Although the linear cost is a special case of the quadratic cost (see section 4.4.1), we define a special circuit for linear cost since it promotes understanding of the analog optimization circuit and this form is useful for practical purposes.

Consider the circuit in Fig. 3.7. In this circuit the potential of node α is equal to U_{cost} and the current that exits the node is I_{cost}. From (3.14) we have

$$c^T V = I_{\text{cost}} + U_{\text{cost}} \sum_{k=1}^{n} \frac{1}{R_k} \triangleq J. \tag{3.24}$$

where $c = [1/R_1 \ \dots \ 1/R_n]^T$, $V = [V_1 \ \dots \ V_n]^T$ and J is the cost function. This part of the circuit implements the minimization of the linear cost function. A thorough explanation of the cost circuit requires the equations of the whole LP circuit which will be presented in Section 4.4. Here we present a brief intuitive interpretation.

When U_{cost} is set to a low value, the voltages V_k are driven in a direction that minimizes the current I_{cost}. Consequently, the cost J is decreased by decreasing U_{cost}.

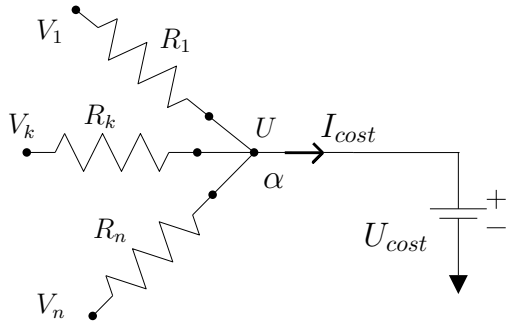


Figure 3.7: Linear cost circuit.

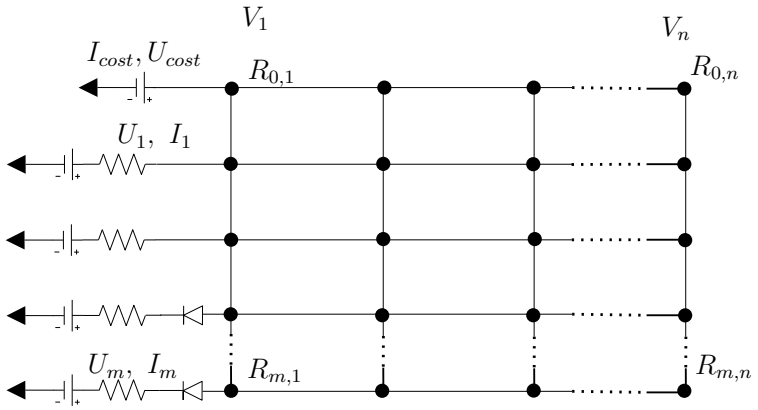


Figure 3.8: Electric circuit solving an LP. Vertical wires are variable nodes with potentials $V_1 \dots V_n$. Black dots represent resistances that connects vertical and horizontal wires. Horizontal wires are cost or constraint nodes. Each horizontal wire is connected to a ground via a negative resistance, a constant voltage source and a diode for inequalities nodes. The topmost horizontal wire is the linear cost circuit which is connected to a constant voltage source U_{cost}.

Note that we can obtain the circuit in Fig. 3.7 from Fig. 3.4 simply by setting one of the variables to a constant voltage U_{cost}.

3.3.2 Connecting the basic circuits to form an LP circuit

This section presents how to construct the circuit that solves a general LP. A similar circuit to the QP circuit in Fig. 3.5 for solving LP is shown in Fig. 3.8. The circuit includes a linear cost circuit instead of quadratic cost circuits. Each row of the circuit in Fig. 3.8 is one of the basic circuits presented in Sections 3.2.1, 3.2.2 and 3.3.1. The LP circuit in Fig. 3.8 is a special case of the QP circuit Fig. 3.5 as will be shown in section 4.4.

Remark 1. *Note that one can easily change the rhs of equality constraints* (3.12) *or/and inequality constrains* (3.16) *to a different value b by simply using a voltage source equal to*

$^{b}/\sum_{k=1}^{n} \frac{1}{R_k}$. *This allows one to solve parametric problems by simply changing the value of the external voltage sources.*

The circuit as shown in Fig. 3.5 contains no dynamic elements such as capacitors or inductors. Therefore, the time required to reach steady-state is governed by the parasitic effects (e.g. wires inductance and capacitance) and by the properties of the elements used to realize negative resistance (usually opamp) and diode. Hence, a good electronic design can achieve solution times on the order of these parasitic effects as shown in Chapters 5 and 7.

Chapter 4

Steady state analysis of the QP/LP circuit

Consider the QP circuit in Fig. 3.5 with R_{ij} defined by Eqs. (3.22)-(3.23). In this chapter we show that the QP circuit in Fig. 3.5 solves the optimization problem (3.1). In particular, the steady-state circuit voltages are the components of an QP optimal solution. First, we derive the steady state equations of the electric circuit and then we show the equivalence.

4.1 Steady state solution of the QP circuit

Consider the circuit in Fig. 3.5. Let $U = [U_1, \ldots, U_m]^T$ be the voltages of the constraint nodes as shown on Fig. 3.5. By applying the KCL (Kirchhoff's current law) to every variable node with potential $V_1, \ldots, V_n$, we obtain

$$\sum_{i=1}^{m} A_{i,j}(U_i - V_j) = 0, \;\; j = 1, \ldots, n \tag{4.1}$$

which can be rewritten in the matrix form

$$\begin{bmatrix} A_{11} & . & A_{1n} \\ \vdots & . & \vdots \\ A_{m1} & . & A_{mn} \end{bmatrix}^T \begin{bmatrix} U_1 \\ \vdots \\ U_m \end{bmatrix} = \begin{bmatrix} (\sum_{i=1}^{m} A_{i,1})V_1 \\ \vdots \\ (\sum_{i=1}^{m} A_{i,n})V_n \end{bmatrix}. \tag{4.2}$$

Eq. (4.2) can be compactly written as

$$A^T U = \mathrm{diag}(\mathbf{1}^T A)V, \tag{4.3}$$

where m is the number of equality and inequality constraints, $\mathbf{1}$ is a vector of ones, and $\mathrm{diag}(x)$ is a diagonal matrix with x on its diagonal.

Next, we apply KCL on all nodes with potentials $[U_1, \ldots, U_m]$ to obtain

$$\sum_{j=1}^{n} A_{i,j}(U_i - V_j) = I_i, \quad i = 1, \ldots, m, \tag{4.4}$$

which can be written in the matrix form

$$\begin{bmatrix} A_{11} & . & A_{1n} \\ \vdots & . & \vdots \\ A_{m1} & . & A_{mn} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} U_1 \sum_{j=1}^{n} A_{1,j} \\ \vdots \\ U_m \sum_{j=1}^{n} A_{m,j} \end{bmatrix} + I, \tag{4.5}$$

where $I = [I_1 \ \ldots \ I_n]$. Eq. (4.5) can be compactly rewritten as

$$AV = \operatorname{diag}\left(\mathbf{1}^T A^T\right) U + I. \tag{4.6}$$

The equality voltage regulator law (3.15) and the inequality law (3.17) can be compactly written as

$$\operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} = b_{\text{eq}} - I_{\text{eq}} \tag{4.7a}$$

$$\operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} \leq b_{\text{ineq}} - I_{\text{ineq}}. \tag{4.7b}$$

By substituting (4.7) into (4.6), we obtain

$$A_{\text{eq}} V = b_{\text{eq}} \tag{4.8a}$$

$$A_{\text{ineq}} V \leq b_{\text{ineq}}. \tag{4.8b}$$

Substitution of (4.6) for inequalities to the diode constraint (3.20) yields

$$\left[A_{\text{ineq}} V - b_{\text{ineq}}\right]_i \left[I_{\text{ineq}}\right]_i = 0, \ \forall i \in \mathcal{I}, \tag{4.9}$$

where $\mathcal{I}$ is the set of all inequality constraints.

We collect (4.3), (4.1), (4.8), and (3.19a) into one set of equations which characterize the circuit

$$AV = \operatorname{diag}\left(\mathbf{1}^T A^T\right) U + I \tag{4.10a}$$

$$A^T U = \operatorname{diag}(\mathbf{1}^T A) V \tag{4.10b}$$

$$A_{\text{eq}} V = b_{\text{eq}} \tag{4.10c}$$

$$A_{\text{ineq}} V \leq b_{\text{ineq}} \tag{4.10d}$$

$$I_{\text{ineq}} \geq 0 \tag{4.10e}$$

$$\left[A_{\text{ineq}} V - b_{\text{ineq}}\right]_i \left[I_{\text{ineq}}\right]_i = 0, \forall i \in \mathcal{I} \tag{4.10f}$$

where U, I and V are the unknowns. The equations (4.10a) and (4.10b) are derived by appling KCL for all V nodes and U nodes respectively, equation (4.10c) originates from voltage control law for the equality nodes, equations (4.10e), (4.10d), (4.10f) describe ideal diode model and voltage control law for the inequality nodes

4.2 Equivalence of the QP optimization problem and the electric circuit

Assumption 1. *The QP (3.1) is feasible and the feasible set is bounded.*

Assumption 2. *The matrices A_{eq} and A_{ineq} in the QP (3.1) are non-negative, $\mathbf{1}^T A > 0$ and $\mathbf{1}^T A^T > 0$.*

Assumption 3. *The matrix Q in the QP (3.1) is positive definite and strictly diagonally dominant.*

The Assumption 2 is almost trivial, since A_{eq} and A_{ineq} can be made non-negative as follows from Proposition 1, $\mathbf{1}^T A > 0$ holds if there are no zero columns (unused variables), and $\mathbf{1}^T A^T > 0$ holds if there are no zero rows (empty constraints).

The Assumption 3 is not very restrictive, since any positive definite matrix can be transformed to a strictly diagonal dominant form by coordinate transformation, e.g. by an eigenvalue decomposition.

Theorem 1 (Steady state of the circuit is a solution to a QP)**.** *Let Assumptions 1 and 2 hold. Then, the Eqs.* (4.10) *have a solution, and the solution is the optimizer of the QP* (3.1) *with*

$$Q = Q_A = \operatorname{diag}\left(\mathbf{1}^T A\right) - A^T \operatorname{diag}\left(\mathbf{1}^T A^T\right)^{-1} A. \tag{4.11}$$

Proof. First we rearrange (4.10). Eq. (4.10a) can be split into equality and inequality parts

$$A_{\text{eq}} = \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} + I_{\text{eq}} \tag{4.12}$$
$$A_{\text{ineq}} = \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} + I_{\text{ineq}}. \tag{4.13}$$

Eq. (4.10b) can be rewritten as

$$A_{\text{eq}}^T U_{\text{eq}} + A_{\text{ineq}}^T U_{\text{ineq}} = \operatorname{diag}\left(\mathbf{1}^T A\right) V. \tag{4.14}$$

Therefore, (4.10) can be written as

$$A_{\text{eq}} V = \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} + I_{\text{eq}} \tag{4.15a}$$
$$A_{\text{ineq}} V = \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} + I_{\text{ineq}} \tag{4.15b}$$
$$A_{\text{eq}}^T U_{\text{eq}} + A_{\text{ineq}}^T U_{\text{ineq}} = \operatorname{diag}\left(\mathbf{1}^T A\right) V \tag{4.15c}$$
$$A_{\text{eq}} V = b_{\text{eq}} \tag{4.15d}$$
$$A_{\text{ineq}} V \leq b_{\text{ineq}} \tag{4.15e}$$
$$I_{\text{ineq}} \geq 0 \tag{4.15f}$$
$$\left(A_{\text{ineq}} V - b_{\text{ineq}}\right)_i I_{\text{ineq}_i} = 0, \ \forall i \in \mathcal{I}. \tag{4.15g}$$

Next, consider the following quadratic program (QP)

$$\begin{aligned}
&\min_V \ \frac{1}{2} V^T Q_A V \\
&s.t.\ A_{\text{eq}} V = b_{\text{eq}} && \text{(4.16a)} \\
&\quad A_{\text{ineq}} V \leq b_{\text{ineq}}, && \text{(4.16b)}
\end{aligned}$$

From Assumption 1, Problem (4.16) has a finite solution for any Q_A because the feasibility domain is bounded and not empty. The value of Q_A will be selected later. We use this problem to find a solution to (4.10). The KKT conditions are necessary optimality conditions for problems with linear constraints [8, Theorem 5.1.3]. Therefore, there exist $V^\star$, $\mu^\star$, $\lambda^\star$ which satisfy the KKT conditions

$$\begin{aligned}
&A_{\text{eq}}^T \mu^\star + A_{\text{ineq}}^T \lambda^\star + Q_A V^\star = 0 && \text{(4.17a)} \\
&A_{\text{eq}} V^\star = b_{\text{eq}} && \text{(4.17b)} \\
&A_{\text{ineq}} V^\star \leq b_{\text{ineq}} && \text{(4.17c)} \\
&\lambda^\star \geq 0 && \text{(4.17d)} \\
&(A_{\text{ineq}} V^\star - b_{\text{ineq}})_i \lambda_i^\star = 0,\ i \in \mathcal{I}, && \text{(4.17e)}
\end{aligned}$$

where $\mu^\star$ and $\lambda^\star$ are the dual variables of the QP (4.16).

We choose Q_A, $U_{\text{eq}}^\star$, $U_{\text{ineq}}^\star$, $I_{\text{eq}}^\star$ and $I_{\text{ineq}}^\star$ as described by the following equations.

$$\begin{aligned}
Q_A =& \operatorname{diag}\left(\mathbf{1}^T A\right) - A_{\text{eq}}^T \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right)^{-1} A_{\text{eq}} \\
&- A_{\text{ineq}}^T \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)^{-1} A_{\text{ineq}} \\
=& \operatorname{diag}\left(\mathbf{1}^T A\right) - A^T \operatorname{diag}\left(\mathbf{1}^T A^T\right)^{-1} A && \text{(4.18a)} \\
I_{\text{eq}}^\star =& \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) \mu^\star && \text{(4.18b)} \\
U_{\text{eq}}^\star =& \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right)^{-1} A_{\text{eq}} V^\star - \mu^\star && \text{(4.18c)} \\
I_{\text{ineq}}^\star =& \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) \lambda^\star && \text{(4.18d)} \\
U_{\text{ineq}}^\star =& \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)^{-1} A_{\text{ineq}} V^\star - \lambda^\star. && \text{(4.18e)}
\end{aligned}$$

Note that the rhs of Eqs. (4.18) consists of quantities one can compute. Note that the matrices $\operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)$ and $\operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)$ are invertible and positive from the assumptions of Theorem 1. Eqs. (4.18) are combined with (4.17) to obtain

$$\begin{aligned}
&A_{\text{eq}} V^\star = \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}}^\star + I_{\text{eq}}^\star && \text{(4.19a)} \\
&A_{\text{ineq}} V^\star = \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}}^\star + I_{\text{ineq}}^\star && \text{(4.19b)} \\
&A_{\text{eq}}^T U_{\text{eq}}^\star + A_{\text{ineq}}^T U_{\text{ineq}}^\star = \operatorname{diag}\left(\mathbf{1}^T A\right) V^\star && \text{(4.19c)} \\
&A_{\text{eq}} V^\star = b_{\text{eq}} && \text{(4.19d)} \\
&A_{\text{ineq}} V^\star \leq b_{\text{ineq}} && \text{(4.19e)} \\
&I_{\text{ineq}}^\star \geq 0 && \text{(4.19f)} \\
&(A_{\text{ineq}} V^\star - b_{\text{ineq}})_i {I_{\text{ineq}}}_i^\star = 0,\ i \in \mathcal{I}. && \text{(4.19g)}
\end{aligned}$$

In particular, substitution of (4.18b) into (4.18c) and of (4.18d) into (4.18e) yields Eqs. (4.19a) and (4.19b) respectively; substitution of (4.18a), (4.18b) and (4.18d) into (4.17a) yields (4.19c); substitution of (4.18d) into (4.17d) and into (4.17e) yields (4.19f) and (4.19g) respectively.

In conclusion, Eqs. (4.19) are Eqs. (4.15) evaluated at $V^\star$, $U^\star$, and $I^\star$ defined as above. Therefore, there exist $V^\star$, $U^\star$, and $I^\star$ that solve (4.10) and $V^\star$ is an optimizer of the QP (4.16) with $Q = Q_A$ as in (4.18a). □

4.3 Designing quadratic cost objective

Theorem 1 states that the analog circuit solves a QP with the cost matrix defined by the constraint matrix A (4.18a). Naturally, we would like to design the cost matrix independently. This section describes how to shape the quadratic cost function using the quadratic cost circuit from section 3.2.3.

4.3.1 Properties of the quadratic cost matrix

First, we prove that the matrix Q_A as in (4.18a) is positive semi-definite:

Lemma 1. *Let $A \in \mathbb{R}^{m\times n}$ be non-negative, $\boldsymbol{1}^T A > 0$, and $\boldsymbol{1}^T A^T > 0$. Then the matrix*

$$Q_A = \operatorname{diag}(\boldsymbol{1}^T A) - A^T \operatorname{diag}\left(\boldsymbol{1}^T A^T\right)^{-1} A \tag{4.20}$$

is positive semi-definite.

Proof. The matrix Q_A is the Schur complement of

$$S \triangleq \begin{bmatrix} \operatorname{diag}\left(\mathbf{1}^T A\right) & A^T \\ A & \operatorname{diag}\left(\mathbf{1}^T A^T\right) \end{bmatrix}. \tag{4.21}$$

From the properties of Schur complement we know that the matrix S is positive semi-definite if and only if Q_A and $\operatorname{diag}\left(\mathbf{1}^T A^T\right)$ are positive

$$\begin{aligned} \begin{bmatrix} x^T & y^T \end{bmatrix} S \begin{bmatrix} x \\ y \end{bmatrix} &= x^T \operatorname{diag}\left(\mathbf{1}^T A^T\right) x + y^T \operatorname{diag}(\mathbf{1}^T A) y + 2x^T A y \\ &= \sum_{j=1}^{m} x_j^2 \sum_{i=1}^{n} a_{ji} + \sum_{i=1}^{n} y_i^2 \sum_{j=1}^{m} a_{ji} + 2\sum_{i=1}^{n}\sum_{j=1}^{m} x_j y_i a_{ji} \\ &= \sum_{j=1}^{m}\sum_{i=1}^{n} a_{ji}\left(x_j + y_i\right)^2. \end{aligned} \tag{4.22}$$

The matrix S is positive semi-definite as can be seen at (4.22). The matrix $\operatorname{diag}\left(\mathbf{1}^T A^T\right) > 0$ due to the Assumption 2. Therefore, Q_A is positive semi-definite. □

4.3.2 Augmenting the quadratic cost

From eq. (4.18a) follows that the cost matrix Q_A is ultimately set by the constraint coefficient matrix A. In general, the matrix Q_A differs from the required matrix Q in QP (3.1). However, not all constraints influence the solution. Obviously, the inactive constraints have no effect on the solution. We are going to utilize inactive constraints to construct the required cost matrix.

The next theorem presents the main result of this section.

Theorem 2 (QP circuit shaping)**.** *Consider the QP that is equivalent to the circuit in Fig. 3.5 as in Theorem 1*

$$\min_{\bar{V}=[\bar{V}_1,\ldots,\bar{V}_n]^T} \bar{V}^T \bar{Q}_A \bar{V} \tag{4.23a}$$

$$s.t. \quad \bar{A}_{eq}\bar{V} = \bar{b}_{eq} \tag{4.23b}$$

$$\bar{A}_{ineq}\bar{V} \leq \bar{b}_{ineq}, \tag{4.23c}$$

and let Assumptions 1-3 hold for QP (3.1) *and for QP* (4.23)*. Then, there exist* $\bar{A}_{eq}$*,* $\bar{b}_{eq}$*,* $\bar{A}_{ineq}$*,* $\bar{b}_{ineq}$ *such that the optimizer of QP* (4.23) *is the optimizer of QP* (3.1)*.*

Definition 1 (ΔQ^{ij})**.** *Let the matrix* $\Delta Q^{ij} \in \mathbb{R}^{n\times n}$ *with* $i \neq j$ *have all zero elements with the exception of two diagonal elements* (i,i) *and* (j,j) *equal to* 1 *and two off-diagonal elements* (i,j) *and* (j,i) *equal to* -1*. And, let the matrix* $\Delta Q^{ii} \in \mathbb{R}^{n\times n}$ *have all zero elements with the exception of* 1 *at position* (i,i)*.*

Proof of Theorem 2. We prove Theorem 2 by construction. First, we use the constraints of QP (3.1) for QP (4.23) as is. Thus,

$$\bar{A}_{\text{eq}} = A_{\text{eq}}, \quad \bar{b}_{\text{eq}} = b_{\text{eq}} \tag{4.24a}$$

$$\bar{A}_{\text{ineq}} = A_{\text{ineq}}, \quad \bar{b}_{\text{ineq}} = b_{\text{ineq}}. \tag{4.24b}$$

Next, we augment $\bar{A}_{\text{ineq}}$. Let the problem (4.23) be augmented with a constraint that is always inactive

$$a^T V < \infty, \tag{4.25}$$

where $a^T \geq 0$ is a non-negative row vector. This constraint has no influence on the feasible set since it is redundant. Define

$$A' \triangleq \begin{bmatrix} \bar{A} \\ a^T \end{bmatrix}. \tag{4.26}$$

From (4.18a), it follows that

$$Q_{A'} = Q_{\bar{A}} + \text{diag}(a) - \frac{aa^T}{1^T a}, \tag{4.27}$$

where $Q_{\bar{A}} = \mathrm{diag}(\mathbf{1}^T\bar{A}) - \bar{A}^T \mathrm{diag}\left(\mathbf{1}^T\bar{A}^T\right)^{-1}\bar{A}$ is the "natural" cost matrix of the QP (4.23) as defined in (4.18a). Let a have only two non-zero entries a_i and a_j. Then, $Q_{A'}$ is the sum of the quadratic term $Q_{\bar{A}}$ arising from the original constraints $\bar{A}$ and the matrix $\alpha_{ij}\Delta Q^{ij}$

$$Q_{A'} = Q_{\bar{A}} + \alpha_{ij}\Delta Q^{ij},\ i \neq j \tag{4.28a}$$

$$\alpha_{ij} = \frac{a_i a_j}{a_i + a_j} \geq 0, \tag{4.28b}$$

where ΔQ^{ij} as in Definition 1. The redundant constraint is implemented by connecting each variable node V_i with resistor $1/a_i$ to a common node. Since the constraint is always inactive, the diode is always in the non-conducting mode. Therefore, there is no need to include the diode and the negative resistance in the circuit, as shown in Fig. 3.4.

Linear combination of matrices ΔQ^{ij} when $i \neq j$ restricts the value of a diagonal term to be equal to the sum of the off-diagonal terms in the same row. However, we would like to set the diagonal term independently. To achieve this, we augment the vector $\bar{V}$ with an additional constant zero variable

$$V' \triangleq \begin{bmatrix} \bar{V} \\ 0 \end{bmatrix}, \tag{4.29}$$

and augment the QP with a redundant constraint

$$a^T V' < \infty, \tag{4.30}$$

where $a = [0, \ldots, 0, \alpha_{ii}, 0, \ldots, 0, \alpha_{ii}]$ is a $n+1$ dimensional vector of all zeros with the exception of α_{ii} at positions i and $n+1$. Then,

$$\frac{1}{2}V'^T Q_{A'} V' = \frac{1}{2}\bar{V}^T Q_{\bar{A}}\bar{V} + \frac{1}{2}\alpha_{ii}\bar{V}_i^2 = \frac{1}{2}\bar{V}^T\left(Q_{\bar{A}} + \alpha_{ii}\Delta Q^{ii}\right)\bar{V}, \tag{4.31}$$

where ΔQ^{ii} as in Definition 1. This is a special case of the circuit in Fig. 3.4 with one of the variables connected to a zero voltage source (the ground).

From (4.28a) and (4.31) follows that the cost matrix of the augmented problem is

$$\bar{Q}_{\bar{A}} = Q_{\bar{A}} + \sum_{i=1}^{n}\sum_{j=i}^{n}\Delta Q^{ij}\alpha_{ij}. \tag{4.32}$$

The additional inactive constraints represented by α_{ij} are the optimizer of the following LP

$$\min_{k,\{\alpha_{ij}\}_{i,j=1,\ldots,n}} \quad \sum_{i=1}^{n}\sum_{j=1}^{n}\|\alpha_{ij}\|_1 \tag{4.33a}$$

$$s.t.\ kM^T Q M = M^T\left(Q_{\bar{A}} + \sum_{i=1}^{n}\sum_{j=i}^{n}\Delta Q^{ij}\alpha_{ij}\right)M \tag{4.33b}$$

$$k \geq 0 \tag{4.33c}$$

$$\alpha_{ij} \geq 0,\ i,j = 1,\ldots,n, \tag{4.33d}$$

where Q in (4.33b) is the required cost matrix in QP (3.1), M is the transformation from $\tilde{V}$ to V as in (3.6), the optimization variables α_{ij} are the coefficients of the additional inactive constraints as defined in (4.28b), and k is a positive scalar. The LP (4.33) yields the additional constraints required to match the cost function.

The term $M^T \left(\sum_{i=1}^{n} \sum_{j=i}^{n} \Delta Q^{ij} \alpha_{ij} \right) M$ allows constructing any diagonally dominant matrix. The term in $kM^TQM - M^TQ_{\bar{A}}M$ from (4.33b) is diagonally dominant if k is large enough and Q is positive definite from Assumption 3. Therefore, the LP (4.33) is always feasible. Consequently, an augmented QP can be constructed by adding redundant constraints. □

Remark 2. *The LP* (4.33) *may be feasible for some cases even if the matrix Q is not positive definite. For example, if $Q_A = 0$, the LP is feasible for any positive semi-definite Q. Therefore, if the required cost matrix Q is not positive definite but LP* (4.33) *is feasible, it may be implemented with the optimization circuit. Moreover, it is possible to approximate the required cost matrix by relaxing the constraint* (4.33b) *to allow a small error.*

4.4 Steady state solution of the LP circuit

Consider a linear program (LP)

$$\min_{V_\mathtt{f}} \; cV_\mathtt{f} \tag{4.34a}$$

$$\text{s.t.} \quad A_{\text{eq}}V_\mathtt{f} = b_{\text{eq}} \tag{4.34b}$$

$$A_{\text{ineq}}V_\mathtt{f} \leq b_{\text{ineq}} \tag{4.34c}$$

where c is a row vector.

We consider the following assumptions.

Assumption 4. *The LP* (4.34) *is feasible and the feasible set is bounded.*

Assumption 5. *In the LP* (4.34)*, A and c are non-negative, $\mathbf{1}^TA > 0$ and $\mathbf{1}^TA^T > 0$.*

And one of the following two related assumptions:

Assumption 6.A. *The LP* (4.34) *and the dual of LP* (4.34) *are not degenerate [9].*

Assumption 6.B. *The dual of LP* (4.34) *is feasible and the set of dual optimal solutions is bounded.*

Theorem 3 (LP circuit equivalence)**.** *Let Assumptions 4, 5 and one of 6 hold. Then, there exists a circuit as shown in Fig. 3.8 with U_{cost}^{crit}, such that a solution V^* to* (4.10) *is also an optimizer of the LP* (4.34) *for all $U_{cost} \leq U_{cost}^{crit}$.*

The Theorem 3 is proved in two different ways. In the first way, Assumption 6.A is used and an LP is treated as a special case of a QP. In the second way, Assumption 6.B is used and the optimization circuit is analyzed as an LP circuit. The first way is simple and straightforward, and the second way is more involved yet provides additional interesting insights.

Proposition 4. *The LP circuit in Fig. 3.8 is a special case of a QP circuit in Fig. 3.5 and, therefore, is described by Eqs.* (4.10)*.*

Proof. The circuit Fig. 3.8 differs from Fig. 3.5 only by the linear cost circuit as in Fig. 3.7. The linear cost circuit is a quadratic cost circuit, as in Fig. 3.4, where one of the variable nodes is set to a constant value U_{cost} using an equality constraint $V_i = U_{\text{cost}}$. □

4.4.1 Approach 1: LP circuit as a special case of a QP circuit

Our goal is to find an optimizer to the LP (4.34) using the QP (3.1). First, we partition the vector V to a constant ($V_{\mathtt{c}} = \mathtt{const}$) and a free ($V_{\mathtt{f}}$) parts and constraint the constant subset of the vector V in (3.1) to be constant. Second, using this partition we write the quadratic cost matrix Q as

$$Q = \begin{bmatrix} Q_{\mathtt{f},\mathtt{f}} & Q_{\mathtt{f},\mathtt{c}} \\ Q_{\mathtt{c},\mathtt{f}} & Q_{\mathtt{c},\mathtt{c}} \end{bmatrix}. \tag{4.35}$$

Third, we choose such $V_{\mathtt{c}}$ and $Q_{\mathtt{c},\mathtt{f}}$ that $V_{\mathtt{c}} Q_{\mathtt{c},\mathtt{f}} = \frac{1}{\varepsilon} c$. Therefore, the quadratic cross cost term $V_{\mathtt{c}} Q_{\mathtt{c},\mathtt{f}} V_{\mathtt{f}}$ equals to a linear term $\frac{1}{\varepsilon} c V_{\mathtt{f}}$. Note that the choice of $V_{\mathtt{c}}$ and $Q_{\mathtt{c},\mathtt{f}}$ is not unique. The resulting problem has the form

$$\min_{V_{\mathtt{f}}} \ \varepsilon V_{\mathtt{f}}^T Q_{\mathtt{f},\mathtt{f}} V_{\mathtt{f}} + c V_{\mathtt{f}} \tag{4.36a}$$

$$\text{s.t.} \quad A_{\text{eq}} V_{\mathtt{f}} = b_{\text{eq}} \tag{4.36b}$$

$$A_{\text{ineq}} V_{\mathtt{f}} \leq b_{\text{ineq}}. \tag{4.36c}$$

Proposition 5. *There exists a scalar $\varepsilon \geq 0$, such that a solution $V^\star_{f,QP}$ to the QP* (4.36) *is also a solution $V^\star_{f,LP}$ to the LP* (4.34)

Proof. The KKT optimality conditions of the LP (4.34) are

$$c + A_{\text{eq}}^T \mu^\star_{\mathtt{LP}} + A_{\text{ineq}}^T \lambda^\star_{\mathtt{LP}} = 0 \tag{4.37a}$$

$$A_{\text{eq}} V^\star_{\mathtt{f},\mathtt{LP}} = b_{\text{eq}} \tag{4.37b}$$

$$A_{\text{ineq}} V^\star_{\mathtt{f},\mathtt{LP}} \leq b_{\text{ineq}} \tag{4.37c}$$

$$\lambda^\star_{\mathtt{LP}} \geq 0 \tag{4.37d}$$

$$(A_{\text{ineq}} V^\star_{\mathtt{f},\mathtt{LP}} - b_{\text{ineq}})_i \lambda^\star_{i,\mathtt{LP}} = 0, \ \forall i. \tag{4.37e}$$

And the KKT of the QP (4.36) are

$$\varepsilon Q_{\mathtt{f},\mathtt{f}} V^\star_{\mathtt{f},\mathtt{QP}} + c + A^T_{\text{eq}} \mu^\star_{\mathtt{QP}} + A^T_{\text{ineq}} \lambda^\star_{\mathtt{QP}} = 0 \tag{4.38a}$$
$$A_{\text{eq}} V^\star_{\mathtt{f},\mathtt{QP}} = b_{\text{eq}} \tag{4.38b}$$
$$A_{\text{ineq}} V^\star_{\mathtt{f},\mathtt{QP}} \leq b_{\text{ineq}} \tag{4.38c}$$
$$\lambda^\star_{\mathtt{QP}} \geq 0 \tag{4.38d}$$
$$(A_{\text{ineq}} V^\star_{\mathtt{f},\mathtt{QP}} - b_{\text{ineq}})_i \lambda^\star_{i,\mathtt{QP}} = 0, \ \forall i. \tag{4.38e}$$

We are looking for $\varepsilon^{\mathtt{crit}}$ such that for any ε, $0 \geq \varepsilon \geq \varepsilon^{\mathtt{crit}}$ there exists a common primal solution to (4.37) and (4.38), thus $V_{\mathtt{f},\mathtt{LP}} = V_{\mathtt{f},\mathtt{QP}}$.

The KKT conditions (4.37) and (4.38) differ only by the Lagrangian condition (4.37a) and (4.38a). Suppose there exist $V^\star_{\mathtt{f},\mathtt{LP}} = V^\star_{\mathtt{f},\mathtt{QP}}$. that satisfies both KKT conditions. The complimentarity conditions (4.37e) and (4.38e) enforce zero value in the same entries of $\lambda^\star_{\mathtt{LP}}$ and $\lambda^\star_{\mathtt{QP}}$ since $V^\star_{\mathtt{f},\mathtt{LP}} = V^\star_{\mathtt{f},\mathtt{QP}}$. We denote as $\lambda^\star_{\mathtt{active},\mathtt{LP}}$ and $\lambda^\star_{\mathtt{active},\mathtt{QP}}$ the non-zero entries of the dual vector. Therefore, to satisfy that $V^\star_{\mathtt{f},\mathtt{LP}} = V^\star_{\mathtt{f},\mathtt{QP}}$ it is required that the following holds

$$\varepsilon Q_{\mathtt{f},\mathtt{f}} V^\star_{\mathtt{f},\mathtt{QP}} + c + A^T_{\text{eq}} \mu^\star_{\mathtt{QP}} + A^T_{\text{ineq}_{\mathtt{active}}} \lambda^\star_{\mathtt{active},\mathtt{QP}} = 0 \tag{4.39a}$$
$$\lambda^\star_{\mathtt{active},\mathtt{QP}} \geq 0 \tag{4.39b}$$
$$c + A^T_{\text{eq}} \mu^\star_{\mathtt{LP}} + A^T_{\text{ineq}_{\mathtt{active}}} \lambda^\star_{\mathtt{active},\mathtt{LP}} = 0 \tag{4.39c}$$
$$\lambda^\star_{\mathtt{active},\mathtt{LP}} \geq 0 \tag{4.39d}$$

where $V^\star_{\mathtt{f},\mathtt{QP}}$ is given. Equations (4.39) define a polyhedral set in $\varepsilon, \mu^\star_{\mathtt{QP}}, \mu^\star_{\mathtt{LP}}, \lambda^\star_{\mathtt{active},\mathtt{QP}}, \lambda^\star_{\mathtt{active},\mathtt{LP}}$. We are looking for the maximum possible ε in this set by solving the LP

$$\varepsilon^{\mathtt{crit}} = \arg\max_{\varepsilon \geq 0} \ \varepsilon \tag{4.40a}$$
$$s.t. \ \varepsilon Q_{\mathtt{f},\mathtt{f}} V^\star_{\mathtt{f},\mathtt{QP}} + c + A^T_{\text{eq}} \mu^\star_{\mathtt{QP}} + A^T_{\text{ineq}_{\mathtt{active}}} \lambda^\star_{\mathtt{active},\mathtt{QP}} = 0 \tag{4.40b}$$
$$\lambda^\star_{\mathtt{active},\mathtt{QP}} \geq 0 \tag{4.40c}$$
$$c + A^T_{\text{eq}} \mu^\star_{\mathtt{LP}} + A^T_{\text{ineq}_{\mathtt{active}}} \lambda^\star_{\mathtt{active},\mathtt{LP}} = 0 \tag{4.40d}$$
$$\lambda^\star_{\mathtt{active},\mathtt{LP}} \geq 0. \tag{4.40e}$$

The LP (4.40) is always feasible since the point $\varepsilon = 0$ is trivially satisfied. □

Proof of Theorem 3. In order to complete the proof, we set $Q_{\mathtt{c},\mathtt{f}} = -c$ and $V_{\mathtt{c}} = U_{\text{cost}} = -\frac{1}{\varepsilon}$. Note that c is non-negative due to Assumption 5 and $Q_{\mathtt{c},\mathtt{f}}$ is non-positive since it includes only the off-diagonal elements which are non-positive by construction (4.18a). Due to Assumption 6.A, for the LP (4.34) there exists a ball with non-empty interior around the cost vector c such that for every cost vector inside this ball the optimizer stays the same [9]. Therefore, there exists $\varepsilon > 0$ such that $c + \varepsilon Q_{\mathtt{f},\mathtt{f}} V^\star_{\mathtt{f},\mathtt{QP}}$ is inside that ball and, consequently, the LP 4.40 yields $\varepsilon^{\mathtt{crit}} > 0$. Therefore, any $U_{\text{cost}} < U^{\text{crit}}_{\text{cost}} = -\frac{1}{\varepsilon^{\mathtt{crit}}}$ satisfies Theorem 3. □

The problem has a solution $\varepsilon^{\texttt{crit}} > 0$ in most practical cases, since it is equivalent to a sensitivity analysis of an LP problem for change in the cost vector c [9]. For many, if not most cases, an LP problem yields the same optimizer for small changes in the cost vector. For the corner cases when the Assumption 6.A does not hold and $\varepsilon^{\texttt{crit}} = 0$, the QP (4.36) can only approximate the solution of the LP (4.34). When $\varepsilon^{\texttt{crit}} > 0$, the solution to QP (4.36) is an exact solution of LP (4.34).

4.4.2 Approach 2: using LP dual

Consider the LP circuit in Fig. 3.8 with R_{ij} defined by (3.23). In this section we show that there exists a range of U_{cost} values such that the LP circuit in Fig. 3.8 solves the optimization problem (4.34). In particular, the steady-state circuit voltages are the components of an LP optimal solution.

Theorem 3 will be proven in the following way. First, we show that there exists $U_{\text{cost}} = U_{\text{cost}}^{\text{crit}}$ such that any solution to (4.10) is also an LP solution; second, we show that for all $U_{\text{cost}} \leq U_{\text{cost}}^{\text{crit}}$ any solution to (4.10) is also an LP solution.

In Assumption 6.B, we require that the sets of primal optimal and dual optimal solutions are bounded. This can be guaranteed if the primal feasible set is bounded and linear independence constraint qualification (LICQ) [41, p. 29] holds.

Remark 3. *In Theorem 3, we require the LP to be primal and dual feasible. This requirement may be relaxed by using a different LP formulation, such as the big-M two-phase simplex method [9, p. 117] or a homogeneous self-dual problem [100].*

Our next goal is to show that there exists a U_{cost} such that the circuit solution is also a solution to the LP (4.34). To show this we make use of the LP dual problem [9]

$$\max_{\lambda} \; b^T\lambda \tag{4.41a}$$

$$\text{s.t. } [A_{\text{eq}}^T \; A_{\text{ineq}}^T]\lambda = c \tag{4.41b}$$

$$\begin{bmatrix}0 \; \mathbb{I}_{|\mathcal{I}|}\end{bmatrix} \lambda \geq 0, \tag{4.41c}$$

where $\mathbb{I}_{|\mathcal{I}|}$ is an identity matrix of size equal to the number of inequality constraints. We create the following feasibility problem

$$\min_{\lambda, V} \; 0 \tag{4.42a}$$

$$\text{s.t. } A_{\text{eq}}V = b_{\text{eq}}, \; A_{\text{ineq}}V \leq b_{\text{ineq}} \tag{4.42b}$$

$$[A_{\text{eq}}^T \; A_{\text{ineq}}^T]\lambda = c, \; \begin{bmatrix}0 \; \mathbb{I}_{|\mathcal{I}|}\end{bmatrix} \lambda \geq 0 \tag{4.42c}$$

$$c^TV + b_-^T\lambda + b_+^T\lambda_- = 0, \; \lambda + \lambda_- = 0, \tag{4.42d}$$

where b_+ and b_- are the absolute values of the positive and the negative components of b respectively, and λ_- equals $-\lambda$. Note that in Eq. (4.42d) all coefficients are non-negative, and that (4.42d) is equivalent to $c^TV = b^T\lambda$. All feasible points of problem (4.42) are primal (4.34) and dual (4.41) optimal solutions [9].

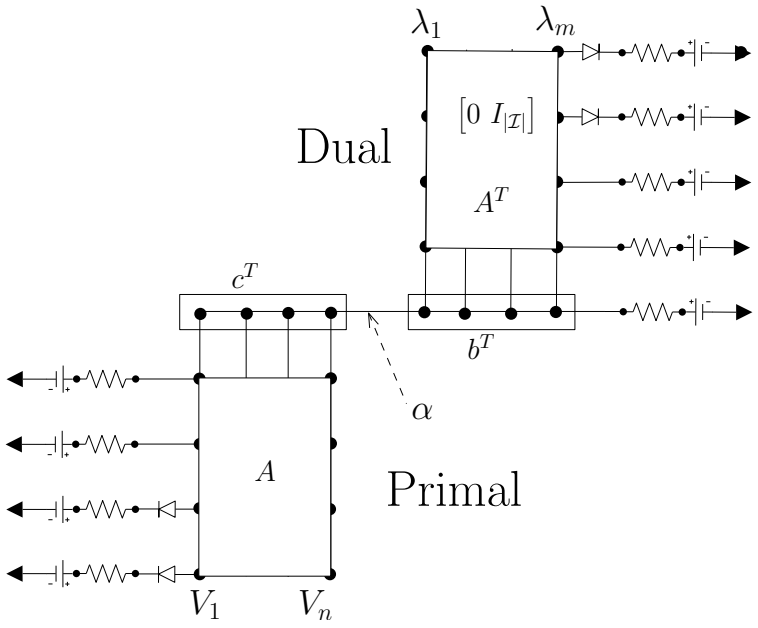


Figure 4.1: Circuit implementing the primal-dual feasibility problem (4.42). Primal and dual parts are connected via the zero duality gap constraint. For compactness, b_+ and b_- are represented as b, and λ_- is part of λ.

Remark 4. *From the Assumption 5 and from the structure of* (4.42d)*, it follows that the matrix of equality and inequality constraints has non-negative coefficients and non-zero rows and columns.*

Problem (4.42) is solved by the circuit shown in Fig. 4.1. The circuit contains two parts: the primal circuit at the bottom and the dual circuit at the top. Primal and dual circuits have the form described in Fig. 3.5 and consist of equality and inequality sub circuits, corresponding to primal and dual constraints, respectively. Note that the cost circuit is not present in the primal and the dual circuits. Instead, the primal and dual circuits are connected by an equality sub circuit that corresponds to the zero duality gap constraint (4.42d).

Proposition 6. *Let Assumptions 4,5 and 6.B hold. The circuit in Fig. 4.1 admits a solution. Moreover, at any circuit solution, the voltages V^* of the variable nodes are a solution to the original LP* (4.34)*.*

Proof. The circuit in Fig. 4.1 consists only of equality and inequality sub circuits. As shown in sections 3.2.1 and 3.2.2, the variable node voltages must satisfy the associated equality or inequality constraints and thus must satisfy Eqs. (4.42). The feasible set of problem (4.42) is the set of all primal optimal and dual optimal variables of problem (4.34). This feasible set is bounded by Assumptions 4-6.B . This fact and the results from Remark 4 imply that all the assumptions of Theorem 1 are satisfied. We conclude that the circuit admits a solution.

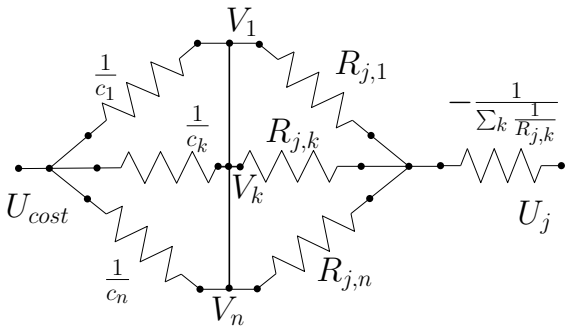


Figure 4.2: Subnetwork that connects the cost node and node j, when the remaining resistors are assumed to be zero.

Moreover, every solution must be a solution of the original LP (4.34) because it satisfies simultaneously dual and primal problems with zero duality gap [9]. □

Note that the circuit in Fig. 4.1 is not a practical way to implement an LP solver. In fact, the matrix A, and vectors c and b appear in two places and a small mismatch can lead to an infeasible problem. Moreover, the ability of easily modifying the LP rhs is lost (see Remark 1). In fact, the components of the rhs vector b also appear as resistors in the zero duality gap constraint.

In the circuit shown in Fig. 4.1, the dual and the primal circuits are connected with a single wire. We denote by U_{cost}^{crit} the voltage of this connection when the circuit settles.

Lemma 2 (Existence of U_{cost}^{crit})**.** *Let Assumptions 4,5 and 6.B hold. Consider the circuit in Fig. 3.8. A steady state voltage V^* with $U_{cost} = U_{cost}^{crit}$ is an optimizer of the LP* (4.34)*.*

Proof. If a voltage equals to $U_{\text{cost}}^{\text{crit}}$ is applied externally to the wire that connects the primal and the dual parts (at point α in Fig. 4.1), we can remove the dual circuit without affecting the primal one. Therefore, the circuit in Fig. 3.8 admits the same solution as the primal circuit in Fig. 4.1. □

Not that the the remaining part of the duality gap equality sub circuit in the primal circuit has exactly the form of the linear cost sub circuit as defined in 3.3.1 and shown in Fig. 3.7.

To complete the proof of Theorem 3 we need to show that for any voltage $U_{\text{cost}} \leq U_{\text{cost}}^{crit}$, the circuit will continue to yield the optimal solution. Assume that U_{cost} is perturbed by ΔU_{cost} from the value U_{cost}^{crit}. We denote perturbed values of variable voltages V as ΔV and perturbed values of the cost current I_{cost} as ΔI_{cost}. Next, we examine the Thevenin equivalent resistance [14] as seen from the cost node. Refer to Fig. 4.2 showing a subnetwork connecting a cost node and an arbitrary node j. We want to compute a lower bound on the equivalent resistance as seen from the cost node. To this aim, we conservatively assume that all other positive resistors in the network are zero, i.e. $R_{k,l} = 0, \forall k, l$ s.t. $k \neq j$. In this scenario, all the variable nodes have the same potential that is equal to the potential U_j.

This implies that the total resistance R_{total} which can be seen from the cost node is greater than or equal to all the cost resistances in parallel. Therefore we have:

$$R_{\text{total}} \geq \frac{1}{\sum_{i=1}^{n} c_i}. \tag{4.43}$$

From applying KCL on the cost node U_{cost} exactly as in (4.4) follows that

$$c^T \Delta V = \left(\sum_{i=1}^{n} c_i \right) \Delta U_{\text{cost}} + \Delta I_{\text{cost}}. \tag{4.44}$$

Using the total equivalent resistance we know that

$$\Delta I_{\text{cost}} = -\frac{\Delta U_{\text{cost}}}{R_{\text{total}}}. \tag{4.45}$$

Combination of (4.44), (4.45) and (4.43) yields

$$\frac{c^T \Delta V}{\Delta U_{\text{cost}}} = \sum_{i=1}^{n} c_i - \frac{1}{R_{\text{total}}} \geq 0. \tag{4.46}$$

Eq. (4.46) states that the change in cost value ($c^T \Delta V$) must have the same sign as the change in ΔU_{cost}. Therefore, when U_{cost} is decreased the cost must decrease or stay the same. However, the cost cannot decrease, since it is already optimal. Therefore the cost must remain constant, and the circuit holds the solution to the problem (3.1) for any $U_{\text{cost}} \leq U_{\text{cost}}^{crit}$. This result completes the proof of Theorem 3.

Remark 5 (U_{cost}^{crit} computation)**.** *Consider the rhs vector b of constraints* (4.34)*. If b is contained in a polytope Θ, the value of U_{cost}^{crit} needs to be low enough to yield a correct solution for any $b \in \Theta$. A lower bound to $U_{cost}^{crit}(b)$ for any $b \in \Theta$ can be computed in many ways. A simple way is to solve for U_{cost} for all vertices of Θ and choose the minimum.*

Chapter 5

Dynamical analysis

The ideal model of the circuit, as presented in Section 3.2, does not contain dynamical elements. In practice there will be parasitic effects and time constants associated to the implementation of a negative resistance. Moreover, the combination of a negative resistance and a capacitance is potentially unstable. Therefore, stability of the circuit must be addressed. This section presents the stability analysis of the QP circuit assuming the presence of a parasitic capacitances and the realization of a negative resistance by using an operational amplifier (opamp). The concluding section of this chapter shows how the speed of the circuit depends on the parasitic effects and design parameters.

Circuits that combine linear dynamics and switching elements have been extensively studied in the past [58, 40]. We describe the circuit as continuous-time piecewise affine system with restricted switching logic and we derive a criterion for the asymptotic stability using a piecewise quadratic Lyapunov function. Stability of a piecewise affine system can be shown by numerically solving an appropriate LMI [45, 39, 29, 58]. In this work we exploit the structure of the circuit to show that the Lyapunov function exists for a range of critical circuit parameters. We make use of an eigenvalue decomposition and KYP lemma to derive the circuit parameter bound. Our results allow to quantify the maximum circuit speed as a function of the circuit parasitic effects.

5.1 Dynamic Model

The negative resistor element that is required for equality and inequality constraints can be realized using an operational amplifier with resistor feedback, as shown in Fig. 5.1. In this circuit a voltage U is applied on an input terminal and the circuit yields a current I (or *vice-versa*). The two input voltages of an ideal opamp are equal in steady state ($U = V_f$), and it is immediate to show that $I = -\frac{U}{R} + b$. Thus, the circuit functions as a negative resistance of $-R$.

In summary, we use the representation in Fig. 5.2 of the analog QP circuit and study its stability. The circuit in Fig. 5.2 is obtained from the circuit in Fig. 3.5 by replacing diodes

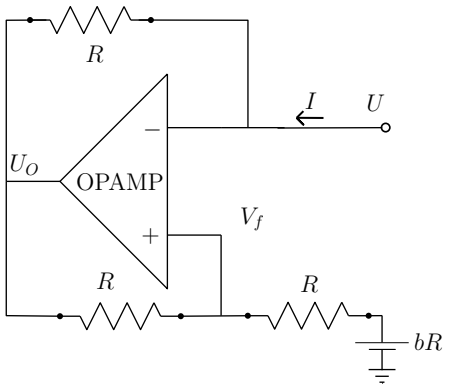


Figure 5.1: Realization of negative resistance using operational amplifier.

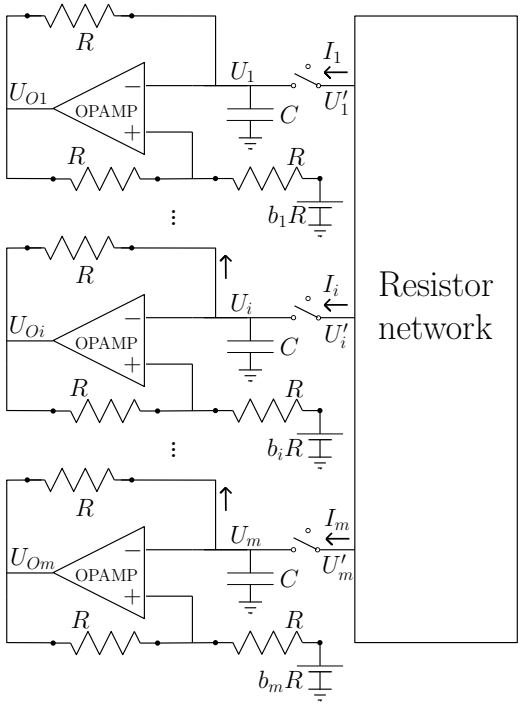


Figure 5.2: Circuit model with opamps and parasitic capacitances.

with switches and using the model of negative resistance as in Fig. 5.1. In addition, the capacitances in Fig. 5.2 capture the dominant parasitic effect. We remind the reader that the circuit consists of m negative resistors connected through m switches to a passive resistor network. It models the optimization circuit, where switches can be either always on (equality constraint), or switching on and off (representing a diode for an inequality constraint), or always off (quadratic cost).

We assume that the circuit is scaled in such a way that the sum of each row of the matrix

A is the same and equals R^{-1}, thus

$$\operatorname{diag}\left(\mathbf{1}^T A^T\right) = R^{-1}\mathbb{I}^m, \tag{5.1}$$

where $\mathbb{I}^m$ is the identity matrix of size m. Any problem can be scaled in this way by multiplying every constraint row in (3.1) by a positive constant. Furthermore, this scaling yields practical benefits by unifying the design of the negative resistors.

We describe the dynamics of an operational amplifier with the first order differential equation

$$\frac{dU_O}{dt} = -\frac{U_O}{\tau} + (V_f - U)\frac{K}{\tau}, \tag{5.2}$$

where K is the gain of an opamp and τ is the time constant of an opamp. Then, the dynamics of each negative resistance circuit and each parasitic capacitor connected to U_i node (as in Fig. 5.2) is given by

$$\frac{dU_i}{dt} = -\frac{U_i - U_{Oi}}{CR} + \frac{I_i}{C} \qquad i = 1, \ldots, m \tag{5.3a}$$

$$\frac{dU_{Oi}}{dt} = U_{Oi}\frac{K-2}{2\tau} - U_i\frac{K}{\tau} + \frac{b_i RK}{2\tau} \qquad i = 1, \ldots, m, \tag{5.3b}$$

where U_i is the voltage of i-th negative resistance, U_{Oi} is the output voltage of i-th opamp, and b_i is the rhs constant from (3.1). Denoting

$$\gamma \triangleq \frac{RCK}{\tau} \tag{5.4}$$

we rewrite (5.3) as

$$\frac{dU_i}{dt'} = -(U_i - U_{Oi}) + RI_i \qquad i = 1, \ldots, m \tag{5.5a}$$

$$\frac{dU_{Oi}}{dt'} = (\frac{\gamma}{2} - \frac{\gamma}{K})U_{Oi} - \gamma U_i + \frac{\gamma b_i R}{2} \qquad i = 1, \ldots, m, \tag{5.5b}$$

where $t' \triangleq {}^{t}/_{RC}$ is the normalized time. We notice that the steady state solution for $K \to \infty$ of these equations recovers the ideal negative resistor characteristics $U_i - Rb_i = -RI_i$.

The non-dimensional parameter γ is the ratio of the circuit RC time constant to an approximated closed loop time constant of the opamp ${}^{\tau}/_{K}$. We will show that the value of this parameter is critical for the circuit stability and we will show that there exist a range of values that make the circuit stable.

5.2 Compact Form – Hybrid Model

Next we rewrite the circuit dynamics in a compact form as a switched affine system. The negative resistor circuits are connected via the resistor network that can be modeled as a

coupling matrix. When potentials $U_1, \ldots, U_m$ are applied to the resistor network as in Fig. 5.2 the current of every port can be obtained by solving (4.10b) and (4.10a). From (4.10b) we know that $V = \operatorname{diag}\left(\mathbf{1}^T A\right)^{-1} A^T U'$ and substitution into (4.10a) yields

$$I = \left(A \operatorname{diag}\left(\mathbf{1}^T A\right)^{-1} A - \operatorname{diag}\left(\mathbf{1}^T A^T\right)\right) U'. \tag{5.6}$$

Let $\bar{A} \triangleq \operatorname{diag}\left(\mathbf{1}^T A^T\right)^{-1} A$ be a normalized conductance matrix, such that sum of each row equals to 1. Denote normalized current as $\bar{I} = RI$ and after substitution of $\bar{I}$ and $\bar{A}$ in (5.6) the current voltage relation is written as

$$\bar{I} = \bar{\mathcal{A}} U' \tag{5.7a}$$

$$\bar{\mathcal{A}} = \bar{A} \operatorname{diag}\left(\mathbf{1}^T \bar{A}\right)^{-1} \bar{A}^T - \mathbb{I}^m, \tag{5.7b}$$

where U' is the vector of voltages U'_i applied to the resistor network as in Fig. 5.2. If an associated switch i is closed, then $U_i = U'_i$. We want to use only the voltages U in the model and, therefore, need to solve for and substitute voltages U' that correspond to open switches.

Define the circuit state vector as

$$X \triangleq [U_1, U_{O1}, \ldots, U_m, U_{Om}]^T. \tag{5.8}$$

We divide the state space $\mathbb{R}^{2m}$ into regions $\mathcal{R}^v$ that correspond to a given switch combination. Let v be the integer representation of the binary vector modeling the status of the switches in Fig. 5.2, where $v \in [0, 2^{|\mathcal{I}|} - 1]$ and $|\mathcal{I}|$ is the number of inequalities in the circuit. Let the matrix $S^v \in \mathbb{R}^{m \times m}$ be a permutation matrix that sorts U in a way that the first variables are associated with the closed switches of a given switch combination v. Let $m_{c,v}$ be a number of closed and $m_{o,v}$ be a number of open switches. X_c^v denotes all elements of the vector X corresponding to the closed switches of the switch index v. Similarly X_o^v refers to open switches. With this notation we have

$$S^v U = \begin{bmatrix} U_c^v \\ U_o^v \end{bmatrix}. \tag{5.9}$$

The matrix $\bar{\mathcal{A}}$ in (5.7b) can be partitioned to closed and open switch blocks

$$\bar{\mathcal{A}} = S^{v,-1} \begin{bmatrix} \bar{\mathcal{A}}_{cc}^v & \bar{\mathcal{A}}_{co}^v \\ \bar{\mathcal{A}}_{oc}^v & \bar{\mathcal{A}}_{oo}^v \end{bmatrix} S^v. \tag{5.10}$$

For closed switches ${U'}_c^v = U_c^v$ and for open switches the current $\bar{I}_o^v$ must be zero. We use those constraints and substitute (5.10) into (5.7)

$$\begin{bmatrix} \bar{I}_c^v \\ 0 \end{bmatrix} = \begin{bmatrix} \bar{\mathcal{A}}_{cc}^v & \bar{\mathcal{A}}_{co}^v \\ \bar{\mathcal{A}}_{oc}^v & \bar{\mathcal{A}}_{oo}^v \end{bmatrix} \begin{bmatrix} U_c^v \\ {U'}_o^v \end{bmatrix}. \tag{5.11}$$

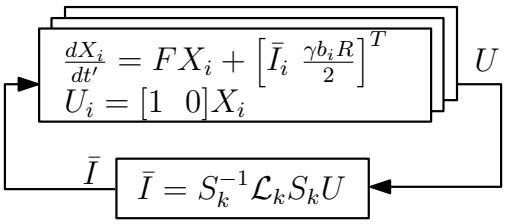


Figure 5.3: Feedback system interconnection. The coupling matrix represents resistor network that is driven by potentials U applied to its connected ports and its output is the current $\bar{I}$.

From the second row of (5.11) we know that $U'^v_o = -\bar{\mathcal{A}}^{v,-1}_{oo}\bar{\mathcal{A}}^v_{oc}U^v_c$. Therefore, from the first row of (5.11) we get $\bar{I}^v_c = \left(\bar{\mathcal{A}}^v_{cc} - \bar{\mathcal{A}}^v_{co}\bar{\mathcal{A}}^{v,-1}_{oo}\bar{\mathcal{A}}^v_{oc}\right)U^v_c$. Consequently, for a given v, the current/voltage model is

$$\bar{I} = S^{v,-1}\mathcal{L}^v S^v U \tag{5.12a}$$

$$\mathcal{L}^v = \begin{bmatrix} \mathcal{A}^v_c & 0 \\ 0 & 0 \end{bmatrix} \tag{5.12b}$$

$$\mathcal{A}^v_c \triangleq \bar{\mathcal{A}}^v_{cc} - \bar{\mathcal{A}}^v_{co}\bar{\mathcal{A}}^{v,-1}_{oo}\bar{\mathcal{A}}^v_{oc} \tag{5.12c}$$

where $\mathcal{A}^v_c \in \mathbb{R}^{m_{c,v}\times m_{c,v}}$ is the Schur complement matrix of the conductivity matrix $\bar{\mathcal{A}}$ and it represents the voltage/current relation of partially connected resistor network corresponding to the switch combination v.

We will denote by $\mathcal{R}^v$ the set of states X for which a switch combination v is feasible. The regions $\mathcal{R}^v$ are polyhedra defined by the diode properties

$$\mathcal{R}^v \triangleq \{X : I^v_o = 0,\ U^v_o - U'^v_o \geq 0,\ I^v_c \geq 0\}. \tag{5.13}$$

The conditions in (5.13) can be rewritten as a set of equalities and inequalities in the X variable by recalling from (5.12) that $U = (\mathbb{I}^m \otimes [1\ 0])X$ and $\bar{I} = S^{v,-1}\mathcal{L}^v S^v U$

$$\mathcal{R}^v \triangleq \{X : [0\ \mathbb{I}^{m_o}]\mathcal{L}^v S^v(\mathbb{I}^m \otimes [1\ 0])X = 0, \tag{5.14a}$$

$$\left([0\ \mathbb{I}^{m_o}] + (\bar{\mathcal{A}}^{v,-1}_{oo}\bar{\mathcal{A}}^v_{oc})[\mathbb{I}^{m_c}\ 0]\right) S^v(\mathbb{I}^m \otimes [1\ 0])X \geq 0, \tag{5.14b}$$

$$[\mathbb{I}^{m_c}\ 0]\mathcal{L}^v S^v(\mathbb{I}^m \otimes [1\ 0])X \geq 0\}, \tag{5.14c}$$

where $\mathbb{I}^m$ is the identity matrix of size m.

Model (5.5) is then rewritten as the interconnection between m decoupled systems and a coupling feedback as shown in Fig. 5.3. Using (5.5) and (5.12) the closed loop system can be written as

$$\begin{aligned}\frac{dX}{dt'} = f(X) =&(\mathbb{I}^m \otimes F)X + (S^{v,-1}\mathcal{L}^v S^v \otimes E)X \\ &+ [b_1 \dots b_m]^T \otimes \begin{bmatrix} 0 \\ \frac{R\gamma}{2} \end{bmatrix},\ X \in \mathcal{R}^v\end{aligned} \tag{5.15}$$

where $\otimes$ is the Kronecker product, F describes the dynamics of a single system and E is a constant matrix

$$F \triangleq \begin{bmatrix} -1 & 1 \\ -\gamma & \frac{\gamma-\gamma\varepsilon}{2} \end{bmatrix}, \quad \varepsilon \triangleq \frac{2}{K} \tag{5.16a}$$

$$E \triangleq \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}. \tag{5.16b}$$

Rewrite (5.15) as a piecewise affine system

$$\dot{X} = f(X) = A^v X + B, \; X \in \mathcal{R}^v \tag{5.17a}$$

$$A^v \triangleq \mathbb{I}^m \otimes F + S^{v,-1}\mathcal{L}^v S^v \otimes E \tag{5.17b}$$

$$B \triangleq [b_1 \dots b_m]^T \otimes \begin{bmatrix} 0 \\ \frac{R\gamma}{2} \end{bmatrix} \tag{5.17c}$$

where the polyhedra $\mathcal{R}^v$ are defined in (5.14).

Lemma 3 (Continuity of $f(X)$)**.** *The function $f(X)$ in* (5.17) *is continuous on its domain.*

Proof. In the interior of each region $\mathcal{R}^v$, the $f(X)$ is affine and thus continuous. We need to prove continuity of $f(X)$ on the borders of region $\mathcal{R}^v$. Let v_1 and v_2 be two switch combinations and consider the shared border $\mathcal{B}$ of regions $\mathcal{R}^{v_1}$ and $\mathcal{R}^{v_2}$, $\mathcal{B} = \mathcal{R}^{v_1} \cap \mathcal{R}^{v_2}$.

Recall that the only term of the dynamic model (5.17) that depends on v is the term $S^{v,-1}\mathcal{L}^v S^v U$ where $\bar{I} = S^{v,-1}\mathcal{L}^v S^v U$. We will prove that the current $\bar{I}$ on the set $\mathcal{B}$ is equal for switch combinations v_1 and v_2, $\bar{I}^{v_1} = \bar{I}^{v_2}$. Let $\mathcal{C}$ be the set of switches which have the same status in v_1 and v_2 and its complement $\bar{\mathcal{C}} = [0, |\mathcal{I}|] \setminus \mathcal{C}$. The switches in $\bar{\mathcal{C}}$ change their state in $\mathcal{B}$ and, therefore, necessarily satisfy diode switch conditions: $I_i = 0$ and $U = U'$.

Consider the switch combinations v_1 and the set $\bar{\mathcal{C}}$. From the definition of $\mathcal{B}$, the currents across the switches $\bar{\mathcal{C}}$ must be equal to zero, either because the switch is open in v_1 or because it is open in v_2. In addition, for such switches $U = U'$ either because the switch is closed in v_1 or because it is closed in v_2. Also currents across open switches in $\mathcal{C}$ are zero both in v_1 and v_2. Similarly $U = U'$ for closed switches in $\mathcal{C}$. The same arguments can be repeated for the switch combination v_2. In conclusion, if we partition the currents $\bar{I}^{v_1}$ and $\bar{I}^{v_2}$ as

$$\bar{I}^{v_1} = [\bar{I}^{v_1,T}_{c,\mathcal{C}}, \bar{I}^{v_1,T}_{o,\mathcal{C}}, \bar{I}^{v_1,T}_{\bar{\mathcal{C}}}]^T \tag{5.18}$$

$$\bar{I}^{v_2,T} = [\bar{I}^{v_2,T}_{c,\mathcal{C}}, \bar{I}^{v_2}_{o,\mathcal{C}}, \bar{I}^{v_2,T}_{\bar{\mathcal{C}}}]^T, \tag{5.19}$$

on the border $\mathcal{B}$ we have:

$$\begin{aligned} &\bar{I}^{v_1}_{\bar{\mathcal{C}}} = \bar{I}^{v_2}_{\bar{\mathcal{C}}} = 0 \\ &\bar{I}^{v_1}_{o,\mathcal{C}} = \bar{I}^{v_2}_{o,\mathcal{C}} = 0 \\ &U'^{v_1}_{c,\mathcal{C}} = U'^{v_2}_{c,\mathcal{C}} = X_{c,\mathcal{C}} \\ &U'^{v_1}_{\bar{\mathcal{C}}} = U'^{v_2}_{\bar{\mathcal{C}}} = X_{\bar{\mathcal{C}}} \end{aligned} \tag{5.20}$$

where $X_\square$ denotes the state variables U in X indexed by $\square$. Rewrite (5.7) for switch v_1 as

$$\begin{bmatrix} \bar{I}^{v_1}_{c,\mathcal{C}} \\ \bar{I}^{v_1}_{o,\mathcal{C}} \\ \bar{I}^{v_1}_{\bar{\mathcal{C}}} \end{bmatrix} = \bar{\mathcal{A}} \begin{bmatrix} U'^{v_1}_{c,\mathcal{C}} \\ U'^{v_1}_{o,\mathcal{C}} \\ U'^{v_1}_{\bar{\mathcal{C}}}, \end{bmatrix} \tag{5.21}$$

and for v_2 as

$$\begin{bmatrix} \bar{I}^{v_2}_{c,\mathcal{C}} \\ \bar{I}^{v_2}_{o,\mathcal{C}} \\ \bar{I}^{v_2}_{\bar{\mathcal{C}}} \end{bmatrix} = \bar{\mathcal{A}} \begin{bmatrix} U'^{v_2}_{c,\mathcal{C}} \\ U'^{v_2}_{o,\mathcal{C}} \\ U'^{v_2}_{\bar{\mathcal{C}}} \end{bmatrix}. \tag{5.22}$$

The linear systems (5.21) and (5.22) have m equations and $2m$ variables ($\bar{I}$ and U'). On the border $\mathcal{B}$, from (5.20) m of the variables are fixed and equal for both switch combinations from (5.20). The solution of $\bar{I}^{v_2}_{c,\mathcal{C}}$ and $\bar{I}^{v_1}_{c,\mathcal{C}}$ (and $U'^{v_1}_{o,\mathcal{C}}$, $U'^{v_2}_{o,\mathcal{C}}$) will yield the same value, thus proving the lemma. □

5.3 Global Asymptotic Stability

Assumption 7. *The circuit in Figure 5.2 has a unique equilibrium point.*

As shown in [98], the circuit has a unique equilibrium that corresponds to the solution of (3.1) for an ideal negative resistance ($\varepsilon \to 0$). Therefore, in the limit $\varepsilon \to 0$ the assumption is equivalent to an assumption that (3.1) is feasible and admits a unique solution.

Theorem 4 (Global asymptotic stability)**.** *Let Assumption 7 hold. For any $\varepsilon > 0$ there exists $\gamma_{crit} > 0$ such that for any γ, $0 < \gamma < \gamma_{crit}$ the equilibrium of the optimization circuit in Figure 5.2 is globally asymptotically stable.*

We prove the theorem using a piecewise quadratic Lyapunov function.The derivative of the Lyapunov function is proved to be negative definite using an eigenvalue decomposition of the resistance matrix. This Lyapunov function has the form (5.24) below due to Krasovskiĭ [54] (see also [49] and [21]).

Lemma 4 (Locally Lipshitz Lyapunov function)**.** *For the system defined in* (5.17)*, if A^v is not singular and there exists $\mathcal{P} = \mathcal{P}^T > 0$ such that*

$$\mathcal{P}A^v + A^{vT}\mathcal{P} \prec 0, \ \forall v \in [0, 2^{|\mathcal{I}|} - 1], \tag{5.23}$$

then

$$L(X) = f(X)^T \mathcal{P} f(X) \tag{5.24}$$

is a Lyapunov function and the equilibrium point is globally asymptotically stable.

Proof. The function $L(X)$ equals zero only at equilibrium and $L(X) > 0$ elsewhere. The function $L(X)$ is differentiable almost everywhere, except in a set of measure zero (region borders). From (5.23) we know that, for almost all t,

$$\begin{aligned}\dot{L}(X(t)) &= f(X(t))^T \left(\mathcal{P}A^v + A^{vT}\mathcal{P}\right) f(X(t)) \\ &\leq -\alpha L(X(t)),\end{aligned} \tag{5.25}$$

where $\alpha > 0$ is such that

$$\mathcal{P}A^v + A^{vT}\mathcal{P} \leq -\alpha\mathcal{P}. \tag{5.26}$$

The function $L(X(t))$ is a locally Lipschitz continuous function of $X(t)$. $X(t)$ is absolutely continuous since it is the solution of the ordinary differential equation (5.15) [20]. Therefore, $L(X(t))$ is an absolutely continuous function of t, and since (5.25) holds for almost all t,

$$L(X(t)) \leq L(X(t_0))e^{-\alpha(t-t_0)}, \quad \forall t > t_0 \tag{5.27}$$

and the asymptotic stability trivially follows from (5.27). Global stability is achieved since the Lyapunov function (5.24) is radially unbounded because both $\mathcal{P}$ and A^v are non singular from the lemma assumptions. □

Lemma 5 (Existence of Lyapunov matrix)**.** *Let A^v be as defined in* (5.17b)*, where $\mathcal{L}^v = \mathcal{L}^{vT}$ as defined in* (5.12b)*, and $\lambda_{vj}(\mathcal{L}^v) \in [\lambda_{\min}, 0]$ is the j-th eigenvalue of $\mathcal{L}^v$, and F, E as defined in* (5.16)*. If there exists P such that*

$$P(F + \lambda E) + (F + \lambda E)^T P \prec 0 \tag{5.28}$$

for all $\lambda \in [\lambda_{\min}, 0]$, then $\mathcal{P} = \mathbb{I}^m \otimes P$ satisfies (5.23)*.*

Proof. Define $T \in \mathbb{R}^{m_c \times m_c}$, $T^T T = \mathbb{I}^m$ to be a matrix whose j-th column is an eigenvector corresponding to
$\lambda_{vj}(S^{v,-1}\mathcal{L}^v S^v)$. Then $T^{v,-1}S^{v,-1}\mathcal{L}^v S^v T^v = \Lambda^v$ diagonalizes $S^{v,-1}\mathcal{L}^v S^v$. Motivated by an observation that the variable transformation $Z = (T^{v,-1} \otimes \mathbb{I}^2)X$ diagonalizes the system, we multiply the matrix $(\mathcal{P}A^k + A^{vT}\mathcal{P})$ from (5.25) by this transformation from left and right and use the definition of A^v and $\mathcal{P}$ to get

$$\begin{aligned}&(T^{v,-1} \otimes \mathbb{I}^2)(\mathcal{P}A^v + A^{vT}\mathcal{P})(T^v \otimes \mathbb{I}^2) \\ &\quad= (T^{v,-1} \otimes \mathbb{I}^2)\left[(\mathbb{I}^m \otimes P)(\mathbb{I}^m \otimes F + S^{v,-1}\mathcal{L}^v S^v \otimes E)\right. \\ &\qquad \left.+(\mathbb{I}^m \otimes F + S^{v,-1}\mathcal{L}^v S^v \otimes E)^T(\mathbb{I}^m \otimes P)\right](T^v \otimes \mathbb{I}^2) \\ &\quad= (Tv, -1 \otimes \mathbb{I}^2)\left[\mathbb{I}^m \otimes (PF + F^T P) + \right. \\ &\qquad \left.+S^{v,-1}\mathcal{L}^v S^v \otimes (PE + E^T P)\right](T^v \otimes \mathbb{I}^2) \\ &\quad= \mathbb{I}^m \otimes (PF + F^T P) + \Lambda^v \otimes (PE + E^T P).\end{aligned} \tag{5.29}$$

This is a block diagonal matrix where each block is given by $P(F + \lambda_{vj}E) + (F + \lambda_{vj}E)^T P$. Since this block is a negative definite matrix according to (5.28), the matrix $\mathcal{P}$ ensures $\mathcal{P}A^v + A^{vT}\mathcal{P} \prec 0$ for all $v \in [0, 2^{|\mathcal{I}|} - 1]$. □

Lemma 6 (Eigenvalues of $\bar{\mathcal{A}}$)**.** *The eigenvalues of*

$$\bar{\mathcal{A}} = \bar{A}\,\mathrm{diag}\left(\boldsymbol{1}^T\bar{A}\right)^{-1}\bar{A}^T - \mathbb{I}^m$$

are in $[-1, 0]$.

Proof. The matrix $\bar{\mathcal{A}}$ is negative semi-definite (see Lemma 1). The matrix $\bar{A}\,\mathrm{diag}\left(\mathbf{1}^T\bar{A}\right)^{-1}\bar{A}^T = CC^T$ is positive semi-definite, where $C = \bar{A}\,\mathrm{diag}\left(\mathbf{1}^T\bar{A}\right)^{-1/2}$. Therefore, eigenvalues of $\bar{A}\,\mathrm{diag}\left(\mathbf{1}^T\bar{A}\right)^{-1}\bar{A}^T$ are non-negative. Consequently, eigenvalues of $\bar{A}\,\mathrm{diag}\left(\mathbf{1}^T\bar{A}\right)^{-1}\bar{A}^T - \mathbb{I}^m = \bar{\mathcal{A}}$ are greater or equal then -1. □

Lemma 7 (Eigenvalues of $\mathcal{A}_c$)**.** *The eigenvalues of*

$$\mathcal{A}_c = \bar{\mathcal{A}}_{cc} - \bar{\mathcal{A}}_{co}\bar{\mathcal{A}}_{oo}^{-1}\bar{\mathcal{A}}_{oc}$$

are in $[-1, 0]$ *for any partitioning of* $\bar{\mathcal{A}}$.

Proof. The matrix $\mathcal{A}_c$ is a Schur complement of the block $\bar{\mathcal{A}}_{oo}$ in the symmetric matrix $\bar{\mathcal{A}}$. Therefore, the eigenvalues of $\mathcal{A}_c$ are bounded between -1 and 0, since eigenvalues of a Schur complement matrix [59] are bounded by the eigenvalues of the original matrix $\bar{\mathcal{A}}$. □

For the next lemma we decompose the matrix E as

$$E = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}\begin{bmatrix} 1 & 0 \end{bmatrix} \triangleq BC. \tag{5.30}$$

Lemma 8 (Existence of P)**.** *There exists a matrix* $P = P^T > 0$ *satisfying*

$$P(F + \lambda BC) + (F + \lambda BC)^T P < 0 \quad \forall\lambda \in [-1, 0] \tag{5.31}$$

if and only if there exists $\tilde{P} = \tilde{P}^T > 0$ *such that*

$$\begin{bmatrix} \tilde{P}F + F^T\tilde{P} & \tilde{P}B - C^T \\ B^T\tilde{P} - C & -2 \end{bmatrix} < 0. \tag{5.32}$$

Proof. We first rewrite (5.31) as:

$$x^T[P(F + \lambda BC) + (F + \lambda BC)^T P]x < 0 \tag{5.33}$$

$\forall x \neq 0,\ \forall\lambda \in [-1, 0]$. Next we define $y \triangleq \lambda Cx$ and rewrite (5.33) as:

$$\begin{bmatrix} x \\ y \end{bmatrix}^T \begin{bmatrix} PF + F^T P & PB \\ B^T P & 0 \end{bmatrix}\begin{bmatrix} x \\ y \end{bmatrix} < 0. \tag{5.34}$$

Since $\lambda \in [-1, 0]$ and $y = \lambda Cx$, we get

$$yCx \leq -y^2; \tag{5.35}$$

that is,

$$\begin{bmatrix} x \\ y \end{bmatrix}^T \begin{bmatrix} 0 & -C^T \\ -C & -2 \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} \geq 0. \tag{5.36}$$

Thus, (5.31) means that (5.34) holds for all $x \neq 0, y \neq 0$ restricted by (5.36).

We now invoke the *S-procedure* [10] which states that, for symmetric matrices T_0, T_1,

$$\zeta^T T_0 \zeta < 0 \quad \text{for all } \zeta \neq 0 \text{ satisfying} \quad \zeta^T T_1 \zeta \geq 0 \tag{5.37}$$

if there exists $q_1 > 0$ such that

$$T_0 + q_1 T_1 < 0. \tag{5.38}$$

Since the matrices in (5.34) and (5.36) play the role of T_0 and T_1 respectively, we conclude from the S-procedure that (5.31) holds if:

$$\begin{bmatrix} PF + F^T P & PB - q_1 C^T \\ B^T P - q_1 C & -2q_1 \end{bmatrix} < 0 \tag{5.39}$$

for some $q_1 > 0$. To prove the "if" part of the lemma, we take the $\tilde{P}$ satisfying (5.32), substitute $P = \tilde{P}$ and $q_1 = 1$ in (5.39), and conclude that (5.31) holds with $P = \tilde{P}$.

To prove the "only if" part, we recall that the S-procedure states that (5.37) also implies (5.38) for some $q_1 \geq 0$, provided there exists ζ_0 such that $\zeta_0^T T_1 \zeta_0 > 0$ [10]. Selecting an x_0 such that $Cx_0 \neq 0$, we confirm that $\zeta_0 \triangleq [x_0^T - \frac{1}{2} Cx_0]^T$ satisfies $\zeta_0^T T_1 \zeta_0 > 0$ for the matrix T_1 in (5.36). Thus, (5.31) implies (5.39) for some $q_1 \geq 0$; in fact, $q_1 > 0$ since the matrix in (5.39) cannot be negative definite with $q_1 = 0$. It then follows that (5.32) holds with the choice $\tilde{P} = \frac{1}{q_1} P$. □

Lemma 9 (KYP)**.** *For any value of $\varepsilon > 0$ there exists $\gamma_{crit} > 0$ such that for any $0 < \gamma < \gamma_{crit}$ there exists $\tilde{P}$ satisfying* (5.32)*.*

Proof. It follows from the Kalman-Yakubovich-Popov (KYP) Lemma [78] that there exists $\tilde{P} > 0$ satisfying (5.32) if

$$\begin{bmatrix} (j\omega I_2 - F)^{-1} B \\ 1 \end{bmatrix}^* \begin{bmatrix} 0 & -C^T \\ -C & -2 \end{bmatrix} \begin{bmatrix} (j\omega I_2 - F)^{-1} B \\ 1 \end{bmatrix} =$$
$$\frac{2(1-\varepsilon^2)\gamma^2 - 8\omega^2}{4\omega^4 + \omega^2\left((\varepsilon-1)^2\gamma^2 - 8\gamma + 4\right) + (\varepsilon+1)^2\gamma^2} - 2 < 0, \forall \omega \in \mathbb{R}. \tag{5.40}$$

When $\omega^2 \to \infty$, (5.40) converges to -2. The expression (5.40) can yield positive values either by continuously crossing zero or when the fraction denominator vanishes while the expression is negative and causes a leap via $-\infty$ to a positive value.

The zero crossing can be checked from

$$8\omega^4 + (2(\varepsilon-1)^2\gamma^2 - 16\gamma + 16)\omega^2 + 4\varepsilon^2\gamma^2 + 4\varepsilon\gamma^2 = 0. \tag{5.41}$$

This is a polynomial in ω^2 and has no roots with positive real part ($\omega^2 < 0$) if all the coefficients have the same sign, according to Routh-Hurwitz criterion for second order polynomials. The last term $4\varepsilon^2\gamma^2 + 4\varepsilon\gamma^2$ is positive for $\varepsilon > 0$ and $\gamma > 0$. It is immediate to see that the second term is positive for a small γ

$$\gamma < \frac{4 - 2\sqrt{4 - 2(\varepsilon-1)^2}}{(\varepsilon-1)^2} = \gamma_{\texttt{crit},(5.42)}. \tag{5.42}$$

The denominator in (5.40) is a second order polynomial in ω^2 as well and we can bound γ in a similar manner using Routh-Hurwitz criterion which yields

$$\gamma < \frac{4 - 2\sqrt{4 - (\varepsilon-1)^2}}{(\varepsilon-1)^2} = \gamma_{\texttt{crit},(5.43)}. \tag{5.43}$$

Thus, there is no ω that cause the denominator to vanish if γ satisfies (5.43). Therefore, for a γ satisfying (5.42) and (5.43) there is no real ω that can make (5.40) positive, consequently, there exists $\gamma_{\texttt{crit}}$ such that $0 < \gamma < \gamma_{\texttt{crit}}$ satisfies (5.32). □

Note that the criteria (5.42) and (5.43) are conservative, since Routh-Hurwitz criterion excludes not only real positive roots but complex positive roots as well. A tight bound for $\gamma_{\texttt{crit}}$ may be obtained when we exclude imaginary roots by examining the discriminant of (5.41) and the discriminant of the denominator in (5.40). As can be seen in Fig. 5.4, $\gamma_{\texttt{crit}}$ approaches 1.1716 as $\varepsilon \to 0$ and admits larger values for a larger ε.

Remark 6. *The existence of the matrix P as required in Lemma 5 can be alternatively shown by numerically checking feasibility as function of γ and ε of the LMI*

$$P \succ 0 \tag{5.44a}$$

$$F^T P + PF + \lambda_i(EP + PE) \prec 0, \quad \lambda_i = -1, 0 \tag{5.44b}$$

where F is a function of γ and ε as in (5.16).

The following lemma is required to prove that the stability is global.

Lemma 10 (Nonsingularity of A^v)**.** *If $\gamma < 2$, the matrix A^v in* (5.17b) *is non-singular for all $v \in [0, 2^{|\mathcal{I}|} - 1]$.*

Proof. From (5.17b) the eigenvalues of A^v are bounded by the sum of eigenvalues of $I_m \otimes F$ and $S^{v,-1}\mathcal{L}^v S^v \otimes E$. The later eigenvalues belong to $[-1, 0]$ as from Lemma 7. The eigenvalues of F are strictly negative for $\gamma < (2 + \varepsilon) < 2$, as can be easily shown using (5.16) and Routh-Hurwitz stability criterion. Therefore, the eigenvalues of A^v are strictly negative for $\gamma < 2$. □

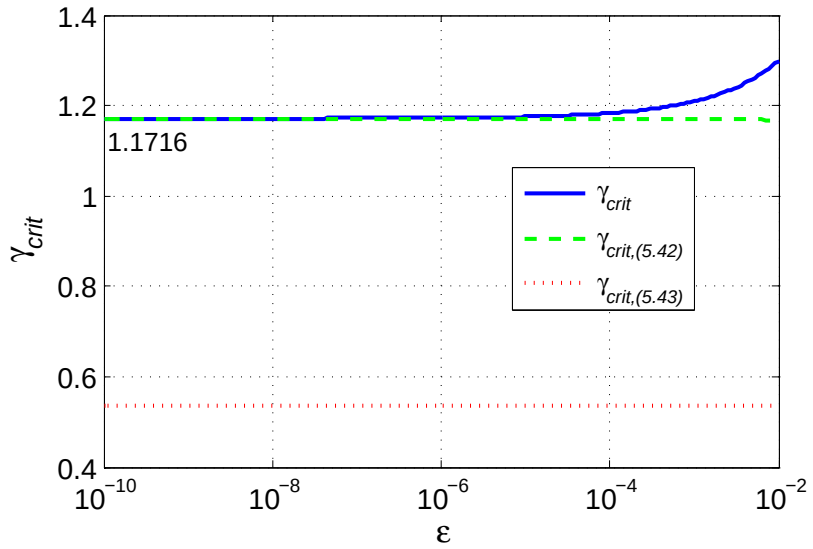


Figure 5.4: The tight bound $\gamma_{\texttt{crit}}$, and the conservative bounds $\gamma_{\texttt{crit},(5.42)}$ and $\gamma_{\texttt{crit},(5.43)}$ vs ε as in Lemma 9.

Proof of Theorem 4: We complete the proof of Theorem 4 by assembling the intermediate results. Lemma 9 states that there exists $\tilde{P}$ for a correct range of γ such that (5.32) holds. Then from Lemma 8 we conclude that there exists P such that (5.31) holds, and, thus, Lemma 5 holds with $\lambda_{\texttt{min}} = -1$ as from Lemmas 6 and 7. Lemma 10 holds for any $\gamma < 2$ ($\gamma_{\texttt{crit}}$ is actually bounded to a lower values as in Fig. 5.4). Lemmas 5 and 10 yield the conditions for Lemma 4 to hold and this completes the proof. ■

5.4 Practical implications of the circuit stability criterion

We have proven that the QP optimization circuit is asymptotically stable if $\gamma = \frac{RCK}{\tau} < \min(2, \gamma_{\texttt{crit}})$. The gain-bandwidth-product (GBWP) of an opamp is given by $\frac{2\pi K}{\tau}$ and the stability condition may be interpreted as $\texttt{GBWP} < \frac{2\pi\gamma_{\texttt{crit}}}{RC}$, meaning that the closed loop time constant of opamp is limited by the RC time constant.

When the circuit is implemented in a nanoscale using analog VLSI technology (as in Chapter 7) with $R \simeq 1\ K\Omega$ and $C \simeq 10\ fF$ ($RC \simeq 10^{-12}$ sec), the gain-bandwidth-product is limited by roughly 120 GHz. For a larger implementation on a printed circuit board (PCB) (as in Chapter 6) with $R \simeq 10\ K\Omega$ and $C \simeq 100\ pF$, the gain-bandwidth-product is limited by 1.2 MHz. Therefore, the circuit should achieve nanosecond range convergence time if implemented using high speed technology, such as analog VLSI.

Chapter 6

Implementation of QP solver on a PCB

6.1 Introduction

The previous chapters established the theoretical basis and studied properties of the proposed QP/LP analog optimization circuit. In this chapter we present the design and performance of an experimental circuit that was built in order to validate the theoretical results. The circuit is implemented on a printed circuit board (PCB) using programmable components to allow solution of QP problems with variable rhs as well as programmable constraint and cost matrices. The board is built for the implementation of an MPC controller for buck DC-DC converter.

6.2 Motivation - buck DC-DC controller

Controllers for buck DC-DC converters have been widely studied in the literature. MPC controllers seem to be an attractive option [63, 62]. In order to reduce the size of passive components in a converter, it is desired that the DC-DC converter operate at higher frequency. Consequently, low latency controllers are required. Low latency technologies, such as FPGA, can be used. We study the feasibility of using an analog circuit as an MPC controller.

A schematic of a DC-DC buck converter system is shown in Fig. 6.1. The input to the converter is the voltage U_s that is usually significantly higher than the required voltage. The converter supplies voltage to an external system represented by the variable resistance $R_{\texttt{load}}$. The controller is responsible to regulate the capacitor voltage u_C to a required voltage v_{ref}. To achieve this, it commands the switch which connects the source voltage U_s and charges the capacitor C. The induction L serves as a low pass buffer that prevents short circuit to the high voltage source. The converter is power efficient since it does not include a heat dissipating components, such as resistors.

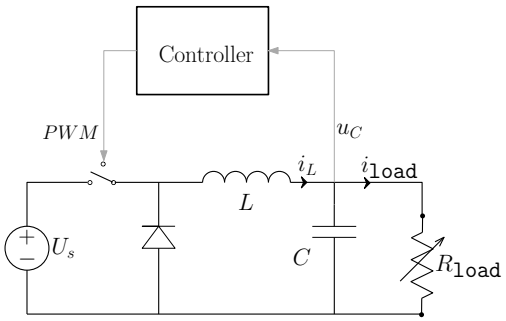


Figure 6.1: Buck DC-DC converter

The model of DC-DC converter used in this thesis is extracted from [62]. The equations describing the continuous time dynamics of the buck converter system shown in Fig. 6.1 can be written as:

$$\dot{x} = A_c x + B_c U_s d + B_{w,c} I_{\texttt{load}} \tag{6.1a}$$

$$A_c = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & -\frac{R_{\texttt{load}}}{L} \end{bmatrix},\ B_c = \begin{bmatrix} 0 \\ \frac{1}{L} \end{bmatrix},\ B_{w,c} = \begin{bmatrix} -\frac{1}{C} \\ 0 \end{bmatrix} \tag{6.1b}$$

$$x \triangleq \begin{bmatrix} u_c \\ I_{\texttt{L}} \end{bmatrix} \tag{6.1c}$$

where d is the duty cycle of the PWM control, u_c is the output voltage of the converter (and of the capacitor C), $I_{\texttt{L}}$ is the current through the inductance L, U_s is the unregulated supply voltage, $I_{\texttt{load}}$ is the supplied load current, C and L are the converter capacitor and inductance values.

For the controller synthesis we use a discrete-time model that we can derive using matrix exponential and zero-order hold approximation from the continuous time model:

$$x_{k+1} = Ax_k + BU_{s,k}d_k + B_w I_{\texttt{load},k} \tag{6.2a}$$

$$A = e^{A_c T_s} \tag{6.2b}$$

$$B = \int_0^{T_s} e^{A_c \tau} d\tau B_c,\ B_w = \int_0^{T_s} e^{A_c \tau} d\tau B_{w,c} \tag{6.2c}$$

The finite time optimal control (FTOC) problem is given by:

$$\min_{x_k, d_k, k=1,\dots N} \sum_{k=1}^{N} (x_{k+1} - x_{\texttt{ref}})^T Q (x_{k+1} - x_{\texttt{ref}}) + (d_k - d_{\texttt{ref}}) R (d_k - d_{\texttt{ref}}) \tag{6.3a}$$

$$\texttt{s.t. } x_{k+1} = Ax_k + BU_{s,k}d_k + B_w I_{\texttt{load},k} \tag{6.3b}$$

$$d_{\min} \leq d_k \leq d_{\max} \tag{6.3c}$$

$$I_{L,k} \leq I_{L\max} \tag{6.3d}$$

$$x_1 = x_{\texttt{measured}} \tag{6.3e}$$

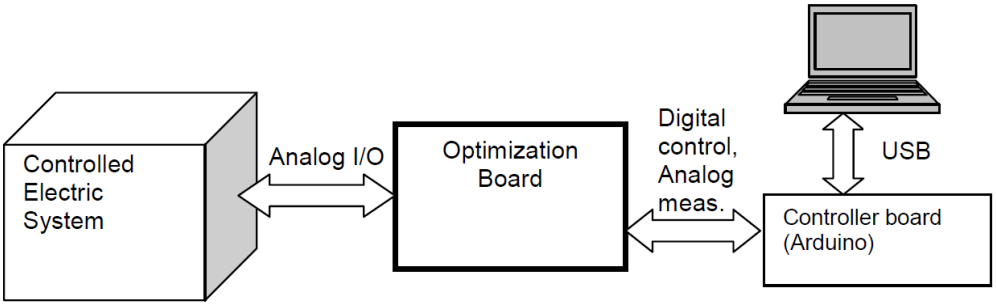


Figure 6.2: Block diagram of a system that includes an optimization board.

where N is the prediction horizon, $d_{\min}$ and $d_{\max}$ are duty cycle limits, $I_{L\,\max}$ is the maximum admissible current that prevents saturation and semiconductor destruction, $x_{\texttt{ref}}$ and $d_{\texttt{ref}}$ are the reference states and command, and $x_{\texttt{measured}}$ is the measured (or estimated) system state.

The MPC controller can be used with prediction horizon of 2 or more. The sampling time T_s and update rate are from 10 KHz to 1 MHz.

6.3 Board design

In this section we detail the design and the main requirements that guided the design process. The optimization board is the main element of the high speed optimal control system (Fig. 6.2) that also includes a controlled system, the optimization board, a controller board and a PC. The controller board (Arduino [6]) is responsible to program and calibrate the board before the operation and monitor its status during the operation. The PC downloads the board setup and software to the controller. During the operation phase, the board receives analog signals from the controlled system and outputs analog control signals to the controlled system. The controlled system in Fig. 6.2 applies to any embedded system. Next we focus on the DC/DC converter as the controlled system.

6.3.1 Requirements and design restrictions

6.3.1.1 QP Problem definition

The board is designed so it can solve the QP in eq. (6.4) as follows

$$\min_{v\in\mathbb{R}^{21}} v^T Q v \tag{6.4a}$$

$$s.t.\ Av = 0 \tag{6.4b}$$

$$l_i < v_i < u_i,\ i = 2, 5, 10, 19 \tag{6.4c}$$

$$v_{11} = 1.21,\ v_{20} = -1.22,\ v_{21} = 0 \tag{6.4d}$$

$$v_i = b_i,\ i = 3, 4, 6, 7, 8, 9, 14, 15, 16, 17, \tag{6.4e}$$

Table 6.1: Variables in the QP board.

Var.#	Type	Bounded	Name
v_{01}	Free		dynamics.Out1.t1
v_{02}	Free	$\surd$	dynamics.Out2.t1
v_{03}	Input		state.Out1.t1
v_{04}	Input		state.Out2.t1
v_{05}	Free	$\surd$	u.Out1.t1
v_{06}	Input		iload.Out1.t1
v_{07}	Input		ref.Out1.t1
v_{08}	Input		ref.Out2.t1
v_{09}	Input		ref_u.Out1.t1
v_{10}	Free	$\surd$	u.Out1.t2
v_{11}	Const		const_max
v_{12}	Free		neg_dynamics.Out1.t1
v_{13}	Free		neg_dynamics.Out2.t1
v_{14}	Input		neg_state.Out1.t1
v_{15}	Input		neg_iload.Out1.t1
v_{16}	Input		neg_ref.Out1.t1
v_{17}	Input		neg_ref.Out2.t1
v_{18}	Free		neg_dynamics.Out1.t2
v_{19}	Free	$\surd$	neg_dynamics.Out2.t2
v_{20}	Const		const_min
v_{21}	Const		zero

where the matrices A and Q are configurable constraint and cost matrices, l_i and u_i are configurable bounds, and b_i are input voltages. The FTOC problem (6.3) can be written as (6.4).

The variables in this problem are of 3 types: input (6.4e), constant (6.4d) and free variables. The input variable are set by an external system in realtime, constant are hardwired to reference voltages, and free variables are the free optimization variables. Four of the free variables are bounded from above and below (6.4c). The variables are detailed in Table 6.1.

6.3.1.2 Accuracy requirements

The board is required to yield a solution with 1% error. The dynamic range of variables is from $-100mV$ to $100mV$, therefore the required accuracy is $2mV$.

6.3.2 Main components

In this section we describe the core components of the PCB board. The board has a number of additional components that are not described in this section. Those include power supplies,

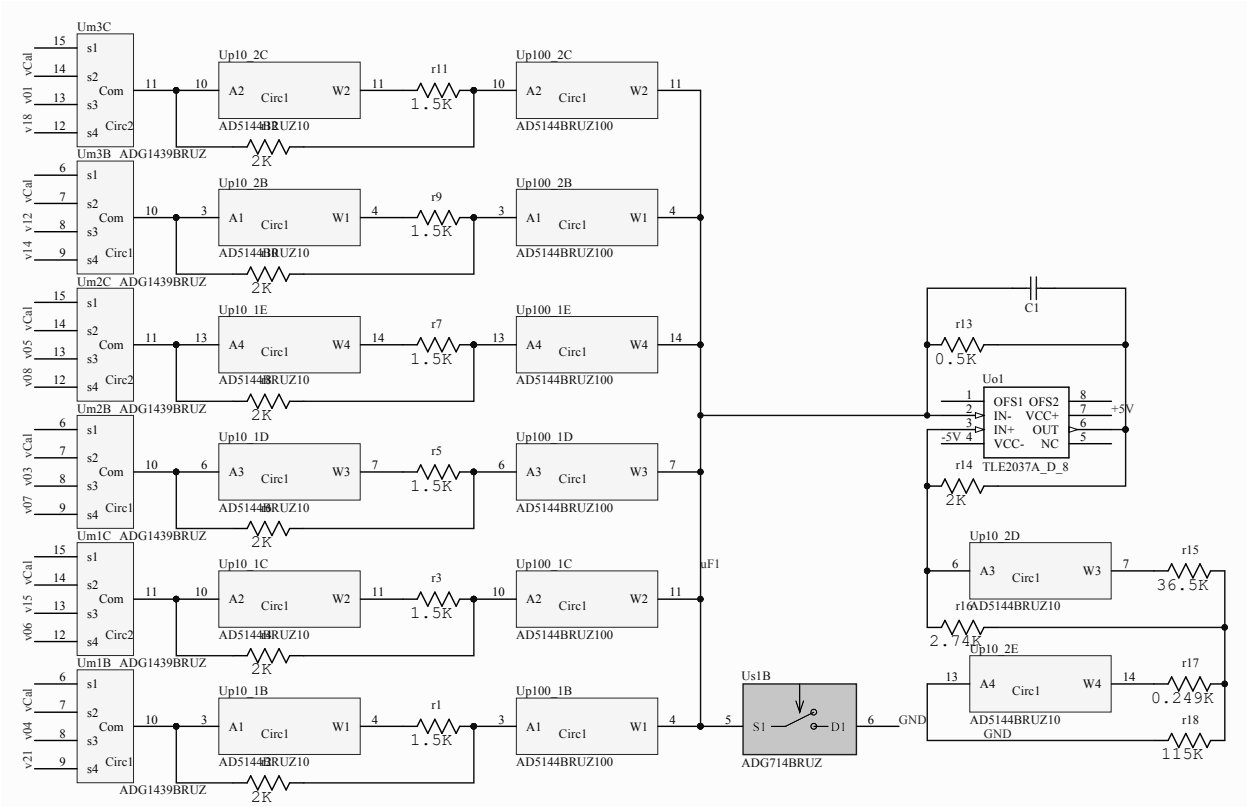


Figure 6.3: Schematics of a 6-variable equality constraint.

reference voltages, sample and hold devices, input and output buffers, clock distribution and signal routing for calibration. Instead, this section is focused on the optimization related functionality – equality and inequality constraints and cost function.

6.3.2.1 Equality constraint

The board implements the equality constraint as suggested in Chapter 3, Fig. 3.1. Two types of equality constraint circuits where used: 6-variable constraint and 2-variable constraint.

The 6-variable constraint is shown in Fig. 6.3. For this constraint, each variable resistor is implemented with two 8-bits AD5144 [1] potentiometers of $10K\Omega$ and $100K\Omega$ connected in series that yield the total resistance given by

$$R_{total} = R_{p100K\Omega} + \frac{2K\Omega(1.5K\Omega + R_{p10K\Omega})}{3.5K\Omega + R_{p10K\Omega}} \tag{6.5}$$

where $R_{p10K\Omega}$ and $R_{p100K\Omega}$ are the resistances of the potentiometers. Eq. (6.5) yields dynamic range of $102K\Omega$ with resolution of roughly 3Ω that is equivalent to about 15 bit resolution. Each variable branch is connected to a multiplexer that allows to connect this branch to 3

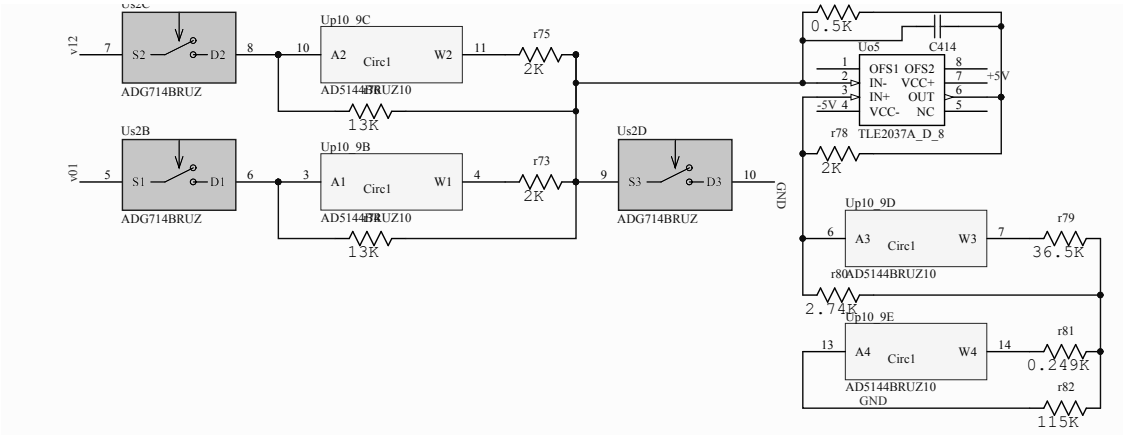


Figure 6.4: Schematics of a 2-variable equality constraint.

different variables. Connection options include special calibration variable that is a current source.

The negative resistor is implemented with a TLE2037a [93] operational amplifier, feedback resistors of 0.5 and 2 $K\Omega$, and two $10K\Omega$ potentiometers that are used for calibration. Using the values of the two feedback resistors, the negative resistor value is $R_{\texttt{eff}} = -\frac{0.5}{2}R_p = -0.25R_p$, where R_p is the total resistance of a bottom branch ($r15, r16, r17, r18$ and the potentiometers Up10_2D and Up10_2E in Fig. 6.3). Tuning accuracy of the negative resistor is smaller than 1 Ω.

The 2-variable constraint is shown in Fig. 6.4. It has the same negative resistance circuit as the 6-variable constraint. The two variable branches consists of $10K\Omega$ potentiometer and static resistors. Each branch can have a resistance between 1733Ω to 6240Ω with 8-bit resolution.

6.3.2.2 Inequality constraint

The PCB board implements a single variable inequality constraint (6.6) that is a special case of the general inequality circuit from Section 3.2.2

$$l_i \leq x_i \leq u_i. \tag{6.6}$$

We use a combination of a switch and a comparator to implement the functionality of a diode, since a regular diode does not provide the required accuracy. Fig. 6.5 shows the conceptual design of a single variable inequality that includes a comparator, a switch and resistors. The comparator measures the direction of current through the constraint and opens and closes the switch accordingly. By reversing the input of the comparator a "less then" or "greater then" functionality is achieved. Fig. 6.6 show the detailed schematics of the inequality constraint. A combination of an analog switch ADG4612 [3] and a comparator MAX9031 [64] was used to implement the functionality of a diode. The bound value (l_i

or u_i) is set using a $10K\Omega$ potentiometer that is shown in the upper left corner and can yield voltages between $-100mV$ to $100mV$. The negative resistance is implemented with OPA4727 [70] operational amplifier and precise $1K\Omega$ resistors.

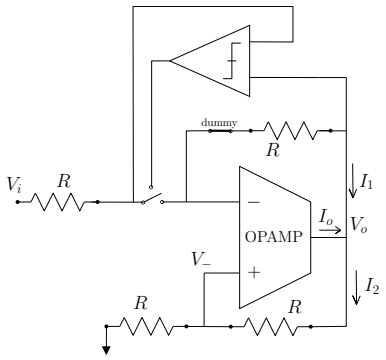


Figure 6.5: Conceptual schematics of an inequality constraint.

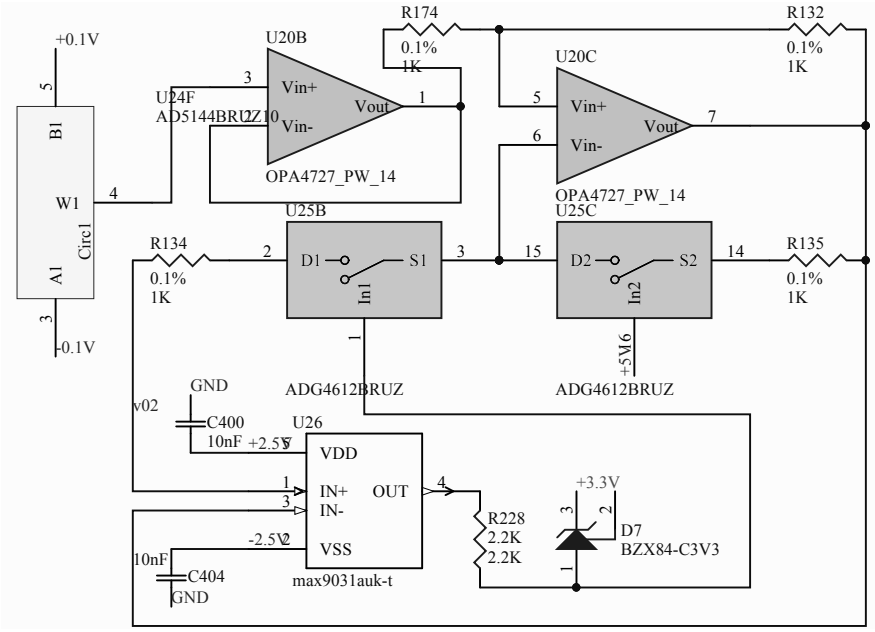


Figure 6.6: Schematics of an inequality constraint.

6.3.2.3 Cost function

The quadratic cost circuit as shown in Fig. 6.7 is the simplest element of all. It consists of a single resistor connecting two variables as described in section 3.2.3. The resistor is connected via a switch ADG714 [4] that can disconnect the two variables if required.

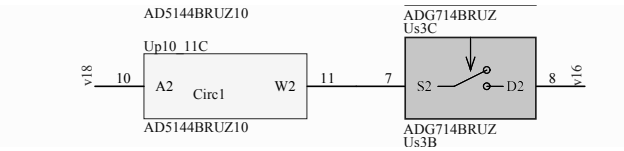


Figure 6.7: Schematics of a cost circuit.

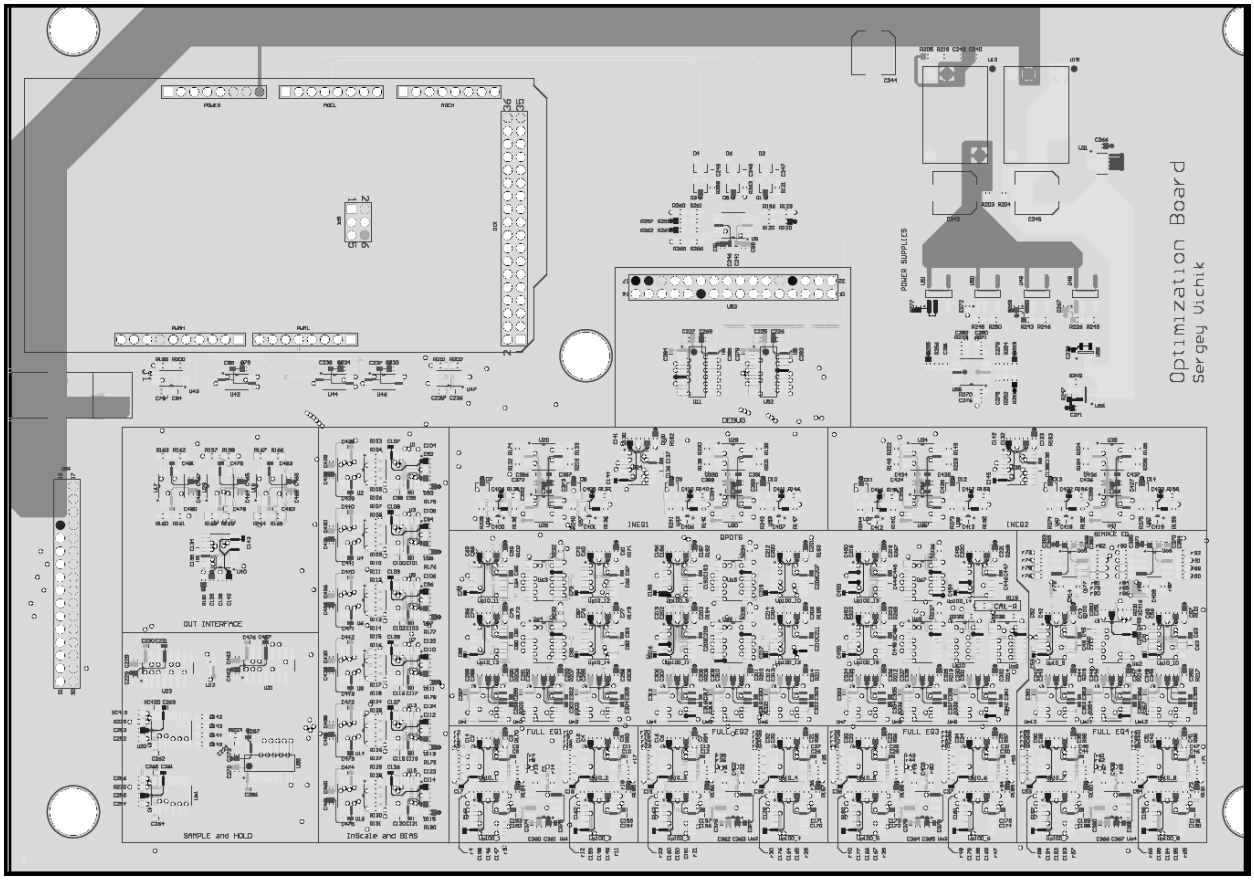


Figure 6.8: PCB layout.

6.3.2.4 PCB layout

The actual layout of the board is shown in Fig. 6.8. It includes an interface to Arduino in upper left corner, power supplies at upper right corner, I/O connector and input scale and bias circuitry at the left center and bottom. The main analog circuitry occupies center and bottom right parts of the board. The manufactured board with the Arduino controller in place is shown in Fig. 6.9.

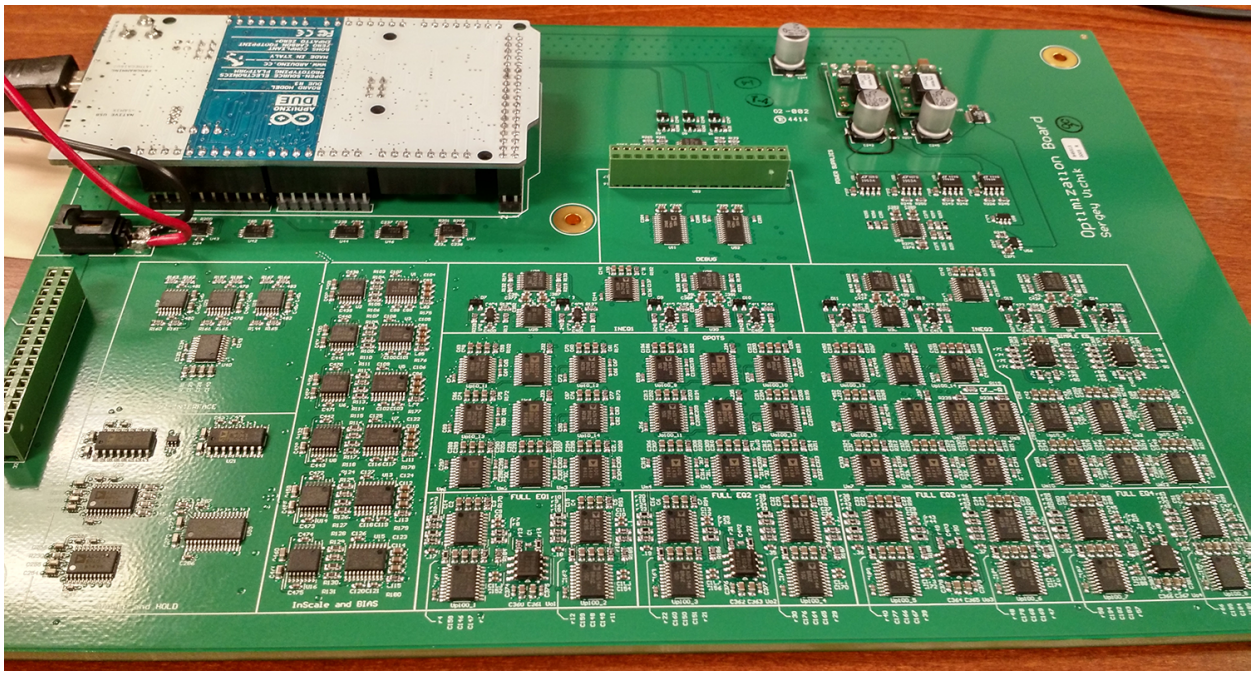


Figure 6.9: The QP board.

6.3.3 Calibration

Calibration is crucial for analog circuits and the board design was driven by a calibration process. The board is configurable with digitally controlled analog switches that allow to calibrate a single component while disconnecting the rest of the board.

All the resistor values in the board are calibrated using a single $10K\Omega$ calibration resistor that is connected with one side to $2.5V$ reference voltage source and the other side can be connected to a required point using digitally controlled analog switches. For all calibrations, a voltage divider is created with switches, where one of the participating resistor is the calibration resistor. By measuring the voltage of the calibration node, (the other port of calibration resistor that is not connected to $2.5V$) we calibrate the other resistance.

The calibration process, as implemented using Arduino micro-controller, includes the following steps:

1. Calibration of Arduino measurement function with known reference voltages and voltage divider using digital potentiometer.
2. Calibration of every variable branch in equality constraints to the required value using the calibration node.
3. Calibration of negative resistance in equality constraints to yield total zero resistance of serial connection with the variable branches.
4. Setting the correct bound values in inequality constraints.
5. Calibrating all the cost resistors to the required value.
6. Calibration of input scale and bias for input variables.
7. Calibration of output scale and bias for output variables.

6.3.4 Arduino software

The board is tested and calibrated using an Arduino DUE micro-controller [6]. The software is responsible for the following tasks

1. Self test.
2. Programming the configurable devices to required values and calibrating.
3. Monitoring variable values during an operational phase.

The software architecture reflects the above requirements and consists of the following modules

1. Programming manager that is responsible to send SPI commands to the programmable devices.

2. Measurement manager that is responsible provide accurate measurement using A/D component of Arduino and the relevant board circuitry.

3. Self-Test is responsible to verify the correctness and functionality of all reference voltages, analog switches and potentiometers.

4. Calibration manager is running the calibration procedure using services from the measurement and the programming managers.

5. Execution manager monitors value of variables, checks constraint satisfaction and recalibrates the circuit is needed.

6.3.5 Voltage measurement with Arduino

The system is required to measure voltage level from $-2.5\ V$ to $2.5\ V$ of any variable with an accuracy better than $1\ mV$ for voltages less then $100\ mV$. The Arduino micro-controller has a built-in 12 bit analog to digital converters that accepts voltages from $0\ V$ to $3.3\ V$. We use 3 ADC inputs of Arduino.

The measurement function of the board consists of the following elements

1. Two 16-port analog multiplexers ADG1406 (U11 and U52 at Fig. 6.10) that select between 21 optimization variables, 6 input variables and reference voltages.

2. An inverting buffer (U9B at Fig. 6.10) that shields the measured variable from the measuring circuit.

3. Three different gains and biases (U9C, U9D and U9E at Fig. 6.10) that translate the measured voltage to the range acceptable by Arduino. The amplified voltage is clamped by diodes to protect Arduino.

The three different gains are 0.665, 3.32, 10. For higher voltage the higher gain saturate Arduino inputs and lower gain is used as described in the following code snippet

```
if (!MSRM_IsSaturated(AD2))
      return AD2*scale[2]+bias[2];
if (!MSRM_IsSaturated(AD1))
      return AD1*scale[1]+bias[1];
return AD1*scale[0]+bias[0];
```

Significant non-linearities and inaccuracies were discovered in the ADC converters. Therefore, an extensive calibration mechanism is established. For the calibration procedure we use a digital potentiometer connected in a voltage divider circuit with either constant resistance or another potentiometer.

Although the total resistance of a potentiometer is inaccurate (8% for AD5144) the resistance changes linearly with the digital code. The calibration procedure is based on

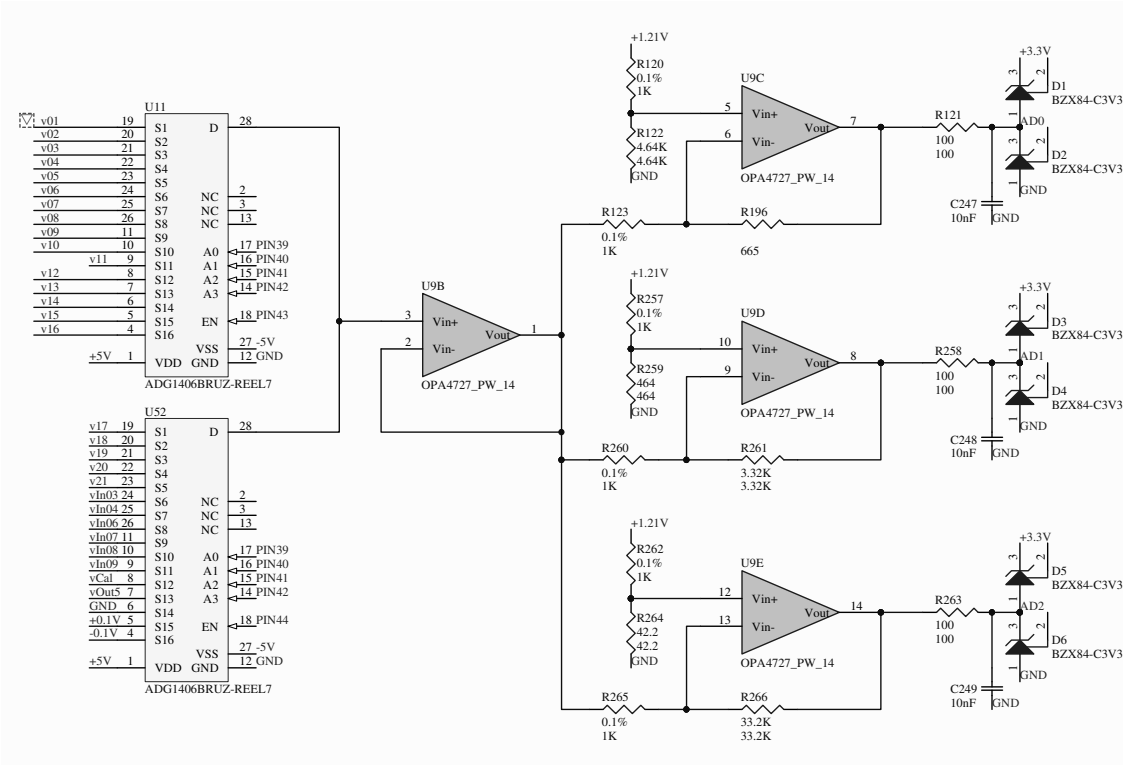


Figure 6.10: Schematics of the measurement function.

this observation. First, a known reference voltage is sampled. Second, by controlling the digitial potentiometer we set a measured voltage equal to the reference voltage. Third, a total resistance of the potentiometer is estimated from the digital value. Fourth, with the complete model of the potentiometer we can set the measured voltage to any desired value. Finally, the table of voltages and the measured digital ADC values is stored in Arduino and is interpolated to translate a digital ADC reading to a physical voltage value. Using this procedure we achieve measurement accuracy of 1 mV.

6.4 Experiments

6.4.1 Solution of a QP with the analog board

The board is used to solve a QP problem of the form (6.4). The coefficients of the problem are listed in (A.2) in the Appendix. The analog solution is compared to the digital solution.

Experiment setup For this experiment the board is wired to a digital to analog converter that sets the 6 input variables of the board. The D/A converter is controlled by a PC running

Matlab software. The constant variables and the input variables are shown in Fig. A.1 in the Appendix.

The onboard Arduino controller samples and stores all optimization variables. The input variables as measured on the board may differ from the values in Matlab due to inaccuracies of the D/A converter and input buffers of the board. In order to overcome this problem, the actual value of the input variables as sampled by the Arduino controller and is used as input to a digital solver. This method eliminates the input bias and gain error but introduces measurement noise. As described in section 6.3.5, the voltage can be measured with an accuracy that is usually better then 1 mV.

Experimental results Fig. 6.11 shows the optimization variable values as measured on the board and the values obtained with a digital solver vs sample number. The input has a sine wave form and some of the variables follow this form. There is a clear active set change when $v19$ hits a low constraint. Some variable have a small consistent bias, such as $v13$ and $v10$. Because of this bias the digital solution for $v10$ hits a constraint at sample 110, while the analog does not. This difference is propagated to $v13$, $v5$ and $v2$ that exhibit slightly different behavior at this time.

Overall, Fig. 6.11 shows a good match between analog and digital solutions (output variables). The input variables are shown in Fig. A.1 in the Appendix. The histogram of distribution of the mismatch between the analog and digital is shown in Fig. 6.12. The distribution has a standard deviation of 1.4 mV out of a dynamic range of roughly $200mV$. This is roughly equivalent to 0.7% average accuracy.

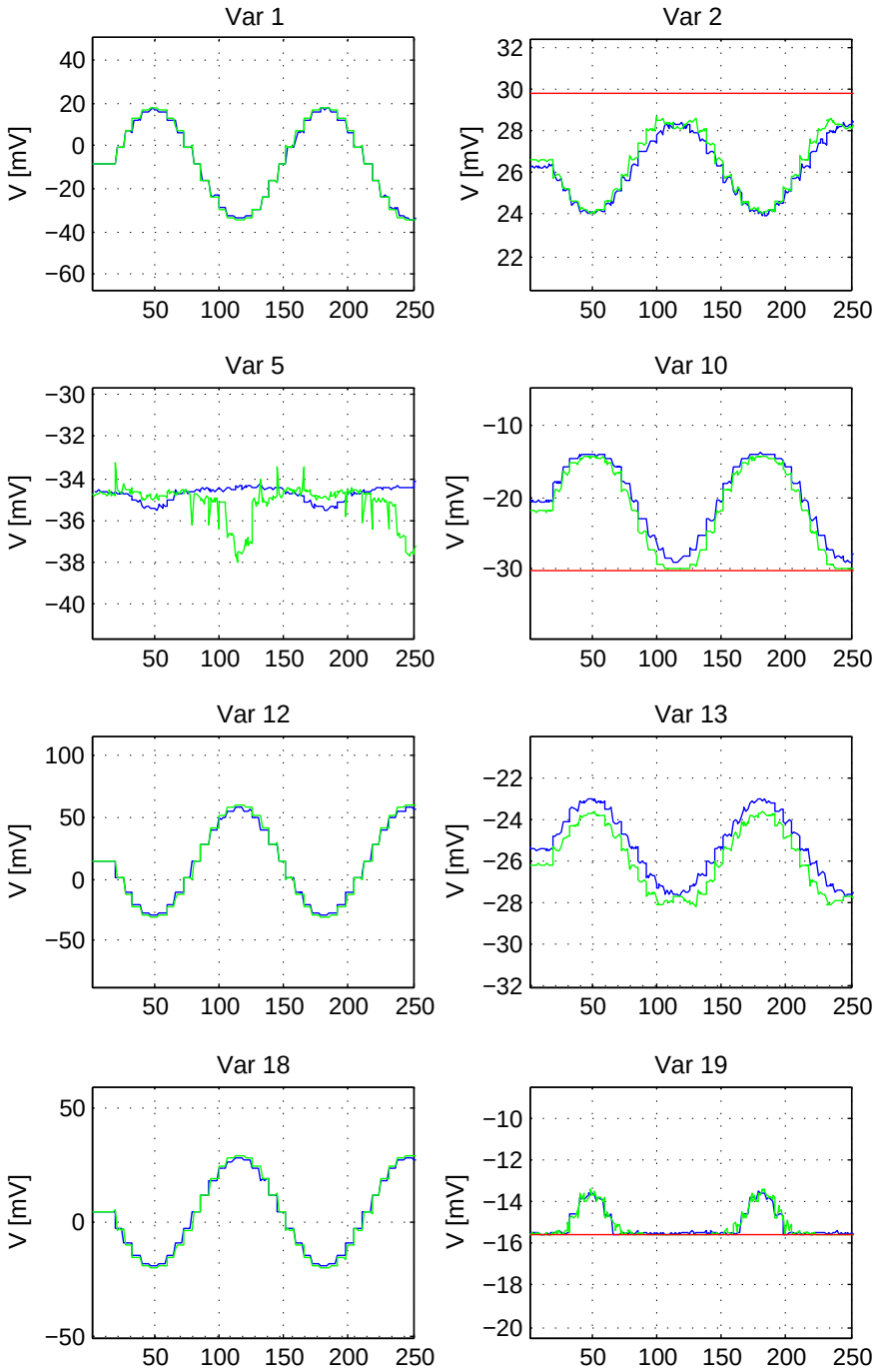


Figure 6.11: Comparison of analog and digtial solutions. Blue line is digtial and green is analog. Red line shows constraints.

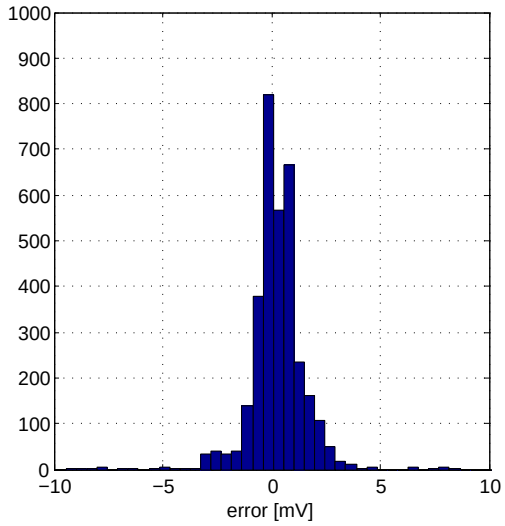


Figure 6.12: Histogram of the difference between analog and digital solutions.

6.4.2 Closed loop hardware-in-the-loop (HIL) experiment.

Experiment setup For this experiment the board is wired to a digital to analog (D/A) converter that sets the 6 input variables of the board and its output variables are sampled by an analog to digital (A/D) converter. The D/A and A/D converters are controlled by a PC running Matlab software. A simulation of the DC-DC converter (6.1) is running in Matlab. It is controlled by the output of the optimization board and the measured state of the plant is transferred to the optimization board via the D/A converter.

This QP problem is solved by the board and its solution is sampled and is fed to the simulation.

Experimental results Fig. 6.13 shows the output of the buck DC-DC converter (that is the capacitor voltage u_C) in closed loop scenario. The reference voltage is 5 V, the initial voltage is 4.5 V and there is a step in load resistance $R_{\texttt{load}}$ in $t = 1$ ms. The effect of 100 KHz PWM frequency can be seen on the u_C line as a high frequency signal riding on the lower frequency. The steady state voltage in steady state is higher then the desired reference voltage, because of inaccuracies due to a discretization in potentiometer settings as described in the sequel.

Fig. 6.14 compares three methods of computing the duty cycle command. The red line is the output of the analog optimization board, the green dashed line is the output of a digital solver for the required FTOC problem (6.3). However, due to a discrete nature of the digital potentiometers on the board it is impossible to represent this problem exactly. The Arduino software reports the value of all the calibrated potentiometers, and a QP problem can be constructed that represents the QP implemented by the board. The coefficients of the implemented FTOC problem are listed in (A.4) in the Appendix. The blue dash-dot line is the digital solution of the implemented QP problem.

As can be seen in Fig. 6.14, there exists a significant bias between the analog and the required digital solution. A significant portion of the bias is explained by the potentiometer discretization effect, since the implemented QP solution almost coincide with the analog. Therefore, the unaccounted error is only the difference between the implemented and the analog curves in Fig. 6.14.

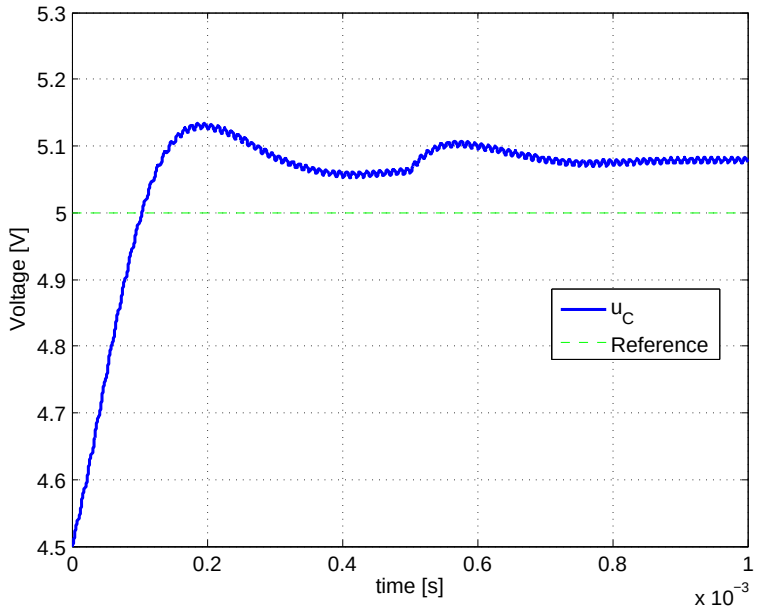


Figure 6.13: Output of a buck DC-DC converter in closed loop control by the analog optimization board.

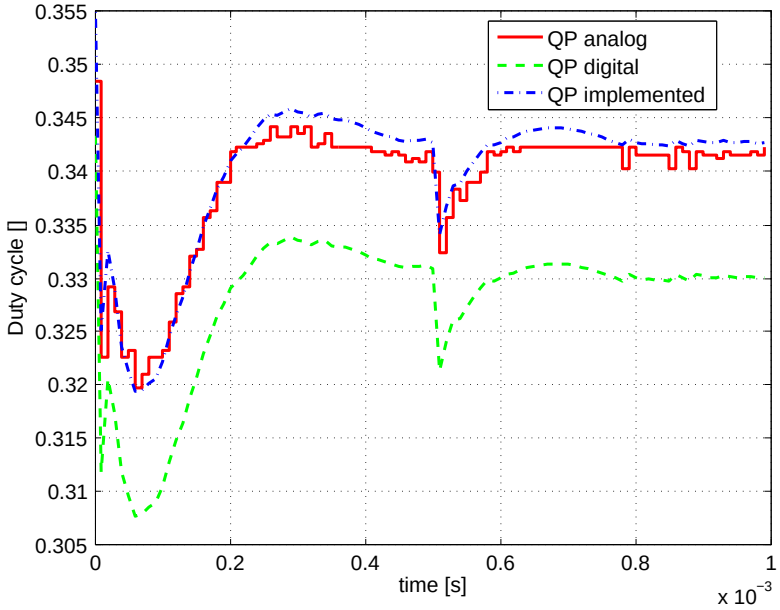


Figure 6.14: Duty cycle command as computed by the analog optimization board, by an exact digital solver and by a digital solver using the implemented resistance values.

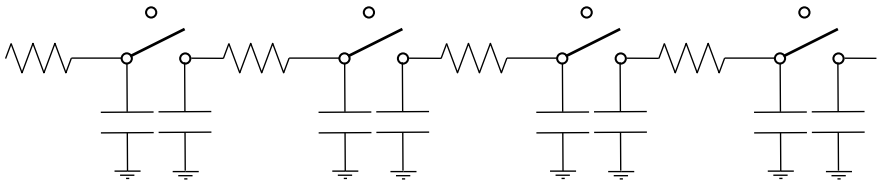


Figure 6.15: Schematics of a digital potentiometer.

6.4.3 Main challenges and limitations

We discovered two main phenomena that affected the performance of the board. Both stem from usage of digital potentiometers as the main component. A digital potentiometer is a resistor ladder with CMOS switches connecting the resistors as shown in Fig. 6.15. CMOS switches have significant parasitic capacitance and a non-linear resistance due to semiconductor effects. However, digital switches allow software only calibration that can be done automatically. Since the board includes 152 potentiometers manual calibration is impractical.

6.4.3.1 Non-linearity of the potentiometer

For a fixed setting, a potentiometer is generally assumed to behave as a resistor, thus, the current voltage curve is linear. This is the case for mechanical potentiometers. However, digital potentiometers have many CMOS switches in series with resistors as shown in Fig. 6.15 and, consequently, may exhibit non-linear behavior. Indeed, the AD5144 digital potentiometers are found to have non-linear current voltage curve.

In order to check non-linearity of the potentiometer we conducted an experiment: two potentiometers, A and B, are connected in series to a varying voltage source and voltage drop on each of them is measured with external voltmeters. If the potentiometers were linear, the ratio of voltage drop on A to the drop on B ($\frac{\Delta V_A}{\Delta V_B}$) would be constant. Experiment results are shown on Fig. 6.16. The figure shows the deviation from a constant of $\frac{\Delta V_A}{\Delta V_B}$. For low currents (less than $1mA$), the non linearity is very small, however, for larger currents the non-linearity increases up to 0.8%. Worst case measurement error due to voltmeter inaccuracies is shown as red dashed line. As can be seen, the non-linearity is clearly above any measurement error. The AD5144 device is rated for $6mA$ current [1], but the nonlinearity is substantial already at $2mA$. Therefore, we conclude that the digital potentiometer has a significant non-linear behavior for currents greater than $1mA$.

This potentiometer non-linearity is the main source of error in constraint satisfaction. An experiment was conducted to measure the accuracy of a negative resistance as implemented in Fig. 6.3. In this experiment all variables of a calibrated equality constraint are connected to a current source as shown in Fig. 6.17a. The voltage at point A in Fig. 6.17a is expected to be zero, since the total resistance from the point A to the ground on the right is zero. This voltage is measured for range of currents and the result is plotted in Fig. 6.17b. As shown, the voltage is indeed zero for a range of current values, but is substantially different

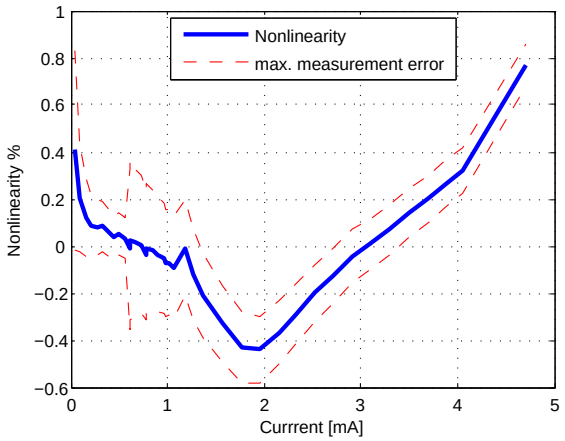
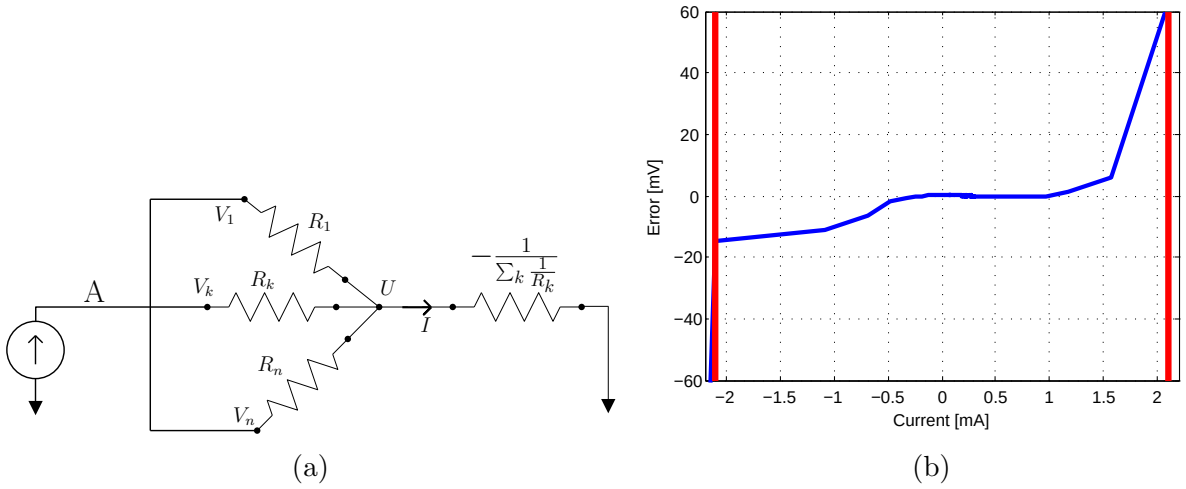


Figure 6.16: Nonlinearity of AD5144 potentiometer.



(a) (b)

Figure 6.17: (a) Circuit for the non-linearity experiment. (b) Negative resistance non-linearity.

from zero for larger currents. A voltage of over $10mV$ is observed for a large portion of admissible currents. The plot is limited from left and right by saturation of an opamp that implements the negative resistance. As can be seen, the error appears far away from the saturation limit.

For this experiment, negative resistance was equal to 1024Ω. Therefore, every 0.1% of non-linearity results in 1Ω mismatch. Consequently, a current of $1mA$ yields $1mV$ error. The error shown in Fig. 6.17b is explained by non-linearity of about 0.8% for negative currents or larger positive currents.

The error curve at Fig. 6.17b provides a hint on how to partially overcome this phenomenon. If we can limit the circuit to stay at the linear zone ($|I| < 0.5mA$), the constraint

Table 6.2: Capacitances of AD5144 potentiometer.

Potentiometer	C_A	C_W	C_{in}
$10K\Omega$	$25pF$	$12pF$	$34pF$
$100K\Omega$	$12pF$	$5pF$	$27pF$

will be satisfied with good accuracy. This solution is only partial, since the design of the board requires a larger dynamic range to handle the full range of input variables. Better solution should solve the non-linearity problem by better selection of the components when especial attention is given to non-linearities.

6.4.3.2 Bandwidth limits imposed by parasitic capacitance.

In this subsection we analyze the mechanisms that limit the bandwidth of the optimization board. The speed of an analog optimization system is set by the time it takes for a circuit to reach an equilibrium. As it was shown in section 5.4 the speed of an operational amplifier in equality constraint is set by $\texttt{GBWP} < \frac{2\pi\gamma_{\texttt{crit}}}{RC}$. Therefore, the most important constant parameter is the RC time constant of the circuit. The resistance is tightly controlled and calibrated. In contrast, the capacitance originates from parasitic effects and it is hard to predict.

In the PCB board the parasitic capacitance originates from the following sources

1. Capacitance inherent to the digital potentiometers.
2. Trace capacitance of the PCB board
3. Input capacitance of switches and opamps.

Some of the above capacitances were known in the design phase, and some were discovered at later phase.

Potentiometer capacitance. According to [1], the AD5144 potentiometer has a terminal parasitic capacitance of $12pF$ for $100K\Omega$ or $25pF$ for $10K\Omega$ version. In addition, there is an internal capacitance that was unaccounted for in the design phase. For the analysis a simplified potentiometer model is used as shown in Fig. 6.18. The model includes terminal capacitances on terminals A and W, and an internal capacitance marked as C_{in}. This internal capacitance can be identified using bandwidth data from [1] that is shown in Fig. 6.19. The model assumes that $R_{p1} = R_{p2} = \frac{R_p}{2}$, where R_p is the potentiometer value. The parameters are summarized in Table 6.2.

Trace capacitance. According to Chapter 5 the dynamical response of the circuit depends on the capacitance of a node that connects the negative resistance to positive resistances (the point α in Fig. 3.1). The trace that represents this node in the PCB board has a length

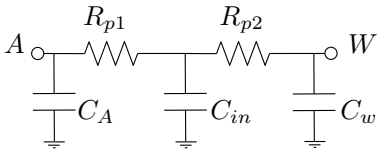


Figure 6.18: PotModel.

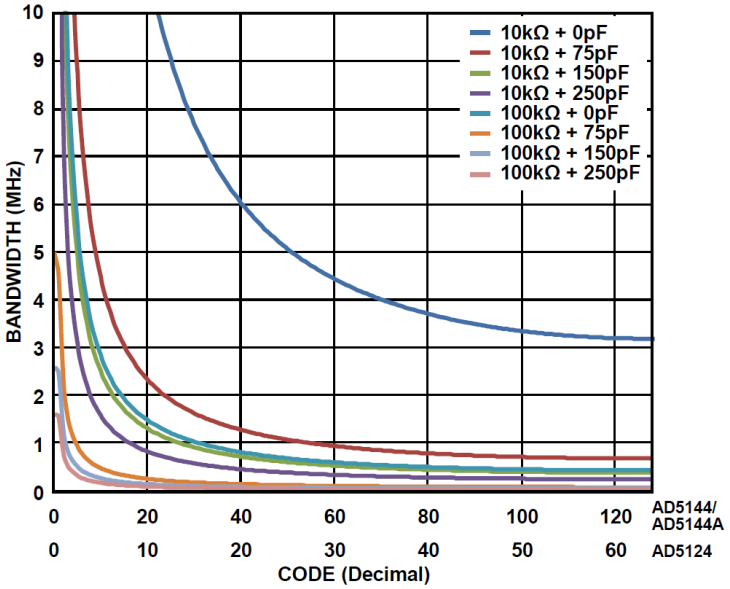


Figure 6.19: Maximum bandwidth of AD5144 vs. Code vs. Net Capacitance, from [1].

Table 6.3: Input capacitances.

Component	Input cap. in ON state	Input cap. in OFF state	notes
Opamp TLE2037A	$8pF$	–	from [93]
Multiplexer ADG1438	$286pF$	$58pF$	from [2]
Switch ADG714	$22pF$	$11pF$	from [4]

of 235 mm, average width of 0.15 mm and is located between two other signal layers each separated by 0.3 mm with a relative permittivity of the dielectric equals to 4.3. This yields an estimate of trace capacitance of $25pF$.

Input capacitances. There is an additional capacitance in the input ports of the operational amplifier, switch and multiplexer. The capacitances are summarized in Table 6.3.

Bandwidth analysis by simulaiton and experiment. The step response of an optimization circuit can be modeled using a model in Fig. 6.20 that is a simplified version of the equality constraint in Fig. 6.3. The model was created and simulated using TINA-TI SPICE

simulation software [92]. In the simplified model potentiometers are replaced with the model in Fig. 6.18, additional parasitic capacitance are added to simulate the effect of trace and input capacitances. The model uses a library model of TLE2037 amplifier. The system input is a step function Vin that represents a state variable set by an external system. The output is the voltage Vout that represents a free optimization variable. This model captures the main dynamical properties of the circuit, although it has only one equality constraint and no cost function components.

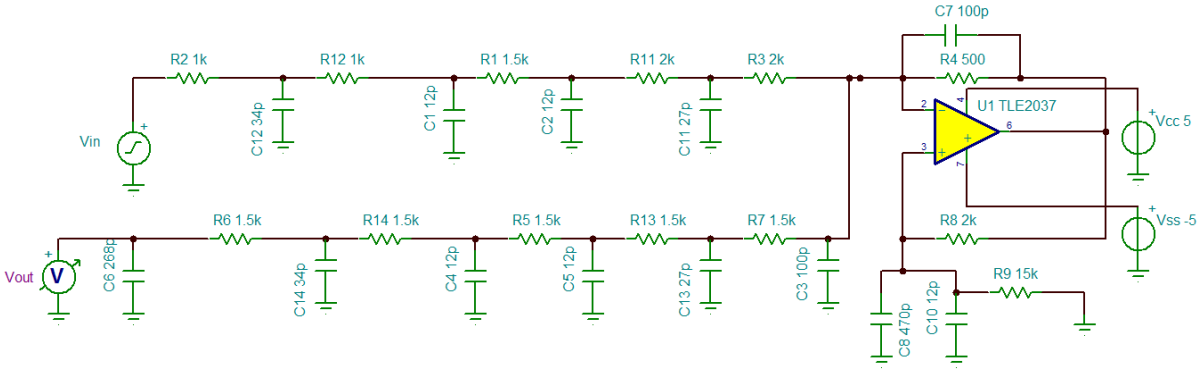


Figure 6.20: Simplified dynamical model of full equality consraint using TINA-TI.

Fig. 6.21 shows the step response of the model in Fig. 6.20. The original design goal curve (solid blue) shows the initial expected performance. However, after the board was manufactured, it showed non-stable behavior due to unaccounted capacitances. In order to stabilize the board, additional compensating capacitance was added to feedback loops of the opamp (C7 and C8 in Fig. 6.20). Consequently, the step response was slowed and the "current board" line (dashed green) shows the performance after all the information that was learned about parasitic capacitances was added to the model in Fig. 6.20. This step response has a settling time of about 50 μs. Fig. 6.22 shows the measured step response of the board as captured by an oscilloscope. The real step response has a longer settling time of about 80 μs, which can be explained by additional unaccounted capacitances and interaction with other equality constraints and cost circuits.

An additional offline "design iteration" with the learned capacitance values yields the step response that is shown in Fig. 6.21 with red dash-dot line. In this design R4 and R8 are set to $1K\Omega$, R9 to $3.75K\Omega$, C8 is set to $1.1nF$ and C7 to $1pF$. This design demonstrates that better performance is achievable with parameter tuning, although the original goal (blue line) is beyond the reach without a major redesign that reduces parasitic capacitance.

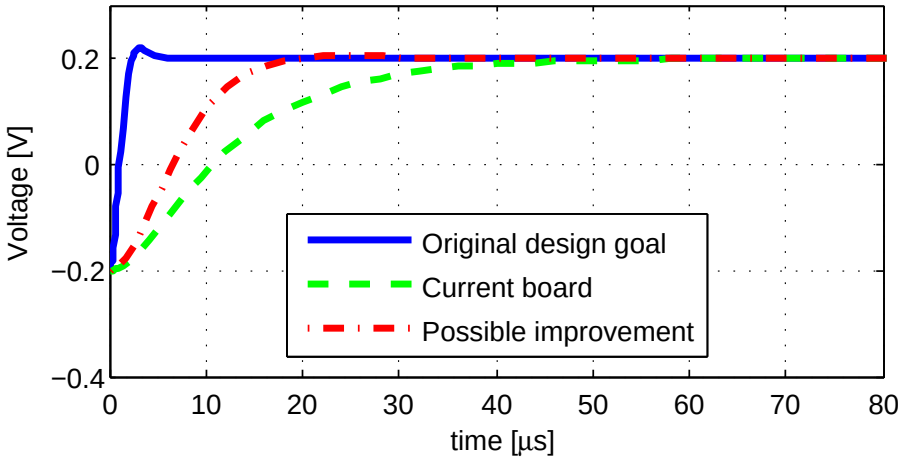


Figure 6.21: Simulation of step response of the model 6.20.

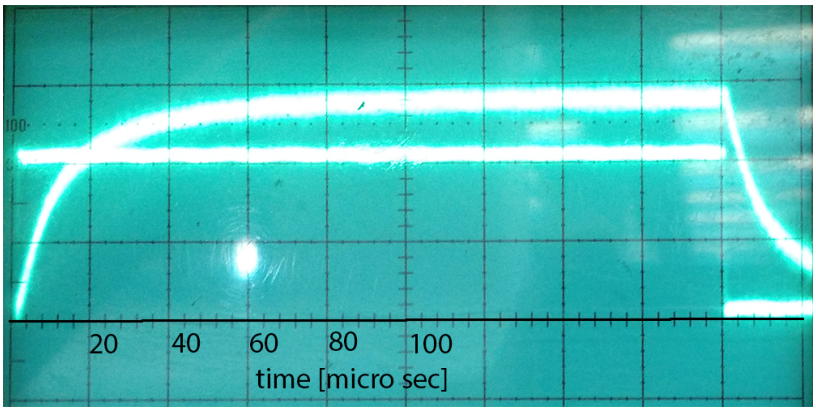


Figure 6.22: Step response of the board as captured with an oscilloscope.

6.5 Conclusion

In this chapter a prototype analog optimization PCB board was described and studied. The board was designed for configurability to solve various optimization problems. In the trade-off between performance and flexibility the flexibility was preferred, and digital potentiometer was selected as the main building block. Therefore, the prototype board demonstrates only a lower bound for performance achievable with this methodology.

In spite of the fact that the performance was not the main goal, the prototype demonstrates excellent (better than 1%) accuracy performance, was used in closed loop control of a simulated buck DC-DC converter and exhibits 80 μs convergence time. This proves that the method is realizable with current technology and the theory correctly predicts real life behavior.

However, this work highlighted the significant challenges in designing analog optimizers.

When high accuracy is desired, the design must account for non-linear effects. For instance, the board cannot maintain its accuracy for the whole dynamic range because of non-linearity of resistance in potentiometers. In addition, when high speed is desired, the design must minimize parasitic capacitance because of its major effect on a solution time.

Chapter 7

Analog VLSI chip implementation

This chapter studies the feasibility of very high speed implementation of the optimization circuit using Very Large Scale Integration (VLSI) technology. In VLSI, all the required circuit components are built on top of a silicon substrate using advanced photo-lithographic technologies. Analog VLSI circuits are fast, small and cheap. However, there are significant challenges in analog VLSI design due to the very small size that produces significant tolerances and parasitic effects.

The theory developed in Chapters 3, 4 and 5 uses a resistor as the main circuit component. However, other elements, such as capacitor, may be used for the basic element. Capacitors are very popular in analog VLSI designs, since it is possible to manufacture capacitors with tolerances better than resistor tolerances, capacitors do not generate thermal noise and do not consume power at steady state.

Section 7.1 describes a feasibility study of resistor based analog VLSI design. Section 7.2 proposes the design of a capacitor based circuit instead of resistor in analog optimization circuit. Section 7.3 presents the main results of a detailed design of capacitor based optimization circuit using $65nm$ technology, which was done by Kristel Deems and is detailed in her Master thesis [25].

7.1 Resistor based VLSI design

In this section an analog VLSI design of a high speed linear optimization circuit is carried out. The target technology is CMOS 45nm, with 1 V voltage. We assume dynamic range of $\pm 50mV$ for variable nodes and $\pm 200mV$ for constraint nodes.

We require accuracy of 1%. Resistors can be produced with relative accuracy of 0.5%. Therefore, the rest of the circuit should contribute errors less than 0.5%. Therefore, we allocate 0.1% to amplifier induced negative resistance error. The circuit should function at $1GHz$ speed, and this is the required closed loop bandwidth from the amplifier. The resistors should be large, in order to reduce power consumption, therefore we use representative value of $100K\Omega$.

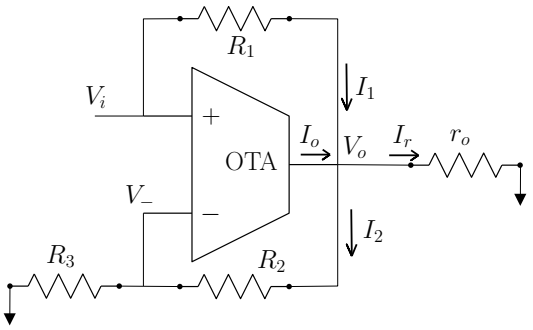


Figure 7.1: Negative resistance implementation with OTA.

7.1.1 Negative resistance top level design

The negative resistance is implemented with the circuit shown in Fig. 7.1. Using KCL, KVL and Operational Transconductance Amplifier (OTA) laws we can show that the voltage gain is given by

$$Av_0 = g_m \alpha R_e > \frac{1}{\epsilon}\left(\alpha \frac{2+K+K^2}{K^2} + \frac{(1+K)^2}{K}\right), \tag{7.1}$$

where Av_0 is the voltage DC gain, g_m is the transconductance of the amplifier, ϵ is the required error, R_e is the equivalent resistance value, and

$$R_1 = KR_e,\ R_2 = K^2 R_e,\ R_3 = KR_e \tag{7.2}$$

$$\alpha = \frac{R_e}{r_0} \tag{7.3}$$

with R_1, R_2, R_3, r_0 as shown in Fig. 7.1.

The amplifier must generate enough current to maintain equilibrium for the largest signal swing. Suppose that g_m is big enough and V_i is very close to V_-, then the equilibrium currents are

$$I_1 = -\frac{V_i}{R_e} \tag{7.4}$$

$$I_2 = \frac{(1+K)V_i - V_i}{R_2} = \frac{V_i}{KR_e} \tag{7.5}$$

$$I_o = \frac{V_i}{R_e}\frac{1+K}{K}. \tag{7.6}$$

The power consumption of the negative resistance consists of energy that is dissipated in the resistors and energy consumption of the amplifier. Energy consumption of the amplifier depends on the specific design and is treated in amplifier design section. Total power

dissipation in the resistors is given by

$$P = \frac{V_i^2}{R_e}K + \frac{V_i^2}{R_e} + \frac{V_i^2}{KR_e} = \frac{V_i^2}{R_e}\left(K + 1 + \frac{1}{K}\right). \tag{7.7}$$

The power is minimal when $K = 1$.

For bandwidth requirements, we assume simplified 1-st order model of the amplifier

$$\frac{I_o}{\Delta V_i}(s) = \frac{g_m}{1 + \frac{s}{p}} \tag{7.8}$$

where p is the dominant pole of the amplifier. Suppose the required bandwidth is ω_{cl}, then the open loop dominant pole has to be at

$$p = \frac{\omega_{cl}}{Fg_m} = \omega_{cl}\frac{\epsilon K}{\alpha}\frac{K^2 + K + \alpha(2 + K)}{2 + K + K^2}. \tag{7.9}$$

7.1.1.1 Summary of amplifier requirements

Using equation (7.1), (7.6), and (7.9) we can derive amplifier requirements as shown in Table 7.1. The first part of the table shows the top-level parameters and requirements allocations and the second part of the table lists amplifier parameters, that were calculated from the top-level requirements. Another very important requirement is the common mode rejection. This requirement can be expressed as the ratio between differential mode gain and common mode gain, or as the value of differential signal that is required to compensate the common mode signal. The later form is easier to validate in simulation and is shown in the table as ΔV_{CM}.

7.1.2 Amplifier design for the negative resistance

7.1.2.1 Amplifier topology

The requirements in Table 7.1 include a non-standard combination of very high value for g_m and low steady state output current. The required bandwidth is relatively low. The main challenge in selecting the topology and design was high input swing, high gain and high common mode rejection. After many tested topologies - cascode, fully differential, fully differential cascode, 3 stages we selected the simple dual stage differential amplifier as shown in Figure 7.2. In this amplifier the first stage is NMOS and the second stage is PMOS. This topology is found to provide the best performance.

7.1.2.2 Design

The total G_m and the output resistance of the dual stage amplifier is given by

$$G_m = g_{m2}(r_{02}||r_{05})g_{m7} \tag{7.10}$$

$$r_0 = r_{06}||r_{07} \tag{7.11}$$

Table 7.1: Requirements from the amplifier

Name	Value	Units
R_e	100	$K\Omega$
ϵ	0.4%	
α	1	
K	0.5	
ω_{cl}	500	MHz
V_i	0.2	V
ΔV_{CM}	0.5	mV
g_m	0.0388	A/V
Av_0	3875	
DC I_o	$6 \cdot 10^{-6}$	A
p	$7.4 \cdot 10^6$	rad/s
ω_p	1.18	MHz
r_0	100	$K\Omega$

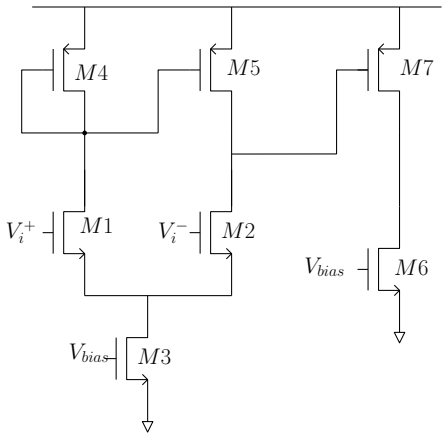


Figure 7.2: Two stage differential amplifier

The Table 7.3 shows the geometry of the devices and the resulted performances based on Cadence simulation.

The 2-stage amplifier was implemented in CAD as shown in Figure 7.3. Open loop responses are shown in Figure 7.4. The performances from this plot are summarized in Table 7.3. As can be seen it was impossible to meet all the requirements, the main discrepancy is the required bandwidth. The amplifier is roughly two times slower that the requirement.

7.1.2.3 Negative resistance

The negative resistance was implemented as shown in Figure 7.1. The performance of the negative resistor block were evaluated in DC and AC mode. Figure 7.5 presents the current

Table 7.2: Amplifier sizing

Name	Value	Units
$L_{M1,M2,M4,M5,M6,M7}$	250	nm
L_{M3}	375	nm
W_{stage1}	200	nm
W_{stage2}	1000	nm
Av_0	3900	Gain
ω_p	500	KHz. Dominant pole
ΔV_{CM}	0.55	mV

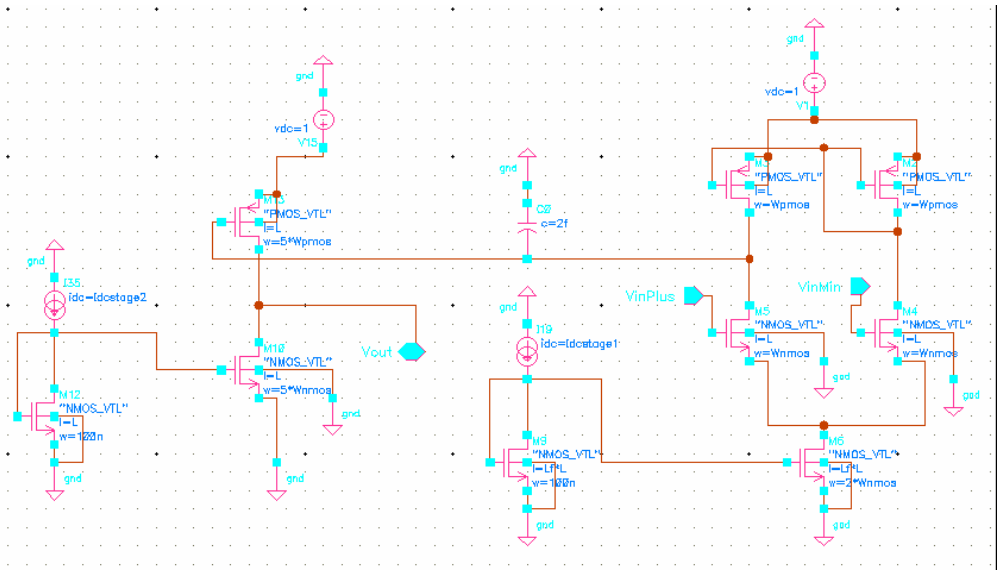


Figure 7.3: Dual stage amplifier.

for all the required input swing. The current line is linear and has the same properties for all input voltages. To quantify the performance an error in current was computed and presented at Figure 7.6. The error is less the 12.5 nA for all input voltages. This value is equivalent to 0.62% of the maximum current, that is very close to the requirement of 0.4%.

The AC response in Figure 7.5 shows unusual behavior around 1 GHz frequency. In this region a transition occurs from low frequency response that is dominated by the amplifier to high frequency response that bypasses the amplifier via the direct resistor connections. The system has a RHP zero due to existence of direct resistor only path. The zero is RHP because the resistor path has positive resistance, in juxtaposition to the negative amplifier path. As well the high-frequency gain is two times higher then the low frequency, since the former is created by R_1 that is two times smaller than R_e. This type of behavior makes it impossible to determine exactly the bandwidth. However, the bandwidth appears to be in hundreds of megahertz range.

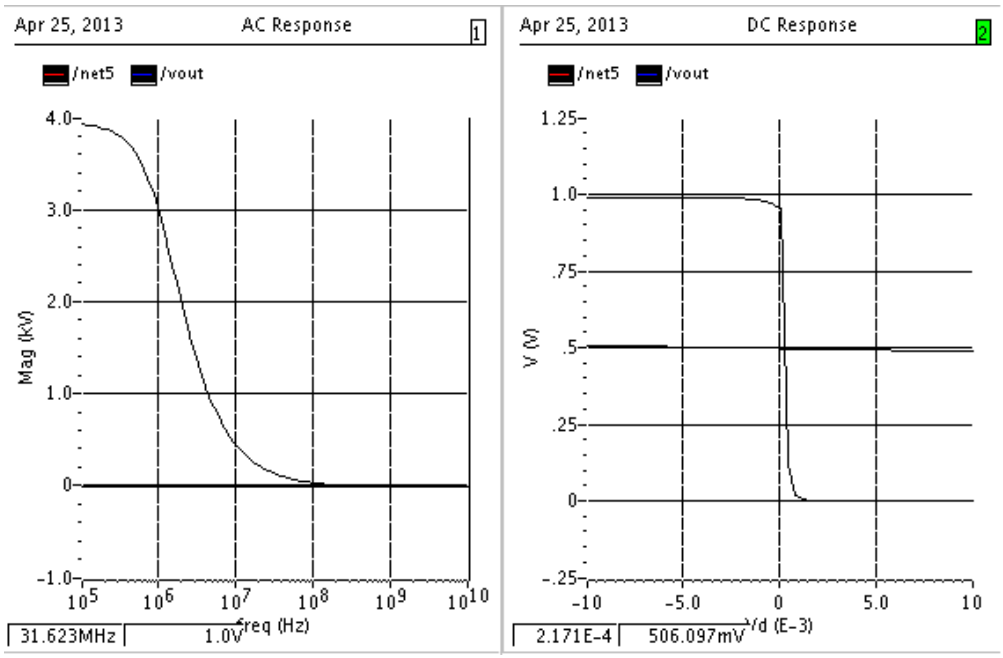


Figure 7.4: AC and DC response of the amplifier

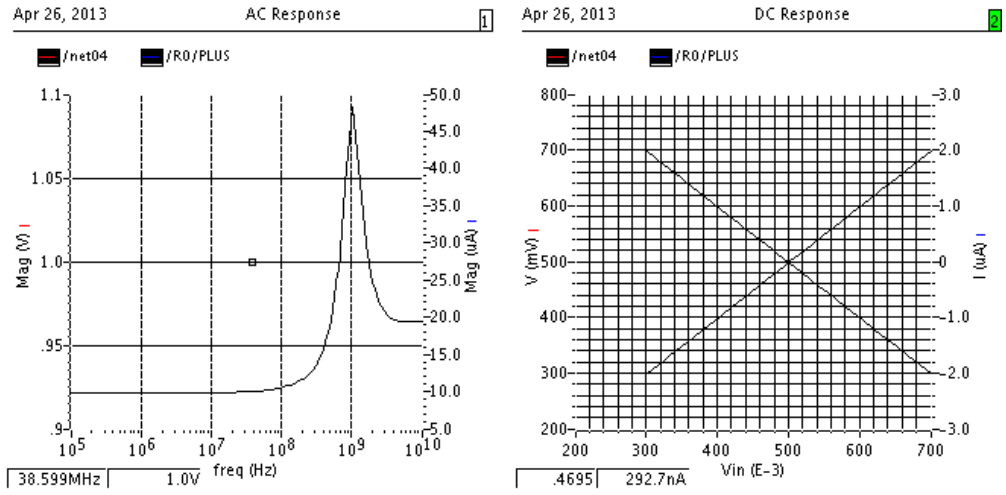


Figure 7.5: The negative resistance AC and DC response

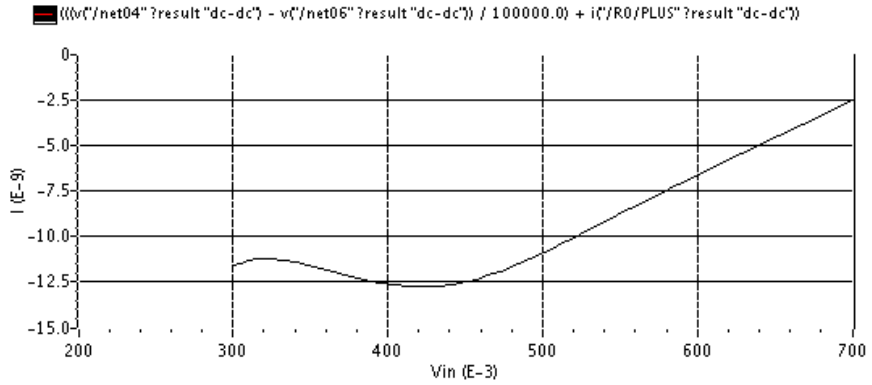


Figure 7.6: Error of negative resistant current. The error is less then 15 nA.

7.1.2.4 A basic LP

The negative resistance was used to create the simplest possible LP:

$$\begin{aligned} &\min_{x_1,x_2} 0 \\ &s.t.\ x_1 + x_2 = 0 \\ &\quad x_1 = V_{ref} \end{aligned} \tag{7.12}$$

The circuit in Figure 7.7 solves the above problem. In this circuit we vary the input voltage V_{ref} from $450mV$ to $550mV$. The variable x_2 should hold the negative with reference to $500mV$ value. The error of this value is shown in Figure 7.8. The dynamic range of variables is $100mV$, the error is bounded by $500\mu V$. Therefore the total error is less then 0.5% as required.

Dynamic properties of the circuit were analyzed the result is shown in Figure 7.9. The right plot shows the AC characteristics of the transfer function $\frac{x_2}{V_{ref}}(s)$. Appropriate and expected behavior can be observed. The bandwidth of the circuit is about 300 MHz, that is slightly below the requirements, but this was expected, since the amplifier is slower than required.

The step response is shown on the left of Figure 7.9. Rise time of less then 2 nanoseconds is observed. The settling time is 8 nanoseconds. Overall the step behavior is good.

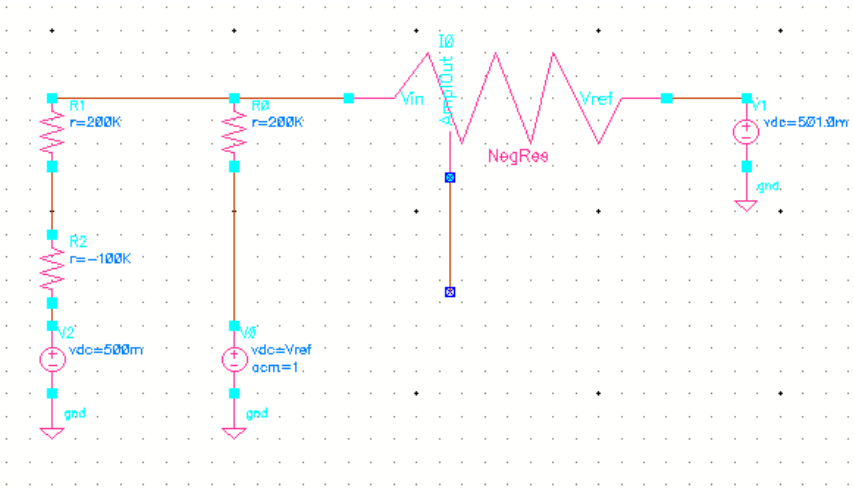


Figure 7.7: The circuit for LP (7.12)

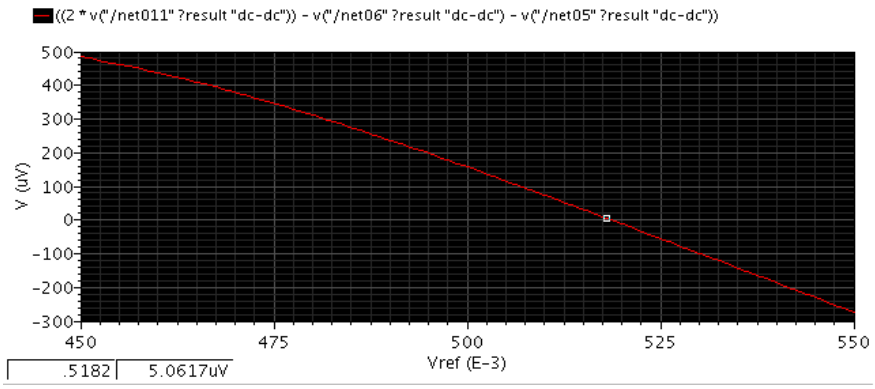


Figure 7.8: Error of x_2 computation in LP (7.12).

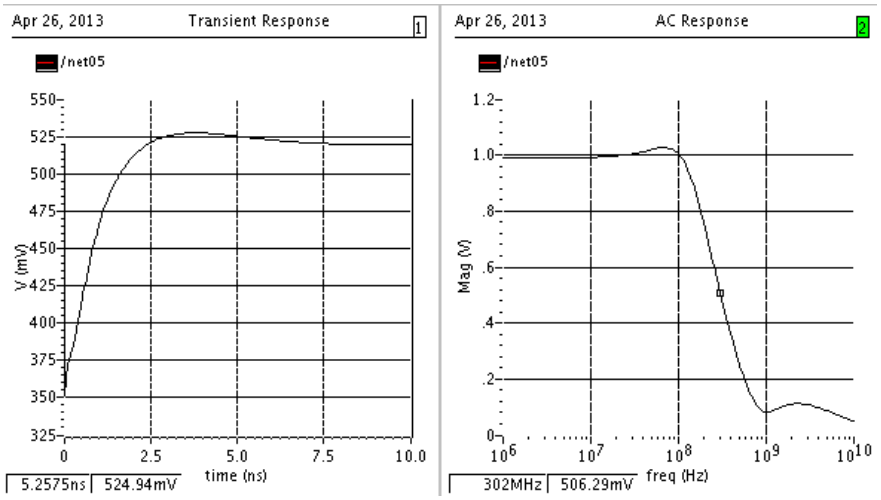


Figure 7.9: Step response and AC response of the LP circuit.

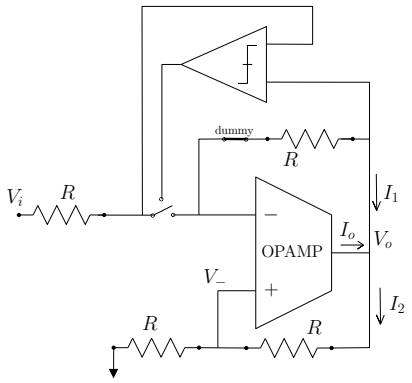


Figure 7.10: Negative resistance circuit with the diode model in feedback

7.1.3 Inequality circuit: Negative resistance with active diode

An inequality circuit as in Fig. 3.3 includes a diode. A real diode has an uncertain voltage drop that degrades the accuracy of a circuit. For this reason an active circuit that mimics an ideal diode behavior is used. The proposed topology is shown in Figure 7.10. In this topology the comparator is connected to both ends of resistor R_1. This connection improves the sensitivity of the comparator because the voltage drop on R_1 is bigger than the drop on the switch alone. The switch is positioned on the input node. Initial design had the switch on R_1 feedback, but this feedback must remain closed for stability. The negative resistance is very sensitive to impedance matching between the stable and the unstable feedbacks. When the active diode is connected to the "minus" port of the amplifier it adds parasitic capacitance that we must compensate by a similar or larger capacitance on the "plus" port. Without the compensation, the amplifier may be unstable.

The active diode is includes 3 main elements

1. Comparator
2. Switch
3. Dummy switch that is placed in the feedback line to compensate the resistance of the main switch.

7.1.3.1 Comparator

The comparator is has the same topology as the differential amplifier that is shown in Figure 7.2. The sizing is different, because in the comparator case we can trade gain for more speed.

The comparator performance are similar to performance of the differential amplifier. Due to shorter device length, the comparator has higher bandwidth then the amplifier.

Table 7.3: Comparator sizing

Name	Value	Units
$L_{M1,M2,M4,M5,M6,M7}$	60	nm
L_{M3}	360	nm
W_{stage1}	200	nm
W_{stage2}	1000	nm

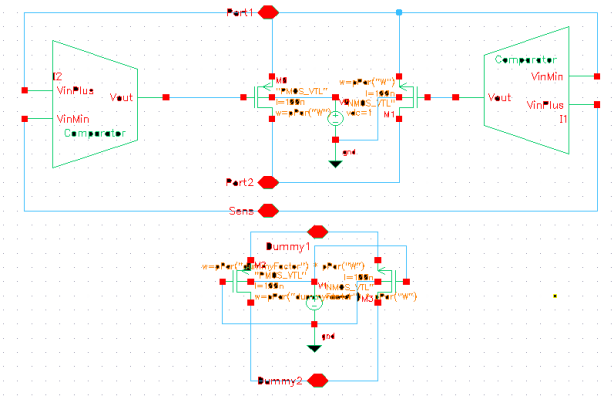


Figure 7.11: Active Diode

7.1.3.2 Switch

The switch is required to operate from 0.3 to 0.7 V. In order to achieve low resistance in all range dual NMOS/PMOS switch with dimensions $100/1000nm$ is used.

7.1.3.3 Dummy switch

The sizing of the dummy switch is different from the main switch, since any resistance of value KR placed in the R_1 feedback yield $-R$ negative resistance. In order to compensate the resistance of the main switch, the dummy switch must have width larger by $\frac{1}{K}$.

7.1.3.4 Active diode schematics

The active diode schematics is shown in Figure 7.11. As can be seen, two comparators with switched polarity are used to drive the NMOS and PMOS transistors.

7.1.3.5 Performance of Negative Resistance with Active Diode

An example of currents and voltage is shown in Figure 7.12. The plot show transient response when the input voltage changes from an active zone, when the diode is on, to inactive zone, when the diode is off. The current ("/I7/Vin") initially has a linear negative slope, when the voltage crosses $500mv$, which is the reference voltage, the current stays zero. A small

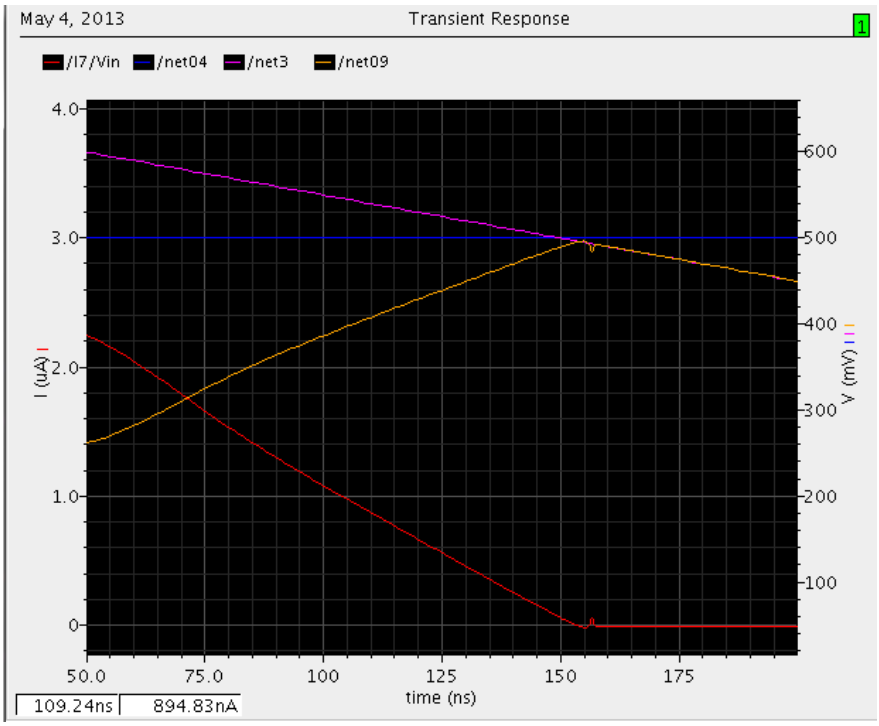


Figure 7.12: Transient response to a ramp voltage of negative resistance with active diode

disturbance can be seen at the switching moment. This disturbance is due to time delay of the comparators and due to charge injection when the switches are closed.

7.1.4 Integration of all circuit elements

Consider the following LP

$$\min_{V_1,V_2,V_3} V_1 \tag{7.13a}$$

$$\text{s.t.} \quad V_1 + V_2 = 0.5 \tag{7.13b}$$

$$\frac{V_3}{3} + \frac{V_2}{1.5} \leq 0.53 \tag{7.13c}$$

$$V_3 = V_{ext} \tag{7.13d}$$

where $V_{ext} = 0.5 + 0.02\sin(\omega t)$ with $\omega = 100\text{MHz}$. This LP is implemented using a circuit that is shown in Figure 7.13. This circuit includes one equality constraint, one inequality constraint and the cost circuit. The variable V_3 is connected to a controlled voltage source that generates the sine wave.

The transient simulation of the circuit is shown in Figure 7.14. As can be seen V_3 oscillates between 0.52 to 0.48 volt, V_2 has half magnitude and satisfies in every time point (7.13c). A

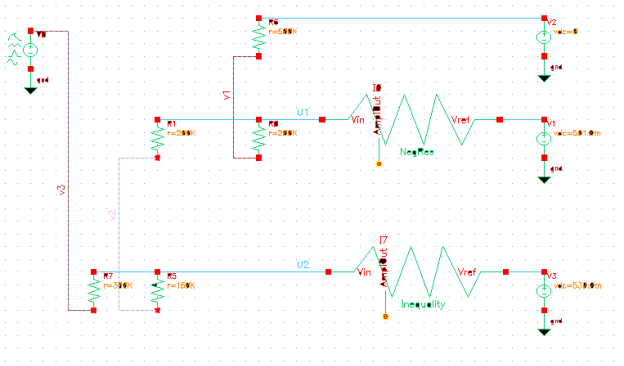


Figure 7.13: Schematics of LP (7.13)

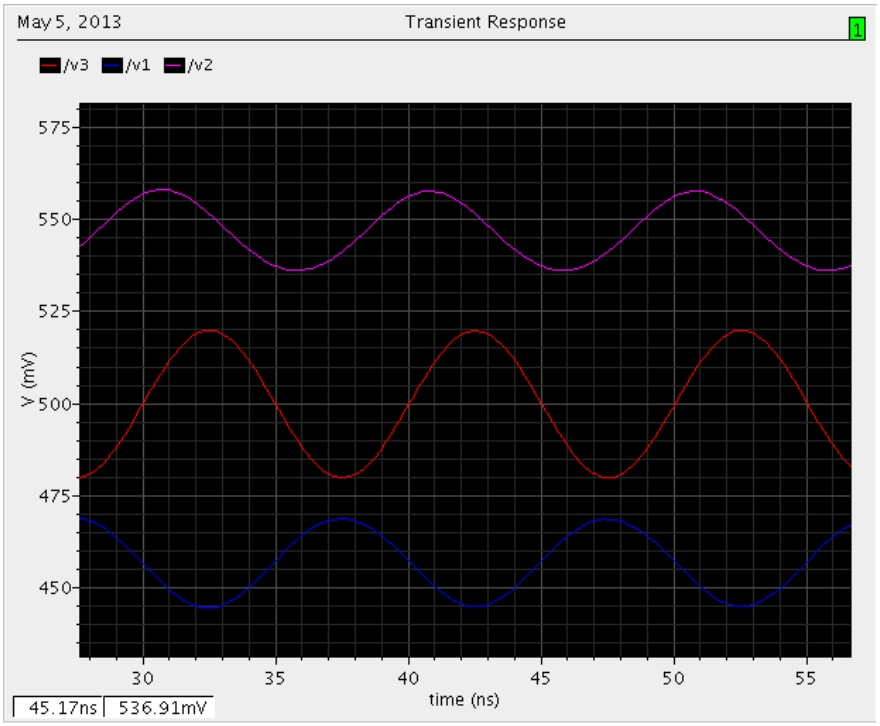


Figure 7.14: Simulation results of LP (7.13). 100 MHz input.

phase shift of about $2ns$ can be observed between V_3 and V_2. V_1 is mirrored w.r.t. 0.5 V. A similar phase shift of about $2ns$ can be observed from V_2 to V_1.

The LP (7.13) has an explicit solution.

$$V_2 = (0.530 - V_3/3)1.5 = 0.545 - 0.01\sin(\omega t) \tag{7.14}$$

$$V_1 = 0.455 + 0.01\sin(\omega t) \tag{7.15}$$

The plots in Figure 7.14 are very similat to the explicit solution.

7.1.5 Conclusion

In this section a circuit that solves LP was designed and evaluated. Detailed design of the amplifier was performed using the Cadence VLSI design toolchain. A negative resistance module was created and tested. Moreover, a simple version of LP circuit was designed and tested using the equality constraints only.

An active diode element was developed. In the next phase an inequality was designed using the negative resistor and the active diode. A simple LP that includes inequality, equality and cost function was generated using all the basic blocks: negative resistors, active diodes and regular resistors. The designed LP was evaluated using 100 MHz signal. The circuit handles successfully such high frequency signal and yields results with 4 ns delay and 2-3 mV (2%-3%) accuracy.

This work demonstrates the feasibility of constructing high speed LP solver on CMOS technology. The main challenges are the trade-offs between speed, accuracy and power consumption. The design does not account for the parasitic effects, such as parasitic capacitance and resistance that present in a real hardware implementation. Such an analysis requires a detailed circuit layout and it will be presented in section 7.3.

7.2 Capacitor variant of the optimization circuit

The main contribution of this section is an analog optimization circuit based on capacitors instead of resistors. Similarly to the original circuit as is shown in Section 3.2, capacitor based circuit version can be developed. The capacitor version is driven by an observation that the triple voltage (U), current (I) and resistance (R) are similar to the triple voltage (U), charge (q) and capacitance (C), since $U = IR$ and $U = q/C$. One major difference between the two is the steady state behavior. A network that consists of resistors dissipates energy in steady-state, but capacitor only network does not. In addition, unlike resistors, capacitors do not generate thermal noise. Those are very important properties for VLSI design. Laws of current distribution that minimize energy dissipation in resistor network are similar to laws of charge distribution in capacitor network that minimize the total energy stored in capacitors. Thus, a cost function can be designed using a similar approach.

It is possible to yield the capacitor circuit by replacing resistors with capacitors and current with charge, but for completeness, the complete circuit is derived from the basic elements.

7.2.1 Equality constraint using capacitors

Consider the circuit depicted in Fig. 7.15. V_k is the potential of node k, C_k is the capacitance between node k and the common node α with potential U, $-\sum_k C_k$ is a negative capacitance, and $\frac{b}{\sum_k C_k}$ is a constant voltage source. Here, and in the rest of this chapter we assume that the initial charge of all capacitors is zero.

Proposition 7 (Equality constraint circuit)**.** *The circuit in Fig. 7.15 enforces the equality constraint*

$$[C_1 \ \dots \ C_n] \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = b. \tag{7.16}$$

Proof. Consider the circuit depicted in Fig. 7.16. In this circuit, n wires are connected to a common node. We call this common node α, its potential U, and the charge that exits this

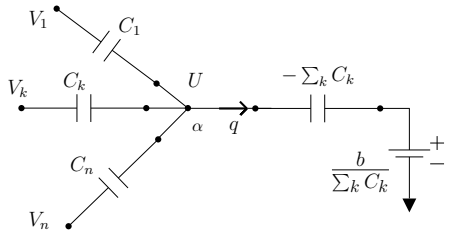


Figure 7.15: Equality enforcing circuit consisting of n capacitors ($C_1 \dots C_n$), a negative capacitance, and a reference voltage.

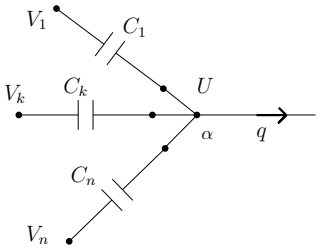


Figure 7.16: A node with n connected wires.

node q. Charge conservation and capacitor voltage laws imply

$$\sum_{k=1}^{n} q_k = \sum_{k=1}^{n} (V_k - U)C_k = q, \tag{7.17}$$

where q_k is the charge of capacitor C_k, and C_k is the capacitance between node k and node α. Eq. (7.17) can be written as an equality constraint on potentials V_k,

$$\sum_{k=1}^{n} V_k C_k = q + U \sum_{k=1}^{n} C_k. \tag{7.18}$$

If the right hand side (rhs) of (7.18) is set to any desired value b, then (7.18) enforces an equality constraint on a linear combination of V_k. The voltage U is set to

$$U = -\frac{q}{\sum_{k=1}^{n} C_k} + \frac{b}{\sum_{k=1}^{n} C_k}. \tag{7.19}$$

The rhs in (7.19) is implemented by a negative capacitance of $-\sum_{k=1}^{n} C_k$ and a constant voltage source of $\frac{b}{\sum_{k=1}^{n} C_k}$. Eq. (7.19) together with (7.18) yield the desired (7.16). Therefore, the circuit shown in Fig. 7.15 enforces (7.16). □

Note that the negative capacitance $-\sum_k C_k$ in the circuit in Fig. 7.15 can be realized by using an operational amplifier similar to Fig. 5.1.

7.2.2 Inequality constraint

Consider the circuit shown in Fig. 7.17. Similarly to the equality constraint circuit, n wires are connected to a common node α. α's potential is U and the charge exiting this node is I. A new device named *charge-diode* connects node α to node β. A *charge-diode* is a device that allows only positive charge to pass to another side. The voltage drop ΔU and an amount of charge passed through the charge-diode satisfy $\Delta U q = 0$ and $q \geq 0$. The potential of node β is U'.

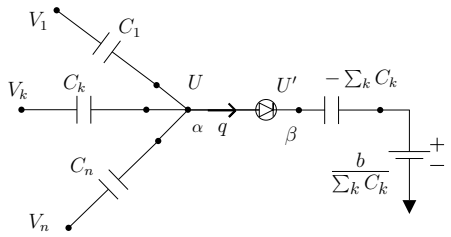


Figure 7.17: Inequality enforcing circuit.

Proposition 8 (Inequality constraint circuit)**.** *The circuit in Fig. 7.17 enforces the inequality constraint*

$$\begin{bmatrix} \frac{1}{R_1} & \cdots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \leq b. \tag{7.20}$$

Proof. Charge conservation and capacitor voltage laws imply (7.17) as in the previous case.

The charge-diode can be in open or closed state. If the charge-diode is closed the current is free to flow through the diode, the voltage drop is zero and $U = U'$. If the charge-diode is open, the charge is zero. For this case, if $U' > U$, any current will reduce the charge below zero, therefore, the charge-diode must remain closed. If $U' < U$, the charge will increase above zero, and the charge-diode will close, yielding $U' = U$. Therefore, for all cases we can say that the charge-diode enforces $U' \geq U$. In Fig. 7.17, the voltage U' can be computed as follows

$$U' = \frac{b - q}{\sum_{k=1}^{n} C_k} \geq U. \tag{7.21}$$

Eq. (7.17) and $U \leq U'$ yield

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = q + U \sum_{k=1}^{n} C_k \leq q + U' \sum_{k=1}^{n} C_k = b, \tag{7.22}$$

which can be compactly rewritten as (7.20). Therefore, the circuit shown in Fig. 7.17 enforces (7.20).

□

The charge-diode in Fig. 7.17 enforces

$$q \geq 0, \tag{7.23a}$$
$$q(U - U') = 0. \tag{7.23b}$$

By using (7.21) and rearranging its terms, (7.23b) can be rewritten as:

$$q \left(\left(\sum_{k=1}^{n} C_k \right) U - b + q \right) = 0. \tag{7.24}$$

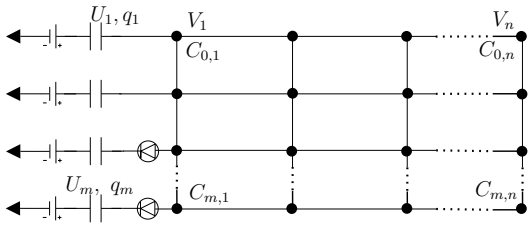


Figure 7.18: Electric circuit solving an LP. Vertical wires are variable nodes with potentials $V_1 \dots V_n$. Black dots represent capacitances that connects vertical and horizontal wires. Horizontal wires are cost or constraint nodes. Each horizontal wire is connected to a ground via a negative capacitance, a constant voltage source and a diode for inequalities nodes. The topmost horizontal wire is the cost circuit which is connected to a constant voltage source.

Remark 7. *The device charge-diode is a non-standard device that requires special implementation. Although it is required in the general case, a simpler case can utilize a standard diode. If an inequality is a "box inequality" and includes only single variable, thus $V_i < b_i$, the circuit need not include any capacitors (positive and negative capacitors cancel out) and the inequality circuit is reduced to a voltage source connected via a simple diode to a variable.*

7.2.3 Connecting the basic circuits

This section presents how to construct the circuit that solves a general QP. We construct the capacitance matrix $A \in \mathbb{R}^{m \times n}$ as

$$A = \begin{bmatrix} A_{\text{eq}} \\ A_{\text{ineq}} \end{bmatrix}, \tag{7.25}$$

and denote A_{ij} as the i, j element of A. For a given LP (3.1), the C_{ij} capacitor is defined as

$$C_{ij} \triangleq A_{ij}, \;\; i = 0, \dots m, \quad j = 1, \dots, n, . \tag{7.26}$$

Consider the circuit shown in Fig. 7.18. The circuit is shown using a compact notation where each capacitor C_{ij} is represented by a dot, vertical wires represent variable nodes with potentials $V_1 \dots V_n$ and horizontal wires represent *constraint nodes*. The compact representation of a capacitor through the dot symbol is clarified in Fig. 7.19. If $A_{ij} = 0$, then no capacitor is present at the corresponding dot.

The LP circuit is constructed by connecting the nodes associated with the variables $V_1 \dots V_n$ to all types of the basic circuits: equality and inequality. We will refer to such nodes as *variable nodes*. Each row of the circuit in Fig. 7.18 is one of the basic circuits presented in Sections 7.2.1, 7.2.2.

7.2.4 Steady state solution for capacitor circuit

In this section we show that the circuit in Fig 7.18 solves the QP (3.1).

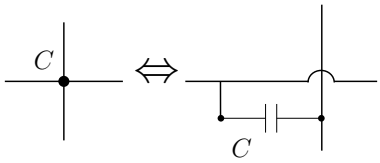


Figure 7.19: Compact representation of a capacitor.

Consider the circuit in Fig. 7.18. Let $U = [U_1, \ldots, U_m]^T$ be the voltages of the constraint nodes as shown on Fig. 7.18. By applying the charge conservation, capacitor voltage laws and charge-diode characteristics we can show in a way identical to section 4.1 that the circuit is characterized by

$$A_{\text{eq}}V = \text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} + q_{\text{eq}} \tag{7.27a}$$
$$A_{\text{ineq}}V = \text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} + q_{\text{ineq}} \tag{7.27b}$$
$$A_{\text{eq}}^T U_{\text{eq}} + A_{\text{ineq}}^T U_{\text{ineq}} = \text{diag}\left(\mathbf{1}^T A\right) V \tag{7.27c}$$
$$A_{\text{eq}}V = b_{\text{eq}},\ A_{\text{ineq}}V \leq b_{\text{ineq}},\ q_{\text{ineq}} \geq 0 \tag{7.27d}$$
$$\left[A_{\text{ineq}}V - b_{\text{ineq}}\right]_i \left[q_{\text{ineq}}\right]_i = 0, \forall i \in \mathcal{I} \tag{7.27e}$$

Next, consider the following quadratic program (QP)

$$\begin{aligned} &\min_V \ \frac{1}{2}V^T Q V \\ &s.t.\ A_{\text{eq}}V = b_{\text{eq}} && (7.28a)\\ &\quad\ A_{\text{ineq}}V \leq b_{\text{ineq}}, && (7.28b)\end{aligned}$$

The KKT conditions are necessary optimality conditions for problems with linear constraints [8, Theorem 5.1.3]. Therefore, there exist $V^\star$, $\mu^\star$, $\lambda^\star$ which satisfy the KKT conditions

$$A_{\text{eq}}^T\mu^\star + A_{\text{ineq}}^T\lambda^\star + QV^\star = 0 \tag{7.29a}$$
$$A_{\text{eq}}V^\star = b_{\text{eq}} \tag{7.29b}$$
$$A_{\text{ineq}}V^\star \leq b_{\text{ineq}} \tag{7.29c}$$
$$\lambda^\star \geq 0 \tag{7.29d}$$
$$(A_{\text{ineq}}V^\star - b_{\text{ineq}})_i\lambda_i^\star = 0,\ i \in \mathcal{I}, \tag{7.29e}$$

where $\mu^\star$ and $\lambda^\star$ are the dual variables of the QP (7.28).

We choose Q, $U^\star_{\text{eq}}$, $U^\star_{\text{ineq}}$, $q^\star_{\text{eq}}$ and $q^\star_{\text{ineq}}$ as described by the following equations.

$$\begin{aligned} Q &= \operatorname{diag}\left(\mathbf{1}^T A\right) - A_{\text{eq}}^T \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right)^{-1} A_{\text{eq}} \\ &\quad - A_{\text{ineq}}^T \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)^{-1} A_{\text{ineq}} && \text{(7.30a)} \\ q^\star_{\text{eq}} &= \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) \mu^\star && \text{(7.30b)} \\ U^\star_{\text{eq}} &= \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right)^{-1} A_{\text{eq}} V^\star - \mu^\star && \text{(7.30c)} \\ q^\star_{\text{ineq}} &= \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) \lambda^\star && \text{(7.30d)} \\ U^\star_{\text{ineq}} &= \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)^{-1} A_{\text{ineq}} V^\star - \lambda^\star. && \text{(7.30e)} \end{aligned}$$

Note that the rhs of Eqs. (7.30) consists of quantities one can compute. Eqs. (7.30) are combined with (7.29) to obtain

$$\begin{aligned} A_{\text{eq}} V^\star &= \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U^\star_{\text{eq}} + q^\star_{\text{eq}} && \text{(7.31a)} \\ A_{\text{ineq}} V^\star &= \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U^\star_{\text{ineq}} + q^\star_{\text{ineq}} && \text{(7.31b)} \\ A_{\text{eq}}^T U^\star_{\text{eq}} + A_{\text{ineq}}^T U^\star_{\text{ineq}} &= \operatorname{diag}\left(\mathbf{1}^T A\right) V^\star && \text{(7.31c)} \\ A_{\text{eq}} V^\star &= b_{\text{eq}} && \text{(7.31d)} \\ A_{\text{ineq}} V^\star &\leq b_{\text{ineq}} && \text{(7.31e)} \\ q^\star_{\text{ineq}} &\geq 0 && \text{(7.31f)} \\ (A_{\text{ineq}} V^\star - b_{\text{ineq}})_i q_{\text{ineq}_i}^\star &= 0, \ i \in \mathcal{I}. && \text{(7.31g)} \end{aligned}$$

In particular, substitution of (7.30b) into (7.30c) and of (7.30d) into (7.30e) yields Eqs. (7.31a) and (7.31b) respectively; substitution of (7.30a), (7.30b) and (7.30d) into (7.29a) yields (7.31c); substitution of (7.30d) into (7.29d) and into (7.29e) yields (7.31f) and (7.31g) respectively.

In conclusion, the electrical equations (7.27) are equivalent to the KKT conditions of QP (3.1). Therefore, there exist $V^\star$, $U^\star$, and $I^\star$ that solve (7.27) and $V^\star$ is an optimizer of QP (3.1).

7.3 Capacitor based VLSI design

The main contribution of this section is a detailed design and layout of high speed optimization circuit using analog VLSI technologies. This section presents only the main results and an interested reader will find more details in the Master thesis of Kristel Deems [25].

In this work the optimization circuit was designed using a switched-capacitor technology. The capacitor version of the circuit developed in section 7.2 cannot be implemented as-is, since real life capacitors tend to lose charge due to leakages. Therefore, the circuit requires reset every time the charge losses are substantial. This combination of capacitor based circuit and periodic resets is the switched-capacitor technology.

7.3.1 Fully differential equality constraint

We chose to implement a fully differential circuit due to advantages such as high output swing and reduced noise. We use a fully differential amplifier as shown in Fig. 7.20. When an input voltages of $U_i^+ = -U_i^-$ are applied to the circuit, the opamp zeros the input voltage difference, and, due to the symmetry, a a virtual ground (zero voltage) is created at opamp input ports. Therefore, due to charge flow the output voltages of the opamp satisfy

$$U_o^+ = -\frac{C_{f1}}{C_{f2}} U_i^+ \tag{7.32a}$$

$$U_o^- = -\frac{C_{f1}}{C_{f2}} U_i^- . \tag{7.32b}$$

The total charge flow via an input node is given by

$$q^+ = C_{f1} U_i^+ + C_{f3}(U_i^+ - U_o^-) \tag{7.33}$$

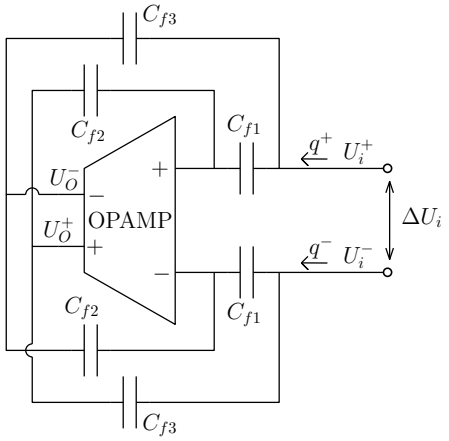


Figure 7.20: Differential negative capacitor.

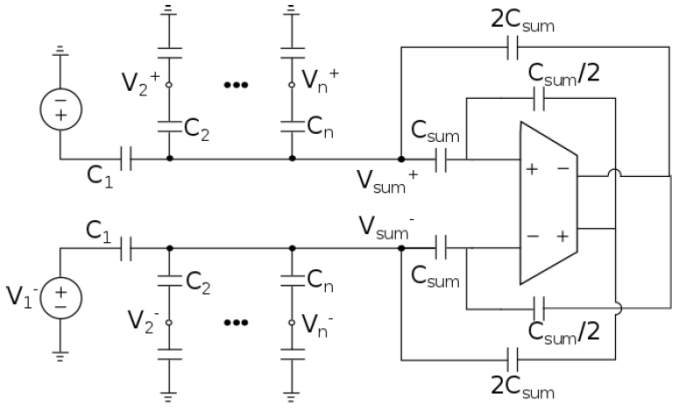


Figure 7.21: Fully differential equality constraint with capacitor values, where $C_{\texttt{sum}} = \sum_i C_i$.

Substitution of (7.32) yields the effective capacitance

$$\frac{q^+}{U_i^+} = C_{f1} + C_{f3}\left(1 - \frac{C_{f1}}{C_{f2}}\right). \tag{7.34}$$

As can be seen in (7.34) by choosing the values C_{f1}, C_{f2} and C_{f3} we can set the effective capacitance to any value, including negative. In this work we chose

$$C_{f1} = C_{\texttt{eff}}, \quad C_{f2} = \frac{1}{2}C_{\texttt{eff}}, \quad C_{f3} = 2C_{\texttt{eff}} \tag{7.35}$$

that yields a effective negative capacitance of $-C_{\texttt{eff}}$. More on the selection of the capacitor values can be found in [25].

A fully differential constraint is shown in Fig. 7.21. Unlike the single ended constraint in Fig. 7.15, the differential constraint does not have the free coefficient b. However, this is easily solved by transforming a constraint of the form $Ax = b$ to $Ax - b = 0$ and making b a variable. Indeed, this is the purpose of the voltage source V_1 in Fig. 7.21.

7.3.2 Fully differential inequality constraint

Until now we have described the inequality constraint as an equality constraint with an ideal charge-diode. However, in reality this diode is a transmission gate with gate inputs driven by a fully differential comparator. Since we can not compare two differential signals and we do not want to implement a floating voltage source, we can adjust our constraints such that the inequality is enforced on a single differential variable in comparison with zero. This inequality is shown in Fig. 7.22. The circuit is connected to V_x^- and V_x^+ variable nodes. When $V_x^- > V_x^+$ the switch (PMOS and NMOS transistors) are open, and the variable nodes are not restricted. When $V_x^- \leq V_x^+$, the comparator closes the switch and enforces $V_x^- = V_x^+$. Inequalities of the QP 3.1 can be trivially changed to the form $V_i \leq 0$ by adding optimization variables and equality constraints.

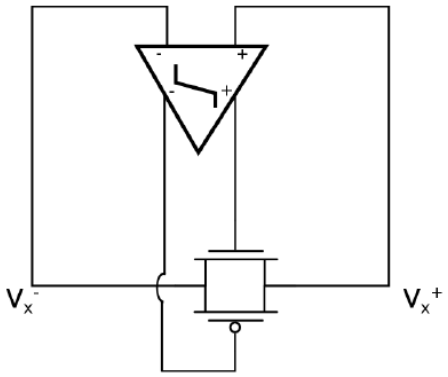


Figure 7.22: Inequality enforcing $V_x \leq 0$. The comparator includes an SR latch to hold the outputs constant during the comparator reset phase.

7.3.3 Analog VLSI design considerations

Because the ability to implement the correct optimization problem depends completely on charge transfer, the accuracy of the solution is highly sensitive to parasitic capacitance. As such, all routing to capacitances has ground shielding and the capacitors are sized to be large enough such that any unaccounted parasitic capacitance won't affect accuracy. Then the only parasitics we are concerned with are the capacitances to the substrate from routing and coupling capacitance to the shielding. These parasitics add extra load capacitance from the variable nodes to ground as well as a large capacitance from the summing node to ground as shown in Fig. 7.23. The summing node capacitance $C_{\texttt{err}}$ is the most problematic parasitic because then the cancellation this circuit is meant to implement is no longer perfect. However, it is simple to account for this with an added capacitance $C_{\texttt{comp}}$ in parallel with the feedback capacitor. The value of $C_{\texttt{comp}}$ is equal to $C_{\texttt{err}}$ in order to correctly compensate for it. Practically, this compensation capacitor would be implemented with a bank of switched capacitors to allow for tunability. Then as long as the capacitance from the summing node to ground is the only significant parasitic capacitance, the compensation will correct for the error and the circuit will be accurate for multiple input values.

The added load capacitances on variable nodes will change the cost function that the circuit implements. Therefore, they need to be accounted for when determining redundant constraints to implement the cost function. On the other hand, $C_{\texttt{err}}$ will not affect the cost function. It effectively adds a new variable to the constraint which needs to be corrected with $C_{\texttt{comp}}$. However, because this variable is ground, any cross terms in the cost function created by $C_{\texttt{err}}$ would be multiplied by zero.

The OTA used in all the constraint blocks is a fully differential two stage telescopic cascode amplifier as shown in Figs. 7.24 and 7.25. Since both accuracy and speed of the system are important, we needed an architecture with high gain. To be able to handle a wider variety of constraints and therefore dynamic range ratios, we also want high output swing. This allows for more freedom when choosing capacitance values and redundant constraints.

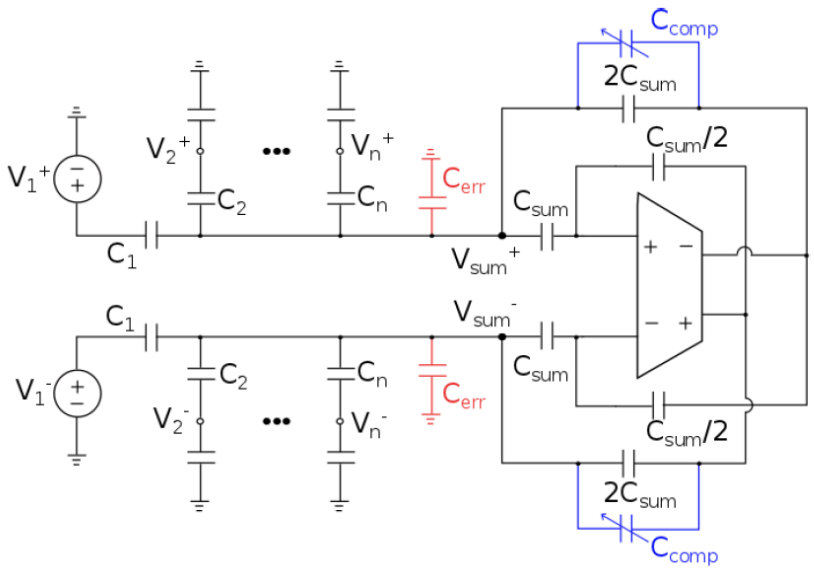


Figure 7.23: Diagram showing addition of compensation capacitor $C_{\texttt{comp}}$ to correct for error due to summing node parasitic capacitance $C_{\texttt{err}}$.

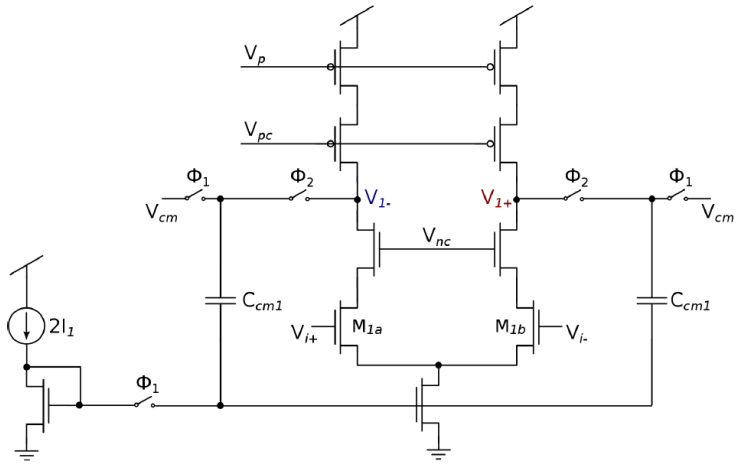


Figure 7.24: First stage of fully differential two stage telescopic cascode amplifier with common mode feedback.

Since we are already using a switched-capacitor configuration with our feedback capacitors, it is simplest to use a switched-capacitor common mode feedback (CMFB) as well. The common mode feedback keeps the differential output of the OTA centered at a predefined value. Additional details on the design process can be found at [25].

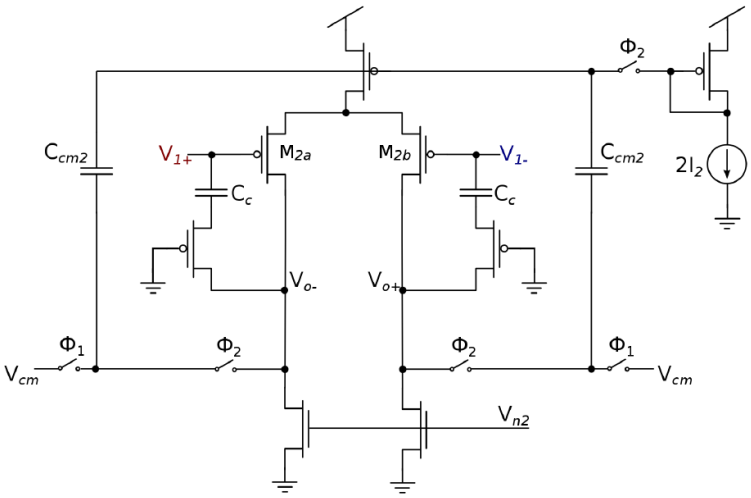


Figure 7.25: Second stage of fully differential two stage telescopic cascode amplifier with common mode feedback.

7.3.4 Design and simulation results

The example we implemented is a simple QP

$$\min_{V_x,V_y,V_z} \; [V_x \; V_y \; V_z] Q \begin{bmatrix} V_x \\ V_y \\ V_z \end{bmatrix} \tag{7.36a}$$

$$\texttt{s.t. } V_x + 2V_y + 0.5V_z = 0.1 \tag{7.36b}$$

the schematics for which shown in Fig. 7.26 and the layout in Fig. 4.5. We used metal-oxide-metal (*mom*) capacitors with a unit capacitance of 75 fF, so the smallest capacitance is 150 fF. To shape the cost function additional load capacitances are required. However, because the parasitic capacitance from each variable to ground is significant, we did not implement load capacitances in the array and simply relied on the coupling capacitance to ground shielding and capacitance from routing to the substrate.

The resulting capacitances after extraction from the complete layout are shown in Table 4.1 below. After calculating Q as in (7.30a) and substituting $-100mV$ into the cost function for V_s, the cost function is

$$\begin{aligned}[V_x \; V_y \; V_z] Q \begin{bmatrix} V_x \\ V_y \\ V_z \end{bmatrix} =& 2749V_x^2 + 3760V_y^2 + 1657V_z^2 - 2000V_xV_y - 500V_xV_z - 1000V_yV_z \\ &+ 100000V_x + 200000V_y + 50000V_z. \end{aligned} \tag{7.37}$$

As a result, we expect the differential values $V_x = 26.93mV$, $V_y = 30.38mV$, and $V_z = 24.61mV$. The extracted results without design iterations after layout are shown in Fig. 7.28.

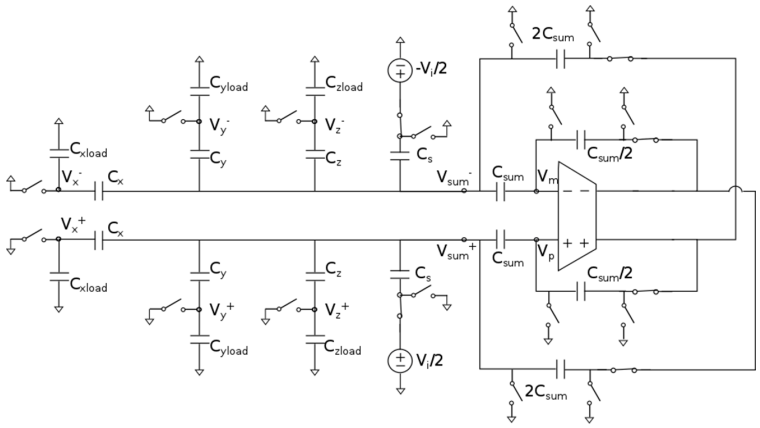


Figure 7.26: Schematics for the QP (7.36).

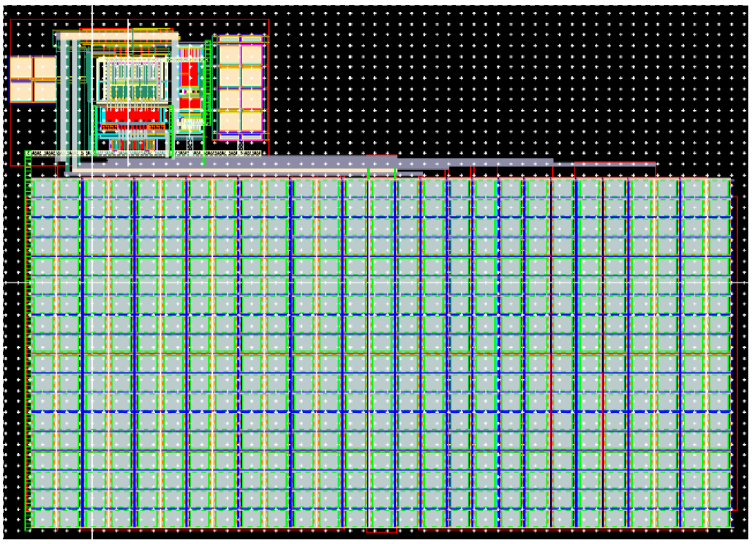


Figure 7.27: Layout for the QP (7.36) implemented in TSMC 65nm. Total size is $240\mu m \times 300\mu m$. The bottom part are the capacitors and the upper left part is the OTA.

Looking at these results, the variables at Fig. 7.28 solve the equality constraint within $\pm 1\%$ error in $50ns$. This is done with a power consumption of $4.32mW$.

7.3.5 Conclusion

The results from extracted simulations show that we can solve a QP with 1% accuracy in $50ns$ while consuming $4.32mW$ of power. To our knowledge, this is faster than any other reported results.

Considering that the solution speed should improve with further design iterations after layout, our results are promising. Additionally, power consumption can potentially improve,

Table 7.4: Absolute and Normalized Capacitor Values.

Capacitor	Value	Ratio to Cs
C_x	298.7 fF	1
C_y	597.5 fF	2
C_z	149.6 fF	0.5
C_s	298.7 fF	1
$C_{\texttt{x,load}}$	132.7 fF	0.444
$C_{\texttt{y,load}}$	167.2 fF	0.56
$C_{\texttt{z,load}}$	87.3 fF	0.292

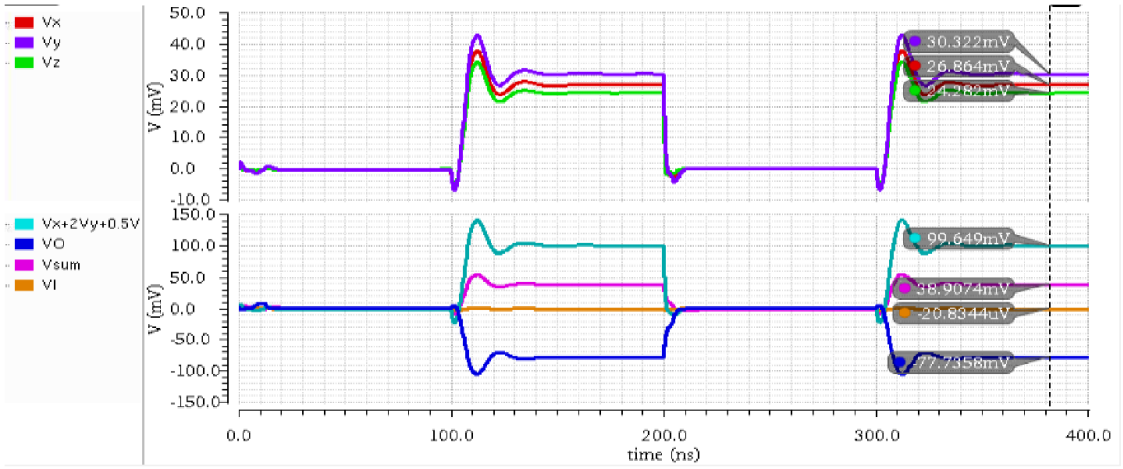


Figure 7.28: Extracted results showing settling time of $50ns$ for the QP (7.36) with a switching period of $200ns$. The differential values of the summing node and amplifier input and output are also shown.

as power conservation methods were not explored in this work. Further research on this proposed circuit can also include implementing more complex problems to determine latency scaling and fabricating and testing a chip.

Chapter 8

Applications of analog optimization

In this chapter we present and study possible applications of analog optimization that go beyond MPC. In section 8.1 we show how the proposed analog optimization circuit can be used as a co-processor for fast solution of linear systems. In section 8.2 we propose to decode error correcting codes faster than any digital circuit. Section 8.3 shows how it can be used in highly parallel image processing device.

8.1 Solution of a linear system of equalities.

8.1.1 Existing digital solution

Digital solution to $AX = B$ for small sizes of $A \in \mathbb{R}^{N\times N}$ (N less than 10000) is done using a direct method that requires $(^2/_3N^3 + 2N^2)$ operations [94]. Iterative methods are not considered for small matrices. There are multiple published curves that provide FLOPS (operations per second) that can be achieved using the current hardware. The FLOPS curve reaches maximum for large size of A but is very far from maximum for lower sizes. Highest performance is achieved by the latest Intel CPUs that can yield 40 GFLOPS for large matrices [36, 101] or even more for large matrices and parallel processors [72]. For smaller sizes, the performance is about 1 GFLOPS or lower. FPGAs can be used as well for this purpose. However, the published results are surprisingly dull – FPGAs are shown to achieve improvement of 2 times at most [101]. The main reason is that FPGA must use a lower clock frequency (200MHz), compared to an optimal and custom design of the CPUs that use up to 3GHz. Therefore, massive parallelization in FPGAs does not immediately pays off.

8.1.2 Analog solution

The current VLSI design in chapter 7 requires 50 *nsec* for a three variables problem. The main unknown is how the speed degrades with the number of variables, N. The speed is dependent on the specific design and trade-off decisions. Every additional row introduces

one active element (negative impedance) and N passive elements. However, because of the negative impedance matching requirement, the additional negative and total positive impedances are equal.

A common electric delay model for an RC chain (Elmore delay [28]) is proportional to N^2. However, it is not obvious that the square model is applicable in this case, since we introduce a new active component for each stage. From the other hand, another common rule for cascading N identical transfer functions is that the total rise time is proportional to N. More accurate analysis that uses a specific design is required to estimate the computing speed. It seems reasonable to assume that the settling time of the circuit is somewhere between N^2 and N curves.

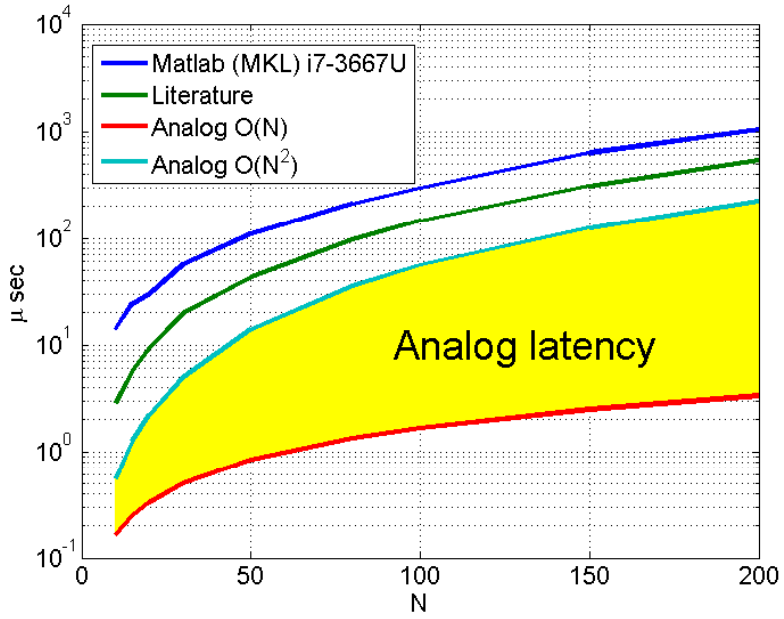


Figure 8.1: Comparison of digital and analog latencies of solution to $AX = B$.

Fig. 8.1 shows computation delay using 4 methods:

1. Matlab software with MKL BLAS library on Intel Core-i7 CPU 2.5 GHz.
2. Theoretical estimate using published curves of FLOPS vs N and the known number of operations.
3. Analog computation extrapolated using N^2 model.
4. Analog computation extrapolated using N model.

The analog solution by itself has a low accuracy that may be improved by an iterative refinement [94]. First, an approximated analog solution to $AX = B$ is obtained. Second, the

residual is computed using digital hardware as $r = AX - B$. Third, a refined X is obtained from the analog solution ΔX to $A\Delta X = r$.

Each iteration of the refinement adds digits of accuracy to the solution according to the accuracy of the analog solver. Therefore, we imagine a linear algebra co-processor that includes analog and digital component which yield solutions with the latency of analog circuit and accuracy of the digital technology.

8.2 Error correcting decoding of linear codes

8.2.1 Introduction

Error correcting decoding is ubiquitous in modern electronic equipment. All storage devices, magnetic and solid state, rely on error correction codes to achieve higher information density without sacrificing data integrity. Thus, a device can use a high density physical layer with greater error rate that is compensated using error correcting codes. Similar reasoning in modern communication equipment, such as WIFI and 4G LTE standards, yields obligatory use of advanced error correcting decoding that maximize the available bandwidth. Every mobile phone has at least 3 decoders: in wireless receiver, in WIFI module and in every flash memory chip. In addition, every computer has multiple decoders and the emerging field of internet-of-things will have multiple decoders in every device as well.

Modern error correcting codes, such as Low Density Parity Check (LDPC), practically achieve the maximum theoretical channel throughput (Shannon's capacity [61]). Therefore, the main industry challenge is to shrink the price, latency and power consumption of the decoder that remains a significant contributor to all of the above. This subject is studied intensively in academia [34, 73, 46, 57] and in industry [43, 23, 60] in order to build sophisticated and highly efficient decoders using state of the art digital technologies. The current designs struggle with trade-off of power, speed and space. We propose to improve all three altogether by utilizing the novel analog optimization technology.

This work proposes to build a fast, compact and energy efficient decoder for linear codes family, such as LDPC, based on an analog optimization solver as proposed in this dissertation. The analog/digital implementation is faster, potentially more power efficient and compact then pure digital.

We demonstrate the decoding of a linear code, that is a code that satisfies linear constraint, with an LDPC example. A low-density parity-check (LDPC) code is a linear error correcting code, a method of transmitting a message over a noisy transmission channel [61]. An LDPC is constructed using a sparse bipartite graph. LDPC codes are capacity-approaching codes, which means that practical constructions exist that allow the noise threshold to be set very close to the theoretical maximum (the Shannon limit) for a symmetric memoryless channel. The noise threshold defines an upper bound for the channel noise, up to which the probability of lost information can be made as small as desired. Using

iterative belief propagation techniques, LDPC codes can be decoded in time linear to their block length.

LDPC codes are also known as Gallager codes, in honor of Robert G. Gallager, who developed the LDPC concept in his doctoral dissertation at the Massachusetts Institute of Technology in 1960 [32].

LDPC code is described by a parity check matrix H

$$Hx = 0, \tag{8.1}$$

where $H \in \{0,1\}^{m \times n}$ is a sparse matrix, and $x \in \{0,1\}^n$ is a code word. Any x that satisfies (8.1) is a valid code word. Therefore, the decoding problem may be formulated as following: *Given a measured code word x_m that may contain errors, find a code word x that satisfies* (8.1) *and is the closest (in some sense) to x_m.*

There are belief propagation algorithms that are able to recover error-free x from a noisy sample in time that is linear with the length of x. Therefore, practical implementation is able to use code length of thousands. For example, the WIFI standard IEEE 802.11n specifies 648, 1296 and 1944 code lengths.

8.2.2 Decoding LDPC using an optimization problem

Let $x_m \in \{0,1\}^n$ be the measured code word. We define the following optimization problem

$$\begin{aligned} &\min_{0 \geq x \geq 1} \|x\|_l \\ &s.t.\ Hx = b, \end{aligned} \tag{8.2}$$

where $x \in \mathbb{R}^n$, the norm qualifier l is either 1, 2 or ∞, $b \in \{0,1\}^n$ is the parity check result computed as

$$b = Hx_m, \tag{8.3}$$

where x_m is the measured, possibly corrupted code word, and the multiplication in Hx_m is boolean (parity check).

The decoding is done by iterative solution of (8.2) as detailed in Algorithm 1. It is immediate to see that if $Hx_m = 0$, the solution to (8.2) is $x = 0$. When a bit is flipped, it causes violation in multiple rows, consequently, it is optimal to alter this bit only in order to satisfy the constraint. Therefore, by flipping the bits that are differ significantly from 0 in the optimizer of (8.2) we may restore the original code word.

The step 3 in Alg. 1 is done by an analog solver, the comparison in line 5 is done by an analog comparator and the steps 2 and 6 are done with digital hardware.

8.2.3 Analog circuit implementation

Analog implementation is based on the basic analog optimization circuit from Chapter 3 and uses digital and analog components.

Algorithm 1 LDPC decoder using optimization

while $Hx_m \neq 0$ **do**
  Compute b as in (8.3)
  Solve (8.2) to get x
  for $i = 1$ to n **do**
    if $x_i > \varepsilon$ **then**
      $x_{mi} \leftarrow 1 - x_{mi}$ ▷ Flip bit
    end if
  end for
end while
Output x_m

8.2.3.1 Norm-2 (QP) implementation

An example of implementation when norm-2 is used in (8.2) is shown in Fig. 8.2. The circuit contains the usual resistor matrix and negative resistances as in chapter 3. All the passive resistors in the circuit have the same value that significantly simplifies the design. For every variable node x_i, there is a fixed node x_{mi} that is externally set to either 0 or 1. Each source voltage of x_{mi} is connected to a comparator, that will cause it to flip if x_i is more then some ε. In addition, on the right side of the circuit m fixed voltage sources b_j for every constraint are shown. Those variables transform parity check to an equality constraint, by

$$Hx = b \Rightarrow Hx - b = 0, \quad b_j \in \{0, 1\}. \tag{8.4}$$

The values of b_j are computed from x_m with a digital binary logic that is not shown in Fig. 8.2 for simplicity.

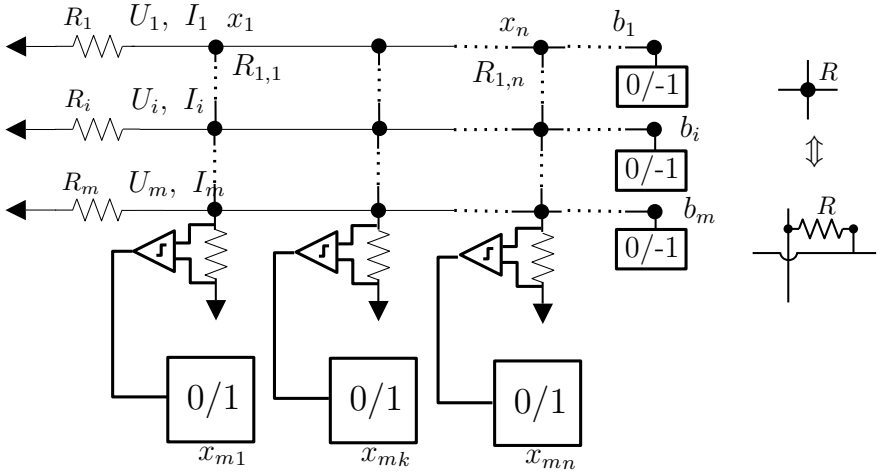


Figure 8.2: Circuit that decodes a linear code using norm-2 (quadratic program).

The circuit is initialized with x_m and operates in asynchronous manner, thus, each comparator may flip its x_{mi} independently. When x_{mi} flips, all affected b_j change as well and the circuit converges to a new equilibrium, unless another x_{mi} is flipped. The solution is found when all parity constraints are satisfied. No A/D sampling or D/A output is required since all the analog interfaces are discrete $\{-1, 0, 1\}$ and x_m may be used directly in digital circuitry.

The accuracy requirements from analog part of the circuit are benign, since all input voltages are discrete, the constraints all have the same weight and small number of variables (just 7 variables for IEEE 802.11n/648 bits). This potentially enables small and power efficient design, since low gain amplifiers and inaccurate passive devices an be used.

8.2.3.2 Norm 1 (LP) implementation

A similar circuit can be designed, based on the same principles, that minimizes norm-1 instead of the quadratic norm-2. The circuit is shown in Fig. 8.3.

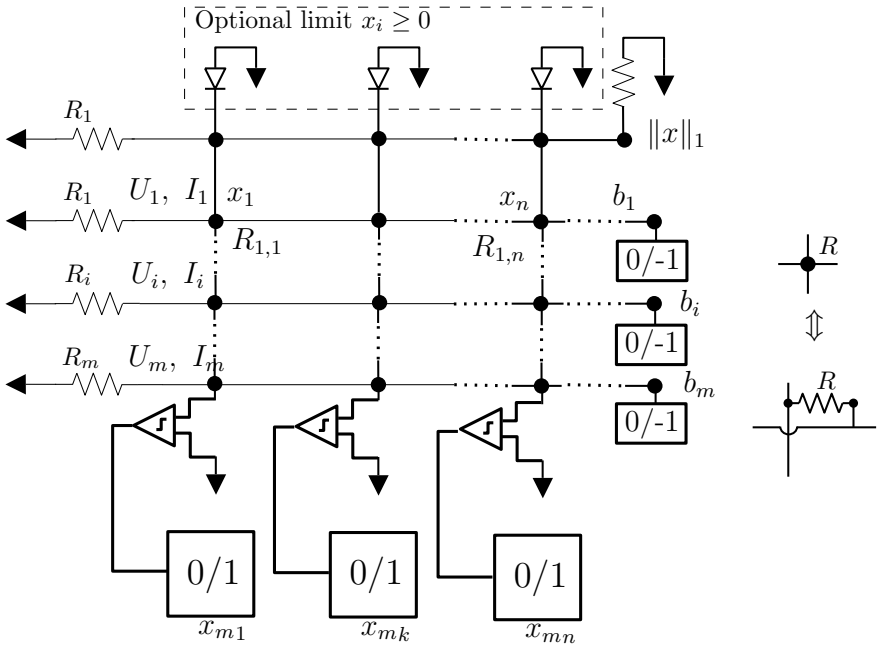


Figure 8.3: Circuit that decodes a linear code using norm-1 (linear program).

The circuit has the central linear constraint lattice similar to Fig. 8.2 and has an additional linear constraint (top row) that computes the sum of all x_i values as $\sum_i x_i$. This variable is being driven to lower value by a resistor to ground that yields the norm-1 optimization function. Optional limiting diodes are shown in the top of the figure. The diodes clamp x_i voltages to zero. Although x_i are expected to be naturally non-negative, the diodes may be needed to account for non-perfect implementation of the optimization problem.

8.2.3.3 Generalization from binary variables to integer variables

The decoding method as presented is defined for binary variables. However, some applications, such as solid state devices, have integer variables. We will show the generalization using Multi Level Cell (MLC) flash memory [24]. In MLC flash each cell can hold 4 distinct voltage levels that can be represented as 2 bits. In this case a typical error will alter voltage by a single level. Therefore, a single bit error depends on values of other bits. In order to accommodate this behavior the simple comparator that is shown in Figs. 8.2 and 8.3 needs to be generalized to take the current value of a variable into account. We call this device a *generalized comparator*.

Fig. 8.4 shows the logic of a *generalized comparator* for the 2 bit MLC flash. For example, if the current state is voltage level 0 that corresponds to bits $0,0$, a reasonable error may change the voltage level to 1 and bit value $0,1$. Therefore, if a large deviation is measured by the circuit in LSB bit b_0 but not in MSB bit b_1 the *generalized comparator* may flip b_0 and raise the expected voltage value to 1. This behavior is encoded in the transition condition from the state $0,0$ to $0,1$ in Fig. 8.4. However, if a deviation is detected in both bits, the *generalized comparator* should not flip any bit since it is unlikely to have an error from $0,0$ to $1,1$. Note that this logic can be significantly simplified if the Gray code [35] is used instead of a regular binary code.

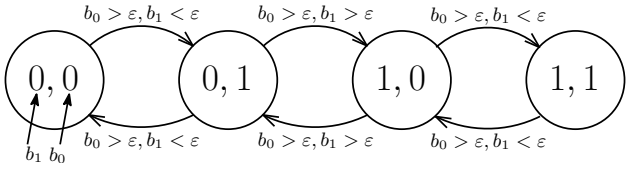


Figure 8.4: Legal correcting transitions for a single MLC flashas implemented by a *generalized comparator*.

8.2.4 Results and Conclusion

LDPC decoding may fail when error bits mask the effects of each other, since they share the same parity check. In this case Algorithm 1 may get stuck. As a remedy, we can switch the cost function in (8.2). The Algorithm 1 was implemented using norm-2 (QP) and norm-1 (LP) with the LDPC matrix of IEEE 802.11n with code length 648 and code ratio of 1/2. The performance are shown in Fig. 8.5 together with an existing modern hardware digital implementation [80] denoted as "HW, BP". As can be seen, the results are comparable to the digital implementation for low SNR range. For higher SNR, the digital implementation rapidly reaches very low error rate, while the analog has significantly higher error rate. The worse performance for high SNR is an open challenge.

If the analog performance is improved (e.g. by applying a smarter unstuck heuristics) to achieve practically required goal such as 10^{-8}, the analog decoder may replace the digital one. Alternatively, one may use the analog decoder as a fast and efficient first phase and for

the 0.01% of blocks that failed (error rate of 10^{-4}) the slower digital decoder may be used to achieve better performance.

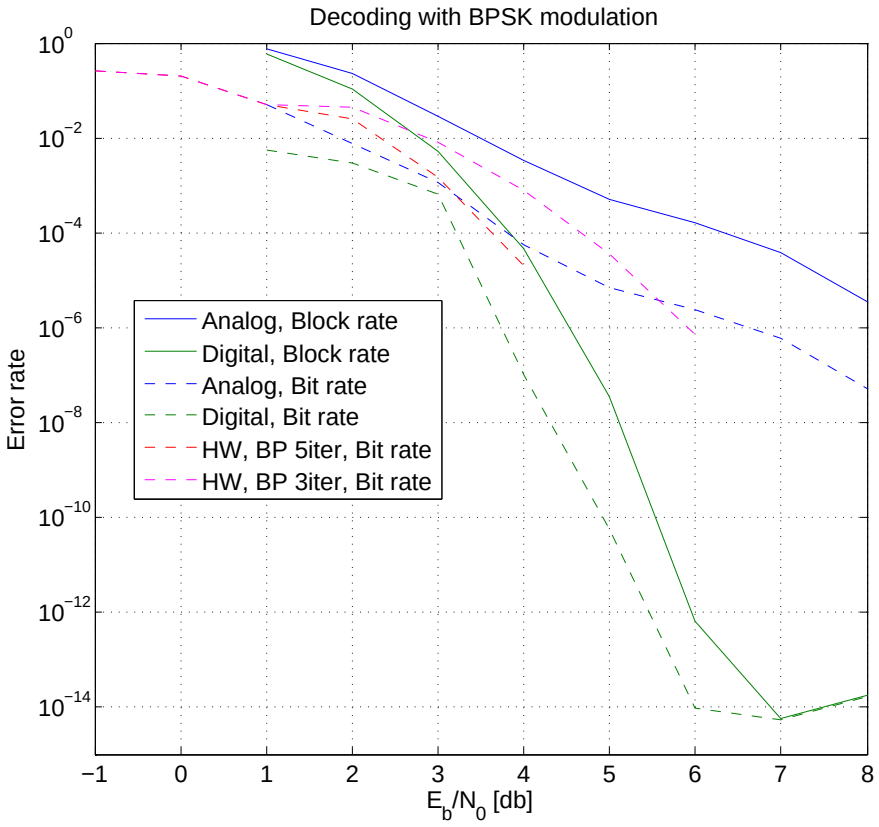


Figure 8.5: Performance of the proposed analog LDPC decoding compared to digital implementation in Matlab toolbox and [80].

8.3 Image processing

Image processing traditionally requires substantial computing power. Many of the image processing algorithms can be formulated as an optimization problem and solved using an analog circuit. In 2012 DARPA driven by the realization that *"The digital processors used for ISR data analysis are limited by power requirements, potentially limiting the speed and type of data analysis that can be done. A new, ultra-low power processing method may enable faster, mission critical analysis of ISR data"* announced the Unconventional Processing of Signals for Intelligent Data Exploitation (UPSIDE) program to *"break the status quo of digital processing with methods of video and imagery analysis based on the physics of nanoscale devices"* [95].

We propose to use the analog optimizing circuit to perform some of the algorithms in an image processing pipeline as shown in Fig 8.6. In a typical CMOS sensor an image is captured as voltage levels using light sensitive diodes for each pixel. Next, voltage levels are sampled by an analog to digital converter (A/D) and transferred to a digital format for further processing. Some of the processing can be done at analog sensor level using an optimizing circuit implemented on the same substrate as the CMOS sensor itself, as for example was done in [88]. By moving the processing before the A/D stage we can potentially reduce latency and reduce power consumption. For some applications the digital part of the system may be powered off completely, and turned on only when the analog part detects an event, such as movement.

One example of an algorithm that is computationally and power intensive is optical flow estimation [99] that is the amount of movement for each pixel between consecutive images. In the next sections we present the method and the circuit that compute optical flow on the CMOS sensor level.

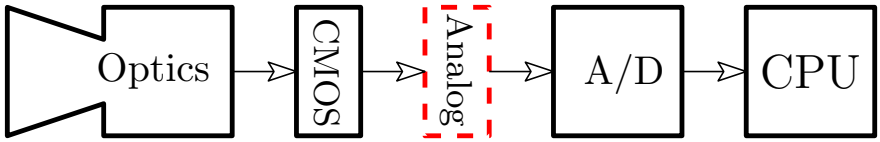


Figure 8.6: Image acquisition and processing pipeline with the proposed analog processing stage at the CCD level. The image is captured as voltage levels by a CCD sensor, those voltages are the input to an analog processor, and its output is sampled by the A/D block and transferred to a processor for further processing.

8.3.1 Optical flow

Let $I(x, y, t)$ be a 2-D image function of time. Assume that the image is only moving and keeping intensity constant and using complete derivative we can write

$$0 = \frac{dI}{dt} = \frac{\partial I}{\partial x}\frac{\partial x}{\partial t} + \frac{\partial I}{\partial x}\frac{\partial x}{\partial t} + \frac{\partial I}{\partial t}, \tag{8.5}$$

where $\frac{\partial I}{\partial x}$ and $\frac{\partial I}{\partial y}$ are spatial image derivatives, $\frac{\partial x}{\partial t}$ and $\frac{\partial y}{\partial t}$ are local image movement speed and $\frac{\partial I}{\partial t}$ is the local intensity change. Therefore, (8.5) may be written as

$$\frac{\partial I}{\partial x}V^x + \frac{\partial I}{\partial x}V^y + \frac{\partial I}{\partial t} = 0, \tag{8.6}$$

where $V^x = \frac{\partial x}{\partial t}$ and $V^y = \frac{\partial y}{\partial t}$ are the components of optical flow we want to estimate, and $\frac{\partial I}{\partial x}$, $\frac{\partial I}{\partial y}$ and $\frac{\partial I}{\partial t}$ are computed from measured image intensities.

The optical flow equation (8.6) needs to be solved for every pixel. Since (8.6) cannot be solved independently for each pixel (2 unknowns and 1 equation), smoothness requirement is required to make the neighboring velocities similar

$$min \sum_{\boxdot\in\{x,y\}} \sum_j \sum_i \left[(V^{\boxdot}_{i,j} - V^{\boxdot}_{i+1,j})^2 + (V^{\boxdot}_{i,j} - V^{\boxdot}_{i,j+1})^2 \right], \tag{8.7}$$

where $V^{\boxdot}_{i,j}$ is the optical flow component of the pixel i, j. Since (8.6) does not have to be satisfied exactly, we want to minimize its violation that is represented by the error variable ε. Therefore, the optical flow estimation problem is the following QP

$$\min_{\substack{V^x_{i,j}, V^y_{i,j}, \varepsilon_{i,j} \\ 1 \le i \le \mathcal{M} \\ 1 \le j \le \mathcal{N}}} \sum_j \sum_i \left(q\varepsilon^2_{i,j} + \sum_{\boxdot\in\{x,y\}} \left[pV^{\boxdot 2}_{i,j} + (V^{\boxdot}_{i,j} - V^{\boxdot}_{i+1,j})^2 + (V^{\boxdot}_{i,j} - V^{\boxdot}_{i,j+1})^2 \right] \right) \tag{8.8a}$$

$$\texttt{s.t.} \quad \frac{\partial I_{i,j}}{\partial x}V^x_{i,j} + \frac{\partial I_{i,j}}{\partial x}V^y_{i,j} + \frac{\partial I_{i,j}}{\partial t} + \varepsilon_{i,j} = 0, \quad 1 \le i \le \mathcal{M}, \quad 1 \le j \le \mathcal{N} \tag{8.8b}$$

where q and p are weights, $\mathcal{M}$ and $\mathcal{N}$ are the number of rows and columns in an image respectively.

Note that the QP (8.8) is of substantial size for modern image sensors. A typical problem has millions of equality constraints (8.8b) and millions of terms in the cost function. For this reason the optical flow is computationally expensive. In the next session we show how the optimization circuit can be used in a modular way to solve the QP (8.8) for any image size.

8.3.2 Electrical circuit

One can build the optimization circuit to solve QP (8.8) using a basic building cell for every pixel. A 2-dimensional array of the basic cells solves the QP (8.8).

The spatial image derivatives in levels per pixel units are given by

$$\frac{\partial I_{i,j}}{\partial x} = \frac{1}{2}(I_{i,j+1} - I_{i,j-1}) \tag{8.9}$$

$$\frac{\partial I_{i,j}}{\partial y} = \frac{1}{2}(I_{i+1,j} - I_{i-1,j}), \tag{8.10}$$

where $I_{i,j}$ is the value of the pixel i, j. Since the optimizing circuit must work with non-negative coefficients (section 3.2), the problem of a single cell takes the form

$$\min_{\substack{V^x_{i,j}, V^y_{i,j}, \varepsilon_{i,j} \\ i \in \mathcal{M}, j \in \mathcal{N}}} \sum_j \sum_i \left(q\varepsilon^2_{i,j} + \sum_{\boxdot \in \{x,y\}} \left[p V^{\boxdot 2}_{i,j} + (V^{\boxdot}_{i,j} - V^{\boxdot}_{i+1,j})^2 + (V^{\boxdot}_{i,j} - V^{\boxdot}_{i,j+1})^2 \right] \right) \tag{8.11a}$$

$$\texttt{s.t.} \quad I_{i,j+1} V^x_{i,j} + I_{i,j-1} V^{-x}_{i,j} + I_{i+1,j} V^y_{i,j} + I_{i-1,j} V^{-y}_{i,j} + \varepsilon_{i,j} = -\frac{\partial I_{i,j}}{\partial t}, \quad i \in \mathcal{M}, j \in \mathcal{N} \tag{8.11b}$$

$$V^x_{i,j} + V^{-x}_{i,j} = 0 \tag{8.11c}$$

$$V^y_{i,j} + V^{-y}_{i,j} = 0 \tag{8.11d}$$

Therefore, each cell consists of 3 equality constraints and 5 variables $(V^x_{i,j}, V^{-x}_{i,j}, V^y_{i,j}, V^{-y}_{i,j}, \varepsilon_{i,j})$.

The QP (8.11) can be solved using a circuit as in Chapter 3. Let the terminals of the circuit be arranged as shown in Fig. 8.7. In this case, we can solve arbitrary large QP (8.6) by tiling the basic cells. In Fig. 8.7 the bi-directional arrow stands for a variable node shared between the neighboring tiles. The directional arrows are used to transfer the pixel intensity information to and from the neighboring tiles.

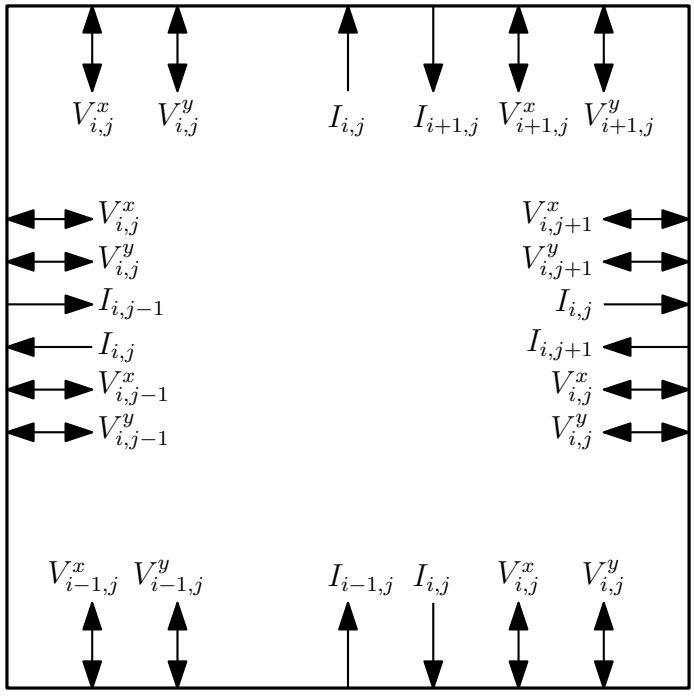


Figure 8.7: Single cell of an optical flow array.

After an image is sampled and the values of $I_{i,j}$ are set, each cell adjusts coefficients of its equality constraint. This step is non-trivial, since the circuit needs to change the resistance (or capacitance) as function of $I_{i,j}$. This can be accomplished with a switched bank of components that are connected according to the voltage level of $I_{i,j}$. The steady state voltages of the array built of the cells are the optimizers of QP (8.6). The latency of the solution should be very small, not much bigger than the latency of a single cell, since the amount of influence between cells is diminishing with distance, therefore, the transients are essentially local.

8.4 Conclusion

In this chapter we presented three ideas to apply the analog optimization technique to a broad range of applications. Obviously, this list is not exhaustive and the analog optimization can be used for even more tasks. The proposed applications can be developed into real products or inspire other uses that we cannot foresee now. We believe that nanoseconds computation latencies will open the road to new, currently unimaginable technologies. In the future, we may find an analog co-processor in all our devices, have analog processing integrated in sensors on the pre-digitized stage, etc.

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Appendix A

Optimization problems for PCB board

The optimization problem that is solved by the PCB board as described in Section 6.4.1

$$\min_{V=[v_1,\ldots,v_{21}]} V^T Q V \tag{A.1}$$

$$s.t. \begin{bmatrix} 0.32625\,v_3 + 0.13178\,v_4 + 0.015088\,v_5 + 0.43493\,v_{12} + 0.067787\,v_{15} \\ 0.3816\,v_4 + 0.088449\,v_5 + 0.0013333\,v_6 + 0.27573\,v_{13} + 0.025823\,v_{14} \\ 0.40722\,v_1 + 0.04964\,v_2 + 0.017973\,v_{10} + 0.037029\,v_{15} + 0.42335\,v_{18} \\ 0.14322\,v_2 + 0.00072566\,v_6 + 0.10498\,v_{10} + 0.014214\,v_{12} + 0.10962\,v_{19} \\ 0.55916\,v_1 + 0.32288\,v_{12} \\ 0.20262\,v_2 + 0.20585\,v_{13} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} v_2 \\ v_{13} \\ v_5 \\ -v_5 \\ -v_{19} \\ v_{19} \\ v_{10} \\ -v_{10} \end{bmatrix} \leq \begin{bmatrix} 0.0298 \\ 0.0248 \\ 0.0723 \\ -0.0697 \\ -0.0156 \\ 0.0417 \\ 0.0358 \\ -0.03 \end{bmatrix}$$

were the cost matrix Q is

$$Q = \begin{bmatrix}
92.9 & -2.16 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -0.782 \\
-2.16 & 73.9 & 0 & 0 & 0 & -0.354 & 0 & 0 & 0 & -4.04 \\
0 & 0 & 21.7 & -4.41 & -0.506 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & -4.41 & 30.9 & -4.52 & -0.463 & 0 & 0 & 0 & 0 \\
0 & 0 & -0.506 & -4.52 & 59.3 & -0.107 & 0 & 0 & 0 & 0 \\
0 & -0.354 & 0 & -0.463 & -0.107 & 1.86 & 0 & 0 & 0 & -0.26 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-0.782 & -4.04 & 0 & 0 & 0 & -0.26 & 0 & 0 & 0 & 59.4 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-20.4 & -0.531 & -14.5 & -5.87 & -0.675 & -0.035 & 0 & 0 & 0 & -0.389 \\
0 & -10.2 & 0 & -13.5 & -3.12 & -0.335 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -1.26 & -0.292 & -0.0313 & 0 & 0 & 0 & 0 \\
-1.62 & -0.197 & -2.27 & -0.916 & -0.105 & 0 & 0 & 0 & 0 & -0.0713 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-18.4 & -2.25 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -0.813 \\
0 & -4.12 & 0 & 0 & 0 & -0.271 & 0 & 0 & 0 & -3.02 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-49.5 & -50.0 & 0 & 0 & -50.0 & 0 & 0 & 0 & 0 & -50.0
\end{bmatrix}$$

$$\begin{bmatrix}
0 & -20.4 & 0 & 0 & -1.62 & 0 & 0 & -18.4 & 0 & 0 & -49.5 \\
0 & -0.531 & -10.2 & 0 & -0.197 & 0 & 0 & -2.25 & -4.12 & 0 & -50.0 \\
0 & -14.5 & 0 & 0 & -2.27 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -5.87 & -13.5 & -1.26 & -0.916 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -0.675 & -3.12 & -0.292 & -0.105 & 0 & 0 & 0 & 0 & 0 & -50.0 \\
0 & -0.035 & -0.335 & -0.0313 & 0 & 0 & 0 & 0 & -0.271 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -0.389 & 0 & 0 & -0.0713 & 0 & 0 & -0.813 & -3.02 & 0 & -50.0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 95.4 & 0 & 0 & -3.02 & 0 & 0 & 0 & -0.406 & 0 & -49.6 \\
0 & 0 & 77.9 & -0.91 & 0 & 0 & 0 & 0 & 0 & 0 & -49.8 \\
0 & 0 & -0.91 & 2.49 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -3.02 & 0 & 0 & 9.88 & 0 & 0 & -1.68 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & -1.68 & 0 & 0 & 72.9 & 0 & 0 & -49.8 \\
0 & -0.406 & 0 & 0 & 0 & 0 & 0 & 0 & 57.8 & 0 & -50.0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -49.6 & -49.8 & 0 & 0 & 0 & 0 & -49.8 & -50.0 & 0 & 399.0
\end{bmatrix} \quad \text{(A.2)}$$

The optimization problem that is solved by the PCB board as described in Section 6.4.2

$$\min_{V=[v_1,\ldots,v_{21}]} V^T Q V \tag{A.3}$$

$$s.t. \begin{bmatrix} 0.32625\,v_3 + 0.13178\,v_4 + 0.015088\,v_5 + 0.43493\,v_{12} + 0.067787\,v_{15} \\ 0.3816\,v_4 + 0.088449\,v_5 + 0.0013333\,v_6 + 0.27573\,v_{13} + 0.025823\,v_{14} \\ 0.40722\,v_1 + 0.04964\,v_2 + 0.017973\,v_{10} + 0.037029\,v_{15} + 0.42335\,v_{18} \\ 0.14322\,v_2 + 0.00072566\,v_6 + 0.10498\,v_{10} + 0.014214\,v_{12} + 0.10962\,v_{19} \\ 0.55916\,v_1 + 0.32288\,v_{12} \\ 0.20262\,v_2 + 0.20585\,v_{13} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} v_2 \\ v_{13} \\ v_5 \\ -v_5 \\ -v_{19} \\ v_{19} \\ v_{10} \\ -v_{10} \end{bmatrix} \leqslant \begin{bmatrix} 0.029828 \\ 0.024792 \\ 0.072253 \\ -0.069672 \\ -0.032432 \\ 0.041706 \\ 0.035832 \\ -0.029251 \end{bmatrix}$$

were the cost matrix Q is

$$Q = \begin{bmatrix}
703.0 & -2.16 & 0 & -3.39 & 0 & -2.48 & -260.0 & 0 & 0 & -0.783 \\
-2.16 & 74.6 & 0 & -13.8 & 0 & -0.33 & 0 & -13.1 & 0 & -4.13 \\
0 & 0 & 23.3 & -4.41 & -0.89 & 0 & 0 & 0 & 0 & 0 \\
-3.39 & -13.8 & -4.41 & 47.9 & -4.57 & -0.0658 & 0 & 0 & 0 & 0 \\
0 & 0 & -0.89 & -4.57 & 95.4 & -0.177 & 0 & 0 & -75.7 & 0 \\
-2.48 & -0.33 & 0 & -0.0658 & -0.177 & 10.5 & 0 & 0 & 0 & -0.13 \\
-260.0 & 0 & 0 & 0 & 0 & 0 & 260.0 & 0 & 0 & 0 \\
0 & -13.1 & 0 & 0 & 0 & 0 & 0 & 13.1 & 0 & 0 \\
0 & 0 & 0 & 0 & -75.7 & 0 & 0 & 0 & 241.0 & -165.0 \\
-0.783 & -4.13 & 0 & 0 & 0 & -0.13 & 0 & 0 & -165.0 & 453.0 \\
0 & -0.233 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -0.0271 \\
-20.5 & -0.546 & -14.5 & -5.87 & -0.672 & -4.65 & 0 & 0 & 0 & -0.4 \\
0 & -10.2 & -1.2 & -13.6 & -3.16 & -0.0476 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -1.27 & -0.682 & -0.00445 & 0 & 0 & 0 & 0 \\
-1.61 & -0.215 & -2.27 & -0.915 & -0.115 & 0 & 0 & 0 & 0 & -0.0844 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-18.4 & -2.25 & 0 & 0 & 0 & -2.58 & 0 & 0 & 0 & -0.814 \\
0 & -4.21 & 0 & 0 & 0 & -0.0213 & 0 & 0 & 0 & -3.09 \\
-0.149 & 0 & 0 & 0 & -0.906 & 0 & 0 & 0 & 0 & 0 \\
-394.0 & -23.4 & 0 & 0 & -8.58 & 0 & 0 & 0 & 0 & -278.0
\end{bmatrix}$$

$$\begin{bmatrix}
0 & -20.5 & 0 & 0 & -1.61 & 0 & 0 & -18.4 & 0 & -0.149 & -394.0 \\
-0.233 & -0.546 & -10.2 & 0 & -0.215 & 0 & 0 & -2.25 & -4.21 & 0 & -23.4 \\
0 & -14.5 & -1.2 & 0 & -2.27 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -5.87 & -13.6 & -1.27 & -0.915 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -0.672 & -3.16 & -0.682 & -0.115 & 0 & 0 & 0 & 0 & -0.906 & -8.58 \\
0 & -4.65 & -0.0476 & -0.00445 & 0 & 0 & 0 & -2.58 & -0.0213 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-0.0271 & -0.4 & 0 & 0 & -0.0844 & 0 & 0 & -0.814 & -3.09 & 0 & -278.0 \\
0.86 & -0.0869 & 0 & 0 & 0 & 0 & 0 & 0 & -0.513 & 0 & 0 \\
-0.0869 & 227.0 & 0 & -11.1 & -3.02 & -141.0 & 0 & 0 & -0.418 & 0 & -25.0 \\
0 & 0 & 49.2 & -0.921 & -0.0309 & 0 & -6.62 & 0 & 0 & -0.235 & -13.1 \\
0 & -11.1 & -0.921 & 14.0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -3.02 & -0.0309 & 0 & 9.95 & 0 & 0 & -1.68 & -0.0139 & 0 & 0 \\
0 & -141.0 & 0 & 0 & 0 & 642.0 & 0 & -501.0 & 0 & 0 & 0 \\
0 & 0 & -6.62 & 0 & 0 & 0 & 16.3 & 0 & -9.68 & 0 & 0 \\
0 & 0 & 0 & 0 & -1.68 & -501.0 & 0 & 1499.0 & 0 & -9.19 & -946.0 \\
-0.513 & -0.418 & 0 & 0 & -0.0139 & 0 & -9.68 & 0 & 67.0 & 0 & -49.0 \\
0 & 0 & -0.235 & 0 & 0 & 0 & 0 & -9.19 & 0 & 10.5 & 0 \\
0 & -25.0 & -13.1 & 0 & 0 & 0 & 0 & -946.0 & -49.0 & 0 & 1744.0
\end{bmatrix} \tag{A.4}$$

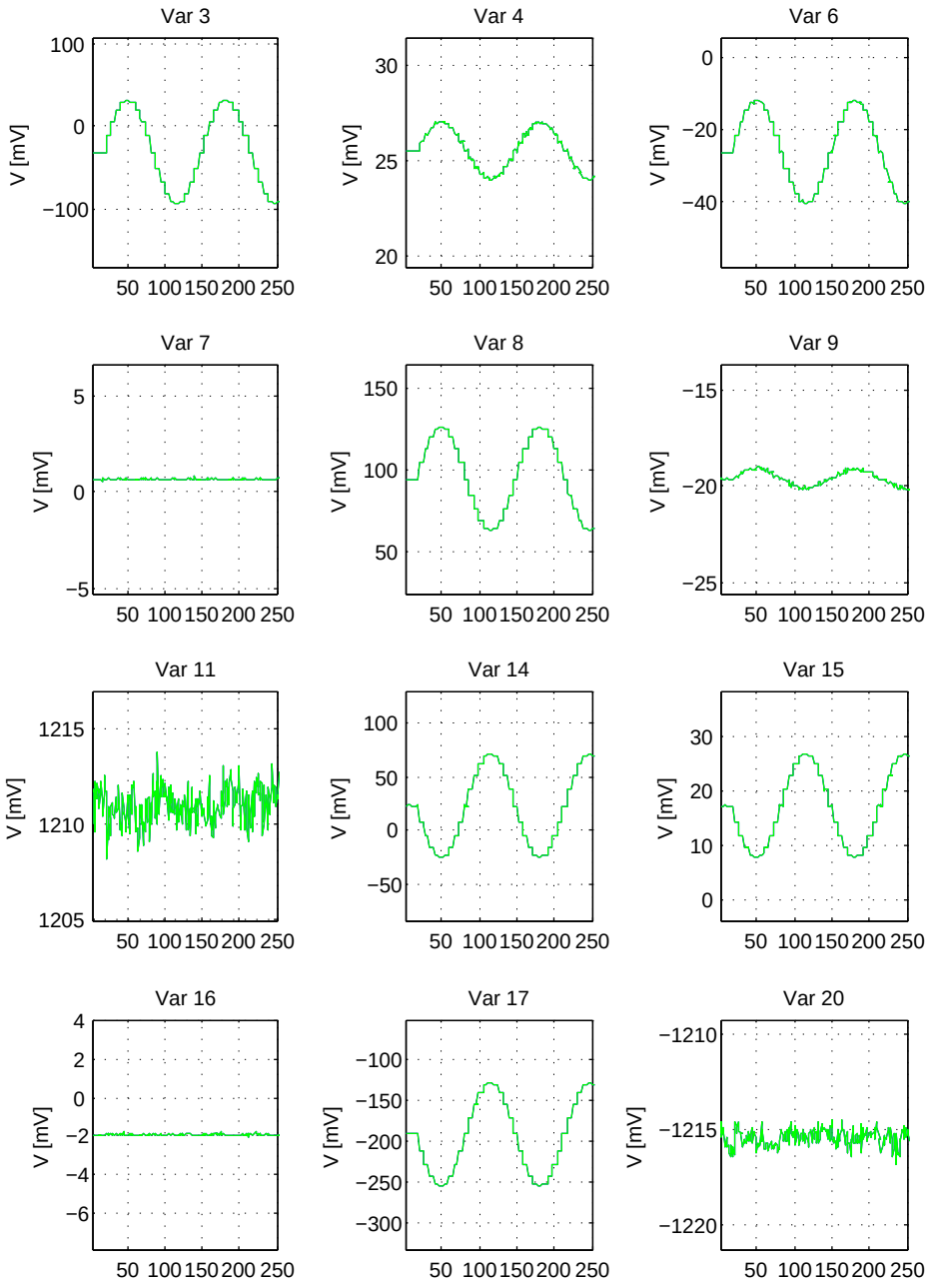

Figure A.1: Input and constant variables of the circuit.