A 12.9 fA/rtHz Power-Efficient High-Dynamic-Range Current Front-end for Light-to-Digital Conversion

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***Abstract*—Light-to-digital converters are critical in bio-signal acquisition systems such as photoplethysmography (PPG) and fluorescence sensors. These applications demand converters with low input-referred noise (IRN) and high dynamic range (DR) to detect low-level signals from sensing targets in the presence of large varying background levels. Typically, noise performance is limited by the operational transconductance amplifier (OTA) in the capacitive transimpedance amplifier (CTIA) and kT/C noise sampled on the feedback capacitor. kT/C noise is commonly canceled through correlated double sampling, which suffers from noise folding of the high frequency OTA noise. This work presents a four-channel light-to-digital converter IC that utilizes multi-sample line fitting to suppress kT/C noise and noise folding. A power-efficient gain-boosted folded-cascode OTA topology is employed within the CTIA to further reduce the dominant noise during integration. Compared to recent light-to-digital converter designs, the fabricated IC achieves the lowest IRN of 12.9 fA/rtHz, the best power efficiency of 0.646 fA^2·W/Hz, and a high DR of 119.4 dB.**

I. Introduction

Light-to-digital conversion is widely utilized for bio-signal acquisition such as photoplethysmogram (PPG) monitoring [1]–[3] and cellular or chemical detection using fluorescent probes [4]–[6]. Typically in these systems, photodiodes are used to convert incident light into photocurrent, which is amplified by a transimpedance amplifier (TIA) into a voltage signal followed by analog-to-digital conversion. The weak light source necessitates low input-referred noise (IRN), while large fluctuations due to motion artifacts or changes in ambient light demand a high dynamic range (DR).

Prior arts have focused on circuit techniques to maximize DR with low power consumption, but simultaneously achieving high DR, low IRN with low power remains a challenge. Among commonly used light-to-digital converter architectures, capacitive TIAs (CTIAs) are preferred because they avoid additional thermal noise introduced by the feedback resistor required in resistive TIAs. The feedback capacitor in the CTIA plays a crucial role in determining the noise performance. A reduction in feedback capacitance enhances the gain of the CTIA and lowers the IRN originating from the operational transconductance amplifier (OTA). However, this approach is fundamentally constrained by the input parasitic capacitance [7]. Moreover, decreasing the feedback capacitance leads to an increase in kT/C noise during the reset phase. Conventionally, kT/C noise is canceled using correlated double sampling (CDS) [6], [7] (Fig. 1(a)), which samples the voltages at the beginning and end of integration and computes the difference. In this approach, the smaller feedback capacitance can not further improve IRN but introduces larger kT/C that reduces the available CTIA voltage range during integration, thereby degrading DR. Moreover, CDS suffers from noise folding due to aliasing from high-frequency OTA thermal noise [7]. An alternative approach is direct current-to-digital conversion using continuous-time delta-sigma modulation (CTDSM) [2], [5] (Fig. 1(b)), where the CTIA is incorporated into the feedback loop. This approach benefits from oversampling and noise shaping to suppress kT/C noise and reduce OTA noise. However, the feedback current DACs introduce additional noise that directly adds to the signal and adversely impacts performance.

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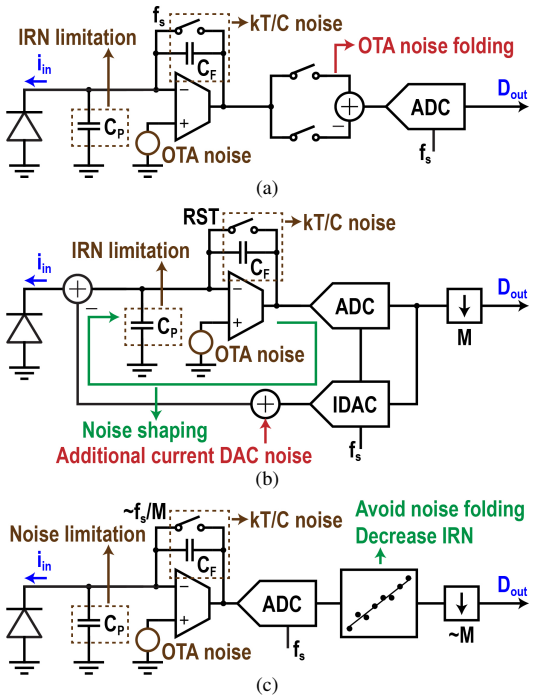
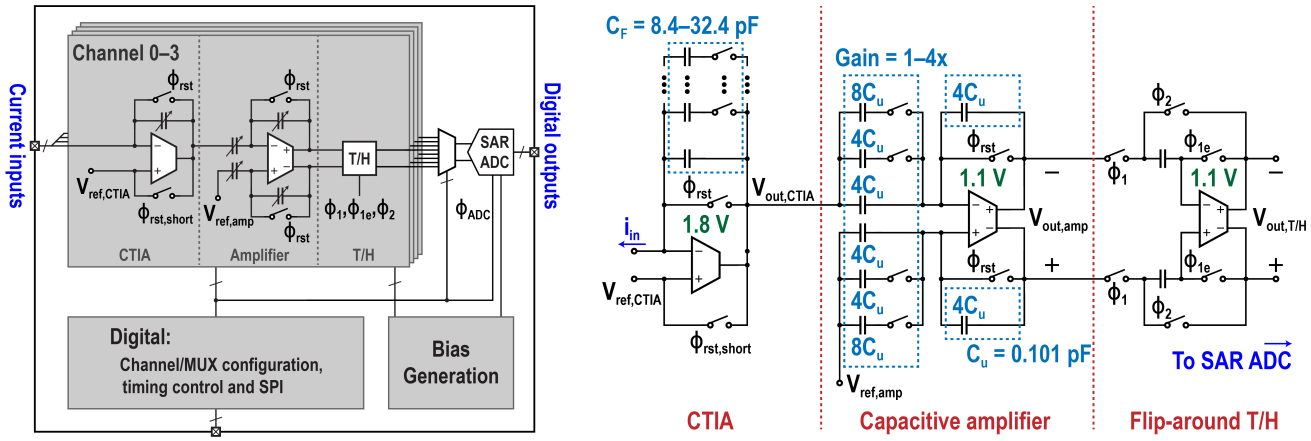


Fig. 1. Pros and cons of common light-to-digital converter architectures. (a) Correlated double sampling. (b) Continuous-time delta-sigma modulation. (c) Multi-sample line fitting.



(a) (b)

Fig. 2. (a) Proposed top-level block diagram and (b) the detailed current front-end channel design. The capacitor configurations are done by enabling/disabling the switches. Multi-sample line fitting is executed off-chip for design flexibility.

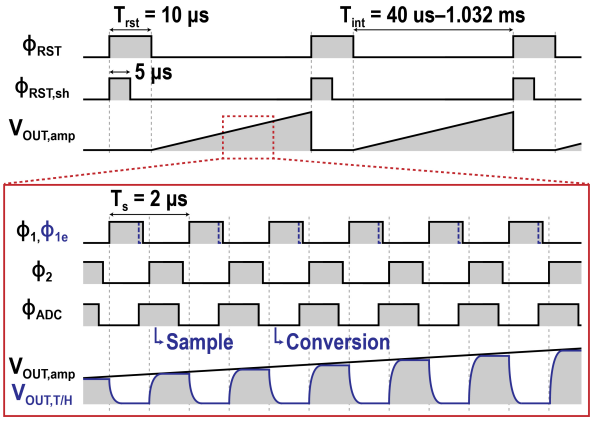


Fig. 3. Timing diagram for multi-sample line fitting. The integration time T_{int} is configurable for fitting 16–512 samples.

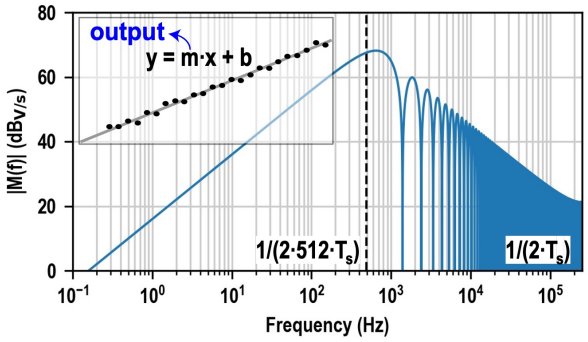


Fig. 4. Magnitude response $|M(f)|$ of 512-sample line fitting assuming zero reset time (T_s =2 µs).

This work enhances the conventional CDS technique by incorporating oversampled integration with multi-sample line fitting [8] (Fig. 1(c)). Instead of directly measuring the voltage difference, kT/C noise is effectively suppressed through the inherent slope extraction mechanism of the line-fitting process. For a given feedback capacitance, oversampling reduces noise folding, resulting in lower IRN compared to traditional CDS. Unlike CTDSM, this architecture eliminates the need for current DACs, thereby avoiding their associated IRN contributions and reducing overall power consumption.

II. Proposed Current Front-end Design

Fig. 2(a) presents the top-level block diagram. Four current front-end channels are implemented to interface with different light sensors and are multiplexed into a single asynchronous SAR ADC. Fig. 2(b) illustrates the detailed channel implementation. After the CTIA stage, the single-ended output voltage is converted to a differential signal by a fully differential capacitive amplifier, followed by oversampling through a flip-around track-and-hold (T/H) stage. To maximize DR, both the CTIA feedback capacitance and the the capacitive amplifier gain are configurable via the embedded serial peripheral interface (SPI). The corresponding timing diagram is shown in Fig. 3. After a fixed reset time T_{rst}, the CTIA starts integration. Minimizing the reset time reduces the overall line-fitting sampling period $T_{rst}+T_{int}$, so a combination of ϕ_{RST} and $\phi_{RST,sh}$ is used to accelerate settling. To avoid settling errors at the beginning of integration, samples are taken after a short time interval. By adjusting the integration time T_{int} while maintaining a constant T/H sampling period T_s, the system can collect 16–512 samples per integration. Although oversampling increases power consumption in the T/H stage and SAR ADC, its overall impact on system power efficiency is minimal (Fig. 7).

Oversampling the integrated signal followed by line fitting reduces thermal noise by a factor of $\sqrt{N/12}\times$ [8]. Line fitting also provides filtering. Assuming zero reset time and a sampling period T_s, an N-sample line-fitting operation is essentially an FIR filter, whose transfer function is:

$$M(z) = \frac{1/T_s}{\left(\sum_{i=0}^{N-1} i^2\right) - \left(\sum_{i=0}^{N-1} i\right)^2} \sum_{i=0}^{N-1} \left(\frac{N-1}{2} - i\right) z^{-i}. \quad (1)$$

Fig. 4 visualizes the magnitude response. At low frequency, line fitting acts as a differentiator (20 dB/dec), which can filter

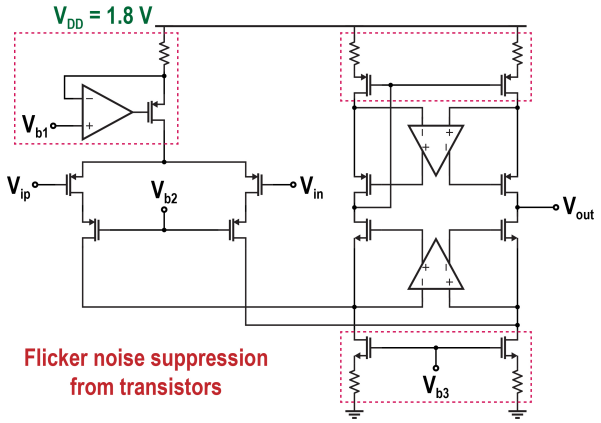
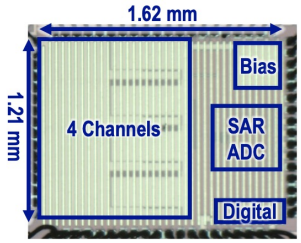


Fig. 5. Implemented power-efficient gain-boosted folded-cascode OTA design in the CTIA. V_{b1}, V_{b2}, and V_{b3} are all bias voltages.



Chip Area Summary

1 Channel	0.231 mm^2
SAR ADC	0.212 mm^2
Bias	0.172 mm^2
Digital	0.078 mm^2

Fig. 6. Chip die photo and area summary.

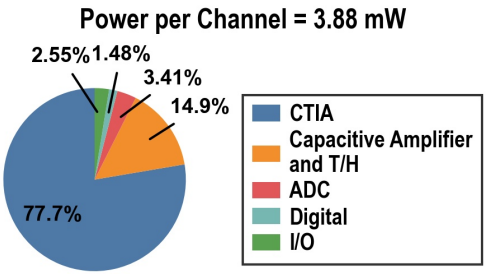


Fig. 7. Chip power breakdown.

out the low-frequency kT/C and the OTA flicker noise. At high frequency, the decreasing trend of -20 dB/dec can also filter out the high-frequency OTA thermal noise to avoid noise folding when downsampling.

Since the noise of the proposed current front-end is primarily limited by the OTA in the CTIA, a gain-boosted folded-cascode topology (Fig. 5) is employed to minimize this dominant noise and maximize power efficiency simultaneously. The large input devices minimize the flicker and thermal noise while maintaining a high current efficiency factor (g_m/I_D). All top and bottom transistors are degenerated to minimize flicker noise contribution from the current sources. Considering different feedback capacitance configurations, a single stage topology is utilized to guarantee closed-loop stability. Cascoding the input pair further reduces the Miller effect from the C_{GD} at the input, enhancing the closed-loop bandwidth.

III. Chip Measurement Results

The IC was fabricated in TSMC's 28 nm HPM process. The die photo and area breakdown are presented in Fig. 6.

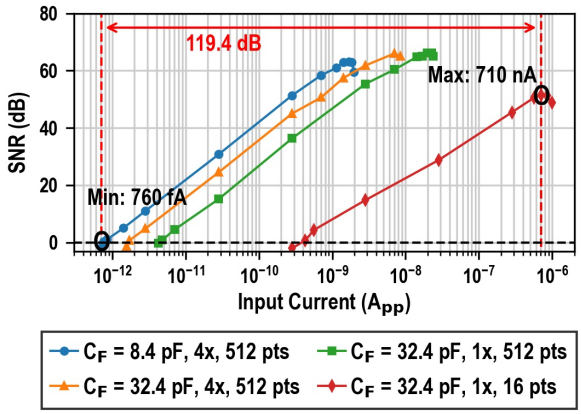


Fig. 8. Measured dynamic range (DR) given different configurations.

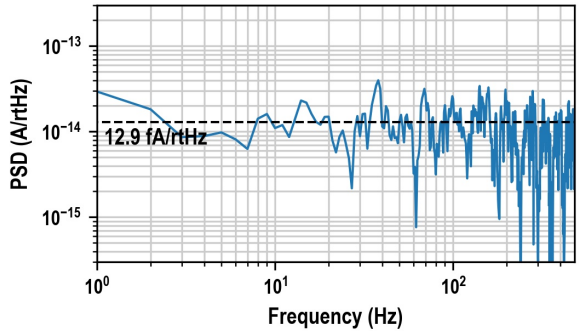


Fig. 9. Measured noise spectrum under the most sensitive configuration (C_F =8.4 pF, 4× gain, 512 samples).

The core area is 1.96 mm^2. Each channel occupies 0.23 mm^2, and the SAR ADC occupies 0.21 mm^2. Fig. 7 shows the power breakdown. The IC consumes 3.88 mW per channel, 77.7% of which is from the CTIA.

Fig. 8 illustrates the measured DR under different configurations. A low-distortion wave generator (SRS DS360) in series with different SMD resistors (1–360 MΩ) was used to generate a 10 Hz sinusoidal current waveform. The system achieves a minimum detectable current of 760 fA$_{pp}$ with a high DR of 119.4 dB under different configurations. Moreover, using the most sensitive configuration (C_F =8.4 pF, 4× gain, 512 samples), an IRN of 12.9 fA/rtHz is achieved (Fig. 9).

To verify the light-to-digital functionality, an XFAB XS018.O.EC.A doa photodiode with an area of 500×500 µm^2 was connected to the chip for characterization. A 554 nm fiber-coupled LED excitation source followed by an attenuating absorptive filter enabled a broad input light intensity range. Fig. 10 demonstrates the measurement setup, and Fig. 11 illustrates the measured photocurrent as a function of input light intensity under the most and the least sensitive configurations. The detectable optical intensity ranges from 2.80 pW to 2.40 µW, which is almost six orders of magnitude.

IV. Summary and Comparison

The proposed power-efficient high-DR current front-end IC for light-to-digital conversion employs oversampling during

TABLE I
COMPARISON TABLE WITH THE STATE-OF-THE-ART LIGHT-TO-DIGITAL CONVERTER DESIGNS

	ISSCC'11 [4]	TBioCAS'18 [5]	TCAS-I'19 [6]	TBioCAS'21 [1]	ISSCC'23 [2]	JSSC'24 [3]	**This work**
Technology	180 nm	180 nm	180 nm	180 nm	180 nm	55 nm	**28 nm**
Area (mm^2)	1.26[a]	0.494	0.475	8.37[a]	0.66	4.59[a]	**1.96**
# Channels	1	1	1	2	1	1	**4**
VDD (V)	1.8	1.8	3.3	1.2	1.0	1.8	**1.8**
Power/channel (mW)	2.4	0.041	0.093	0.028	0.26	0.03	**3.88**
Bandwidth (Hz)	800	50	50	20	4000	20	**480**
IRN (fA/rtHz)	141	348	184	8940	456	11040	**12.9**
Power efficiency[b] (fA^2·W/Hz)	47.7	4.97	3.15	2240	54.1	3660	**0.646**
DR (dB)	77	86	104	134	136.6	136.5	**119.4**

[a] Only die area was reported. [b] Power efficiency = IRN^2· power.

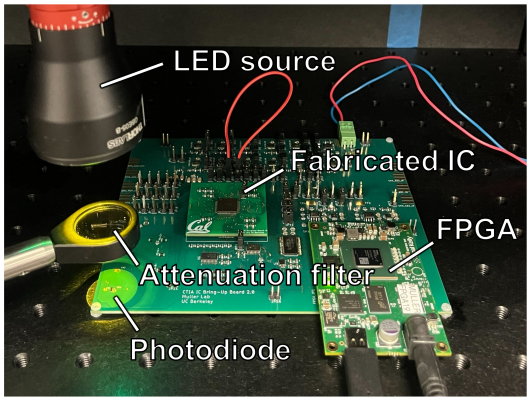


Fig. 10. Optical incident power measurement setup. A fiber-coupled LED at 554 nm followed by an attenuating absorptive filter enabled a broad light intensity range.

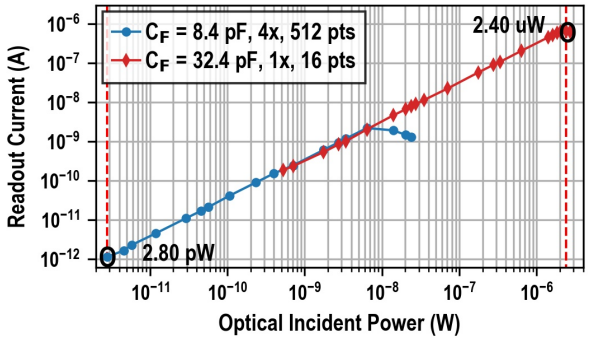


Fig. 11. Readout current as a function of incident light intensity power using the most and the least sensitive configurations (C_F =8.4 pF, 4× gain, 512 samples and C_F =32.4 pF, 1× gain, 16 samples, respectively).

integration and applies multi-sample line fitting. The magnitude response of line fitting filters out low-frequency kT/C and OTA flicker noise, and prevents folding of high-frequency OTA thermal noise. The OTA noise is further minimized using a power-efficient gain-boosted folded-cascode topology.

Table I compares the proposed light-to-digital converter with state-of-the-art designs. This work achieves the lowest IRN of 12.9 fA/rtHz with a high DR of 119.4 dB. To analyze power efficiency based on the noise-power tradeoff, we evaluate the product of noise power and power dissipation (IRN^2·power in fA^2·W/Hz) by adapting the definition of the power efficiency factor (PEF) from [9]. Compared with the best-performing high-DR (>70 dB) light-to-digital converters, this work achieves a 5× improvement in power efficiency with a simultaneous 14× reduction in IRN.

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REFERENCES

[1] Q. Lin *et al.*, "A 134 DB dynamic range noise shaping slope light-to-digital converter for wearable chest PPG applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 6, pp. 1224–1235, Dec. 2021.

[2] T. Seol *et al.*, "A 1V 136.6dB-DR 4kHz-BW ΔΣ current-to-digital converter with a truncation-noise-shaped baseline-servo-loop in 0.18μm CMOS," in *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2023, pp. 482–484.

[3] M. Li *et al.*, "A 30-μW 94.7-dB SNDR noise-shaping current-mode direct-to-digital converter using triple-slope quantizer for PPG/NIRS readout," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 6, pp. 1722–1734, Jun. 2024.

[4] R. T. Heitz, D. B. Barkin, T. D. O'Sullivan, N. Parashurama, S. S. Gambhir, and B. A. Wooley, "A low noise current readout architecture for fluorescence detection in living subjects," in *2011 IEEE International Solid-State Circuits Conference*, Feb. 2011, pp. 308–310.

[5] M. N. Khiarak *et al.*, "A wireless fiber photometry system based on a high-precision cmos biosensor with embedded continuous-time ΣΔ modulation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 12, no. 3, pp. 495–509, Jun. 2018.

[6] M. Noormohammadi Khiarak, S. Martel, Y. De Koninck, and B. Gosselin, "High-DR CMOS fluorescence biosensor with extended counting ADC and noise cancellation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 6, pp. 2077–2087, Jun. 2019.

[7] M. Crescentini, M. Bennati, M. Carminati, and M. Tartagni, "Noise limits of CMOS current interfaces for biosensors: A review," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 2, pp. 278–292, Apr. 2014.

[8] A. M. Fowler and I. Gatley, "Noise reduction strategy for hybrid IR focal-plane arrays," in *Infrared Sensors: Detectors, Electronics, and Signal Processing*, vol. 1541. SPIE, Nov. 1991, pp. 127–133.

[9] R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013 mm^2, 5 μW, DC-coupled neural signal acquisition IC with 0.5 V supply," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 232–243, Jan. 2012.