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A Dual-Polarity Graphene NEMS Switch ESD Protection Structure

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***Abstract*— Conventional on-chip electrostatic discharge (ESD) protection structures for integrated circuits (ICs) rely on in-Si p-n-junction-based devices, which have many inherent disadvantages unsuitable for ICs at nanonodes. This letter reports a novel above-IC graphene-based nanoelectromechanical system (gNEMS) transient switch ESD protection mechanism and structure. Transmission line pulse testing shows dual-polarity transient ESD switching effect with a response time down to 200 ps. This gNEMS switch is a potential ESD protection solution to realize the above-Si ESD protection designs through 3-D integration in IC back end of line.**

***Index Terms*— Graphene, gNEMS, switch, ESD, TLP.**

I. Introduction

ESD PROTECTION design is a major reliability challenge as IC technologies rapidly migrate to nano nodes. For decades, conventional ESD protection structures relied on PN-junction-based device structures inside silicon to provide active paths to discharge fast ESD transients safely. In principle, an ESD protection structure is a switch that may be turned on by an ESD transient to shunt ESD surges [1]. ESD protection structures are characterized by ESD-critical parameters including triggering voltage, current and time (V_{t1}, I_{t1}, t_1), holding voltage and current (V_h, I_h), discharging resistance (R_{ON}), and failure voltage and current (V_{t2}, I_{t2}) [1]–[3]. However, in-Si PN-type ESD protection structures have inherent disadvantages such as parasitic junction leakage (I_{leak}), easily being a few tens of nA for typical ESD structures and becoming intolerable to ICs at nano nodes [3]–[5]. It hence calls for novel ESD protection mechanisms and structures for future ICs. A revolutionary ESD protection concept may be an ideal zero-leakage mechanical switch built above Si that is triggered by ESD transients.

Graphene were widely investigated to make electron devices due to its high electron mobility (~5000 cm^2/V-s) [6], [7], however, with little practical success due to its zero bandgap nature. On the other hand, its excellent mechanical properties, e.g., Young's modulus of ~1T Pa [8] and light mass density, make it possible to build graphene-based mechanical devices. For example, low-current DC graphene mechanical switching phenomena was reported recently [9], [10]. Targeting for low static power dissipation for ICs, the reported DC graphene switches have major problems: it has slow switching time (~40ns) and can only survive a few switching times before failure [9], [10]. We report the first dual-polarity transient graphene NEMS (gNEMS) switch ESD protection mechanism and structures in this letter.

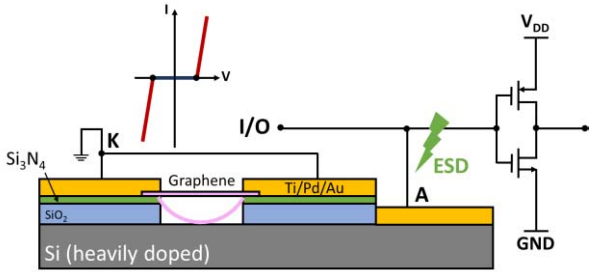

Fig. 1. Cross-section and circuit scenario for the new gNEMS switch ESD protection structure. The normal-OFF switch can be turned on by pulling down the graphene membrane by ESD pulses. The inset illustrates an ideal ON-OFF I-V behavior for the gNEMS ESD switch.

II. Graphene Nems Esd Switch

A. A Novel ESD Concept

Figure 1 illustrates a conceptual graphene NEMS switch ESD protection structure and its application scenario. The gNEMS ESD switch is a two-terminal device with a vacuum gap between a conducting substrate (Si or metal serving as the anode, A) at the bottom and a suspended graphene membrane on top serving as the cathode (K). In a typical on-chip ESD protection design, A is connected to an I/O pad and K is connected to the supply or ground buses (V_{DD}, GND). Unlike traditional in-Si PN-type ESD structures, the new gNEMS switch is a mechanical switch built in the BEOL module of ICs above the Si substrates. In normal IC operations, the gNEMS ESD switch stays OFF with minimum parasitic C_{ESD} and zero I_{leak}, ideally. As an ESD pulse appears at the I/O, the transient electrostatic force will pull down the graphene membrane to in contact with the anode, hence forming a discharge (ON) path to shunt the ESD surge. After the ESD pulse is over, the elastic force of the graphene will pull the graphene membrane back to its original position, i.e., return to OFF. The new gNEMS switch have several superior features highly desired for an ESD structure: The high carrier

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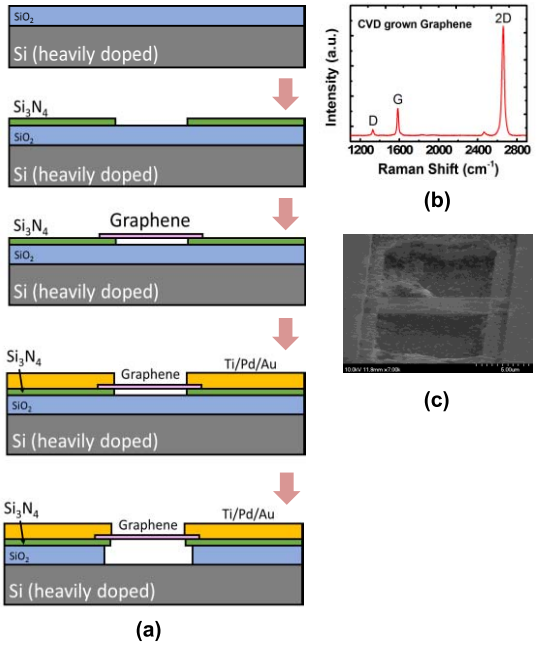

Fig. 2. (a) New CMOS-compatible gNEMS fabrication process flow. (b) Raman spectroscopy of monolayer graphene grown by CVD. (c) SEM images of a sample gNEMS switch.

mobility of graphene film ensures low R_{ON}. The high graphene thermal conductivity ($\kappa = 4.84 \sim 5.30 \times 10^3$W/m·K) [6] prevents over heating during ESD stressing. The gap-based gNEMS structure minimized ESD-induced parasitic effects including C_{ESD}, noises and I_{leak}. The light mass and relatively high Young's modulus [8], [11] allows fast switching, critical to fast ESD protection requirements. The super mechanical strength of graphene also ensure high ESD robustness. Ideally, a gNEMS switch is a dual-polarity device that can significantly reduce the total ESD device head counts in ICs [1]. A big advantage of gNEMS ESD switch is that, because it is an above-IC device, the new gNEMS ESD structures can be placed above Si ICs through 3D heterogeneous integration. Since ESD structures are often very large, the new above-IC gNEMS ESD switch can not only alleviate IC layout headaches, but also save the precious Si assets. This means that normal IC designers will not have to include ESD protection structures during their core circuit designs, which may be handled in the back-end flow of IC designs and fabrication, thus, a paradigm change in on-chip ESD protection designs.

B. gNEMS ESD Switch Fabrication

A fully CMOS-compatible device fabrication process flow is critical to achieving 3D heterogeneous integration of the proposed gNEMS switches with ICs, hence realize the novel above-IC ESD protection concept. Figure 2a illustrates the device fabrication process flow developed in this work. First, a thin Si_3N_4 layer of 100nm is grown on a SiO_2(300nm)/Si (heavily doped p-type) substrate by low pressure chemical vapor deposition (LPCVD). The Si_3N_4 was then patterned by etching to define the gNEMS trench. Next, single (or many) layer graphene film was produced by CVD method, suitable for making large area graphene film, followed by Raman evaluation (Figure 2b). The graphene film was then transferred

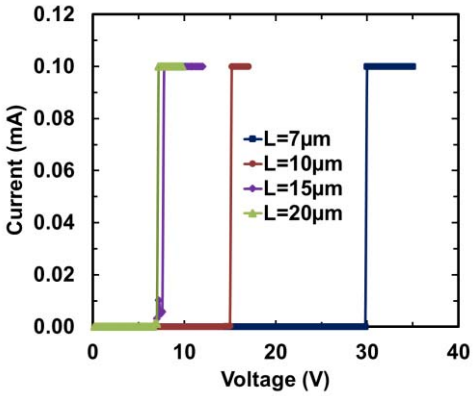

Fig. 3. DC sweeping test for sample gNEMS devices shows static switching effect with V_{ON} affected by the graphene membrane length (7.0, 7.6, 15, 29.8V).

onto the trenched substrate where graphene is completely attached to the surface to avoid graphene breakage during subsequent steps. Next, the graphene was patterned by oxygen plasma to form graphene beams. The top electrodes were made of Ti/Pd/Au (5/30/50nm) by deposition and etching. Last, the graphene membrane was released by HF vapor etch of SiO_2 using Si_3N_4 as hard mask to form an air chamber, resulting in a gNEMS switch device. Si_3N_4 layer was used to prevent graphene lift-off from electrode pads, because etching into Si_3N_4/graphene interface by HF vapor is negligible compared to SiO_2/graphene interface. The graphene membrane was released using HF steaming to avoid liquid environment to improve device yield and possibly use the hydrophilic property of monolayer graphene [9]. The undercut into the SiO_2 trench by HF vapor is negligible because the SiO_2 layer is very thin. Figure 2c is SEM image of a gNEMS ESD switch fabricated where the suspended graphene membrane is observed.

III. Characterization and Discussions

A large number of prototype gNEMS ESD switch structures were designed and fabricated for both static and transient switching characterization. The ESD-critical parameters of the gNEMS switch structures are affected by many factors such as shapes, sizes and dimensions of the chamber and graphene membranes, as well as the fabrication processes and quality of the gNEMS devices. Various device parameters (i.e., design splits) were used for the gNEMS prototypes, including chamber depth (d = 350nm), graphene membrane film length (L = 7/10/15/20μm) and width (W = 5/7/10μm).

Static switching effect was first characterized by applying a DC bias between the top and bottom contacts. As the bias increases, the suspended graphene film is pulled-in towards the bottom by electrostatic forces, resulting in DC switching, as shown in Figure 3 where DC turn-on voltage (V_{ON}) is related to L of the sample gNEMS devices, likely due to changes in the pull-in forces associated with a varying L.

For ESD protection operations, transient ESD switching is critical, which were performed using TLP test for human body model (HBM) ESD characterization. Figure 4 depicts a transient I-V curve for a sample gNEMS switch (L = 7μm, W = 5μm) under TLP stress (ESD pulse rising time t_r = 200ps and duration t_d = 100ns), which clearly shows

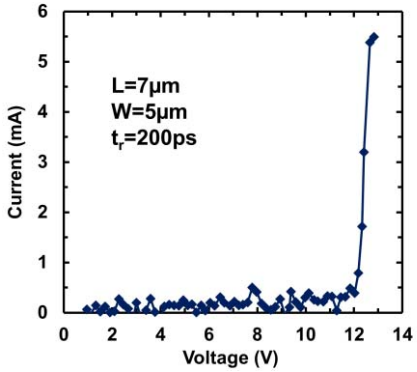

Fig. 4. Measured I-V curve by TLP pulsing for a prototype gNEMS device shows transient ESD switching with a fast response time down to 200ps.

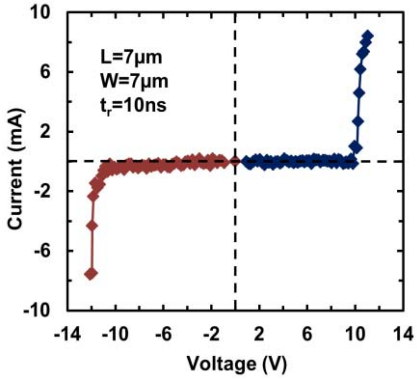

Fig. 5. Measured I-V curve by TLP for a prototype gNEMS device shows near symmetric I-V switching behaviors desired for ICs. The slight asymmetry is attributed to the asymmetric prototype device structure used (Figure 1).

ultra-fast switching behavior with $V_{t1} \sim 12V$. The transient switching effect induced by fast ESD pulse is different from static switching caused by a DC bias in that transient switching may be greatly affected by extra pulling force associated with the large and sudden change in electrostatic force density induced by an ESD pulse. Hence, a lower V_{t1} threshold and much faster switching time are expected that were confirmed in TLP test. Uniquely, an ESD switch must be able to respond to extremely fast ESD transients, which is made possible due to the light mass and relatively high Young's modulus of a graphene film. The critical ESD triggering voltage (V_{t1}) values may be accurately controlled by careful designs of L, W and d of a gNEMS switch, which showed a wide range of V_{t1} (7∼17.5V) measured. The accurate relationship between V_{t1} and gNEMS switch dimensions requires more research to improve the fabrication processes and device quality. Figure 5 depicts a near symmetric switching I-V behavior, which is highly desirable for full-chip ESD protection to reduce ESD device head counts [1], hence ESD area size and parasitic effects. Measurement shows ultra-low leakage of I_{leak}∼3-13pA at DC bias of 0.5-3V expected for normal IC operations. TLP testing reveals exceptionally high current handling capability of $I_{max} \sim 10^8 A/cm^2$ ($>1.5kV/\mu m^2$), much higher than existing in-Si PN-type ESD structures (e.g., $\sim 7.5V/\mu m^2$ for an SCR ESD device).

Reliability of the new gNEMS switch structures were characterized by repeating ESD switching tests by TLP stresses. It was observed that the prototype gNEMS devices maintained good switching property after more than 30 switching times by TLP tests. Considering that the measured samples were initial prototype devices only, it is expected that both switching performance and reliability of the gNEMS switches can be much improved to enable practical applications. Our on-going optimization research include graphene growth, switch structures and fabrication processes. For example, graphene quality must be controlled for better switch reliability and dielectric leakage has to be avoided.

IV. Conclusion

We report the first transient graphene gNEMS ESD switch structures. TLP testing shows symmetric transient switching with ultra-fast ESD response time down to 200ps, adjustable ESD V_{t1} by design splits and low leakage of a few pA. The gNEMS devices remain functional after 30 times of TLP zapping. A CMOS-compatible process flow was developed to allow 3D heterogeneous integration with ICs. The novel 3D above-IC gNEMS ESD switch structure offers a revolutionary on-chip ESD protection solution for future ICs.

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