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Integrated Circuits and Wireless Receiver Arrays Above 100 GHz with Dynamic Power Consumption

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Jonathan Gar-Kai Tao

Committee in charge:

Professor James Buckwalter , Chair
Professor Mark Rodwell
Professor Loai Salem
Professor Forrest Brewer

September 2026

The Dissertation of Jonathan Gar-Kai Tao is approved.

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June 2026

Integrated Circuits and Wireless Receiver Arrays Above 100 GHz with Dynamic Power Consumption

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by

Jonathan Gar-Kai Tao

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First, I express gratitude and thanks to my advisor, Professor James Buckwalter, who granted me the privilege of working under his mentorship throughout my Ph.D. studies. He has guided me and my circuits to connect with larger systems, even when those systems seemed too far away to comprehend. He has supported me through moments of extreme delays, especially during the final stages of building systems where so much work is at stake. I thank my committee members, Professor Mark Rodwell, Professor Loai Salem, and Professor Forrest Brewer for their teaching and advice on this work. I am grateful for the opportunity provided by the Semiconductor Research Corporations (SRC), through ComSenTer and CogniSense, to connect and collaborate with other researchers in the community. I appreciate the support granted to me by the SRC and pSEMI through their generous funding.

Taking circuits from design to physical reality would not have been possible without access to integrated circuit technologies and fabrication. I thank GlobalFoundries, for access to the 90-nm SiGe 9HP+ technology, Bill Deal at Northrop Grumman, for access to the 35-nm InP HEMT technology. I am grateful to the staff of the UCSB Makerspace, for making it possible to make printed mounts for measurement in a tight timeframe, and also of the UCSB College of Engineering machine shop under Andy Weinberg, for access and guidance to designing and machining my own parts for packaging. For assembly of the receiver modules, I greatly appreciate the patience and tenacity of Advotech in working with my non-standard materials and creative assembly processes.

The community in which I developed this work was unequivocally instrumental. I thank Utku Soylu for inspiration, as we worked on frequency multipliers at around the same time and encountered similar problems with them. I am thankful to Wonho Lee, who worked beside me and guided me through the beginnings of my own highly integrated

BiCMOS circuit design with those ideas, Aaron Wissing, for helping me begin my own journey into the world of module packaging, and Cheol So, who showed me what I should expect towards the end of creating a large arrayed system. For guiding me through measurement of my own circuits, I thank Jeff Chien, Rohit Karnaty, Andrea Arias-Purdue, and Everett O'Malley. I thank Professor Gabriel Rebeiz for lending measurement equipment on a short notice. I am indebted to Wanshu Zheng at Georgia Tech who saved my antenna project with countless hours in fabrication. I express my appreciation to current and former members of the Buckwalter, Rodwell, and Schow groups, with whom I often traded knowledge, measurement assistance, equipment, and food.

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Curriculum Vitæ

Jonathan Gar-Kai Tao

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J. Tao, M. Tom and J. F. Buckwalter, "An Ultra-Compact D-Band SiGe Low Noise Amplifier for Array Integration," 2025 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Phoenix, AZ, USA, 2025, pp. 1-4, doi: 10.1109/BCICTS63111.2025.11211424.

J. Tao and J. F. Buckwalter, "A D-band SiGe Subharmonic Downconverter with Dynamic Conversion Gain and Fixed Input Compression," 2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Fort Lauderdale, FL, USA, 2024, pp. 199-202, doi: 10.1109/BCICTS59662.2024.10745700.

J. Tao, E. Lam and J. F. Buckwalter, "A 170-260 GHz SiGe Frequency Doubler with 5-dBm Output Power and 13-dB Input Power Range," 2024 19th European Microwave Integrated Circuits Conference (EuMIC), Paris, France, 2024, pp. 22-25, doi: 10.23919/EuMIC61603.2024.10732812.

J. S. -C. Chien, E. Lam, **J. Tao** and J. F. Buckwalter, "Strong Fundamental Rejection in Frequency Doublers at 220–260 GHz Using a 250-nm InP HBT Process," 2024

IEEE/MTT-S International Microwave Symposium - IMS 2024, Washington, DC, USA, 2024, pp. 166-169, doi: 10.1109/IMS40175.2024.10600368.

J. Tao, W. Lee, J. S. -C. Chien and J. F. Buckwalter, "A 185-GHz Low-Noise Amplifier Using a 35-nm InP HEMT Process," in IEEE Microwave and Wireless Technology Letters, vol. 34, no. 5, pp. 501-503, May 2024, doi: 10.1109/LMWT.2024.3351069.

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A. Hamza, A. Nagulu, A. F. Davidson, **J. Tao**, C. Hill, H. AlShammary, H. Krishnaswamy and J. Buckwalter, "A Code-Domain, In-Band, Full-Duplex Wireless Communication Link With Greater Than 100-dB Rejection," in IEEE Transactions on Microwave Theory and Techniques, vol. 69, no. 1, pp. 955-968, Jan. 2021,
doi: 10.1109/TMTT.2020.3035354.

Abstract

Integrated Circuits and Wireless Receiver Arrays Above 100 GHz with Dynamic Power Consumption

by

Jonathan Gar-Kai Tao

Wireless systems for sensing and communication networks are under increasing demand to provide the fusion of radar and radio into a single hardware platform to cooperatively take advantage of the wide spectrum availability in the frequency bands from 100 GHz - 300 GHz. The cooperation enhances communication by spatial localization and improves radar by distributed coordination in dynamic channel environments with an MIMO system. However, the power consumption of transmit and receive arrays increases at higher frequency and becomes prohibitive in mobile applications where the power budget is limiting. Because wireless environments are dynamic, there is potential to save power in advantageous conditions to enable these systems.

First, we present circuit techniques for frequency multiplication that enable dynamic reduction of power in the LO chain to improve energy efficiency in array receivers. This is in contrast with conventional receiver arrays using a single LO power and system power consumption for a specific condition. We present a G-band frequency doubler in 90-nm SiGe BiCMOS technology with a novel bias feedback adaptation. This technique linearizes gain and improves controllability of the frequency doubler's output power with no penalty in power consumption, area, or output power. Second, the technique applied to a fourth subharmonic D-band downconverter in 90-nm SiGe is presented, showing tradeoffs of downconversion performance against power consumption through LO power. Third, LNA designs in 35-nm InP HEMT for heterogeneous integration and 90-nm SiGe

BiCMOS for monolithic array integration are presented, with exploration of noise measure as a metric to optimally extract transistor performance. Finally, we present a 4-element IQ receiver array in 90-nm SiGe packaged as a module with wideband dual slotted patch antennas to exhibit application of the bias feedback technique in adapting receiver power consumption to varying FMCW radar sensing conditions. In over-the-air experiments, the module exhibits reconfigurability along a SNR-to-power cost for varying target detection, highly supporting the use of bias feedback adaptation for varying LO power in applications of joint radar and radio systems in highly dynamic environments.

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Chapter 1

Introduction

1.1 Wireless Systems in Dynamic Environments Above 100 GHz

Wireless systems for sensing and communication networks are under increasing demand to provide the fusion of radar and radio into a single hardware platform to cooperatively take advantage of the wide spectrum availability in the frequency bands from 100 GHz - 300 GHz. The cooperation enhances communication by spatial localization and improves radar by distributed coordination in dynamic channel environments with an MIMO system. However, the power consumption of transmit and receive arrays increases at higher frequency and becomes prohibitive in mobile applications where the power budget is limiting [1]. Because wireless environments are dynamic, there is potential to save power in advantageous conditions to enable these systems.

In addition to circuit and process technologies requiring higher power consumption at high frequencies above 100 GHz, systems at these frequencies must scale their number of elements to compensate for the path loss [2]. The received power P_t over a distance

can be expressed as

$$P_r = SA_r = \left(\frac{P_t G_t}{4\pi d^2}\right)\left(\frac{G_r \lambda^2}{4\pi}\right) \tag{1.1}$$

where P_t is the transmitted power, G_t and G_r are the transmit and receive antenna gains, λ is the wavelength of the transmitted power, and d is the distance of the transmission path. S is the radiated power density, while A_r is the effective aperture area. Substituting the antenna gains with a representation involving number of elements and total beam scan width in solid angle, the path loss is presented as

$$\frac{P_r}{P_t} = \frac{N_t N_r}{\Omega_t \Omega_r}\left(\frac{\lambda^2}{d^2}\right) \tag{1.2}$$

where N_t and N_r are the number of transmit and receive elements with Ω_t and Ω_r representing the total beam scan width of the arrays as a solid angle. This representation of path loss, shows that wireless arrays must scale with increasing frequency to maintain the same path loss, which leads to an even higher power consumption in the case where the power per element remains constant with scaling.

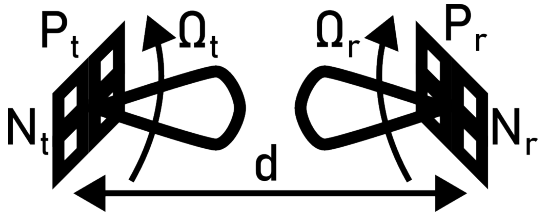


Figure 1.1: Path loss of power between transmitter and receiver and their parameters.

The typical path loss represents ideal wireless propagation conditions, but applications of both communications and sensing in real-world conditions, atmospheric attenuation is a significant source of additional loss, especially at frequencies above 100 GHz,

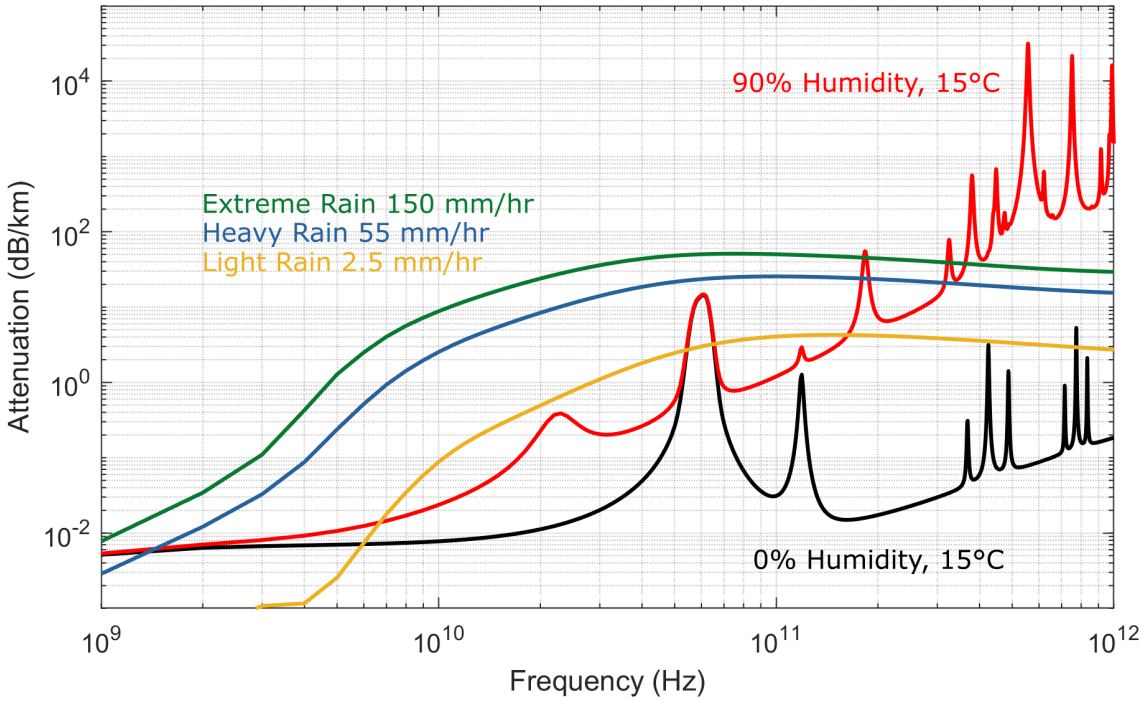


Figure 1.2: Atmospheric attenuation across frequency with dynamic moisture and rain variation specified by models from the International Telecommunication Union (ITU)[3][4].

as shown in Fig. 1.2. In this case, with $e^{-\alpha d}$ representing the atmospheric attenuation over distance included, the signal power arriving at the receiver is

$$P_r = P_t \frac{N_t N_r}{\Omega_t \Omega_r} \left(\frac{\lambda^2}{d^2}\right) e^{-\alpha d} \geq MDS \tag{1.3}$$

with the receiver's minimum detectable signal $MDS = kTBF \cdot SNR$, where k is the Boltzmann constant, T is temperature, B is signal bandwidth, F is the receiver's noise factor, and SNR is the signal to noise ratio requirement of the system. The path loss with atmospheric attenuation represents an additional challenge for systems above 100 GHz, since systems must compensate for the higher path loss in situations with high moisture or rain. Potentially, an array system could adapt to these dynamic conditions to save power in dry conditions while maintaining SNR.

Another case of dynamic conditions is with wireless sensing. In the case of ranging with a frequency-modulated continuous wave (FMCW) signal, the SNR is given as

$$SNR = \left(\frac{\sigma}{d^4}\right)\left(\frac{G_T G_R \lambda^2}{(4\pi)^3 kT}\right)\left(\frac{P_T T_c}{F}\right), \tag{1.4}$$

where σ is target radar cross section (RCS), P_T is the transmitted power, G_T and G_R are the transmitter and receiver antenna gain, λ is the wavelength, T_c is the dwell time, d is the range, T is the receiver temperature , and F is the receiver noise factor [5]. The SNR of sensing varies with the dynamic conditions of the RCS, of physically different targets with changing orientation, and the range, of targets in different positions and moving. The first term in parenthesis is determined by the target, the second term are parameters of the transmit and receive antenna array, and the third term are parameters that can be readily adapted in real time by the transmit and receive systems. A system may adapt to the sensing conditions to maintain SNR using parameters in the third term, with P_t from the transmitter and T_c from sampling for a longer period of time. From the standpoint of using the receiver to adapt its performance to these conditions, a conventional receiver's F represents another potential for adaptation.

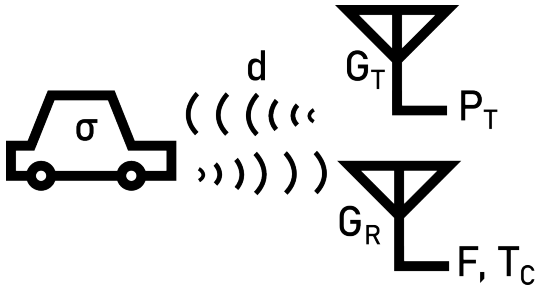


Figure 1.3: Power and parameters for SNR in radar detection of a target.

Implementing systems above 100 GHz requires scaling to arrays, which also scales power consumption to a point that may be prohibitive. Yet, environmental conditions are dynamic, granting an opportunity to have a system with less power consumption

compared to the worst case. The challenge is to have the ability at all to take advantage of better conditions. A typical receiver is shown in Fig. 1.4, with an LNA to suppress noise, a mixer for frequency conversion, an IF gain block to signal amplification, and an LO system to generate high frequencies to drive the mixer. Conventional receiver arrays use a single saturating LO power, which results in a single system power consumption. Their designs are optimized for that LO power with the intention of achieving acceptable SNR performance for a specific wireless channel condition [6]. For a highly dynamic receiving condition, high power consumption would result from optimizing for the worst case conditions to maintain performance, despite potential to operate at a lower power at other times when higher performance is not necessary. Notably, the circuits within systems that dominate system power consumption, especially above 100 GHz, are typically low-noise amplifiers (LNA) and the LO multiplier chain, exemplified in Table 1.1. Thus, the ability of a receiver to change its power consumption through its LO chain is significant in its potential to adapt system power consumption to dynamic communication or sensing environments.

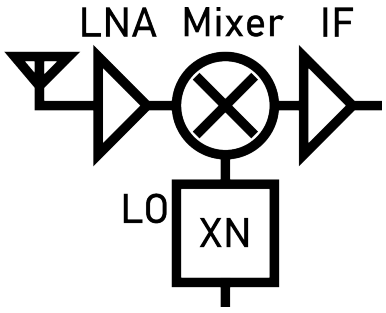


Figure 1.4: Basic components of a receiver.

The goal of this work is to develop circuit techniques that enable dynamic reduction of power in the LO chain, implementation of those concepts in a full receiver array above 100 GHz, and demonstration of system power consumption adaptation to change or maintain SNR. The culminating demonstrator is a 4-element IQ receiver module in 90-nm SiGe

Table 1.1: Examples of D-band System Power Consumption by Component

Ref.	Type	LNA (mW)	TX PA (mW)	Mixer (mW)	IF (mW)	Digital Beamformer (mW)	LO (mW)	Total (mW)	LO Portion of Total
[7]	4Rx, IQ	163	-	0	109	-	233	495	47%
[8]	1Rx/1Tx, IQ	42	126	0	22	-	215	405	53%
[9]	1Rx	30	-	14	32	-	57	133	42%
[1]	64Rx Simulated	325	-	0	828+ 261 (ADC)	204.8	6272	7881	80%

* Calculated with insertion gain $\|S_{21}\|^2$ and average of the reported range of noise figures.
† Calculated with power consumption per stage, $P_{DC,Stage}$.

BiCMOS that includes components and techniques developed in this work.

The first challenge encountered with varying power through the LO chain, particularly ones implemented with frequency multipliers, is extreme sensitivity to input power, as shown in Fig. 1.5.

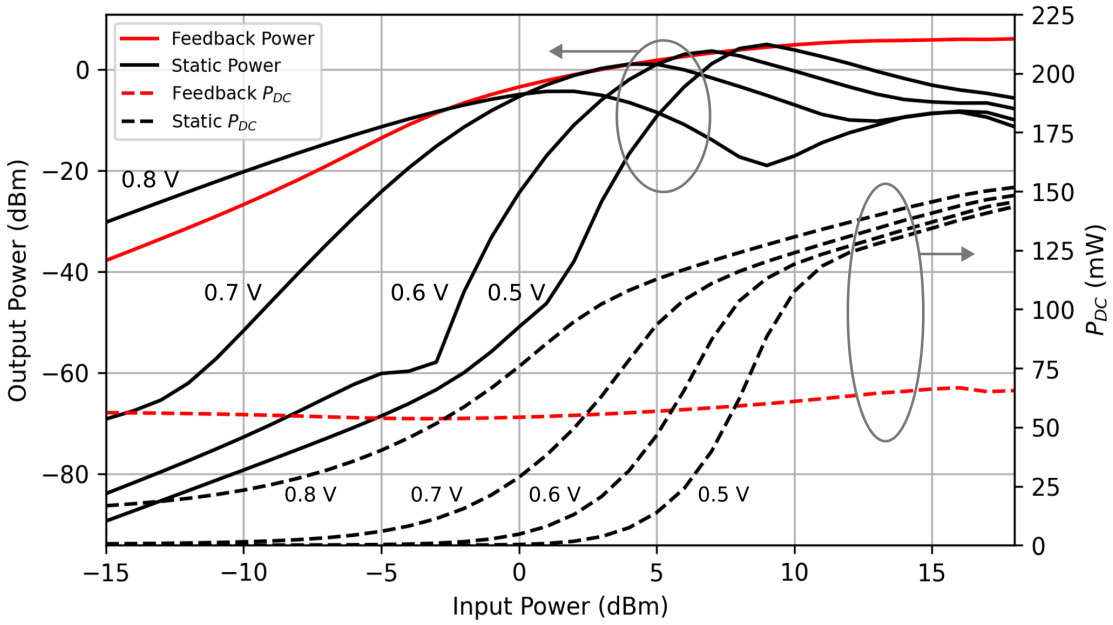


Figure 1.5: Simulation of power sensitivity in a typical static bias frequency multiplier compared to one with novel bias feedback technique.

This sensitivity was found to be caused by inherent variation in circuit bias current as one varies input power these frequency multiplier circuits, and a solution in the form of novel bias feedback is found and presented. Since the goal is to apply these concepts to a

receiver, a downconverter that takes advantage of the bias feedback technique is presented with demonstration of LO control trading off performance and power consumption.

With the goal of saving power in the receiver, LNAs for heterogeneous and monolithic integration are explored. Heterogeneous integration of other process technologies provides better performance for the power consumption paid compared to monolithic integration in typical CMOS technology, and an example in InP is presented. While technologies for heterogeneous has performance advantages, it has drawbacks in the costs of yield and physical integration with a receiver. Due to these drawbacks, a SiGe LNA for monolithic integration is explored and presented in contrast to ones in alternate process technologies.

Each of these works are major components in receivers, as shown in in Fig. 1.4, and were brought together in the final culminating demonstrator receiver. LO control was implemented for both phase and power control for delivery for the full array receiver, allowing for dynamic control of LO power and power consumption saving. A dynamic sensing environment with FMCW radar was used to demonstrate tradeoffs between SNR and power through this control. This resulted in a quantifiable cost in that tradeoff and proved the ability to dynamically move along that cost to obtain a target SNR or lower power consumption, shown in Fig. 1.6. These experiments clearly demonstrate the ability of receivers with LO control to adapt and save power in dynamic environments, enabling radio above 100 GHz for mobile applications.

1.2 Contributions and Organization

Chapter 2 presents circuit techniques for frequency multiplication that enable dynamic reduction of power in the LO chain to improve energy efficiency in array receivers. This is in contrast with conventional receiver arrays using a single LO power and system power consumption for a specific condition. We present a G-band frequency doubler in

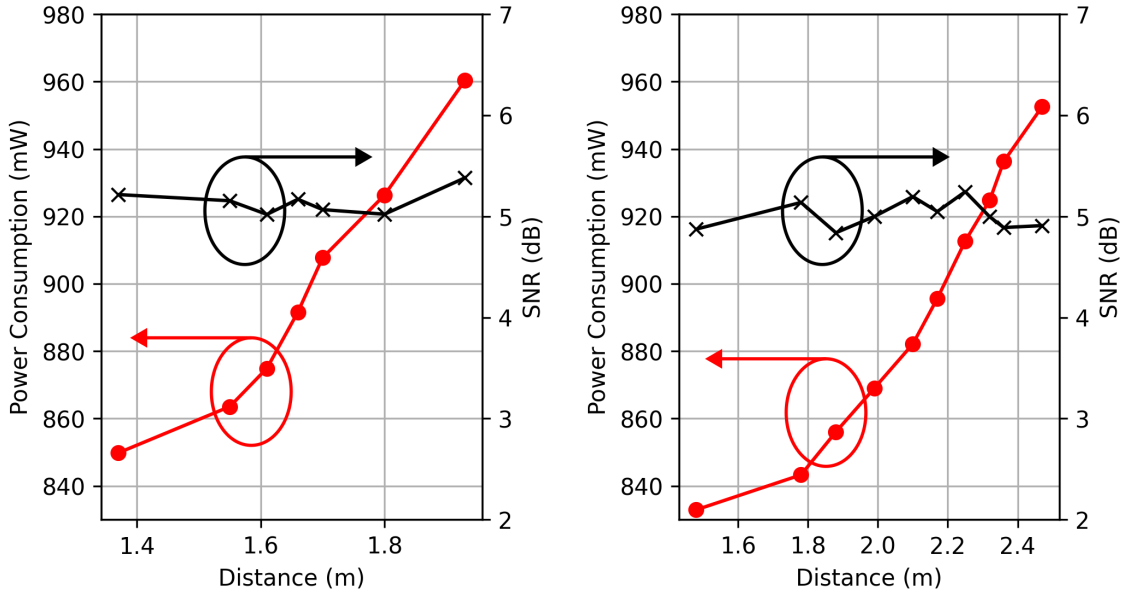


Figure 1.6: Measured power consumption of the culminating receiver module in FMCW ranging. The receiver maintains 5 dB of SNR for spherical target detection across distances for (a) 0° and (b) 40° of array beam steering, trading off with power consumption.

90-nm SiGe BiCMOS technology with a novel bias feedback adaptation. This technique linearizes gain and improves controllability of the frequency doubler's output power with no penalty in power consumption, area, or output power.

Chapter 3 presents the bias feedback technique applied to a fourth subharmonic D-band downconverter in 90-nm SiGe. The technique enables adaptation of performance and power consumption through LO power. The circuit exploits the fourth harmonic content of a push-pull frequency multiplier to achieve a high multiplication factor without sacrificing additional area, power consumption, or LO power requirement for a cascaded multiplier chain. The adaptation makes this circuit suitable for applications of joint radar and radio systems in dynamic environments. Tradeoffs of downconversion performance against power consumption through LO power are shown.

Chapter 4 presents a 4-stage 35-nm InP HEMT for heterogeneous integration with a CMOS receiver system. The use of noise measure is explored as a way to extract maximum performance from the transistors in the LNA. The design features coplanar transmission line design with source degeneration. First P1dB compression measurements across frequency in this technology are presented.

Chapter 5 presents a wideband, ultra-compact LNA in 90-nm SiGe BiCMOS for monolithic array integration are presented. The design features multiple cascaded stages with staggered tuning to provide gain at multiple bands, leading to wideband performance. The LNA achieves comparable performance with other LNA above 100 GHz, while consuming an extremely low amount of chip area. With an order of magnitude less in area consumption in comparison to others, this design is suitable for highly scaled receiver systems.

Finally in Chapter 6, we present a 4-element IQ receiver array in 90-nm SiGe packaged as a module with wideband dual slotted patch antennas to exhibit application of the bias feedback technique in adapting receiver power consumption to varying FMCW radar sensing conditions. In over-the-air experiments, the module demonstrates reconfigurability along a SNR-to-power cost for varying target detection, highly supporting the use of bias feedback adaptation for varying LO power in applications of joint radar and radio systems in highly dynamic environments.

1.3 Permissions and Attributions

The material in the following publications is used in this dissertation. The primary contributor to those publications is the author of this dissertation.

1. J. Tao, E. Lam, and J. F. Buckwalter, "A 170-260 GHz SiGe Frequency Doubler with 5-dBm Output Power and 13-dB Input Power Range," in 2024 19th European Microwave Integrated Circuits Conference (EuMIC), Sep. 2024, pp. 22–25. doi: 10.23919/EuMIC61603.2024.10732812.

2. J. Tao and J. F. Buckwalter, "A D-band SiGe Subharmonic Downconverter with Dynamic Conversion Gain and Fixed Input Compression," in 2024 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Oct. 2024, pp. 199–202. doi: 10.1109/BCICTS59662.2024.10745700.

3. J. Tao, W. Lee, J. S.-C. Chien, and J. F. Buckwalter, "A 185-GHz Low-Noise Amplifier Using a 35-nm InP HEMT Process," IEEE Microwave and Wireless Technology Letters, vol. 34, no. 5, pp. 501–503, May 2024, doi: 10.1109/LMWT.2024.3351069.

4. J. Tao, M. Tom, and J. F. Buckwalter, "An Ultra-Compact D-Band SiGe Low Noise Amplifier for Array Integration," in 2025 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), Oct. 2025, pp. 1–4. doi: 10.1109/BCICTS63111.2025.11211424.

Chapter 2

Push-pull Frequency Doubler with Bias Feedback Adaptation

2.1 Introduction

As wireless communications or sensing requirements change, the conversion gain of the mixer can be adjusted with LO power, eliminating other variable-gain amplifiers in beamforming applications, further decreasing system power consumption and area. A variable power frequency multiplier can adaptively respond to link and power requirements. The LO chain, illustrated in Fig. 2.1a, multiplies a reference frequency and amplifies the LO signal for frequency conversion. Based on the frequency multiplication factor and the LO power required to drive the mixer into saturation, the LO chain above 100 GHz places significant demands on the circuit power consumption. Circuit techniques that reduce power consumption in the LO chain support more energy efficiency in the transmitter and receiver.

The basic frequency multiplier is illustrated in Fig. 2.1a and uses push-pull transistors operating in class B or C mode. To increase the conversion of the input frequency f_0 to

a $2f_0$, the doubler might include a bypassed resistive degeneration or use a bypassed tail current [10] as shown in Fig. 2.1b. These methods consume voltage headroom, which require either higher voltage operation or sacrificing maximum output power in a low voltage system.

In this chapter, a G-band (170-260 GHz) frequency doubler is realized in a 90-nm SiGe BiCMOS process. Bias-feedback circuitry adapts the conversion gain over a wide range of input powers. At 190 GHz, the doubler has a peak gain of -2.0 dB and remains within 3 dB of the peak gain over a 13 dB input power range. The doubler without pads has compact dimensions of 95 µm x 135 µm, which makes it suitable for an LO chain in an array. In Section 2, we review the operation of the push-pull frequency doubler to describe the sensitivity to input power variation. Section 3 describes the proposed bias-feedback circuit. Section 4 presents the measurements between 170 and 260 GHz.

2.2 Fundamentals of Push-Pull Frequency Doublers

The schematic of the doubler in this work is presented in Fig. 2.2. Heterojunction bipolar transistors (HBTs) Q1 and Q2 form an active push-pull doubler, while Q3 forms a common-base amplifier to buffer the current and to maintain bias conditions. The current flowing through Q3 is reused by the push-pull doubler, saving power compared to an AC-coupled connection to a power amplifier stage.

In a typical doubler, the bases of Q1 and Q2 are biased with a static voltage V_{B12}, shown in Fig. 2.1a. The frequency doubler creates an output waveform that contains the desired second harmonic of the sinusoidal input frequency by rectifying a balanced signal from the input balun. Using the Fourier series expansion of the output as a current cosine pulse train, we observe that the output waveform creates additional DC current in addition to the output harmonics of interest [11][12]. The average effective output

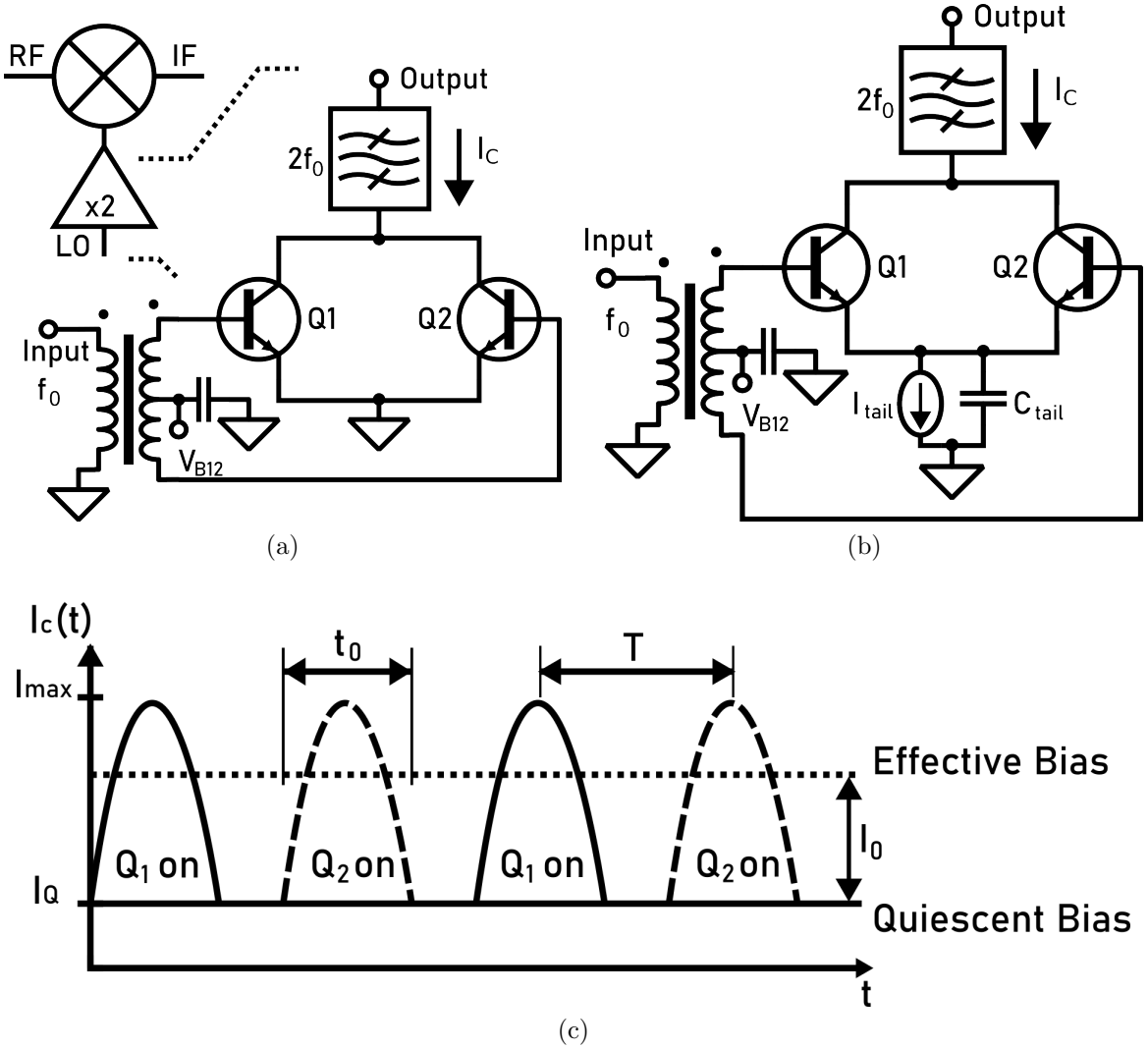


Figure 2.1: Doublers using (a) static voltage biasing and (b) degenerated tail biasing with application in a frequency conversion system. (c) Instantaneous output current from a frequency doubler and its time-average impact on bias.

current is $I_C = I_Q + I_0$, where I_Q is the quiescent bias current and I_0 is the additional current generated from the rectification of the input sinusoid.

This additional current from the output waveform changes with input voltage v_i on the bases of Q1 and Q2. The AC output current can be estimated from the linearization of the small-signal collector current i_C, based on the DC collector current I_C through the devices, e.g. $i_C = G_m(I_C)v_i$, where G_m is the time average effective transconductance.

The bias shift is calculated from

$$I_0 = \frac{4t_0}{\pi T} i_C = \frac{4t_0}{\pi T} G_m(I_Q + I_0) v_i. \tag{2.1}$$

Since the transistor transconductance is sensitive to additional rectified current, i.e. $G_m(I_Q + I_0)$, the inherently non-linear transconductance causes the conversion gain for a static bias doubler to change with the input power. The result is that the frequency multiplier would have high gain only within a narrow range of input powers, and the sensitivity to input power diminishes the ability to control and deliver a desired output power in a system. Using a bypassed tail current source on Q1 and Q2, as shown in Fig. 2.1b, can force the DC current to be constant at the expense of power consumption [10].

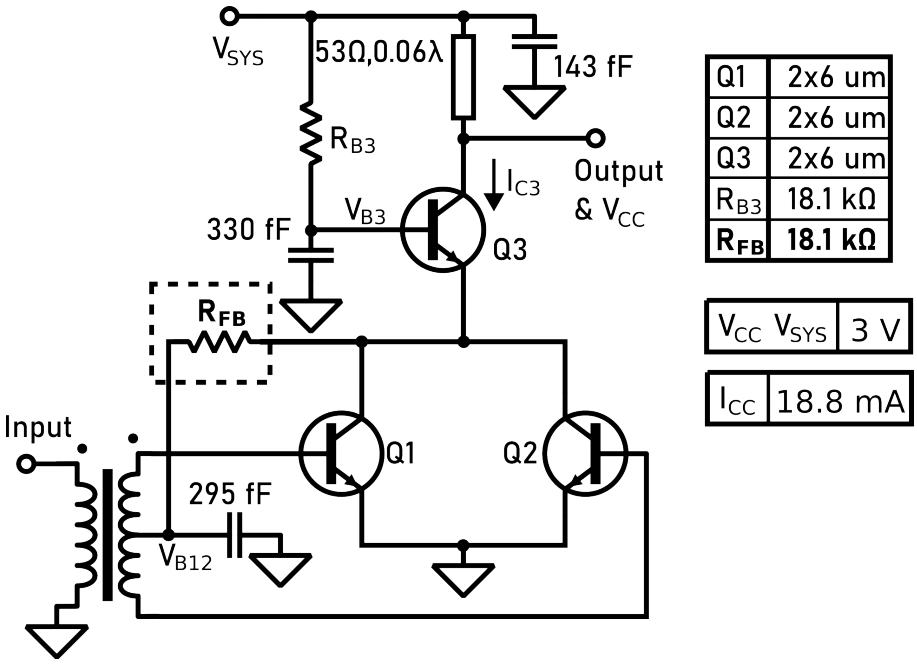


Figure 2.2: Schematic of the frequency doubler in this work with bias-feedback adaptation resistor R_{FB}. V_{CC} is provided by an output bias tee for this test structure, while V_{SYS} would be the supply for system integration.

2.3 Proposed Adaptive Bias Feedback

We propose a resistive feedback technique within frequency doublers to change base bias voltage (V_{B1} and V_{B2}), which mitigates the decrease in the bias current with decreasing input power to maintain gain. Transistor Q3 not only provides amplification but also output current detection, while resistor R_{FB} implements the feedback for adaptation. This technique does not have the drawback of increased power consumption from additional components for bias control.

The time average V_{BE3} decreases in response to a decrease in effective bias current I_C caused by the output waveform. The voltage signal from V_{BE3} is fed-back through resistor R_{FB} into the bases of Q1 and Q2 to compensate for the change in DC bias current. The AC component is not significantly affected by the resistive feedback, because the feedback resistance is large compared to the emitter impedance of Q3. In the following DC analysis of the biasing system, Q1 and Q2 are combined into an equivalent Q12, because they are shorted together at DC. The Q3 base voltage, $V_{B3} = V_{CC} - \frac{I_{C3}}{\beta_3} R_{B3}$, changes with the collector current. In this work, V_{B3} is set to 2.2 V to maximize output voltage swing. If we consider $V_{BE3} \approx V_{BE12}$ and $I_{C3} \approx I_{C12}$,

$$I_{C3} = \beta_{12} \frac{V_{B3} - 2V_{BE}}{R_{FB}} = \frac{V_{CC} - 2V_{BE}}{R_{FB}/\beta_{12} + R_{B3}/\beta_3}. \tag{2.2}$$

In this manner, the bias current for the frequency doubler is set by V_{CC} and a selection of R_{FB} and R_{B3}, reducing the influence from the additional rectified DC current through V_{BE}. Instead of being dependent on a non-linear $G_m(I_Q + I_0)$, the gain with resistive feedback is dependent on $G_m(I_{C3})$. Refer to Appendix A for additional details on the effect of this adaptive bias feedback.

The effect of the input power on gain with this bias-feedback adaptation is illustrated in Fig. 2.3, where the conversion gain varies by less than 3 dB from the peak value over a 14-dB input power range, compared to only 6-dB input power range in the static biasing case illustrated in the black curves. Fig. 2.4 plots the output power variation and DC current for the static and bias-feedback doubler circuit. While the static biasing produces similar peak output power as the feedback case, static biasing is strongly dependent on the input power with rapidly changing current consumption. The proposed bias-feedback circuit maintains bias current across a large input power range and delivers the same saturated power as a static-bias circuit with a bias tuned for a particular input power to deliver maximum power.

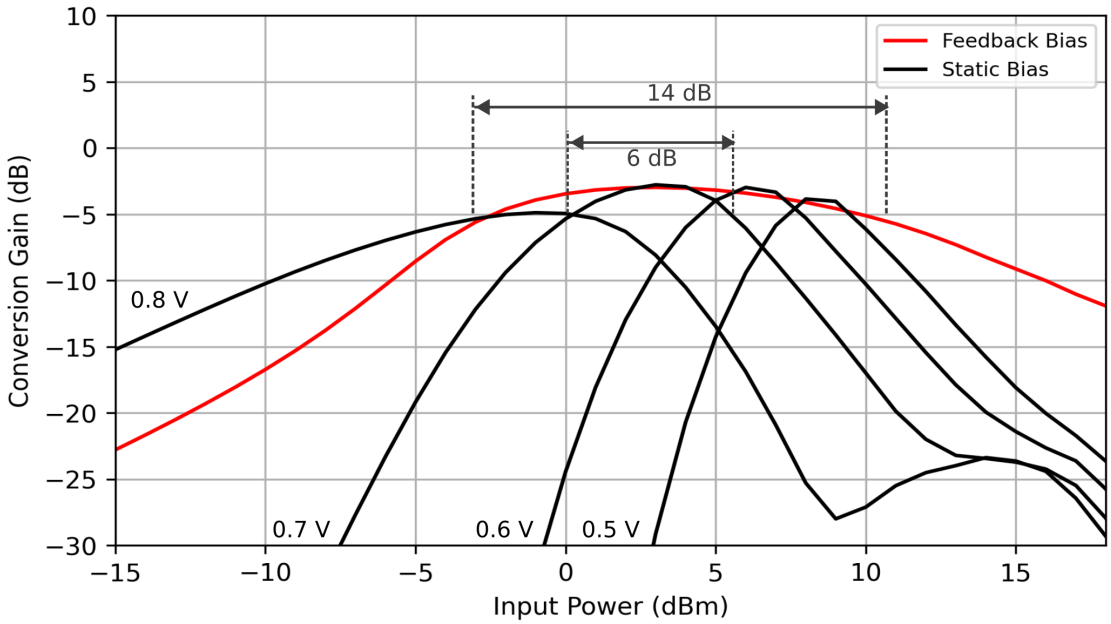


Figure 2.3: Simulated comparison on conversion gain between feedback biased and static biased frequency doubler at 210 GHz. Static bias voltages are applied at V_{B12} with no feedback resistor, as shown in Fig 2.1a.

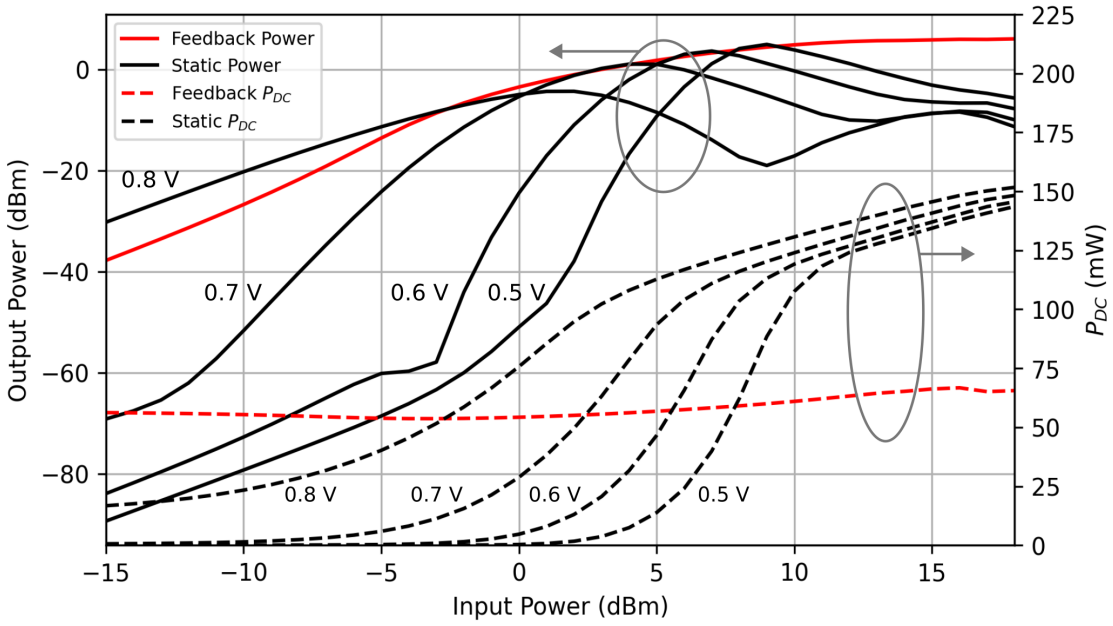


Figure 2.4: Simulated comparison on output power and power consumption between feedback biased and static biased frequency doubler at 210 GHz.

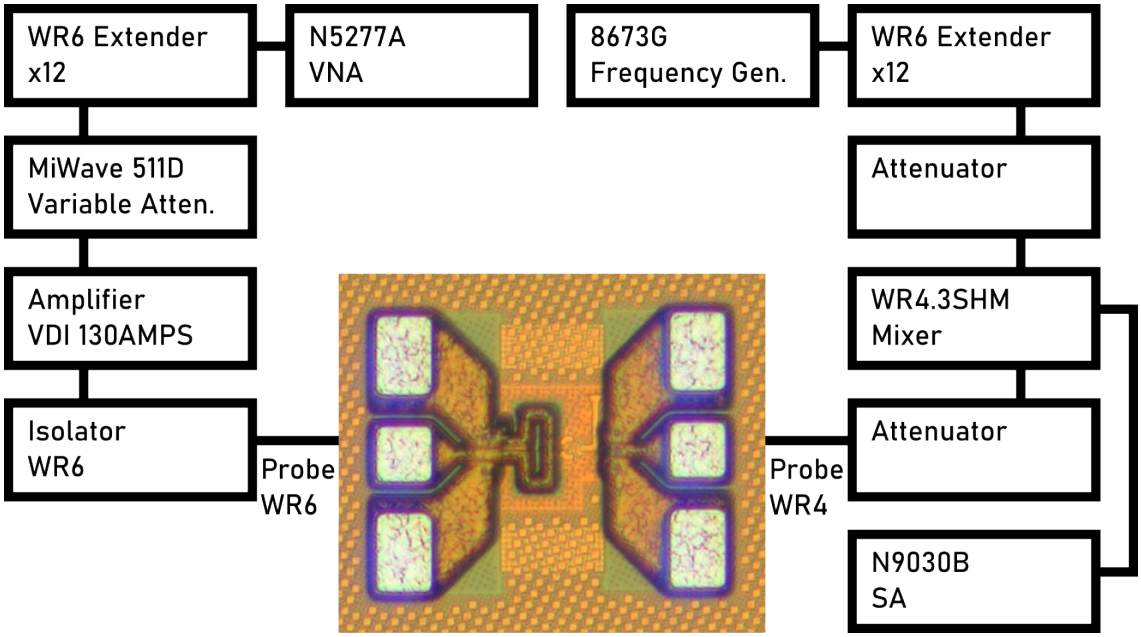


Figure 2.5: Measurement setup with D-band input and micrograph of G-band doubler with dimensions 0.095 mm x 0.135 mm without pads and 0.303 mm x 0.243 mm with pads.

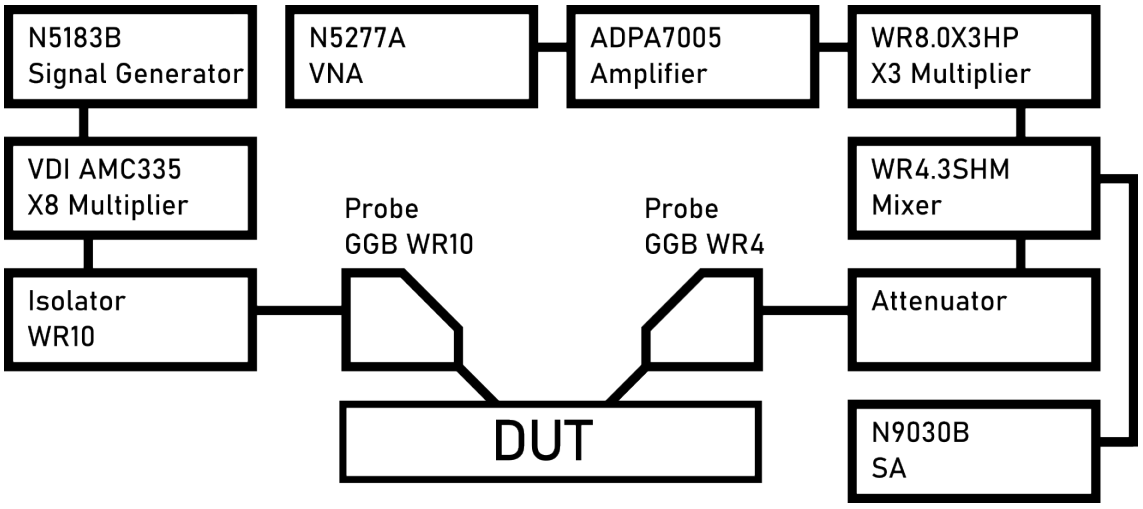


Figure 2.6: Measurement setup with W-Band input

2.4 Measurements and Results

Measurements were made on the bias-feedback frequency doubler with a 3-V supply through an output probe bias tee, supplying 14.4 mA of quiescent current on V_{CC}, while V_{SYS} is open and not implemented for this test structure. Because of the wide output bandwidth of the doubler, the measurement was split into two frequency ranges. Fig. 2.5 shows the power measurement setup at the higher D-band input range with the chip micrograph, while Fig. 2.6 shows setup at the lower W-band input range. The setup is calibrated with a VDI PM5B power meter for the input source across its power range and the output detection. The output is measured by down-converting the output spectrum of the doubler to a spectrum analyzer. The detected narrow-band power is adjusted by using the power meter as the primary calibration reference.

The doubler's output gain is measured across a range of input powers across frequency with results in agreement with simulation as shown in Fig. 2.7. In Fig. 2.8, the frequency doubler exhibits the predicted gain flatness across a wide range of input powers. At 190 GHz, the doubler has 13.0 dB of 3-dB input power range, where the gain is within 3 dB

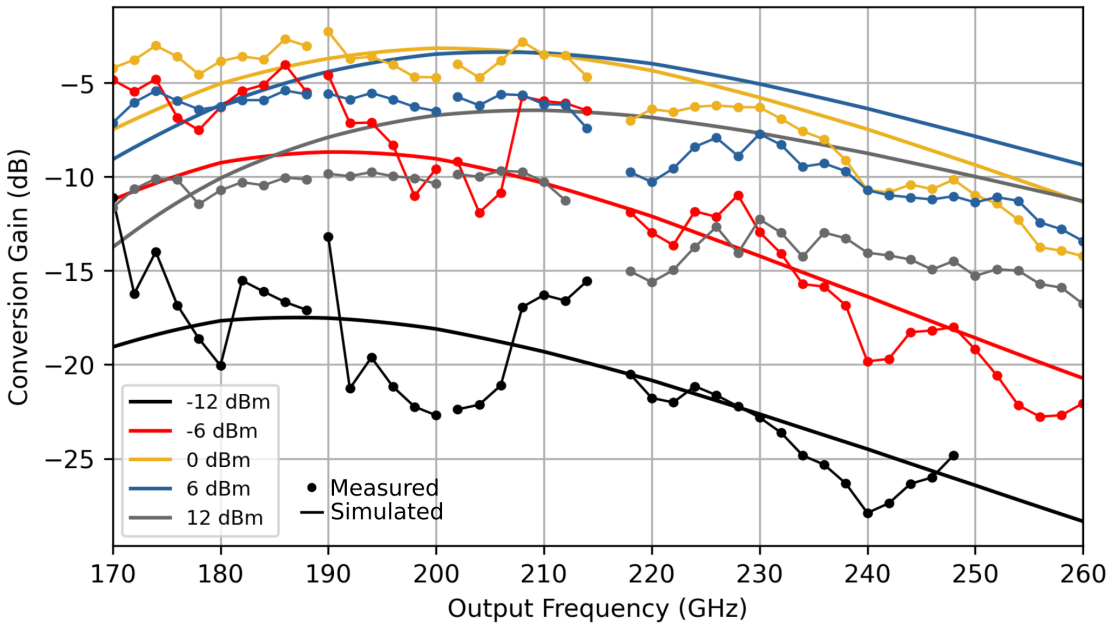


Figure 2.7: Measured gains over frequency with a selected range of input powers.

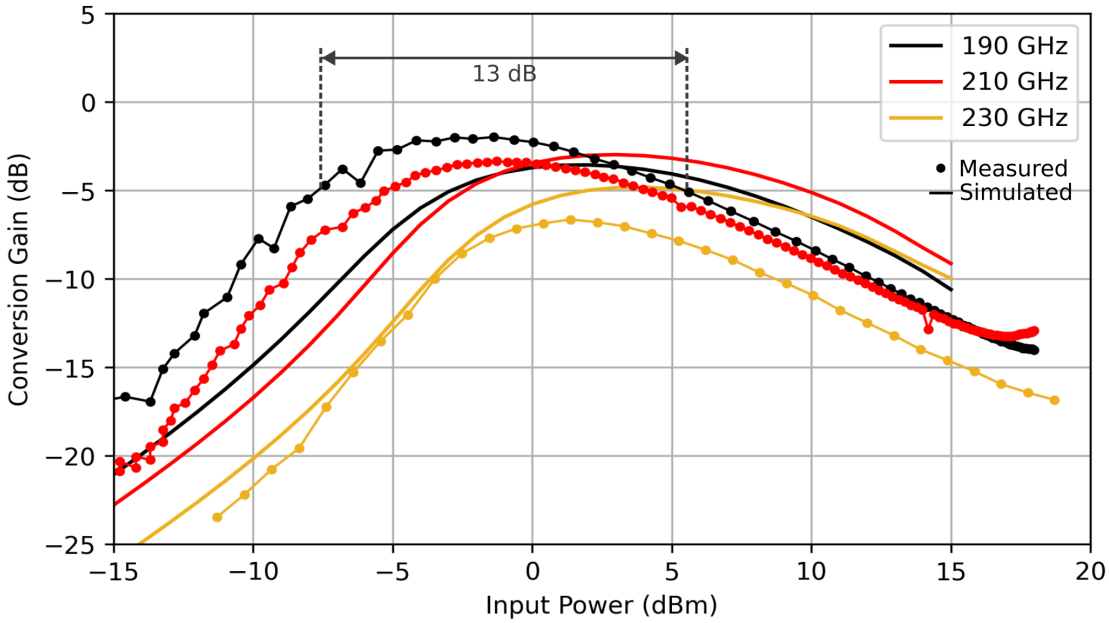


Figure 2.8: Measured gains across input powers.

of the peak gain at -2.0 dB, exemplifying the primary effect of adapting the bias of the doubler. Fig. 2.9 shows that saturated output power relationship is close to simulation,

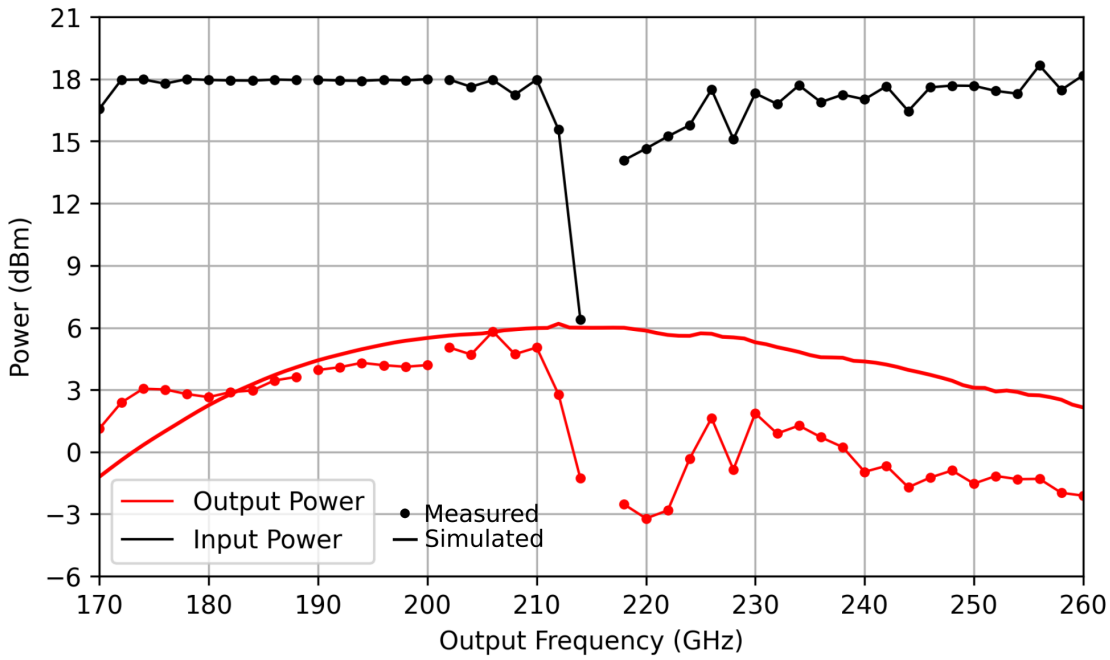


Figure 2.9: Maximum measured output power with associated input power across frequency.

Table 2.1: Performance Summary of Frequency Multipliers Above 100 GHz

Ref.	This Work	[13]	[14]	[15]	[16]	[17]
Technology	90-nm SiGe BiCMOS	55-nm SiGe BiCMOS	130-nm SiGe BiCMOS	130-nm SiGe BiCMOS	90-nm SiGe BiCMOS	45-nm SOI CMOS
Type	Doubler + Amplifier	Doubler + Amplifier	Doubler + Amplifier	Doubler	Doubler	Doubler
Output Frequency (GHz)	206	245	152	204	228	150
BW_{3dB} (GHz)	170-218 ‡	220-260	138-170	165-230	200-245	135-160
Peak Gain (dB)	-2.0 §	10.9	4.9	-8.6	-15	-3
P_{sat} (dBm)	5.8	5.5	5.6	-2.6	2	3.5
P_{DC} (mW)	53	240	36	39	35	25
Efficiency (%)	7.2	9.5	10.9	1.4	4.5	9.0
Area (mm^2)	0.013†, 0.074	0.253	0.485	0.090	0.246	0.441
3-dB Gain Input Range (dB)	13.0 §	6 *	9 *	¿7 *	¿6 *	11 *

* Estimated from plot.
† Area without pads.
‡ Lower end limited by G-band measurement, with 12 dBm input.
§ At 190 GHz.

despite being limited by equipment input power. The gain bandwidth with a 12 dBm input is 170-218 GHz. The peak output power is 5.8 dBm, an equivalent 1.2 V_{PP} on 50 Ω, at 206 GHz with 18.0 dBm of input power. The doubler delivers more than -3.3 dBm over 170-260 GHz.

Fig. 2.10 shows a trend of flatness in power consumption, indicating that the bias feedback is controlling bias current across a wide range of input powers, despite an offset from simulation. The target quiescent current was 18.8 mA while the measured current was 14.4 mA. The current discrepancy could be due to poor tolerance of the small, high sheet resistance polysilicon resistors in the design, in addition to some V_{BE} variation. With peak output power at 206 GHz the collector efficiency is 7.2%, while DC consumption is 53 mW. As shown by Table 6.1, the bias adaptation in this work enables higher output power over a wide input power range without significant sacrifice of other performance attributes.

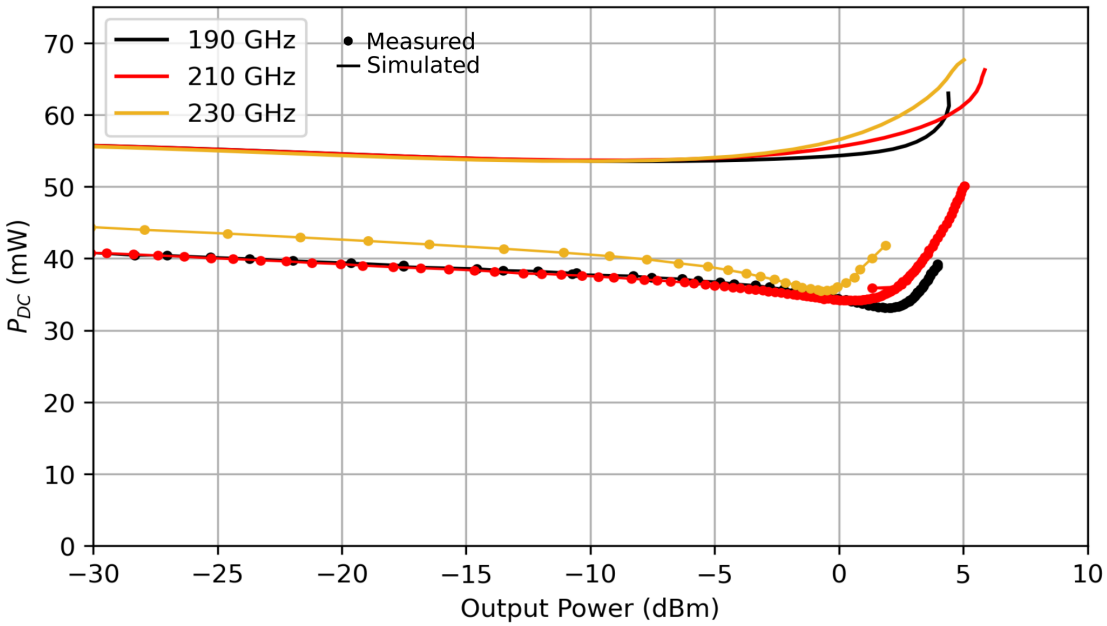


Figure 2.10: Measured DC supply power consumption across output power

2.5 Conclusion

A G-band frequency doubler in 90-nm SiGe BiCMOS technology with a novel resistive feedback adaptation is presented. With a peak gain of -2.0 dB measured at 190 GHz and

a 13-dB input power range defined by the 3-dB gain variation, this doubler demonstrates the benefit of the adaptive biasing with no penalty in power consumption, area, or output power. The doubler delivers more than -3.3 dBm over 170-260 GHz, with a peak of 5.8 dBm. These results strongly support the potential for implementing efficient LO multiplier chains in adaptive transceivers that can take advantage of variable LO power.

Chapter 3

Subharmonic Downconverter with Dynamic Conversion Gain and Power Consumption

3.1 Introduction

This chapter explores circuit techniques that reduce power consumption in the LO chain to improve energy efficiency in the array receiver, especially for adapting to dynamic channel environments where the received power P_{RX} varies by target or transmitter distance. To accommodate high dynamic range of the received radar signal, the conversion gain of the mixer is adjusted by saving LO power, eliminating additional variable-gain amplifiers in the signal path and decreasing system power consumption and circuit area. To demonstrate this adaptation, a subharmonic downconverter is realized in a 90-nm SiGe BiCMOS process for D-band (110-170 GHz), shown in Fig. 5.1a(b). Bias-feedback circuitry adapts the LO current to enable gain control in the mixer through the LO power. The design adjusts the fourth harmonic content in a push-pull frequency multi-

plier to achieve a high multiplication factor without sacrificing additional area or power for a cascaded multiplier chain. Additionally, the design inherently contains an LO power detector to monitor and support closed-loop gain control in a system. Section 2 presents the subharmonic downconverter circuit and the details of the fourth harmonic push-pull circuit are presented in Section 3. Section 4 presents measurements of the wideband downconverter.

Fig. 5.1a(a) illustrates a single receive channel of an array, which distributes LO power to each mixer with a variable-gain amplifier (VGA) in the intermediate frequency (IF). Millimeter-wave receiver circuitry typically consumes more power than circuits at lower frequencies. In addition to low noise amplifiers (LNA) having lower gain per stage above 100 GHz, the receiver needs large frequency multiplication factors with high local oscillator (LO) powers to drive the mixer, substantially contributing to power consumption. Conventional receiver arrays use a single saturating LO power to drive a mixer since the relationship between the input and output power of a conventional frequency multiplier circuit is nonlinear and difficult to control. This constant LO power assures relatively high DC power consumption.

3.2 Subharmonic-based Downconverter

The circuit of the downconverter is shown in Fig. 5.2 and is realized with a push-pull frequency multiplier generating a fourth harmonic to a single-balanced mixer. The RF input is split through a balun in the single balanced mixer.

The first proposed innovation is to replace the tail current source of the mixer with a push-pull frequency multiplier. With the active mixer directly attached the multiplier, the transistors form a cascode structure which increases conversion gain by suppressing the Miller effect and saves power by reusing the current for the multiplier in the mixer.

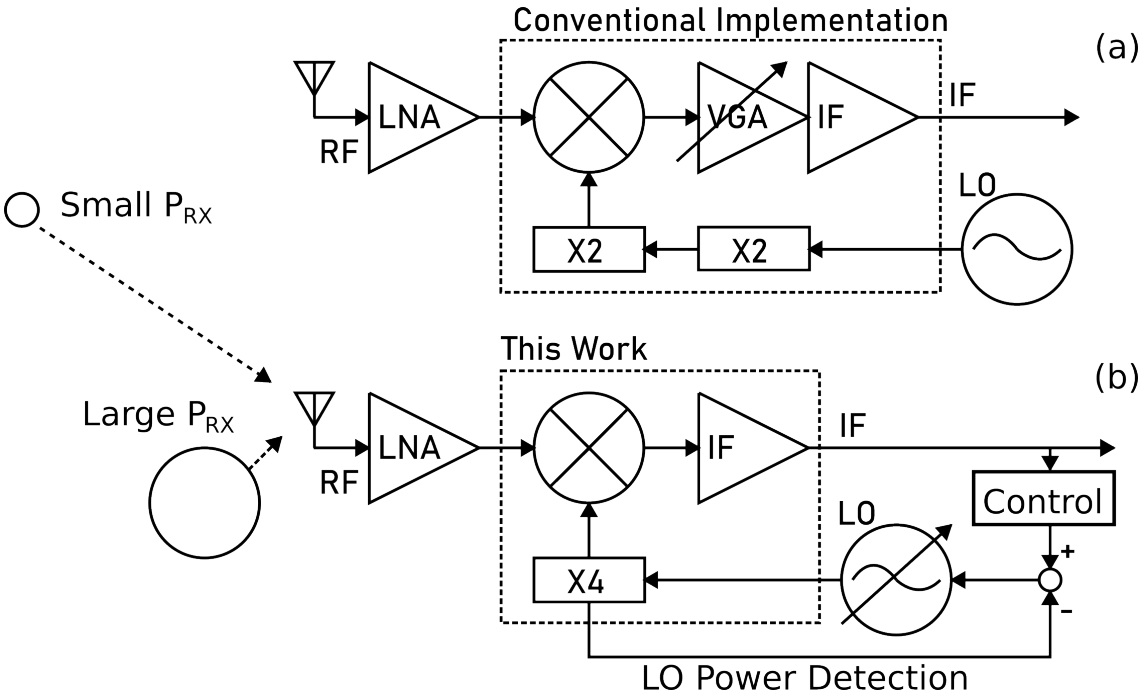


Figure 3.1: (a) Conventional and (b) proposed downconversion system element in a dynamic channel environment.

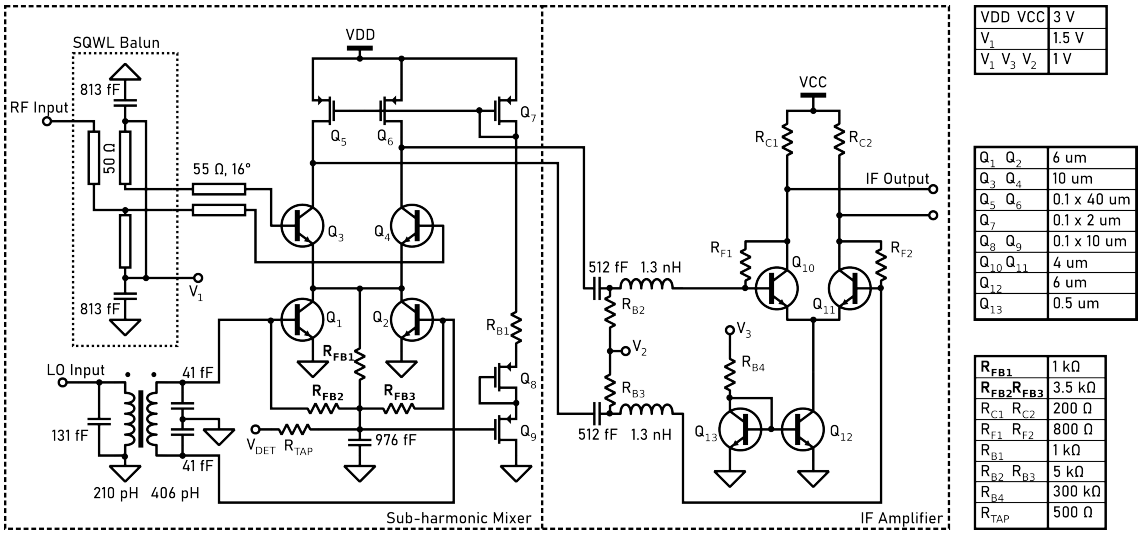


Figure 3.2: Schematic of proposed downconverter with bias feedback and dynamic conversion gain.

The load of the mixer is a pair of saturated PFETs that are biased through a common mode connection to the frequency multiplier, with their drain bias point set by device

parasitics.

The LO path includes a transformer balun that produces a differential LO to drive a pair of HBTs that generate the fourth harmonic. Since the LO is presented in the common mode in the mixer, it is suppressed by using differential mode in the RF path, through Q_3 and Q_4, and the IF path, though Q_{10} and Q_{11}. In the IF path, A differential wideband TIA with inductive peaking buffers and amplifies the converted signal from the mixer into difference voltage outputs.

The second proposed innovation is use of resistive feedback at the common node of the mixer to bias the multiplying transistors Q_1 and Q_2. The biasing supports frequency generation over a wide range of LO powers, enabling adjustable conversion gain at the mixer.

3.3 Dynamic Subharmonic Generation

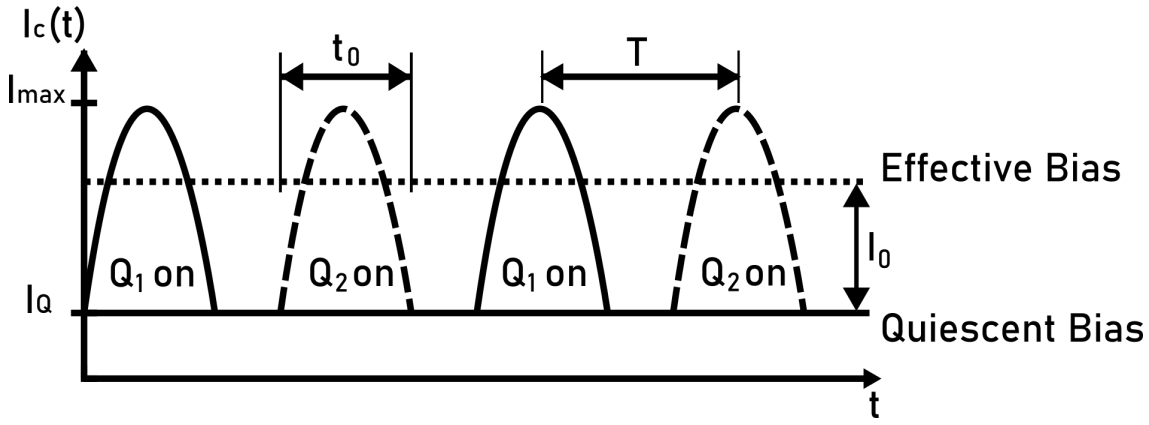


Figure 3.3: Instantaneous output current from a push pull frequency multiplier stage and its time-average impact on bias.

A typical push-pull frequency multiplier or sub-harmonic mixer uses a second harmonic [18]. The proposed subharmonic mixer utilizes the fourth harmonic from a push-pull frequency multiplier implemented with transistors Q_1 and Q_2, shown in Fig. 5.2.

The harmonic content of the combined collector currents I_C of Q_1 and Q_2 depend on the conduction cycle, which is controlled through their base voltage bias.

Modeling the collector current as a half-wave rectified sinusoidal pulse train, illustrated in Fig. 6.6, the Fourier series expansion presents the current harmonics as in Eq. 6.7 [11][12].

$$I_n = I_{max}\frac{4t_0}{\pi T}\begin{cases} 1 & \text{, if } n = 0 \\ 2\cdot\left|\frac{\cos\left(\frac{n\pi t_0}{T}\right)}{1-\left(\frac{n\pi t_0}{T}\right)^2}\right| & \text{, if } n \text{ even} \\ 0 & \text{, if } n \text{ odd} \end{cases} \tag{3.1}$$

A maximum fourth harmonic current of $0.27 \cdot I_{max}$ is obtained with conduction cycle $t_0/T = 0.17$. The ratio between the maximum harmonic current and generated DC current is $I_4/I_0 = 1.25$ for the maximum fourth harmonic. In this work, the conduction cycle is set by optimizing the combined resistance of $R_{FB1,2,3}$ for maximum conversion gain or fourth harmonic current. Despite the lower current in the fourth harmonic compared to the second, the ratio between the desired harmonic and generated DC current is fixed relative to the second or fourth harmonic. Thus, configuring a push-pull frequency multiplier for the fourth harmonic generation does not sacrifice DC power consumption.

In a typical multiplier, the bases of Q_1 and Q_2 are biased with a static voltage which is tuned for a particular LO input power [11]. This method, however, does not provide the best bias across input powers. As shown by the DC current where $n = 0$ in Eq. (6.7), the average effective output current of Q_1 and Q_2 is $I_C = I_Q + I_0$, where I_Q is the quiescent bias current and I_0 is the additional current generated from the rectification of the input sinusoid. The additional current causes the transconductance to change with output power, a source of nonlinear gain in the multiplier.

To counteract the current variation, large feedback resistances, R_{FB1}, R_{FB2}, and R_{FB3}, from the collectors of Q_1 and Q_2 set the base bias and to compensate for the

additional current created by the output waveform at DC. If we consider $V_{BE1,2} \approx V_{BE3,4}$, and $I_{C3,4} \approx I_{C1,2}$,

$$I_{C3,4} = \beta_{1,2} \frac{V_1 - 2V_{BE}}{R_{FB1} + R_{FB2}||R_{FB3}} \tag{3.2}$$

Thus, the feedback resistance reduces the influence from the additional rectified DC current. Although feedback compensates for the additional rectified current, the current change is not completely cancelled due to variations in the effective time-averaged $\beta_{1,2}$ over power variation. The feedback bias allows for a gradual change in gain over a wider range of LO input powers compared to the static bias approach, as shown in Fig. 6.8. The conversion gain remains higher over reduced LO power and improves the robustness of the circuit to LO power variation. With a -6 dB LO power backoff from peak conversion gain, the feedback biased circuit has 17 dB more gain than the static biased version. Additionally, the feedback network provides voltage V_{DET} corresponding to output current, enabling monitoring of conversion gain.

3.4 Measurement Results

Measurements were made on the subharmonic downconverter shown in Fig. 3.5 using a 3-V supply on VDD and VCC, with quiescent currents of 8.6 mA to the IF amplifier and 0.9 mA to the mixer. A VDI PM5B power meter was used as the power reference for calibrating the D-band extender as the RF input source, and output leveling was performed with an electronically controlled variable attenuator. DC blocks were used with an oscilloscope to measure the differential IF. The LO was directly provided by a signal generator.

The downconverter's conversion gain was measured across a range of LO powers across frequency with results in agreement with the simulation, shown in Fig. 3.6. The supplied

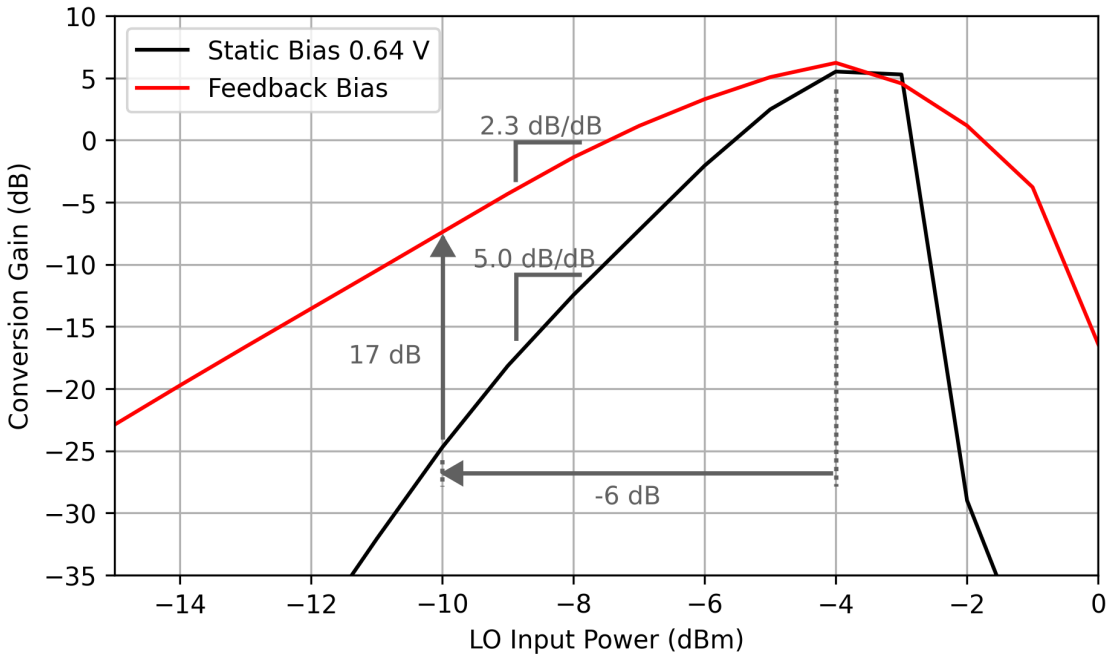


Figure 3.4: Simulated effect of bias feedback in the downconverter, compared to a typical static bias approach.

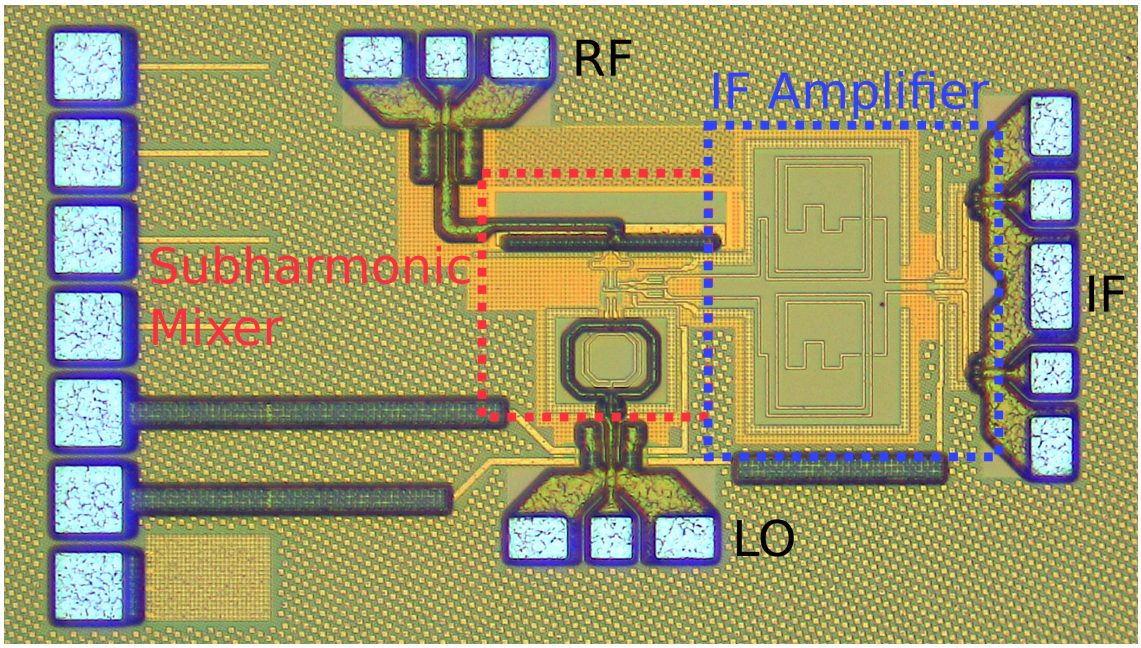


Figure 3.5: Micrograph of downconverter with dimensions of 1.18 mm x 0.68 mm and core area of 0.56 mm x 0.35 mm.

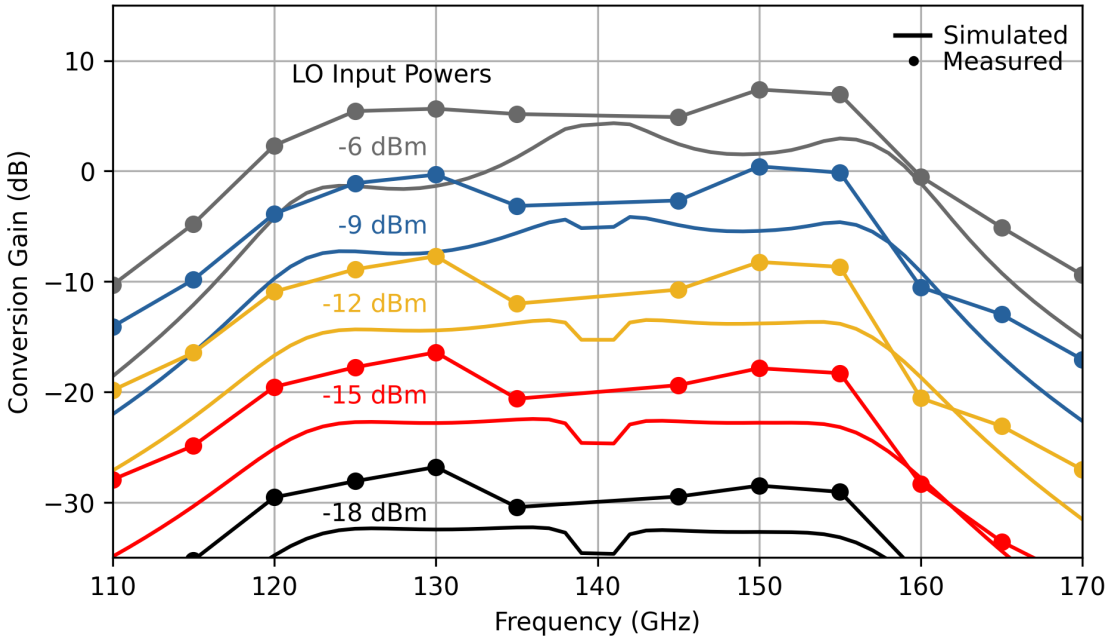
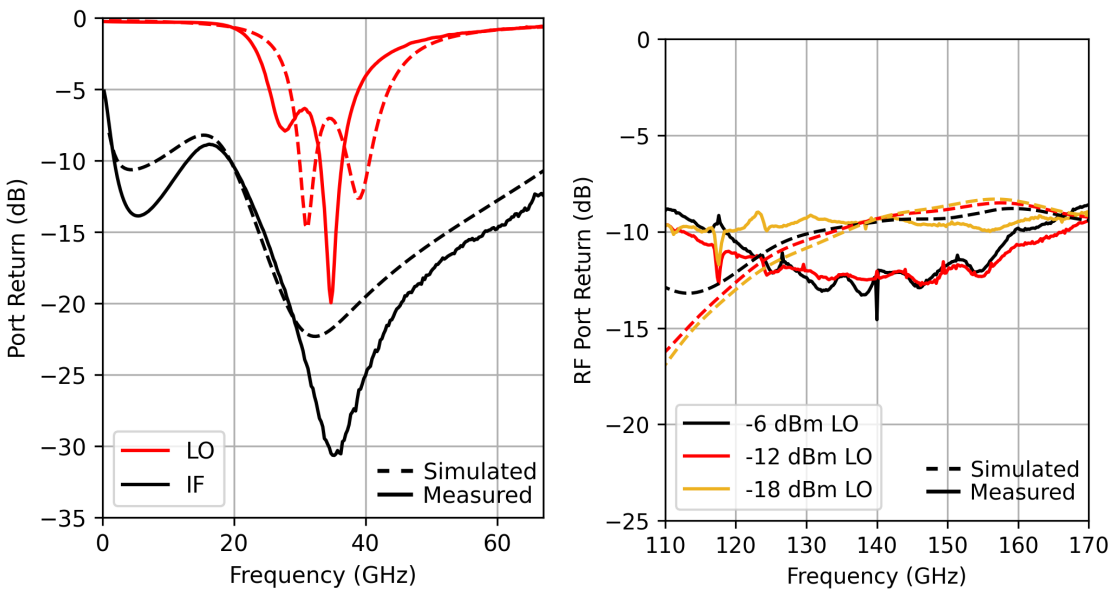


Figure 3.6: Conversion gain over RF frequency across LO powers on a 140 GHz LO, with -24 dBm of RF input power.

RF input power was -24 dBm and the LO was supplied at 35 GHz for an effective 140 GHz LO at the mixer. With -6 dBm of LO power, the maximum gain across the band was 7.4 dB at 150 GHz with a 3-dB bandwidth of 35 GHz, spanning 123 GHz to 158 GHz. The measured gain of the down-converter is higher than simulated due to a frequency shift in the return loss of the LO, shown in Fig. 3.7a. The shift lead to a better match at the LO frequency and more delivered LO power. Additionally the RF return loss, shown in Fig. 3.7b, was close to simulation with slightly better return loss.

Measurements at 155 GHz with a 140 GHz LO confirming the relationship between LO power and resulting conversion gain are shown in Fig. 6.9. The downconverter's conversion gain was controlled with LO power at 1.9 dB/dB, leading to the ability to reliably trade off between conversion gain and power consumption. A maximum gain of 7.5 dB was observed at 155 GHz with -5 dBm of input power, while consuming 55 mW of DC power. By backing off LO power from -5 dBm to -11 dBm to decrease gain from



(a) (b)

Figure 3.7: Port return S-parameters for (a) single-ended LO with differential IF and (b) RF port with varying LO powers.

the peak by 11.7 dB, DC power consumption was decreased by 19 mW, 35% less than consumption at peak gain.

The LO power detection voltage V_{DET} was measured to be close to simulation, shown in Fig. 3.9. The power detection is predictable and monotonic, making it suitable for use in system level control of LO power. With a 155 GHz RF and 140 GHz LO, the lowest demonstrated 1-dB input compression is -15 dBm, shown in Fig. 3.9. With less than -4 dBm LO power, the input compression remains fixed between -15 dBm and -10 dBm while the output compression changes with LO power.

3.5 Conclusion

A wideband fourth subharmonic D-band downconverter is presented with bias feedback to enable adaptation of performance and power consumption through LO power.

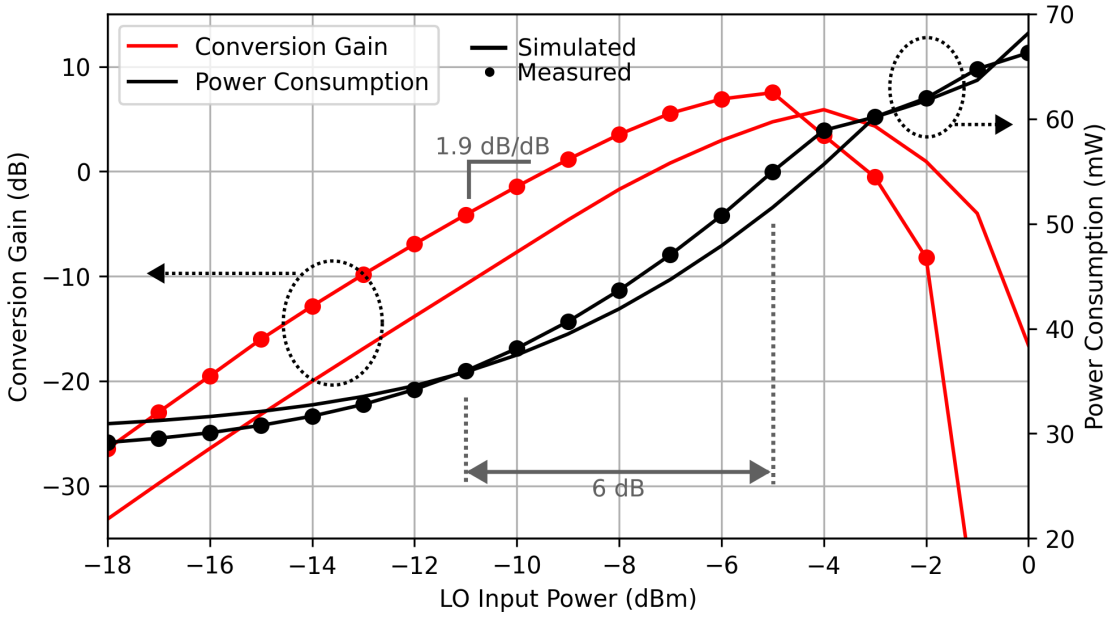


Figure 3.8: Conversion gain and DC power consumption at 155 GHz RF and 140 GHz LO, with -24 dBm of RF input power.

Table 3.1: Comparison with Downconverters Above 100 GHz

Reference	This Work	[18]	[19]	[20]
Technology	90-nm SiGe	90-nm SiGe	130-nm SiGe	130-nm SiGe
Subharmonic	4	2	2	1
f_C (GHz)	140	136	121	140
BW_{3dB} (GHz)	35	38	>14	35
Gain (dB)	7.5	5.1	4	32
P_{i1dB} (dBm)	-15	-7	-	-41
Noise Figure (dB)	21.7*	-	23*	9.5
LO (dBm)	-5	2	7	-2
P_{DC} (mW)	55	51	89	65
Area (mm^2)	0.196†	0.450†	-	0.191†

* Simulated † Area without pads.

The circuit exploits the fourth harmonic content of a push-pull frequency multiplier to achieve a high multiplication factor without sacrificing additional area, power consumption, or LO power requirement for a cascaded multiplier chain, exemplified in Table 6.1. The adaptation makes this circuit suitable for applications of joint radar and radio

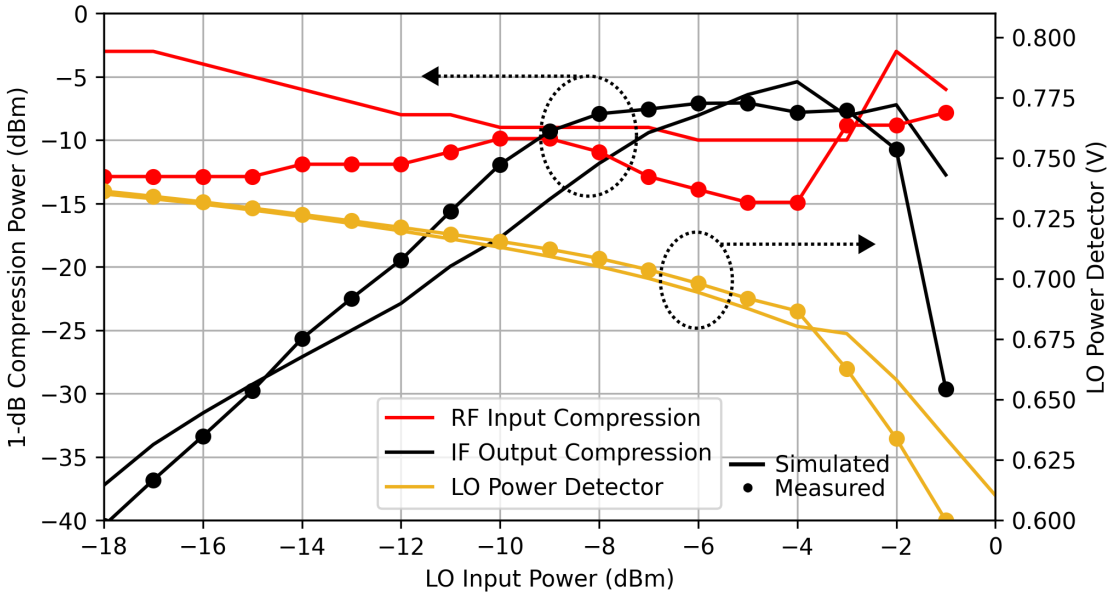


Figure 3.9: 1-dB input and output power compression at 155 GHz RF and 140 GHz LO with LO power detection voltage (V_{DET}).

systems in dynamic environments.

Chapter 4

Millimeter-Wave Low-noise Amplifier in 35-nm InP HEMT for Heterogenous Integration

4.1 Introduction

It is attractive to combine CMOS with external low noise amplifiers in technologies such as InP HEMT for better receiver sensitivity and reduced demand for transmit power [21]. Reducing power consumed by an LNA is a way to significantly reduce power consumption in addition to optimizing the LO for lower power, since those are typically the highest consumers of power in a receiver system. In this chapter, a 185-GHz InP HEMT low-noise amplifier (LNA) is presented with compact form suitable for heterogenous integration with CMOS in a multi-channel system as illustrated in Fig. 5.1a. The LNA design procedure uses noise measure based on inductive degeneration for simultaneous noise and gain matching. With dimensions of 1285 µm x 600 µm, it can be tiled along its width to fit under the free-space half-wavelength at 210 GHz, which is 714

µm. The following sections present the design procedure based on noise measure, noise measurements, and the first P1dB measurements across frequency for this technology.

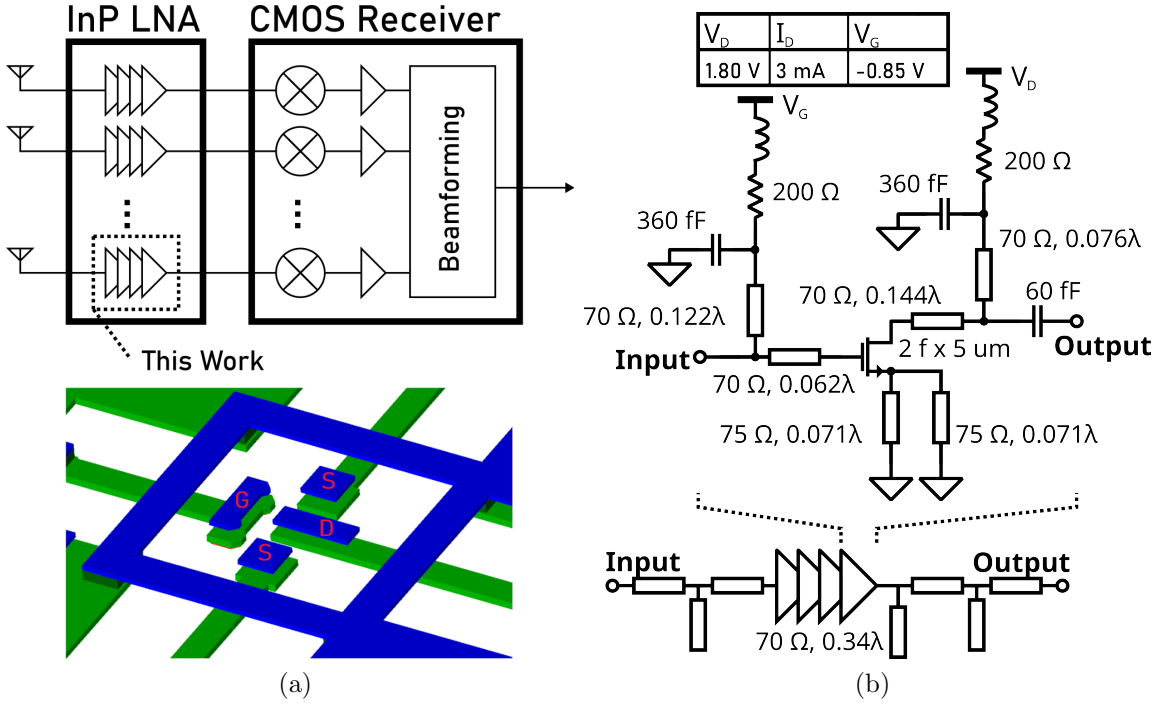


Figure 4.1: (a) Diagram of heterogenous integration between an InP LNA and a CMOS receiver in a multi-channel system and transistor layout with (b) schematic of a single stage of this work's 4-stage LNA. All stages in the amplifier are identical.

4.2 Design

The LNA, shown in Fig. 4.2, was designed and fabricated based on a Northrop Grumman 35-nm InP HEMT process. The process has a single metal layer for interconnect with a top air-bridge metal. Resistors are available as thin films at 20 Ω/□ and 100 Ω/□ with 600 pF/mm^2 capacitors. At 300 mA/mm, the HEMT has a maximum 866 GHz unity power gain frequency (f_{max}) under a nominal drain voltage of 1.2 V. With a substrate thickness of 51 µm, coplanar layout was chosen over the microstrip alternative to achieve practical line impedance and compatibility with packaging [22].

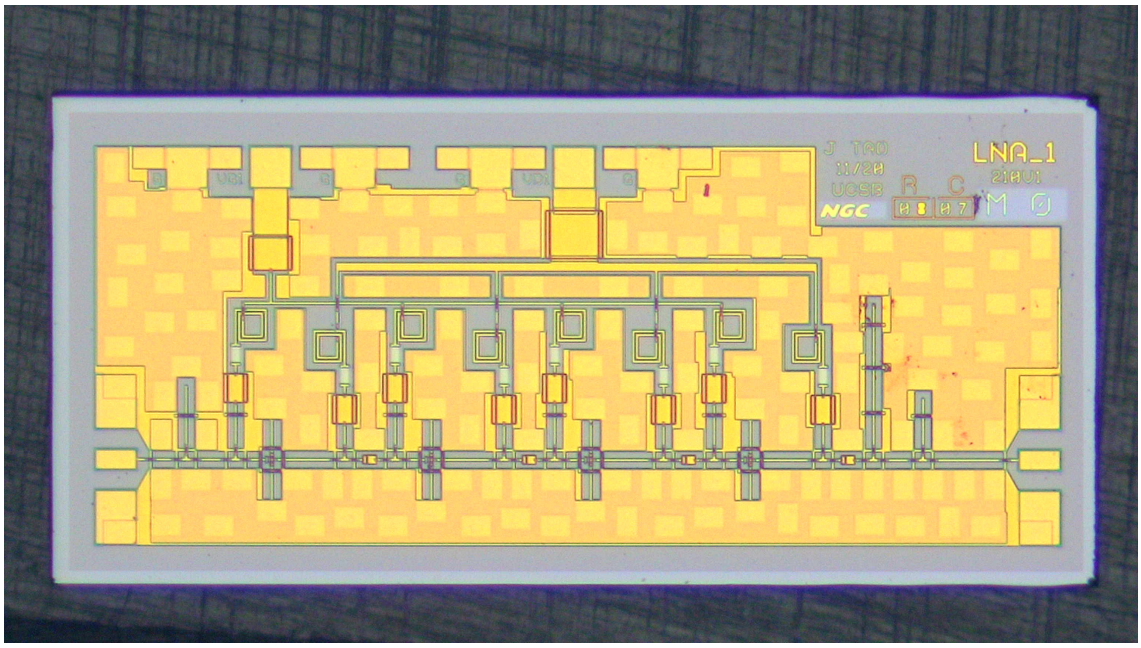


Figure 4.2: Micrograph of the 4-stage low noise amplifier. The total die dimensions are 1285 µm x 600 µm with a total area of 0.77 mm^2.

4.2.1 Noise Measure Design Procedure

A minimum noise measure technique was used to optimize and perform simultaneous power and noise matching. Noise measure M is defined by

$$M = \frac{F-1}{1-1/G_A} \tag{4.1}$$

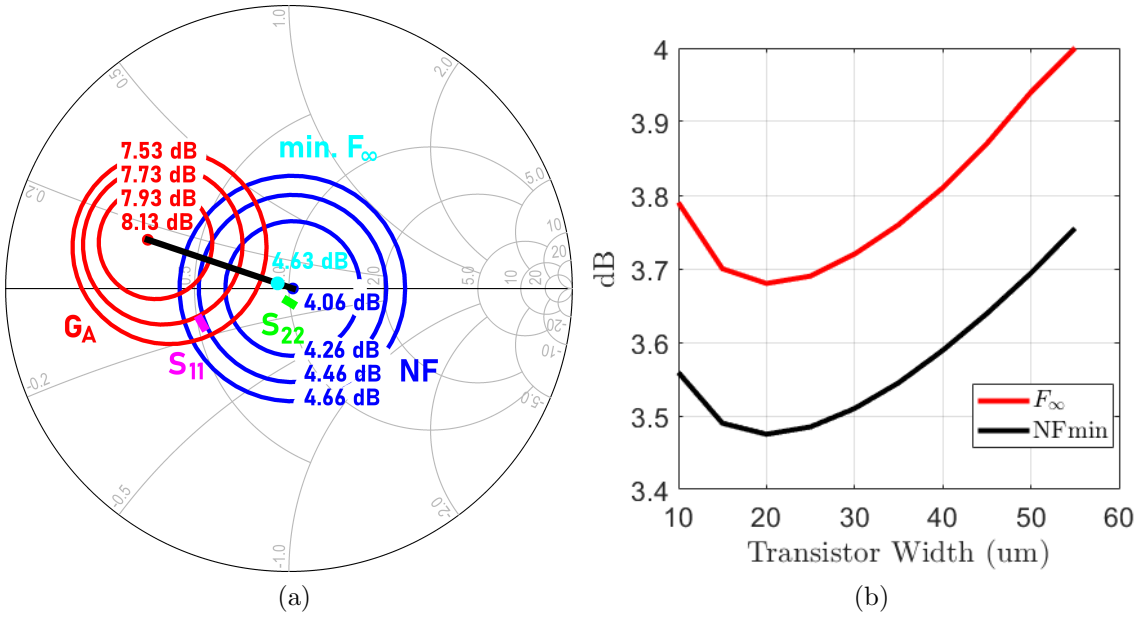
where G_A is the available gain and F is the noise factor of the amplifier [23]. The upper bound for an infinite cascade of LNA stages can be represented with noise measure as

$$F_\infty = F + \sum_{k>=1}^{\infty} \frac{(F-1)}{G_A^k} = \frac{F-1}{1-1/G_A} + 1 = M + 1. \tag{4.2}$$

F_∞ is intrinsic to the underlying transistor since any passive, lossless, and reciprocal additions to implement the transistor into a circuit do not affect this metric [23]. It is more relevant in most applications since a low-noise stage with low gain is unable to

buffer the noise contributions of subsequent stages.

The optimum source impedance to achieve minimum F_∞ was approximately determined in Keysight ADS by finding the impedance between the G_A and NF circle centers that yield the minimum F_∞ as illustrated in Fig. 4.3a using an algorithm from [24]. The external source is matched to present the impedance of minimum F_∞ to the input of the transistor, while the output of the transistor is power matched to the external impedance. In implementation, the input match for best noise measure is different from a conjugate match, so techniques such as inductive degeneration in this work are used to reduce the gain effects of this difference to achieve the ability to cascade stages while maintaining noise measure performance.



(a) (b)

Figure 4.3: (a) Minimum noise measure impedance match with a single LNA stage in simulation at 210 GHz, and (b) Minimum F_∞ over 2-finger transistor widths at 300 mA/mm.

4.2.2 Circuit Implementation

In this design, the minimum F_∞ of the chosen 2-finger 10 µm transistor at 210 GHz is 3.8 dB. Although the scalable fixed-bias transistor models showed that other sizes had slightly better F_∞, as shown in Fig. 4.3b, lossy matching applied to the transistor outweighed the small variations in F_∞ by width. Transistor width was chosen for the matching topology with inductive degeneration, shown in Fig. 5.2. Fig. 4.3a shows that the implementation of the transistor into a single stage of the LNA degrades the F_∞ from 3.8 dB to 4.6 dB, and then to 5.2 dB with cascade and addition of matched pads in layout.

Table 4.1: Comparison of Recently Published LNA Above 100 GHz

Ref.	Technology	Freq. (GHz)	Gain (dB)	Stages	NF (dB)	Pi1dB (dBm)	P_{DC} (mW)	F_∞ * (dB)	$1/MP_{DC,Stage}$ † (mW^{-1})
[24]	250 nm InP HBT	196-216	13	4	6.8-7.6	-19.1	19.2	7.4	0.047
[24]	250 nm InP HBT	196-216	14.5	2	6.7-8.1	-17.5	9.2	7.5	0.047
[25]	50 nm InP mHEMT	220-325	31	8	5.6-7	-29.3	56	6.3	0.044
[26]	50 nm InP mHEMT	178-185	24.5	5	3.5-4.5	-	24	4.0	0.137
[27]	25 nm InP HEMT	215-225	36	-	3.9-4.5	-	-	4.2	-
[28]	75 nm InP HEMT	180-270	12.5	2	5.3-7	-	18	6.3	0.034
[29]	35 nm InP HEMT	158-220	22	4	4.8-5.2	-	-	5.0	-
[29]	35 nm InP HEMT	164-220	25	3	4.8-5.6	-	-	5.2	-
This work	35 nm InP HEMT	175-200	19.6	4	9.8-11.4	-23.7	22	10.6	0.017

* Calculated with insertion gain $\|S_{21}\|^2$ and average of the reported range of noise figures.
† Calculated with power consumption per stage, $P_{DC,Stage}$.

4.3 Measurements and Results

Measurements for gain, power, and noise were made on the LNA with transistor current density at 300 mA/mm, set with a gate voltage of -0.85 V. The transistor in each stage,

with periphery of 10 µm split across two gate fingers, draws 3 mA. The drain bias is set through a ballast resistor that drops the 1.8 V supply to 1.2 V at the transistor. The LNA consumes a total of 12 mA at 1.8 V, resulting in 21.6 mW of DC power consumption.

4.3.1 S-Parameter Measurement

S-parameters were measured using a Keysight N5277A network analyzer with 140-220 GHz OML frequency extender modules with WR4 GGB probes. The measured S-parameters are shown in Fig. 4.4, and the peak small signal gain was 19.6 dB at 194 GHz. Between the simulated and measured S-parameters, a reduction in gain and a downward frequency shift of about 15% from the design was observed. The simulation can be adjusted to approximate measurement by reducing g_m by 5%, increasing R_i by 30 times, reducing R_{DS} by 50%, reducing R_G, R_D, and R_S by 30%, raising C_{gd} by 100%, and adding 8 pH in series to both the gate and the drain of the transistor. The extra inductance may be caused by the removal of the ground plane immediately next to the transistor to fit the CPW degeneration lines. The impact of this simulation adjustment is shown in Fig. 4.5. The sample yield is 8.3%, indicating high process variation.

4.3.2 Power Measurement

Power measurements were made with a Keysight E8267D signal generator and a VDI WR4.3SGX-M extender, and then measuring the output with a VDI PM5B power meter. From 170 GHz to 210 GHz, the measured gain, shown in Fig. 4.6a, was in agreement with the measured S-parameters. The 1-dB input power compression points are plotted in Fig. 4.6b. The lowest compression point of -23.7 dBm was measured at 190 GHz with the highest P_{1dB} was -12 dBm at 210 GHz. To our knowledge, this is the first P1dB measurement over frequency for this 35-nm InP HEMT technology.

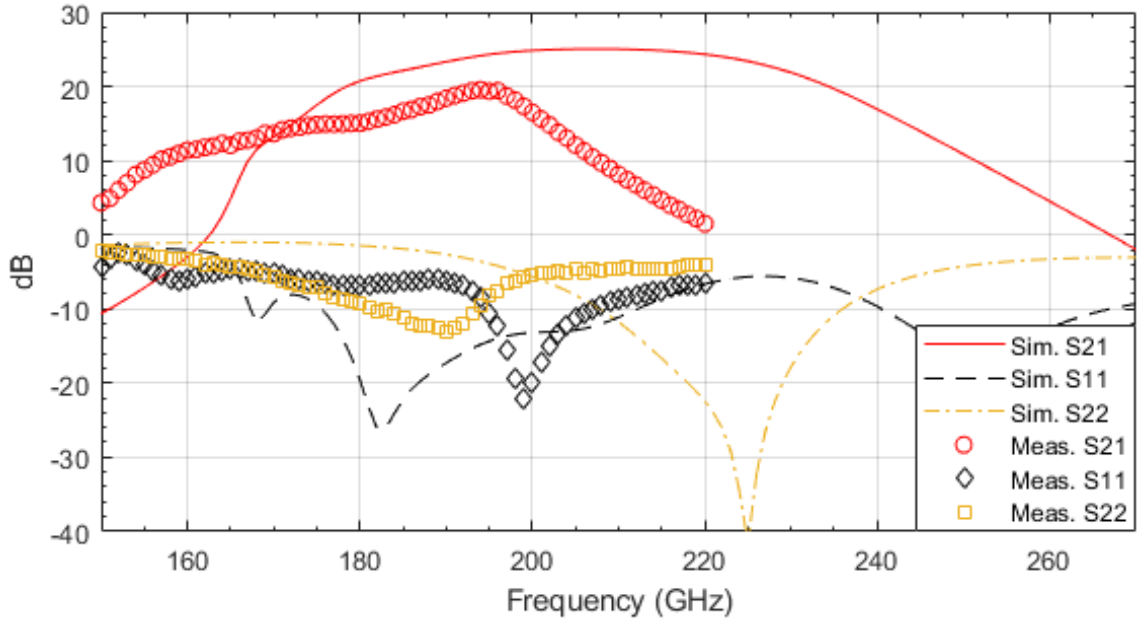


Figure 4.4: Measured and simulated S-parameters of the LNA

4.3.3 Noise Measurement

Noise figure was measured using a VDI WR5.1NS hot-cold noise source and a down-conversion chain, as shown in Fig. 4.7. Effects of measured probe loss were removed by calculation, since the calibrated reference planes are set to the output of the noise source and input to the down-conversion, using noise source manufacturer ENR data. The noise source has excess noise ratios (ENR) ranging from 6.0 dB to 10.9 dB.

The results of the noise measurement are shown in Fig. 4.5 with the gain and noise from a simulation with the adjusted transistor parameters. The gain derived from the Y-factor noise measurement is close to that of the S-parameter measurements and adjusted simulation. Over 175 GHz to 200 GHz, the amplifier demonstrates NF ranging from 9.8 dB to 11.4 dB, with the point of lowest noise occurring at 185 GHz. In spite of the adjustment device model to correct the S-parameters, our noise measurements remained significantly higher than the NF predicted from the device model.

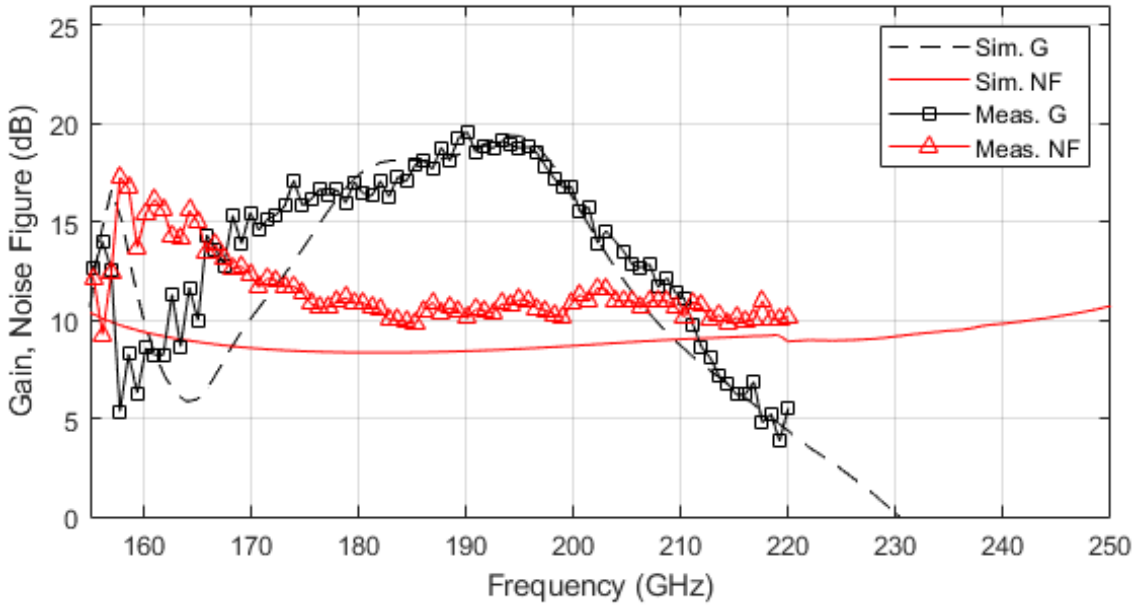
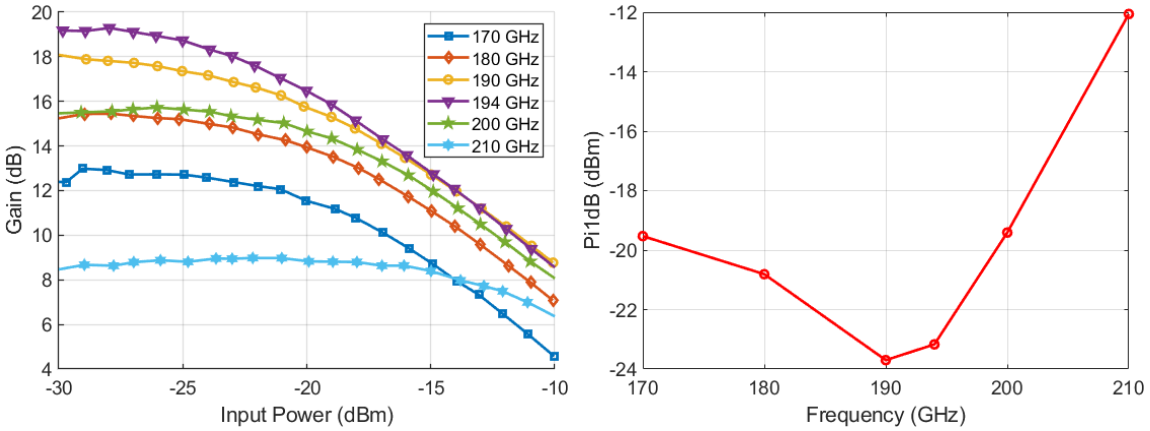


Figure 4.5: Measured amplifier noise with adjusted simulation.



(a) (b)

Figure 4.6: (a) Measured gain across input power with frequency and (b) measured 1-dB input power compression point over frequency

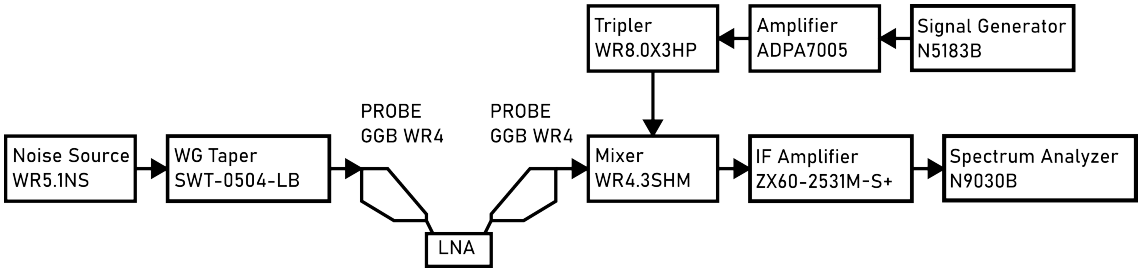


Figure 4.7: Noise measurement setup

Table 6.1 compares the current work against the state of the art. F_∞ and $1/MP_{DC,stage}$ are computed using the average noise figure. Performance is quantified with a novel $1/MP_{DC,stage}$ as a figure of merit. The FOM represents the noise performance capability of the underlying technology through M and the power consumed to achieve that noise performance through $P_{DC,stage}$. This metric is invariant with number of stages and is supported by the design theory with noise measure M, used by the design procedure in this work.

4.4 Conclusion

A 4-stage 185 GHz InP HEMT LNA for heterogenous integration was designed and fabricated, demonstrating used of noise measure in design. In the first P1dB measurements across frequency for this technology, the amplifier exhibits a P1dB of -23.7 dBm at 190 GHz. Over 175 GHz to 200 GHz, the amplifier demonstrated noise figures ranging from 9.8 dB to 11.4 dB. The amplifier shows a peak 19.6 dB of gain at 194 GHz. The circuit consumes 22 mW of DC power. With dimensions of 1285 µm x 600 µm, it is dimensionally suitable for multi-channel arrays. While an LNA fabricated with alternate technologies may have a lower power consumption and noise performance, the lower yield is not necessarily an advantage to a large scale array system. Additionally, the interconnects to implement heterogenous integration have been shown to have a significant

impact on system performance that is difficult to control [30].

Chapter 5

Ultra-compact Low-noise Amplifier in 90-nm SiGe for Monolithic Array Integration

5.1 Introduction

In this chapter, a D-Band SiGe HBT LNA fabricated in a 90-nm SiGe BiCMOS technology for array integration is presented. The receiver blocks that dominate power consumption in higher frequency bands are typically low-noise amplifiers (LNA) and the LO multiplier chain. This is especially important when the power consumption of transmit and receive arrays increases at higher frequencies and would be prohibitive in applications such as handsets where the power budget is limited [1]. Due to the array element spacing demanded at 170 GHz, e.g. 0.8 mm, this LNA has a compact form suitable for integration in digital beamforming front-ends as illustrated in Fig. 5.1a and Fig. 5.1b. Because of low conversion gain of passive or dynamically controlled mixers, the noise figure seen at the input of the mixer can be greater than 15 dB. The design

focuses on maximizing gain per area and noise figure through noise measure matching. By reducing the number of stages, both the size and overall power consumption is also reduced.

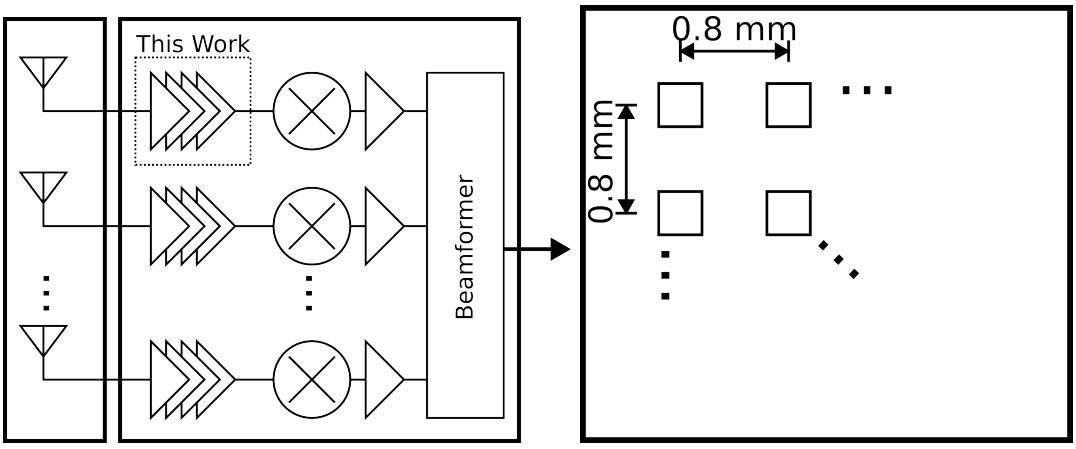


Figure 5.1: (a) Diagram of monolithic integration between the LNA of this work and a SiGe BiCMOS receiver system with external antenna packaging, and (b) receiver system in 2-dimensional tiling with half-wavelength spacing requirements.

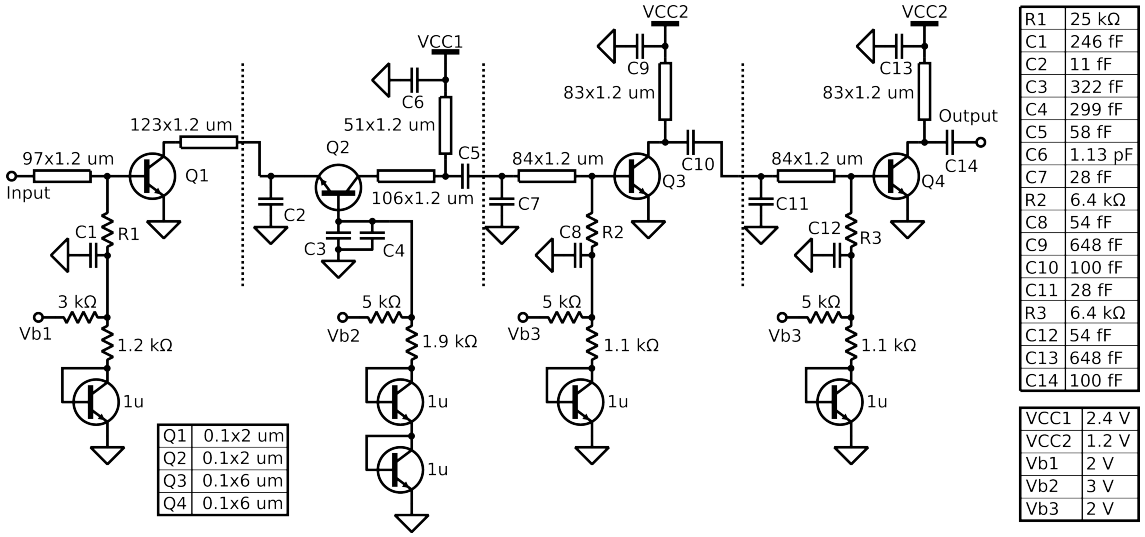


Figure 5.2: Schematic of proposed low-noise amplifier with biasing circuity.

5.2 Design

The circuit is illustrated in Fig 5.2 and indicates a 4-stage LNA composed of a common-emitter first stage, a common-base second stage, followed by two identical common-emitter stages. All stages are designed with 50 Ω input and output impedances. The first stage is used to provide noise performance and wide-band input matching, while the other stages are used to shape the gain and increase output power with their contributions to gain shown in Fig. 5.4.

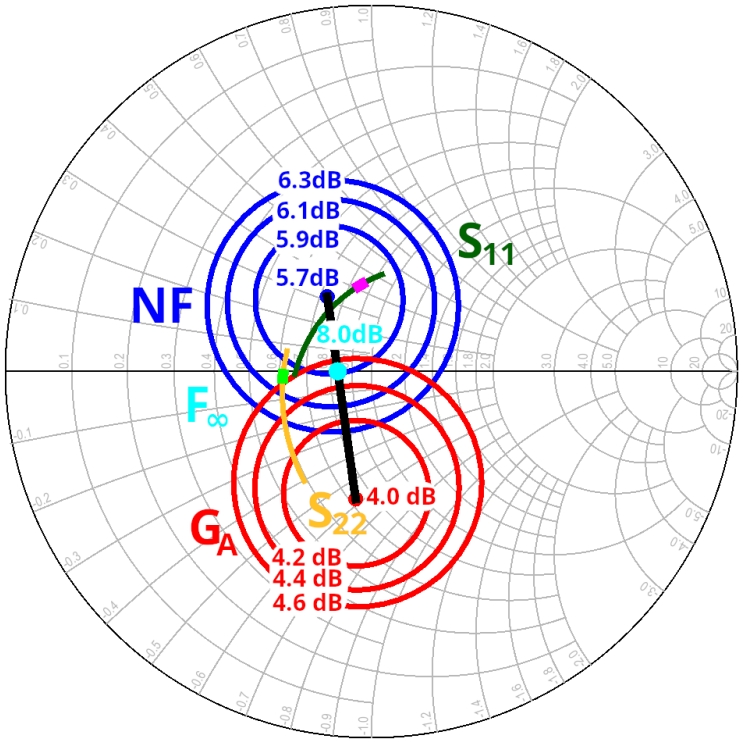


Figure 5.3: Minimum noise measure impedance match with first LNA stage at 158 GHz. Input and output impedances are shown from 110-170 GHz with 158 GHz marked.

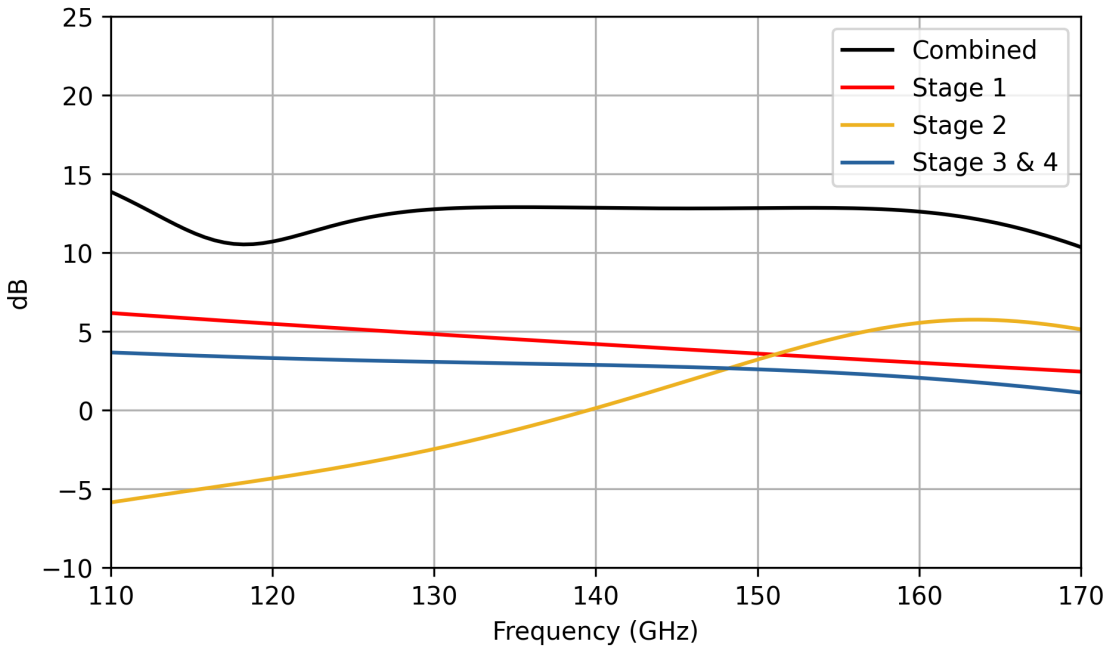


Figure 5.4: Simulated gain per stage contributions with staggered tuning and combined gain of full 4-stage LNA.

5.2.1 First Stage Design

The first stage uses a transistor with an emitter length of 2 um in CBEBC configuration. The length of the transistor emitter was chosen to facilitate high-bandwidth input matching with the intention of providing a predictable interface with an antenna for integration. The transistor's base impedance is 42.8 - j59.6 Ω at 140 GHz, which is easily matched to 50 Ω with a short series line for low loss and matching bandwidth instead of a large transformer.

The chosen bias provides the highest available gain in anticipation of loss from the implementation of the matching network. The bias also allows the use of fewer stages to achieve sufficient gain to suppress the noise contributions from the following integrated subsystems, such as a mixer, minimizing area consumption. To evaluate this trade-off, the cascaded noise figure is used, since it is related to the noise measure, M, which is

invariant to transistor embedding [23], related in the following equation.

$$F_\infty = F + \sum_{k\geq 1}^{\infty} \frac{(F-1)}{G_A^k} = \frac{F-1}{1-1/G_A} + 1 = M + 1. \tag{5.1}$$

The minimum cascaded noise figure ($F_{\infty,min}$) at the chosen collector current at 4.0 mA is 7.1 dB with 5.7 dB of available gain, while the minimum noise measure at the optimum bias of 0.9 mA is 5.7 dB with 4.4 dB of gain at 170 GHz. The chosen bias yields an implemented stage gain at 170 GHz of 2.4 dB, which gives a reasonable margin for the fabrication and simulation deviation. The stage's cascaded noise figure is 9.2 dB at 170 GHz.

The first stage implements staggered tuning where the input match is tuned for a slightly lower frequency than the output, which is intended to work with the second stage, which supplements gain at high frequencies. This match is illustrated in Fig. 5.3, along with the minimum noise measure impedance match. Since the minimum noise figure and the available gain decrease at high frequencies, the optimum noise measure impedance was matched at a higher frequency to extract the transistor noise measure performance.

5.2.2 Second Stage Design

The second stage is a 2-um emitter HBT in common-base configuration (CBEBC) for increased gain at the high-frequency edge of the band to achieve gain flatness in the D-band. A matched common-base configuration was chosen over a direct connection to the first stage as a cascode, since it provides higher gain for the power consumed, avoiding the need to add additional stages to meet the gain requirement of the larger system. Bias current supplied through the common-base stage is reused by the first common-emitter stage. This DC connection obviates need for a blocking capacitor, which reduces area

consumption. This transistor has the same collector current as the first stage.

5.2.3 Third and Fourth Stage Design

The identical third and fourth stages use 6 um emitter CBEBC transistors in common-emitter configuration to increase the maximum output power and to increase gain with the remaining available area. The transistor size was chosen to obtain an output 1-dB compression point of about 0 dBm, and each has 9.4 mA of collector current.

5.2.4 Circuit Implementation

Due to the need to minimize the area of the LNA, techniques to improve performance with large passives were avoided. For example, inductive degeneration can simultaneously match both noise and gain, but it was not used due to the high loss and area trade-off. Although techniques such as coupled lines yield high bandwidth with similar performance to transmission lines [31], simple transmission line matching in an LNA with staggered tuning, transistor sizing, and bias tuning can achieve similar results with shorter and thinner lines to minimize area.

For the presented LNA test structure, a 50 Ω transmission line of 450 µm length connects the LNA to the output pad, as shown in Fig. 5.5. Due to the small size of the LNA, the line gives physical clearance for probing. In D-band, it has a measured insertion loss ranging from 0.5 dB to 1.7 dB, while return loss remains under 14.6 dB.

5.3 Measurement Results

Measurements were made on the LNA, with voltage biases shown in Fig. 5.2. The LNA itself consumed 35.7 mW, while the biasing circuits consumed 1.9 mW, leading

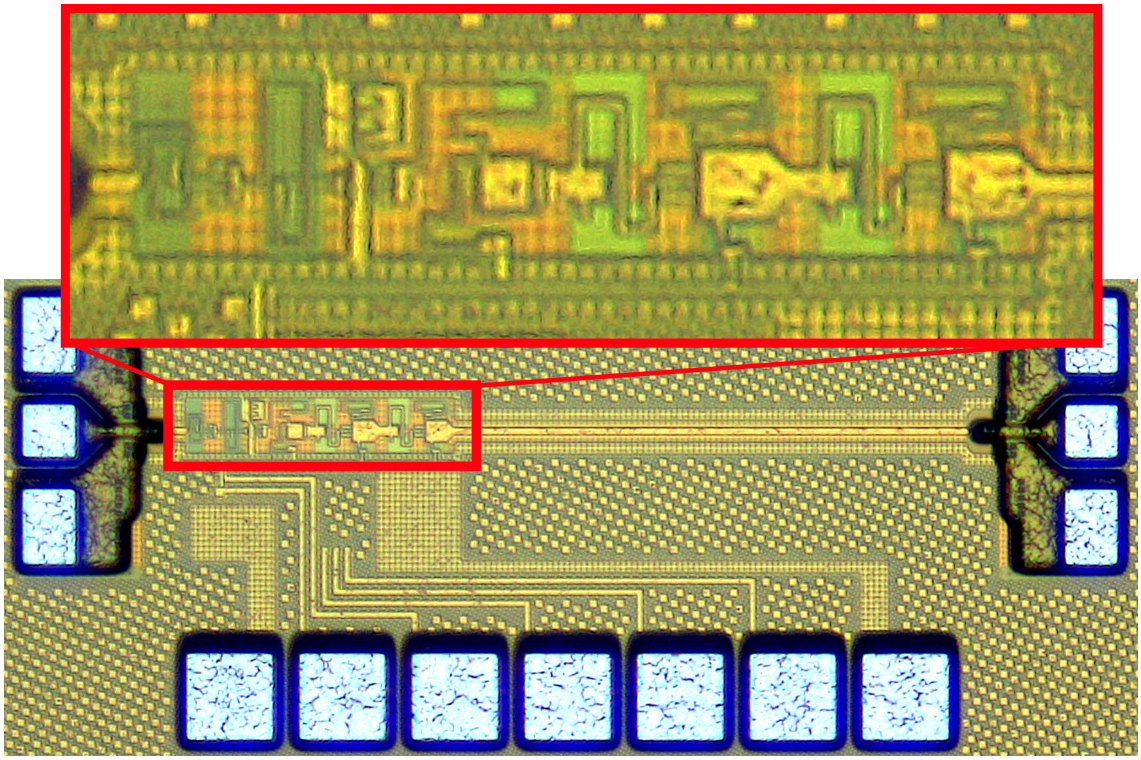


Figure 5.5: Micrograph of LNA test structure with output extension and chip dimensions of 395 um x 975 um and magnification of integrable LNA core with size of 60 um x 245 um.

to 37.6 mW of total power consumption. Because the LNA was intended to integrated into a larger system with voltage supply, the biases were set by voltage through biasing circuits. The simulated total collector current is 22.8 mA, while the measured collector current is 25.5 mA. For all measurements and simulations, the output extension line was not de-embedded from the results.

5.3.1 S-Parameter Measurements

S-parameters were measured from 110 GHz to 170 GHz on a Keysight N5277A network analyzer with D-band (110-170 GHz) VDI frequency extenders and WR-06 probes. The LNA achieves more than 12 dB of gain across D-band, with a maximum of 19.7 dB at 118 GHz. The gain remains in a 3-dB range from 123 to 164 GHz. In addition to

higher gain, there is also a downward frequency shift of approximately 15%.

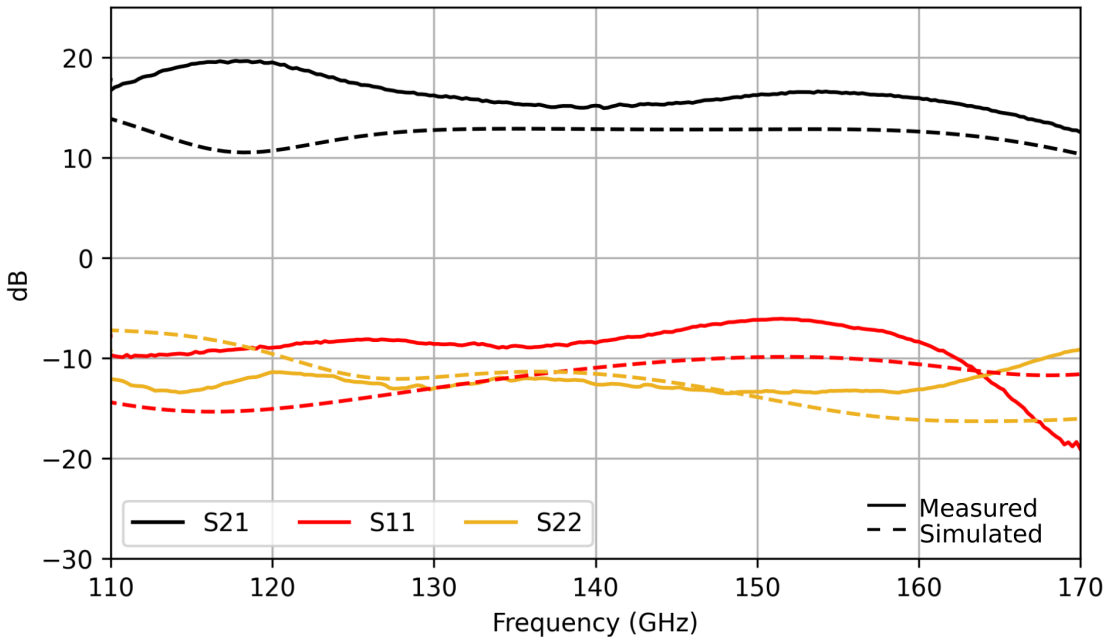


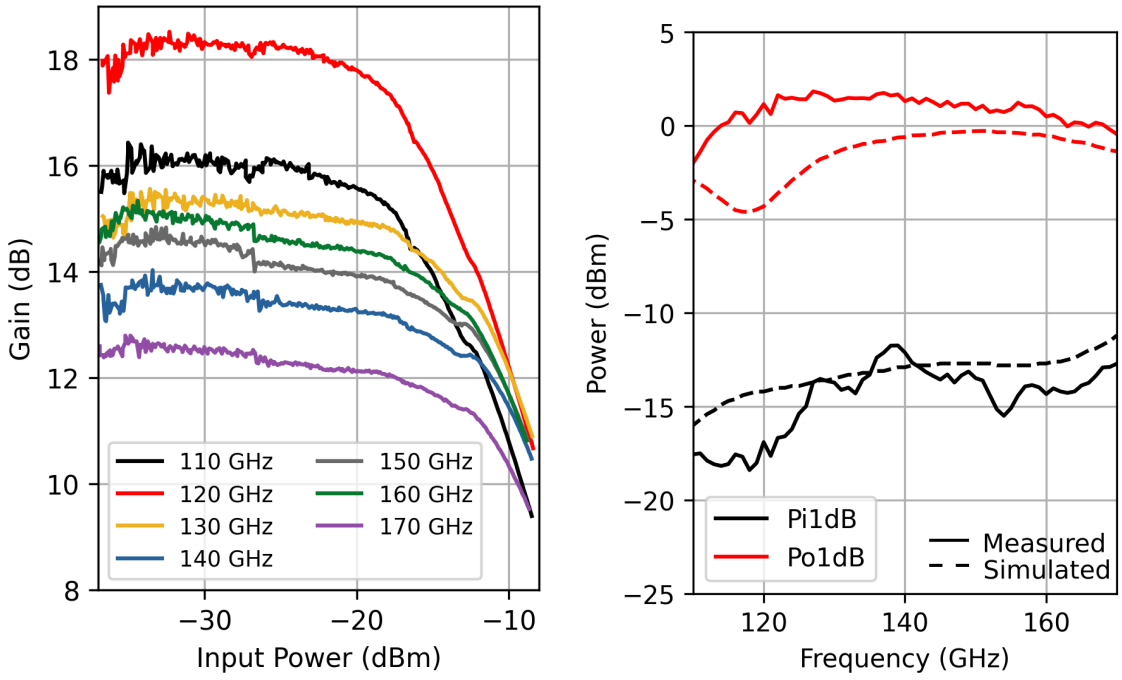
Figure 5.6: S-parameter Measurement.

5.3.2 Power Measurement

Power measurements in D-band were made on the LNA by down-converting continuous wave output from the LNA to a VDI WR6.5SAX-M spectrum analyzer extender and detecting narrow-band power with a Keysight N9030B spectrum analyzer. The input to the LNA was generated with the network analyzer as the signal source, up-converted with the D-Band frequency extenders, and then attenuated with a Mi-Wave 511D programmable rotary vane attenuator followed by an isolator. For sweeping across input powers, the programmable attenuator was used to control power due to extreme sensitivity to input power changes on the extenders. The generated input power level over frequency was calibrated using a VDI PM5B power meter as the reference. Then, the down-conversion gain to the spectrum analyzer was calibrated using the known power

from the calibrated input chain.

The power measurements across frequency shown in Fig. 5.7a are in agreement with the gain from S-parameter measurement for small input power levels. The measurement is presented as 1-dB compression points of the LNA in Fig. 5.7b, which are close to simulation. The lower input compression and higher output compression than simulation are consistent with the higher observed gain. The 1-dB input compression points range from -18.4 dBm to -11.7 dBm.



(a) (b)

Figure 5.7: (a) Measured gain across input power with frequencies, and (b) Measured LNA output and input 1-dB compression powers.

5.3.3 Noise Measurement

Noise measurements in D-band were made using an Eravant STZ-06-IT2 WR-06 hot-cold noise source, with a nominal ENR of 15 dB, through the Y-factor technique. The

Table 5.1: Comparison with D-band Silicon LNAs

Reference	**This Work**	[31]	[32]	[33]	[34]	[35]
Technology	90-nm SiGe	90-nm SiGe	90-nm SiGe	55-nm SiGe	130-nm SiGe	130-nm SiGe
Freq. (GHz)	144	139.8	140	140	140	140
BW_{3dB} (GHz)	41	37.6	28	70	52	23.2
Max. Gain (dB)	19.7	26.5	30	23	32.6	32.8
P_{i1dB} (dBm)	-13.4	-31	-	-21.3	-37.6	-28.6
NF (dB)	7.0-9.3	7.2	6.2	5-6.5	4.8-6.1	7.8*
P_{DC} (mW)	37.6	20.6	45	60	28	39.6
Core Area (mm^2)	0.015	0.69 †	0.11	0.109	0.6	0.075†

* Simulated † Die Area

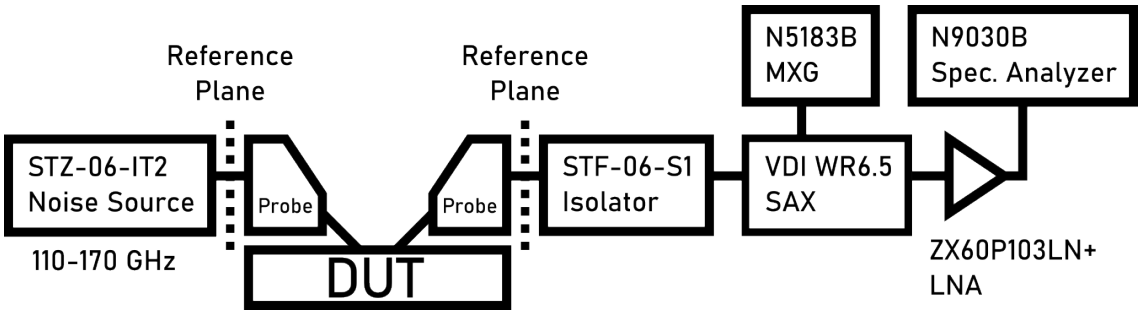


Figure 5.8: LNA Measurement Setup.

down-conversion equipment and calibrated reference planes are shown in Fig. 5.8. The dual side-band detection was done at a 1 GHz IF with a 240 kHz RBW. The noise contribution of the probe losses was removed by calculation, since the noise calibration reference plane was set at the input of the down-conversion chain. The probe loss was obtained with a measurement in a back-to-back configuration with a pair on an on-chip through.

As shown in Fig. 5.9, the measured noise figure remains below 9.3 dB for the entire D-band, while the lowest observed noise figure was 7.0 dB at 145 GHz. The noise is lower than simulated and a source of error may come from scalar de-embedding of the probe gain and noise contribution, since their losses were obtained with a scalar power measurement.

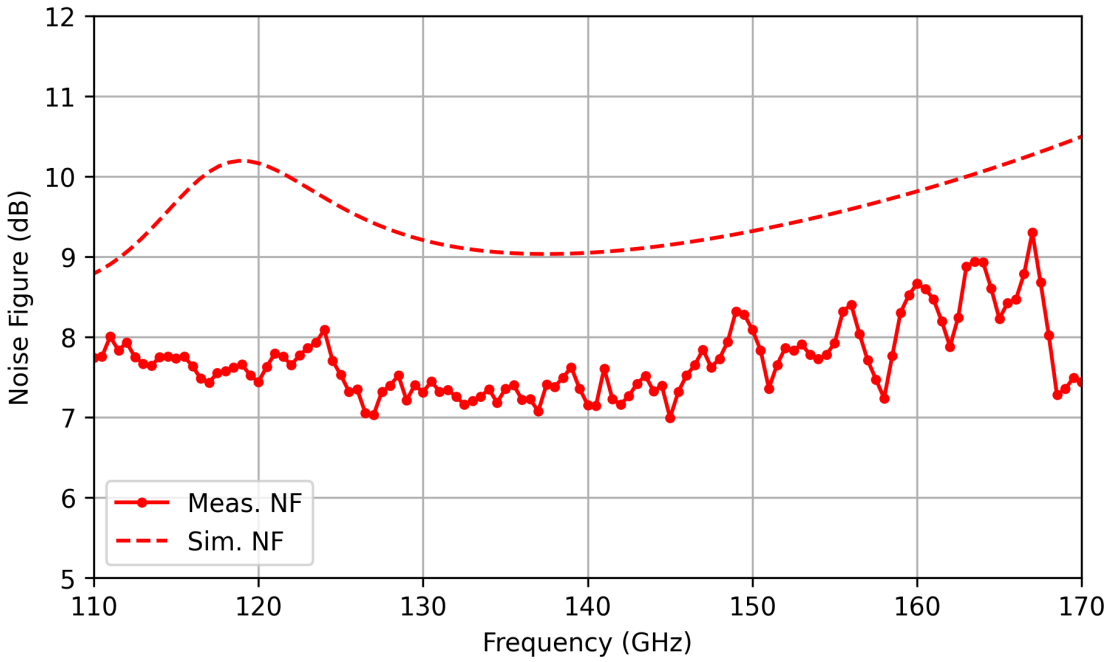


Figure 5.9: Measured Noise Figure.

Monte Carlo analysis on process and mismatch variation show that transistor does not totally account for the difference, with a 1.1 dB standard deviation for gain and a 0.4 dB standard deviation for noise figure. Bias sweeps in both simulation and measurement did not replicate the difference. The estimated noise measurement uncertainty is ± 0.7 dB over 2σ at 140 GHz. A reason that would explain both higher gain and lower noise than in simulation is that the simulation overestimates the loss of matching networks. The LNA was simulated with EMX in parts by stage, which could be a source of this difference.

5.4 Conclusion

An ultra-compact 4-stage D-band LNA for monolithic array integration, with demonstration of design with noise measure, is presented. Gain greater than 12 dB across D-

band is achieved by designing multiple cascaded stages with staggered tuning to provide gain at multiple bands. A minimum noise figure of 7.0 dB is demonstrated along with a 1-dB input compression power of -13.4 dBm. The LNA achieves this performance with an extremely low area consumption of only 0.015 mm^2, making it suitable for highly scaled receiver systems, without the need for additional packing as with heterogeneous integration.

Chapter 6

D-band Adaptive Receiver Array for Radar Using Dynamic LO Feedback

6.1 Introduction

This chapter explores implementation of circuit techniques that dynamically reduce power consumption in the LO chain to improve energy efficiency array receivers above 100 GHz, especially for adapting to dynamic channel environments where the received power P_{RX} varies by target or transmitter distance, illustrated in Fig. 6.1. This adaptation is especially important to save power when power consumption of transmit and receive arrays increases at higher frequency and would be prohibitive in mobile applications where the power budget is limited [1]. To accommodate high dynamic range of the received radar signal, the conversion gain and noise of the mixer is adjusted through the available LO power, eliminating additional variable-gain amplifiers in the signal path and decreasing system power consumption and circuit area. The circuits in this work implement the ability to trade off between noise contributions F and power consumption to achieve required SNR for particular tracking targets, conditions and ranges.

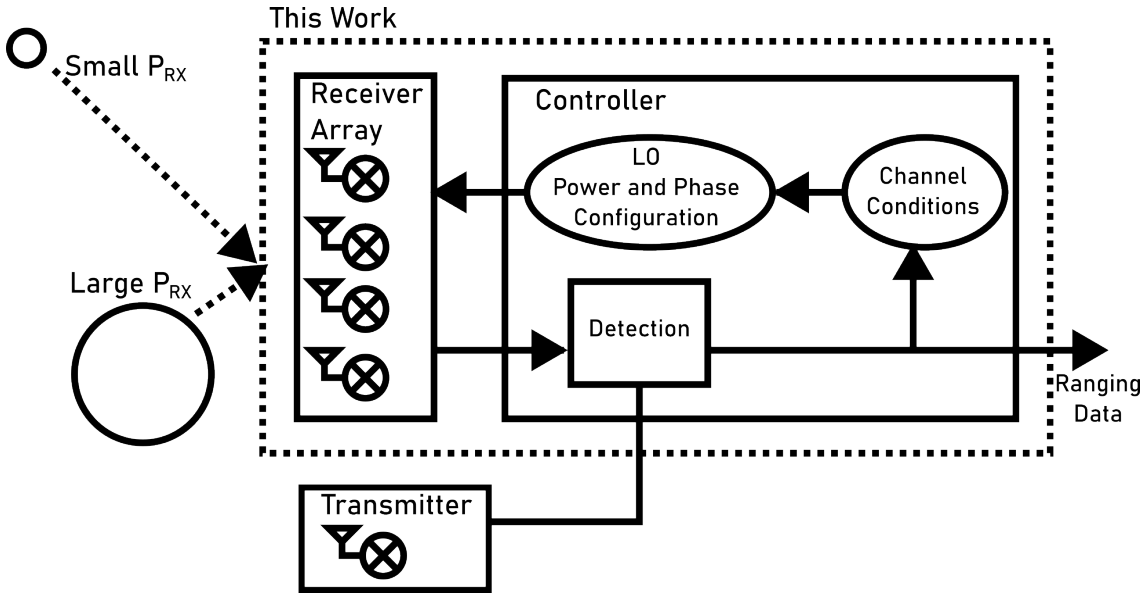


Figure 6.1: Proposed LO adaptation to dynamic sensing conditions in a FMCW radar application.

In addition to performance and power requirements, communication links and sensing at these frequencies require the receiver or transmitter integrated circuits (ICs) to be interfaced and packaged with high frequency antennas. Silicon semiconductor substrates have high dielectric constants which lead to a decrease in radiation efficiency. Additionally, an array implementation would require a high area consumption on the die at half wavelength spacing for the elements, which is cost intensive. This work integrates a glass substrate antenna with the receiver into a single module.

6.2 Adaptation Through Dynamic LO Control

The SNR for radar has the following relationship for a transmit-receive system [5].

$$SNR = \left(\frac{\sigma}{d^4}\right)\left(\frac{G_T G_R \lambda^2}{(4\pi)^3 kT}\right)\left(\frac{P_T T_c}{F}\right) = \frac{SNR_F}{F}, \tag{6.1}$$

where σ is target radar cross section (RCS), P_T is the transmitted power, G_T and G_R are the transmitter and receiver antenna gain, λ is the wavelength, T_c is the dwell time, d is the range, T is the receiver temperature , and F receiver noise factor. The first term in parenthesis is determined by the target, the second term is the transmit/receive antenna array, and the third term are parameters that can be readily adapted in real time. To control the power consumption for a fixed SNR, the output power of the transmitter or the noise figure of the receiver might be dynamic along with the dwell time. While the number of elements and power per element suggests a benefit of $20\log_{10} N$ for the TX, the reflected signal might be sensed to save power through the linear behavior of the RX. The final equality in (6.1) groups SNR terms except F into the term SNR_F for analysis. SNR_F is an upperbound on the possible SNR since $F > 1$.

Noise figure in the receiver is determined by the low-noise amplifier (LNA) as well as subsequent mixer and IF stages. A model for the receiver path in each channel would be

$$F = F_{LNA} + \frac{F_{MIX} - 1}{G_{LNA}} + \frac{F_{IF} - 1}{G_{LNA} G_{MIX}}, \tag{6.2}$$

where the Friis formula is applied assuming perfect image rejection of the noise. Variable LNA gain might change the reflection coefficient at the antenna while providing marginal changes in power. Considering how power consumption is partitioned in the RX, we can construct a power model related to the noise figure. In general, the noise factor might be - to first order - inversely related the DC power consumption. In other words, $F_{LNA} = \frac{\rho_{LNA}}{P_{LNA}}$ and $F_{IF} = \frac{\rho_{IF}}{P_{IF}}$. In a mixer, the LO power would contribute to conversion gain and also mixer noise factor $F_{MIX} = \frac{\rho_{MIX}}{P_{LO}}$. Substituting these power dependent terms,

$$F = \frac{\rho_{LNA}}{P_{LNA}} + \frac{\rho_{MIX} - P_{LO}}{G_{LNA} P_{LO}} + \frac{\rho_{IF} - P_{IF}}{G_{LNA} \gamma_{MIX} P_{LO} P_{IF}}. \tag{6.3}$$

This model can develop an approximation for the LO power dependent terms in the receiver noise figure.

$$F = F_0 + \frac{F_1}{P_{LO}}, \tag{6.4}$$

where $F_0 = \frac{\rho_{LNA}}{P_{LNA}} - \frac{1}{G_{LNA}}$ and $F_1 = \frac{1}{G_{LNA}}\left(\rho_{MIX} + \frac{\rho_{IF}-P_{IF}}{\gamma_{MIX}P_{IF}}\right)$. Consequently, the SNR can be directly controlled through LO power consumption.

$$SNR = SNR_F\left(\frac{P_{LO}}{F_1 + P_{LO}F_0}\right), \tag{6.5}$$

Large values of F_1 relative to F_0 better leverage LO power adaptation in mm-wave systems where LNA gain is low. To translate the LO power to DC power consumption, we account for the power consumption required for frequency multiplication with η_{MULT}, the RF-to-DC energy efficiency of the multiplier. For mm-wave receivers, the large multiplication factor typically suggests an η_{MULT} of less than 10%. The total power consumption of the receiver is $P_{DC} = P_{LNA} + P_{IF} + P_{LO}/\eta_{MULT}$. If we desire a minimum SNR, (6.5) can be rewritten in terms of the required DC power consumption.

$$P_{DC,min} = P_{LNA} + P_{IF} + \frac{F_1}{\eta_{MULT}\left(\frac{SNR_F}{SNR_{MIN}} - F_0\right)} \tag{6.6}$$

In millimeter-wave receivers, the trade-off between power consumption is captured in Fig. 6.2 for different η_{MULT}. The SNR power adaptation is possible with the low multiplier efficiency. In the case of $\eta_{MULT} = 0.01$, a change of 5 dB in SNR can reduce the required channel DC power from around 420 mW to 200 mW. Across an array of receivers, this is a substantial power savings but is of critical important for a D-band radar receiver array.

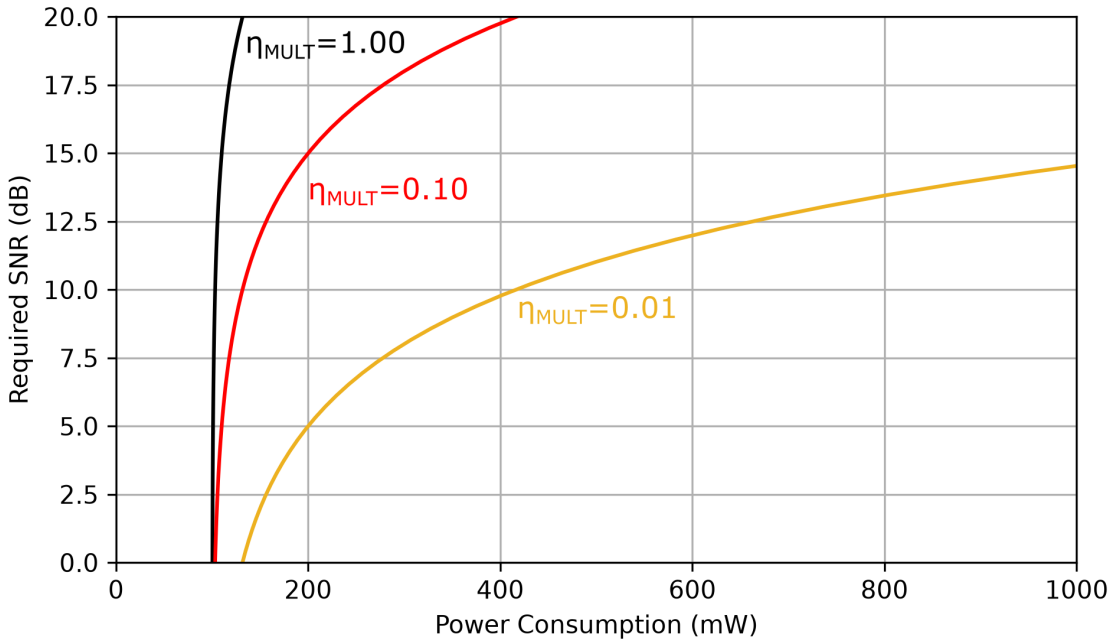
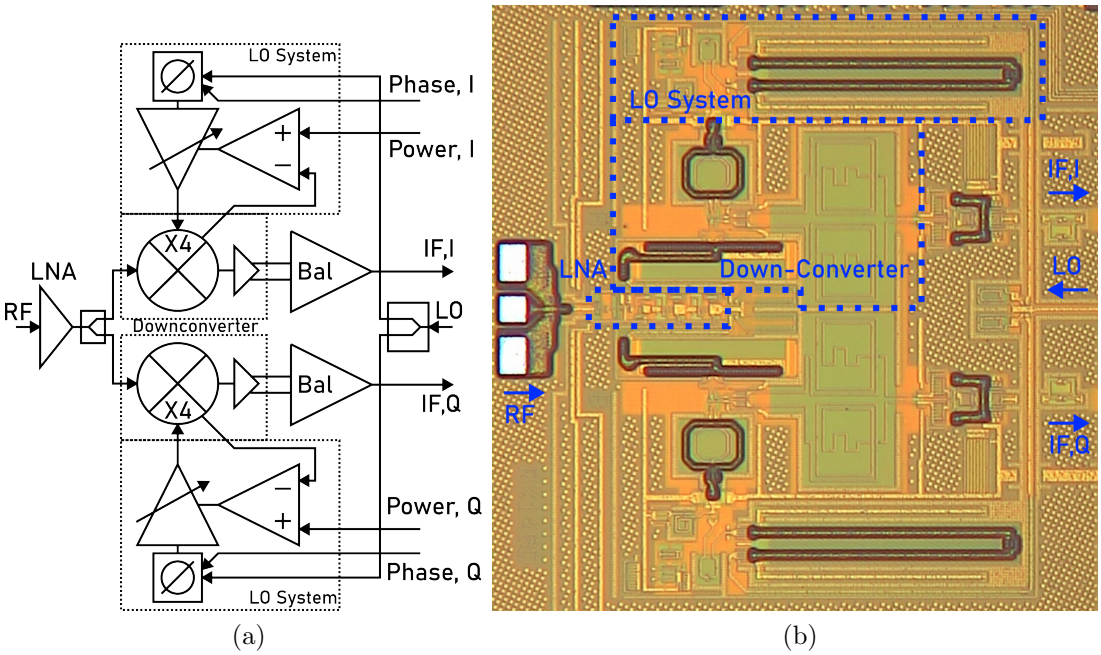


Figure 6.2: Minimum power consumption required for a target SNR in a radar application ($F_0 = 10$, $F_1 = 100$, $P_0 = 100$ mW).

6.3 Receiver Design

The receiver is a 4-element RX array, where each element has an I and Q channel subharmonic downconverter with independent control of their LO power and phase, shown in Fig. 6.3. By implementing variable power and phase shifting in the LO path, receiver configuration can be achieved across a wide bandwidth, without additional components loss in the RF path. This LO control is enabled by the design of the downconverter, which linearizes the relationship between gain and LO power variation and detects delivered LO power for feedback. Ultimately, this control allows the receiver to adapt to channel conditions and save power, as shown in Fig. 6.5 Each element has one LNA, and its output is split by a wilkinson divider to the I and Q channels. An active balun converts the IF signal from differential to single ended mode. In the array, elements are placed every half wavelength of 1070 µm. The LO power is distributed to each element

at 35 GHz with a lumped element Wilkinson divider tree.



(a) (b)

Figure 6.3: (a) Diagram and (b) chip micrograph of a single IQ element in the arrayed receiver system.

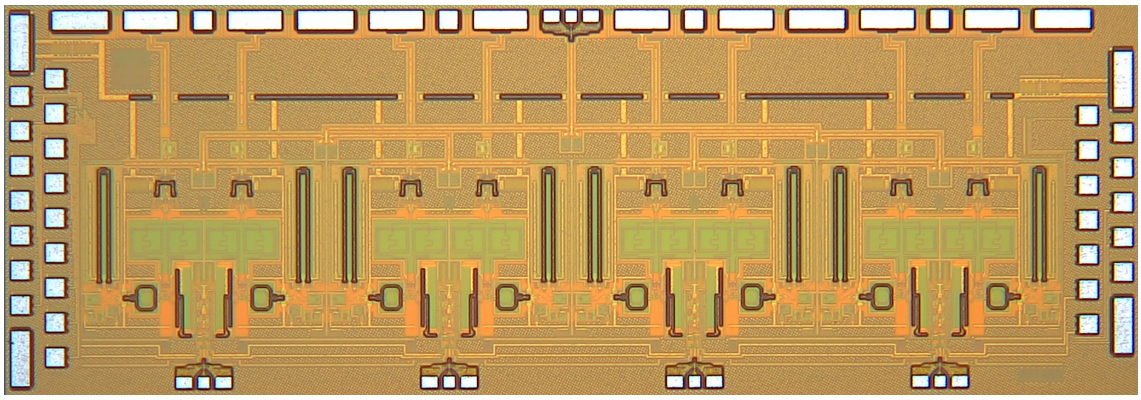
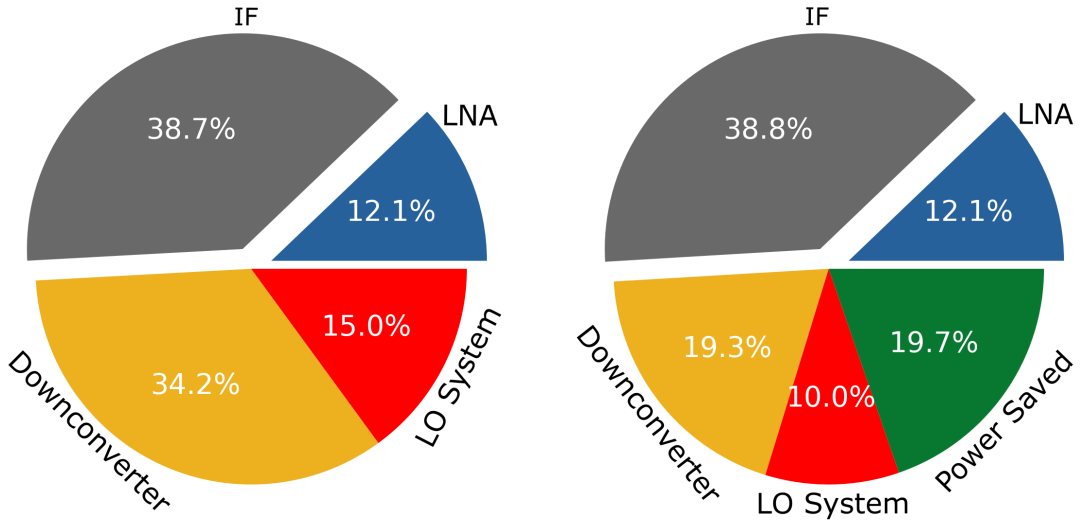


Figure 6.4: D-band 4-element IQ array with dimensions 2841 um x 1628 um.



(a) (b)

Figure 6.5: Simulated (a) maximum and (b) minimum power consumption of a single IQ element of this work through dynamic LO control. LNA: 32.3 mW, IF: 103 mW, Downconverter: 51.4-90.9mW, LO Control System: 26.7-39.8 mW, Power saved: 52.4 mW

6.3.1 Downconverter with Bias Feedback

The down-conversion system implements a novel sub-harmonic mixer that linearizes its gain response to changes in LO power through resistive feedback [36]. The circuit provides voltage signal V_{det}, which corresponds to the LO power used for down-conversion, to control LO power to adapt the dynamic range.

A typical push-pull frequency multiplier or sub-harmonic mixer generates a second harmonic [18]. The proposed subharmonic mixer utilizes the fourth harmonic from a push-pull frequency multiplier implemented with transistors Q_1 and Q_2, shown in Fig. 6.7. The harmonic content of the combined collector currents I_C of Q_1 and Q_2 depend on the conduction cycle, which is controlled through their base voltage bias. Modeling the collector current as a half-wave rectified sinusoidal pulse train, illustrated in Fig. 6.6, the Fourier series expansion presents the current harmonics as in Eq. 6.7 [11][12].

$$I_n = I_{max}\frac{4t_0}{\pi T}\begin{cases} 1 & \text{, if } n = 0 \\ 2\cdot\left|\frac{\cos\left(\frac{n\pi t_0}{T}\right)}{1-\left(\frac{n\pi t_0}{T}\right)^2}\right| & \text{, if } n \text{ even} \\ 0 & \text{, if } n \text{ odd} \end{cases} \tag{6.7}$$

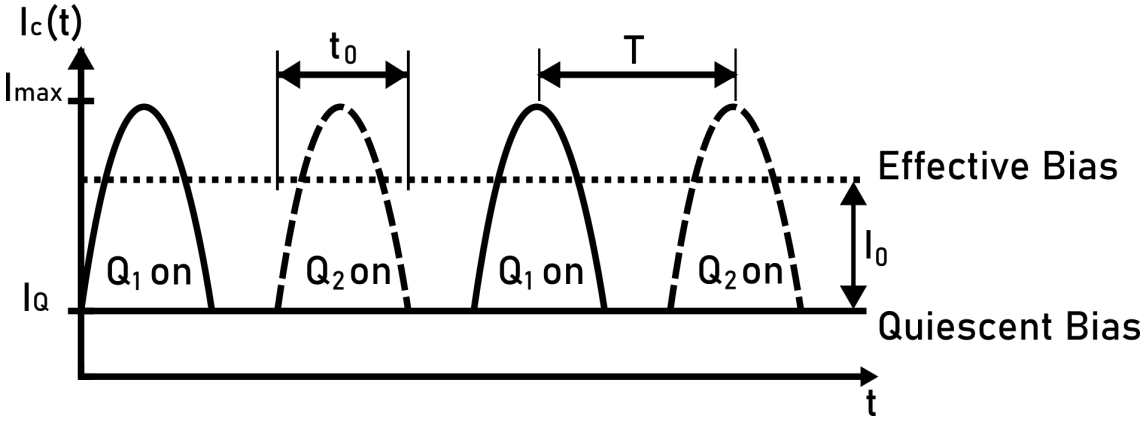


Figure 6.6: Instantaneous output current from a push pull frequency multiplier stage and its time-average impact on bias.

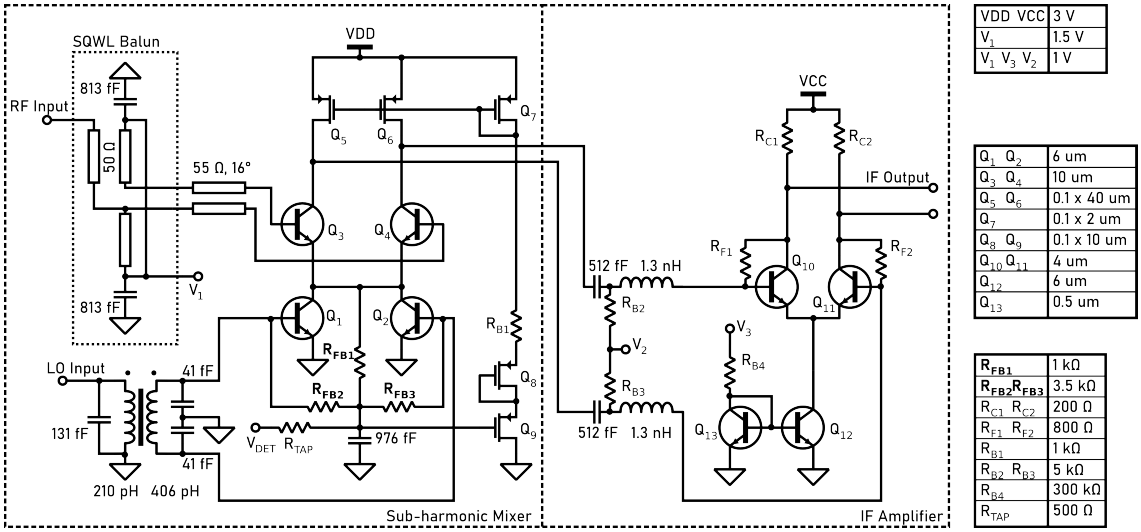


Figure 6.7: Schematic of downconverter with bias feedback and dynamic conversion gain. V_{DET} provides a voltage signal corresponding to detected LO power in the mixer.

In a typical multiplier, the bases of Q_1 and Q_2 are biased with a static voltage, tuned

for a particular LO input power [11]. This method, however, does not provide the best bias across a range of input powers. As shown by the DC current where $n = 0$ in Eq. (6.7), the average effective output current of Q_1 and Q_2 is $I_C = I_Q + I_0$, where I_Q is the quiescent bias current and I_0 is the additional current generated from the rectification of the input sinusoid. The additional current causes the transconductance to change with output power, a source of nonlinear gain in the multiplier.

To counteract the current variation, large feedback resistances, R_{FB1}, R_{FB2}, and R_{FB3}, from the collectors of Q_1 and Q_2 set the common mode base bias and compensate for the additional current created by the output waveform at DC. If we consider $V_{BE1,2} \approx V_{BE3,4}$, and $I_{C3,4} \approx I_{C1,2}$,

$$I_{C3,4} = \beta_{1,2} \frac{V_1 - 2V_{BE}}{R_{FB1} + R_{FB2}||R_{FB3}} \tag{6.8}$$

Thus, the feedback resistance reduces the influence from the additional rectified DC current. Although feedback compensates for the additional rectified current, the current change is not completely canceled due to variations in the effective time-averaged $\beta_{1,2}$ over power variation. The feedback bias allows for a gradual change in gain over a wider range of LO input powers compared to the static bias approach, as shown in Fig. 6.8. The conversion gain remains high over a range of LO power and improves the robustness of the circuit to LO power variation. With a 6 dB LO power backoff from peak conversion gain, the feedback biased circuit has 17 dB more gain than the static biased version. Additionally, the feedback network provides voltage V_{DET} corresponding to output current, enabling monitoring of conversion gain.

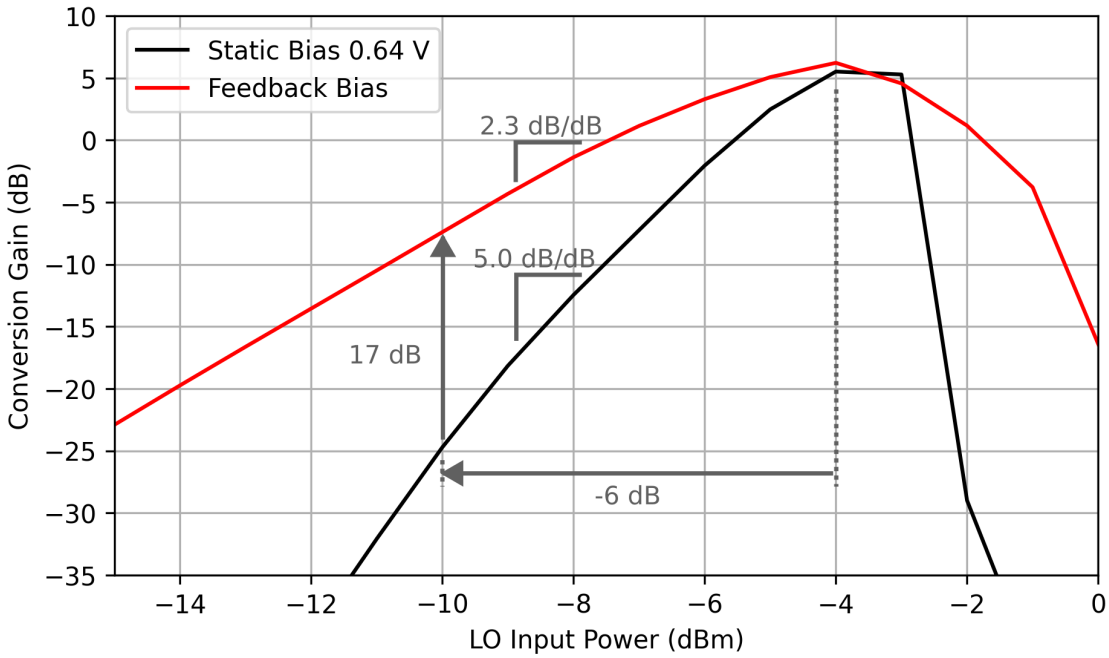


Figure 6.8: Simulated effect of bias feedback in the downconverter compared to a typical static bias approach.

6.3.2 LO-based Phased Array Control System

The V_{det} signal monitors and sets the power delivered to the downconverter with feedback through the LO system, shown in Fig. 6.10. To control the LO, a reflection-type-phase-shifter (RTPS) provides the phase shift, while a variable-gain amplifier (VGA) controls the power of the LO before the LO is delivered the the downconverter. An op-amp compares the down-converter's LO power detection voltage V_{det} to a provided reference power control voltage, V_{REF}, and sets the VGA at a gain level that maintains a desired LO power. Since the VGA is placed after the phase shifter, variation in phase shifter gain is also suppressed in this system. With feedback, this system maintains LO power delivered to the downconverter, independent of supplied LO power to this system and phase setting. The RTPS and VGA are measured as standalone test blocks. The RTPS is tested with control voltage supplied through the op-amp configured as a non-

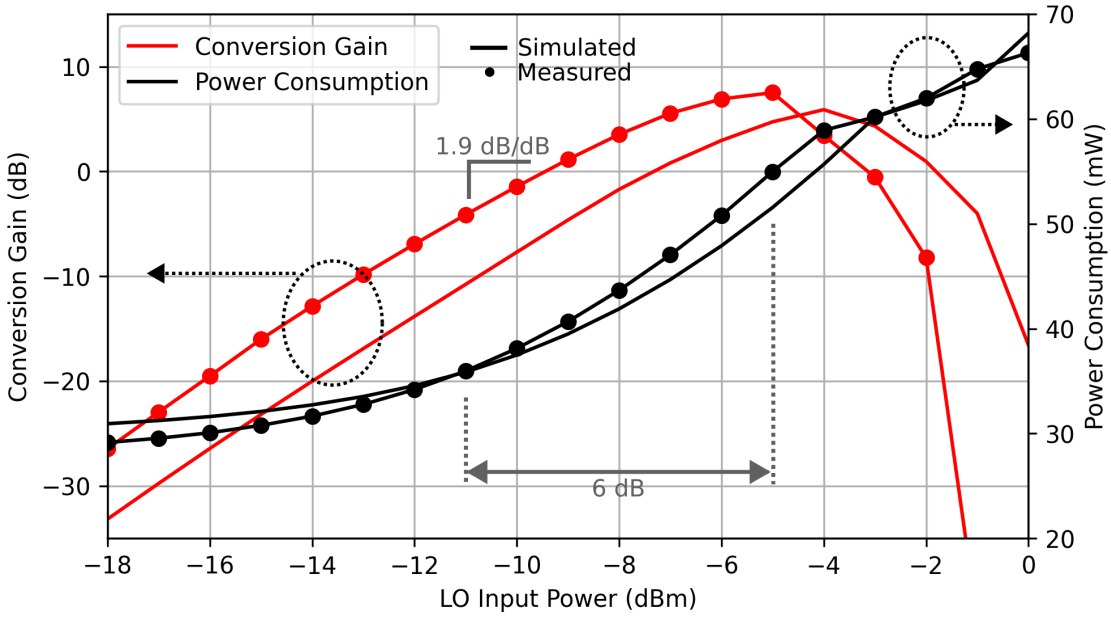
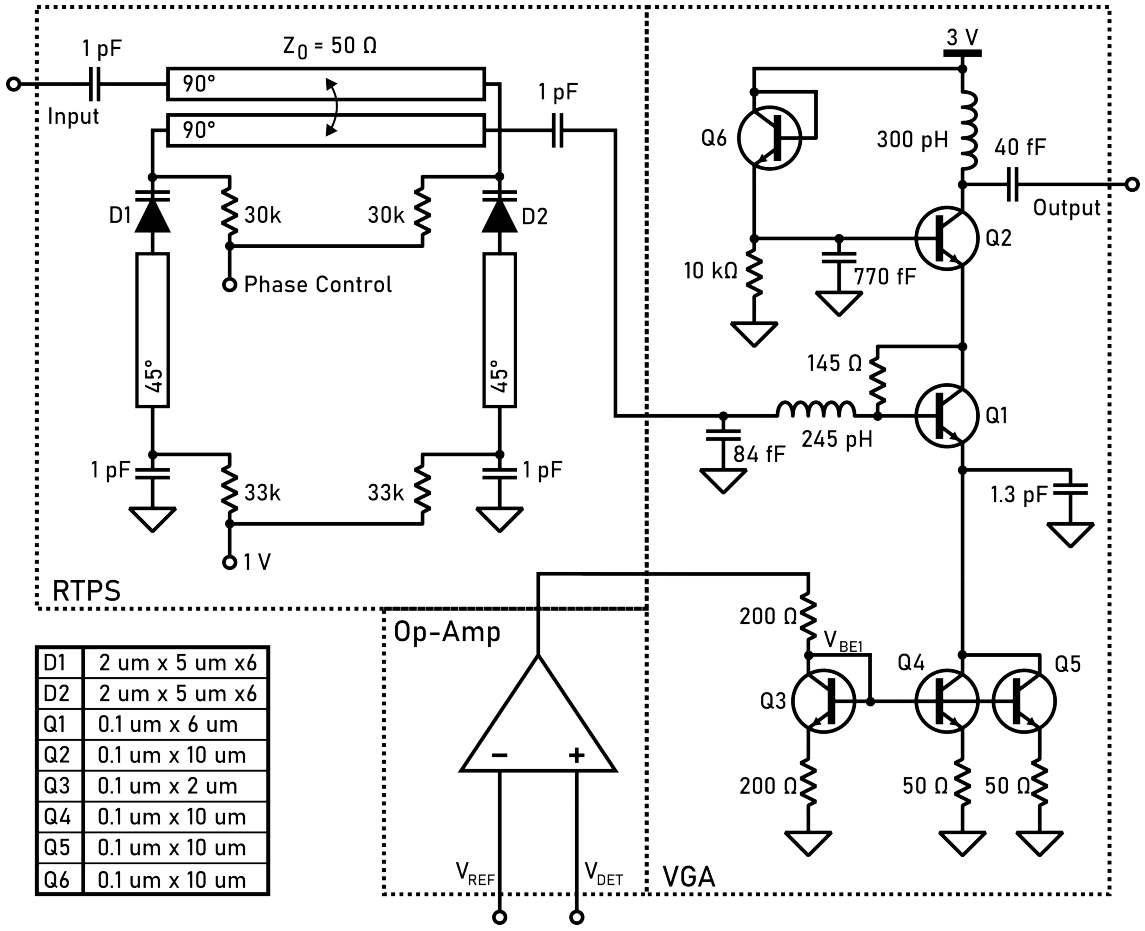


Figure 6.9: Measured conversion gain and DC power consumption at 155 GHz RF and 140 GHz LO with -24 dBm of RF input power.

inverting voltage follower. The measured phase shift control and undesired gain variation in the RTPS is shown in Fig. 6.11, while Fig. 6.12 shows VGA gain control and undesired phase variation. Measured results are close to simulation for both circuits, except the RTPS phase shift range extends towards the upper voltage extremity of the simulation model. Each downconverter channel in the arrayed system has independent polar vector control of the LO phase and power, provided by a pair of reference voltages to set the control. For consistent distribution of the power control voltage V_{REF}, a current mirror is added in the array to reduce sensitivity to process variation and voltage drop across the chip for this signal.

6.3.3 Low Noise Amplifier

A compact 4-stage D-band LNA is implemented to suppress noise before the RF signal is split by a Wilkinson divider to the I and Q downconverters [37]. Gain greater than 12



D1	2 um x 5 um x6
D2	2 um x 5 um x6
Q1	0.1 um x 6 um
Q2	0.1 um x 10 um
Q3	0.1 um x 2 um
Q4	0.1 um x 10 um
Q5	0.1 um x 10 um
Q6	0.1 um x 10 um

Figure 6.10: Schematic of LO phase and power control system.

dB across D-band is achieved by designing multiple cascaded stages with staggered tuning to provide gain at multiple bands. A minimum noise figure of 7.0 dB is demonstrated along with a 1-dB input compression power of -13.4 dBm at 37.6 mW of DC power consumption. The LNA achieves this performance with compact area consumption of only 0.015 mm^2.

6.4 Dual-Slotted Patch Antenna

An array of patch antennas with a dual slot feature is implemented on glass substrate with the stackup shown in Fig. 6.15. The substrate is composed of Asahi Glass Company

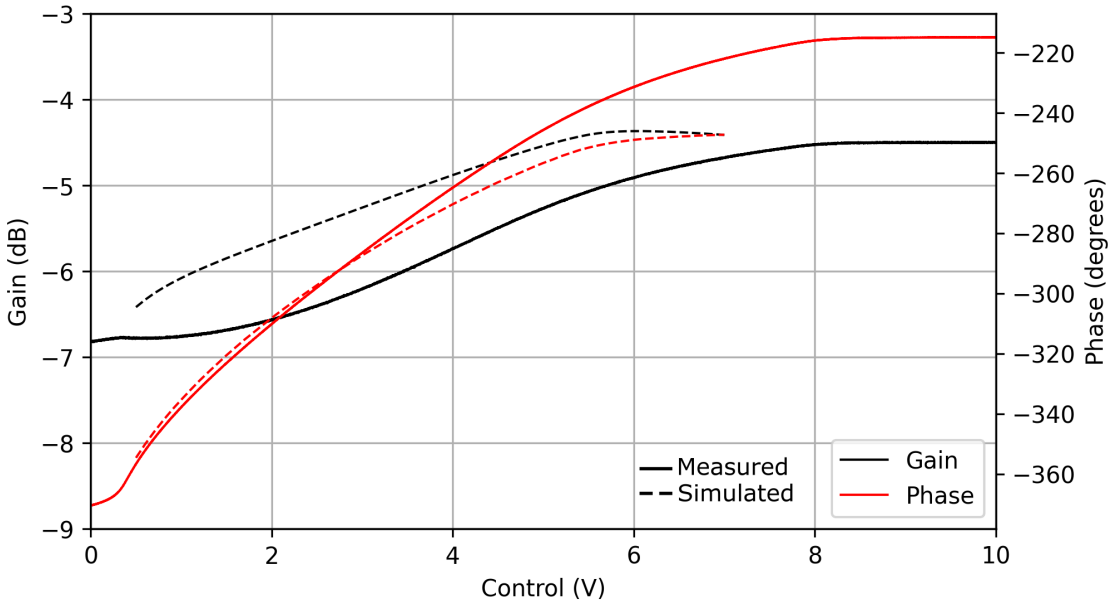


Figure 6.11: Measured gain and phase characteristics of RTPS over control voltages at 35 GHz

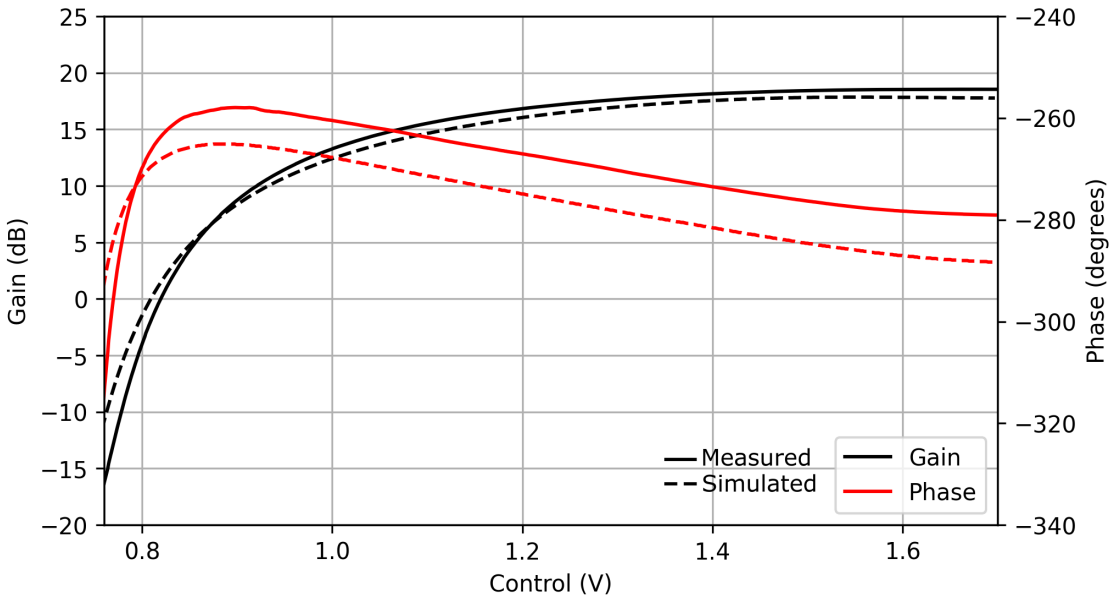


Figure 6.12: Measured gain and phase characteristics of VGA over control voltages at 35 GHz

(AGC) ENA1 boro-aluminosilicate glass laminated with a ABF GL102 polymer film. The metallization is 7 µm of electro-plated copper on both sides, where only the top side is

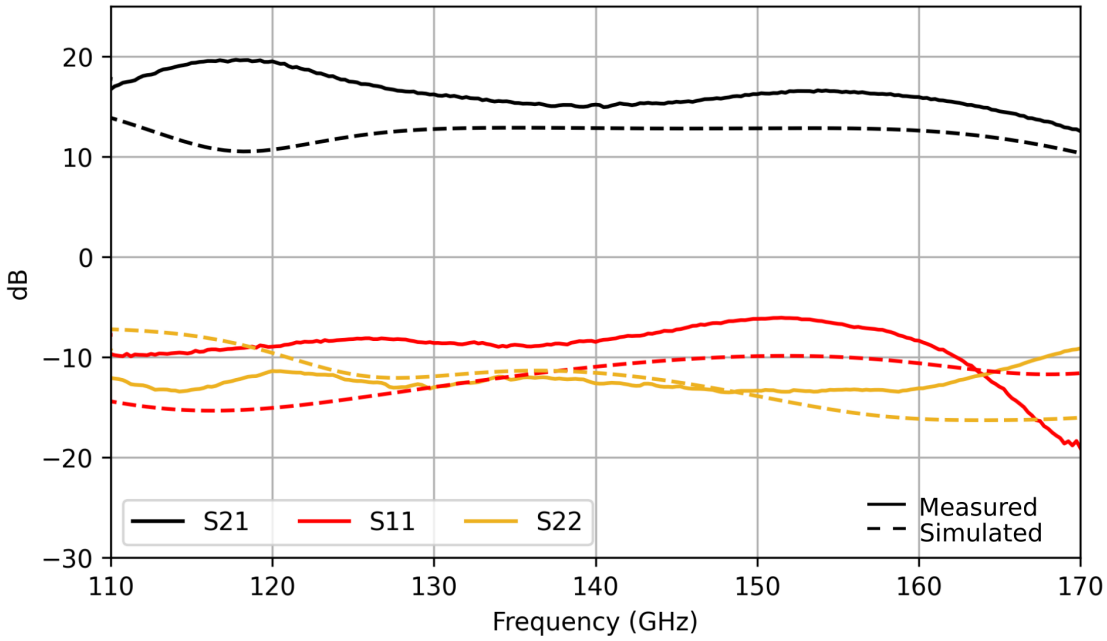


Figure 6.13: Measured S-parameters of the LNA.

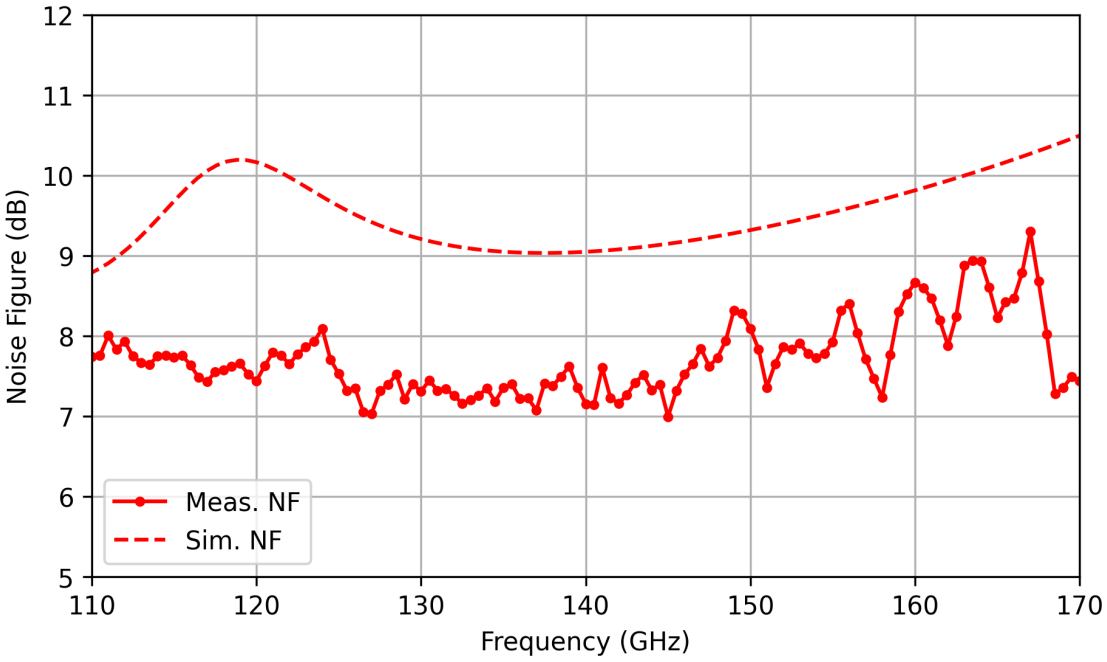


Figure 6.14: Measured noise figure of the LNA.

patterned. A deposition of 50 nm Ti, 300 nm Ni, and 300 nm of Au was used as the surface finish on top of the copper to support wire bond adhesion. The substrate has an effective dielectric constant of 4.72 with a loss tangent of 0.012 at 140 GHz as measured in [38]. Additionally, plated through glass vias (TGVs) of 100 µm were used to connect the top and bottom metallization.

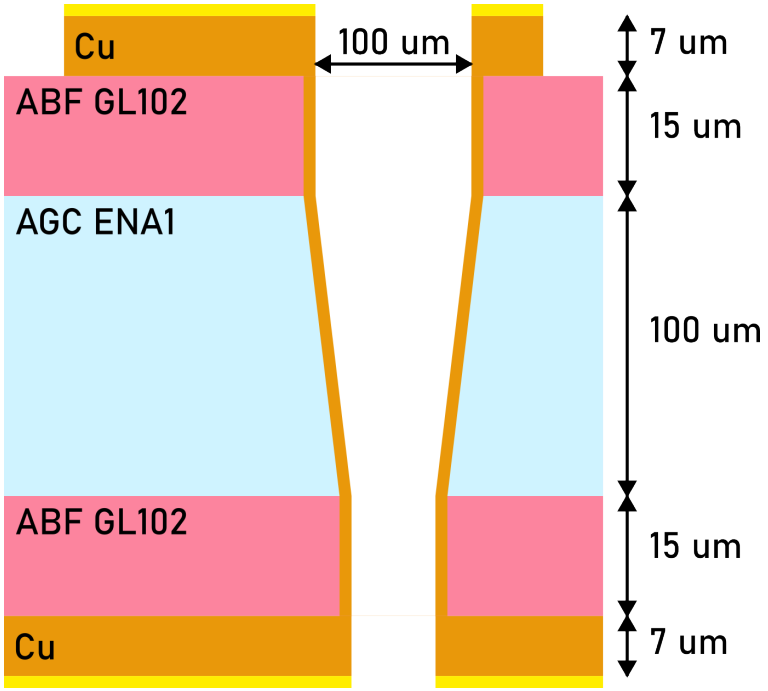


Figure 6.15: Antenna substrate stack-up with through-glass-via and gold finishing plating.

Connection to the receiver chip is through a coplanar feed through wire-bonds, which necessitated a transition from coplanar to microstrip on the antenna's glass substrate, shown in Fig. 6.17b. Radial stubs were used to provide a virtual electrical short for the top side ground metal to the back metal, in addition to the 130µm tall through-glass-vias (TGV). A tapered microstrip line is used within this transition to match the coplanar 50 Ω to the antenna's microstrip mode of 120 Ω. Because a 50 Ω microstrip line with this substrate is excessively wide compared to the antenna dimensions, the antenna patch was designed for a 120 Ω feed line which also facilitated connection to the transition.

Since the patch antenna has inherent DC isolation from ground, no DC-blocking element is needed on the antenna nor the receiver integrated circuit, which reduces area and loss.

Dual slots in the patch antenna were used to facilitate matching, and the resulting structure is shown in Fig. 6.17a. Each slot introduces a resonance in the patch structure that allows for a wider bandwidth of matching, compared to typical patch antennas [39] [30]. In this slotted patch antenna, $D_2 - D_1$ and $L1$ implements a second resonance from conventional design, in addition to the patch's intrinsic resonance, to match at high frequencies, while D_2 and L_2 implements a third resonance to facilitate low frequency matching, and their effects are shown in Fig. 6.16. These dimensional parameters were optimized to yield the best match and gain, resulting in a simulated radiation efficiency of 81%. In the antenna array, six of the patches were placed every 1070 µm, half wavelength at 140 GHz. Of the 6 antennas only the center 4 are used, while the outer 2 are dummy antennas for a more consistent radiation pattern across used antennas.

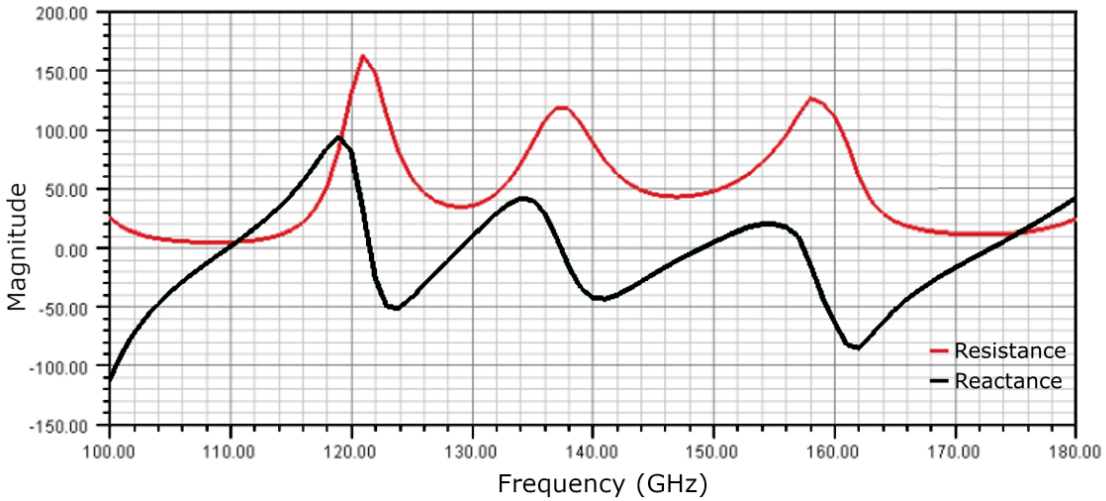
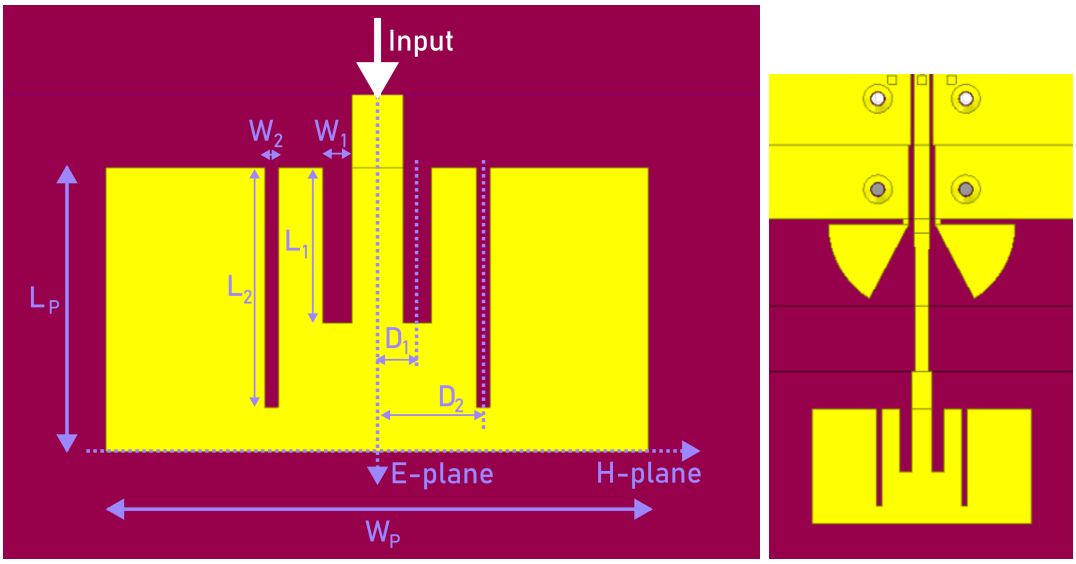


Figure 6.16: Simulated real and imaginary impedance for the dual slot patch antenna with coplanar feed.



(a) (b)

Figure 6.17: (a)140-GHz dual slotted patch antenna on glass substrate, with a feed impedance of 120 Ω It has dimensions $L_P = 391\,\mu m$, $W_P = 745\,\mu m$, $W_1 = 39\,\mu m$, $L_1 = 214\,\mu m$, $D_1 = 55\,\mu m$, $W_2 = 19\,\mu m$, and $L_2 = 329\,\mu m$, $D_1 = 145\,\mu m$. (b) Dual slotted patch antenna implemented with coplanar transition feed.

6.4.1 Antenna Measurement

The phase center of the antennas is offset from the distance measurement references, so the offset is inferred with a distance sweep. Then, the effective radiation distance and antenna pair gain is obtained using that offset [40]. The relation for this inference is obtained through Friis transmission equation which takes the following form.

$$\frac{P_R}{P_T} = |S_{21}|^2 = G_R G_T \left(\frac{\lambda_0}{4\pi d}\right)^2 \tag{6.9}$$

The formula can be expressed, in logarithmic form, as a relation that relates antenna pair gain $G_R + G_T$ to the measured gain G_{21}, with the effect of placing the antenna pair a distance d apart. Since distance measurement is made offset from the antennas' phase centers, true distance d of the phase centers is expressed as the measured distance d_M with an offset Δd.

$$\begin{aligned} G_{21} &= G_R + G_T + 20\log\left(\frac{\lambda}{4\pi}\right) - 20\log(d) \\ G_R + G_T &= G_{21} + 20\log(d) - 20\log\left(\frac{\lambda}{4\pi}\right) \\ G_R + G_T &= G_{21} + 20\log(d_M - \Delta d) - 20\log\left(\frac{\lambda}{4\pi}\right) \end{aligned} \tag{6.10}$$

In this relation, the pair gain is invariant with the measured gain with the loss from Friis transmission relation, if Δd is known and subtracted from the distance measurement to obtain the true distance. In this way, measurements of pair gains at multiple distances can be used to search for a Δd offset that achieves the relation's invariance. In implementation, this search is to find a Δd such that the root mean square error of the measured gain is minimized over multiple measurement distances to optimize towards the invariance condition.

The antenna was measured with the setup shown in Fig. with the setup shown in Fig. 6.18. First, measurements across swept distances with a pair of standard horn antennas to obtain the offset as well as their pair gain. Then, this method is applied to the test antenna and the standard horn antenna to measure the test antenna's gain. Distances between 0.30 m to 0.42 m were used to evaluate the gain. Although the exact threshold between near-field and far-field was not determined, these distances are sufficiently in the far-field to satisfy the relation's invariance across distance. Fig. 6.19 shows the measured and simulated antenna gain and return loss obtained with this method. The reduction in gain at 147 GHz is probably due to interference from the probe, since the probe used to measure the antenna chip is very close to the antenna. The gain measurement is repeated with a packaged antenna in the module, with results in Fig. 6.36 showing that the gain reduction at 147 GHz is not present without the probe.

The antenna's radiation pattern was measured with a receiving extender on a pivoting

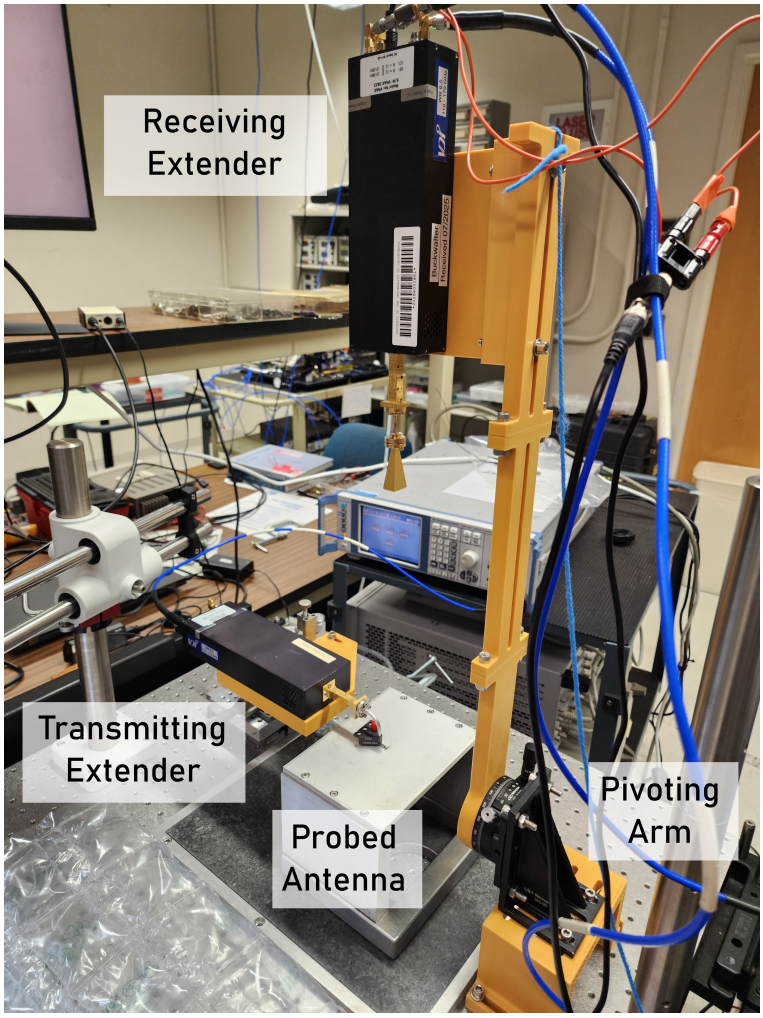


Figure 6.18: Probed antenna measurement setup with pivoting arm.

arm, and its results are shown in Fig. 6.20. A 90° waveguide twist was used when switching from E-plane to H-plane measurements to maintain antenna polarization. The radiation patterns are close to simulation. For angles where the probe and equipment is physically close to the line of sight, there is a reduction in gain, shown in Fig. 6.20b for angles below 0°.

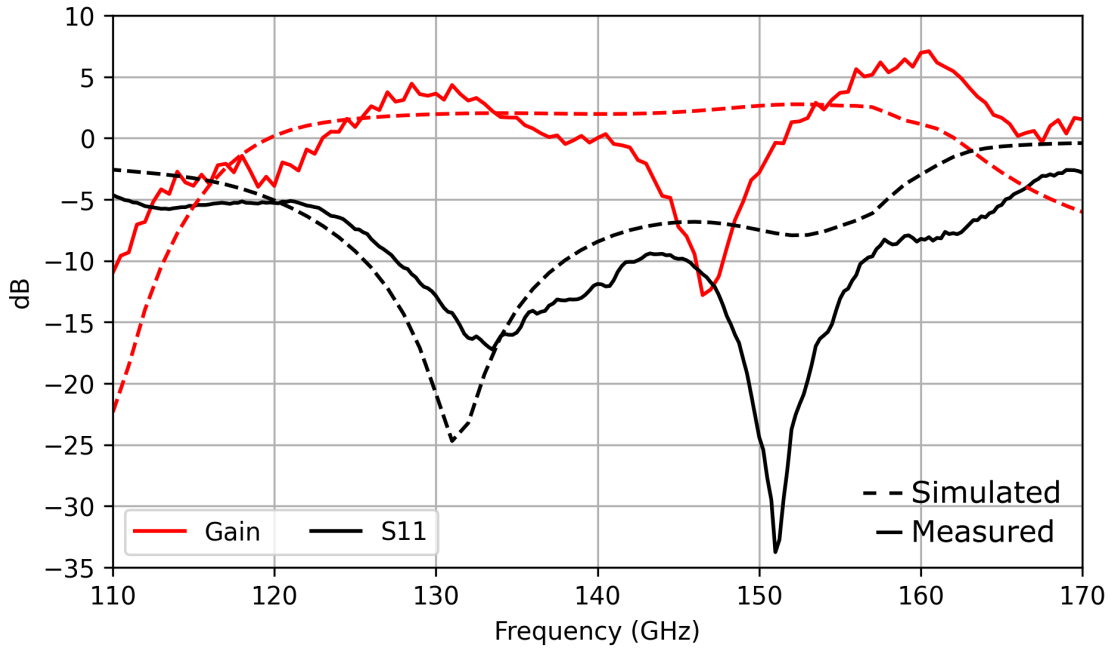


Figure 6.19: Measured return loss and gain of single antenna element.

6.5 Receiver Module Packaging

The receiver and glass antenna chips were packaged together onto a printed circuit board of Rogers 3010 material, with dielectric constant of 11.2 and a loss tangent of 0.0022, assembled as shown in Fig. 6.21. Bulk capacitance for supply lines were added in the form of wire-bondable capacitors next to the chip with liquid silver epoxy, supplemented with soldered chip capacitors. Mini-SMP connectors were used connect LO and IF lines from the board, and gold bond wires were used to connect the receiver chip to both the board and the antenna chip. The circuit board assembly is mounted on a machined aluminum backing with fasteners and silver thermal paste for structural rigidity and thermal sinking, shown in Fig. 6.22b. A PTFE shield was added to the mechanical assembly for protection, but was removed for electrical characterization of the system. A version of the module was made without the antenna chip for testing the receiver chip by itself through a probe on its RF ports.

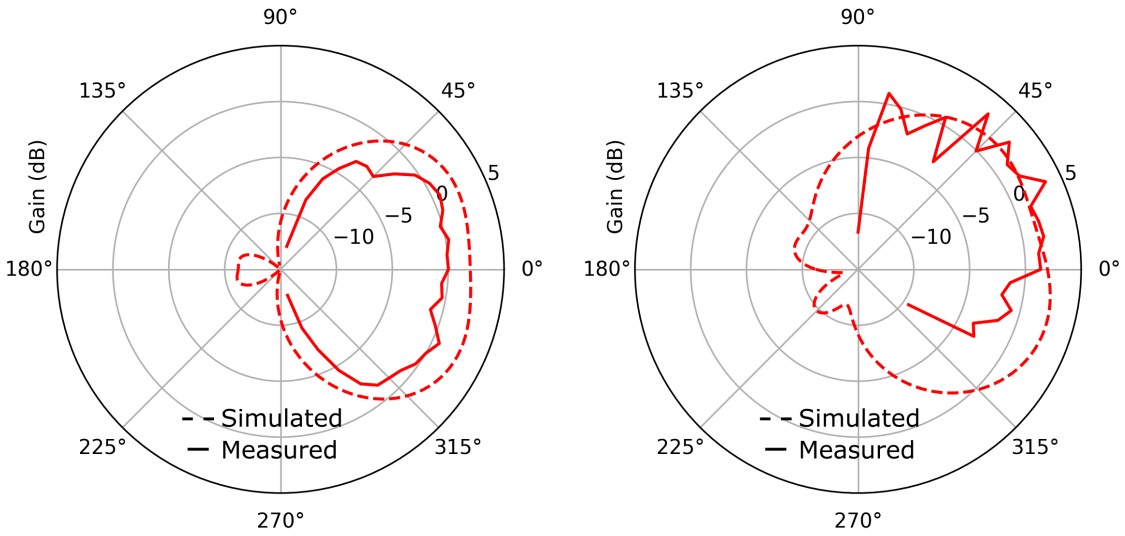


Figure 6.20: (a) H-plane and (b) E-plane gain patterns of the antenna element at 140 GHz.

6.5.1 Chip Height Leveling with Epoxy

Due of the height difference between the chips, Hysol CF3350 epoxy preforms of different thicknesses were used to level the top surfaces of the attached chips to reduce the bondwire length between them. The total height of the glass antenna chip is 144 µm, while the height of the receiver chip is 108 µm. The receiver chip was attached with a 4 mil (101.6 µm) preform while the antenna chip was attached with a 2 mil (50.8 µm) preform.

First, both die were placed on their epoxy preforms next to each other. Then with the bonder placement tool, 5 N was applied to both chips. The epoxy was cured for 30 minutes under pressure at 125°C. The epoxy preform dimensions were linearly undersized by 15% relative to the chip dimensions to take into account lateral expansion of the preforms from the compression force applied during curing. Because the force is applied to both chips at the same time, the chips are leveled in height by the same contact surface of the bonder placement tool. Optical profilometer measurements made on bonded samples

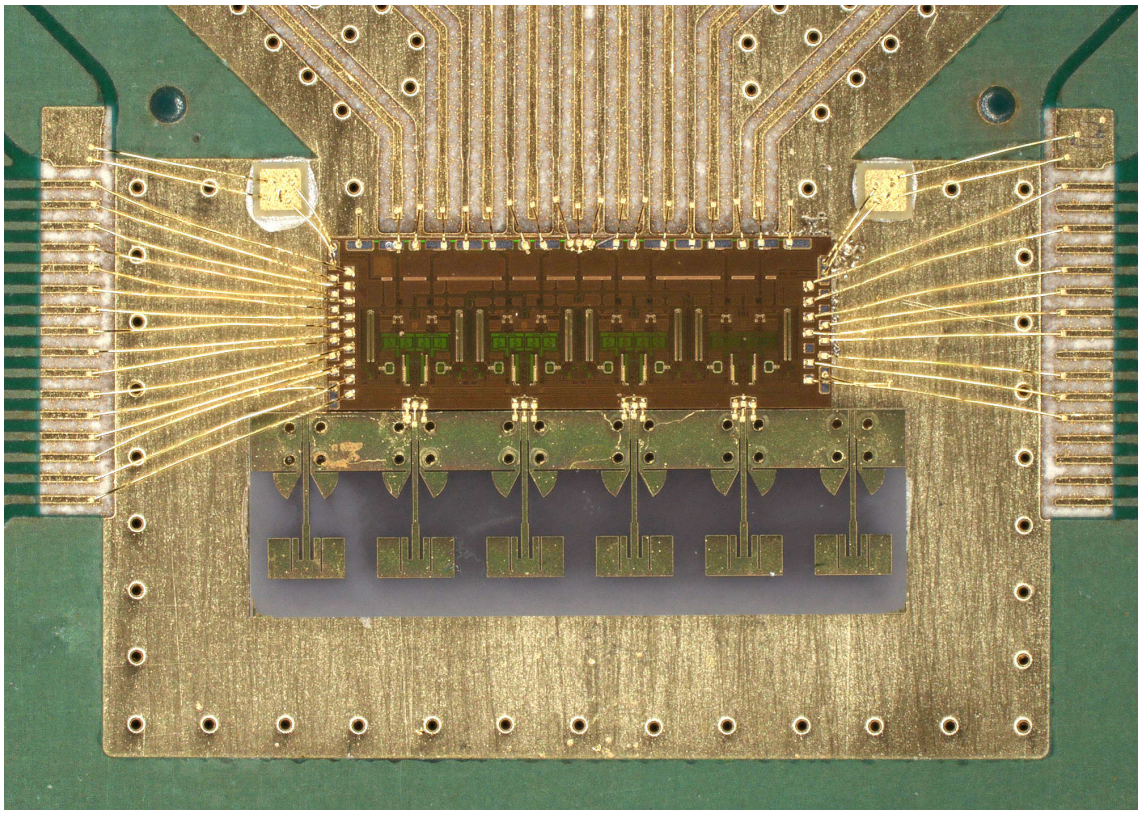
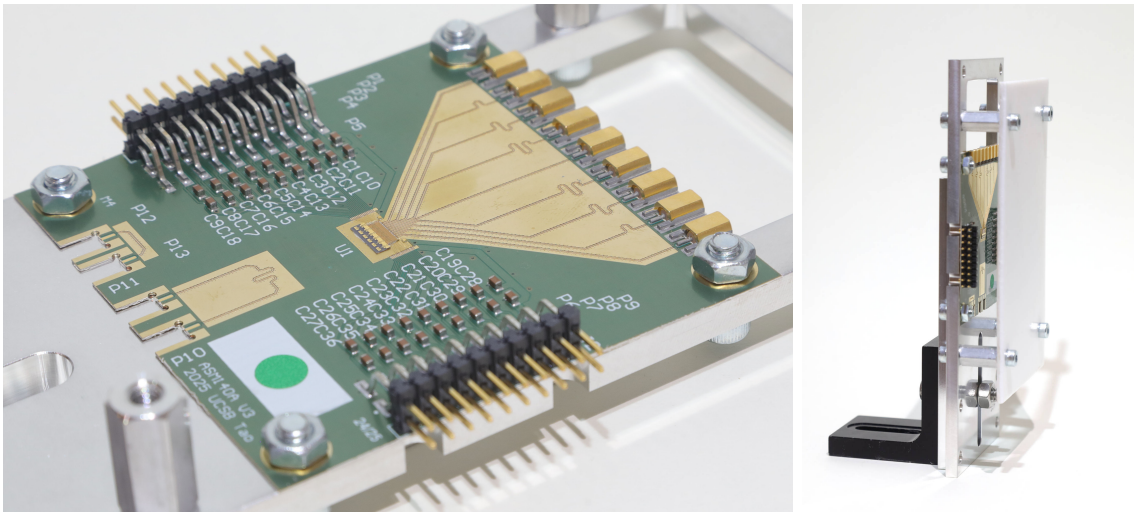


Figure 6.21: Attached receiver array with glass substrate antenna on a PCB within the packaged receiver module. The receiver chip has dimensions of 4841 um x 1628 um, while the antenna chip has dimensions of 6360 um x 1985 um

show that this method matches chip heights to about 10 µm.

6.5.2 Receiver Module Controller

The receiver module controller, shown in Fig. 6.23, provides power, power consumption measurement, and analog control to the receiver module from a computer. A STMicroelectronics STM32F411RE microcontroller is used with USB connectivity, allowing a connected computer to find mapping between receiver settings and receiver performance, as well as to implement that mapping for adaptation of the receiver's power consumption to performance requirements in dynamic sensing conditions. Since the receiver's configuration is set by analog bias voltages, the module controller implements 12-bit



(a) (b)

Figure 6.22: (a) Receiver PCB assembly and (b) receiver module with PTFE protective shield

digital-to-analog converters (DAC) to set the receiver's LO power and phase settings.

6.6 Receiver Channel Measurement Results

For measurements of channels on the receiver chip itself, a version of the receiver module was fabricated without the antenna to provide RF power to the receiver chip through a probe instead, while all other connections remain the same. Since there are 4 separate elements in the array, only one is tested at a time with the probed measurements.

6.6.1 Probed Receiver Power and Gain

Gain and phase characteristics of the receiver chip were measured by providing RF power through a probe, with the signal generated from a network analyzer, D-band extender, and variable attenuator. The LO was provided to the module's connectorized port, and the IF was measured with a spectrum analyzer. The losses from the packaged board

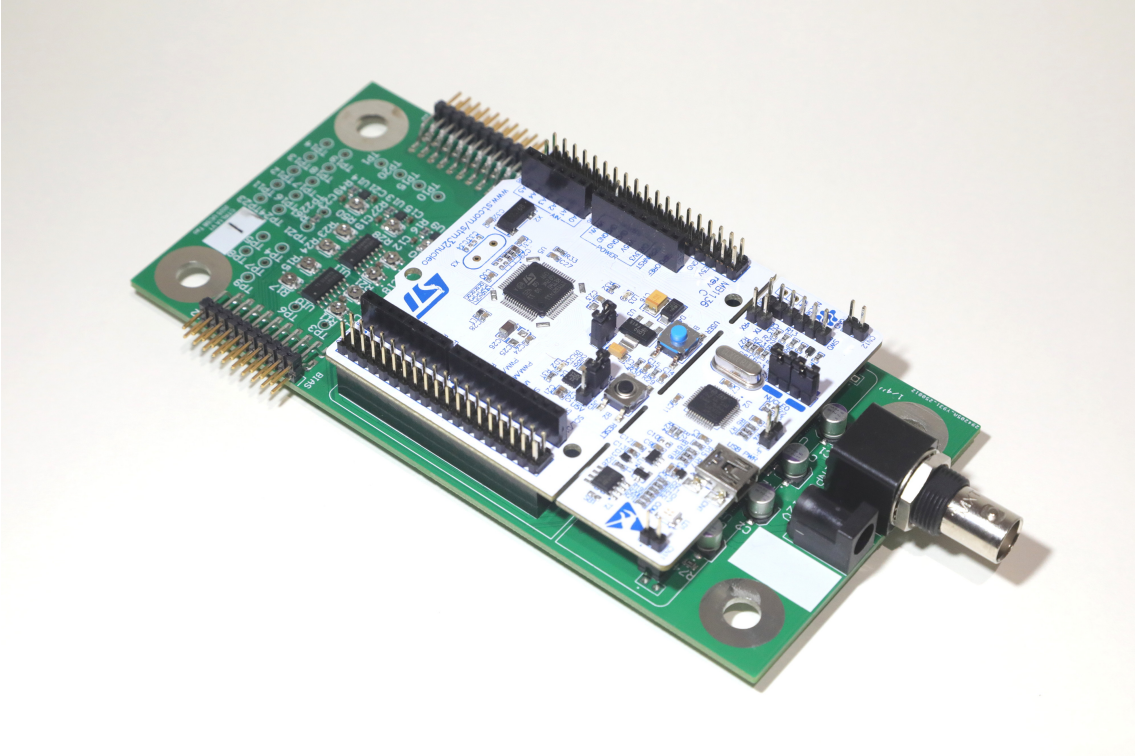


Figure 6.23: Receiver module controller to supply power and receiver configuration by computer control through USB connectivity.

and cables were measured and de-embedded from the measurements. For small signal measurements, a delivered RF power of under -45 dBm was used. Fig. 6.24 demonstrates the ability of the receiver's LO automatic gain control system to hold performance across LO power variation, with a gain tuning range of about 20 dB. A lower control voltage corresponds with a higher LO power setting delivered to the downconverter. The minimum supplied LO power to demonstrate performance across its tuning range with suppression of input LO power variations is 2 dBm. Fig. 6.25 illustrates the receiver's ability to reliably change its performance while maintaining bandwidth through LO gain control, with its maximum gain at 27.2 dB at 137 GHz with maximum LO power setting. The ability of the LO power setting to affect compression is illustrated in Fig. 6.26. Since, the gain not only decreases but also increases with large input power, Pi1dB compression

results, shown in Fig 6.27, are treated as the power where the gain varies by more than 1 dB from its small signal value. The receiver channel demonstrates a Pi1dB -15.9 dB with a LO power control voltage of 2.2 V and a minimum of -24.5 dB at 2.9 V.

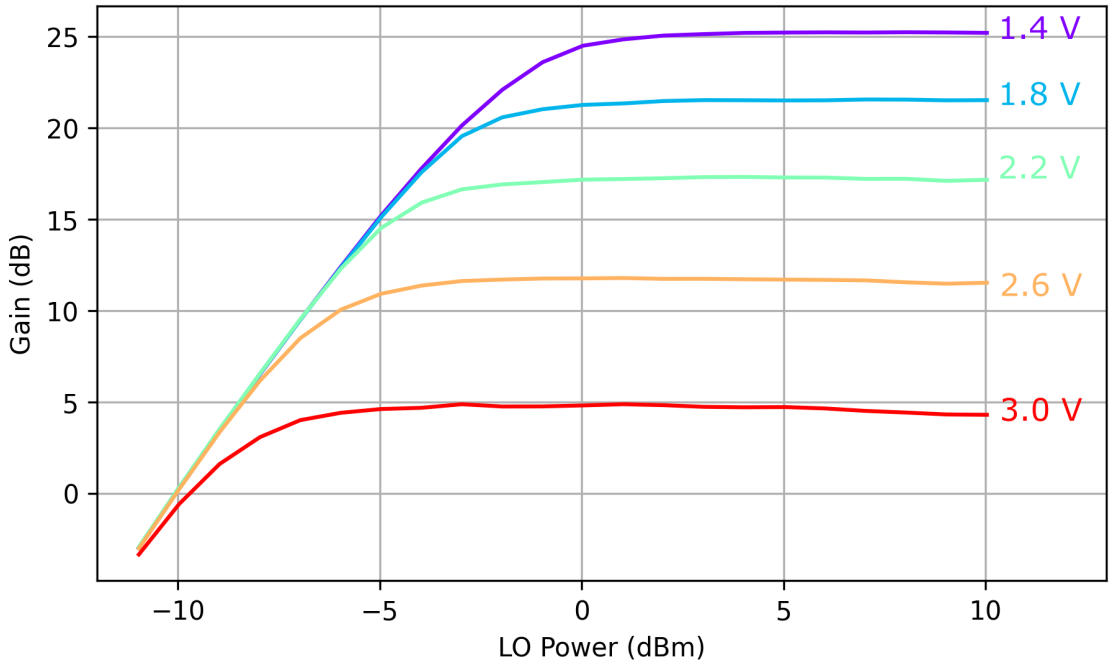


Figure 6.24: Measured receiver channel conversion gain at 135 GHz across delivered LO powers at 35 GHz (effectively 140 GHz), varying with LO power setting.

6.6.2 Probed Receiver Phase Control

To characterize the receiver chip's phase control, the spectrum analyzer in the setup for measuring probed gain and power was substituted with an oscilloscope. Relative phase shift of the downconverted signal was measured in the time domain between two different channels in the receiver array by varying one channel's LO phase setting while keeping the other constant. As shown in Fig. 6.28, the LO control system demonstrates the ability to shift more than 360°, separately from setting gain. Although the phase shifter is not capable of 360° of tuning range at the supplied LO frequency, the subharmonic

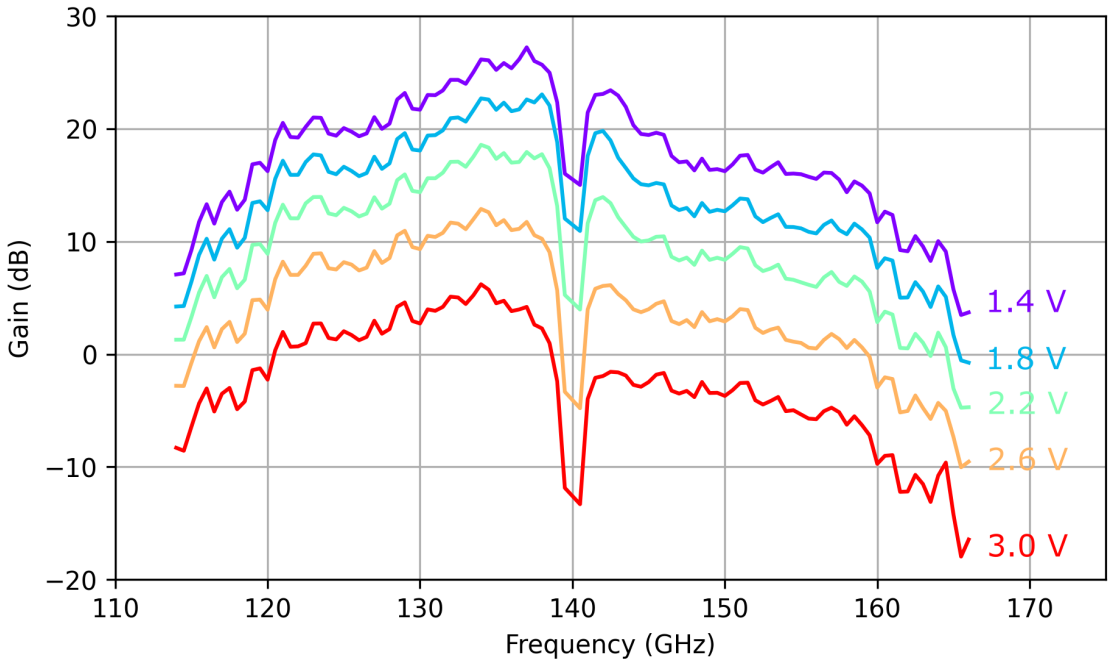


Figure 6.25: Measured receiver channel conversion gain across frequency with 140 GHz LO at 2.0 dBm, varying with LO power setting

mixer multiplies that tuning range by a factor of four, allowing full phase coverage.

6.6.3 Probed Receiver Noise Measurement

Dual sideband noise measurements on the receiver chip were made using an Eravant STZ-06-IT2 WR-06 hot-cold noise source, with a nominal ENR of 15 dB, through the Y-factor technique. The losses from the packaged board, cables, and RF probe were measured and de-embedded from the noise measurements. A low frequency LNA with a spectrum analyzer was used to measure the noise, and their noise contribution was calibrated with a low frequency noise source. For a single frequency, Fig. 6.29 demonstrates that this dynamic control of LO power and noise figure leading to a receiver power tradeoff. This is the key feature that allows the receiver to adapts its power consumption to the sensing environment it is used in. The measured noise figure is that of a single

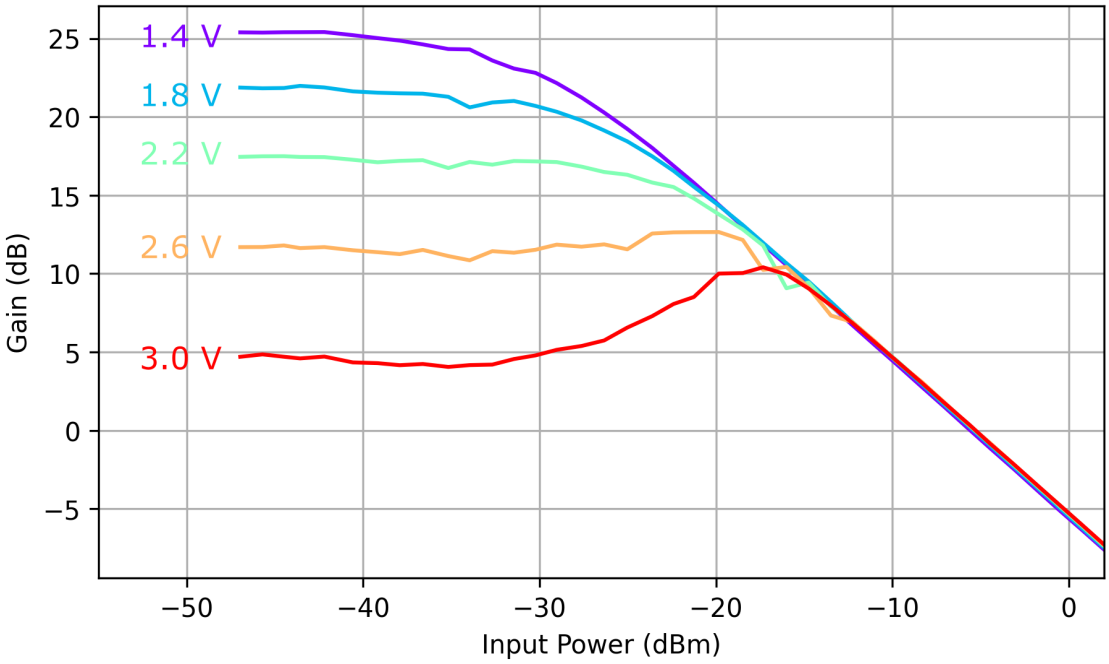


Figure 6.26: Measured receiver channel conversion gain vs. RF input power at 145 GHz RF and 140 GHz LO, varying with LO power setting.

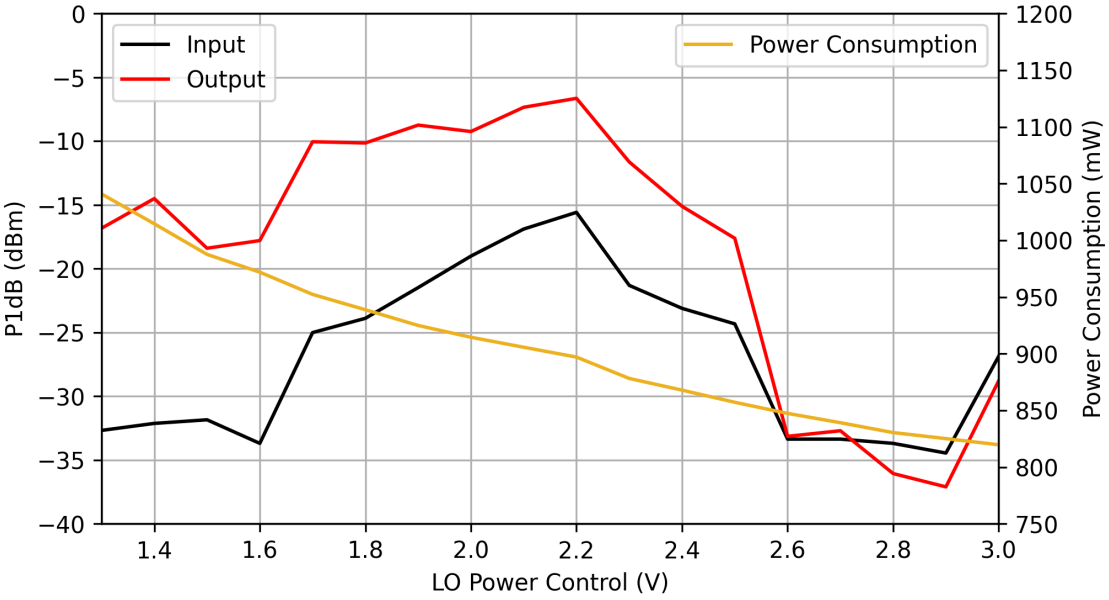


Figure 6.27: Measured receiver channel input and output 1 dB power compression at 135 GHz RF and 35 GHz LO input, varying with LO power setting

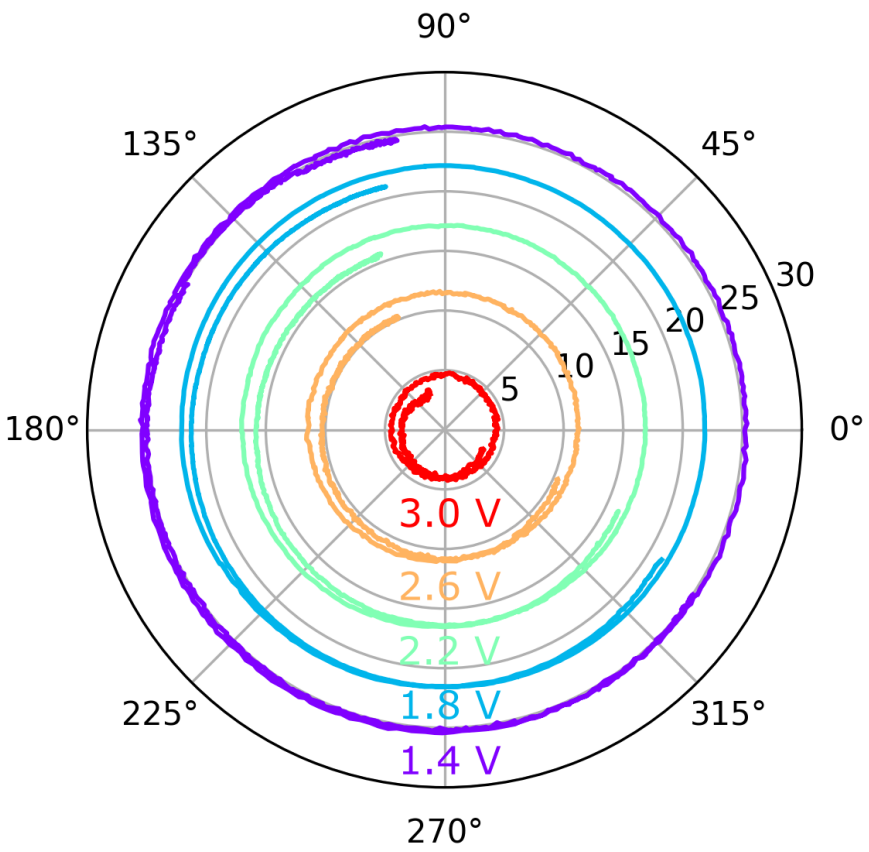


Figure 6.28: Measured receiver chip conversion gain in dB and relative phase shift at 135 GHz with LO at 35 GHz (effectively 140 GHz), varying LO phase setting for each power setting.

channel in the array, while the power consumption is the total of all channels with the same LO control settings as the single channel. An upward shift in the control voltage is observed, which is likely due to how the voltage is linearized with a current mirror with mismatch combined with the power control op-amp's input offset voltage. The receiver channel achieves a minimum noise figure of 17.2 dB with a LO power control voltage of 1.3 V, while consuming 1042 mW. With a control voltage of 2.9 V, the channel achieves a noise figure of 30.4 dB, consuming 819 mW of power. This demonstrates the channel's ability to trade off 13.2 dB of noise figure to reduce power consumption by 223 mW across the array. Fig. 6.30 shows noise across frequency, demonstrating the receiver's ability

to use the LO control system to dynamically change the receiver's noise figure across its bandwidth. Since the control relationship is shifted up by 0.4 V, the simulation is shown with that offset for comparison.

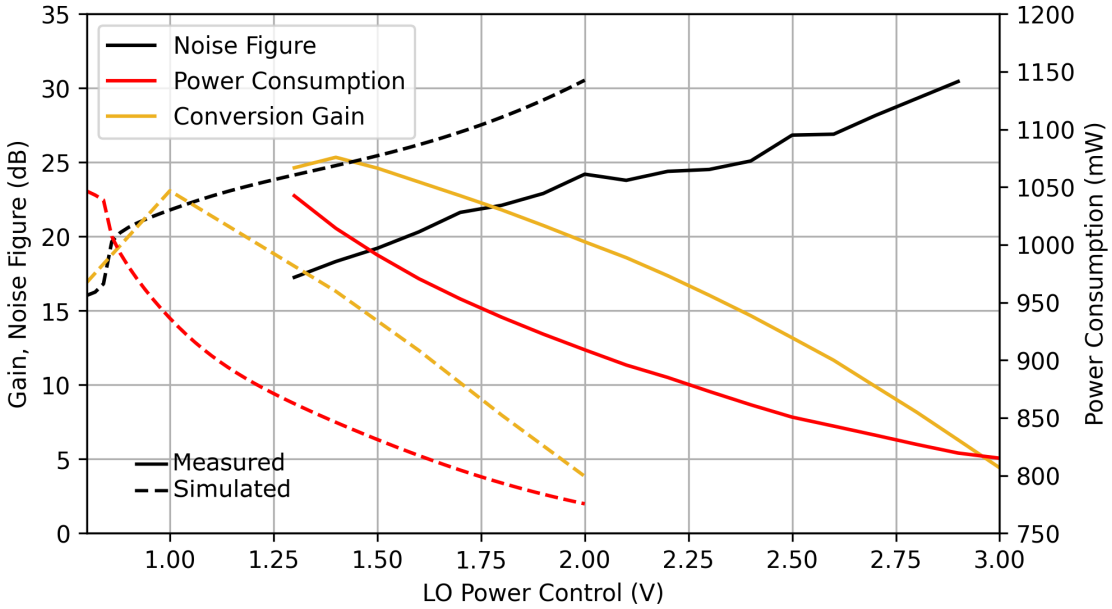


Figure 6.29: Measured receiver channel noise figure, conversion gain, and power consumption tradeoffs through LO power setting at 135 GHz RF and 35 GHz LO input.

6.7 Over-the-air Array Measurement Results

For over-the-air measurements, the receiver array module with antenna assembly was mounted on an electronically controlled gimbal with an instrumentation transmitter on a static pedestal in an anechoic chamber. All over-the-air measurements were made with the protective PTFE shield removed. The receiver array was first calibrated using the receiver calibration path, and then the results are measured with IF combining and image rejection with a quadrature hybrid, as shown in Fig. 6.32.

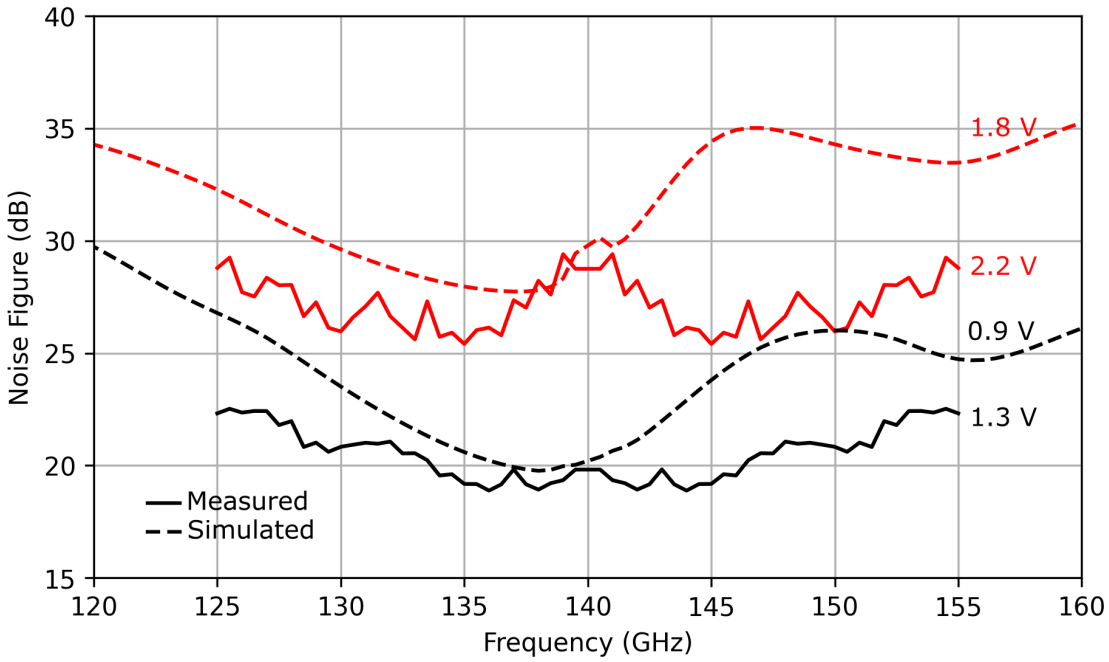


Figure 6.30: Measured receiver channel noise figure at a 35 GHz LO input across LO power control settings. Measured dual sideband noise results are mirrored across the effective LO frequency, and the control voltage of the simulation is shifted down by 0.4 V.

6.7.1 Receiver Array Channel Calibration for Beamforming and Image Rejection Optimization

Full array gain and phase calibration of the receiver module was performed over-the-air, as illustrated in Fig. 6.32, to map LO power and phase settings to receiver element gain and relative phase shift through software. The calibration controller software is implemented on a computer connected to the receiver control module. For every horizontal angle that the receiver module may electronically steer to, the array is calibrated to match channel gain and phase for a single transmitted frequency. The LO power and phase control system does not have perfectly orthogonal polar coordinate control, and there is channel-to-channel variation in the receiver chip, which are detriments that this calibration process suppresses. First, the gimbal turns the receiver module to face

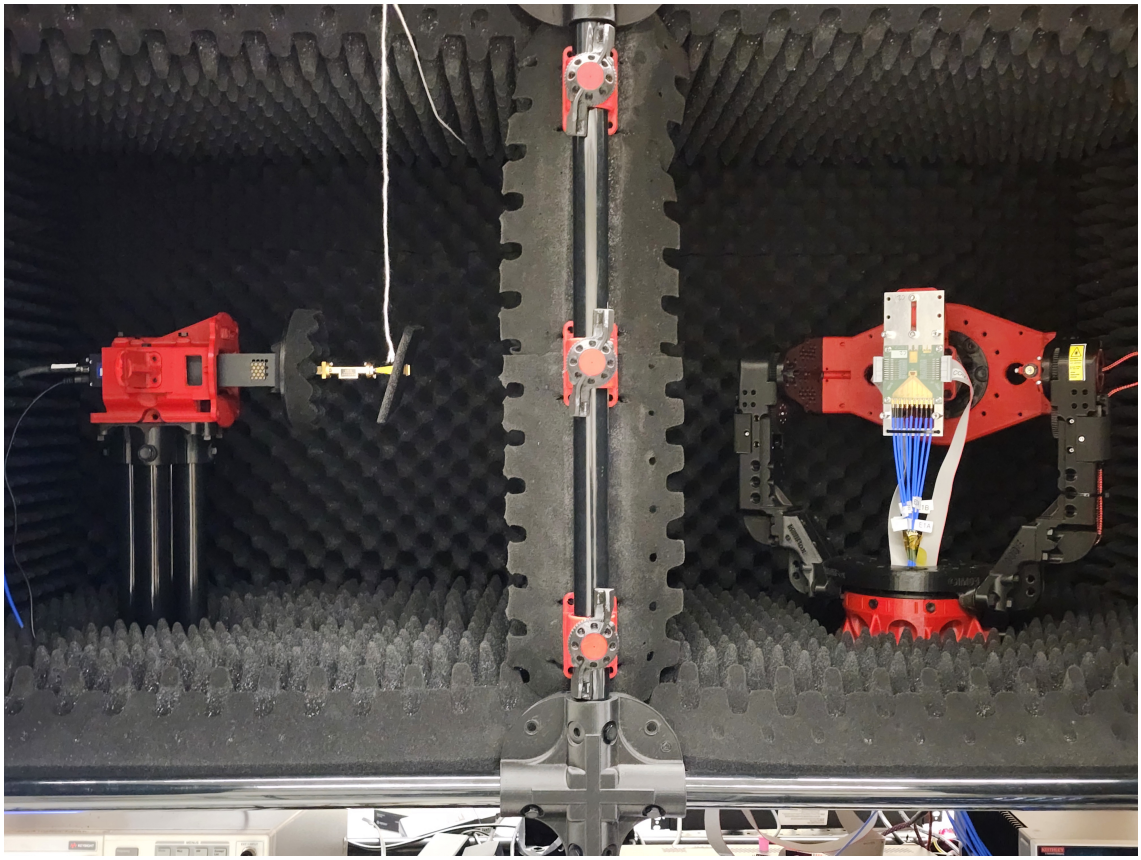


Figure 6.31: Over-the-air array module calibration and measurement setup within an anechoic chamber.

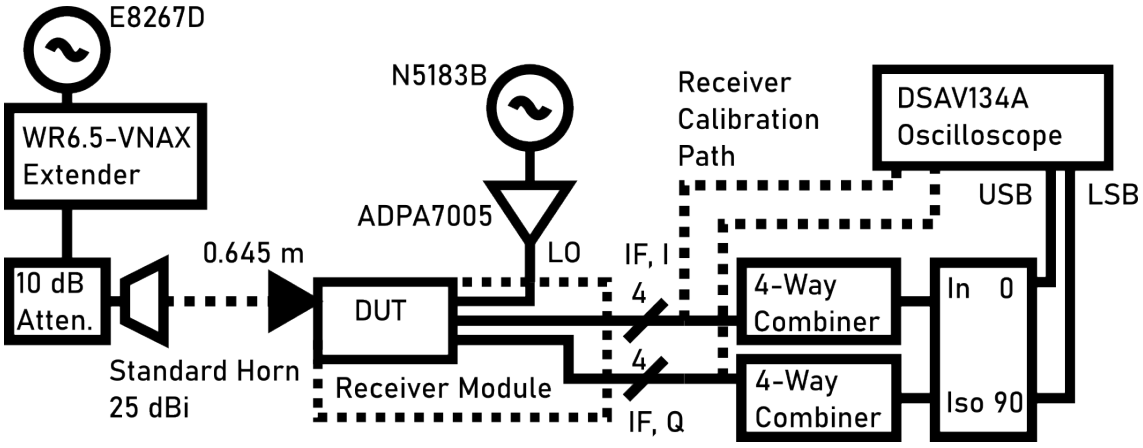


Figure 6.32: Measurement setup within an anechoic chamber.

the transmitter at the calibrating angle. The first element was set to a reference LO power and phase setting, and then LO power settings V_{PnI} and phase settings $V_{\phi nI}$ were

determined for every nth element's I channel to simultaneously match their measured gains and phases through PID control loops, shown in Fig 6.33a. This calibration was performed for each beam angle to be formed and for each LO power setting. Since the receiver module is physically rotated opposite of the beam steering direction, the target phase $\Delta\phi$ is 0°.

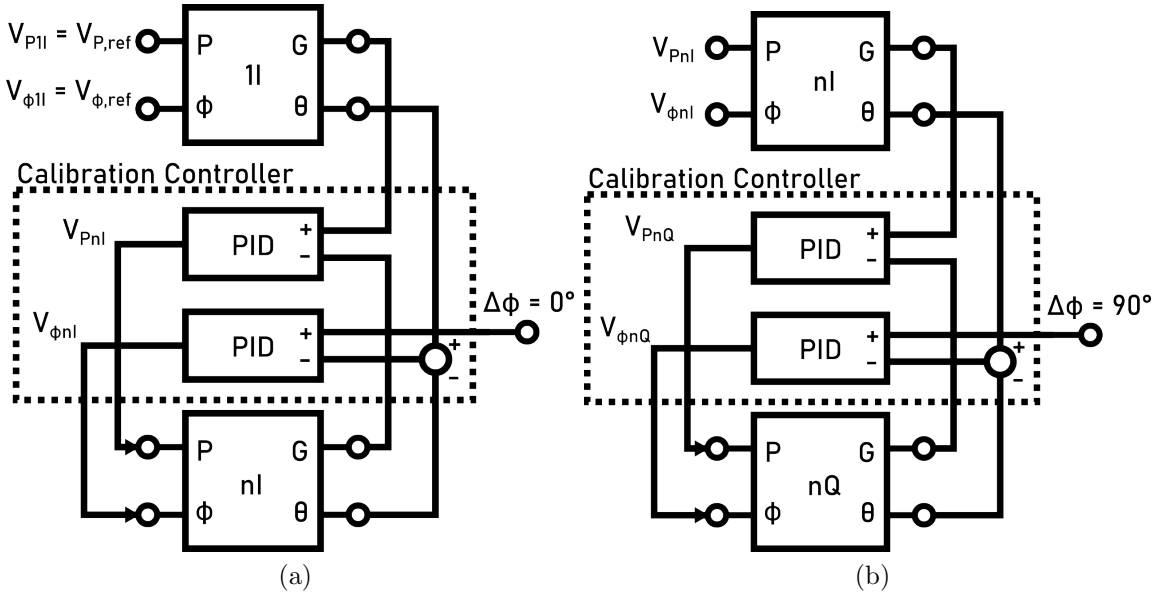


Figure 6.33: Channel calibration loops for (a) all I channels in n elements and (b) each I and Q channel pair within n elements.

In a second step, each element's I channel is set to the previously found V_{PnI} and $V_{\phi nI}$ that corresponds to a receiver configuration. Then, the element's Q channel LO power and phase settings were determined such that it matched the gain and presented a quadrature phase shift relative to the I channel in their respective elements, illustrated in Fig. 6.33b. Since the calibration is performed at a single RF frequency, the calibration has the ability to optimize for either the upper or lower sideband at the expense of the other, as Fig. 6.34 shows. The optimization at 135 GHz yields a combined multi-element IRR of 26.4 dB, while the optimization at 145 GHz yields 26.0 dB. The calibration is saved in a codebook with parameters of beam angle, target LO power setting, and optimized

IRR frequency.

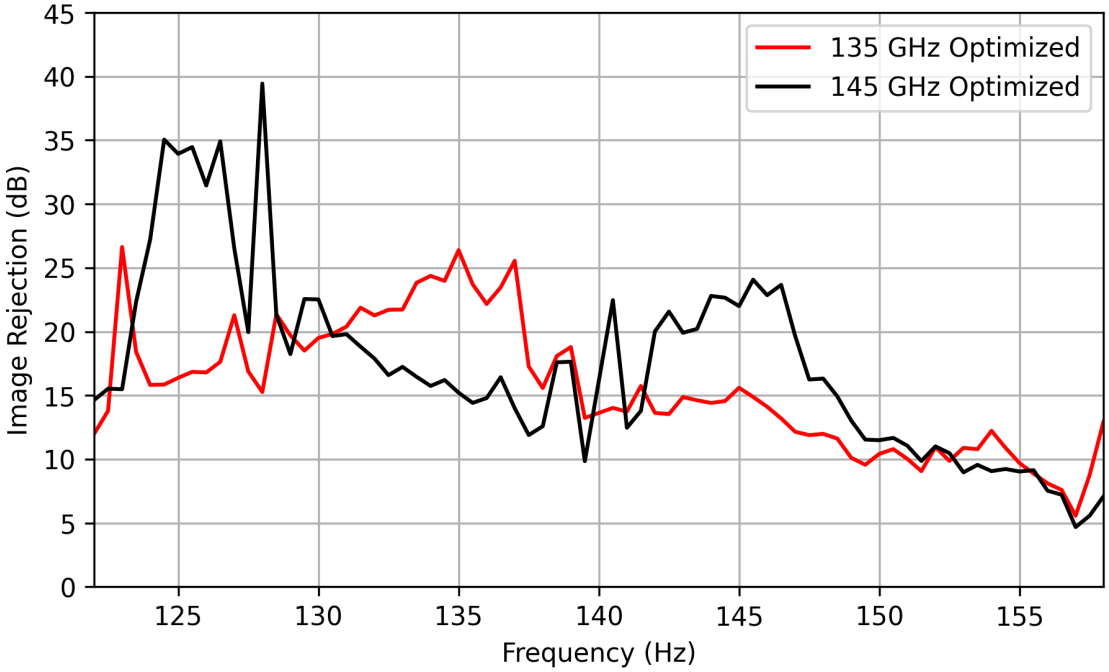


Figure 6.34: Image rejection results for optimizing at 135 GHz (lower sideband) and at 145 GHz (upper sideband) on a 0° formed beam with a 35 GHz LO input and maximum array-calibrated LO power setting.

In addition to image rejection optimization, the calibration process also produces LO control settings to form beams at different angles. Beam patterns were measured by sweeping the receiver's gimbal rotation horizontally for each LO control setting. The gain is measured after image rejection, and the losses of the package board, 4-way combiner, and quadrature hybrid are removed. The results of the beam patterns are shown in Fig. 6.35.

6.7.2 Inferred Antenna Gain

Because the gain of the receiver is known, the gain of the antenna chip with package interconnect can be inferred without interference of a nearby probe. An over-the-air measurement was performed to determine the gain of a single channel across bandwidth.

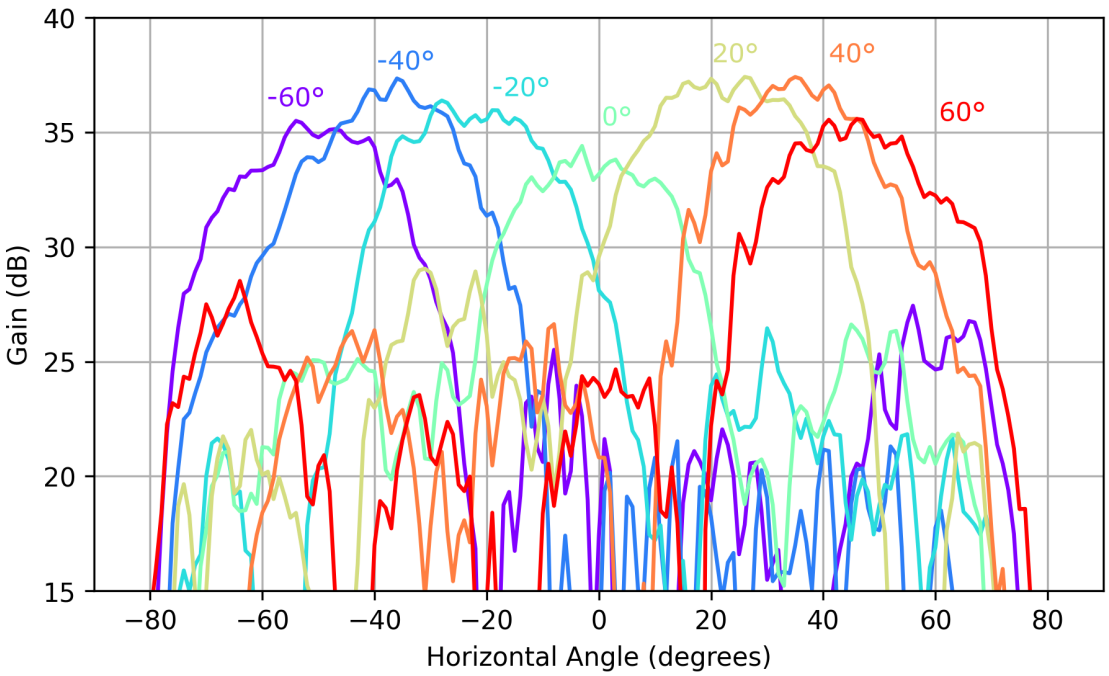


Figure 6.35: Measured array beam patterns of maximum power settings at 135 GHz as receiver module conversion gain, with a 35 GHz LO input.

Then, the gain of that channel from the probed receiver measurement, for the same LO power and phase setting, was subtracted from those results to obtain an inferred antenna gain within the package. For this measurement, the oscilloscope was replaced with a spectrum analyzer for a larger measurement bandwidth and the IF combining with quadrature hybrid is removed. Fig. 6.36 shows that the reduction in gain from the measurement of Fig. 6.19 at 147 GHz is not present when the antenna is packaged in the module with bond wires.

6.8 Over-the-air FMCW Measurement Results

The receiver's ranging performance with FMCW radar signals was carried out with the setup shown in Fig. 6.37. The instrumentation transmitter is built using an Eravant SFB-06-E2 mixer, an Eravant SWF-14428340-06-B1 bandpass filter (125 GHz - 150 GHz),

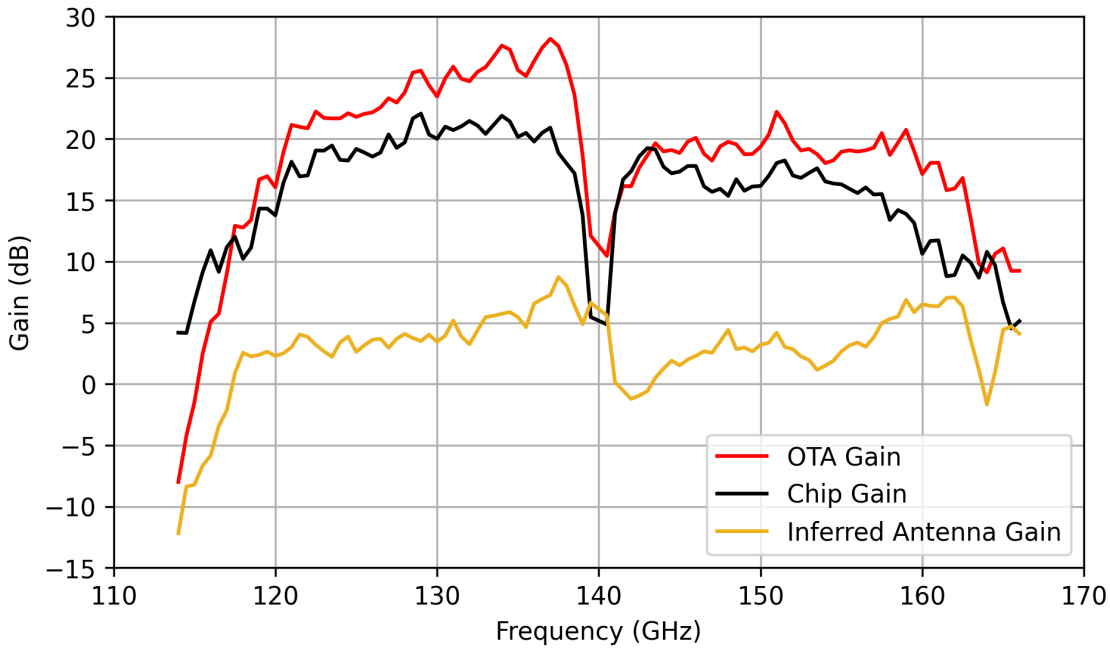


Figure 6.36: Inferred antenna gain with over-the-air measurement at 0°.

an Eravant SBP-1141543010-0606-E1 amplifier, a VDI 130AMP amplifier, and a 25 dBi standard horn antenna. The LO for the transmitter is provided through a multiplier chain with an Eravant SFA-553903616-12SF-E1 E-band X6 multiplier and an Eravant SFP-06212-S1-M D-band X2 multiplier. An input of 13.0833 GHz was used to produce an effective upconversion LO of 157 GHz, and the bandpass filter in the RF chain is used to reject the LO feedthrough and image of the upconversion. An arbitrary waveform generator (AWG) is used to generate the FMCW signal to the upconversion mixer and a reference FMCW signal that is split through a quadrature hybrid coupler for demodulation in the oscilloscope. The quadrature FMCW reference signal for demodulation is delivered to the oscilloscope without a frequency offset. The receive system consists of the receiver module with its IF outputs combined and then delivered to the oscilloscope where demodulation is digitally implemented, forming a Weaver receiver architecture with image rejection.

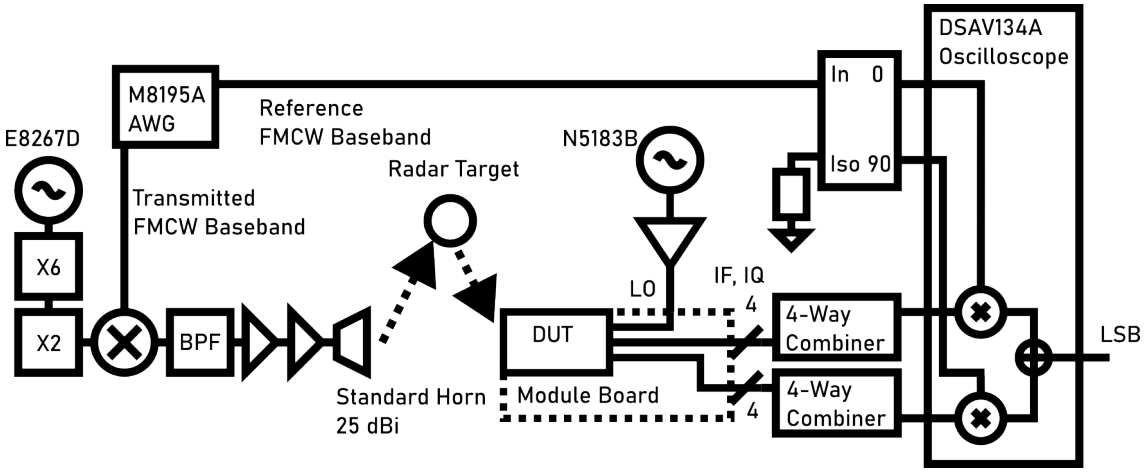
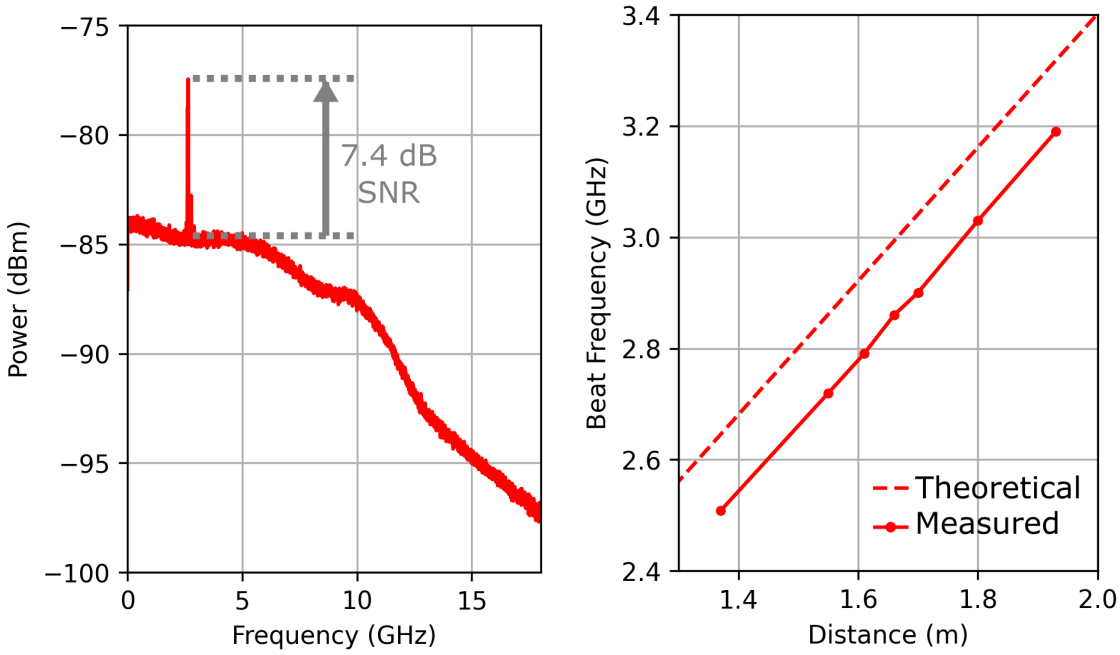


Figure 6.37: Electrical setup for FMCW ranging and SNR measurement

The FMCW signal used is a linear ramp of 18 GHz, with a chirp time of 100 ns. Due to the upconversion architecture, the transmitted FMCW baseband signal is offset by 18 GHz to place the upconverted signal into the lower side band of the receiver, from 121 GHz to 139 GHz. The measured average output power of the transmitter chain in this band, before its antenna, is 12.3 dBm. For the ranging experiments, a total dwell time of 500 ns is used, which captures 5 chirps. The downconversion of this signal by the receiver module is followed by digital demodulation in the oscilloscope with the reference FMCW signal. Fig. 6.38a shows an example of the final detected signal and noise floor spectrum from this system on a target. Fig. 6.38b shows that the beat frequency successfully corresponds to distance variation with an offset of 135 MHz, representing the system delay between the FMCW signal and reference along with a physically offset transmitter.

For ranging experiments, the receiver module on its gimbal was pointed out of an open anechoic chamber, so that the ranging could be performed across a room, shown in Fig. 6.39. The instrumentation transmitter is mounted with the receiver on its gimbal, 10 cm away from the receiver antenna. A radar target was constructed using a 30 cm



(a) (b)

Figure 6.38: (a) Measured demodulated spectrum for a spherical target at 1.47 m with beam steering on 0° and maximum LO power setting, indicating the target's location as a frequency. (b) Measured ranging beat frequency, with the theoretical beat frequency including the 1 GHz offset from upconversion.

diameter foam hemisphere wrapped in aluminum foil to approximate an ideal spherical reflector with a maximum radar cross section of -11.5 dB, following from $\sigma = \pi r^2$ where the range and size of the target is much larger than the transmitted signal's wavelength [41]. A spherical reflector was chosen to minimize radar cross section variation by the target's rotation. Distance between the receiver module and target was measured with a laser telemeter.

First, the SNR of radar target detection was measured for a single target distance across LO control power settings for two different beam angles. The results, shown in Fig. 6.41, demonstrate the receiver's ability to tradeoff SNR to power consumption simultaneously with its ability to form and steer a beam. Best fit lines in Fig. 6.41

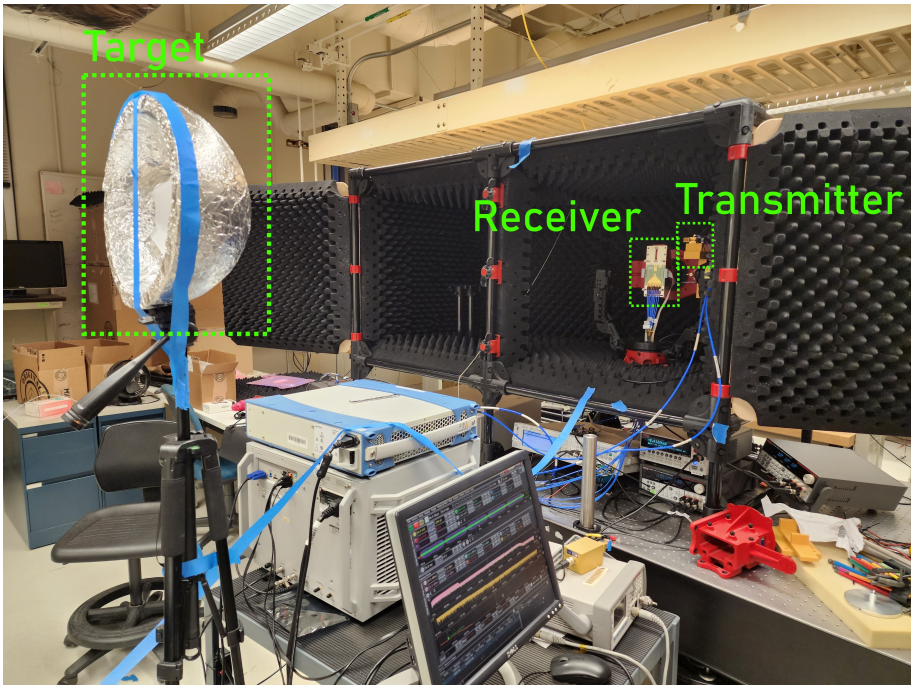


Figure 6.39: Target setup for FMCW ranging and SNR measurement.

illustrate a metric of efficiency that quantifies the power consumption cost needed to achieve an improvement in SNR. With a 0° beam, the receiver achieves a tradeoff is 0.0244 dB mW^{-1}, while with the 40° beam the tradeoff is 0.0210 dB mW^{-1}. Additionally, the fit line at 0 dB of SNR represents the receiver's minimum required power to detect the target for a given distance. The minimum power for the target at 1.47 m with a 0° beam is 654 mW, while the minimum power for the target at 1.97 m with a 40° beam is 622 mW. The lower power needed to detect a target at 40° is consistent with the higher performance of the receiver at that beam angle, as shown in Fig. 6.35.

Second, an experiment was carried out to demonstrate the receiver's adaptation with the dynamic LO control. The target was moved to a distance away from the receiver for each LO power setting, such that the receiver detects the target with 5 dB of SNR. The results in Fig. 6.42 show the power consumption cost needed to detect the target at a certain distance with a constant SNR and demonstrates the ability of the receiver

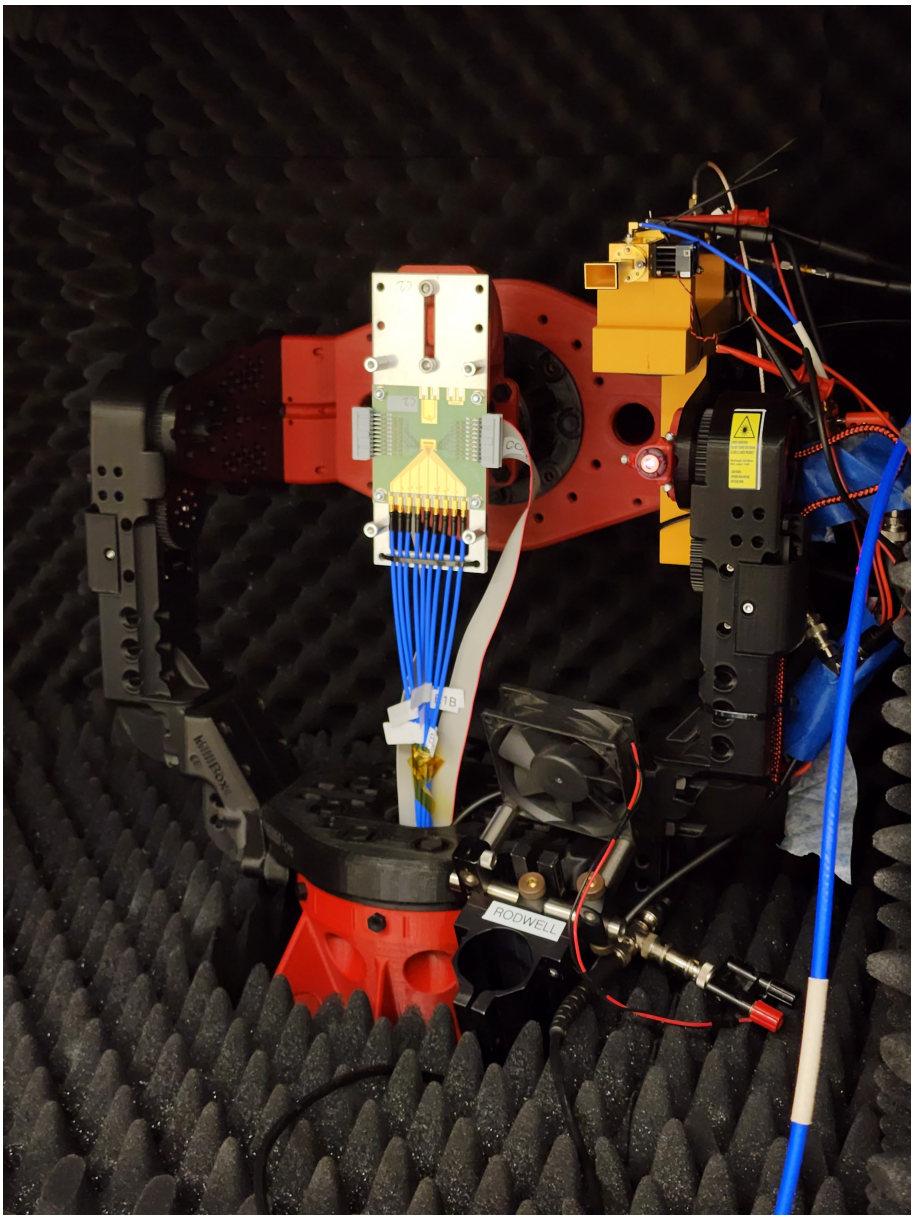
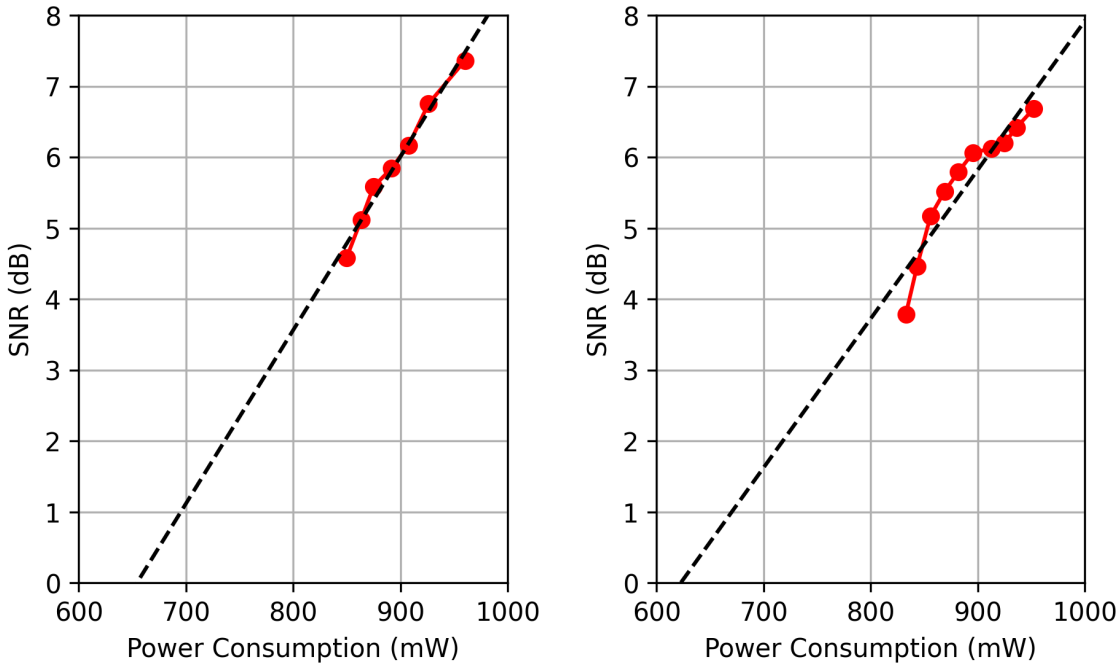


Figure 6.40: Instrument transmitter with receiver module for FMCW ranging and SNR measurement.



(a) (b)

Figure 6.41: Measured SNR to power consumption tradeoff for a spherical target with beam steering on (a) 0° at 1.47 m with 0.0244 dB mW^{-1} of SNR trade-off and on (b) 40° at 1.97 m with 0.0210 dB mW^{-1} of SNR tradeoff.

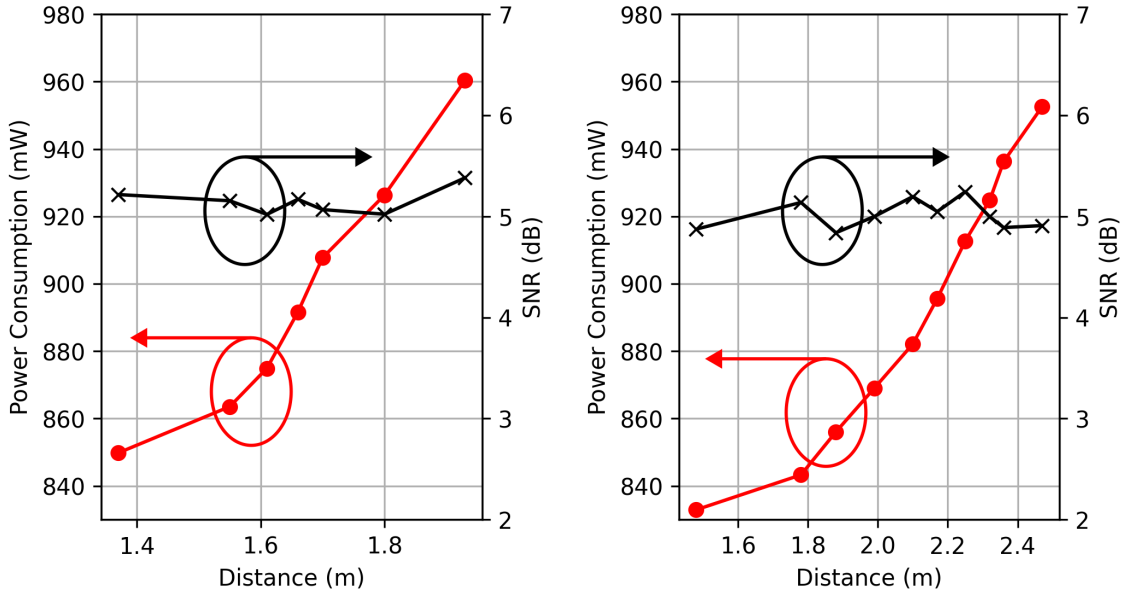


Figure 6.42: Measured power consumption to maintain 5 dB of SNR for spherical target detection across distances for (a) 0° and (b) 40° of array beam steering.

module to perform adaptation for a target SNR simultaneously with beamforming. For example with a 0° beam while maintaining a 5 dB SNR, the receiver needs 960 mW to detect a target at 1.93 m but only 850 mW to detect the target at 1.36 m, saving power in sensing conditions where the target is closer.

6.9 Conclusion

A D-band adaptive receiver array is presented with dynamic LO feedback for power adaptation in varying channel conditions with radar. The receiver array circuits implement linearization through feedback to enable LO control to tradeoff performance with power consumption. Simultaneous optimization of this control is simultaneously demonstrated with beamforming, image rejection, and power control. Tradeoffs in performance and power consumption with respect to sensing environment conditions were

Table 6.1: Comparison of D-band Receivers

Reference	**This Work**	[42]	[43]	[44]	[45]	[46]	[47]
Technology	90-nm SiGe	130-nm SiGe	130-nm SiGe	130-nm SiGe	40-nm CMOS	28-nm CMOS	28-nm CMOS
Antenna Type	4x1 Slotted Patch on Glass	4x4 Patch	-	Folded Dipole	4x1 Series Patch	Patch on Organic Interposer	-
Antenna Connection	Bondwire	Coupling Aperture	-	On-chip	Coupling Aperture	Flip-chip	Bondwire
Type	4Rx, IQ	16Tx/16Rx, IQ	3Rx	4Tx/4Rx	8Rx	4RX, IQ	1Tx/1Rx
Frequency (GHz)	140	150	120	120	120	135	150
Receiver Gain (dBi)	37.3	22[§]	-	31[§]	-	-	-
Channel Gain (dB)	27.2	8	12.5	21	53.8	58	108
Channel P_{i1dB} (dBm)	-15.9	-10.4	-4.8	-11	-	-	-5
Channel NF (dB)	17.2	15.6	13	12.7	9.5	7.8	14.5
IRR (dB)	26.4	30	-	-	-	-	-
P_{DC}/Element (mW)	205 - 261[*]	211 [†]	66	433 [‡]	46	98	366 [†]
LO	Mult.	Mult.	Mult.	Mult.	Mult.	PLL + Mult.	PLL + Mult.
LO Mult.	X4	X6	X5	X2	X32	X6	X8
LO Input (dBm)	2	0	0	-	2	-	-
Area (mm^2)	7.881	20.992 [†]	2.07	25 [‡]	8.8	4.8	9.17 [‡]

[*] Adaptive Range [†] TX excluded [‡] TX included [§] Estimated from in-phase antenna gain

demonstrated with an FMCW on a target across distances over the air. In particular, an SNR-to-power tradeoff cost of 0.0244 $\mathrm{dB\,mW^{-1}}$ is demonstrated. The adaptation shows that bias feedback circuit concepts combined with LO control is suitable for applications of joint radar and radio systems in highly dynamic environments.

Chapter 7

Conclusions and Future Work

This dissertation presents circuits, techniques, and systems for building millimeter-wave phased arrays in dynamic environments. First, a novel bias feedback adaptation circuit technique for frequency doublers is presented, demonstrated with a G-band doubler circuit in 90-nm SiGe BiCMOS technology. This technique enables linearized dynamic reduction of power in frequency multipliers, which allows for optimized performance and control of its output power. Second, the bias feedback technique is applied to a downconverter design. This is demonstrated with a fourth subharmonic D-band downconverter in 90-nm SiGe BiCMOS technology. The downconverter circuit exploits the fourth harmonic content of a push-pull frequency multiplier to achieve a high multiplication factor without sacrificing additional area, power consumption, or LO power requirement for a cascaded multiplier chain, while demonstrating it ability to trade its performance against power consumption through LO power. Third, a four-stage LNA in 35-nm InP HEMT for heterogenous integration involving noise measure matching is presented. This is followed by the presentation of a four-stage ultra-compact wideband LNA in 90-nm SiGe BiCMOS designed with staggered gain tuning for monolithic integration in a highly scaled arrayed receiver system. Fourth, a 4-element IQ receiver array packaged in a module with

a dual-slot patch antenna array is presented. The receiver array combines the concepts from this work on frequency multipliers, low-noise amplifiers, and downconverters, into a culminating receiver system module that demonstrates system power consumption adaptation to change or maintain SNR in dynamic FMCW sensing conditions. In over-the-air experiments, the module exhibits reconfigurability along a SNR-to-power cost for varying target detection, highly supporting the use of bias feedback adaptation for varying LO power in applications of joint radar and radio systems in dynamic environments.

For future endeavors, the concepts presented in this work for using the LO power to adapt to wireless conditions were primarily presented between 100-200 GHz, but they could be applied to systems higher in frequency where environmental impacts for communications or sensing are even more significant. Additionally, performance of a system with an LO chain implementing bias feedback could be improved with other downconversion architectures and system scaling topologies, leading to a wider range of SNR and thus more power saved. These methods could be demonstrated in communication systems and for transmitters. The research direction towards use of dynamic power consumption in wireless systems to adapt to changing wireless conditions holds promise for implementing systems above 100 GHz in real-world environments, especially where the power budget is limiting.

Appendix A

Frequency Multiplier Bias Feedback

A.1 Rectified Current Cancellation

A schematic of a frequency doubler with output buffer stage and bias feedback is shown in Fig. A.1b. At DC, frequency multiplying transistors Q2A and Q2B can be combined into a single Q2 for analysis, as in Fig. A.1. The derivation for the bias of the doubler, set by the resistors and basic transistor parameters, is shown in Eq. A.1.

$$\begin{aligned} I_{C2} &= \beta_2 I_{B2} \\ I_{C2} &= \beta_2 \frac{(V_1 - V_{BE1}) - V_{BE2}}{R_{FB}} \\ I_{C2} &= \beta_2 \frac{V_1 - 2V_{BE}}{R_{FB}}, V_{BE1} \approx V_{BE2} \\ I_{C2} &= \beta_2 \frac{V_C - (I_{C2}/\beta_1)R_1 - 2V_{BE}}{R_{FB}}, V_1 = V_C - \frac{I_{C2}}{\beta_1} R_1 \\ I_{C2} &= \frac{V_C - 2V_{BE}}{R_{FB}/\beta_2 + R_1/\beta_1} \end{aligned} \tag{A.1}$$

In the case of a frequency multiplier, the current flowing through the transistors is the current coming from the quiescent bias I_Q plus the additional current I_0 injected

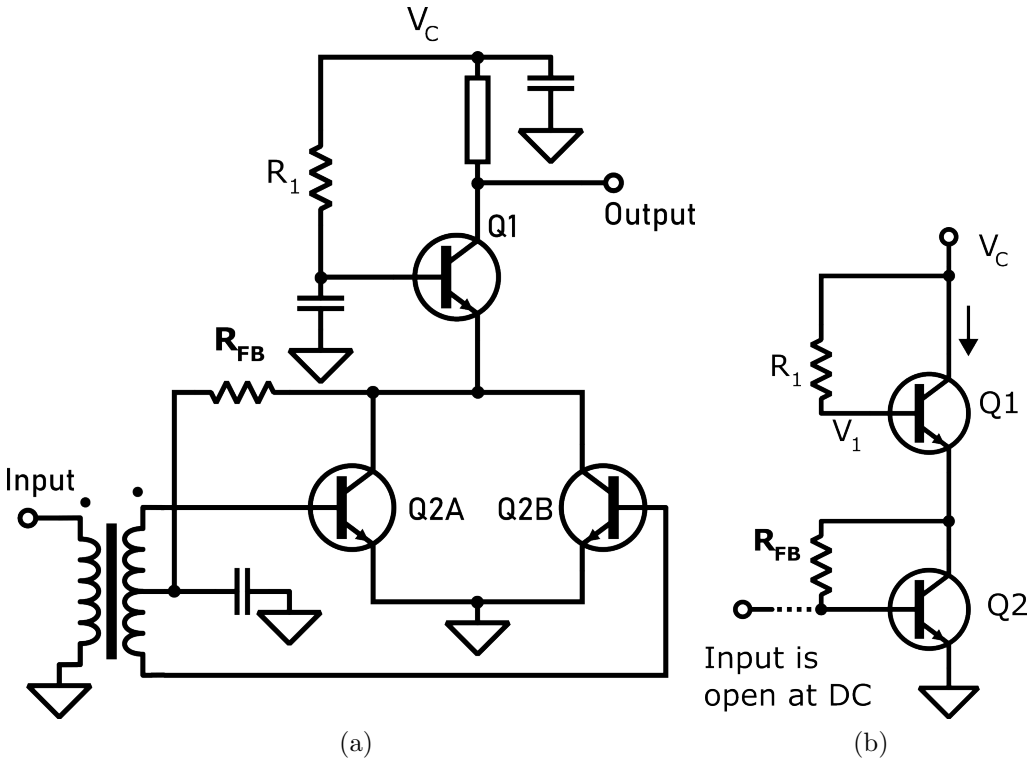


Figure A.1: (a) Frequency doubler schematic with bias feedback, and (b) its DC equivalent circuit.

through the current rectification action of $Q2A$ and $Q2B$, shown in Fig. A.2. The resulting current at the output of the frequency multiplication transistors can be found in the form of a Fourier series of a rectified cosine A.2, where the injected DC current is $I_0 = I_{max}\frac{4t_0}{\pi T}$. Its effect shown in Fig. A.3 as an elevated average current adding to the selected output harmonic amplitude.

$$I_n = I_{max}\frac{4t_0}{\pi T}\begin{cases} 1 & \text{, if } n = 0 \\ 2 \cdot \left|\frac{\cos\left(\frac{n\pi t_0}{T}\right)}{1-\left(\frac{n\pi t_0}{T}\right)^2}\right| & \text{, if } n \text{ even} \\ 0 & \text{, if } n \text{ odd} \end{cases} \tag{A.2}$$

For a bipolar transistor, $V_{BE} = V_T ln(I_C/I_S)$. V_{BE} corresponds to current I_C flowing through the transistor, so detecting V_{BE} is analogous to detecting I_C. When there is

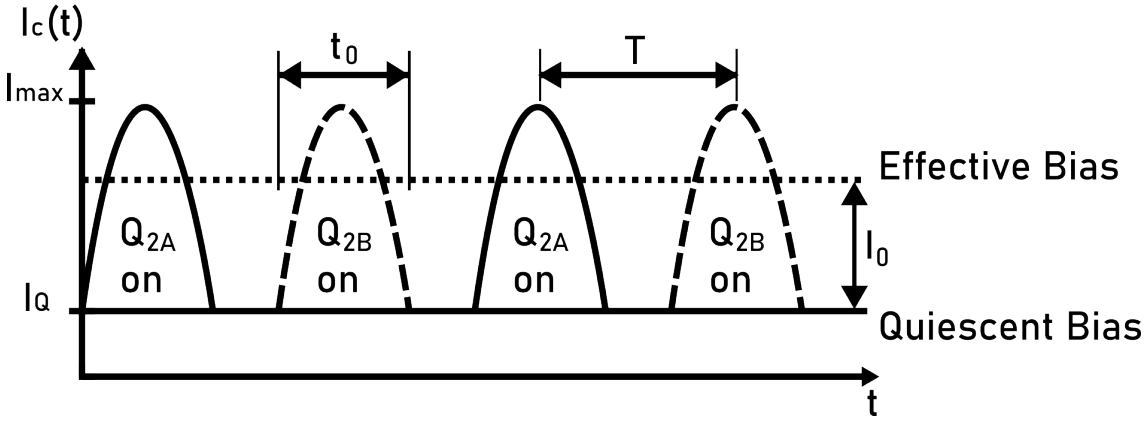


Figure A.2: Effective biases for a frequency multiplier.

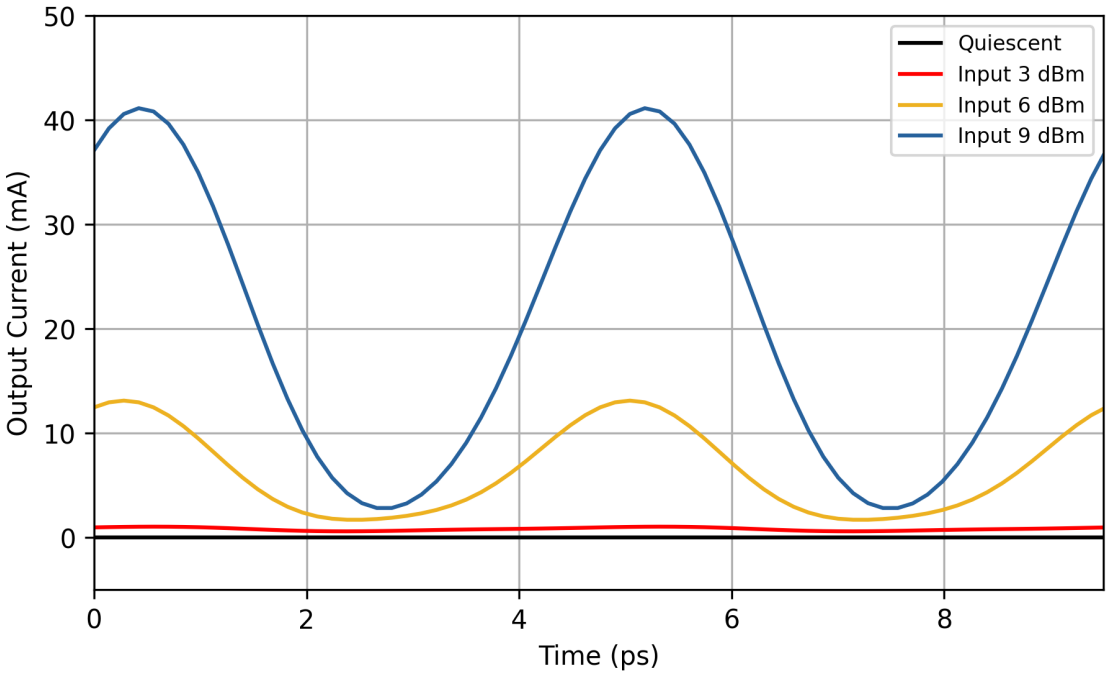


Figure A.3: Simulated time-domain current output of a conventional frequency doubler with no feedback bias after output matching selects for the second harmonic.

more of the injected current from a higher input amplitude, the transistors' V_{BE} rises in response, indicating that the bias current through the transistors is changing and affecting the gain of the frequency multiplier. However, with the feedback bias circuit implemented, it can be observed that an increase in V_{BE} leads to a reduction in the overall bias current, an effect that is negative feedback. This maintains the bias condition of the multiplier, linearizing its gain. The sensitivity of the feedback is

$$\frac{\partial I_{C2}}{\partial V_{BE}} = \frac{-2}{R_{FB}/\beta_2 + R_1/\beta_1} = G_{FB} \tag{A.3}$$

This sensitivity is essentially a negative transconductance in parallel to the typical transconductance of transistors. To cancel the injected current I_0, this transconductance from feedback should be equal the effective transconductance of converting an input sinusoid voltage to a DC current component of a rectified sinusoid, as follows.

$$\begin{aligned} 0 &= G_{FB} + \frac{4t_0}{\pi T} G_m \\ \frac{2}{R_{FB}/\beta_2 + R_1/\beta_1} &= \frac{4t_0}{\pi T} G_m \end{aligned} \tag{A.4}$$

Eq. A.4 shows the condition of perfect cancelation of the injected current from the rectification action of $Q2A$ and $Q2B$, where G_m is their large signal transconductance. The resulting effect of maintaining bias conditions is shown in Fig. A.4.

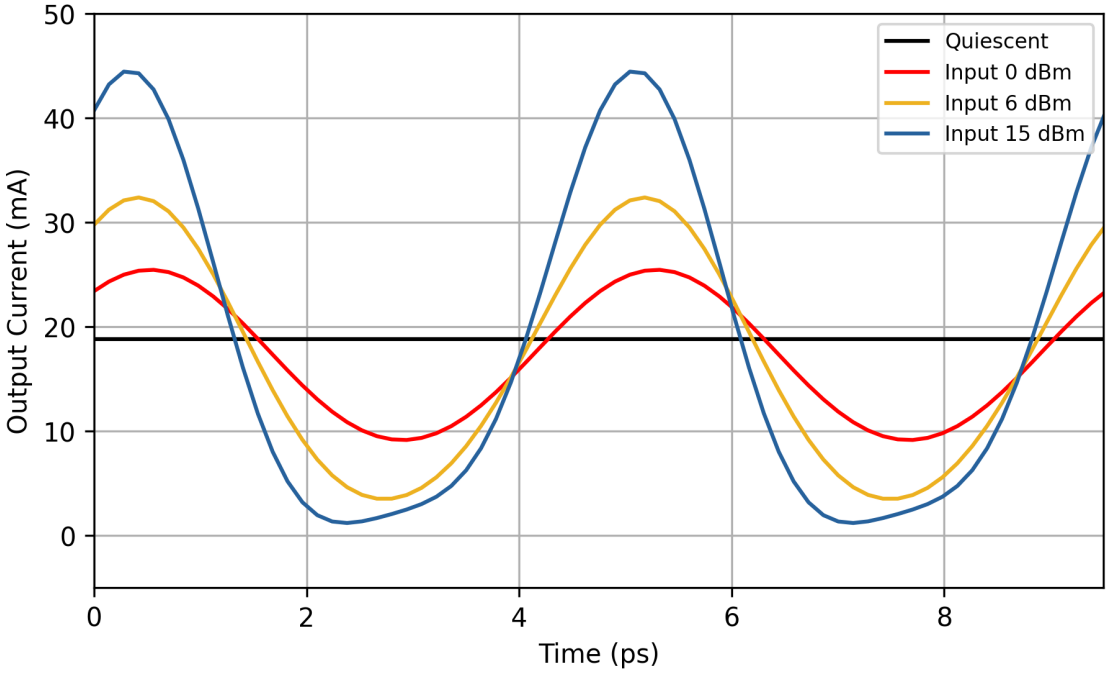


Figure A.4: Simulated time-domain current output of a frequency doubler implementing optimal feedback bias after output matching selects for the second harmonic. Note that the output current at low input amplitude substantially increases compared to Fig. A.3 due to the transistors working at a more optimal bias.

A.2 Independent Feedback Bias Design

By decreasing the size of $R1$, the V_{BE} contribution of the top buffer transistor can increase sensitivity of the feedback by up to a factor of 2, but the overall quiescent current would also change. If R_1 is connected to a voltage V_1 instead of V_C for biasing $Q1$ or entirely removed, as in Fig. A.5, the negative feedback effect can be set independently of quiescent bias current of the entire circuit using V_1, exemplified in Eq. A.5.

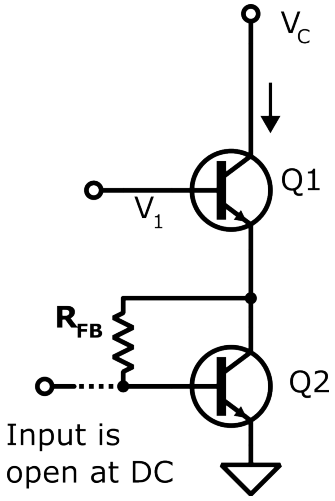


Figure A.5: DC equivalent circuit of frequency multiplier for independent feedback bias design.

$$\begin{aligned} I_{C2} &= \beta_2 I_{B2} \\ I_{C2} &= \beta_2 \frac{(V_1 - V_{BE1}) - V_{BE2}}{R_{FB}} \\ I_{C2} &= \beta_2 \frac{V_1 - 2V_{BE}}{R_{FB}}, V_{BE1} \approx V_{BE2} \\ \frac{\partial I_{C2}}{\partial V_{BE}} &= \beta_2 \frac{-2}{R_{FB}} \end{aligned} \tag{A.5}$$

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