Title
Hurwitz Interconnect Delay Evaluation - HIDE: User's Manual

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User's Manual

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Introduction

This manual describes how to use HIDE as an efficient RC Interconnect Delay Evaluation software. The program features:

- Delay evaluation for any user-defined delay threshold;
- Rise time evaluation between any start and end delay thresholds;
- Waveform evaluation for user-defined test node(s);
- Equivalent load generation for gate delay evaluation;
- Hspice netlist generation for verification;
- Moment generation.

These features will be introduced in detail in the part "Input Command Format" below.

Supported Input Signals

Three types of input signals are supported in the program: exponential, ramp, and step functions. Users can specify the input signal type and the corresponding control parameters in input command files.

- Exponential function:

$$V(t) = \left(1 - e^{-\frac{t}{tr}}\right)U(t) \qquad t \geq 0 \qquad (1)$$

- Ramp function:

$$V(t) = \begin{cases} \frac{t}{tr} & 0 \leq t \leq tr \\ 1 & t > tr \end{cases} \qquad (2)$$

- Step function:

$$V(t) = 1 \qquad t \geq 0 \qquad (3)$$

where tr is the input signal rise time, which is an constant defined in the input command file, and $U(t)$ is the unit step function.

Supported Delay Evaluation

For delay evaluation, presently we provide three delay models:
- Elmore delay model;
- D2M delay model;
- HIDE delay model.

The first two are provided for comparisons with our HIDE model. So waveform evaluation, delay metrics for arbitrary delay threshold(0% ~ 100% of V_{DD}), and rise time for arbitrary starting and ending delay threshold (0% ~ 100% of V_{DD}) are provided only for HIDE delay model. As for Elmore delay model and D2M delay model, we only provide delay metrics.

Input Command Format

*keyword are highlighted.

InputFile: < *input file name* >

InputFile specifies a spice or dspf formatted input netlist file. The file should define a circuit case.

OutputFile: < *output file name* >

OutputFile specifies the output file in which all the evaluation results are going to be saved.

InputFileFormat[dspf/spice]: < *dspf* | *spice* >

InputFileFormat defines the input netlist file format. This file is the one specified in **InputFile** entry.

IsGenHspiceNetlist[Yes/No]: < *Yes* | *No* >

IsGenHspiceNetlist tells the program if the input netlist file <*input file name*> needs to be translated into Hspice-formatted input netlist file. This entry should be checked as <*yes*> if you want to compare HIDE with Hspice.

Fspice: <*hspice-formatted input netlist file name*>

Fspice specifies the hspice-formatted input netlist file name. This file is translated from <*input file name*> indicated in **InputFile** entry. **Fspice** should be checked correctly if **IsGenHspiceNetlist** is checked as <*yes*>. But **Fspice** will be ignored if **IsGenHspiceNetlist** is entered as <*No*>.

InputSignalType[exp/ramp/step]: < *exp* | *ramp* | *step* >

InputSignalType defines the input signal type. <*exp*> denotes the input signal as an exponential function, <*ramp*> as a ramp function, and <*step*> as a step function. Presently only these three types are supported.

InputSignalRiseTime: <*tr*>

InputSignalRiseTime is the parameter defined in equation (1) and (2) above.

DelayThreshold[0-1.0]: $< Delay_{th} >$

DelayThreshold defines the delay observation point at which the output signal is $Delay_{th}$ of V_{DD}. It is effective to HIDE delay model only.

IsRiseTime[Yes/No]: *< Yes | No >*

IsRiseTime tells the program if the rise time of the output signal needs to be printed out. It is effective to HIDE delay model only.

RiseTimeStart[0-0.5]: $< Delay_{start} >$

RiseTimeStart defines the starting delay observation point at which the output signal is $Delay_{start}$ of V_{DD}. It is used with **RiseTimeEnd** together. It is effective to HIDE delay model only.

RiseTimeEnd[0.5-1.0]: $< Delay_{end} >$

RiseTimeEnd defines the ending delay observation point at which the output signal is $Delay_{end}$ of V_{DD}. It is used with **RiseTimeStart** together to specify that from where to where on the output signal users are interested in. It is effective to HIDE delay model only.

IsOutputWaveform[Yes/No]: *< Yes | No >*

IsOutputWaveform tells the program if the output waveform needs to be printed out. This entry is optional. It is effective to HIDE delay model only.

BeginWaveFormParameters
Vdd *< power supply voltage >*
tstep *< step size > /*
tstop *< stop time >*
EndWaveFormParameters

This option is optional and will be ignored if **IsOutputWaveform** is checked as *<No>*. The starting time is assumed to be zero.

IsGenMoment[Yes/No]: *< Yes | No >*

IsGenMoment is optional and if it is checked as *<Yes>*, the program will calculate the moments up to the third order and print them out.

IsElmore[Yes/No]: *< Yes | No >*

IsElmore is optional and if it is checked as *<Yes>*, the program will calculate Elmore delay and print it out.

IsD2M[Yes/No]: *< Yes | No >*

IsD2M is optional and if it is checked as *< Yes >*, the program will calculate D2M delay metrics and print it out.

IsDebug[Yes/No]: *< Yes | No >*

IsDebug is optional and only useful for programmers. When it is checked as *< Yes >*, more detailed information will be printed out.

IsOutputAll[Yes/No]: *< Yes | No >*

IsOutputAll is optional and if it is checked as *< Yes >*, all the nodes in the input netlist file will be printed out.

IsUseDefaultTestNode[Yes/No]: *< Yes | No >*

IsUseDefaultTestNode is optional and if it is checked as *< Yes >*, **TestNodeList** entry will be read in and only listed test nodes will be printed out.

TestNodeList:
<Node Name ... ... >
EndTestNodeList

This entry specifies the test nodes users are interested in. If a test node defined by user is not found in the netlist, this node will be skipped and a warming may be printed out. See **IsUseDefaultTestNode** for details.

Bug report

Please feel free to contact Zhanhai Qin via zqin@cs.ucsd.edu or 1-858-534-8174 if you found any bugs in the program or if you want us to improve it.