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UNIVERSITY OF CALIFORNIA  
RIVERSIDE

Electrical Transport in Suspended Two-Dimensional Materials

A Dissertation submitted in partial satisfaction  
of the requirements for the degree of

Doctor of Philosophy

in

Physics

by

Fenglin Wang

March 2015

Dissertation Committee:

Dr. Chun Ning (Jeanie) Lau, Chairperson

Dr. Robert C. Haddon

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The Dissertation of Fenglin Wang is approved:

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Committee Chairperson

University of California, Riverside

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## ABSTRACT OF THE DISSERTATION

Electrical Transport in Suspended Two-Dimensional Materials

by

Fenglin Wang

Doctor of Philosophy, Graduate Program in Physics  
University of California, Riverside, March 2015  
Dr. Chun Ning (Jeanie) Lau, Chairperson

Two-dimensional (2D) materials are ones that are only single to a few atomic layers in thickness, and exhibit novel material properties not found in their three-dimensional counterparts. The research of 2D materials starts to take off after the isolation and transport measurements of graphene in 2004. Graphene has a unique dispersion relation and unprecedented material properties such as extreme mechanical strength, high thermal conductivity, and exceedingly high charge carrier mobility. The first part of this thesis describes the fabrication and transport measurements of suspended twisted bilayer graphene devices.

The second part of this dissertation focuses on 2D molybdenum disulfide ( $\text{MoS}_2$ ), which, unlike graphene, has a band gap. However, its low mobility severely restricted the applications of  $\text{MoS}_2$  and the mechanism for mobility bottleneck is unclear. To investigate the role played by substrates, we fabricate suspended  $\text{MoS}_2$  field effect transistor devices and develop an effective gas annealing technique that significantly improves device quality and increases conductance by 3–4 orders of magnitude. Mobility

of the suspended devices ranges from 0.01 to 46 cm<sup>2</sup>/Vs before annealing, and from 0.5 to 105 cm<sup>2</sup>/Vs after annealing. Temperature dependence measurements reveal two transport mechanisms: electron–phonon scattering at high temperatures and thermal activation over a gate-tunable barrier height at low temperatures. Our results suggest that transport in these devices is not limited by the substrates, but likely by defects, charge impurities and/or Schottky barriers at the metal–MoS<sub>2</sub> interfaces.

Furthermore, we successfully apply ionic liquid for electrolyte gating on suspended MoS<sub>2</sub> transistors and achieve very high coupling efficiency, up to 4.4×10<sup>13</sup> cm<sup>-2</sup>V<sup>-1</sup>. Electrical characterization reveals contact-dominated electrical transport. From the Schottky emission model, the dielectric constant of ionic liquid DEME-TFSI is estimated to be ~11. Comparison between ionic liquid gating of substrate-supported and suspended devices also demonstrates far higher doping efficiency and better screening of charge impurities as well as Schottky barriers.

Recently, the realization of one-dimensional electrical contacts to hexagonal-boron nitride-encapsulated samples points a direction for transport studies of 2D materials. For instance, such MoS<sub>2</sub> devices with graphene contacts have demonstrated unprecedented mobility. Furthermore, heterostructures consisting of various 2D atomic layers may be built to create artificial superlattices, thus enable the exploration of novel phenomena and devices with new functionalities.



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## Chapter 1 Introduction

The field of two-dimensional (2D) materials arguably starts with the seminal work titled “*Electric Field Effect in Atomically Thin Carbon Films*” [1], which was published in *Science* in October 2004. The first two authors, Konstantin Novoselov and Andre Geim, jointly received the 2010 Nobel Prize in Physics for their innovative work on “atomically thin carbon films”, *i.e.* graphene. The field of graphene research took off since 2004 and significant progress has been made in the past decade.

Graphene has many superior material properties, such as high optical transparency, strong mechanical strength, large thermal conductivity, extraordinary mobility and unique energy-momentum dispersion (see more details in Chapter 2). In addition, the true 2D nature of graphene is by itself very interesting. Two dimensional electron gas (2DEG) systems based on semiconductor heterostructures were realized in early 1960s. Due to confinement in the  $z$  direction, the energy levels of electrons are quantized; for sufficiently low charge density, only the lowest level is occupied, hence give rise to a 2D electron gas. Electrons in 2DEG system can have ultra-high mobility, enabling the observation of phenomena such as integer [2] and fractional quantum Hall effect [3]. In comparison, graphene is truly 2D with unique dispersion, giving rise to the unconventional quantum Hall effect [4,5]. It is also a surface 2DEG that can be easily coupled to special electrodes such as superconductors or ferromagnets.

Despite the intensive efforts at graphene research, graphene is not without its drawbacks. One of the biggest challenges is that its gapless spectrum is not suitable for

digital electronics applications. Researchers soon start to explore other two dimensional materials, such as molybdenum disulfide ( $\text{MoS}_2$ ). As a member of transition metal dicalcogenides (TMD), single layer  $\text{MoS}_2$  has a direct band gap, and intensive efforts have been invested in making  $\text{MoS}_2$  FET transistors. However, the low mobility of  $\text{MoS}_2$  devices seriously limits their applications.

In this thesis, I will summarize my work both on graphene and  $\text{MoS}_2$ . Chapter 2 briefly introduces the background of graphene. Chapter 3 describes the details of the fabrication process to make suspended graphene structures. Results from electrical measurements will be presented in Chapter 4. Chapter 5 summarizes the collaborative projects on graphene in which I have ever participated. In the second half of the thesis, Chapter 6 introduces  $\text{MoS}_2$  and elaborates on its differences from graphene. Chapter 7 describes the fabrication of  $\text{MoS}_2$  devices. Chapter 8 and 9 present the data and discussions on gas annealed and ionic liquid gated suspended  $\text{MoS}_2$  devices respectively. Finally, in Chapter 10, I will conclude and briefly describe possible future projects.

- [1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva and A. A. Firsov, *Electric field effect in atomically thin carbon films*, Science **306**, 666 (2004).
  
- [2] K. V. Klitzing, G. Dorda and M. Pepper, *New method for high-accuracy determination of the fine-structure constant based on quantized Hall resistance*, Phys. Rev. Lett. **45**, 494 (1980).
  
- [3] D. C. Tsui, H. L. Stormer and A. C. Gossard, *Two-Dimensional Magnetotransport in the Extreme Quantum Limit*, Phys. Rev. Lett. **48**, 1559 (1982).
  
- [4] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos and A. A. Firsov, *Two-dimensional gas of massless Dirac fermions in graphene*, Nature **438**, 197 (2005).
  
- [5] Y. B. Zhang, Y. W. Tan, H. L. Stormer and P. Kim, *Experimental observation of the quantum Hall effect and Berry's phase in graphene*, Nature **438**, 201 (2005).

## Chapter 2 Band Structure of Graphene

### 2.1 General Introduction of Graphene

Carbon materials, including graphite, intercalated graphite compounds, fullerenes, and the recently discovered carbon nanotubes and graphene, have remained an exciting frontier of materials science for decades [6]. Annual publications on this topic skyrocketed after the isolation of carbon nanotube and graphene [6] (Figure 2.1).

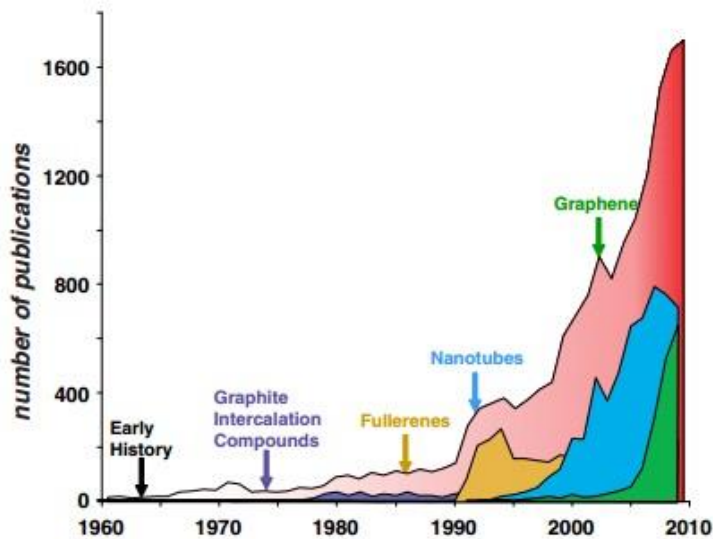


Figure 2.1. Annual publication numbers on carbon material in the last 50 years [6].

Graphene is a monolayer of graphite, and is atomically thin. Tight binding models have been developed for the electronic spectrum of “monolayer graphene” in 1947 [7], though it was considered to be a pure theoretical model system. Certain theories also predict that single layer graphite should be thermodynamically unstable [8,9]. In 1987, the term “graphene” first appeared in Mouras’ work [10]. In 2004, researchers at

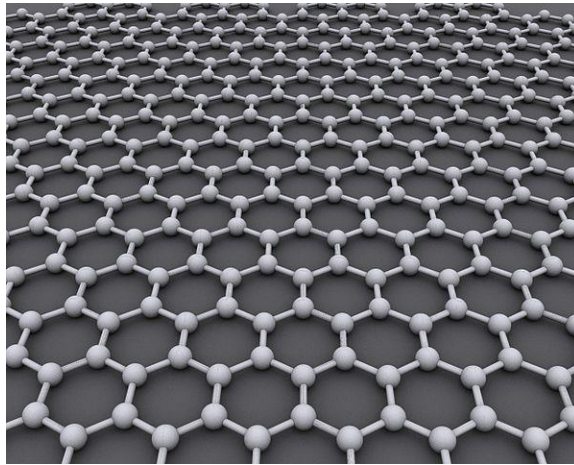
Manchester University (Andre Geim and Konstantin Novoselov) first isolated single layer and few-layer graphene onto dielectric substrate by scotch tape technique [1]. Now the term “graphene” generally refers to single layer, bilayer, trilayer or few-layers of graphite.

Graphene has excellent material properties. For instance, graphene devices on SiO<sub>2</sub> substrates demonstrated high carrier mobility ( $\sim 15,000 \text{ cm}^2/\text{Vs}$  at room temperature) for both electrons and holes, and can sustain very high current density ( $>10^8 \text{ A/cm}^2$ ) [1]. It also has superior thermal conductivity up to  $\sim 5000 \text{ W/mK}$  [11], which outperforms carbon nanotubes [12]. These outstanding thermal properties of graphene provide extra motivation for graphene integration with complementary metal-oxide-semiconductor (CMOS) technology. Also, graphene is one of the strongest materials in the world, with tensile strength of 130 GPa and the Young’s modulus is 1 TPa [13], *i.e.* about 100 times stronger than steel. Thus graphene has extremely high strength-to-weight ratio, it is very promising for mechanical engineering, for example, graphene-based composite materials are found in applications ranging from aerospace engineering to tennis rackets. Moreover, single layer graphene is nearly transparent as it transmits 97.7% of light. Combined with its superior electronic properties, it has great potential applications in transparent electrodes for consumer electronics such as touch screen in cell phones.

Apart from these basic physical properties, graphene is also a real wonder material for exploring many novel physical phenomena such as fractional quantum Hall effect [14-16] and specular Andreev reflection [17]. In the next sections, I will briefly

describe the electronic band structures of the single layer graphene (SLG), electric field induced band gap in bilayer graphene (BLG) and stacking orders in trilayer graphene (TLG).

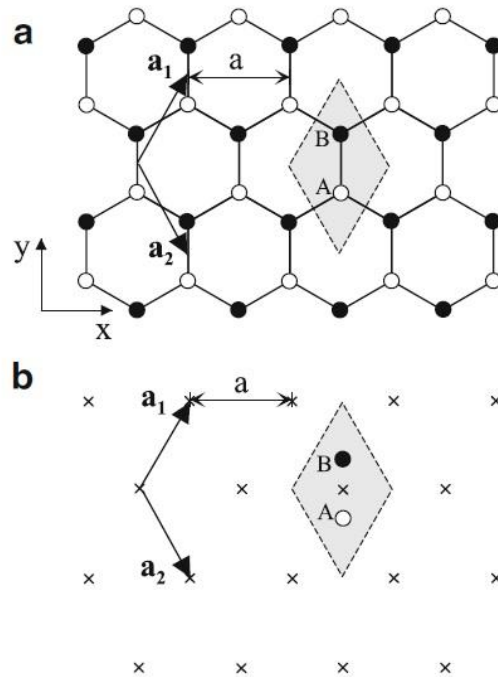
## 2.2 Single Layer Graphene



**Figure 2.2.** Two-dimensional hexagonal lattice structure of single layer graphene.

Single layer graphene (SLG) consists of carbon atoms arranged in a two-dimensional hexagonal lattice structure (Figure 2.2). Its band structure was first derived in 1947 by P. R. Wallace [7] in order to study the properties of bulk graphite, since graphene is considered as the building block of the graphite. The tight binding model is used to calculate the band structure of graphene. Here we derive the band structure calculation following McCann's work [18].

Cartesian coordinate system is used to characterize graphene lattice structure in real space. The  $x$  and  $y$  axes are perpendicular to each other and lie within the plane of graphene layer; the  $z$  axis is perpendicular to the plane. Figure 2.3 shows the real space structure of graphene lattice.  $a = 2.46 \text{ \AA}$  is the lattice constant, which is the distance between two neighboring unit cells [19]. Note that this hexagonal lattice is not a Bravais lattice because the lattice positions A and B are not equivalent.



**Figure 2.3.** (a). Real space structure of graphene. Lattice constant is  $a$ , and vectors  $\mathbf{a}_1$  and  $\mathbf{a}_2$  are primitive vectors with length  $a$ . (b). Crosses indicate the Bravais lattice corresponding to Figure 2.3 (a). Each Bravais lattice point contains two atoms: A and B.

The primitive vectors have coordinates:

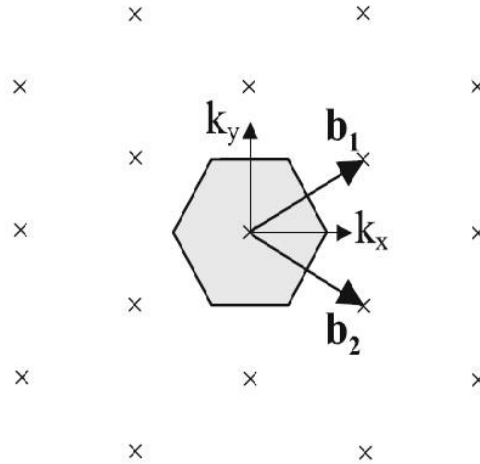
$$\mathbf{a}_1 = \left( \frac{a}{2}, \frac{\sqrt{3}a}{2} \right), \quad \mathbf{a}_2 = \left( \frac{a}{2}, -\frac{\sqrt{3}a}{2} \right)$$



The corresponding reciprocal lattice vectors  $\mathbf{b}_1$  and  $\mathbf{b}_2$  need to satisfy  $\mathbf{a}_1\mathbf{b}_1=\mathbf{a}_2\mathbf{b}_2=2\pi$  and  $\mathbf{a}_1\mathbf{b}_2=\mathbf{a}_2\mathbf{b}_1=0$ . Therefore,  $\mathbf{b}_1$  and  $\mathbf{b}_2$  are defined as following:

$$\mathbf{b}_1=\left(\frac{2\pi}{a}, \frac{2\pi}{\sqrt{3}a}\right), \quad \mathbf{b}_2=\left(\frac{2\pi}{a}, -\frac{2\pi}{\sqrt{3}a}\right)$$

Figure 2.4 shows the reciprocal lattice of monolayer graphene,  $\mathbf{b}_1$  and  $\mathbf{b}_2$  are primitive vectors and the shaded area is the first Brillouin zone.



**Figure 2.4.** Reciprocal lattice of single layer graphene. Primitive vectors  $\mathbf{b}_1$  and  $\mathbf{b}_2$  and the first Brillouin zone (shaded area).

We assume  $N$  unit cells in the hexagonal lattice structure. Every unit cell has two different atoms A and B. Moreover, we consider each carbon atom only one electron in  $2p_z$  orbital for this calculation since other three valence electrons form covalent bounds with neighboring atoms. Thus we consider  $N$  unit cells, each with two electrons. From the structure, the system has translational invariance. Then the model could be written using superposition of the Bloch functions:

$$\Phi_j(\mathbf{k}, \mathbf{r}) = \frac{1}{\sqrt{N}} \sum_{i=1}^N e^{i\mathbf{k}\cdot\mathbf{R}_{j,i}} \phi(\mathbf{r} - \mathbf{R}_{j,i})$$

where the sum is over  $N$  unit cells and  $j=A$  or  $B$  indicating two atomic orbitals from the two atoms in one unit cell. Then, in general, an electronic wave function  $\Psi_j(\mathbf{k}, \mathbf{r})$  is given by superposition of the two different Bloch functions:

$$\begin{aligned} \Psi_j(\mathbf{k}, \mathbf{r}) &= c_{j,A}(\mathbf{k})\Phi_A(\mathbf{k}, \mathbf{r}) + c_{j,B}(\mathbf{k})\Phi_B(\mathbf{k}, \mathbf{r}) \\ &= c_{j,A}(\mathbf{k}) \frac{1}{\sqrt{N}} \sum_{i=1}^N e^{i\mathbf{k}\cdot\mathbf{R}_{A,i}} \phi(\mathbf{r} - \mathbf{R}_{A,i}) + c_{j,B}(\mathbf{k}) \frac{1}{\sqrt{N}} \sum_{i=1}^N e^{i\mathbf{k}\cdot\mathbf{R}_{B,i}} \phi(\mathbf{r} - \mathbf{R}_{B,i}) \end{aligned}$$

where  $c_{j,A}$  and  $c_{j,B}$  are coefficients of the superposition. The energy  $E_j(\mathbf{k})$  of the  $j$ th band is given by

$$E_j(\mathbf{k}) = \frac{\langle \Psi_j | H | \Psi_j \rangle}{\langle \Psi_j | \Psi_j \rangle}$$

where  $H$  is the Hamiltonian. Substituting the  $\Psi_j(\mathbf{k}, \mathbf{r})$  into the energy gives:

$$\begin{aligned} E_j(\mathbf{k}) &= \frac{\langle \Psi_j | H | \Psi_j \rangle}{\langle \Psi_j | \Psi_j \rangle} \\ &= \frac{c_{j,A}^* c_{j,A} \langle \Phi_A | H | \Phi_A \rangle + c_{j,B}^* c_{j,B} \langle \Phi_B | H | \Phi_B \rangle + c_{j,A}^* c_{j,B} \langle \Phi_A | H | \Phi_B \rangle + c_{j,B}^* c_{j,A} \langle \Phi_B | H | \Phi_A \rangle}{c_{j,A}^* c_{j,A} \langle \Phi_A | \Phi_A \rangle + c_{j,B}^* c_{j,B} \langle \Phi_B | \Phi_B \rangle + c_{j,A}^* c_{j,B} \langle \Phi_A | \Phi_B \rangle + c_{j,B}^* c_{j,A} \langle \Phi_B | \Phi_A \rangle} \\ &= \frac{c_{j,A}^* c_{j,A} H_{AA} + c_{j,B}^* c_{j,B} H_{BB} + c_{j,A}^* c_{j,B} H_{AB} + c_{j,B}^* c_{j,A} H_{BA}}{c_{j,A}^* c_{j,A} S_{AA} + c_{j,B}^* c_{j,B} S_{BB} + c_{j,A}^* c_{j,B} S_{AB} + c_{j,B}^* c_{j,A} S_{BA}} \end{aligned}$$

where  $H_{AA} = \langle \Phi_A | H | \Phi_A \rangle$  and  $S_{AA} = \langle \Phi_A | \Phi_A \rangle$ . To obtain the minimized energy of  $E_j$ , we calculate the derivative of  $E_j$  with respect to  $c_{j,A}^*$  and set it equal to zero.

$$\frac{\partial E_j(\mathbf{k})}{\partial c_{jA}^*} = 0$$

Through straightforward but rather long derivation, we arrive at these results:

$$H_{AA}c_{jA} + H_{AB}c_{jB} = E_j(S_{AA}c_{jA} + S_{AB}c_{jB})$$

Similarly, we calculate the derivative of  $E_j$  with respect to  $c_{jB}^*$  and set it to zero, we obtain:

$$H_{BA}c_{jA} + H_{BB}c_{jB} = E_j(S_{BA}c_{jA} + S_{BB}c_{jB})$$

Combined two equations above, we can rewrite them into matrix equation:

$$\begin{pmatrix} H_{AA} & H_{AB} \\ H_{BA} & H_{BB} \end{pmatrix} \begin{pmatrix} c_{jA} \\ c_{jB} \end{pmatrix} = E_j \begin{pmatrix} S_{AA} & S_{AB} \\ S_{BA} & S_{BB} \end{pmatrix} \begin{pmatrix} c_{jA} \\ c_{jB} \end{pmatrix}$$

So the energy values may be determined by solving the equation:

$$\det(H - E_j S) = 0$$

The next step will be calculating all the elements in the determinant.

$$H_{AA} = \frac{1}{N} \sum_{i=1}^N \sum_{j=1}^N e^{i\mathbf{k} \cdot (\mathbf{R}_{A,j} - \mathbf{R}_{A,i})} \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | H | \phi_A(\mathbf{r} - \mathbf{R}_{A,j}) \rangle$$

This equation includes a double summation over all the A sites of the entire lattice. We can safely assume that the dominant contribution comes from within each unit cell, in other words, from the terms with  $j=i$ . Then:

$$H_{AA} \approx \frac{1}{N} \sum_{i=1}^N \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | H | \phi_A(\mathbf{r} - \mathbf{R}_{A,j}) \rangle$$

We set  $\langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | H | \phi_A(\mathbf{r} - \mathbf{R}_{A,j}) \rangle$  equal to a parameter  $\epsilon_{2p}$  and for every A site of its own unit cell, this parameter should be identical for all  $N$  unit cells. Therefore:

$$H_{AA} \approx \frac{1}{N} \sum_{i=1}^N \epsilon_{2p} = \epsilon_{2p}$$

For the B sublattice, it has identical chemical structure as the A sublattice, so it is reasonable to expect:

$$H_{BB} = H_{AA} \approx \epsilon_{2p}$$

The off-diagonal matrix elements will be slightly more complicated.

$$H_{AB} = \frac{1}{N} \sum_{i=1}^N \sum_{j=1}^N e^{i\mathbf{k} \cdot (\mathbf{R}_{B,j} - \mathbf{R}_{A,i})} \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | H | \phi_B(\mathbf{r} - \mathbf{R}_{B,j}) \rangle$$

If we adopt a similar approximation, we can only consider the nearest neighbor atoms. In the hexagonal lattice, every A site is surrounded by three B sites. Then we rewrite the equation above:

$$H_{AB} \approx \frac{1}{N} \sum_{i=1}^N \sum_{l=1}^3 e^{i\mathbf{k} \cdot (\mathbf{R}_{B,l} - \mathbf{R}_{A,i})} \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | H | \phi_B(\mathbf{r} - \mathbf{R}_{B,l}) \rangle$$

Similarly, the term  $\langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | H | \phi_B(\mathbf{r} - \mathbf{R}_{B,l}) \rangle$  between each pair of neighboring atoms should have identical values. We use a positive parameter to express this hopping energy between nearest neighbors:

$$\gamma_0 = -\langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | H | \phi_B(\mathbf{r} - \mathbf{R}_{B,l}) \rangle$$

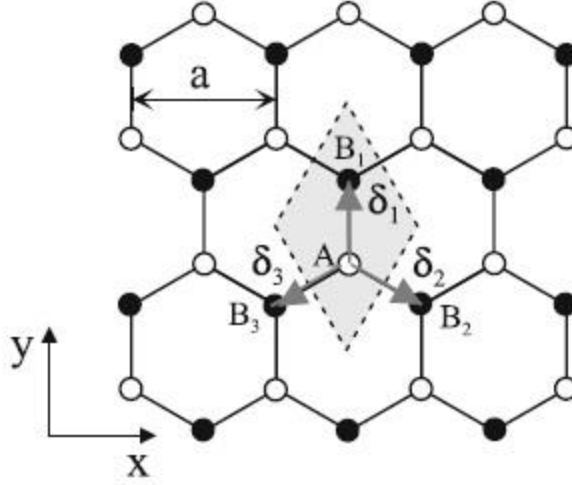
Then,

$$\begin{aligned} H_{AB} &\approx -\frac{1}{N} \sum_{i=1}^N \sum_{l=1}^3 e^{i\mathbf{k} \cdot (\mathbf{R}_{B,l} - \mathbf{R}_{A,i})} \gamma_0 \\ &= -\frac{\gamma_0}{N} \sum_{i=1}^N \sum_{l=1}^3 e^{i\mathbf{k} \cdot \boldsymbol{\delta}_l} \equiv -\gamma_0 f(\mathbf{k}) \end{aligned}$$

$$f(\mathbf{k}) = \sum_{l=1}^3 e^{i\mathbf{k} \cdot \boldsymbol{\delta}_l}$$

where  $\boldsymbol{\delta}_l = \mathbf{R}_{B,l} - \mathbf{R}_{A,i}$  is the position vector from atom  $A_i$  to atom  $B_l$ . We can actually calculate the detailed results of  $f(\mathbf{k})$  if we know  $\boldsymbol{\delta}_1$ ,  $\boldsymbol{\delta}_2$  and  $\boldsymbol{\delta}_3$ . From Figure 2.5, we can write down the coordinates of vector  $\boldsymbol{\delta}_l$ .

$$\boldsymbol{\delta}_1 = \left(0, \frac{a}{\sqrt{3}}\right), \boldsymbol{\delta}_2 = \left(\frac{a}{2}, -\frac{a}{2\sqrt{3}}\right), \boldsymbol{\delta}_3 = \left(-\frac{a}{2}, -\frac{a}{2\sqrt{3}}\right)$$



**Figure 2.5.** Three position vectors  $\delta_1$ ,  $\delta_2$  and  $\delta_3$  from atom A to its three nearest neighbors.

Substituting these vectors into  $f(\mathbf{k})$ , we obtain:

$$f(\mathbf{k}) = e^{ik_y a/\sqrt{3}} + 2e^{-ik_y a/2\sqrt{3}} \cos(k_x a/2)$$

where  $\mathbf{k} = (k_x, k_y)$ . So, we know  $H_{AB}$  now and the other off-diagonal matrix element is just the complex conjugate of  $H_{AB}$ .

$$H_{AB} \approx -\gamma_0 f(\mathbf{k}), \quad H_{BA} \approx -\gamma_0 f^*(\mathbf{k})$$

In summary, matrix  $H$  can be written as:

$$H = \begin{pmatrix} \epsilon_{2p} & -\gamma_0 f(\mathbf{k}) \\ -\gamma_0 f^*(\mathbf{k}) & \epsilon_{2p} \end{pmatrix}$$

Next step, we calculate the elements of matrix  $S$ .

$$\begin{aligned}
S_{AA} &= \frac{1}{N} \sum_{i=1}^N \sum_{j=1}^N e^{i\mathbf{k} \cdot (\mathbf{R}_{A,j} - \mathbf{R}_{A,i})} \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | \phi_A(\mathbf{r} - \mathbf{R}_{A,j}) \rangle \\
&\approx \frac{1}{N} \sum_{i=1}^N \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) \rangle \\
&= \frac{1}{N} \sum_{i=1}^N 1 \\
&= 1
\end{aligned}$$

Again,  $S_{BB} = S_{AA} = 1$ . We calculate the off-diagonal matrix elements in a similar way as for the matrix  $H$ .

$$\begin{aligned}
S_{AB} &= \frac{1}{N} \sum_{i=1}^N \sum_{j=1}^N e^{i\mathbf{k} \cdot (\mathbf{R}_{B,j} - \mathbf{R}_{A,i})} \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | \phi_B(\mathbf{r} - \mathbf{R}_{B,j}) \rangle \\
&= \frac{1}{N} \sum_{i=1}^N \sum_{l=1}^3 e^{i\mathbf{k} \cdot (\mathbf{R}_{B,l} - \mathbf{R}_{A,i})} \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | \phi_B(\mathbf{r} - \mathbf{R}_{B,l}) \rangle \\
&= s_0 f(\mathbf{k})
\end{aligned}$$

where  $s_0 = \langle \phi_A(\mathbf{r} - \mathbf{R}_{A,i}) | \phi_B(\mathbf{r} - \mathbf{R}_{B,l}) \rangle$  and  $S_{BA} = S_{AB}^* = s_0 f^*(\mathbf{k})$ .

Summarizing all the results we have calculated,

$$H = \begin{pmatrix} \epsilon_{2p} & -\gamma_0 f(\mathbf{k}) \\ -\gamma_0 f^*(\mathbf{k}) & \epsilon_{2p} \end{pmatrix}, \quad S = \begin{pmatrix} 1 & s_0 f(\mathbf{k}) \\ s_0 f^*(\mathbf{k}) & 1 \end{pmatrix},$$

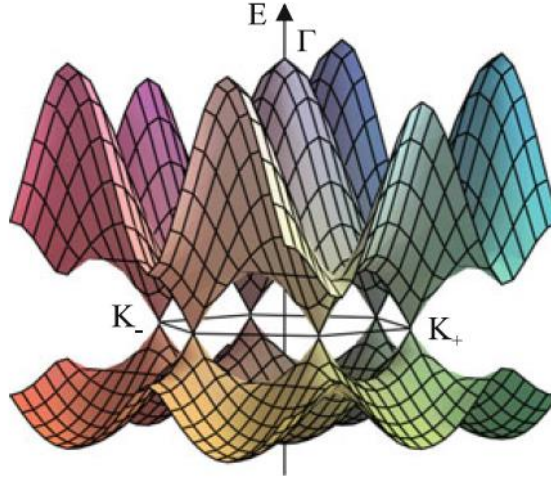
$$f(\mathbf{k}) = e^{ik_y a / \sqrt{3}} + 2e^{-ik_y a / 2\sqrt{3}} \cos(k_x a / 2)$$

$$\det(H - E_j S) = 0$$

we now can solve the equation to get energy:

$$E_{\pm} = \frac{\epsilon_{2p} \pm \gamma_0 |f(\mathbf{k})|}{1 \pm s_0 |f(\mathbf{k})|}$$

This result appears in Saito *et. al.*[19], where parameters  $\epsilon_{2p}$ ,  $\gamma_0$  and  $s_0$  need to be determined separately via alternative methods. Here, in Figure 2.6, we show the energy band structure from Saito *et. al.* [19], using  $\epsilon_{2p} = 0$ ,  $\gamma_0 = 3.033$  eV and  $s_0 = 0.129$ .



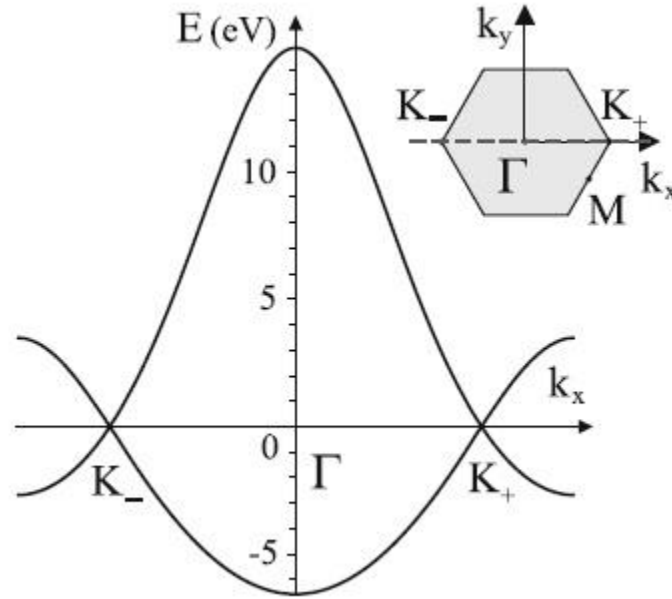
**Figure 2.6.** Band structure of monolayer graphene by tight binding calculation.  $K_+$  and  $K_-$  are two corners and  $\Gamma$  is the center of the Brillouin zone [18].

A slice through the three dimensional band structure yields the dispersion  $E(k)$  commonly plotted in literature (Figure 2.7). Clearly, at  $K_+$  and  $K_-$  points,  $E=0$ . In their vicinity, after Tylor expansion, we obtain the linear dispersion relationship:

$$E_{\pm}(\mathbf{k}) = \pm \hbar v_F |\mathbf{k}|$$



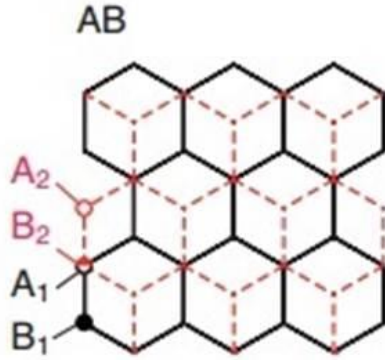
where  $v_F = 10^6 \text{ m/s}$  is the Fermi velocity.



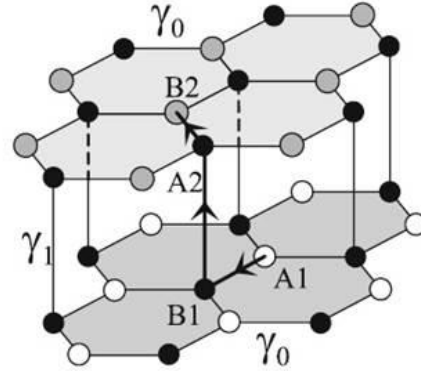
**Figure 2.7.** The low energy band structure of monolayer graphene in  $k_x$ - $k_y$  plane. Inset: Different points  $K_+$ ,  $K_-$  and  $\Gamma$  in the Brillouin zone [18].

### 2.3 Bilayer Graphene and its Tunable Band gap

Bilayer layer graphene (BLG) consists of two atomic layers of hexagonal lattices. Most BLG are AB stacked, *i.e.* carbon atoms from the top layer are located above the center of hexagons of bottom layer (Figure 2.8). The tight binding method can also be used to calculate the band structure of BLG, similar to that of SLG, though we now need to consider the inter-layer coupling when we calculate the matrix elements. In other words, we need to take into account not only  $\gamma_0$  but also  $\gamma_1$ , which is the interlayer coupling between the nearest neighbors (Figure 2.9).



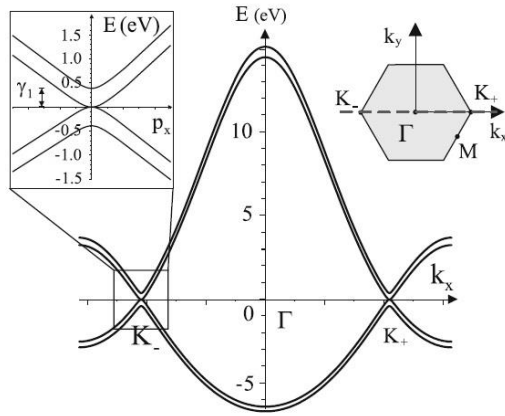
**Figure 2.8.** AB stacked layer structure of BLG.



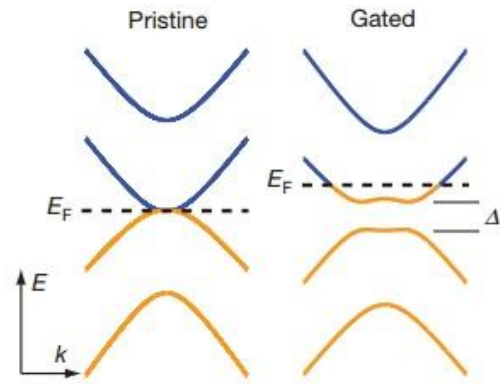
**Figure 2.9.** Coupling between atoms considered when calculating BLG band structure [18].

Using the same method, tight binding model gives the band structure of BLG with the same parameters  $\epsilon_{2p} = 0$ ,  $\gamma_0 = 3.033$  eV,  $s_0 = 0.129$ , plus  $\gamma_1 = 0.39$  eV. Figure 2.10 shows the band structure of BLG in  $k_x$ - $k_z$  plane. In particular, near the vicinity of K points, one pair of conduction and valence band splits away from the zero energy by a magnitude of interlayer coupling  $\gamma_1$ ; the other pair of bands are parabolic and touches at the K points, thus it is also gapless.

Theoretically, a band gap in BLG is expected to open in the presence of a potential difference between the two layers that breaks the inversion symmetry, and the gap size will depend on the Fermi level and the inter-layer potential [20,21]. This is soon verified experimentally using transport [22-28] and optical [29-31] measurements. Typically a dual-gated field effect transistor geometry is employed to independently control the potential difference and carrier density. Alternatively, band gap has also been observed in chemically doped BLG [32].



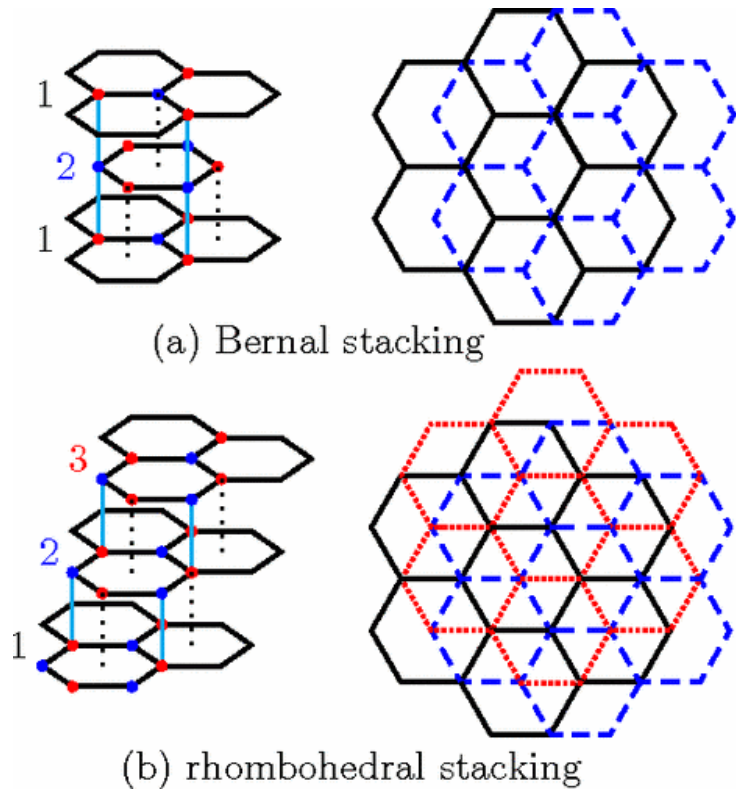
**Figure 2.10.** Band structure of BLG [18].



**Figure 2.11.** Simplified band structure of BLG without and with electric field [33].

## 2.4 Stacking Order in Trilayer Graphene

Adding another layer to bilayer graphene will yield trilayer graphene (TLG). The third layer can be arranged in two distinctive configurations -- if atoms in the top layer are exactly on top of those in the bottom layer, the TLG is Bernal or ABA stacked (B-TLG); alternatively, if one sublattice of the top layer lies above the center of the hexagons of the bottom layer, the TLG is rhombohedral or ABC stacked (r-TLG). The atomic configurations of B-TLG and r-TLG are shown in Figure 2.12. B-TLG is energetically favored and much more common in bulk graphite.



**Figure 2.12.** ABA and ABC stacking of TLG of different views [34].

These two allotropes of TLG have very different material properties. Most noticeably, B-TLG is semi-metallic with a tunable band overlap, and r-TLG is semiconducting with a tunable band gap. Our prior work compared the electric properties of TLG of both stacking orders, and found that r-TLG shows an intrinsic interaction-driven gap  $\sim 6$  meV at the Dirac point [35]. LeRoy's group [36] also discovered the widely tunable band gap as a function of electric field in r-TLG by scanning tunneling microscopy (STM) studies.

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## **Chapter 3          Fabrication of Graphene Devices**

To characterize the electrical transport properties of novel two dimensional materials, we prepare high quality atomic flakes, perform microfabrication in cleanroom, and package the device for various transport measurements. These steps are generally referred to as device fabrication procedures. In this chapter, I will describe a versatile resist-free fabrication technique and a multistep lithography fabrication technique.

### **3.1    Resist-Free Shadow Mask Fabrication technique**

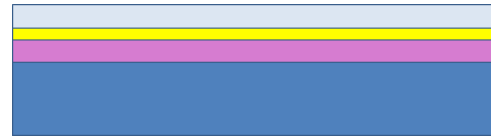
Shadow mask fabrication technique was initially developed by a former group member Wenzhong Bao [37] and modified by me based on my experience. It is a simple one-step process in which metal deposition will be performed directly through the shadow mask that is aligned with target sample, thus forming electrodes. I will elucidate first the fabrication procedures for shadow masks, then their applications for device fabrication and other functions such as patching broken electrodes.

#### **3.1.1   Fabricating Shadow Masks**

Fabrication of the shadow masks is the most time-consuming step in the entire device fabrication process, as it involves multiple etching steps and great care should be taken during the entire fabrication. However, once made, a high-quality shadow mask can be re-used for over 30 times.

(1) We order silicon wafers with 300 nm oxide layer as the substrate. The detailed parameters are: 200- $\mu\text{m}$ -thick silicon, 4 inches in diameter, *p*-type silicon with boron as dopant, resistivity between 0.01~0.02 ohm-cm, with 300 nm wet thermal oxide, prime grade wafers. Apart from the thickness (200  $\mu\text{m}$  versus 500  $\mu\text{m}$ ), these parameters are identical to those for the standard wafers used for the devices. Thinner wafers are used so as to reduce the etching time (see step 8 below).

(2) Clean the wafer thoroughly with acetone, rinse it with isopropyl alcohol (IPA) and then deionized water (DI water). 200 nm of chromium is deposited



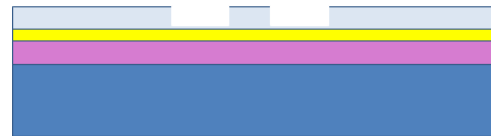
**Figure 3.1.** Si (blue) /SiO<sub>2</sub> (purple) wafer with Cr (yellow) layer and PMMA resist layer.

onto the SiO<sub>2</sub> surface by electron beam (e-beam) evaporation at a steady rate of  $\sim 2 \text{ \AA/s}$ . We then spin one layer of e-beam resist on top of chromium layer. We use positive resist 950 PMMA (polymethyl methacrylate) A4, where 950 refers to the molecular weight (950,000); A4 means it is a 4% solution in anisole. The programmed recipe for spin-coating PMMA is: 4000 rpm for 40 seconds, the acceleration of both ramping up and down is 1000 rpm/s. The entire wafer with PMMA is baked at 180 °C for 10 minutes after spin-coating.

(3) Cut the 4 inch wafers to  $\sim 1 \text{ cm} \times \sim 1.5 \text{ cm}$  rectangular pieces. Do it on a soft and clean cleanroom paper towel, and use a diamond pan to cut it from the back of the wafer.

(4) We now perform electron beam lithography (EBL) to define the pattern on PMMA layer. The pattern represents the layout of electrodes for the devices, for example, simple two-terminal source drain electrodes, or Hall bar geometry electrodes. It should be designed using CAD in advance.

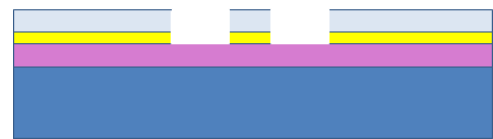
(5) Develop the exposed PMMA in the mixture solution of IPA and MIBK (3:1) for 65 seconds, then rinse it in pure IPA and DI water.



**Figure 3.2.** Pattern opened in PMMA layer.

(6) Chromium etching.

After the EBL and development, the windows of the electrodes pattern in PMMA layer are opened, exposing the underneath chromium layer. We immerse the wafer into chromium etchant to etch away the exposed chromium layer. The standard



**Figure 3.3.** Chromium layer etched.

etching rate is  $\sim 32 \text{ \AA/s}$ , however, in practice, the etching time varies significantly from sample to sample. If the chromium layer is over-etched, the resultant zigzag edges at the chromium layer can significantly affect the profiles of the  $\text{SiO}_2$  and Si layers in the following dry etching procedures. Thus to ensure an accurate etching time, we need to check the color of etching windows in the wafer frequently under optical microscope. This step requires great patience. If inexperienced, it is

best to etch the wafer one by one. After chromium etching, we dissolve the rest of PMMA (10 minutes in acetone and then rinse it with IPA and DI water).

(7) Silicon dioxide etching.

We use reactive ion etcher (RIE) system to etch SiO<sub>2</sub> layer. Put all pieces of wafers on a substrate for RIE. Make sure

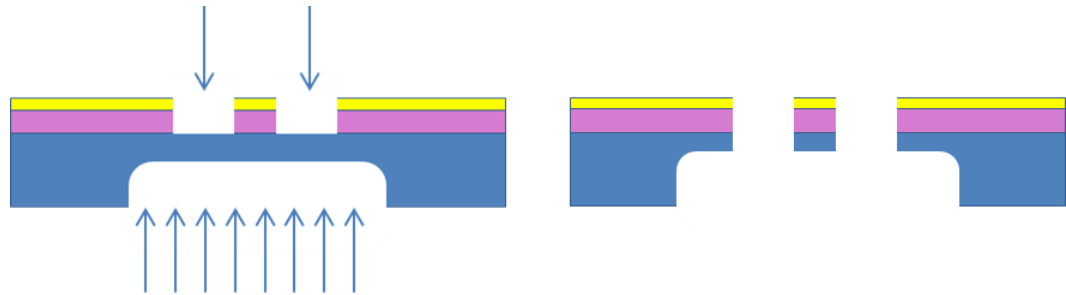


**Figure 3.4.** SiO<sub>2</sub> layer etched.

they are leveled and uniformly dispersed on the substrate. The key parameters of the recipe are: 30 sccm CHF<sub>3</sub> and 20 sccm CF<sub>4</sub> mixture gas under 300W radio frequency power for plasmas; 4 minutes etching time. This recipe completely etches 300 nm SiO<sub>2</sub> layer.

(8) Silicon etching.

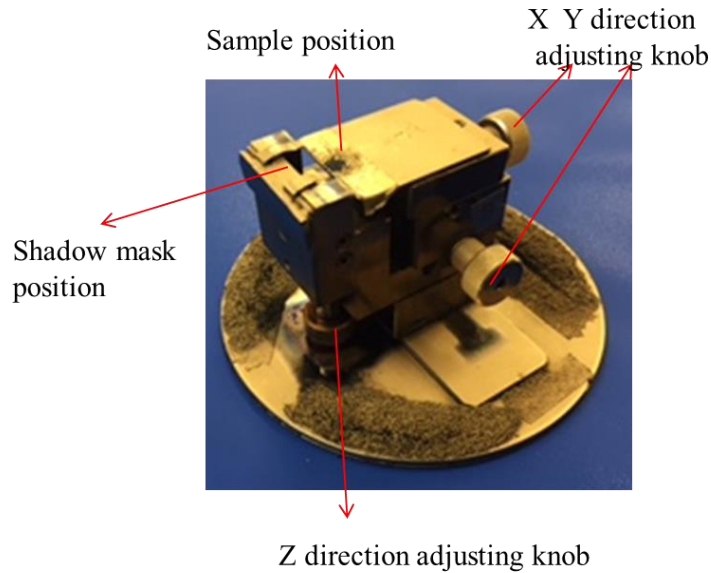
This is the final step of shadow mask fabrication, which demands much time and patience. We use inductively coupled plasma (ICP) etch system to etch silicon. First, use thermal tape to cover the four sides of the rectangle wafer from the back, only leave a window in the center. The window cannot be too large because otherwise the shadow mask would be too fragile; it should also overlap with the pattern in the front. Then, we etch in the window from back until the thickness of silicon layer is reduced to about 30  $\mu\text{m}$ . After the back etching, we etch the wafer from the front. The electrodes pattern on this wafer will be etched through eventually. During this step, we can use Dektak surface Profilometer to measure the depth of etched silicon layer anytime.



**Figure 3.5.** Silicon layer etching process.

### **3.1.2 Using Shadow Masks**

Fabricating devices using shadow masks is quick and easy, as it involves only two steps -- aligning the mask with the target sample followed by metal deposition. Another advantage is that the process is free of lithography; hence the devices may be much cleaner due to the absence of resists. Another application of shadow masks is to patch up broken electrodes of finished devices. Therefore, this versatile fabrication technique complements the primarily used the EBL technique.



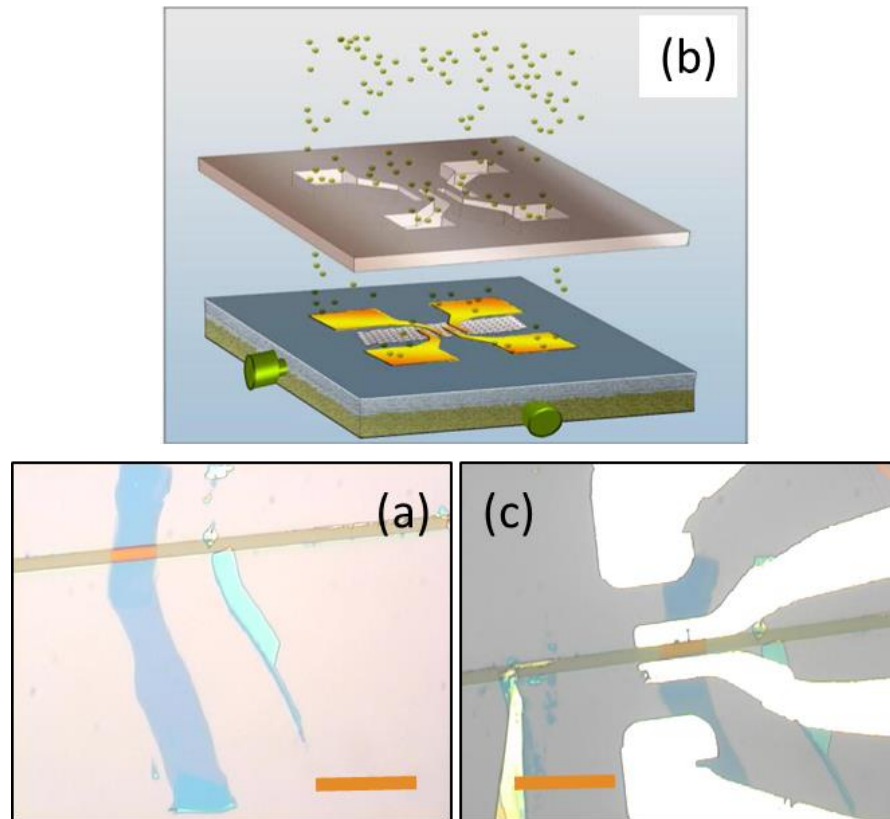
**Figure 3.6.** Alignment stage for shadow masks.

To deposit electrodes onto the selected sample (graphene or other materials) through a shadow mask, we need to align them. Figure 3.6 shows a three-dimension moveable stage. The shadow mask is clamped on the top with front side facing down, and the substrate with the targeted sample will be placed on the top of the stage. Then, the pattern in the mask and the sample will be aligned together using the X, Y, Z adjusting knobs under optical microscope. Figure 3.7 depicts this process. Figure 3.7 (a) shows a picture of few-layer graphene sheet across the predefined trench in the substrate. After the alignment and deposition process in Figure 3.7 (b), source-drain electrodes are deposited onto the graphene sheet forming a suspended graphene device.

There are a few tips during the usage of shadow mask. After the alignment, we should always handle the stage very gently, and avoid any mechanical vibrations that

may affect the alignment. The rotation function should be turned off during the evaporation.

These masks are extremely delicate. Careful handling will greatly extend their lifetime.



**Figure 3.7.** Illustrations of shadow mask fabrication process and image of the device. Scale bar: 10  $\mu\text{m}$ . Figure 3.7. (b). from [37].

## 3.2 Fabrication of Dual-gated Suspended Double Layer Graphene

### Devices

Despite its advantages such as quick turnaround time and clean electrode-sample interface, the shadow mask technique lacks flexibility in terms of device geometries or

electrodes patterns. Electron beam lithography (EBL), which is the primary fabrication tool in our research, complements this drawback. With the assist of various resists and multiple times lithography, different device structures could be fabricated. In this section, I will describe in detail the fabrication procedures of my dual-gated suspended double layer graphene project, which involves the 2D material transfer, suspended top gate and wet etching. In Chapter 5 that lists my other collaborative projects; I will describe another EBL technique that suspends atomic membranes by the electrodes.

### **3.2.1 Sample Preparation and Graphene Transfer**

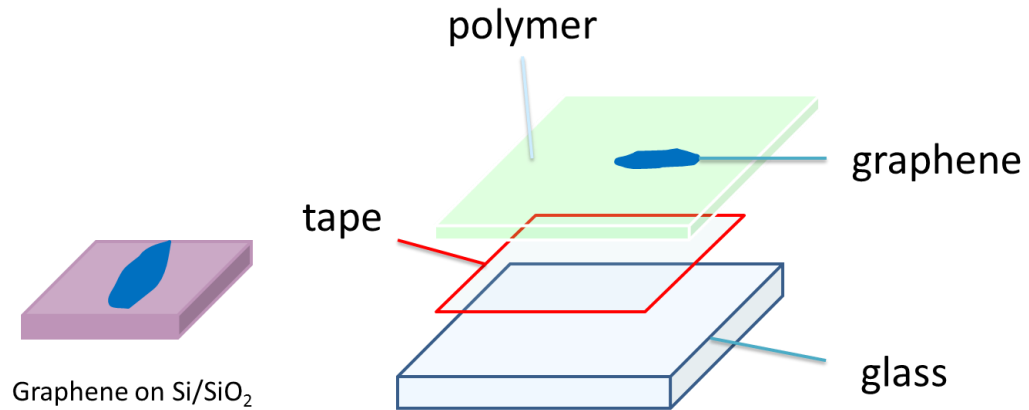
Briefly, the entire process starts with the preparation of two graphene flakes, which will be transferred on top one another forming a cross geometry. Four electrodes are fabricated on both ends of each two flakes, and a contactless suspended top gate will be fabricated above the both two flakes. Finally we use wet etching to remove the underlying SiO<sub>2</sub> substrate and dry the device carefully. The detailed procedures are described as following.

- (1) Prepare two graphene flakes.

We prepare two graphene flakes on different substrates. One is on the standard Si/SiO<sub>2</sub> substrate. For the other flake, we prepare a clean transparent glass substrate, put a layer of transparent tape on the glass, and spin a layer of LOR and PMMA, finally we exfoliate graphene flakes on the top of PMMA layer. Both



flakes should be long and narrow, which facilitates the subsequent alignment (Figure 3.8).

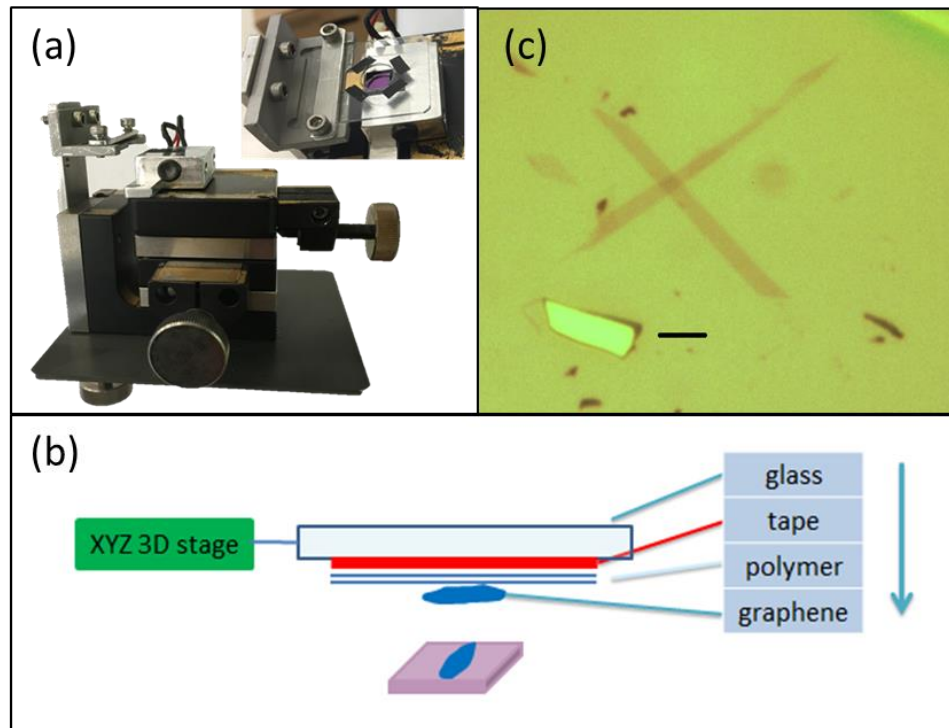


**Figure 3.8.** Two graphene flakes on different substrates ready for transfer.

(2) Flake transfer.

This process is done in a XYZ 3D stage (Figure 3.9 (a)) under 200x magnification of an optical microscope. We first align two flakes together and heat the stack to ~70 °C using the built-in heater. The two substrates will adhere together firmly as PMMA will soften and melt. Notice that the interface between two flakes is clean without contamination from the transfer process. The stack is removed from the transfer stage and heated on hotplate to ~170 °C so to separate the glass substrate and the tape from the stack. Finally, we use PG remover to dissolve the polymer layer (LOR and PMMA), leaving two aligned graphene flakes on top of Si/SiO<sub>2</sub>.

Figure 3.9 (b-c) shows the schematics of the transfer and an optical image of the resultant double layer graphene stack.



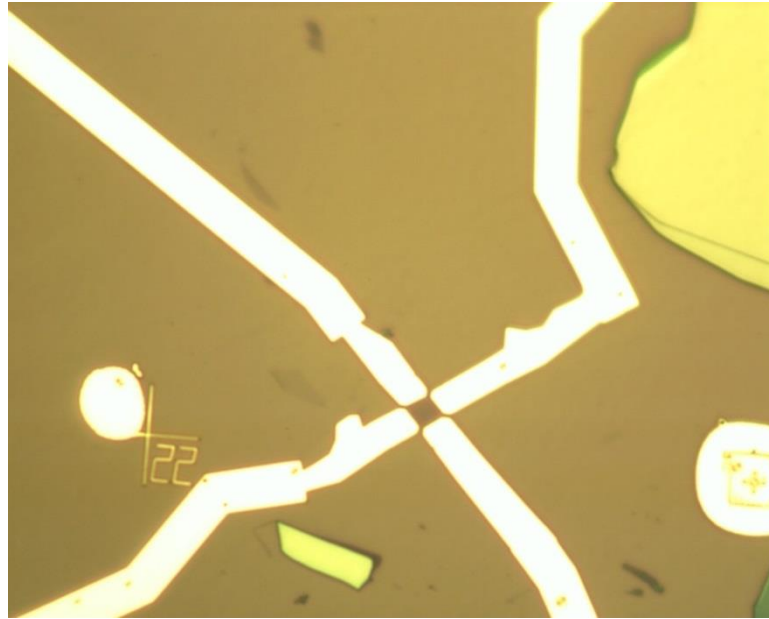
**Figure 3.9.** (a). XYZ 3D transfer stage (b). The schematics of the transfer process (c). Optical image of transferred graphene flakes.

### 3.2.2 Multistep Lithography Fabrication

(3) First e-beam lithography (EBL) step for electrodes.

We spin two layers of PMMA onto the graphene flakes. The spin-coating parameters are: 1000 rpm/s acceleration for ramping up and down, 4000 rpm spinning speed for 40 seconds. The sample is baked at 180 °C for 10 minutes after the spin-coating of each layer. Then we perform the first EBL to write electrodes

pattern and use electron beam evaporation to deposit chromium and gold as the electrodes on both ends of each graphene flakes (Figure 3.10).



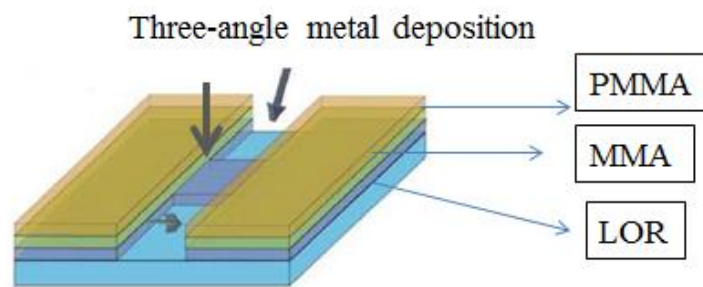
**Figure 3.10.** Graphene flakes with electrodes deposited.

(4) Adding contactless suspended top gate.

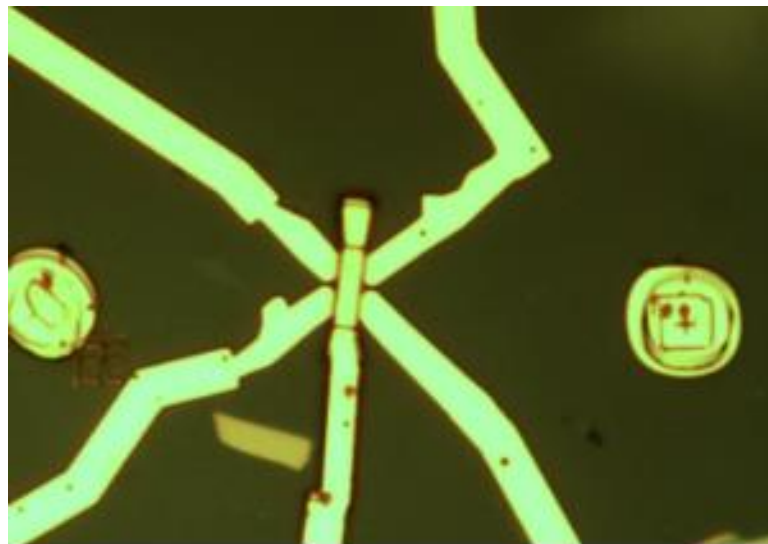
Dual-gated devices can independently control the electric field and charge carrier density. Since the graphene flakes will be suspended, we also need to fabricate suspended top gates. This technique was initially developed by former group members Gang Liu [38] and Jairo Velasco and modified by other group members. Here a brief description is provided.

On top of the graphene flakes and electrodes, a bilayer of LOR and PMMA are spun. The anchors of the suspended top gate will be developed after the first EBL.

The second EBL exposes the bridge part, after development, a step feature is formed. The unique three-angle metal deposition ensures the robust side walls of the suspended top gate (Figure 3.11). For details, please refer to prior work [38]. Figure 3.12 shows an optical microscope image with contactless top gate. The top gate is blurry since it is higher than the focal plane.



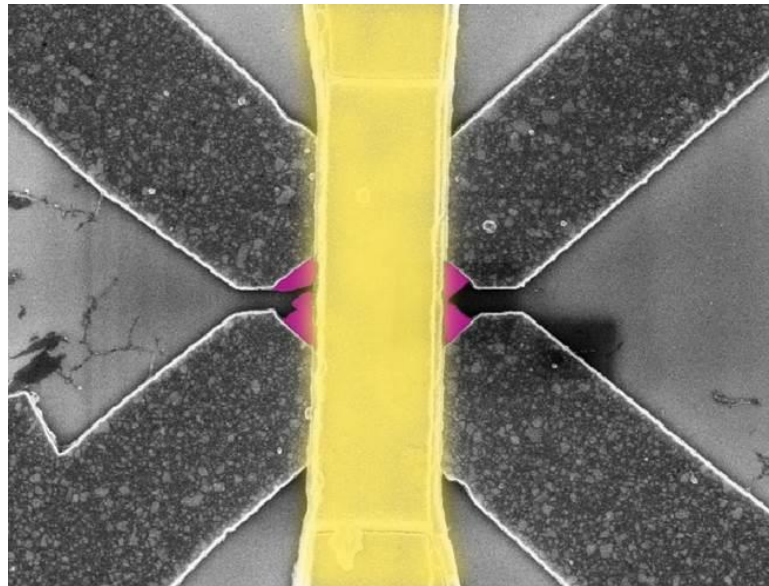
**Figure 3.11.** Three angle metal deposition in top gate fabrication.



**Figure 3.12.** Finished top gate on top of the graphene flakes with electrodes.

(5) Wet etching to suspend graphene flakes.

The final step is the wet etching. We use buffered oxide etchant to partially remove the SiO<sub>2</sub> layer, typically etching ~120 nm in 70 seconds. To minimize surface tension during the drying, a critical point dryer is used. Figure 3.13 shows an SEM image of the final device.

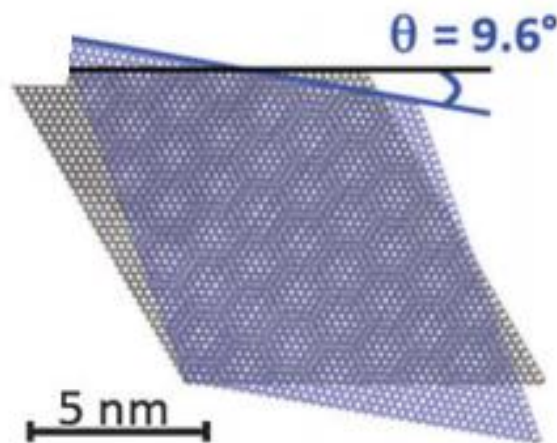


**Figure 3.13.** An SEM image of the device. Gold color labels the top gate, and the purple color shows the two suspended graphene flakes.

- [37] W. Z. Bao, G. Liu, Z. Zhao, H. Zhang, D. Yan, A. Deshpande, B. J. LeRoy and C. N. Lau, *Lithography-free fabrication of high quality substrate-supported and freestanding graphene devices*, Nano Res **3**, 98 (2010).
- [38] G. Liu, J. Velasco, W. Z. Bao and C. N. Lau, *Fabrication of graphene p-n-p junctions with contactless top gates*, Appl. Phys. Lett. **92**, 203103 (2008).

## Chapter 4      Transport Measurements of Suspended Twisted Bilayer Graphene

In this chapter I will describe measurements of suspended twisted bilayer graphene devices. Unlike AB-stacked bilayer graphene, twisted bilayer graphene consists of two separate graphene sheets stacked together with a relative rotation angle  $\theta$ . A weak interlayer coupling exists between two layers of graphene while they retain some degrees of independence. Such a system with a new degree of freedom contains rich physics. For instance, researchers from Rutgers University observed van Hove singularity in twisted graphene layers [39], using the scanning tunneling spectroscopy. Jarillo-Herrero group studied the transport properties of twisted bilayer graphene encapsulated by hexagonal boron nitrides flakes [40]. They found that filling factors of each layer can be independently controlled and hence induced Landau level crossings between the layers.



**Figure 4.1.** Twisted bilayer graphene at angle  $\theta = 9.6$  [41].

## 4.1 Post-fabrication Treatment of Suspended Graphene

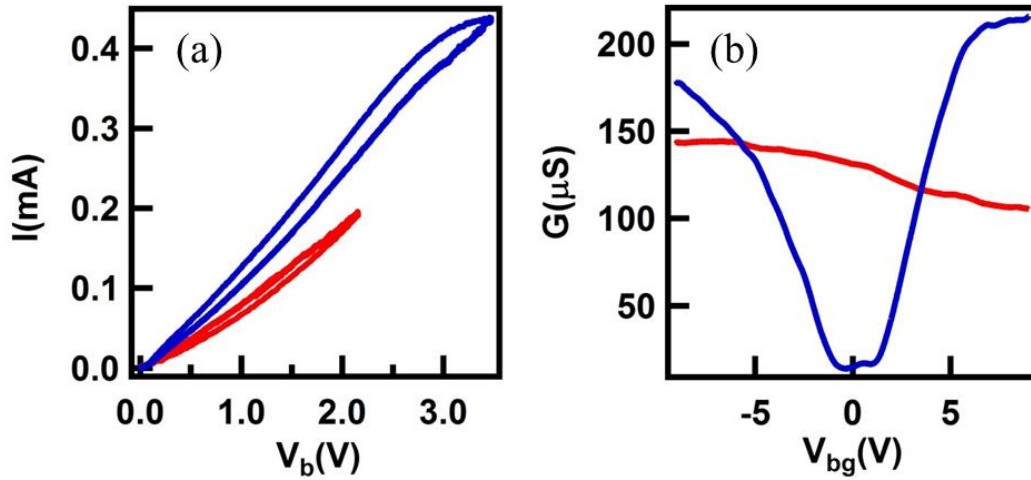
The devices are cooled in our Oxford He<sup>3</sup> cryogenic system to 260 mK. We use an SRS lock-in amplifier to measure the conductance of the fabricated devices. However, all devices need to be annealed before characterization. Instead of vacuum annealing or gas annealing, a current-induced Joule heating technique cleans the suspended graphene very well [42]. In this section, I will describe this technique in the suspended double layer graphene devices and its results.

In our four-terminal suspended devices, any two terminals could be a pair of source-drain electrodes because the interlayer contact resistance is negligibly small. We apply a source-drain bias voltage across one selected pair, while all the unused terminals should be disconnect rather than grounded. We ramp up the bias voltage slowly ( $\sim 10$  mV/s) and monitor the change of induced current (Figure 4.2 (a)). The  $I$ - $V$  curve should be linear for small bias, and starts to saturate at certain point. As soon as current starts to saturate, the bias voltage should be ramped down back to zero. Then we measure the conductance as a function of back gate voltage (Figure 4.2 (b)). Field effect mobility can be estimated from the  $G(V_{bg})$  curve. This process could be repeated several times until a satisfactory result in device mobility is achieved. I have also tried alternative current annealing between different pairs, though with similar annealing effect. We also note that current saturation phenomenon does not reliably appear in single layer graphene.

Figure 4.2 shows the current annealing cycles and corresponding  $G(V_{bg})$  curves in the suspended double layer graphene devices. The blue  $I$ - $V$  characteristics demonstrates



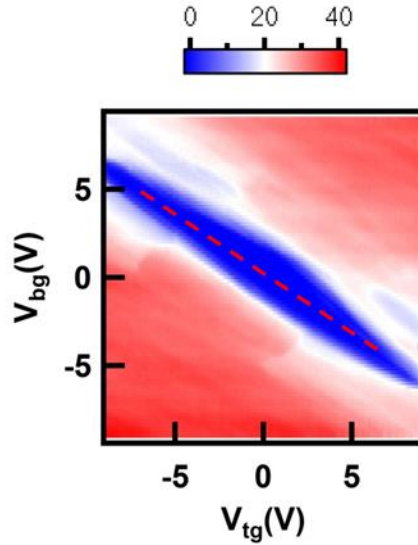
that current is already saturated; while the mobility calculated from the subsequent  $G(V_{bg})$  curve is  $\sim 7500 \text{ cm}^2/\text{Vs}$ .



**Figure 4.2.** (a). Current-Voltage cycles in the current annealing process. (b). Conductance versus back gate voltage after each current annealing cycle.

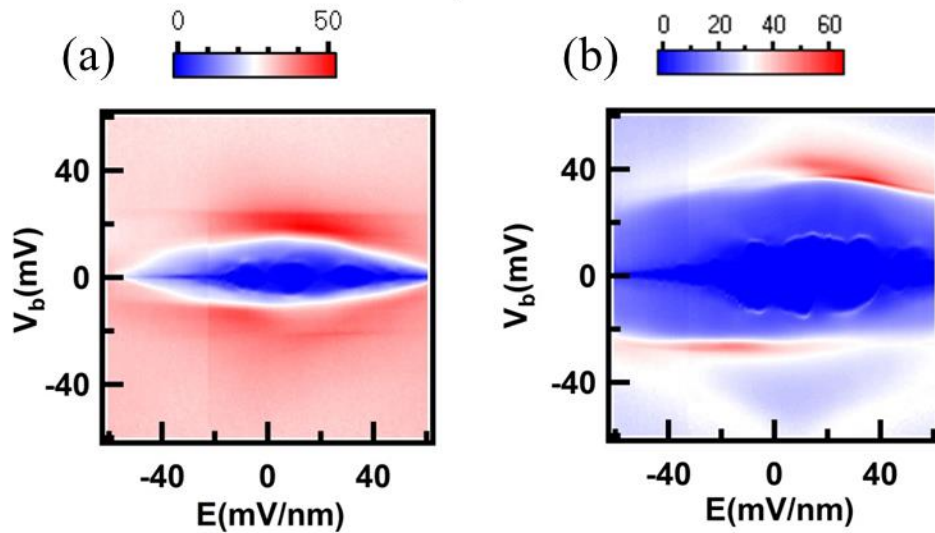
## 4.2 Transport Data

For typical samples, we measure conductance as a function of electrical field, charge density, magnetic field and bias voltage. Since our device is dual-gated, we can independently control the electrical field and carrier density within the graphene flakes. However, we need to determine the coupling ratio between two gates. I will first present the data from the bottom graphene layer, which is a bilayer graphene in this device. We measure conductance as a function of both back gate voltage and top gate voltage and plot them in Figure 4.3. From the red dashed line, we can extract the coupling ratio between the two gates  $\sim 0.64$ .



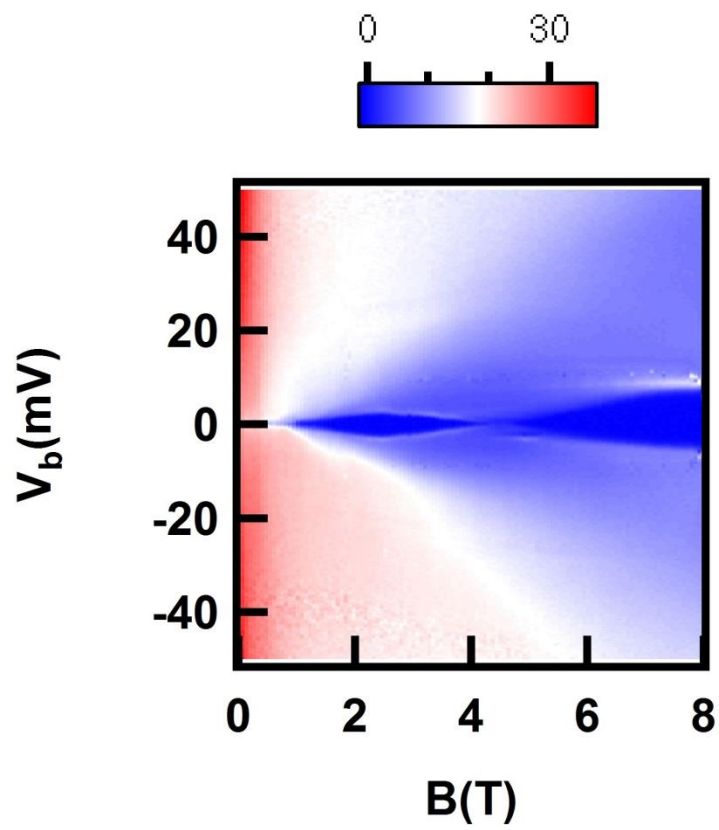
**Figure 4.3.** Conductance as a function of back gate and top gate voltages at  $B=3.5\text{T}$ ,  $T=260\text{mK}$ .

After we obtain the coupling ratio of two gates, we can control the carrier density at zero and measure the conductance as a function of bias voltage and electric field. Figure 4.4 presents two data sets at different magnetic fields with controlled zero carrier density. In Figure 4.4 (a), the 3.5T magnetic field induced gap is gradually closed by applied electrical field from both gates. The gap is extended in a higher magnetic field in Figure 4.4 (b), however, the electrical field still reduces the gap size.



**Figure 4.4.** Conductance as a function of bias voltage and electrical field at different magnetic fields: (a).  $B=3.5T$ ; (b).  $B=7T$ .

The cross-layer transport also shows interesting data. We measure the conductance between two electrodes from the top layer to bottom layer as a function of the bias voltage and magnetic field. Figure 4.5 plots the data. The magnetic field induces a gap at small field but then the gap is closed with the increasing magnetic field, and finally larger magnetic field re-opens the gap. These data are not understood and warrant further experimental studies.



**Figure 4.5.** Conductance as a function of bias voltage and magnetic field.

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## Chapter 5 Collaborative Projects on Graphene

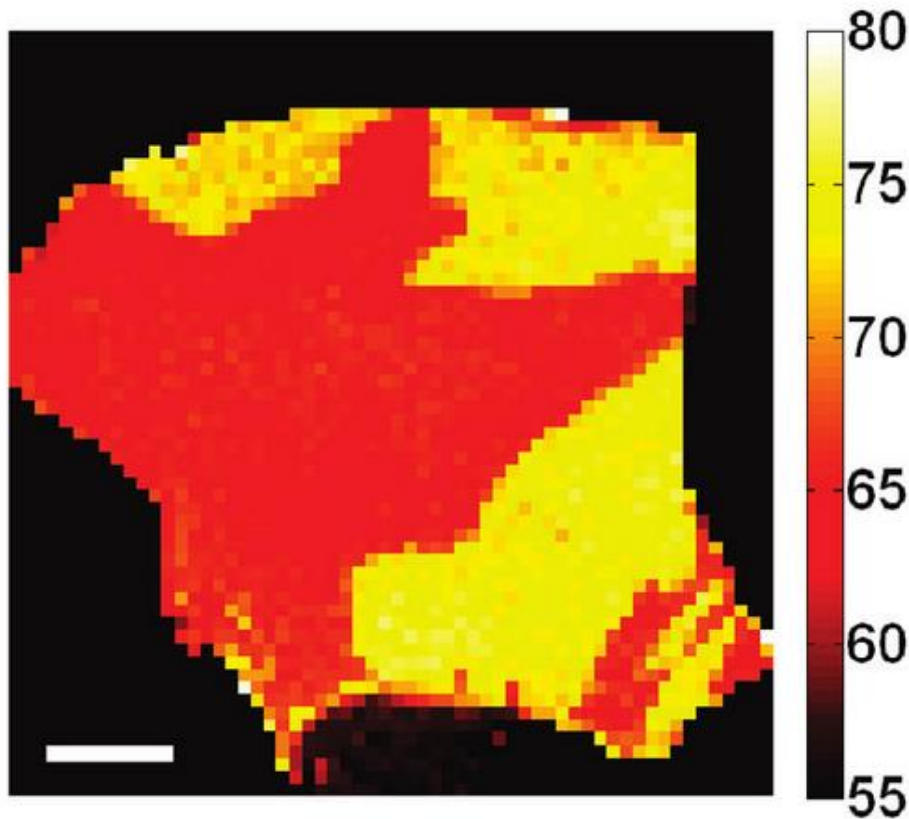
In addition to the twisted bilayer graphene project described in Chapter 4, I also participated in several collaborative projects with group members or other groups. In this chapter, I will briefly introduce my contribution in following works.

### 5.1 Scanning Tunneling Microscope Study of Trilayer Graphene

As previously introduced in Chapter 2, trilayer graphene (TLG) has two stable allotropes: Bernal stacked (ABA) and rhombohedral (ABC) stacked TLG. While ABA TLG remains metallic, ABC TLG exhibits a tunable band gap as a function of electric field. Such different electronic properties in TLG have been demonstrated in electrical transport [35,43] or optical measurements [44]. Yankowitz *et al* employ scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) to measure the samples of both ABA and ABC stacked trilayer graphene on Si/SiO<sub>2</sub> substrates [36]. This work was done in collaboration with Brian LeRoy group at University of Arizona, and I provided the ABA and ABC TLG devices.

Though ABA and ABC TLG are relatively stable, they often co-exist as domains within the same flake, as shown in Figure 5.1. It is relatively easier to obtain a purely ABA stacked TLG than ABC stacked TLG: it is reported that about 85% of the area in TLG flakes is ABA stacked while ABC stacking constitutes only 15% [45], which is

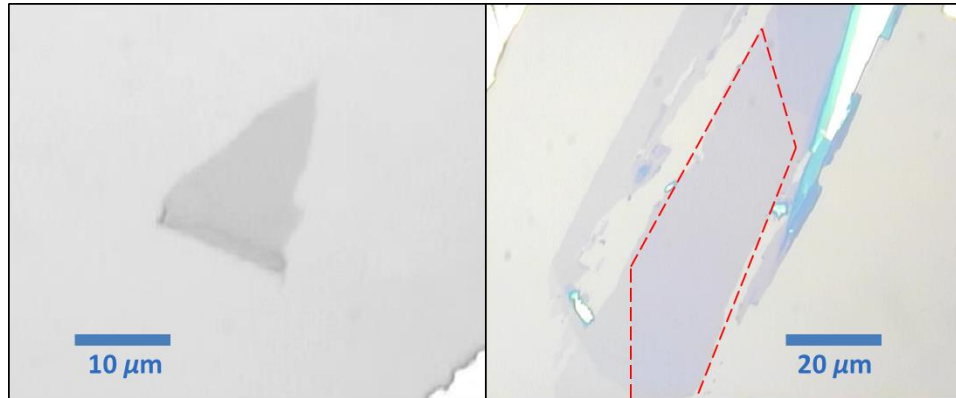
consistent with the fact that graphite typically contains ~80% Bernal-stacking, 14% rhombohedral stacking and 6% random (turbostratic) stacking [46].



**Figure 5.1.** Spatial map of ABA (red) and ABC (yellow) stacking in TLG. Scale bar: 10  $\mu\text{m}$ . Color shows the full width at half maximum of the 2D feature of Raman ( $\lambda=514\text{ nm}$ ) spectra [45].

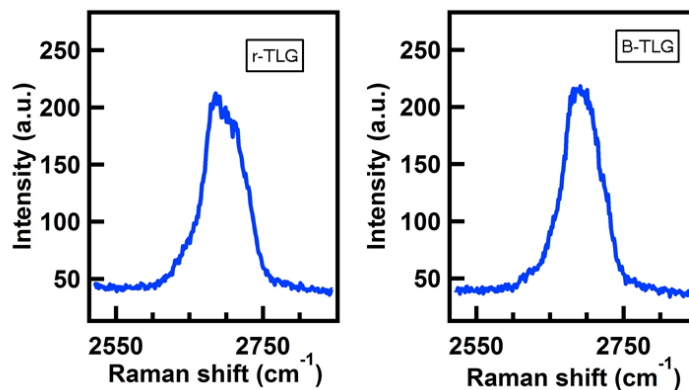
The typical scan area of STM studies is in the scale of tens of square nanometers. However, since the approach of an STM tip is often “blind”, large area samples  $\sim 10\text{-}20\ \mu\text{m}^2$  in size that have single stacking domains are needed. To this end, I use an exfoliation technique that is modified from the conventional ones and yields larger graphene flakes (see Chapter 7 for details). Graphene flakes are exfoliated onto Si/SiO<sub>2</sub> substrates, and TLG candidates are selected by color contrast in an optical microscope. Two optical

images of TLG flakes are shown in Figure 5.2. The stacking orders are unknown at this point.



**Figure 5.2.** Optical images of two typical TLG flakes on Si/SiO<sub>2</sub> substrate.

Raman spectroscopy is used to confirm the number of layers and identify the stacking orders of the TLG flakes. The Raman spectroscope we use is by Horiba LabRam and provides two wavelengths at 532 nm and 785 nm, respectively. All our spectra are taken using the 532 nm wavelength. There are distinctive differences between the 2D modes of the Raman spectra of ABA and ABC TLG from this wavelength. Figure 5.3 shows the 2D modes of the Raman spectra of both ABC and ABA TLG.

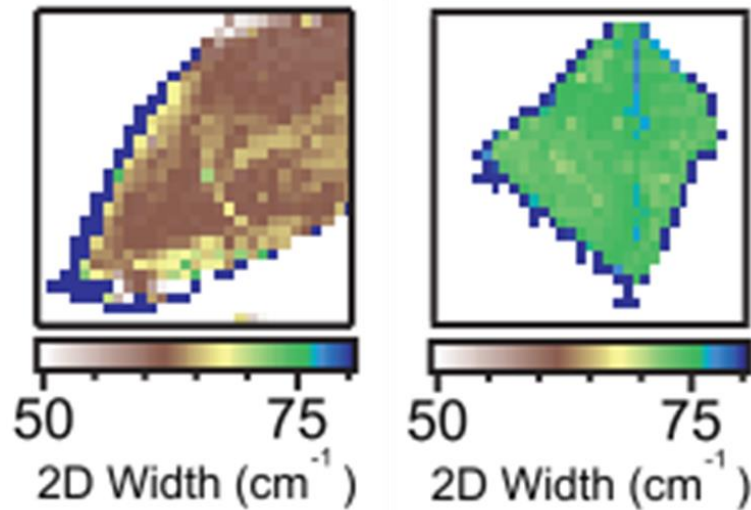


**Figure 5.3.** The 2D modes of the Raman spectra of ABC (left) and ABA (right) TLG, respectively.



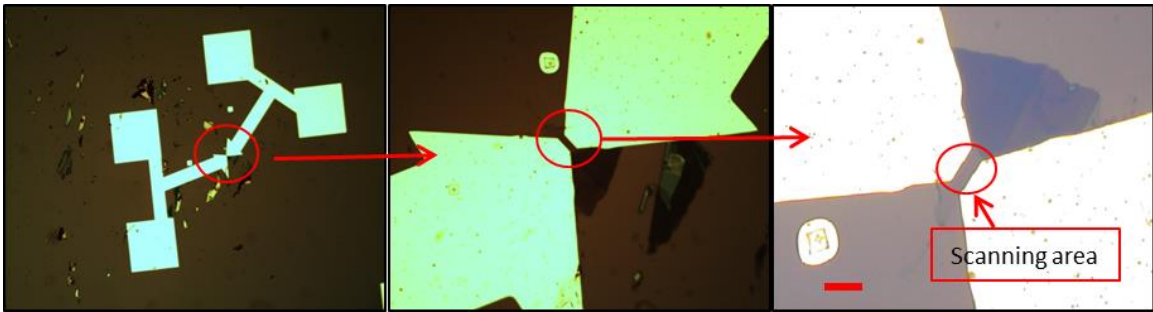
To search for ABA or ABC stacked TLG with a single domain, I randomly do Raman spectroscopy on several spots of a given TLG flake as a screening process. If the Raman shifts indicate that all spots have the same stacking order (either ABA or ABC), I will proceed to examine the entire flake. From my Raman data of ABA and ABC TLG, they appear in the similar ratio as previously quoted [46] -- ~80% of ABA and ~20% of ABC. Figure 5.4 shows two spatial mappings of ABA and ABC TLG respectively. The resolution of mapping is  $0.5 \mu\text{m} \times 0.5 \mu\text{m}$  per data point. From the raw data, we perform the analysis to extract and plot the full width at half maximum (FWHM) using a color scale. Based on these two spatial maps, the flakes have single ABA and ABC domains respectively.

The fabrication procedures and the device geometry are rather straightforward. After we have the flakes prepared, we perform the standard electron beam lithography to deposit



**Figure 5.4.** Spatial mapping of ABA (left) and ABC (right) TLG. Color scale indicates FWHM of the 2D mode of Raman spectra.

one layer of chromium/gold electrodes. The electrodes pattern is specially designed to help the STM to locate the scanning area. Before the measurements, the devices are treated by gas annealing [36]. Figure 5.5 shows the optical images of the devices.



**Figure 5.5.** Optical images of the devices in different magnifications. Scale bar: 5  $\mu\text{m}$ .

## 5.2 Suspension of Graphene without Acid Etching

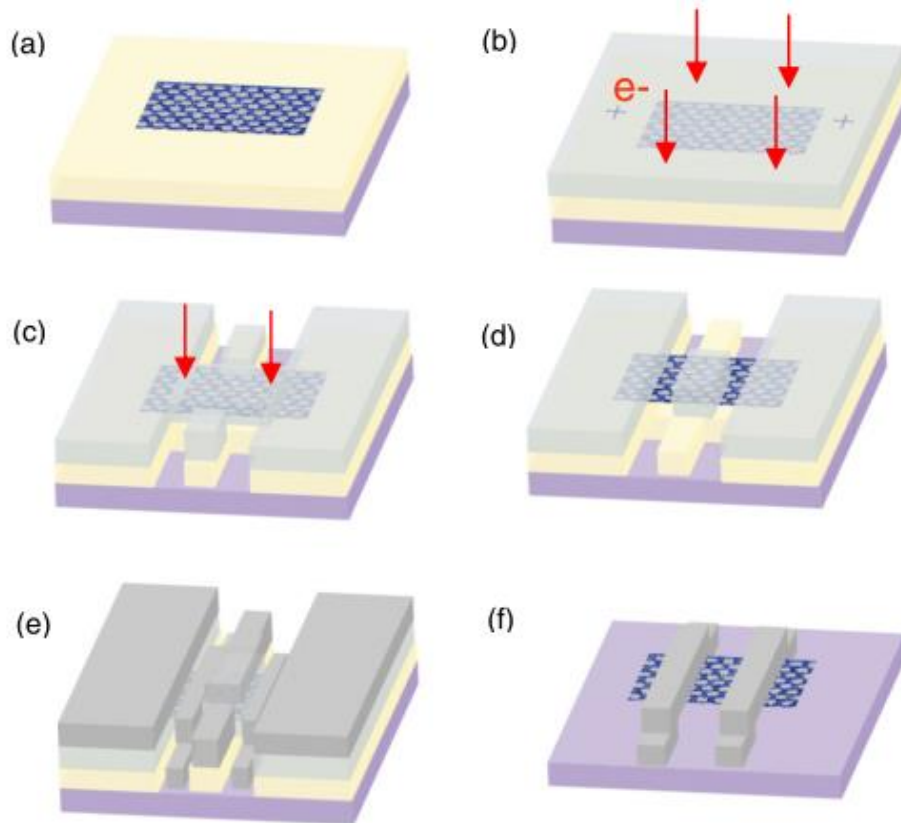
The conventional method to suspend graphene devices is wet etching (using buffered oxide etching), as described in Chapter 3. However, certain metals, such as aluminum and titanium, are unstable in buffered oxide etchant (BOE) or hydrofluoric acid (HF). For instance, this wet etching technique becomes unsuitable if aluminum is used as the electrode in certain projects, *e.g.* to study superconducting proximity effect in graphene.

A multistep fabrication technique is developed to suspend graphene flakes with arbitrary electrodes. This method is initiated by a former graduate student Jairo Velasco [47]. I fabricate many devices with this technique and provide feedbacks for adjusting parameters. The details about this technique are elaborated as following.

(a) Spin and bake a layer of lift-off resist (LOR) onto the standard Si/SiO<sub>2</sub> substrate. The parameters for spinning are: 300 rpm/s as acceleration, 3000 rpm spinning rate for 40 seconds. The chip is baked on the hotplate for 20 minutes at 170 °C. We then directly exfoliate graphene or other layered material onto LOR layer. (Figure 5.6 (a))

(b) Spin and bake another bilayer of methyl methacrylate and poly(methyl methacrylate) (MMA and PMMA) electron beam (e-beam) resists. We use 4000 rpm spinning speed and 10 minutes baking at 180 °C for each layer. Then, the first e-beam lithography (EBL) is written to generate alignment marks, which are used to locate the target graphene flake. Based on these alignment marks, we design the electrodes pattern for the subsequent steps of EBL. (Figure 5.6 (b))

(c) We perform the second EBL to open windows for the anchors of suspension electrodes. The MIBK (methyl isobutyl ketone) and IPA (isopropyl alcohol) mixture solution is used to develop exposed e-beam resist layer and MF319 is used to develop the LOR layer. After this step, the windows for the anchors of suspension electrodes are open and the SiO<sub>2</sub> substrate is exposed. (Figure 5.6 (c))



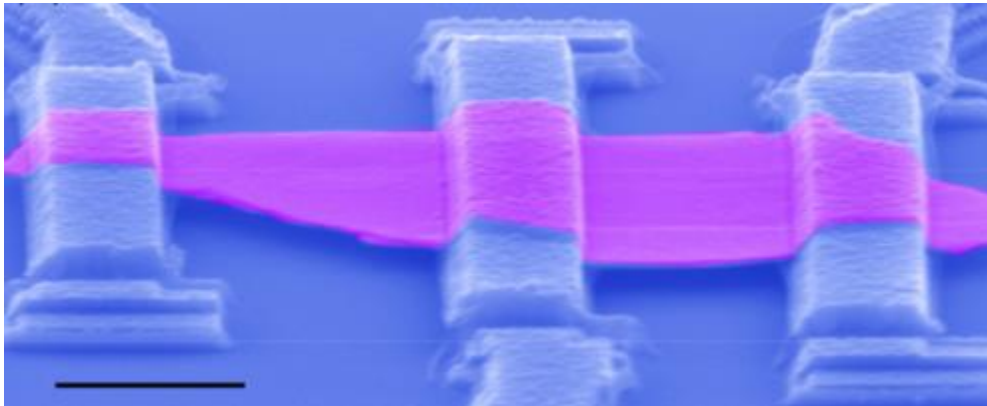
**Figure 5.6.** The schematics of the fabrication process. (a). Graphene on top of LOR. (b). Spin and bake of MMA/PMMA; Alignment marks and windows for anchors are developed. (c). Third EBL for bridge part of suspended electrodes. (d). Development and removal of exposed e-beam resist. (e). Three-angle metal deposition. (f). Lift-off and device drying; schematics of finished device.

(d) The third EBL is performed to expose the e-beam resists for the bridge part of the suspension electrodes, which are across the graphene flakes. After that, only e-beam resist layer is developed by MIBK/IPA. The underneath LOR layer remains. This process is illustrated from Figure 5.6 (c) to 5.6 (d).

(e) Metal deposition is done by e-beam evaporation. To enhance the robustness of the suspended electrodes, we use three-angle deposition. Ti/Al is deposited from  $+45^\circ$ ,  $-45^\circ$  and  $0^\circ$  respectively. (Figure 5.6 (e))

(f) In the final step of liftoff, we use Remover PG to dissolve all the remaining LOR and e-beam resists. A critical point dryer is used to dry the delicate device. The graphene flake should be held by the suspended electrodes (Ti/Al) and suspended above the SiO<sub>2</sub> substrate. (Figure 5.6 (f))

In addition to graphene, this technique can also be used to suspend other thin atomic layers. For instance, topological insulator Bi<sub>2</sub>Se<sub>3</sub> [48] is also a layered material and it can be exfoliated into thin membranes. To approve the versatility of this technique, we fabricated the suspended Bi<sub>2</sub>Se<sub>3</sub> device. Figure 5.7 shows that Bi<sub>2</sub>Se<sub>3</sub> thin crystal is suspended by this acid free technique.



**Figure 5.7.** Angled view of a suspended Bi<sub>2</sub>Se<sub>3</sub> device. Scale bar: 1  $\mu$ m.

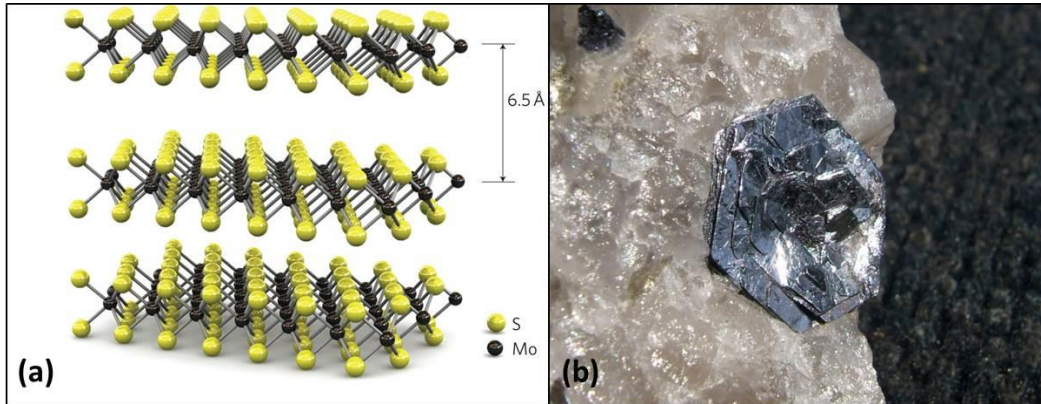
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## Chapter 6 Introduction to Few-layer Molybdenum

### Disulfide

#### 6.1 Introduction

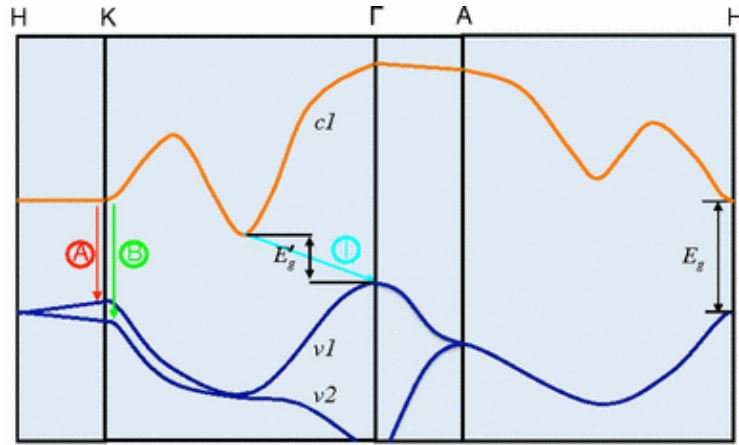
Molybdenum disulfide ( $\text{MoS}_2$ ) is a member of the family of transition metal dichalcogenides (TMDCs). TMDCs has chemical formulas  $\text{MX}_2$ , where M is a transition metal element from group IV, V, VI of the periodic table and X is one of the chalcogen elements, such as S, Se and Te [49,50]. Also, TMDCs often have layered structures, with strong intralayer chemical bonds but relatively weak interlayer van der Waals forces [49,50]. Figure 6.1 (a) shows the layered structure of  $\text{MoS}_2$ . The single layer thickness is  $\sim 0.65$  nm. From the side view, Mo atoms layer is sandwiched by two layers of sulfur atoms. From the top view, Mo and sulfur atoms connect to each other alternatively to form a hexagonal lattice.  $\text{MoS}_2$  has been one of the most studied TMDCs because of its availability in nature as molybdenite (Figure 6.1 (b)). Similar to graphite,  $\text{MoS}_2$  is widely used as a dry lubricant for its weak interlayer adhesion.  $\text{MoS}_2$  has also found applications in the fields of catalysis [51,52], photovoltaics [53,54] and batteries [55-57].



**Figure 6.1.** (a). The schematic of MoS<sub>2</sub> layer structure [58]. (b). Molybdenite in nature (picture from Wikipedia by John Chapman)

MoS<sub>2</sub> as a two-dimension material gains attention after the field of graphene research takes off. Though graphene is a promising candidate as a next generation electronic material, its crucial weakness is its gapless spectrum. Bandgap engineering of graphene has become an important research topic. Hence other two-dimensional materials with intrinsic bandgap, such as MoS<sub>2</sub> become increasingly popular. Bulk MoS<sub>2</sub> has an indirect bandgap  $\sim 1.2$  eV, and increases with decreasing thickness, to  $\sim 1.8$  eV in single layer where the band gap becomes direct [59]. Figure 6.2 shows the simplified band structure of bulk MoS<sub>2</sub>. Field effect transistors based on MoS<sub>2</sub> with large on/off ratio have been demonstrated [58]. However, charge mobility in MoS<sub>2</sub> is rather low, from 0.5 to 55 cm<sup>2</sup>/Vs [58,60].





**Figure 6.2.** Simplified band structure of bulk MoS<sub>2</sub>. *c1*: lowest conduction band; *v1* and *v2*: the highest split valence bands. *A* and *B* are the direct-gap transitions, and *I* is the indirect-gap transition.  $E_g'$  is the indirect gap for the bulk, and  $E_g$  is the direct gap for the monolayer [59].

## 6.2 Making Contacts to MoS<sub>2</sub> Devices

The differences between graphene and MoS<sub>2</sub> require many adjustments in sample preparation, fabrication and characterization procedures. The first difference is the electrodes-MoS<sub>2</sub> contact. Since MoS<sub>2</sub> is a semiconductor, the Schottky barriers at the interfaces between the metal electrodes and MoS<sub>2</sub> greatly increase the contact resistance. Therefore how to make the best contact becomes the prior question.

Schottky barrier is a potential barrier between the metal's Fermi energy and the conduction band (*n*-type semiconductor) or valence band (*p*-type semiconductor) of the semiconductor, due to the work function difference between the two. Different metals form barriers with different heights, leading to various device performances. Other factors such as the presence of resist residue can also adversely affect contact [61].

Much effort has been devoted to improve the electrode-MoS<sub>2</sub> contact. Gold, because of its large work function, is the first one to be experimented [58]. However, since gold needs an adhesion layer such as chromium or titanium, which makes the contact actually a mixture of both metals. Other metals such as nickel [62], scandium [63] and palladium [62,64] are all tested. Although various results on contact were claimed, the most commonly used metals in literature are still Ti/Au contacts, which are also used in our research.

Besides the metals, graphene is also used as a contact material [65], because it is highly conductive and reduces Schottky barrier formation due to its semi metallic nature. The graphene contact on MoS<sub>2</sub> greatly reduces the contact resistance.

### **6.3 Mobility Engineering**

MoS<sub>2</sub> has an intrinsic band gap, and unfortunately, relatively low mobility. The initially reported mobility of single layer MoS<sub>2</sub> is from 0.5 to 3 cm<sup>2</sup>/Vs [60]. The first single-layer MoS<sub>2</sub> transistor was made by the Kis group from Switzerland [58], which reported improved mobility of ~55 cm<sup>2</sup>/Vs by using high-κ dielectric of hafnium oxide as the gate dielectric.

Dielectric engineering is proven to be effective in improving the mobility of MoS<sub>2</sub> devices. Zhou group [66] from Wayne State University reported the mobility enhancement to ~100 cm<sup>2</sup>/Vs by immersing the device into a polymer electrolyte which

enhanced screening of charge impurities and reduced contact resistance. Fuhrer group from University of Maryland used polymethyl methacrylate (PMMA) as a substrate and observed a mobility enhancement to  $\sim 470 \text{ cm}^2/\text{Vs}$  for  $\sim 50 \text{ nm}$ -thick multilayer  $\text{MoS}_2$  [67].

Furthermore, several works aim at understanding the mobility bottleneck of  $\text{MoS}_2$ . Likely culprits include the Schottky barrier at the metal- $\text{MoS}_2$  interfaces, charge impurities and intrinsic defects of the  $\text{MoS}_2$  sheet. For instance, using proper metal contacts with suitable work functions will effectively reduce the barrier and improve mobility [63]. Charge impurities [68,69], possibly coming from the ambient environment adsorption or fabrication residues, increase scattering and degrade device mobility. Sulfur vacancies [70] are observed by several TEM studies [71-73]. Another source of scatterers is charge traps near the surface of  $\text{SiO}_2$  substrates, which constitute one of the main scattering mechanisms for graphene devices on  $\text{SiO}_2$  substrates.

## **6.4 Suspended Molybdenum Disulfide Device Structure**

The motivation of making suspended  $\text{MoS}_2$  devices is two-fold: (1). as dielectric engineering proves effective in improving mobility, removing dielectric material could prove informative; and (2). charge traps and corrugations from  $\text{SiO}_2$  substrates is well known to impede the mobility of low dimensional materials, thus removing  $\text{SiO}_2$  may improve device mobility.

Works on suspended or free-standing MoS<sub>2</sub> devices are limited, and mostly focused on their optical [59,74] or mechanical [75,76] properties. Devices are typically fabricated by direct exfoliation on or transfer over pre-patterned trenches or holes on the substrates. Only one paper reported the electrical transport by the end of 2014, using the wet etching method though the mobility is rather low,  $\sim 0.9 \text{ cm}^2/\text{Vs}$  [77].

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## Chapter 7 MoS<sub>2</sub> Device Preparation and Fabrication

In this chapter, I will describe the MoS<sub>2</sub> sample preparation including exfoliation, flake characterization and the detailed fabrication procedures.

### 7.1 MoS<sub>2</sub> Sample Preparation

#### 7.1.1 Substrate Preparation

We use standard Si/SiO<sub>2</sub> substrates with the following parameters: 4 inch size in diameter, *p*-type doping with boron as dopant, crystalline orientation <100>, thickness about 525 μm, low resistivity 0.01~0.02 Ω·m, 300 nm thermal oxide layer on one side, single side polished prime grade wafer. The wafers are diced by the UC Irvine Nanofabrication Facility into 4 mm × 4 mm chips. Figure 7.1 shows the images of a 4-inch wafer, the diced wafer and the cleaned small chips.



**Figure 7.1.** (a). 4 inch Si/SiO<sub>2</sub> wafer. (b). Laser-diced small chips with protective coating layer. (c). Clean square chips.

The wafers are cleaned immediately before exfoliation. (1) Put the chips into a beaker with acetone, then sonicate for about 20 minutes; (2) Transfer them into a beaker

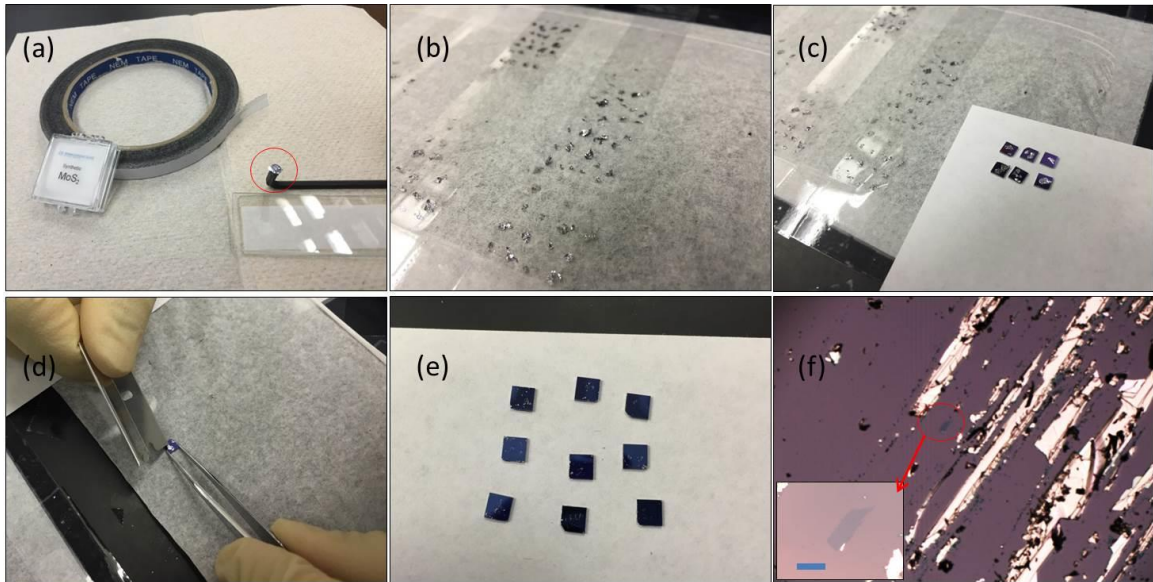
with high quality IPA (isopropyl alcohol) and soak for ~5 minutes. (3) Use the squirt bottle with high quality IPA to rinse every chip, and then dry with N<sub>2</sub> gas.

### 7.1.2 Exfoliation

We first attempted the tape exfoliation technique [1]. However, the yield of suitable MoS<sub>2</sub> flakes is low; and it is particularly difficult to obtain sufficiently large monolayer flakes by this method. We then switched to another mechanical exfoliation technique, “scratching exfoliation” [78], which was developed by our former group member Wenzhong Bao. The detailed procedures are described as following.

- (1) Find a stick with a flat end; attach a piece of double-side tape to the end.
- (2) Place a small piece of bulk MoS<sub>2</sub> bulk onto the tape, and make sure the tape is fully covered. Once the piece of bulk MoS<sub>2</sub> no longer covers the tape, it needs to be replaced. See Figure 7.2 (a).
- (3) Use the stick to tap the bulk MoS<sub>2</sub> on a piece of scotch tape up. Freshly exfoliated, very thin pieces of MoS<sub>2</sub> will be available for picking up. See Figure 7.2 (b)
- (4) Use sharp tweezers to pick up the thin pieces of bulk MoS<sub>2</sub> and attach them onto a clean chip. It is very critical the flakes are so thin that they are very soft and adhere well to the chips’ surfaces. See Figure 7.2 (c).
- (5) Use a clean and sharp razor to scratch along the chip surface. A great amount of practice is needed here to peel the bulk MoS<sub>2</sub> well without damaging the surface of the substrate. See Figure 7.2 (d). The chips afterwards are shown in Figure 7.2 (e).

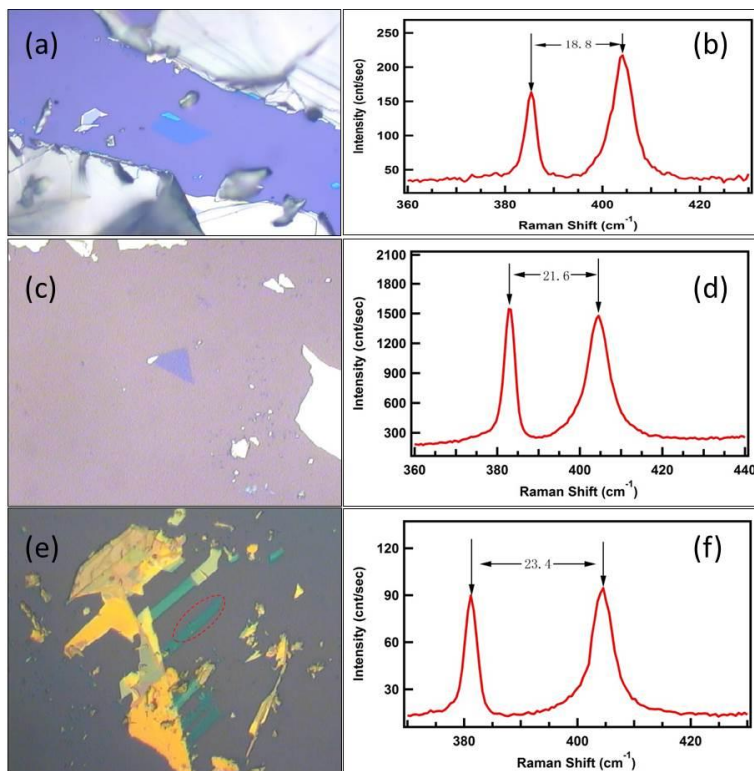
- (6) Search and locate the few-layer MoS<sub>2</sub> using optical microscope. Usually the few-layer MoS<sub>2</sub> flakes are around the area where it is scratched. See Figure 7.2 (f).



**Figure 7.2.** (a). Tools and materials for exfoliation; the red circle shows the MoS<sub>2</sub> piece. (b). Freshly separated thin pieces of bulk MoS<sub>2</sub> on the tape. (c). Transferred thin pieces on the clean chips. (d). Use a razor to scratch the MoS<sub>2</sub> adhered on substrate. (e). Finished chips with very little bulk MoS<sub>2</sub> left, and ready to be examined. (f). A typical optical microscope picture of post-exfoliation sample.

### 7.1.3 Flake Characterization

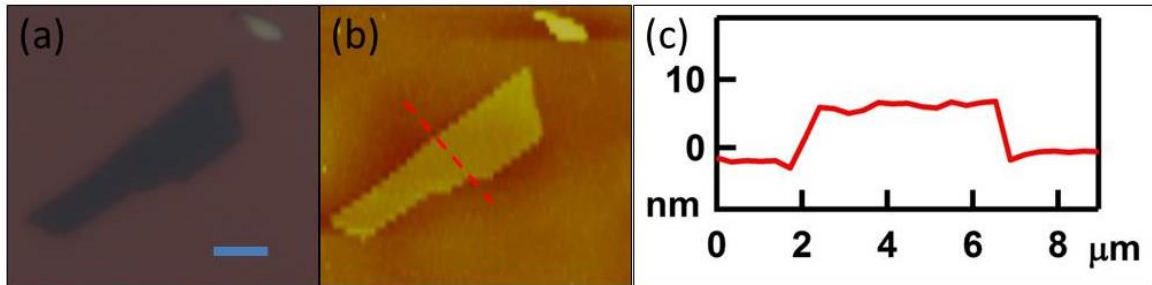
After we find a desirable flake in optical microscope, we use Raman spectroscopy (Horiba LabRam, 532 nm wavelength) to identify monolayer, bilayer and trilayer MoS<sub>2</sub> sheets, and atomic force microscope (AFM) to measure the thickness of thicker flakes. Also, we take Raman or AFM measurements as quickly as we can to minimize the flake exposure to ambient environment, because exposing to the air will degrade the flake quality based on both our experimental experience and other reports [79,80]. Figure 7.3 shows the optical images and corresponding Raman spectra of monolayer, bilayer and trilayer MoS<sub>2</sub> flakes.



**Figure 7.3.** Optical images and Raman spectra of monolayer (a-b), bilayer (c-d) and trilayer (e-f) MoS<sub>2</sub> samples.

MoS<sub>2</sub> could be easily damaged by a focused laser spot [81,82]. Therefore, for Raman spectroscopy on MoS<sub>2</sub>, we use a 1.0 filter (attenuator) to reduce laser power by 90%. Also, the acquisition time is 2 seconds and we only accumulate twice for one spectrum. We note the spot that is exposed to the laser beam, and avoid this local area for the subsequent device fabrication.

For flakes thicker than three layers, AFM is used to measure their thickness and flatness. Relative flat areas are selected for the device fabrication. Figure 7.4 shows a typical AFM image and corresponding height information.



**Figure 7.4.** (a). Optical image of a few-layer MoS<sub>2</sub> flake. Scale bar: 5 μm (b). AFM image of the same flake; the red dash line shows the height profile in next panel (c).

## 7.2 Device Fabrication

To make suspended MoS<sub>2</sub> devices, we use wet etching method to release the sacrificial layer SiO<sub>2</sub>. Titanium makes good contact to MoS<sub>2</sub>, however, it doesn't survive this wet etching method. Thus a second layer of chromium and gold combination is deposited to protect the titanium contact from being etched. The procedures are:

- (1) Spin-coating electron beam (e-beam) resist.

We spin two layers of e-beam resists on top of the target flake. The spin coater used in our lab is Laurell WS-650MZ-23NPP model (Figure 7.5), and the resist is 950 PMMA (polymethyl methacrylate) A4. The programmed recipe for spin-coating PMMA is: 4000 rpm for 40 seconds, ramping rate (up and down) is 1000 rpm/s. Each layer of PMMA is heated at 180 °C for 10 minutes after spin-coating.



**Figure 7.5.** Laurell spin coater.

(2) First EBL for alignment marks.

After the spin-coating, we perform the first EBL for the alignment marks. The equipment we use for EBL is LEO SUPRA 55. A little silver paste is put on the surface of the resist to help the focus. Then, we write the standard alignment marks pattern around the target flake. After e-beam writing, the sample is developed in MIBK:IPA 1:3 for 65 seconds.

(3) Second EBL for electrodes pattern.

We design the pattern of the electrodes of our devices using Design CAD LT 2000, and use EBL to expose the pattern on the old resists spun in step (1). For smaller features, we use small aperture  $20\ \mu\text{m}$ , which gives better resolution but runs slower. For larger features like bonding pads, we use  $120\text{-}\mu\text{m}$  size aperture.

After the exposure, the sample is developed in MIBK:IPA 1:3 for 65 seconds again.

(4) Metal deposition and lift-off.

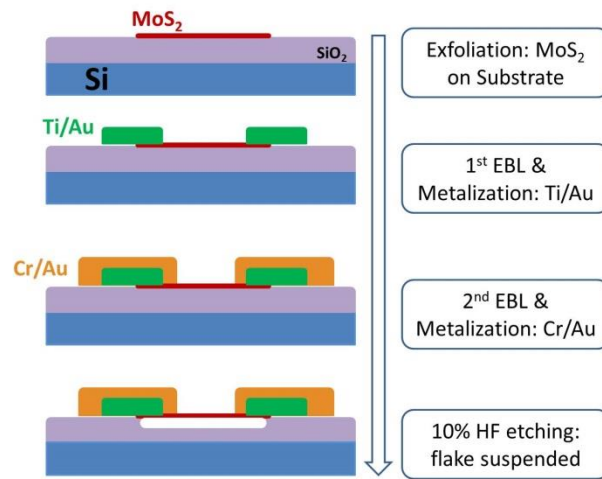
We deposit metals using electron beam evaporator (Temescal BJD 1800 system). Typically 10 nm of titanium and 60 nm of gold are deposited as electrodes. Then we immerse the device in acetone and heat it at 65 °C for more than one hour, to dissolve the rest of e-beam resist and lift off the rest of metal pieces.

(5) Adding another layer of metals.

To protect the titanium contacts from subsequent wet etching, we repeat steps (1) and (3-4) to add a second layer of chromium and gold that surrounds the titanium contact layer.

(6) Wet etching and sample drying.

With the protection layer, we use 10% hydrofluoric acid to etch SiO<sub>2</sub> for 60 seconds during which about 120 nm SiO<sub>2</sub> will be etched. We do not use buffered oxide etchant (BOE) because it appears to etch MoS<sub>2</sub>. After etching, the sample is dried in critical point dryer (CPD).



**Figure 7.6.** The schematics of the lithography procedures of fabricating suspended MoS<sub>2</sub> devices.



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## **Chapter 8      Annealing and Transport Properties of Suspended MoS<sub>2</sub> Devices**

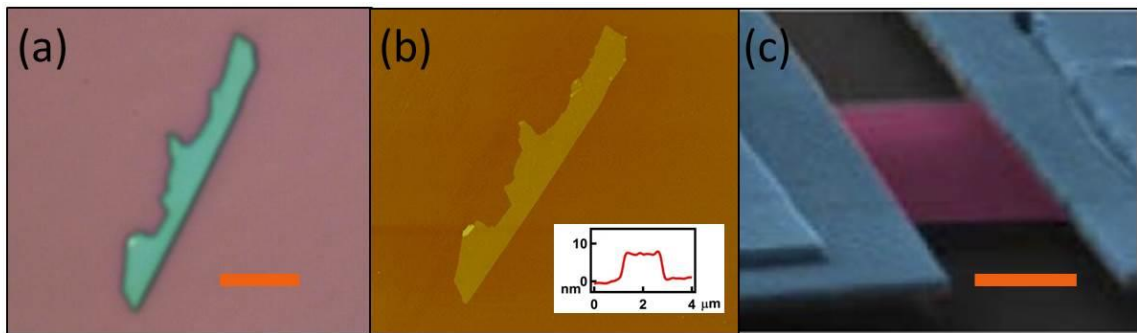
One common source of mobility impediment is the substrate, which can locally dope the few-layer atomic membranes, induce local corrugations and strains, and introduce scatterers such as charged impurities and surface phonons. Particularly, Si/SiO<sub>2</sub> substrates, on which the vast majority of MoS<sub>2</sub> devices are fabricated, are notoriously known for their propensity to trap charges. Using alternative dielectrics or substrates such as high- $\kappa$  dielectric [58] HfO<sub>2</sub> or PMMA [67] may improve mobility; however, the suspended MoS<sub>2</sub> devices can reveal the effect of substrates.

Previous work on other nano-materials such as graphene and carbon nanotubes have shown that removing substrates could yield exceedingly high mobility devices, allowing observation of novel phenomena such as Wigner crystallization [83] and Mott insulating state [84] in nanotubes, fractional quantum Hall state in graphene [14-16] and interaction-induced insulating state in bilayer graphene [85] and ABC-stacked trilayer [35].

In Chapter 6 and 7, I introduced the background of few-layer MoS<sub>2</sub> devices and the detailed fabrication procedures of suspended MoS<sub>2</sub> devices. In this chapter, I will present transport data and discuss the results.

## 8.1 Annealing Technique

Flakes with different thicknesses, which range from single layer  $\sim 1$  nm to multilayer sheets  $\sim 20$  nm, are mechanically exfoliated by the razor method. An optical image and atomic force microscope (AFM) image of a typical few-layer MoS<sub>2</sub> sheet are displayed in Figure 8.1. They are coupled to electrodes and suspended as described in Chapter 7. A SEM image of a suspended device is presented in Figure 8.1 (c).



**Figure 8.1.** (a-b). Optical and AFM images of a typical few-layer MoS<sub>2</sub> sheet, scale bar: 5  $\mu$ m. Inset: height profile indicates 8 nm thickness. (c). SEM image of a suspended MoS<sub>2</sub> device, scale bar: 1  $\mu$ m.

To remove resist residues and improve device performance, we first attempted current annealing [42], *i.e.* Joule heating by driving a current through the device. This annealing technique has been demonstrated to yield very high mobility for suspended graphene samples [86-88]. However, we find that current annealing has little or no effect on our suspended MoS<sub>2</sub> samples.

Another commonly used technique is gas annealing, typically using formic gas at an elevated temperature [58,72,80,89-94] to reduce the organic residue and contact resistance. However, there is much variation among the protocols, and except for

reference [58], no quantitative comparison of the device performance before and after annealing. The detailed annealing protocols and results are summarized in Table 8.1.

Here, we have experimented with different annealing recipes by varying the gas flow rate, annealing temperature and the annealing time. Each recipe was at least tested on two devices. Some of the procedures and results are summarized in Table 8.2. Finally, we find that satisfactory results are achieved via annealing in 600 sccm argon and 20 sccm hydrogen at 200 °C for about 40 minutes. Importantly, the devices can be damaged by higher temperature, longer annealing time or higher hydrogen flow rate. We note that our work demonstrates the biggest improvement in device performance after annealing.

**Table 8.1.** Annealing protocols and results.

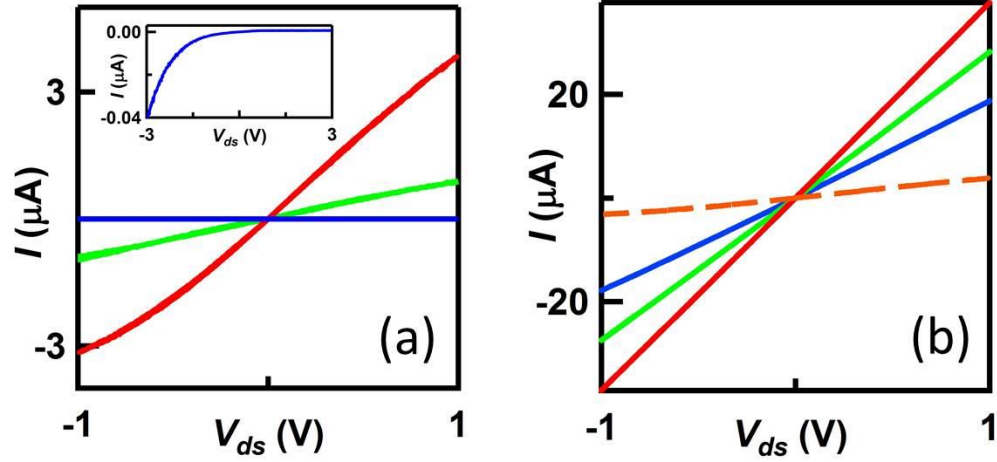
Reference	Gases	Temperature( °C)	Annealing time (hour)	Results
[58]	Ar 100 sccm: H <sub>2</sub> 10 sccm	200	2	“a factor of 10 resistance decrease” for Au contact; no effect for Ti contact
[91]	Ar 100 sccm: H <sub>2</sub> 10 sccm	200	2	--
[72]	Ar: H <sub>2</sub>	300(for contact)	--	--
[72]	Ar: H <sub>2</sub>	200(for TEM)	--	--
[93]	Ar only	200	2	--
[92]	100 sccm Ar only	200	--	--
[80]	Ar: H <sub>2</sub>	400	--	--
[94]	Ar 600 sccm: H <sub>2</sub> 30 sccm	350	3	--
[90]	Ar 500 sccm: H <sub>2</sub> 100 sccm	300	2	--
[89]	Ar: H <sub>2</sub>	350	3	No effect
[This work]	Ar 600 sccm: H <sub>2</sub> 20 sccm	200	0.67	10 <sup>4</sup> times improvement in conductance

**Table 8.2.** Attempted annealing protocols and results.

Attempted Recipes	Ar/H <sub>2</sub> flow rate (sccm)	Temperature( °C)	Time	Results
1st	600/30	300	2 hours	flake broken
2nd	600/20	200	2 hours	no results observed
3rd	600/30	200	40 minutes	improved conductance
4th	600/20	200	~ 40 minutes	repeated improved results

## 8.2 Annealing Results

To investigate the effect of gas annealing, we measure the electrical properties of devices before and after annealing. The as-fabricated devices are characterized immediately after the critical point drying. Typical data sets at  $T=300\text{K}$  are shown in Figure 8.2 (a), which displays the current-voltage ( $I$ - $V$ ) characteristics from a 17 nm thick MoS<sub>2</sub> sample at  $V_{\text{bg}}=0, 10, 20\text{V}$ , respectively. More data from additional samples are shown in following figures. The  $I$ - $V$  curve at  $V_{\text{bg}}=0$  is also shown in the inset with reduced current range. Clearly, the device performance is very poor -- the two-terminal conductance  $G$  is about 13 nS at  $V_{\text{bg}}=0$ . Most of our devices exhibit little hysteresis; larger hysteresis observed in a few devices is likely related to the adsorption of water and other contaminants on MoS<sub>2</sub> surface [95].



**Figure 8.2.** (a).  $I$ - $V$  characteristics of as-fabricated device at  $V_{bg}=0$ (blue), 10V(green), 20V(red) respectively. Inset:  $I$ - $V$  at  $V_{bg}=0$  with reduced current range. (b).  $I$ - $V$  characteristics after gas annealing at  $V_{bg}=0$ (blue), 10V(green), 20V(red) respectively. Orange dashed line corresponds to the red curve in Figure 8.2 (a).

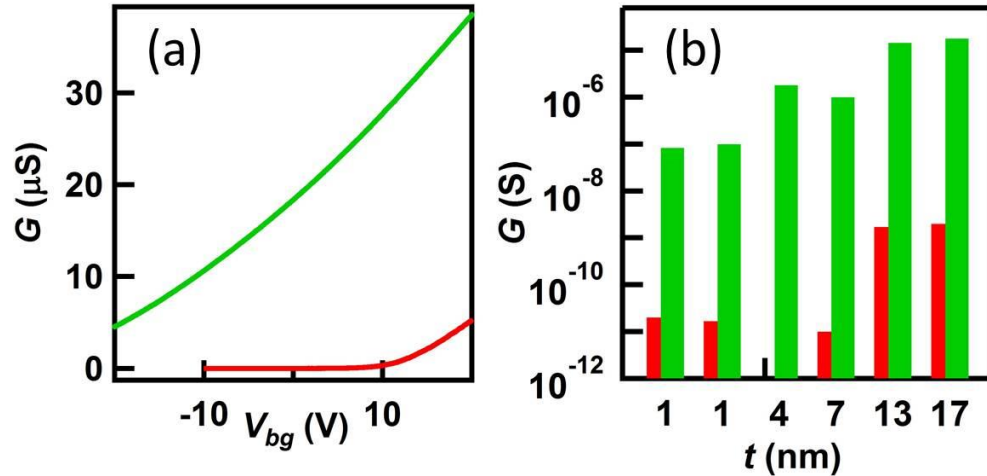
Naively, one expects suspended devices to have higher mobility, due to removal of substrates that induce scatterers, trapped charges and corrugations. However, we have fabricated more than thirty suspended MoS<sub>2</sub> devices, and their average field effect mobility ranges from 0.01 to 46 cm<sup>2</sup>/Vs. The mobility is calculated based on the equation,

$$\mu = \frac{1}{V_{ds}} \frac{\Delta I}{\Delta V_{bg}} \frac{L}{W} \frac{1}{C_g},$$

where the gate capacitance per unit area  $C_g$  can be estimated by using the

parallel plate geometry. Using two dielectric layers (180 nm SiO<sub>2</sub> and 120 nm vacuum) connected in series; we estimate that  $C_g \sim 5.3 \times 10^{-5}$  F/m<sup>2</sup>. We note that the two-terminal geometry of our devices does not permit Hall mobility measurements; however, assuming that the contact resistance is independent of  $V_{bg}$ ,  $\mu$  is a reasonable indication of the devices' channel mobility. We note these mobility values are considerably lower than those of standard substrate-supported devices. Such mobility degradation is very likely due to the additional resist residues from two-step lithography procedures. Thus without

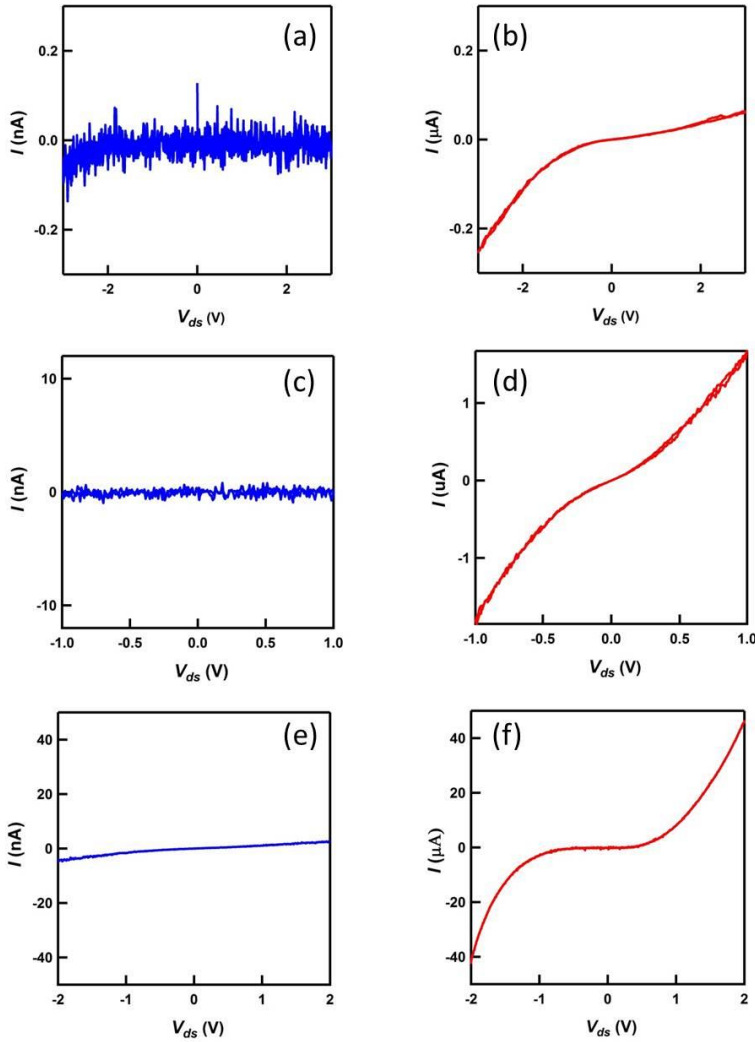
an effective annealing method, as-fabricated suspended MoS<sub>2</sub> devices are less than ideal for electronic applications.



**Figure 8.3.** (a).  $G(V_{bg})$  of the device before (red curve) and after (green) gas annealing. (b). Comparison of conductance before (red) and after (green) gas annealing in samples with different thickness. (Conductance of this 4 nm-thick device before annealing happens to be below the measurement's noise floor ( $<10^{-11}\text{S}$ ), though such low conductance is not thickness-related)

After gas annealing, the  $I$ - $V$  characteristics of the same device at  $T=300\text{K}$  and different  $V_{bg}$  are displayed in Figure 8.2 (b). For comparison, the pre-annealing  $I$ - $V$  at  $V_{bg}=20\text{V}$  is also plotted as the orange dashed line. The device conductance is enhanced dramatically: at  $V_{bg}=0$ ,  $G$  increases from 13 nS before annealing to 18  $\mu\text{S}$  after annealing. Figure 8.3 (a) plots  $G(V_{bg})$  for the device before (red curve) and after (green curve) annealing. The mobility is improved from 46 to 105  $\text{cm}^2/\text{Vs}$ . Such improvement in conduction and mobility after gas annealing is quite robust, and observed across a number of samples of different thicknesses. As shown in Figure 8.3 (b), six devices with thicknesses ranging from 1 nm to 17 nm all exhibit  $10^4$  times improvement in conductance after the gas annealing.

Additional  $I$ - $V$  characteristics of different devices at  $V_{bg}=0$  showing the annealing effect are listed below. Blue curves at the left side and red curves at the right side show data of as-fabricated and post-annealing devices, respectively.



**Figure 8.4.** (a). (c). (e). Left panels display  $I$ - $V$  of as-fabricated devices with 1 nm, 4 nm, 13 nm thickness respectively.  $V_{bg}=0$ , Unit: nA. (b). (d). (f). Right panels display  $I$ - $V$  of the same devices after annealing,  $V_{bg}=0$ . Unit:  $\mu$ A



### 8.3 Temperature Dependent Transport Data

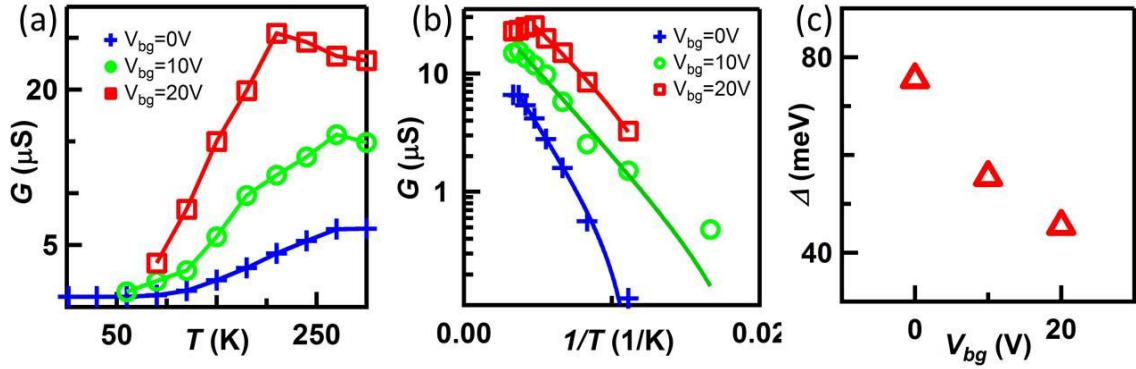
To explore the temperature dependence of the device's transport properties, we measure the device in a He<sup>4</sup> variable temperature cryogenic system. Figure 8.5 (a) presents the device conductance *vs.* temperature *T* at different gate voltages. All data is taken at 10 mV source-drain bias. All three data sets exhibit the same trend: as *T* decreases, the conductance first increases slightly, and then decreases. At large gate voltages, this trend is particularly evident, and the conductance peak shifts to lower temperatures. We attribute this non-monotonic *G(T)* dependence to competition between two scattering processes: electron-phonon scattering that inversely scales with *T* and dominates at high temperature [96,97], and scattering from charged impurities that dominates at low temperature [93]. At higher charge density, effective screening leads to reduced impurity scattering, thus causing the crossover temperature between these two regimes to shift to lower temperatures.

To investigate the transport mechanism at low temperatures, we replot the data in Figure 8.5 (a) as an Arrhenius plot in Figure 8.5 (b). All data points with positive *dG/dT* fall on a straight line, indicating transport via thermal activation. We can extract the thermal activation gap size by fitting the data to the equation:

$$G = G_0 \exp\left(-\frac{\Delta}{2k_B} \cdot \frac{1}{T}\right) \quad (8.1)$$

where  $\Delta$  is the activation barrier height. From the data, we obtain  $\Delta=46, 56$  and  $76$  meV, for  $V_{bg}=0, 10$  and  $20$ V, respectively. Figure 8.5 (c) plots  $\Delta$  as a function of  $V_{bg}$ ; as the device becomes more *n*-doped, the activation energy decreases. This barrier may be the

Schottky barrier at the electrode-MoS<sub>2</sub> interface, and/or the barrier between nearest neighbor hopping sites.



**Figure 8.5.** (a).  $G(T)$  data of the device at  $V_{bg}=0$ (blue), 10V(green), 20V(red), respectively. (b). Same data in (a) plotted as  $G$  versus  $1/T$ . The solid lines are fits to equation (8.1). (c). Extracted activation barrier height versus gate voltage.

## 8.4 Discussion and Conclusion

Since the mobility of our suspended devices after annealing are not significantly higher than that of substrate-supported devices, we exclude substrate as the mobility bottleneck in these devices. Instead, other mobility limitations such as defects [61,72,98,99], Schottky barriers [63], impurities [68,69] and corrugations may be significant, and a combination of these factors is likely the reason for the low mobility in MoS<sub>2</sub> FET devices. Further work would be warranted to ascertain the dominant mechanism. Another limitation of the suspended devices is the relatively small range of charge density that can be induced. Due to the limited range of gate voltage applied and

the smaller capacitive coupling between the sample and the back gate, most devices are not turned “on” and/or “off” completely.

In summary, we successfully fabricated suspended MoS<sub>2</sub> FET device by wet etching, and developed an effective gas annealing technique that significantly improves device quality. We observed the two different temperature regimes corresponding to different transport mechanisms: close to room temperature, electron-phonon coupling appears to dominate transport; at lower temperatures, transport occurs via thermal activation over a band gap that is tunable by gate voltage. Lastly, our suspended MoS<sub>2</sub> device structure provides a versatile platform for investigating other less-explored properties and applications of MoS<sub>2</sub>, such as thermal expansion, strain engineering, nanomechanical resonators and chemical sensors.

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## Chapter 9      Ionic Liquid Gating on Suspended MoS<sub>2</sub>

### Devices

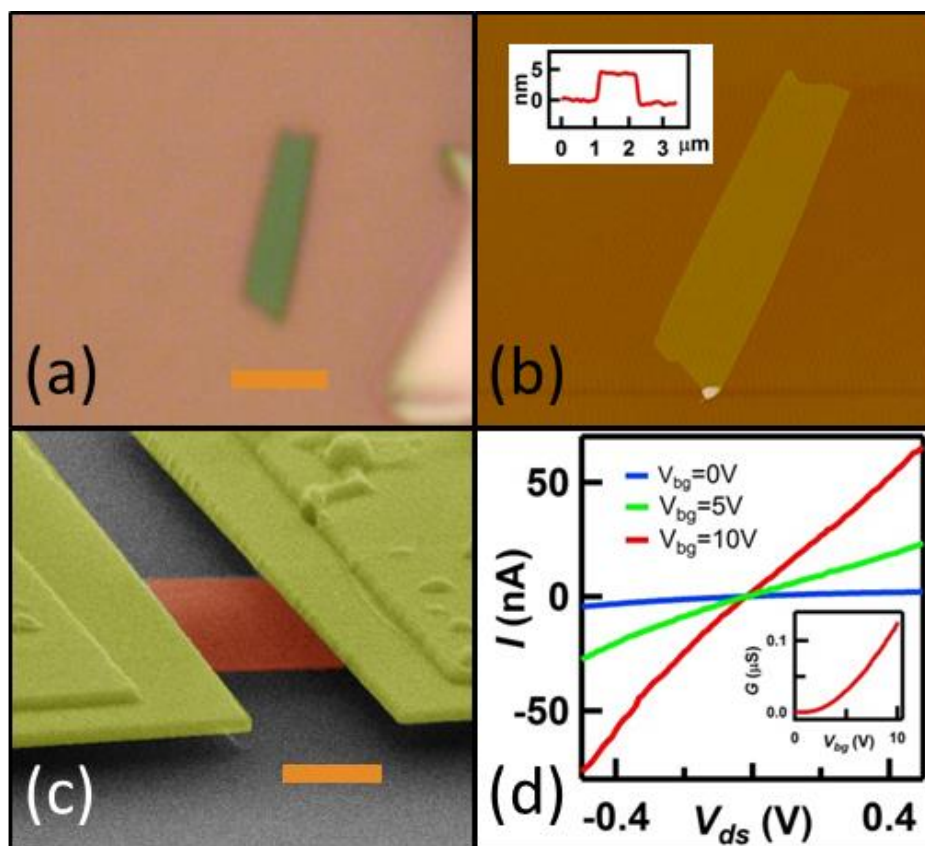
As described in last two chapters, we fabricated and characterized suspended MoS<sub>2</sub> devices. The minimal improvement in mobility leads us to conclude that the Si/SiO<sub>2</sub> substrates are not the mobility bottleneck. Here we seek to modify the device behaviors in a different way -- by using ionic liquid as an electrolyte gating on suspended MoS<sub>2</sub> samples, we modify the dielectric environment as well as achieve extremely high charge density.

Ionic liquid is a liquidized salt at room temperature, and contains separable and mobile cations and anions. The ionic liquid gating has been demonstrated as an effective gating method on many different materials [100-106]. Under an externally applied voltage, the ions in the liquid will separate and a layer of cations or anions accumulates on the sample surface, forming an electric double layer (EDL) that is essentially a nanogap capacitor with huge capacitance. The coupling efficiency is usually orders of magnitude larger than that of conventional silicon back gate. Superconductivity induced by the exceedingly high charge density (up to  $10^{14}$  cm<sup>-2</sup>) under ionic liquid gating has been achieved in 20 nm-thick molybdenum disulfide (MoS<sub>2</sub>) flakes [103]. Ionic liquids usually have a relatively high dielectric constant [107]. Combining the high doping efficiency and its high- $\kappa$  nature, MoS<sub>2</sub> field effect transistor device with ionic liquid gating presents an interesting topic of research.



Few-layer MoS<sub>2</sub> flakes are mechanically exfoliated onto Si/SiO<sub>2</sub> substrates from the bulk material (source: synthetic crystal from 2D Semiconductors), and their thicknesses are determined by atomic force microscope (AFM) and/or Raman spectroscopy. Figure 9.1 (a-b) shows an optical and an AFM image of a 5 nm MoS<sub>2</sub> sheet. The MoS<sub>2</sub> sheet is coupled to titanium/gold electrodes that are covered by a thin protective layer of chromium [108], released from the SiO<sub>2</sub> layer via wet etching in hydrofluoric acid, and dried in a critical point dryer. The width and length of the devices are 2.0 and 0.9  $\mu\text{m}$ , respectively. A “side gate” lead that is separated from the MoS<sub>2</sub> sheet by 20  $\mu\text{m}$  acts as the counter electrode for the ionic liquid. A scanning electron micrograph of a suspended device is shown in Figure 9.1 (c).

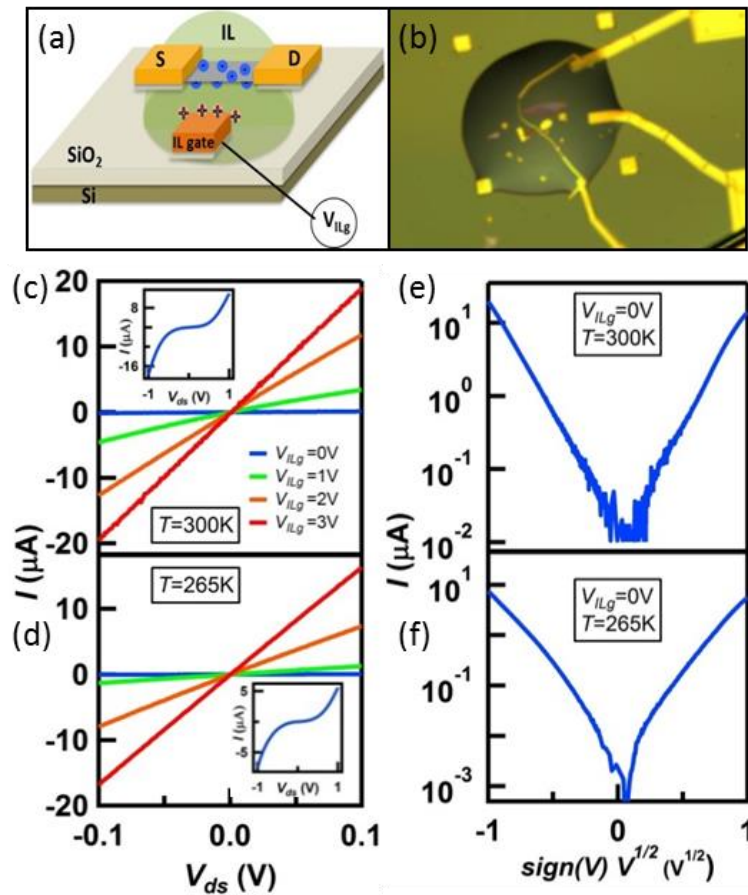
The as-fabricated devices are characterized in vacuum at room temperature. Figure 9.1 (d) displays the current voltage ( $I$ - $V$ ) characteristics of a typical device at different back gate voltages  $V_{bg}$ . The as-fabricated device is highly resistive -- at  $V_{bg} = 10\text{V}$ , its two-terminal resistance is  $\sim 10\text{M}\Omega$ ; from the conductance dependence on back gate voltage  $V_{bg}$  (Figure 9.1 (d) inset), the field-effect mobility is estimated to be  $\sim 2.1 \text{ cm}^2/\text{Vs}$ . In fact, for all as-fabricated devices that are characterized, the mobility values at 300K are quite limited, ranging 0.01 to  $10 \text{ cm}^2/\text{Vs}$ .



**Figure 9.1.** (a-b). Optical and AFM images of a typical few-layer MoS<sub>2</sub> Sheet, scale bar: 2 μm. Inset: height profile indicates 5 nm thickness. (c). SEM image of a suspended MoS<sub>2</sub> device, scale bar: 1 μm. (d). *I-V* characteristics of as-fabricated devices (no IL) at  $V_{bg}=0$ (blue), 5V(green), 10V(red) respectively. Inset:  $G(V_{bg})$  Conductance versus back gate voltage.

After the initial characterization, an ionic liquid (IL, DEME-TFSI from Kanto Chemical Co) droplet is deposited on the device. A schematic illustration of the IL-covered device is shown in Figure 9.2 (a), and an optical image Figure 9.2 (b). Compared to as-fabricated devices, addition of IL invariably improves the device performance -- even without applying any voltage to the counter electrode, the conductance typically increases by a factor of  $10^3$  or  $10^4$ . Mobility is also improved, albeit by to a lesser extent, to 46 cm<sup>2</sup>/Vs. Such dramatic improvement in conduction strongly suggests that IL

screens and modifies the Schottky barrier at the metal-semiconductor interfaces, which constitute the conduction bottleneck in as-fabricated devices. The improvement in mobility indicates that charge impurities are screened by the close proximity of IL, thus reducing the electron scattering.



**Figure 9.2.** (a-b). Schematics and optical image of ionic liquid gating on suspended device. (c-d).  $I$ - $V$  characteristics at  $V_{ILg}=0$ (blue), 1V(green), 2V(orange), 3V(red) of device 1 at 300K and device 2 at 265K. (e-f). Replot data  $I$ - $V$  at  $V_{ILg}=0$  as  $I$  versus  $\text{sign}(V)\sqrt{V}$  for device 1 and 2 respectively.

Figure 9.2 (c-d) presents the  $I$ - $V$  characteristics of two different IL-covered devices at different IL gate voltages  $V_{ILg}$ . The data are taken at  $T= 300\text{K}$  and  $265\text{K}$ ,

respectively. As  $V_{ILg}$  increases from 0 to 3V, the device conductance rises from  $\sim 1$  to  $\sim 180 \mu\text{S}$ , indicating that the Fermi level, which is initially located within the band gap, is tuned to the conduction band. At  $V_{ILg} > 1\text{V}$ , the  $I$ - $V$  curves are linear for  $V$  up to  $\pm 1\text{V}$ . In contrast, at  $V_{ILg} = 0$ , the  $I$ - $V$  curves are linear for relatively small source-drain bias ( $V < 0.1\text{V}$ ) (Figure 9.2 (c-d)), but becomes strongly non-linear for large  $V$  range (Figure 9.2 (c-d) inset).

Insight into transport in intrinsic  $\text{MoS}_2$  devices can be obtained by studying the  $I$ - $V$  characteristics at  $V_{ILg} = 0$ . Figure 9.2 (e-f) replots the same data in Figure 9.2 (c-d) as  $I$  vs  $\sqrt{V}$  in log-linear scale for devices 1 and 2, respectively. Both data sets, spanning 4 decades in  $I$ , fall nicely onto a straight line, indicating that  $I \propto e^{\sqrt{V}}$ . Such a dependence may arise from two different mechanisms [109]: (1) Schottky emission, in which the thermionic emission dominates the carrier transport across the metal-semiconductor interface, or (2) Frenkel-Poole emission, which is due to field-enhanced thermal excitation of trapped electrons into the conduction band of the semiconductor. For both mechanisms, one expects

$$I \propto \exp\left[\frac{a\sqrt{V} - \Phi_B}{k_B T}\right] \quad (9.1)$$

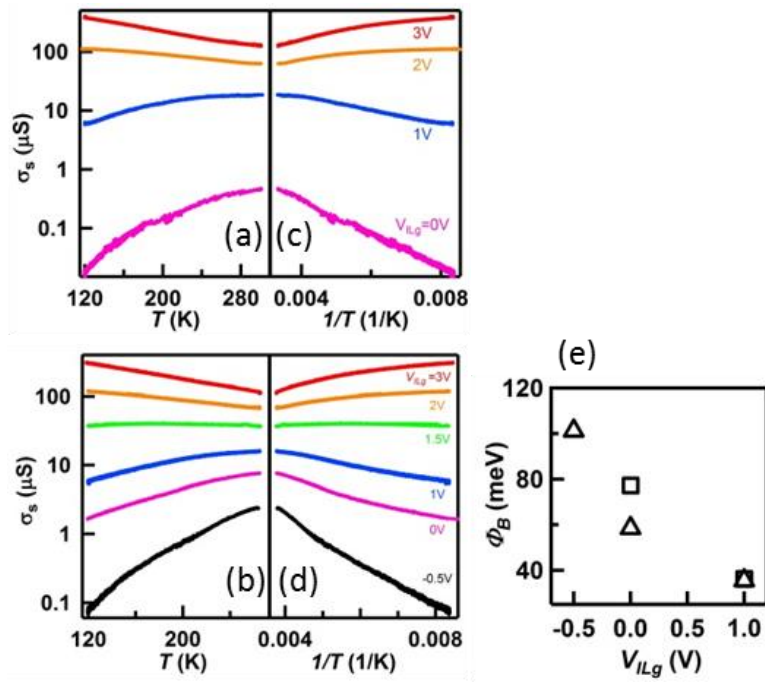
where  $a = \beta e \sqrt{e/4\pi\epsilon_0\epsilon_r d}$ . Here  $e$  is the elementary charge,  $V$  is the bias voltage,  $\epsilon_0$  and  $\epsilon_r$  are the permittivity of vacuum and device, respectively,  $d$  is the distance over which the electric field is applied,  $\Phi_B$  is the barrier height, and  $k_B$  is the Boltzmann constant.  $\beta$  is a constant and is 1 and 2 for Schottky and Frenkel-Poole emission, respectively.

To distinguish between these two transport mechanisms, we note that Schottky emission occurs at the metal-MoS<sub>2</sub> interface, so  $d$  is given by the thickness of the MoS<sub>2</sub> sheet,  $\sim 2$ -10 nm. In contrast, transport via Frenkel-Poole emission takes place laterally in the bulk of the MoS<sub>2</sub> sheet, and the electric field drops across the length of the samples, thus  $d \sim 1 \mu\text{m}$ . Fitting the data in Figure 9.2 (e) and (f) to equation (9.1), we obtain a slope of  $a=6.81$  for device 1 and 6.04 for device 2. This yields  $\epsilon_r d \sim 70$  nm for both devices, and excludes Frenkel-Poole emission as the leading transport mechanism, since  $d \sim 1 \mu\text{m}$  would lead to the unphysically small value of  $\epsilon_r < 1$ . We thus conclude that transport in IL-gated MoS<sub>2</sub> devices is dominated by Schottky emission at the metal-MoS<sub>2</sub> interfaces.

Using values of  $a$  obtained from the fitting,  $T_0=300\text{K}$  (265K) and  $d=6.2$  nm (10 nm) for device 1 (device 2), we estimate that  $\epsilon_r$  to be 10.9 and 11.1 for device 1 and device 2, respectively. Thus we are able to extract the dielectric constant of DEME-TFSI to be  $\epsilon_{IL} \sim 11$  near room temperature, in reasonable agreement with that reported in literature [107,110].

To further investigate transport mechanism in the MoS<sub>2</sub> devices, we explore the dependence of their conductance on temperature  $T$  at different  $V_{ILg}$ . To minimize hysteresis due to the slow-moving ions, the sample is warmed up to 300K, coupled to a new  $V_{ILg}$  value and allowed sufficiently long time lapse so that the equilibrium state is reached. The sample is then cooled slowly and their conductance monitored as a function of  $T$ . Figure 9.3 (a) presents such  $G(T)$  data at different  $V_{ILg}$  values. The most striking feature is the metal-insulator transition: for  $V_{ILg} \geq 2\text{V}$ , the conductance increases with a

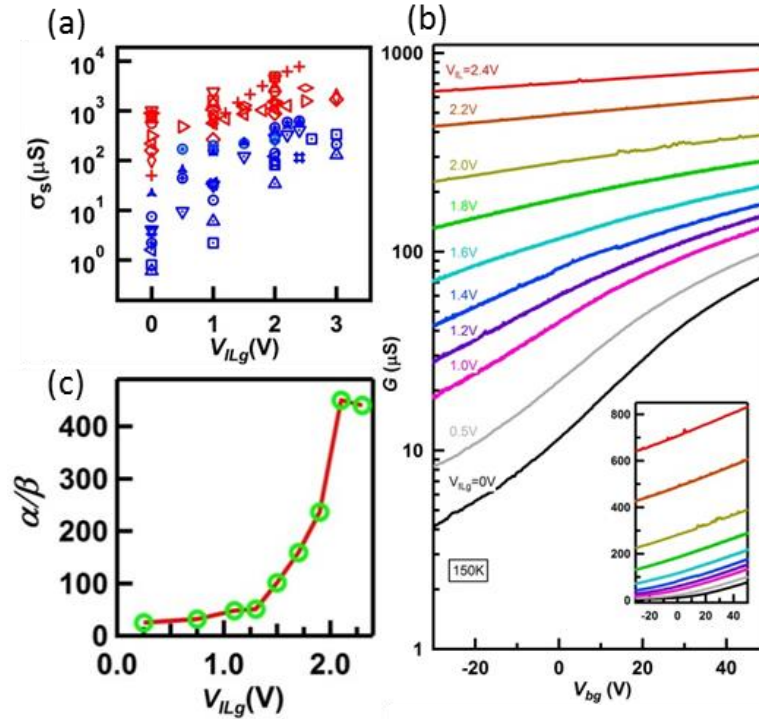
decreasing  $T$ , *i.e.* the device displays metallic behavior. Similar metal-insulator transition tunable by  $V_{ILg}$  is observed in both samples (Figure 9.3 (a-b)). The critical resistivity that separates the metal-insulator transition is  $16 \text{ k}\Omega$  for device 1 and  $28 \text{ k}\Omega$  for device 2. This is close to the theoretical value of  $h/2e^2=12.9 \text{ k}\Omega$  for spin-degenerate thin films [111] (where  $h$  is Planck's constant), particularly considering that two-terminal resistivity measured here may include contact resistance.



**Figure 9.3.** (a-b). Sheet conductance versus temperature at different  $V_{ILg}$  of device 1 and 2 respectively. (c-d). Same data in (a), (b) plotted in Arrhenius scale. (e). Extracted Schottky barrier heights at different  $V_{ILg}$  from device 1 and 2.

Figure 9.3 (c-d) replot the data in Arrhenius plot. For the insulating regime, the  $G(T)$  curves can be described by thermal activation over an energy barrier that is  $V_{ILg}$ -dependent. From equation (9.1),  $G \propto \exp(-b/T)$ , where  $b = \frac{-a\sqrt{V_0 T_0} + \Phi_B}{k_B}$  can be obtained

from the slope of the curves in the Arrhenius plot. Thus, we can extract the Schottky barrier height  $\Phi_B$  from the data. Figure 9.3 (e) shows the barrier height versus ionic liquid gate values. As  $V_{ILg}$  increases from 0 to 1V, the barrier height lowers from  $\sim 70$  to 36 meV.



**Figure 9.4.** (a). Zero-bias sheet conductance at different  $V_{ILg}$  of 9 substrate-supported (Blue) and 9 suspended (Red) samples. (b).  $G(V_{bg})$  at various  $V_{ILg}$  values at  $T=150K$ . Inset: Same data in linear scale. (c). Ratio of coupling efficiencies between IL gate and back gate as a function of  $V_{ILg}$ .

One major advantage offered by IL gating of suspended devices is that ions can accumulate on both sides of  $MoS_2$  sheet, thus enabling even higher doping level than that in substrate-supported samples. To compare the effect of single-sided and double-side IL gating, we measure the zero-bias sheet conductance at different  $V_{ILg}$  for 9 substrate-supported and 9 suspended samples (Figure 9.4 (a)). Despite the scatter in data (which is

expected for mesoscopic samples), the average sheet conductance of suspended samples is 1-2 orders of magnitude higher than that of supported on Si/SiO<sub>2</sub> substrates. Such dramatic enhancement of conductivity may be attributed to two factors: (1). the high doping level due to ion accumulation on both sides of the MoS<sub>2</sub> sheets; in the non-phonon limited conduction regime, larger charge carrier density that participate in transport leads to larger conductivity. (2). better screening provided by the high- $\kappa$  IL that encapsulates MoS<sub>2</sub> on both sides, which reduces scattering from charged impurities as well as Schottky barriers at the metal-semiconductor contacts.

Finally, we estimate the charge density induced by IL by measuring the ratio of coupling efficiencies  $\alpha/\beta$  between the IL gate and the back gate. To this end, we plot the  $G(V_{bg})$  curves at various  $V_{ILg}$  values at  $T=150\text{K}$  (Figure 9.4 (b)). As the curves are approximately parallel, the back gate efficiency does not change with  $V_{ILg}$ . The ratio of coupling efficiencies is then calculated by comparing the gate voltages required to induce the same magnitude change in  $G$ . The resultant data are displayed in Figure 9.4 (c). When the device is highly doped at  $V_{ILg}>2\text{V}$ ,  $\alpha/\beta \sim 450$ ; as the Fermi level moves towards the band edge, this ratio decreases to 51 at  $V_{bg} \sim 1.3\text{V}$  and 25 at  $V_{bg} \sim 0.25\text{V}$ . Such dependence of gate efficiency ratio on  $V_{ILg}$  has been observed in prior experiments [105] and is attributed to the quantum capacitance and negative compressibility of charge carriers in MoS<sub>2</sub> as the Fermi level is tuned close to the band gap.

At relatively large  $V_{ILg}$ ,  $\alpha/\beta \sim 450$ . The back gate's coupling efficiency  $\beta$  can be estimated by using parallel plate capacitance that consists of 180 nm of SiO<sub>2</sub> and 120 nm



of IL. Using  $\epsilon_r=11$  for IL as obtained above,  $\beta\sim 9.7\times 10^{10} \text{ cm}^{-2}\text{V}^{-1}$ . Thus IL's coupling efficiency  $\alpha$  is estimated to be  $4.4\times 10^{13} \text{ cm}^{-2}\text{V}^{-1}$ , which is 4-5 times larger than that reported in prior experiment [104], and consistent with ion accumulation on both sides of the suspended sheet.

In conclusion, by applying ionic liquid gating to suspended  $\text{MoS}_2$  FET devices, we observe dramatically improved conductivity and mobility, which suggest Schottky barrier reduction and dielectric screening by the IL environment. Their transport characteristics indicate that Schottky emission is the dominating transport mechanism. We estimate that the dielectric constant of DEME-TFSI is  $\sim 11$ , with a coupling efficiency of  $4.4\times 10^{13} \text{ cm}^{-2}\text{V}^{-1}$ . With further optimization in choosing the ionic species and in IL handling and storage, we expect even more efficient coupling can be reached. Similar technique can be applied to other atomically thin sheets and enable observation of phase transitions at extremely high charge densities.

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## Chapter 10 Conclusion and Outlook

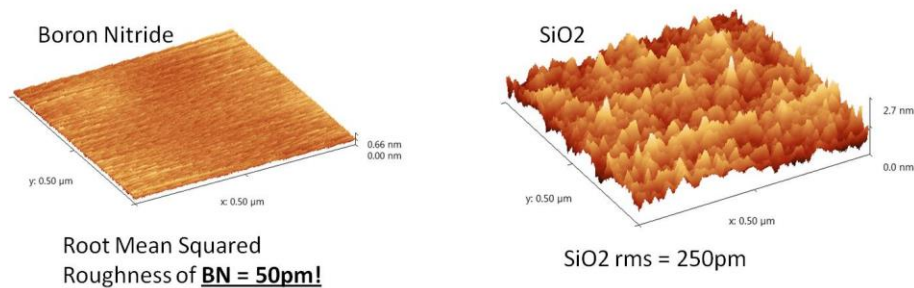
Over the past five years, my work focused on exploring electrical properties of suspended two-dimensional materials, including graphene and molybdenum disulfide ( $\text{MoS}_2$ ).

Graphene is a wonderful material not only because of its extraordinary materials properties, but also because it serves as a platform for exploring novel physical phenomena. To focus on the intrinsic electrical properties, we exclude the external interferences such as scatterings by removing the substrate. Fractional quantum Hall effect [14], interaction-induced insulating states in ultra-clean bilayer graphene [85] and ABC-stacked trilayer samples [35] have been observed in our group. We also studied the twisted bilayer graphene sample with controlled interlayer coupling. More experiments and further device optimization are warranted to obtain more insight into this area.

$\text{MoS}_2$  is another promising 2D material, since it has a thickness-dependent band gap, though its mobility is rather low. To identify the mobility bottleneck, we fabricate suspended  $\text{MoS}_2$  devices to study the influence of  $\text{SiO}_2$  substrate. No significant mobility improvement is observed, thus we exclude the  $\text{SiO}_2$  substrate as the main reason underlying the low mobility of  $\text{MoS}_2$  devices. By applying ionic liquid gating to suspended  $\text{MoS}_2$  devices and studying their transport characteristics, we conclude that Schottky emission at the metal- $\text{MoS}_2$  interface dominates transport. We extract the dielectric constant of the ionic liquid DEME-TFSI to be 11, and are able to induce a very

high coupling efficiency (up to  $4.4 \times 10^{13} \text{ cm}^{-2} \text{ V}^{-1}$ ) by using ionic liquid gating on suspended MoS<sub>2</sub>.

2D materials constitute one of the most active frontiers of material science research. One of the most important developments in this area is the emergence of hexagonal boron nitride (*h*-BN) as substrates, and van der Waals heterostructures. Since *h*-BN is atomically flat with few trapped charges (Figure 10.1), it enables high mobility devices [112]. Heterostructures such as BN-encapsulated MoS<sub>2</sub> are very promising, and recently reported one-dimensional electrical contact [113] can also be adapted to MoS<sub>2</sub> devices. Mobility up to 34,000 cm<sup>2</sup>/Vs at low temperatures in graphene-contacted, BN-encapsulated 6-layer MoS<sub>2</sub> devices has been reported [114]. With further experimental optimization, novel physical phenomena in MoS<sub>2</sub> devices such as quantum Hall effect and coupled spin-valley physics await exploration.



**Figure 10.1.** The surface roughness of BN and SiO<sub>2</sub> from atomic force microscope images (Image from Jarillo-Herrero group website).

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