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Ultra-Low-Power and High-Sensitivity Wake-Up Receivers for IoT Applications

A dissertation submitted in partial satisfaction of the requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Po-Han Wang

Committee in charge:

Professor Patrick P. Mercier, Chair
Professor Gert Cauwenberghs
Professor Drew A. Hall
Professor William S. Hodgkiss
Professor Gabriel M. Rebeiz

2020

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The dissertation of Po-Han Wang is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2020

DEDICATION

To my parents, Tzu-Ying Wang and Min-Shing Lin, my late grandfather, Kuo-Chiang Wang, my fiancée, Chih-Ling Liu, and all of those who shared their lives with me.

EPIGRAPH

I had nothing further to do than to put out my hand and reap what others had sown for me. —Johann Wolfgang von Goethe

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Chapter 4 is based on and mostly a reprint of the following publications: P.-H. P. Wang and P. P. Mercier, "A 220μW -85dBm Sensitivity BLE-Compliant Wake-Up Receiver Achieving -60dB SIR via Single-Die Multi-Channel FBAR-Based Filtering and a 4-Dimentional Wake-Up Signature," *IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2019, pp. 440-442, and P.-H. P. Wang and P. P. Mercier, "An Interference-Resilient BLE-Compatible Wake-Up Receiver Employing Single-Die Multi-Channel FBAR-Based Filtering and a 4-D Wake-Up Signature," *IEEE Journal of Solid-State Circuits*, In Press.

Chapter 5 is based on and mostly a reprint of the following publications: P.-H. P. Wang and P. P. Mercier, "A 4.4μW $-92/-90.3$dBm Sensitivity Dual-Mode BLE/Wi-Fi Wake-up Receiver," *IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, Jun. 2020, pp. 1-2, and P.-H. P. Wang and P. P. Mercier, "A Dual-Mode Wi-Fi/BLE Wake-Up Receiver," *IEEE Journal of Solid-State Circuits*, Under Review.

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PUBLICATIONS

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P.-H. P. Wang, C. Zhang, H. Yang, M. Dunna, D. Bharadia and P. P. Mercier, "A Low-Power Backscatter Modulation System Communicating Across Tens of Meters With Standards-Compliant Wi-Fi Transceivers," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 11, pp. 2959-2969, Nov. 2020.

P.-H. P. Wang and P. P. Mercier, "An Interference-Resilient BLE-Compatible Wake-Up Receiver Employing Single-Die Multi-Channel FBAR-Based Filtering and a 4-D Wake-Up Signature," *IEEE Journal of Solid-State Circuits*, In Press.

P.-H. P. Wang and P. P. Mercier, "A 4.4μW 92/90.3dBm Sensitivity Dual-Mode BLE/Wi-Fi Wake-up Receiver," *IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, Jun. 2020, pp. 1-2.

H. Jiang, P.-H. P. Wang, L. Gao, C. Pochet, G. M. Rebeiz, D. A. Hall, and P. P. Mercier, "A 22.3-nW, 4.55 cm^2 Temperature-Robust Wake-Up Receiver Achieving a Sensitivity of 69.5 dBm at 9 GHz," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 6, pp. 1530-1541, Jun. 2020.

P.-H. P. Wang, C. Zhang, H. Yang, D. Bharadia and P. P. Mercier, "A 28μW IoT Tag That Can Communicate with Commodity WiFi Transceivers via a Single-Side-Band QPSK Backscatter Communication Technique," *IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2020, pp. 312-314.

P.-H. P. Wang and P. P. Mercier, "A 220μW $-$85dBm Sensitivity BLE-Compliant Wake-Up Receiver Achieving $-$60dB SIR via Single-Die Multi-Channel FBAR-Based Filtering and a 4-Dimentional Wake-Up Signature," *IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2019, pp. 440-442.

H. Jiang, P.-H. P. Wang, P. P. Mercier, and D. A. Hall, A 0.4-V 0.93-nW/kHz relaxation oscillator exploiting comparator temperature-dependent delay to achieve 94-ppm/°C stability, *IEEE Journal of Solid-State Circuits*, vol. 53, no. 10, pp. 3004-3011, Oct. 2018.

P.-H. P. Wang, H. Jiang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, P. P. Mercier, and D. A. Hall, "A Near-Zero-Power Wake-Up Receiver Achieving −69-dBm Sensitivity," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1640-1652, Jun. 2018.

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X. Wang, P.-H. P. Wang, Y. Cao, and P. P. Mercier, A 0.6V 75nW all-CMOS temperature sensor with 1.67m°C/mV supply sensitivity, *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2274-2283, Sep. 2017.

H. Jiang, P.-H. P. Wang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, D. A. Hall, and P. P. Mercier, A 4.5nW wake-up radio with −69dBm sensitivity, *IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2017, pp. 416-417.

ABSTRACT OF THE DISSERTATION

Ultra-Low-Power and High-Sensitivity Wake-Up Receivers for IoT Applications

by

Po-Han Wang

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2020

Professor Patrick P. Mercier, Chair

Wireless communication circuits often dominate the power consumption of Internet of Things (IoT) devices such as small battery-powered commercial wearables or low-power-wide-area-network (LPWAN) environmental sensors for infrastructure. More specifically, a large fraction of this power comes from node-to-hub or node-to-node networking requirements, especially when such devices communicate with low-to-medium average throughput. To reduce this power, instead of duty-cycling the main receiver, employing an auxiliary wake-up receiver (WuRX) that monitors the RF spectrum for a pre-defined wake-up signature either continuously or in duty-cycle fashion has been proved to be an effective solution. In this thesis, WuRX designs targeting ultra-low-power and high sensitivity for different usage scenarios are investigated. First, a WuRX for emerging LPWAN applications targeting to be used with the always-on WuRX communication protocol is presented. This design explores architecture-level and circuit-level techniques to operate with near-zero power consumption while achieving high sensitivity. Moreover, an active and a passive envelope detector (ED) that

employ pseudo-balun architectures are also proposed, which further improve sensitivity and enable operation at a higher frequency band. On the other hand, WuRXs for commercial applications targeting to be used primarily with the duty-cycled WuRX communication protocol while being compatible with well-established wireless standards are also presented. First, a Bluetooth Low Energy (BLE) WuRX achieves low power, high sensitivity, interference-resiliency, and standard-compatibility through a combination of communication and circuit techniques, including high-Q filtering by a bank of FBAR resonators and a frequency-hopped mixer-first RF front-end that responds to a 4-dimensional (4-D) wake-up signature. This work is then further enhanced to achieve higher sensitivity while maintaining comparable interference-resiliency and power without the off-chip FBAR filters for a fully integrated solution. More importantly, this enhanced design is the first dual-mode WuRX compatible with both BLE and Wi-Fi transmitters, thanks to a carefully architected frequency plan that supports BLE advertisement channel hopping or a proposed subcarrier-based within-channel Wi-Fi frequency hopping scheme. As a result, the presented WuRX designs could potentially help enable new wireless IoT applications, particularly those that have low-to-medium average throughput requirements.

Chapter 1

Introduction

1.1 Motivation

Years of technological progress on integrated circuits and wireless communication has made the vision of Internet of Things (IoT) from science fiction to reality. The global IoT market will be worth $1.1 trillion in revenue, and there will be more than 25 billion IoT connections by 2025 as predicted by the GSM Association (GSMA) [1].

IoT creates a large class of emerging applications, which can generally be divided into three categories: consumer, infrastructure, and industrial applications. Consumer applications, such as audio streaming, wearables data transfer, beacon broadcasting, and environmental sensing for smart home automation as depicted in Fig. 1.1(a), mainly focus on people's daily life and provide direct user experiences. On the other hand, infrastructure applications, such as metropolitan scale deployments of smart meters and transportation monitoring, environmental monitoring for water leakage, air quality, and wildfire detection, as well as energy management including smart grid and smart lighting, mainly focus on public goods and provide background processing. Finally, industrial applications, such as smart label tracking for warehouse management and environmental sensing for agriculture, focus on providing industrial efficiency and optimization. A detailed look at infrastructure and industrial IoT applications is shown in Fig. 1.1(b) [2].

The cornerstones of IoT are clusters of wireless sensor networks (WSN). Each wireless sensor node has certain requirements depending on applications, but in general, power consumption is always the primary concern. Consumer applications, from "un-

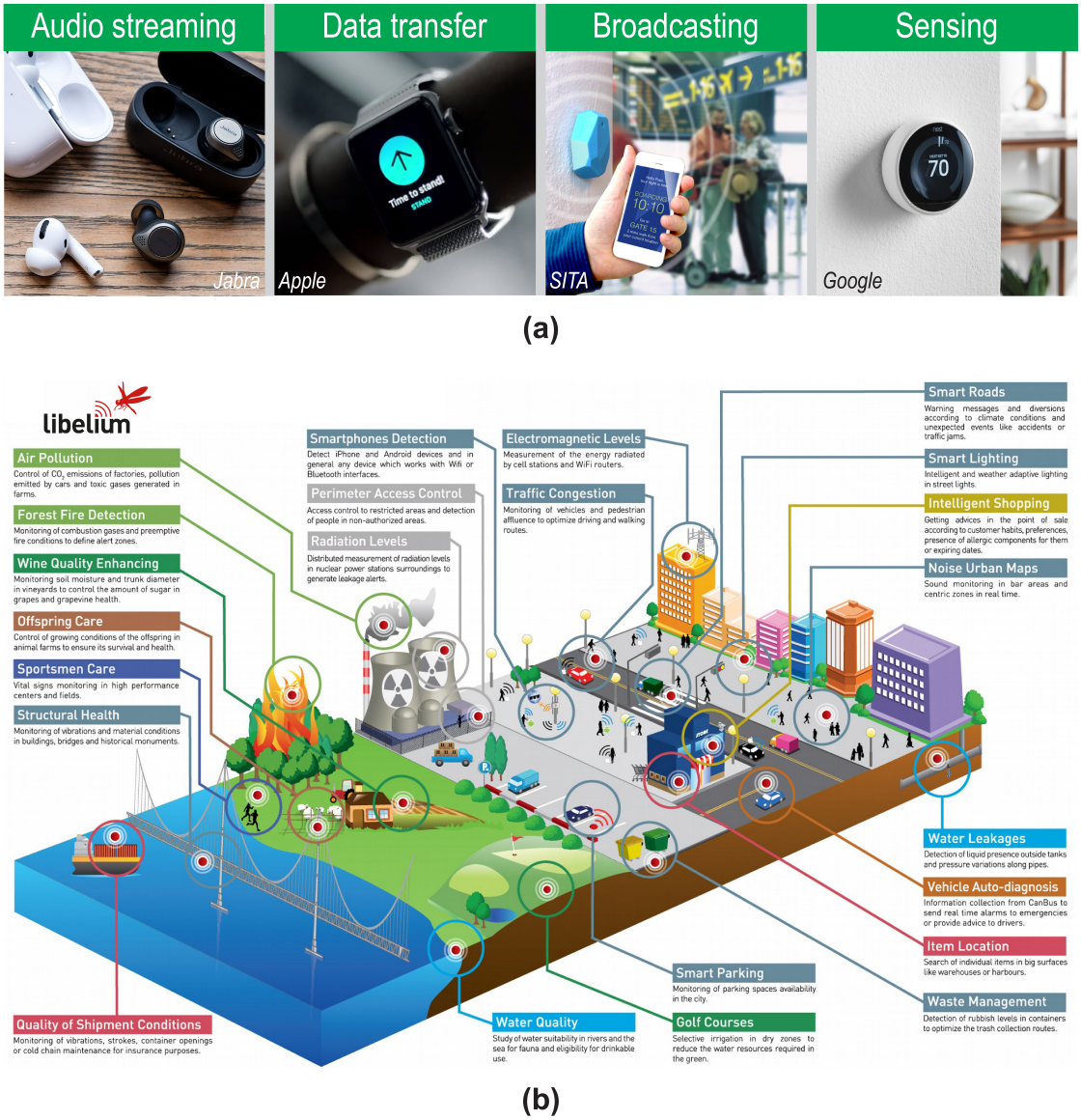


Figure 1.1: IoT-enabled applications categories: (a) consumer applications; and (b) infrastructure and industrial applications [2].

awearable" wearable sensors to future biomedical implants, are typically constrained in size and therefore make no room for high capacity batteries. For instance, a size A10 button cell Zinc-air battery, which has the highest energy density among all button cell materials, has 90 mAH capacity and could only support a typical wireless sensor node up to one week of use. On the other hand, although some of the infrastructure and industrial applications do not require physically small size and can use a larger battery,

these wireless sensor nodes are typically located at places where it is not efficient and cost-effective to replace the battery weekly or monthly (e.g., wild fire detection sensors in forest or water quality sensors in rivers and sea). Therefore, it is ideal for these wireless sensor nodes to operate under low power with years of system lifetime. Since the energy consumed by an IoT wireless sensor node is often not dominated by the sensor itself (e.g., temperature sensors with power ranging from 75 nW [3] to merely 113 pW [4] have been reported) but rather the embedded wireless radio, reducing the power consumption of the radios is an impactful strategy to improve IoT device operational lifetime.

Another important metric for wireless sensor nodes for IoT is the communication distance, which is limited by the operating frequency and sensitivity of the embedded wireless radio receivers. Most of the commercial applications target < 100 meters of communication distance and are within either a wireless local area network (WLAN) or a wireless personal area network (WPAN) that utilizes the 2.4 or 5 GHz industrial, scientific and medical (ISM) band where Wi-Fi and Bluetooth (or Bluetooth Low Energy (BLE)) are the two most popular radio standards. On the other hand, infrastructure and industrial applications often target hundreds meters or even kilometers of communication distance and are within a low-power wide-area network (LPWAN), which utilizes the 400 or 900 MHz ISM band or even the 100 MHz band, owing to the fact that lower frequency waves are less susceptible to obstacles and can propagate further. Under a specified operating frequency, the communication distance is then determined by the receiver sensitivity P_{SEN}, which can be derived as the following for conventional linear receivers [5]:

$$P_{\mathrm{SEN}}(\mathrm{dBm}) = -174(\mathrm{dBm/Hz}) + NF + 10\log BW_{\mathrm{BB}} + SNR_{\mathrm{min}}, \tag{1.1}$$

where NF is the noise figure of the receiver, BW_{BB} is the baseband signal bandwidth, and SNR_{min} is the minimum signal-to-noise ratio (SNR) required for demodulation. Based on (1.1), high sensitivity can be achieved by reducing the following parameters:

1. NF*:* The most direct and effective way to improve P_{SEN} is to reduce receiver NF, which generally dominates by the front-end low noise amplifier (LNA). Unfortunately, since LNA is a RF circuit block, high power consumption is then required for good P_{SEN}, which contradicts with the goal for low power receivers. Moreover, this trade-off becomes more prominent when the operating frequency is higher.

2. BW_{BB}*:* Reducing BW_{BB} effectively reduces the total integrated noise and improves P_{SEN}, but it inevitably reduces the data rate and available throughput. This is one of the key strategies for LPWAN infrastructure and industrial wireless sensors to enlarge communication distance, as such event-driven applications generally do not require continuous transmission and have low-average throughput. For instance, LoRaWAN utilizes a 300 bps to 50 kbps data rate, whereas Sigfox is only 100 bps to 600 bps. On the other hand, commercial IoT wireless sensors can have average throughput from low to high depending on user scenarios, which makes reducing BW_{BB} not always applicable. In general, Bluetooth has 1 MHz channel bandwidth (2 MHz for BLE) and is used by applications with low to medium average throughput, while Wi-Fi has channel bandwidth from 20$\sim$160 MHz and is used by applications with medium to high average throughput.

3. SNR_{min}*:* For wireless communication, data is first modulated onto the carrier wave and then transmitted. To increase spectral efficiency and also average throughput, complex modulation can be adopted, however, at the expense of higher SNR_{min}. This is the fundamental reason that receivers targeting signals with complex modulation normally require higher power consumption to achieve the same sensitivity as receivers targeting signals with less complex modulation. Therefore, for emerging LPWAN infrastructure and industrial wireless sensors, on-off-keying (OOK) and frequency-shift-keying like modulations are usually adopted. For commercial IoT wireless sensors, BLE uses Gaus-

sian frequency-shift keying (GFSK) and is the most suitable standard for low power radios, while Wi-Fi uses much complex orthogonal frequency-division multiplexing (OFDM) based modulation. Therefore, combined with BW_{BB} discussed previously, to achieve the same sensitivity (e.g., < -90 dBm), Bluetooth receivers typically consume $<$10mW, while Wi-Fi receivers can consume 10s to 100s of milliwatt of power.

The discussions so far focus on the performance target and trade-off of the receiver itself for IoT applications. For high-average throughput applications, radio can operate continuously and the radio power equals to the average power. However, in applications with medium-to-low average throughput, a large fraction of this energy consumption typically comes from node-to-node network establishment requirements [6]. Therefore, techniques to reduce this power is of interest, especially for IoT.

1.2 Communication Protocols: Conventional vs. Wake-Up Receiver

Since medium-to-low average throughput applications do not require continuous communication, a potentially impactful way to save energy is to keep the receiver in a low-power sleep state, and only turn it on periodically after a pre-defined sleep timer expires. This duty-cycled receiver approach is depicted in Fig. 1.2(a), and can be deployed both synchronously (e.g., in Wi-Fi) or pseudo-synchronously (e.g., in Bluetooth Low Energy (BLE)) [7]. The effectiveness of this technique is dependent on the accuracy of the sleep timer - if it is not sufficiently accurate, then the receiver must turn on early to ensure it guarantees successful capture of the packet, and/or the transmitted packet must be repeated to guarantee proper reception. Since sleep timers have finite accuracies, this puts a lower bound on the realistically achievable duty cycle of the receiver. This is not a problem in medium-average-throughput applications where the duty cycle cannot be too low for throughput reasons, but can significantly limit the energy consumption of

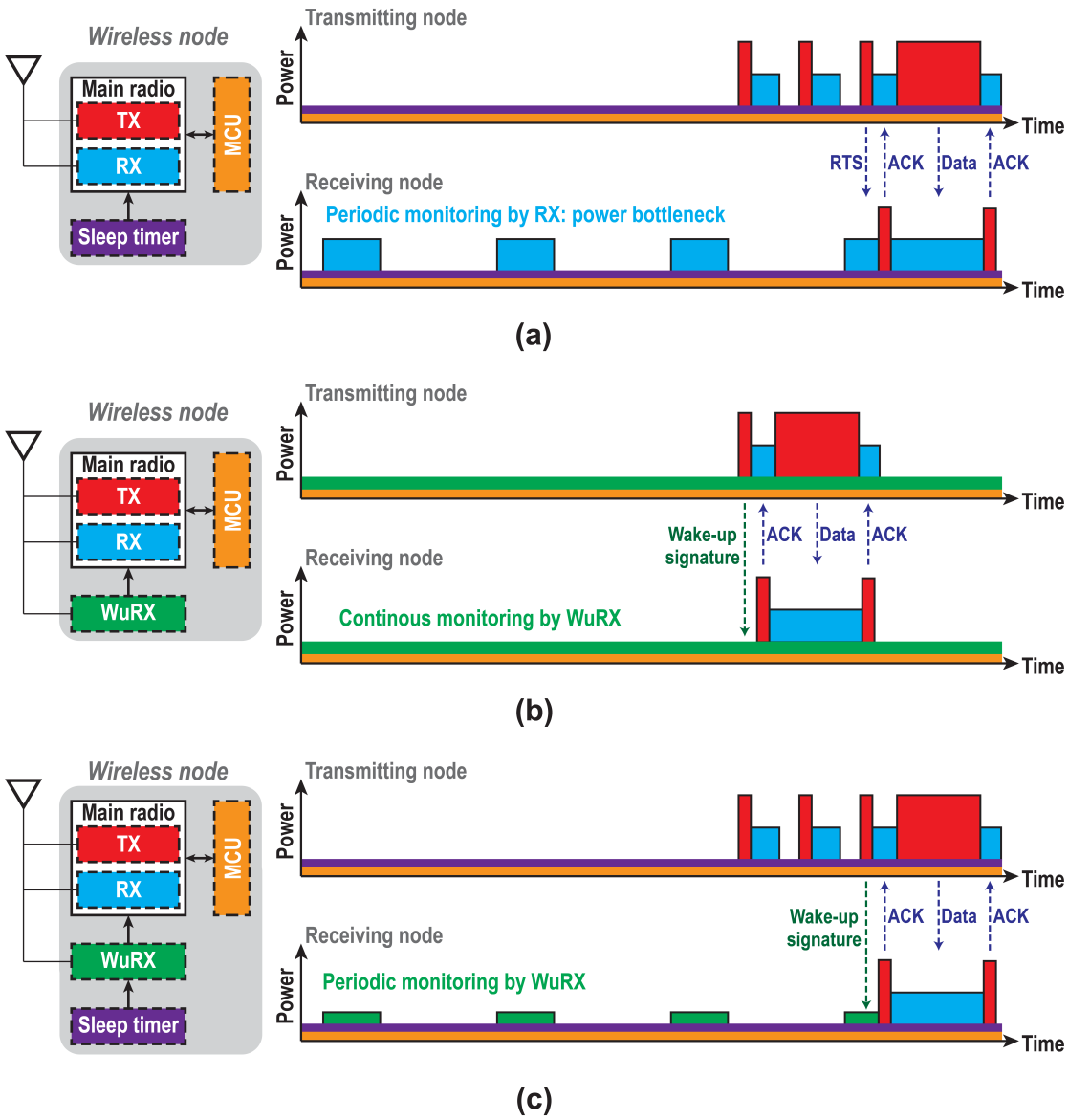


Figure 1.2: Protocols to establish communication between wireless nodes: (a) conventional duty-cycled main radio approach; (b) always-on wake-up receiver approach; and (c) duty-cycled wake-up receiver approach.

low-average-throughput applications due to the need to constantly synchronize with the network even if no data needs to be communicated.

Instead of duty-cycling the main receiver, another approach to reduce energy consumption when continuous communication is not required is to employ an auxiliary always-on wake-up receiver (WuRX) that continuously monitors the RF spectrum for a

pre-defined wake-up signature. Once the wake-up signature is successfully received, as depicted in Fig. 1.2(b), the main radio turns on to perform instantaneously high-speed (and power hungry) communication of one or more packets, after which it goes back into a sleep state until the next wake-up event. In order to impactfully reduce the overall energy burden of communication, the power consumption of the WuRX must be significantly lower than that of the main radio. Fundamentally, this requires trading off power consumption with one or more of: modulation format and data rate (which set the spectral efficiency and wake-up latency), sensitivity, channelization, interference resiliency, or standards compliance [8–14]. This approach is very useful, particularly for emerging LPWAN infrastructure and industrial IoT applications where the most important metric is power consumption.

However, commercial IoT applications typically utilize well established wireless standards (e.g., Wi-Fi and Bluetooth) and sophisticated wireless chipsets/hardwares within an urban area. Therefore, most of the aforementioned items that can be traded off for low power consumption are not recommended to modify below the specifications of the main radio. For example, if the WuRX does not have as good of a sensitivity as the main radio, then there is a mismatch between the achievable communication ranges of the two radios and existing network deployment strategies may have to undergo a costly re-design. Similarly, if the WuRX does not support the same standard as the main radio, then addition custom hardware is required on the transmitting node, which may be costly. Or, if the WuRX does not support similar channelization and interference resiliency compared to the main radio, then the WuRX simply won't be sufficiently robust in congested environments, limiting its usefulness in the same environments the main radio is supposed to work in.

As a result, the main knob in which WuRXs reduce power compared to the main radio is in the data rate and the selection of the modulation format. In many low-average-throughput applications, a relatively long wake-up latency, for example tens-to-hundreds of milliseconds, or even up to one second, can be acceptable. How to achieve this in a manner that is compatible with existing standards will be discussed in Chapter 4

and Chapter 5. Assuming for the moment that it is possible, achievement of the same sensitivity and interference resiliency as the main receiver, even with relaxed data rate and modulation schemes, still requires significant power consumption [15–21].

To further reduce power, it is possible to combine the approaches in Figs. 1.2(a) and (b) to create a duty-cycled WuRX, as depicted in Fig. 1.2(c) [16]. For example, a prior-art Wi-Fi WuRX consumed 700 μW, which is high for a WuRX, but low for a radio with similar sensitivity and interference robustness compared to that of a full fledged Wi-Fi receiver [21]. With careful design and duty-cycling, it is theoretically possible for this power consumption to be reduced by up to 70$\times$ or 3$\times$ if duty-cycled down to wake-up latencies of 10 ms to 1 s, respectively, for example. This can thus be an important knob to trade-off between power and latency, iso other performance parameters.

1.3 Outline

In this thesis, WuRX designs targeting ultra-low-power and high sensitivity for different usage scenarios are investigated. In Chapter 2, a WuRX for emerging LPWAN applications is presented. Targeting to be used with the always-on WuRX communication protocol, this design explores architecture-level and circuit-level techniques to operate with near-zero power consumption while achieve high sensitivity [8]. To improve sensitivity further while operate at a higher frequency band than the design in Chapter 2, an active and a passive envelope detectors (EDs) that employ pseudo-balun architectures are then presented in Chapter 3 [10, 12]. In Chapter 4, a WuRX for commercial applications using BLE standard is presented. This design achieves low power, high sensitivity, interference-resiliency, and standard-compatibility through a combination of communication and circuit techniques, including high-Q filtering by a bank of FBAR resonators and a frequency-hopped mixer-first RF front-end that responds to a 4-dimensional (4-D) wake-up signature [18, 20]. In Chapter 5, the work in Chapter 4 is further enhanced to achieve higher sensitivity while maintain comparable interference-resiliency and power

without the off-chip FBAR filters for a fully integrated solution. More importantly, this design is the first dual-mode WuRX compatible with both BLE and Wi-Fi transmitters, thanks to a carefully architected frequency plan that supports BLE advertisement channel hopping or a proposed subcarrier-based within-channel Wi-Fi frequency hopping scheme [22]. Finally, Chapter 6 concludes this thesis.

Chapter 2

A Near-Zero-Power Wake-Up Receiver Achieving −69-dBm Sensitivity

2.1 Introduction

The high power consumption of conventional low-power wide-area network (LPWAN) receivers employed in applications such as smart meters, environmental sensors, threat monitors, and other Internet of Things (IoT)-like applications often dictates overall device battery life. Even though many such applications communicate at low-average-throughputs, the power of the radio can be high due to the need for frequent network synchronization [6]. To reduce the power consumption, wake-up receivers (WuRXs), which trade-off sensitivity and/or data rate for low-power operation, ideally without seriously compromising interference resilience, have been proposed to monitor the RF environment and wake up a high-performance (and higher power) conventional radio upon the reception of a predetermined wake-up packet.

The two most important metrics for WuRXs used in low-average-throughput applications are the power consumption and sensitivity, as the power of always-on WuRXs ultimately determines the battery life of low-activity devices, while sensitivity determines the communication distance and therefore deployment cost via the total number of nodes required to achieve a given network coverage. Typically, sensitivity and power consumption trade-off with one another, making the design of WuRXs that simultaneously achieve both challenging. Interference resilience is also an important metric for WuRXs, since false alarms cause unwanted power dissipation in sensor nodes, while

missed detections result in sensor network malfunctions. Unlike conventional mobile receiver design, metrics such as physical size and data rate can often be exploited to improve sensitivity or reduce power, as will be shown shortly.

This chapter presents the design of a WuRX that targets LPWAN applications and therefore attempts to achieve both low power and high sensitivity with reasonable interference resilience through a combination of techniques including careful selection of the carrier frequency and data rate, inclusion of a high-Q RF impedance transformer/filter that delivers passive voltage gain as well as interference filtering, a high input impedance and high conversion gain envelope detector, a precise, yet low-power, regenerative comparator, and an optimized digital correlator that provides coding gain while combating false alarms caused by interferers. The overall WuRX architecture is presented in Section 2.2, while Section 2.3 describes the implemented off-chip transformer and circuits. Section 2.4 presents measurement results, followed by Figure of Merit (FoM) landscape of state-of-the-art WuRXs in Section 2.5. Finally, Section 2.6 concludes the chapter.

2.2 Wake-up Receiver Architecture

2.2.1 Overview

Most low-power WuRXs demodulate non-coherent OOK or FSK modulated signals using one of three general architectures illustrated in Fig. 2.1: a) mixer-based low-IF architectures, b) mixer-based uncertain-IF architectures, and c) direct envelope detection architectures. In all cases a front-end matching network is typically employed to filter RF noise/interference and provide a good match to 50 Ω, in some cases via impedance up-conversion to provide passive voltage gain. A low-noise amplifier (LNA) is optionally included to provide active gain at RF, at the expense of additional power consumption.

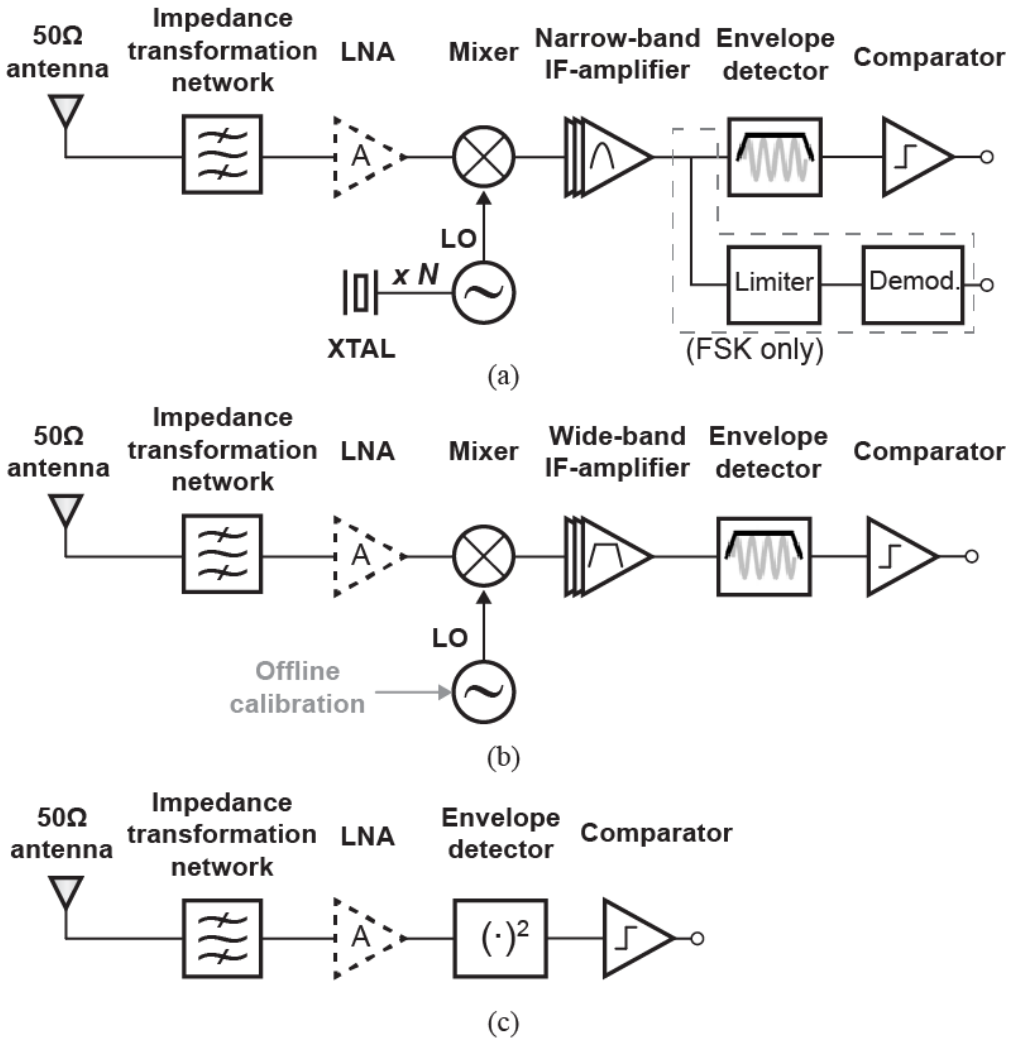


Figure 2.1: Wake-up receiver architectures: (a) mixer-based low-IF, (b) mixer-based uncertain-IF, and (c) direct envelope detection.

Mixer-Based Low-IF Architectures

Most conventional receiver architectures utilize a local oscillator (LO), often stabilized via a low-frequency crystal by means of a PLL [23] or injection locking [24], to mix the incoming RF signal down to a known intermediate frequency (IF) prior to demodulation via an envelope detector (ED) or other means (Fig. 2.1(a)). Since it is much more power-efficient to amplify and filter signals at a low IF than at RF, mixer-first low-IF architectures, where an LNA is not included, can consume relatively low power while achieving good sensitivity. For example, [23, 24] achieve -87 dBm and

-70 dBm at 50 kbps and 200 kbps, respectively. However, even though OOK and FSK are demodulated in a non-coherent manner, the generated LO must be frequency-stable in order to limit bandwidth (and therefore noise) at IF; this requires $\sim$10s of μW when operating between 400-900 MHz, and even more at 2.4 GHz. Thus [23, 24] each consume 44 μW, which is higher than desired for many WuRX applications. For this reason, mixer-based low-IF architectures are typically reserved for WuRX applications where sensitivity is important and μW power levels are acceptable.

Mixer-Based Uncertain-IF Architectures

The power consumption of LO generation can be reduced substantially if the frequency stability specifications are relaxed. For example, by replacing a frequency-locked oscillator with a simple free-running digitally controlled ring oscillator, LO generation has consumed 13/20 μW at 2.0/2.45 GHz in prior work [25, 26], respectively. However, mixing an incoming RF waveform with a free-running oscillator whose precise frequency is not well controlled or known requires a large IF bandwidth to guarantee proper reception for envelope detection. Thus, such architectures are called "uncertain-IF" WuRXs (Fig. 2.1(b)). Since even far away interferers can potentially end up in the wideband IF, high-Q filtering at RF prior to down-conversion is required. This can be accomplished using mechanical resonant structures (e.g., BAW or FBAR filters), or via N-path filters [27]. Generally, uncertain-IF WuRXs should achieve lower power operation than conventional low-IF WuRXs with similar, though typically slightly worse, sensitivity due to increased noise bandwidth. Recent work on multi-stage N-path filters have improved sensitivity via enhanced filtering, albeit at higher power (e.g., -97 dBm at 10 kbps and 99 μW [27]). Thus, mixer-based uncertain-IF WuRXs are capable of operating at lower power and higher frequencies than mixer-based low-IF WuRXs, with similar, though often slightly poorer, sensitivities.

Direct Envelope Detection Architectures

Many applications such as unattended ground sensor networks, smart home automation, and wearables demand sub-μW power consumption to enable ultra-long battery life while achieving always on sensing. Since LO generation and IF amplification dominate the power consumption of mixer-based architectures, an impactful way to reduce power is to eliminate mixers altogether and directly demodulate RF signal to baseband via an envelope detector (ED) [9, 28, 29] (Fig. 2.1(c)). However, since ED demodulates all energy present at their inputs to baseband, such architectures tend to accumulate significant noise and interference, making their sensitivity generally inferior to mixer-based architectures. To get more design insight, noise and sensitivity analysis of direct envelope detection architectures is provided in Appendix A.

2.2.2 Proposed WuRX architecture

The architecture of the proposed WuRX is shown in Fig. 2.2 [30]. The primary optimization objective of this design was to minimize power. This motivated the use of a direct-ED WuRX architecture operating at a low supply voltage (0.4 V in this work). However, the secondary objective was to achieve sensitivity that approaches that of a mixer-based WuRX architecture, while not significantly compromising tolerance to interferers. This was accomplished through a number of architectural and circuit design techniques described below.

2.2.3 Direct Envelope Detection RF Front-End Optimizations

Direct ED architectures demodulate all input RF energy to baseband, and thus any interferers within the input RF bandwidth can inhibit proper reception. In addition, the lack of an LNA together with very low-power demodulating circuits means that the baseband circuit noise often dominates, thereby ultimately limiting the WuRX sensitiv-

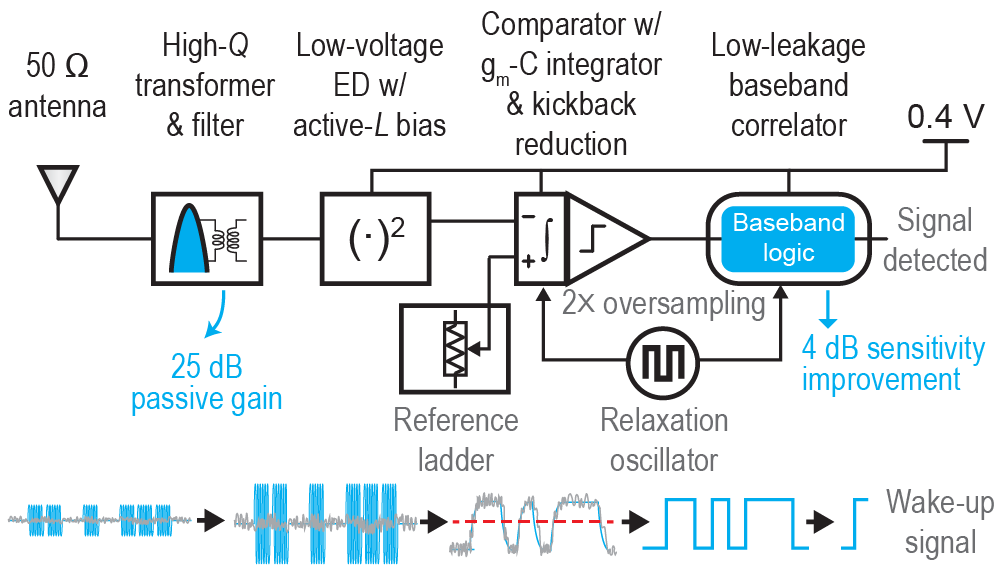


Figure 2.2: Overview of the proposed WuRX.

ity. Fortunately, these two problems, i.e., interference and baseband circuit noise, can be overcome via the following techniques:

Minimizing the influence of interference via high-Q filtering

To reduce the impact of in-band blockers in direct-ED or uncertain-IF mixer-based architectures, a high-Q narrow-band filter is needed to minimize RF bandwidth and block interferers. Most prior-art low-power radios accomplish narrow-band filtering by utilizing high-Q mechanical resonators, which offer attractive narrow filtering capabilities at 1-3 GHz [25, 31]. In this design, however, to attain the highest possible Q for sharp filtering, and, as will be seen shortly, to achieve a large impedance transformation ratio from a 50 Ω source as well as wide communication range, a carrier frequency in the 100 MHz range was selected for use near the FM radio band. Therefore, a high-Q filter (and, as will be described shortly, transformer) was designed out of lumped components directly.

Minimizing baseband circuit noise via passive RF voltage amplification

Envelope detectors are inherently non-linear elements. Unlike linear mixers used for down-conversion, the squaring operation of an ED converts pre-ED noise down to baseband via two mechanisms: self-mixing of noise and noise convolved with the input signal [32]. Since most ultra-low-power WuRXs forgo active gain before the ED, sensitivity is typically limited by baseband noise. Therefore, to improve sensitivity without a power penalty, most direct-ED WuRX designs strive to achieve as much passive voltage gain in the matching network as possible. This is typically achieved by designing the ED to have a large input impedance, and matching this large impedance to 50 Ω via an impedance transformation network. Prior work has shown 5 dB and 12 dB of passive voltage gain which, when coupled to either a rectifier or an active ED, achieved sensitivities of -45.5 dBm and -41 dBm at 12.5 kbps and 100 kbps at powers of 116 nW and 98 nW, respectively [28, 29]. Thus, direct ED systems can achieve ultra-low-power operation, yet without large RF voltage gain and low-noise baseband circuits, do so at limited sensitivities.

To address the aforementioned issues, the proposed WuRX incorporates an ED with a high input impedance that, combined with a high-Q impedance transformer, facilitates up to 25 dB of passive voltage gain at RF before being demodulated by the ED, thus directly resulting in a 25 dB improvement in sensitivity compared to the exclusion of this transformer. Furthermore, the ED is designed to support high conversion gain to further reduce the impact of baseband circuit noise (i.e., to increase SNR).

2.2.4 Baseband Bandwidth Considerations

There are two primary classes of applications where WuRXs can be useful: 1) high-average-throughput applications with asynchronous communication needs where WuRXs are primarily used to eliminate the need for precision watchdog timers that perform network synchronization; and 2) low-average-throughput applications where the

network is largely idle, waiting for an event to occur (e.g., infrastructure and perimeter monitoring, health alarm monitoring, etc.). In high throughput applications it is important to minimize wake-up detection latency, set in part by the WuRX data rate, so as to not adversely affect the average network throughput. In low throughput applications, wake-up latency (and thus the data rate of the WuRX), is less important, as long latency does not adversely affect the overall throughput needed. Most conventional WuRX designs target the first class of applications; this work instead focuses on the design of WuRXs used in low-average-throughput LPWAN applications. One of the key ideas of a LPWAN is to leverage the reduced data rate (and thus integrated baseband noise) to improve sensitivity and enable wide communication range. For example, LoRaWAN utilizes a 300 bps to 50 kbps data rate, whereas Sigfox is only 100 bps to 600 bps. Therefore, a 300 bps data rate was selected for this design.

2.2.5 Digital Baseband Processing

The received RF signal employed in this design is modulated with a custom designed 16-bit sequence. After envelope detection in the proposed architecture, the demodulated signal is $2\times$ oversampled and digitized by a 1-bit regenerative comparator. The output of the comparator feeds a digital correlator that computes the Hamming distance between the received and stored sequence. When the Hamming distance is below a programmable threshold (H_{th}), a wake-up signal is generated. It will be shown in Section 2.4 that the use of this wake-up sequence provides additional coding gain that improves the sensitivity of the proposed WuRX. Moreover, the correlator prevents false alarms caused by unwanted jammers. An on-chip relaxation oscillator provides the required 600 Hz clock.

2.3 Circuit Implementation

2.3.1 Transformer/Filter

The purposes of the transformer/filter is to impedance transform a 50 Ω source impedance to a much larger value to facilitate passive voltage gain, while also performing high-Q RF filtering. The schematic of the implemented transformer/filter is shown in Fig. 2.3(a)

were R_{S} is the 50 Ω source impedance. The primary stage resonator is formed by L_{P} and C_{P}, while the secondary stage is formed by L_{S} and C_{S}, with k denoting the coupling coefficient between L_{P} and L_{S}. C_{chip} and R_{chip} are the equivalent input impedance of the chip at the carrier frequency, which connects to the transformer/filter via a large AC-coupling capacitor, C_{BLK}, and a small parasitic inductor from the PCB trace and bondwire. The primary and secondary stage tanks both resonate at the same operating frequency, $f_{\mathrm{RF}} = 113.5$ MHz. Departing from a traditional 2-port RF filter, which has 50 Ω matching at both ports, the proposed transformer/filter not only provides a 2^{nd} order filter response for interference rejection, but also realizes impedance trans-

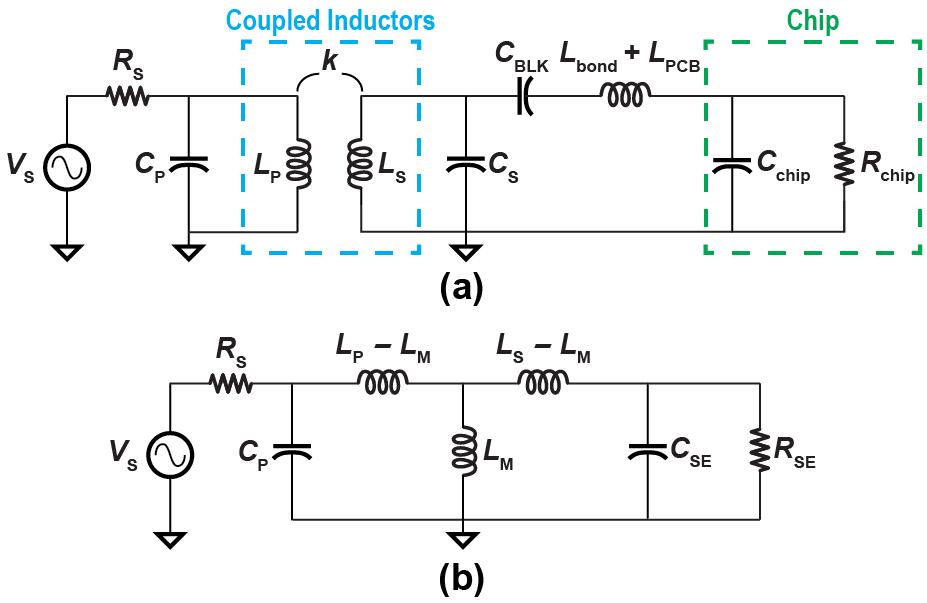


Figure 2.3: Schematics of (a) transformer/filter and (b) equivalent circuit model.

formation between the two ports to achieve passive voltage gain. To analyze the circuit, an equivalent circuit model is derived as shown in Fig. 2.3(b). L_{M} is determined by k and can be written as [33]:

$$L_{\mathrm{M}} = k \cdot \sqrt{L_{\mathrm{P}} L_{\mathrm{S}}} = k \cdot L_{\mathrm{S}} \cdot \sqrt{\frac{1}{N}}, \tag{2.1}$$

where N is the turn ratio between L_{P} and L_{S}. C_{SE} and R_{SE} are the equivalent capacitor and resistor of the secondary stage, with $C_{\mathrm{SE}} = C_{\mathrm{S}} + C_{\mathrm{chip}}$ and $R_{\mathrm{SE}} = R_{\mathrm{EQ,P}} || R_{\mathrm{chip}}$, where $R_{\mathrm{EQ,P}}$ is due to the finite quality factor (Q) of L_{S}. Therefore, the maximum passive voltage gain the transformer/filter can achieve at f_{RF} is:

$$Gain_{\max} = \sqrt{\frac{R_{\mathrm{SE}}}{R_{\mathrm{S}}}} = \sqrt{\frac{R_{\mathrm{EQ,P}} || R_{\mathrm{chip}}}{R_{\mathrm{S}}}}. \tag{2.2}$$

To get large passive voltage gain, a large $R_{\mathrm{EQ,P}}$ must be achieved by either increasing Q or L_{S} for a given C_{SE}. Since Q can only be pushed so high using practical inductors, L_{S} is the only practical tunable parameter. There are two things that limit the achievable value of L_{S}: 1) the chip input capacitance, C_{chip}, and 2) the self-resonant frequency of the inductor. With $C_{\mathrm{S}} = 0$ and $C_{\mathrm{chip}} = 1.8$ pF, the maximum L_{S} is 1.06 μH. Due to the size of the required inductor, it must be off-chip. For commercial inductors with high Q, self-resonance typically occurs when $\omega L \approx$1,400 Ω. To account for variation in C_{chip} and on-board parasitics, $\omega L =$520 Ω was chosen. From the datasheet of the selected inductor [34], a Q of 150 can be obtained at 115 MHz, and thus $R_{\mathrm{EQ,P}} <$78 kΩ.

After determining the value of L_{S} and C_{S}, we considered the coupling coefficient k and the turn ratio N, both of which affect the input matching and passive voltage gain. To have a sharper filter response for out-of-band interference rejection, k should be small and Q should be large [35]. Figs. 2.4(a) and (b) show calculated S_{11} and voltage gain of the transformer/filter varying k with N fixed to be 30. When k is increased from 0.02 to 0.06, the input matching gets better and the voltage gain increases. However, the filter

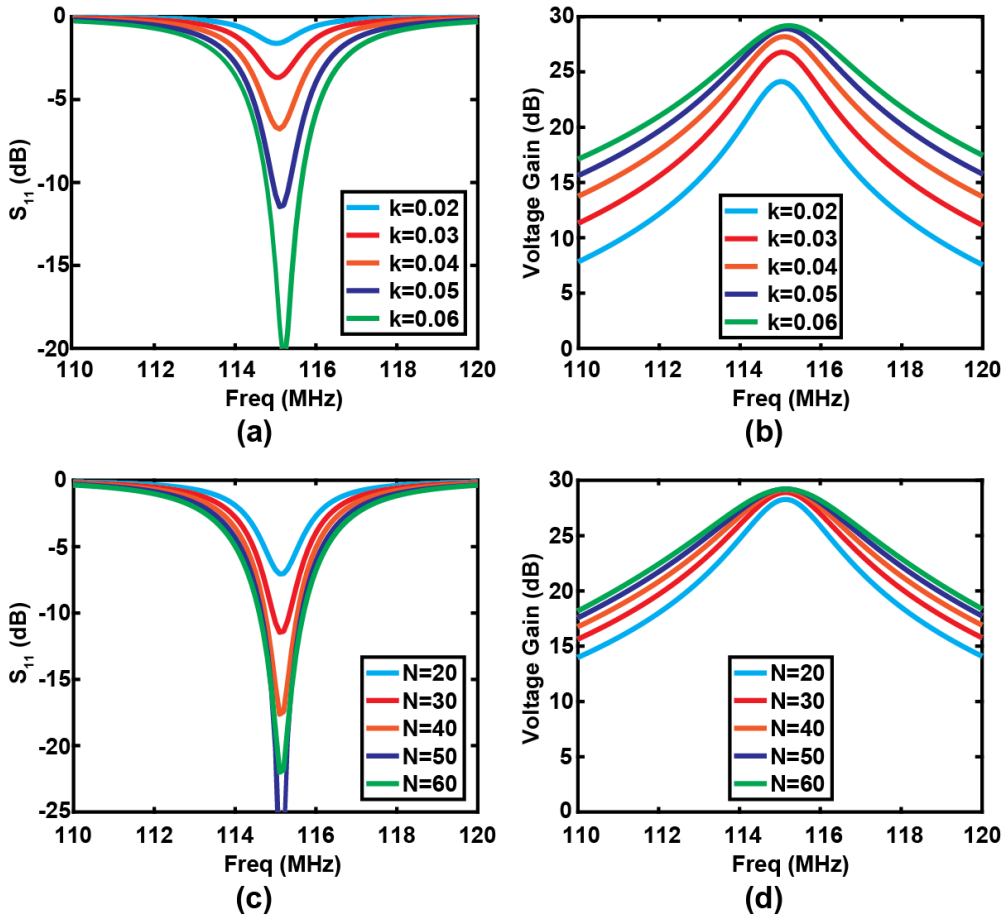


Figure 2.4: Plot showing (a) S_{11} vs. k; (b) voltage gain vs. k; (c) S_{11} vs. N; (d) voltage gain vs. N.

bandwidth also increases. Figs. 2.4(c) and (d) show calculated S_{11} and voltage gain varying N with $k = 0.05$. When N is increased from 20 to 60, the voltage gain does not increase much, but with considerably larger filter bandwidth. Therefore, $k = 0.05$ and $N = 30$ were chosen as a compromise between input matching, voltage gain, and filter bandwidth. Calculations show that S_{11} is better than -10 dB with a passive voltage gain of 28.9 dB and a 3 dB bandwidth of 2.4 MHz.

The key challenge in implementing the proposed transformer/filter is to control the coupling despite the large difference in inductance (720 nH and 24 nH). Implementing the inductors using only lumped elements would make it very hard to control the coupling through positioning, whereas only distributed inductors would take too much

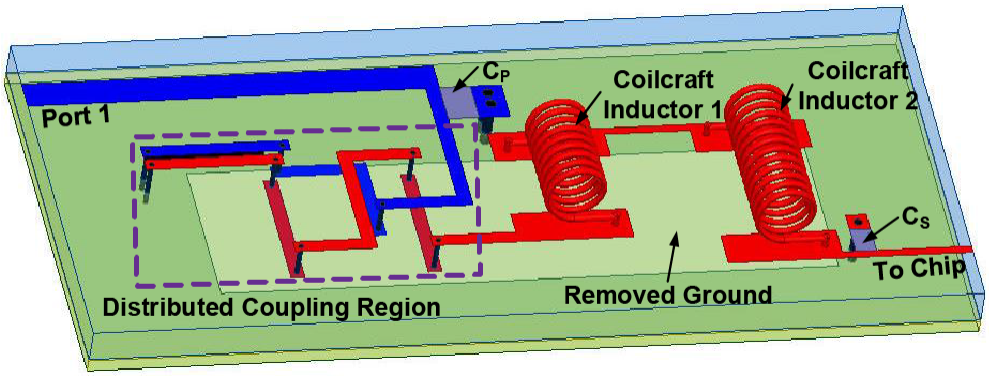


Figure 2.5: 3-D model of the transformer/filter.

area. As such, we used a combination of lumped inductors (220 nH and 160 nH from Coilcraft) and a distributed inductor to realize L_{S} and a distributed inductor to realize L_{P}, which has three advantages. First, L_{S} is realized by both distributed and lumped inductors, thus the value can be large. Second, the coupling is realized by the distributed parts of L_{P} and L_{S}, and thus k is determined by the length and gap of the coupling PCB traces. With modern PCB fabrication techniques, this coupling can be controlled precisely, which is crucial since k affects both passive gain and filter bandwidth. Third, the use of both lumped and distributed inductors provides more freedom to design the transformer. For example, the center frequency can be easily tuned by replacing lumped components, which is an advantage compared to mechanical resonators [25, 31].

Fig. 2.5 shows the 3-D model of the transformer/filter. To reduce the dielectric loss, a Rogers RO4003C substrate was used ($\epsilon_{\mathrm{r}} = 3.55$, thickness of 20 mil, and a loss tangent of 0.0027). From HFSS simulations, we found that at 115 MHz, L_{P} and L_{S} are 28 nH and 756 nH, respectively, and $k = 0.05$. All of the component values are close to the desired values from calculation. The simulated voltage gain was 26.6 dB with a bandwidth of 2.2 MHz.

2.3.2 Envelope Detector

To take full advantage of the gain provided by the transformer/filter, the ED must provide a large enough input resistance R_{chip} so as to not to degrade the corresponding

$R_{\mathrm{EQ,P}}$. Although a passive N-stage RF rectifier [9, 28] is a tempting choice (due to the zero power consumption), it is difficult to achieve high enough R_{chip}. Thus, in this work an active ED was selected. A transistor biased in the sub-V_{t} region can not only operate with a low supply voltage and low power consumption, but also provides an exponential voltage-current relationship. Assuming the transistor is operating in the sub-V_{t} saturation region (i.e., V_{DS} >100 mV) with negligible drain-induced barrier lowering (DIBL), the current can be written as [36]:

$$i_{\mathrm{DS}} = \mu C_{\mathrm{ox}} \frac{W}{L} (n-1) V_{\mathrm{T}}^2 e^{\frac{v_{\mathrm{GS}} - V_{\mathrm{t}}}{nV_{\mathrm{T}}}}, \tag{2.3}$$

where μ is the mobility, C_{ox} is the oxide capacitance, W is the transistor width, L is the transistor length, n is the sub-V_{t} slope factor, V_{T} is the thermal voltage ($k_{\mathrm{B}}T/q$), and v_{GS} is the gate-to-source voltage. This exponential relationship results in a 2^{nd} order non-linearity used for the desired ED functionality. The second order transconductance is given by:

$$g_{\mathrm{m2}} = \frac{1}{2} \cdot \frac{\partial^2 i_{\mathrm{DS}}}{\partial v_{\mathrm{GS}}^2} = \frac{I_{\mathrm{DS}}}{2(nV_{\mathrm{T}})^2}. \tag{2.4}$$

In an SOI process, the floating body can be connected to the gate directly without using deep n-well devices, commonly referred to as the dynamic threshold-voltage MOSFET (DTMOS) configuration [37], to achieve additional 2^{nd} order non-linearity via threshold voltage modulation. The additional transconductance can be derived as:

$$g_{\mathrm{mb2}} = \frac{1}{2} \frac{\partial^2 i_{\mathrm{DS}}}{\partial v_{\mathrm{BS}}^2} = (n-1)^2 \cdot g_{\mathrm{m2}}. \tag{2.5}$$

For the process used in sub-V_{t}, $n \approx 1.4$, meaning that the DTMOS configuration provides an additional 16% transconductance compared to gate input only.

Conventional common source ED biasing schemes use either a diode-connected load or a resistive load. Unfortunately, the diode connected load results in a low output resistance (similar to a source follower ED) and only achieves high conversion gain with large input signals, while a resistive load has limited conversion gain with a 0.4 V supply

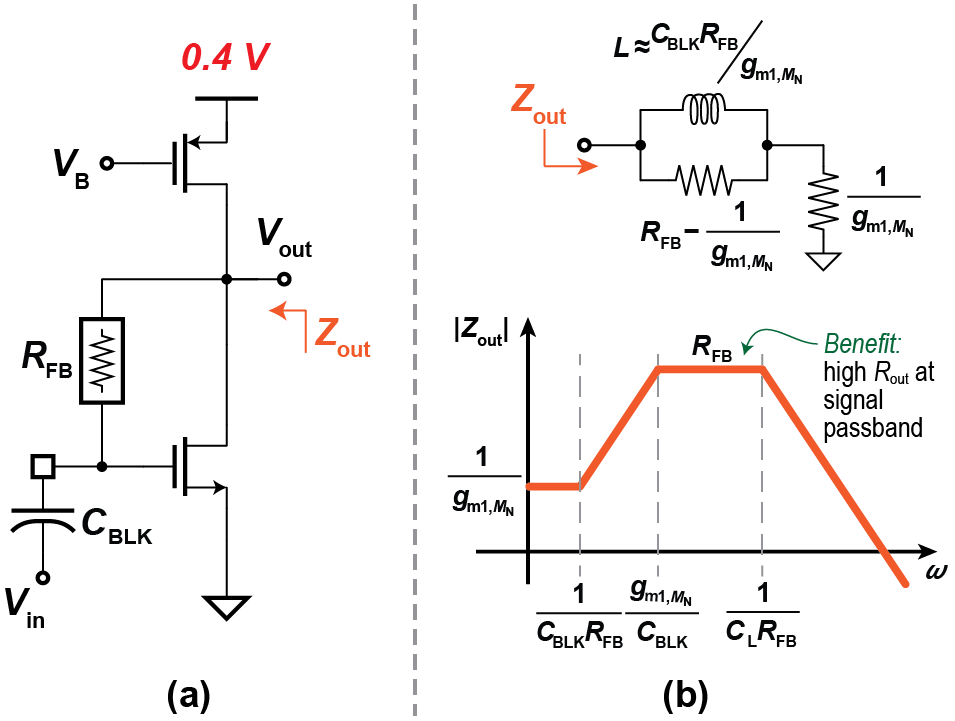


Figure 2.6: (a) Schematic of proposed active-L biased ED; (b) active-L biasing circuit model and Bode plot of ED output impedance.

voltage. Other techniques such as a cascode level shifter provide high output resistance, but require extra voltage headroom [29] not compatible with the employed 0.4 V supply.

To address the aforementioned issues, an active-L self-biased ED was designed (Fig. 2.6a). The feedback resistor sets the DC voltage for both the gate and drain nodes of the input transistor and serves as the output impedance. The output impedance can be written as:

$$Z_{\text{out}} = \left(\frac{g_{\text{m1}} + sC_{\text{BLK}}}{1 + sC_{\text{BLK}}R_{\text{FB}}} + \frac{1}{r_{\text{o}}} + sC_{\text{L}} \right)^{-1} \tag{2.6}$$

where g_{m1} is the transconductance of the NMOS, C_{BLK} is the AC-coupling capacitor, R_{FB} is the feedback resistor, r_{o} is the small-signal intrinsic output resistance of the transistor, and C_{L} is the capacitance at the output node. Assuming $r_{\text{o}} \gg 1/g_{\text{m1}}$ and R_{FB} because of the low current (5 nA in this design, which results in r_{o} ≈1 GΩ and $1/g_{\text{m1}}$ ≈7 MΩ), $C_{\text{BLK}} \gg C_{\text{L}}$, and $C_{\text{BLK}}/g_{\text{m1}} \gg C_{\text{L}}R_{\text{FB}}$, thus (2.6) can be simplified

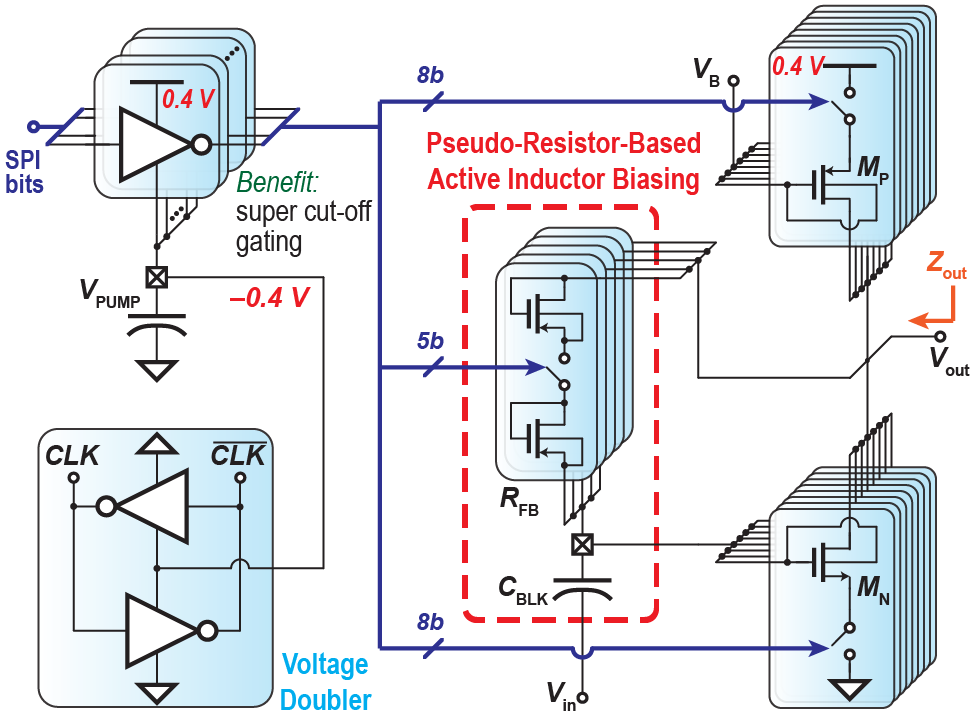


Figure 2.7: Full schematic of the proposed low-voltage active-L biased DTMOS ED with boosted binary-weighted SPI control.

to:

$$Z_{\text{out}} \simeq \frac{1}{g_{\text{m1}}} \cdot \frac{1 + sC_{\text{BLK}}R_{\text{FB}}}{\left(1 + s\frac{C_{\text{BLK}}}{g_{\text{m1}}}\right)(1 + sC_{\text{L}}R_{\text{FB}})}, \tag{2.7}$$

which contains two poles and one zero. The equivalent circuit model and Bode plot of Z_{out} are shown in Fig. 2.6(b). It can be seen that the output impedance is boosted to R_{FB} within the signal passband due to the active-L biasing, which leads to higher conversion gain. Since non-return-to-zero (NRZ) signaling is used, the high pass corner must be low enough to not attenuate the signal power and is set to 20 mHz in this design for $<$ 0.01 dB SNR degradation from baseline wander. Therefore, an off-chip C_{BLK} was used as a DC block and incorporated into the bias network.

The full ED schematic is shown in Fig. 2.7. Due to significant process variation in sub-V_{t} circuits, both M_{N} and M_{P} were designed to have 8-bit binary-weighted tuning capability. To reduce the leakage of unused M_{N} via super-cutoff biasing, and to turn on M_{P} strongly, a voltage doubler [38] was designed to provide -0.4 V, saving up to 3

nA in simulation (at the TT corner). Because of the high required value of the feedback resistor, a MOS-bipolar-pseudo-resistor was used instead of a poly resistor to prevent high capacitive loading of the input node at RF, which ultimately limits the achievable inductor value of the second stage of transformer/filter, and therefore passive voltage gain. For the same reasons as above, and to make the baseband bandwidth tunable, the pseudo-resistor was implemented with 5 binary-weighted bits. Since the baseband bandwidth is 300 Hz, all critical transistors were sized to trade-off the contributions of $1/f$ noise while minimizing parasitic capacitance at the output node, the latter of which ultimately limits the achievable R_{FB} to $\sim$100 MΩ.

The demodulated output signal of the ED is:

$$v_{\mathrm{out}} = Conv_{\mathrm{Gain}} \cdot v_{\mathrm{in}} = \frac{k_{\mathrm{ED}}}{2} \cdot v_{\mathrm{in}}^2, \tag{2.8}$$

where $Conv_{\mathrm{Gain}}$ is the conversion gain of the ED, v_{in} is the input signal amplitude, and k_{ED} is the ED scaling factor (in units of $1/V$). Combining (2.4), (2.5), and (2.7), the k_{ED} of the designed ED in the signal passband is given by:

$$\begin{aligned} k_{\mathrm{ED}} &= (g_{\mathrm{m2}} + g_{\mathrm{mb2}}) \cdot Z_{\mathrm{out}} \\ &\simeq [1 + (n-1)^2] \cdot \frac{I_{\mathrm{DS}}}{2(nV_{\mathrm{T}})^2} \cdot R_{\mathrm{FB}}, \end{aligned} \tag{2.9}$$

which is only dependent on design parameters.

To compare the two conventional biasing schemes with the proposed active-L biasing scheme, the SNR at the ED output was calculated. Assuming all three biasing schemes use the same DTMOS configuration as the input stage, the SNR can be written as:

$$SNR = \frac{(g_{\mathrm{m2}} + g_{\mathrm{mb2}})^2 \cdot \frac{v_{\mathrm{in}}^4}{4} \cdot R_{\mathrm{out}}^2}{\overline{i_{\mathrm{n,ED}}^2} \cdot R_{\mathrm{out}}^2 + \overline{v_{\mathrm{n,comp}}^2}}, \tag{2.10}$$

where $\overline{i_{\mathrm{n,ED}}^2}$ is the total integrated noise current of the ED input transistor, R_{out} is the output resistance in the passband, and $\overline{v_{\mathrm{n,comp}}^2}$ is the total input-referred noise of the

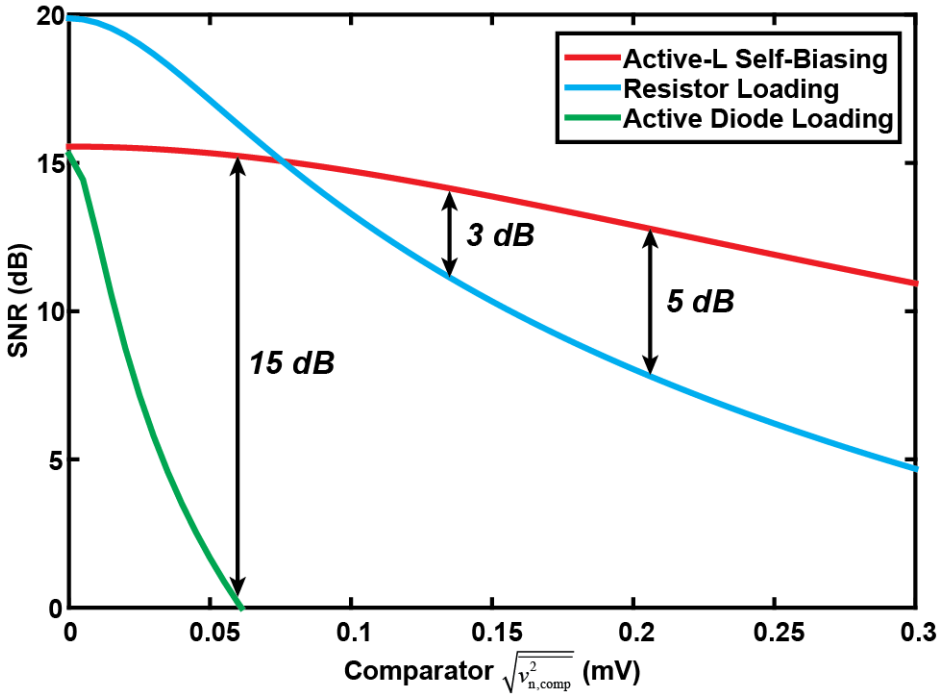


Figure 2.8: Simulated ED output SNR vs. integrated comparator noise voltage for different biasing schemes.

comparator. It can be shown that if the ED loading and comparator are noiseless, the SNR is independent of R_{out} and all the biasing schemes would have the same SNR. However, if $\overline{v_{\text{n,comp}}^2}$ is significant compared to the ED noise, higher R_{out}, and therefore higher k_{ED} lead to better SNR. Simulation with an ED current of 5 nA and a 3.2 mV input signal for these three bias schemes is depicted in Fig. 2.8. If the comparator noise is large, the active-L self-biased scheme achieves the highest SNR.

2.3.3 Comparator and S/H stage

The output of the ED is digitized by a comparator, which serves as a 1-bit quantizer. Due to the $2\times$ oversampling, the comparator operates at 600 Hz. The comparator is implemented with a $g_{\text{m}}C$ integrator as a preamplifier followed by a regenerative latch [39]. The operation is as follows: 1) Once $\overline{\phi}$ goes low, a current determined by the inputs is integrated on C_{F} until 2) the voltage crosses the latch threshold voltage,

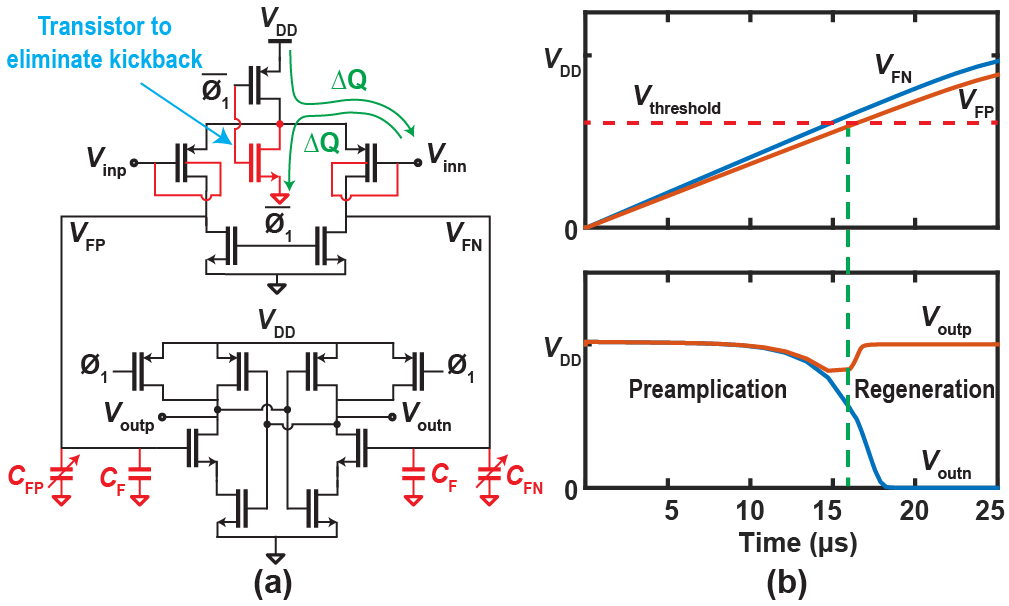


Figure 2.9: (a) Schematic of the dynamic two-stage comparator, and (b) simulation showing $1^{st}/2^{nd}$ stage output voltages.

$V_{\text{threshold}}$, after which the positive feedback latch regenerates producing complementary rail-to-rail outputs. The two-stage dynamic comparator is then reset by the other phase of the clock and ready for the next cycle.

The preamplifier is typically designed with a moderate integration gain of $\sim$5 V/V to suppress the latch input-referred noise. Therefore, the preamplifier usually dominates the noise performance of the entire comparator. As can be observed in [39], adding matched capacitance at the preamplifier output prolongs the integration time and limits preamplifier noise bandwidth, which effectively reduces the comparator noise. In this design, a 480 fF MIM capacitor was used and placed in a common-centroid manner to ensure good matching. Compared to the same comparator without explicitly loading the preamplifier, the noise power is reduced by $8\times$ while the power consumption increases by only $5\times$ in simulation because of the $C_{\text{F}}V_{\text{DD}}^2$ energy. Since the comparator is operating at a low speed and the dynamic power of the preamplifier is minimal, loading the preamplifier results in a good noise versus power trade-off. Moreover, as shown in Fig. 2.9(a), the input pair also uses a DTMOS configuration, which increases

the transconductance resulting in a lower input-referred noise at no power cost. Simulation shows that the effective transconductance increases by 51% and the noise power reduces by 66%. With the help of loading preamplifier and increased transconductance, the simulated comparator noise was suppressed from 505 $\mu\mathrm{V_{RMS}}$ to 104 $\mu\mathrm{V_{RMS}}$.

The comparison threshold voltage is tuned with a dual 5-bit binary weighted capacitor DAC (CDAC) in parallel with C_{F}. By changing the loading capacitance, the comparator offset voltage changes accordingly. Assuming the capacitance difference between the two outputs (ΔC_{F}) is much less than C_{F}, the comparison threshold voltage can be written as

$$v_{\mathrm{os,DAC}} = \frac{\Delta C_{\mathrm{F}}}{C_{\mathrm{F}}} \cdot n \cdot V_{\mathrm{T}}. \tag{2.11}$$

Thus, the threshold voltage increases linearly with ΔC_{F}, and is constant after the CDAC is configured. The CDAC is using MOM capacitors with a unit capacitance of 3.7 fF (C_{F}=0.65 pF), corresponding to $\sim$200 μV resolution. A reference ladder provides a voltage reference to the negative terminal of the comparator. The reference ladder contains 64 diode-connected PMOS transistors in series. A 5-bit mux selects the output node as the reference voltage, providing a tuning step size of 6.25 mV and a range of 200 mV.

The biggest challenge with this dynamic architecture is the comparator kickback via C_{gs}, C_{bs}, C_{gd}, and C_{bd}. Due to the unbalanced output impedances of the ED ($\sim$100 MΩ||1.7 pF) and the reference ladder ($\sim$2 GΩ||50 pF), the kickback charge introduces unequal voltage perturbations. This voltage difference would lead to a comparison error in subsequent cycles since the time constant at both nodes is much larger than one clock period. To eliminate this error, two techniques were implemented: 1) An additional reset transistor was placed at the source of the input pair, which insures that the V_{gs} always resets to V_{DD}, such that the same amount of charge is injected into the input when ϕ is asserted high and is removed when ϕ is deasserted (Fig. 2.9). This results in zero net kickback charge into the ED and reference ladder during each cycle, preventing incomplete settling. 2) A S/H stage was added in front of the comparator that provides

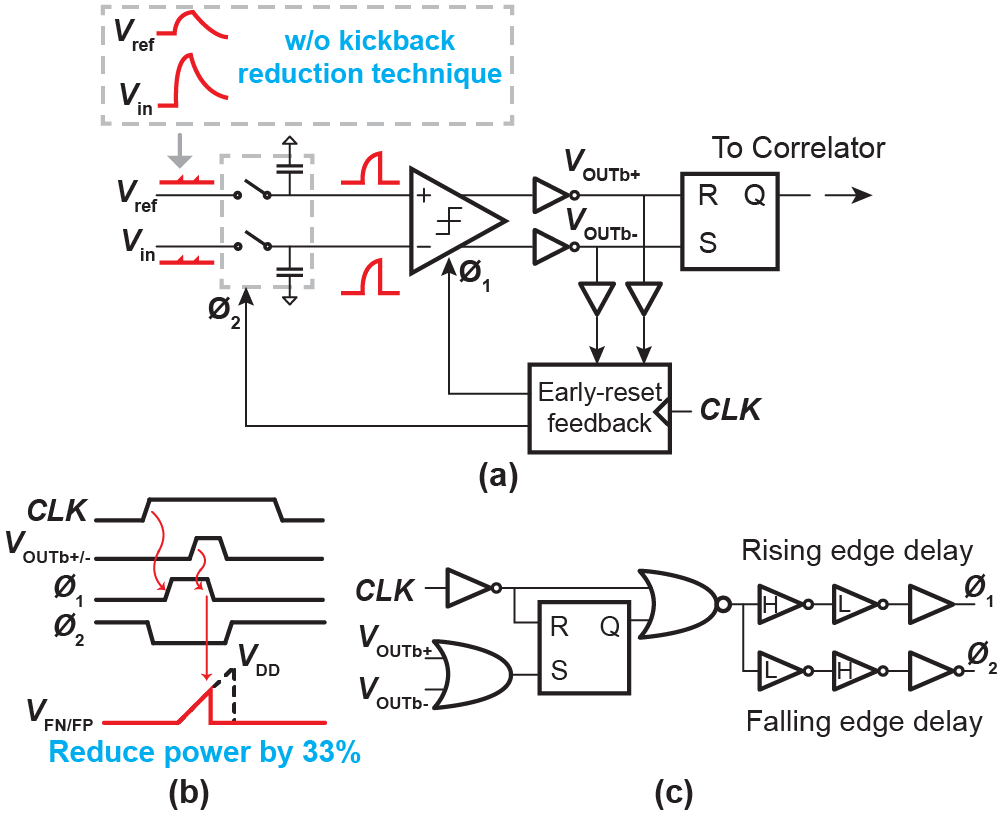


Figure 2.10: (a) Schematic of the comparator, S/H stage and clocking; (b) timing diagram of the of the early-reset feedback; (c) schematic of the early-reset feedback

matched impedances for both inputs and temporarily stores the kickback charge. The sampling capacitor is 1.9 pF, much larger than the parasitic capacitance of the input transistor. Therefore, the only kickback effect is a $\sim$2 mV common-mode spike at the comparator input, which does not lead to a comparison error. The sampling capacitor and the ED output capacitance limit the baseband bandwidth to 300 Hz.

An early-reset feedback was implemented to efficiently generate a two phase non-overlapping clock and save comparator dynamic power simultaneously. As illustrated in Fig. 2.10, the comparator resets once the comparator output is latched, such that the dynamic power of the integrator is reduced from $2fC_{\mathrm{F}}V_{\mathrm{DD}}^2$ to $2fC_{\mathrm{F}}V_{\mathrm{threshold}}^2$. Since a large capacitance C_{F} is added, the power savings are significant. Simulation shows that 33% of total comparator power is saved when the WuRX RF input power is -69 dBm, or 0.7 mV at the comparator input. The early-reset feedback was implemented

as shown in Fig. 2.10(c), where an SR-latch captures the rising edge of either $V_{\mathrm{outb+}}$ or $V_{\mathrm{outb-}}$ and asserts CLK to "low" to turn off the integration. The non-overlapping phases are generated with two inverter chains: one creates a pos-edge delay and the other creates a neg-edge delay. The pos-edge delay was created by four cascaded inverters, where the first was designed to be high-skewed followed by a low-skewed inverter with $W_{\mathrm{P}}/W_{\mathrm{N}}$ of 6 and 0.5, respectively. Similarly, the neg-edge delay was created by flipping the order of the skewed inverters. Compared to a conventional two-phase clock generator where cascaded latches are used, this method has lower power consumption with a 0.4 V supply.

2.3.4 Digital Baseband

Fig. 2.11 shows the digital baseband correlation logic that processes the incoming data from the comparator. With the lack of a power hungry PLL for synchronization, the correlator provides an energy efficient way to overcome phase asynchronization by operating with a 2× oversampling rate to sample the incoming bits [40]. An optimal 16-bit code sequence (1110101101100010) was designed such that it has both a large Ham-

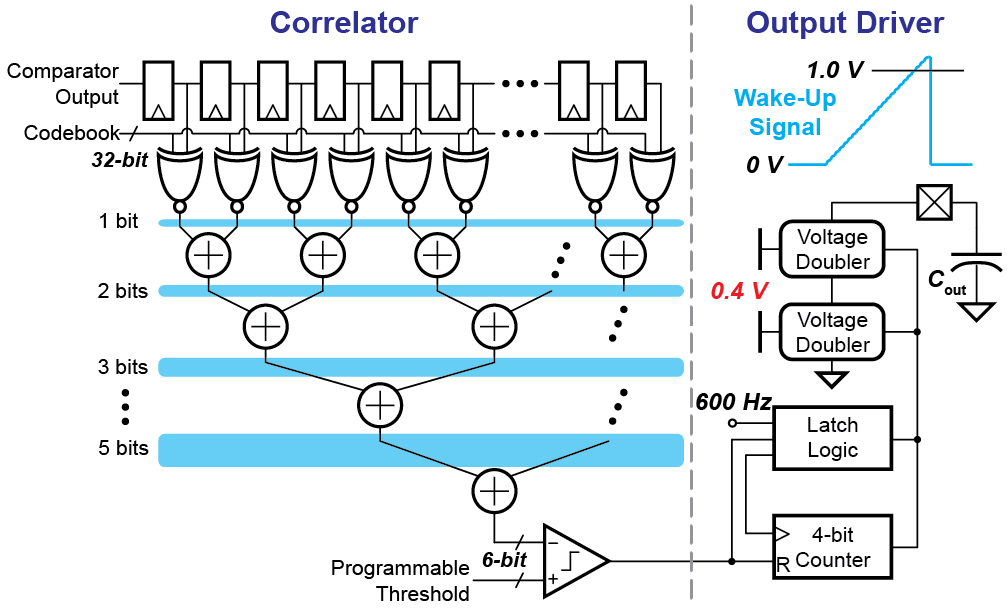


Figure 2.11: Digital correlator baseband logic with wake-up signal output driver.

ming distance from all of its shifted versions (D=9) and from the all-0 sequence (D=9). A family of codes also exists, but with slightly lower Hamming distances (D$\leq$8). As the input sequence shifts along the D flip-flop chain, the correlator computes the Hamming distance between the sequence and the programmable 32-bit oversampled code book. Once the value is below a preset threshold, the desired pattern is declared detected and the correlator generates a wake-up signal. To drive the main receiver with a higher supply voltage, the output driver was designed to generate a >1 V signal with 5 ms duration assuming a 10 pF load. When the correlator sends a wake-up signal to the driver, it resets a 4-bit counter and the signal is latched to leave the cascode voltage doubler enabled until the counter rolls over. The charge pump and counter make the wake-up signal look like a ramp. Also, to use the same 0.4 V supply, the digital baseband operates in the sub-$V_{\rm t}$ region and a custom logic gate library using thick oxide device was designed. All the gates were designed using only inverters and transmission gates for the highest robustness in subthreshold [41].

From a static performance perspective, digital logic gates operating in the sub-$V_{\rm t}$ region need extra attention to the transistor sizing to overcome process variation. To see this, the inverting threshold $V_{\rm M}$ of an inverter with minimum width and length NMOS was simulated across the width of the PMOS at different process corners (Fig. 2.12a), where the solid and dashed lines correspond to a 0.4 V and 1.0 supply voltage, respectively. For an ideal inverter with a negligible transition region, the noise margin is equal to the lower value of either $V_{\rm M}$ or $V_{\rm DD}-V_{\rm M}$. It can be seen that the inverter maintains larger than 30% $V_{\rm DD}$ noise margin when operating above-$V_{\rm t}$ across all corners, while it fails when operating in the sub-$V_{\rm t}$ region without proper sizing. Another important design consideration comes from power dissipation. For a digital circuit, it is well known that the power consumption can be written as:

$$P_{\rm tot}=P_{\rm leak}+P_{\rm dyn}=V_{\rm DD}I_{\rm leak}+\alpha C_{\rm L}V_{\rm DD}^2 f, \tag{2.12}$$

where $I_{\rm leak}$ is the average leakage current, α is the activity factor, $C_{\rm L}$ is the load capaci-

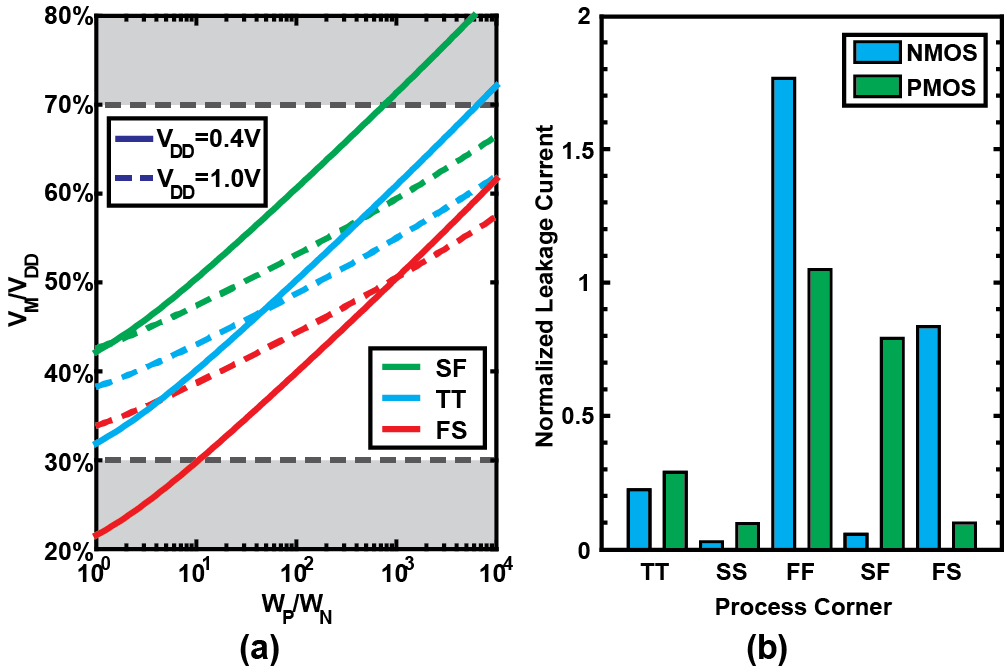


Figure 2.12: (a) Simulated switching threshold for inverter with minimum width and length across different corners and supply voltages; (b) simulated normalized leakage current of the designed inverter across corners.

tor, and f is the clock rate.

In addition to the low clock rate, since ideally the correlator only computes when the signal pattern changes, α is nearly zero, both of which make leakage power dominant and thus the design target here. To equate the NMOS and PMOS leakage in this process where the PMOS has lower mobility and V_{t} is 90 mV higher than an NMOS in the TT corner, 5$\times$ NMOS devices are stacked. Moreover, the PMOS is re-sized to 1.6$\times$ larger width to achieve 30% V_{DD} noise margin even in the worst case FS corner. Fig. 2.12(b) shows the leakage current of the designed inverter across corners, which is normalized to the leakage current of a minimum size inverter at TT. The normalized I_{leak} is 0.26 in the TT corner and 1.41 in the FF corner.

2.3.5 Relaxation Oscillator

The system clock for the comparator, digital baseband, and charge pump is generated from a relaxation oscillator. As shown in Fig. 2.13, the oscillator is composed of a reference generator, where one branch is shared with a pseudo-differential common-gate comparator, an inverter buffer chain, and a reset switch. The reference generator with all four transistors operating in the sub-V_{t} region, generates a reference current I_{REF} and a reference voltage V_{REF} through an off-chip resistor. I_{REF} is used to charge a MIM capacitor that is connected to a common-gate comparator (shown in the dashed box). The comparator output is pulled high after V_{INT} exceeds V_{REF}. Then the inverter chain is triggered to close the reset switch and reset the integration capacitor. The capacitor is charged and discharged periodically with a period of $\sim RC$. The clock buffer was implemented with current-starved inverters whose delay are determined by the I_{REF}, which has better energy efficiency than dynamic inverters (CV_{DD}^2). Since the power consumption is largely determined by the static power of the reference generator and comparator, the oscillator power consumption can be minimized by using a large bias resistor. The resistor was chosen to be 30 MΩ and I_{REF} to be $\sim$0.5 nA. To compensate

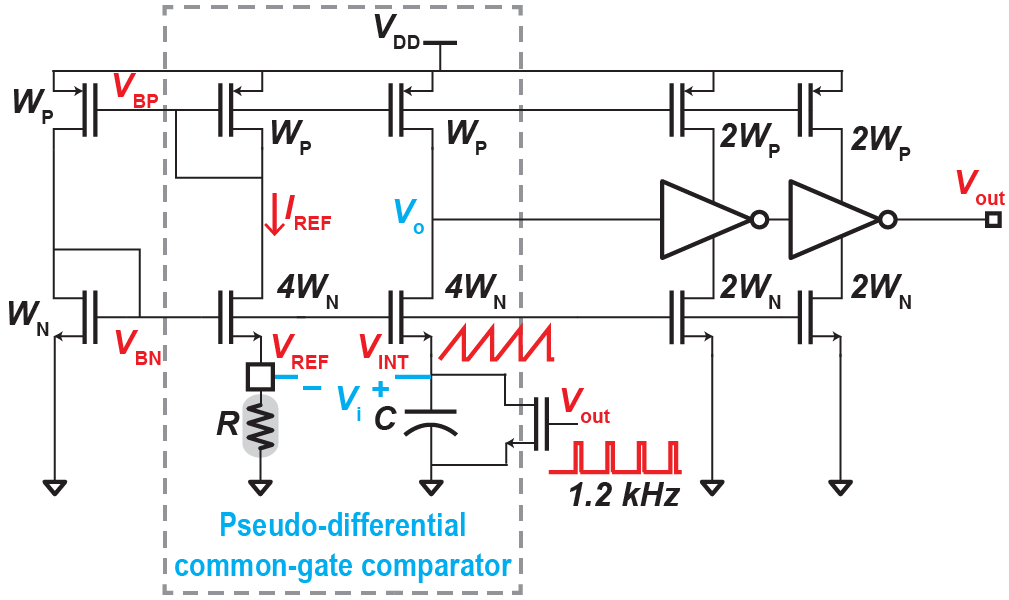


Figure 2.13: Schematic of the relaxation oscillator.

the variation of the capacitor value and comparator delay, the off-chip resistor is tuned to adjust the oscillation frequency to 1.2 kHz. The oscillator output is divided and buffered to a 600 Hz system clock with 50% duty cycle. The frequency varies from 617 Hz to 585 Hz, when the supply voltage changes from 0.35 V to 0.45 V. This corresponds to 5.3% frequency change when the supply changes by 25%. When the temperature changes by 10°C, the frequency changes by 4.9%. The supply and temperature sensitivity are mainly caused by the comparator delay and digital buffer delay. The 2× oversampling scheme and short data sequence (53.3 ms) make the system insensitive to clock mismatch. Based on system level Monte Carlo simulations where the clock mismatch is modeled as normal distribution with 1.5% standard deviation (i.e., 99.7% samples are within +/-4.5% clock mismatch), the sensitivity deviation is less than 0.5 dB.

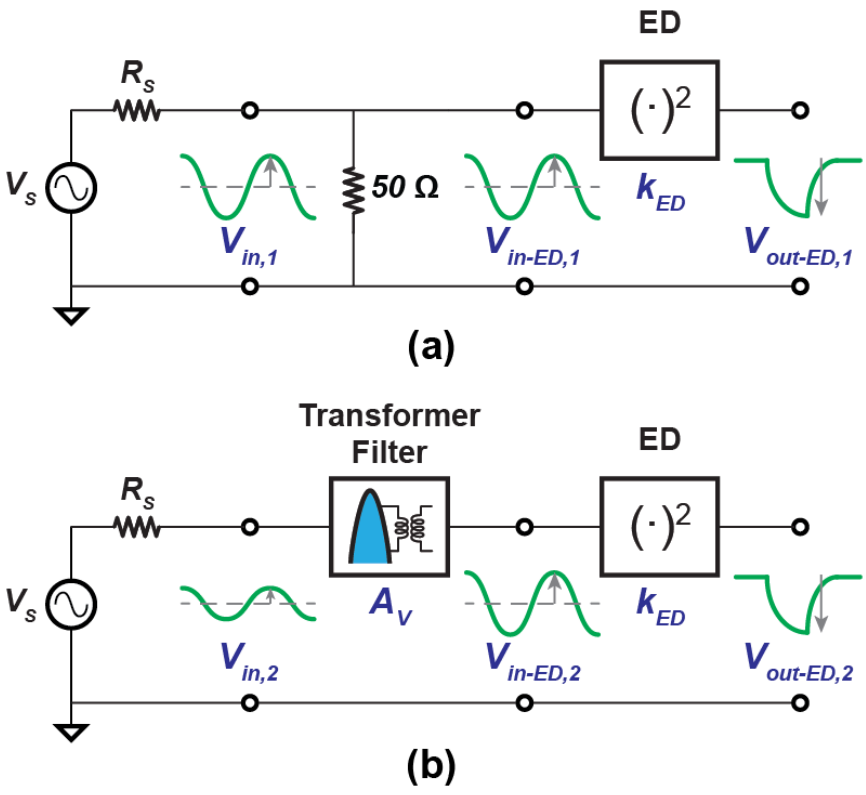


Figure 2.14: Measurement setup for measuring transformer filter gain.

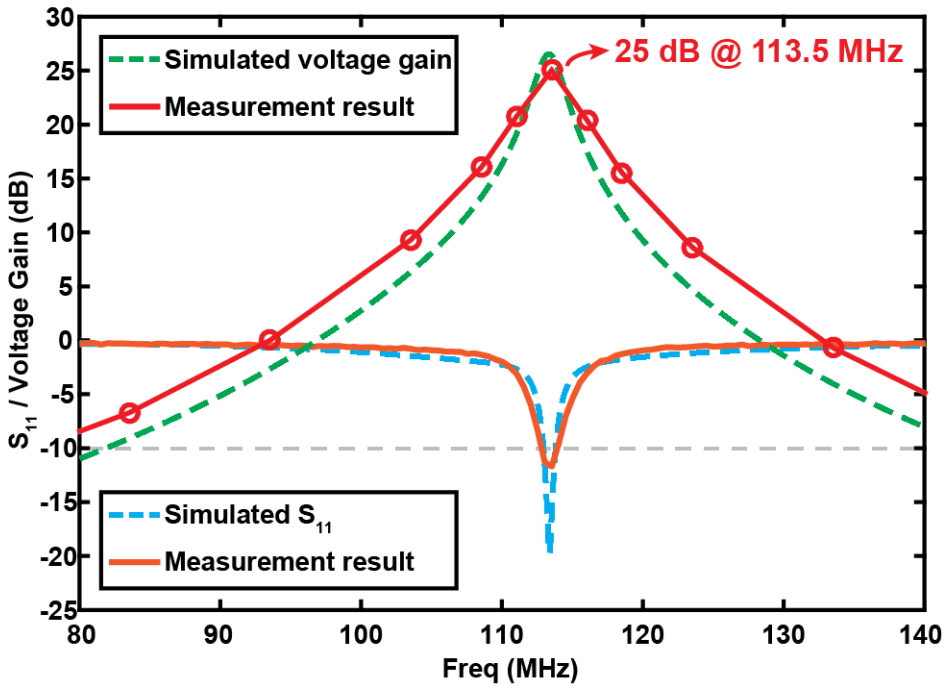


Figure 2.15: Simulated and measured transformer S_{11} and voltage gain.

2.4 Measurement Results

To characterize the passive voltage gain from the transformer/filter, a conventional 2 port measurement such as S_{21} using a vector network analyzer (VNA) is not possible due to the high (i.e., non-50 Ω) output impedance. Instead, we first characterized the ED by connecting a 50 Ω load at the input without the transformer to provide matching and measured the output voltage after applying a known input signal, as shown in Fig. 2.14(a). We then replaced the 50 Ω resistor with the transformer and again measured the output voltage, as shown in Fig. 2.14(b). The transformer gain was then calculated using

$$A_{\mathrm{V}} = \frac{V_{\mathrm{in},1}}{V_{\mathrm{in},2}} \cdot \sqrt{\frac{V_{\mathrm{out-ED},2}}{V_{\mathrm{out-ED},1}}}. \tag{2.13}$$

Using the above procedure, $A_{\mathrm{V}} = 25$ dB was measured, which is in agreement with simulation results (Fig. 2.15). S_{11} measurements show excellent matching at the

signal frequency (113.5 MHz), and is also in agreement with simulations.

The measured conversion gain, $Conv_{\mathrm{Gain}}$, and scaling factor, k_{ED}, versus ED input swing $V_{\mathrm{in-ED,1}}$ for different ED bias current settings are shown in Fig. 2.16. While the $Conv_{\mathrm{Gain}}$ is proportional to $V_{\mathrm{in-ED,1}}$ as shown in Fig. 2.16(a), Fig. 2.16(b) shows that k_{ED} is independent of $V_{\mathrm{in-ED,1}}$, which is expected from (2.8) and (2.9). When the ED is configured for 2 nW (i.e., 1$\times$ ED) with 4 parallel feedback units (i.e., 1/4$\times$ $R_{\mathrm{FB,unit}}$) to achieve a 300 Hz low pass corner, k_{ED} =180.8 (1/V). Using 1/3$\times$ $R_{\mathrm{FB,unit}}$ and 4$\times$ ED, the ED achieves k_{ED} =728 (1/V), which is $\sim$ 4$\times$ larger than the 1$\times$ ED configuration, as expected. At higher powers (e.g., 40$\times$ ED), r_{o} dominates, and thus the improvement in k_{ED} saturates.

The comparator noise was measured by sweeping the input differential voltage and fitting the resulting distribution. Since the comparator noise is mostly white, fitting with a Gaussian distribution allows the noise and offset to be extracted. Nine chips were measured with the input-referred noise varying from 89 μV_{RMS} to 95 μV_{RMS}, slightly lower than the simulated value at the TT corner due to process variation. The measured offset varied from 0.69 mV to 1.16 mV, which is easily covered by the 5-bit tuning range of comparator CDAC.

The performance of the kickback reduction technique was validated by measuring the output voltage of the reference ladder, which connects to one of the comparator inputs, with the transmitted signal at the other input. Since this is a very high impedance node ($\sim$2 GΩ||50 pF), a unity-gain buffer with low input bias current was used to buffer the voltage. The measured data are shown in Fig. 2.17, where the sample (S) and hold (H) phases are annotated. Only small spikes appear during the H phase that are due to the leakage of the sampling switch since the switch off-resistance is not significantly larger than the reference ladder impedance. The spikes always settle before the beginning of the next cycle owing to the zero net charge kickback, and as such do not affect the following comparisons.

Fig. 2.18(a) shows the measured power breakdown of the WuRX. The total power consumption is 4.5 nW when the ED is set to 2.0 nW. Transient waveforms shown

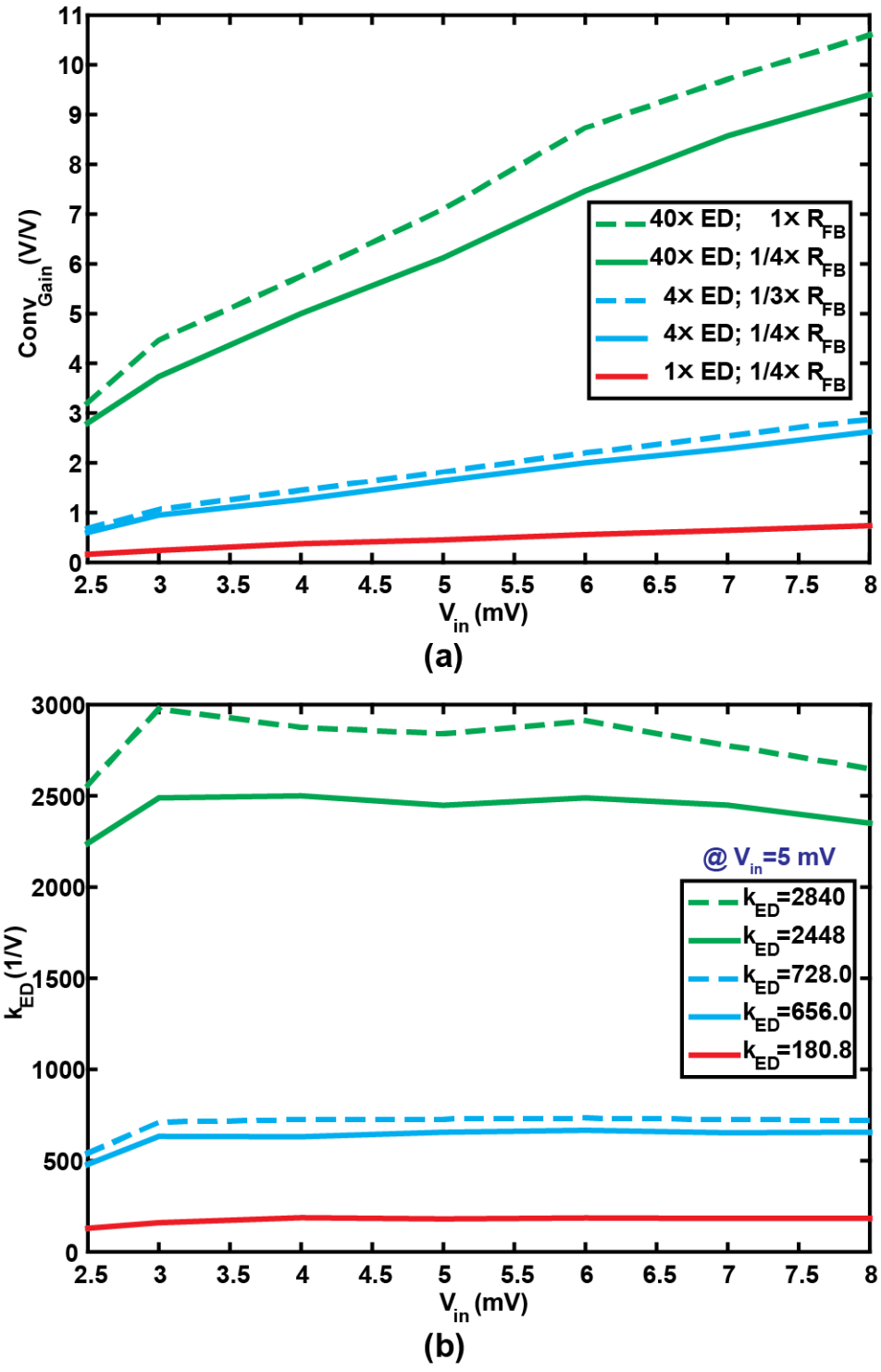


Figure 2.16: Measurement results showing (a) ED conversion gain; (b) Scaling factor k_{ED}.

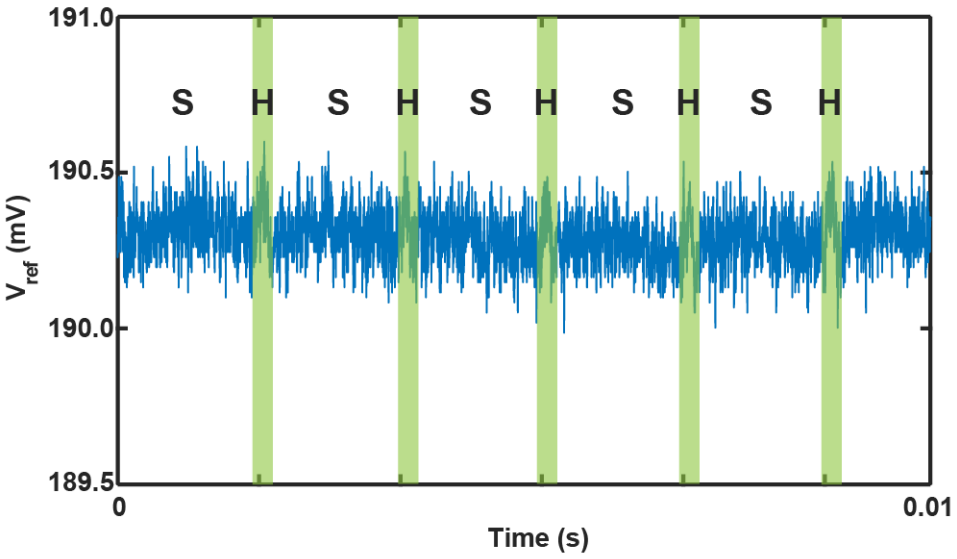


Figure 2.17: Measured reference ladder output voltage with sample and hold phases annotated.

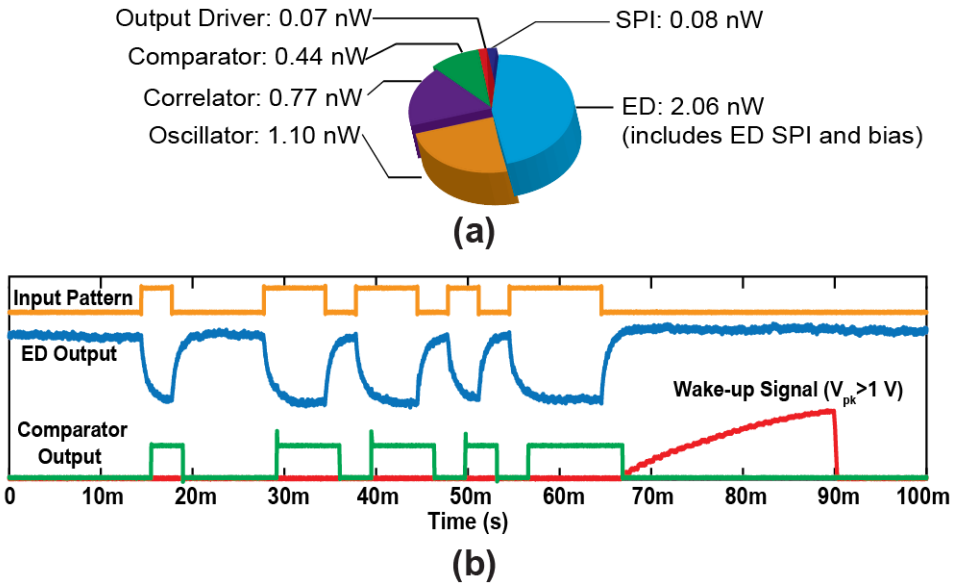


Figure 2.18: (a) System power breakdown pie chart; (b) transient waveforms at each node.

in Fig. 2.18(b) demonstrate correct detection when the correct code is transmitted.

Fig. 2.19 shows the waterfall curves for conventional bit error rate (BER) measured at the comparator output, and the wake-up signal missed detection rate (MDR) measured after the digital BB logic. The BER was measured under the assumption of perfect synchronization between clock and input data, while the MDR was measured

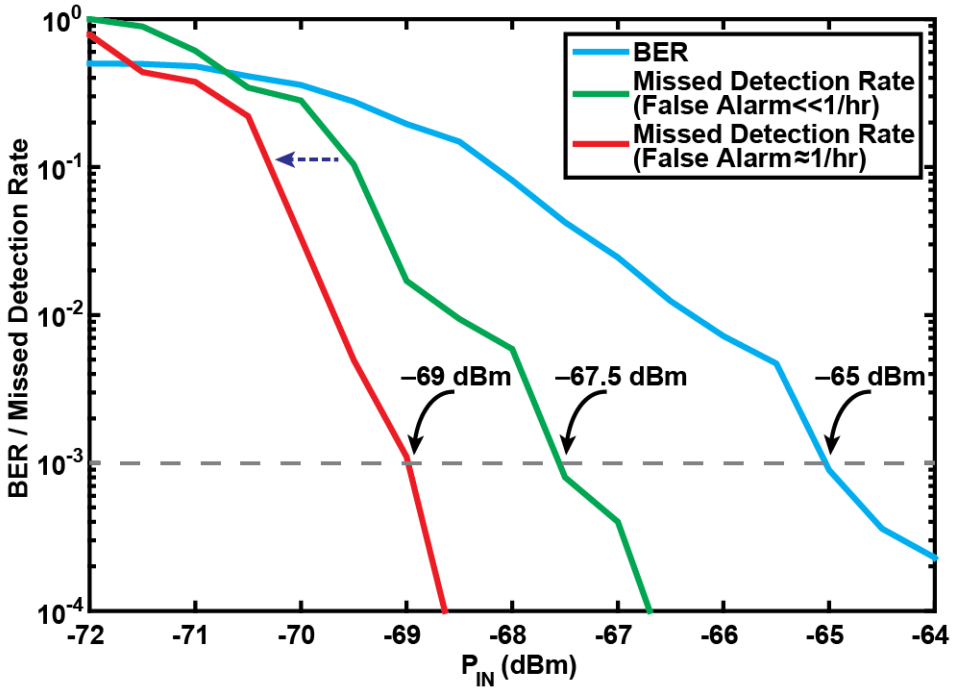


Figure 2.19: BER and MDR waterfall curves with a 300 bps data rate.

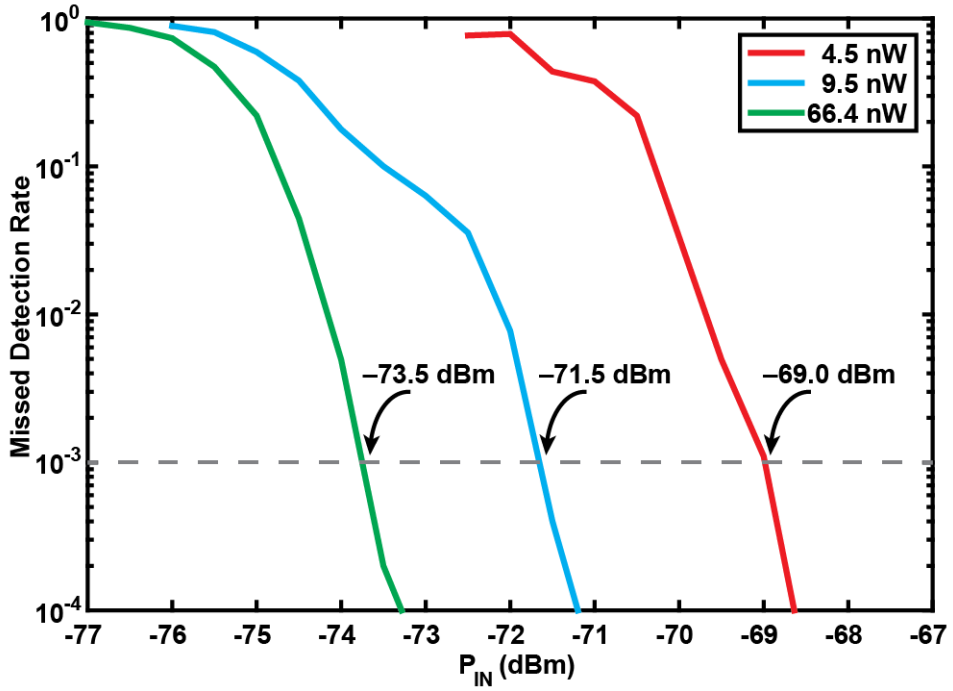


Figure 2.20: MDR waterfall curves for different power settings with a 300 bps data rate.

with random (i.e., not synchronized) transmission. To achieve a BER $= 10^{-3}$, the input signal power $P_{\text{IN}} = -65$ dBm. With the same comparator and correlator threshold, $P_{\text{IN}} = -67.5$ dBm for MDR $= 10^{-3}$ with a false alarm rate of $\ll$ 1/hr. By adjusting the comparator threshold, $P_{\text{IN}} = -69$ dBm was achieved for MDR $= 10^{-3}$ with a false alarm rate of $\approx$ 1/hr, which is where the sensitivity P_{SEN} is defined, and 4 dB coding gain is shown compared to the BER measurement. MDR measurements were also taken at higher power ED settings (Fig. 2.20). For the 4$\times$ ED case, $P_{\text{SEN}} = -71.5$ dBm and the power consumption is 9.5 nW. For the 40$\times$ ED case, $P_{\text{SEN}} = -73.5$ dBm and the power consumption is 66.4 nW.

A modulated signal tone along with a pseudo-random binary sequence (PRBS) modulated or continuous wave (CW) jammer at frequency offset Δf to the signal center frequency were used to test WuRX performance under interference. The input signal power was set to 1 dB higher than the power where BER $= 10^{-3}$ (i.e., at -64 dBm), and the interferer power at Δf was swept until BER$= 10^{-3}$. The signal to interferer

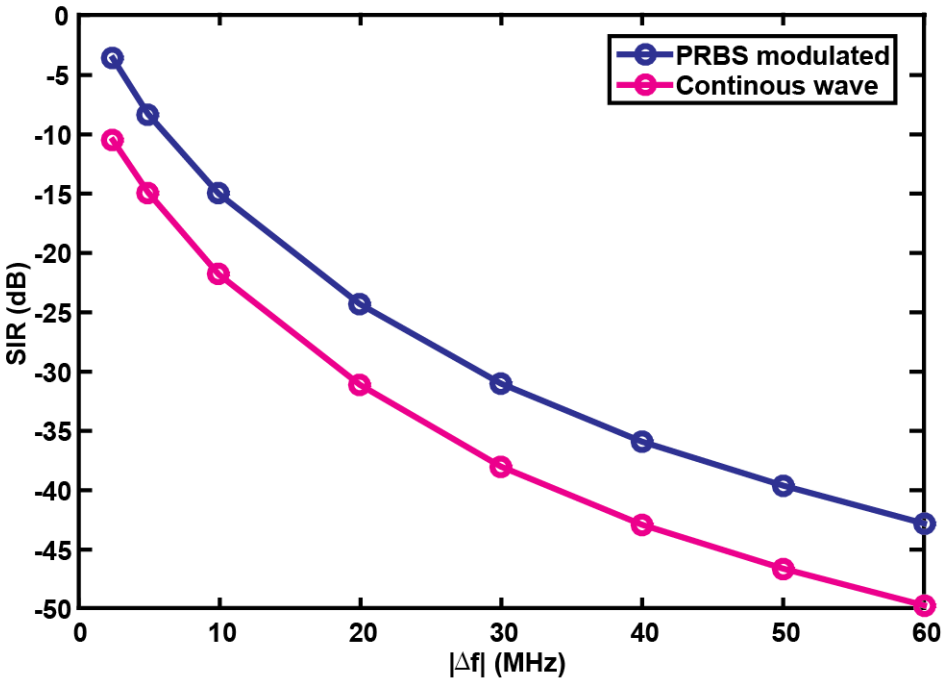


Figure 2.21: SIR curve vs. interferer frequency offset $|\Delta f|$ to carrier frequency for a worst-case 300bps PRBS-modulated jammer and a CW jammer.

ratio (SIR) vs. $|\Delta f|$ is depicted in Fig. 2.21. Because of the high-Q nature of the transformer/filter, for PRBS jammer a SIR< -30 dB was achieved at $|\Delta f| = 30$ MHz. At the chosen FM band, since a narrow-band FM signal would look like a CW jammer and only causes a DC tone at the ED output, an additional 7 dB rejection compared to a PRBS jammer was achieved. Moreover, a CW jammer is unlikely to cause a false alarm due to the correlator. Therefore, by designing a longer-bit correlator, the code space can be increased, which not only improves interferer resilience further in terms of false alarms, but also enables more WuRXs with different wake-up codes in the sensor network. The die micrograph along with the whole system photograph are shown in Fig. 2.22.

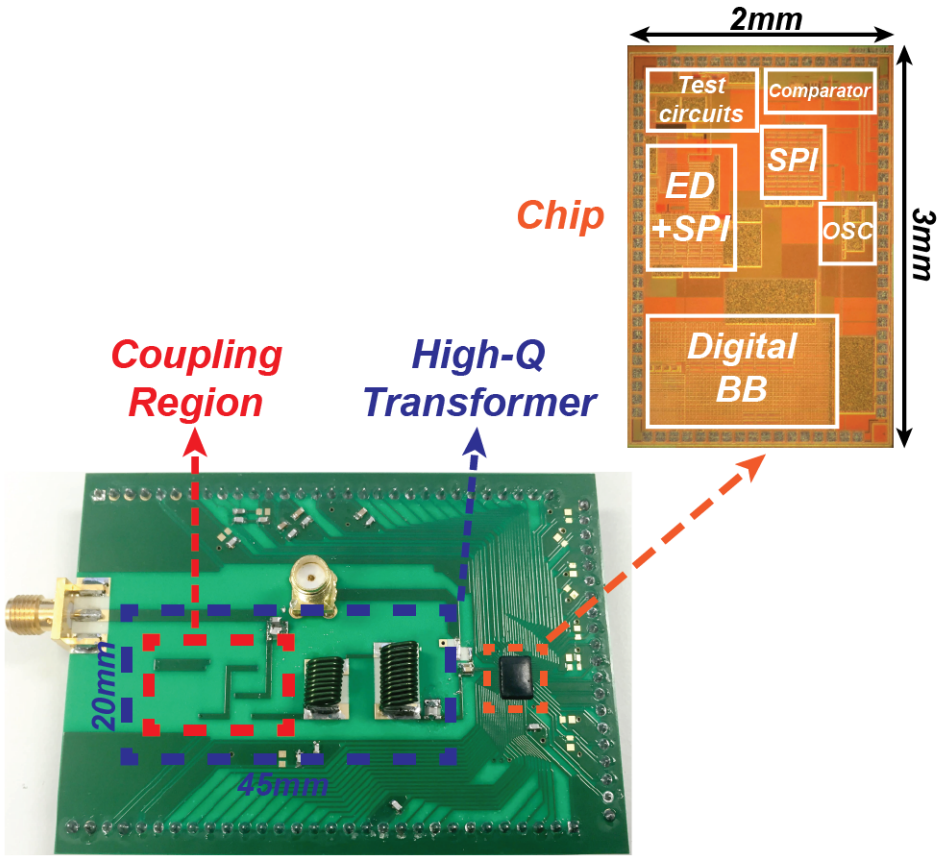


Figure 2.22: Picture of annotated die micrograph (top); whole WuRX (bottom).

2.5 Figure of Merit and Comparison

As discussed in Section 2.1, for WuRXs used in low-average-throughput applications, power consumption and sensitivity are the most important metrics, and thus the following FoM is defined:

$$FoM_{\mathrm{LAT}}(dB) = -P_{\mathrm{SEN}} - 10\log\frac{P_{\mathrm{DC}}}{1mW}, \tag{2.14}$$

where P_{SEN} is the sensitivity in dBm and P_{DC} is the power consumption. For high-average-throughput applications, data rate is important. Therefore, the following FoM is used:

$$FoM_{\mathrm{HAT}}(dB) = -P_{\mathrm{SEN,norm}} - 10\log\frac{P_{\mathrm{DC}}}{1mW}, \tag{2.15}$$

where $P_{\mathrm{SEN,norm}}$ is the sensitivity normalized to data rate and calculated using one of the following equations:

$$P_{\mathrm{SEN,norm}}(dB) = P_{\mathrm{SEN}} - 5\log BW_{\mathrm{BB}}, \tag{2.16}$$

$$P_{\mathrm{SEN,norm}}(dB) = P_{\mathrm{SEN}} - 10\log BW_{\mathrm{BB}}, \tag{2.17}$$

where $5\log BW_{\mathrm{BB}}$ in (2.16) is used for designs with a non-linear squaring function for envelope detection [9, 25, 28–30, 32, 42–48], and $10\log BW_{\mathrm{BB}}$ in (2.17) is used for designs with a linear operation to demodulate the signal [24, 27] or designs using a non-linear squaring function for envelope detection after high active pre-ED gain with sharp filtering [23, 26] (i.e., where convolution noise dominates [32]). A survey of prior-art WuRXs is shown in Fig. 2.23 for both FoMs. The low baseband bandwidth and high passive RF gain afforded by the high input impedance ED and FM-band high-Q passives enabled the proposed design to achieve an $FoM_{\mathrm{LAT}} = 122.5$ dB, which is over an order of magnitude higher than prior works. For high-average-throughput applications where data rate is important, while this design achieved the best $FoM_{\mathrm{HAT}} = 134.9$ dB among the direct ED architectures, mixer-based architectures achieved comparable, and in some

cases better, FoM_{HAT} at the expense of four decades higher power consumption. Table 2.1 summarizes the measurement results of the proposed WuRX design and compares the results to the state-of-the-art WuRXs.

2.6 Conclusions

In this chapter, a 0.4 V 113.5 MHz OOK-modulated WuRX that achieves -69 dBm sensitivity consuming only 4.5 nW in a 0.18 μm SOI CMOS process is presented. The WuRx was designed for emerging event-driven low-average-throughput applications to reduce system power. While conventional direct envelope detection architectures can achieve low power at moderate sensitivities, this design breaks the conventional trade-off to achieve ultra-low power with high sensitivity by: 1) reducing the baseband signal bandwidth to 300 Hz; 2) modulating OOK signal with a custom designed 16-bit code sequence to get 4 dB coding gain; 3) employing an off-chip high-Q transformer/filter with 25 dB passive voltage gain enabled by an ED with high input impedance; 4) achieving higher conversion gain using an active-L biased ED; 5) digitizing the ED output via a regenerative comparator with kickback elimination; 6) decoding the received OOK signal using a high-V_{t} subthreshold digital baseband correlator, operating with $2\times$ oversampling to overcome phase asynchronization, where the clock is generated by a 1.1 nW relaxation oscillator.

This chapter is based on and mostly a reprint of the following publications: H. Jiang, P.-H. P. Wang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, D. A. Hall, and P. P. Mercier, A 4.5nW wake-up radio with -69dBm sensitivity, *IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2017, pp. 416-417, and P.-H. P. Wang, H. Jiang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, P. P. Mercier, and D. A. Hall, "A Near-Zero-Power Wake-Up Receiver Achieving -69-dBm Sensitivity," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1640-1652, June 2018. The dissertation author is the primary author of these materials, and co-authors have approved the use of the material for this dissertation.

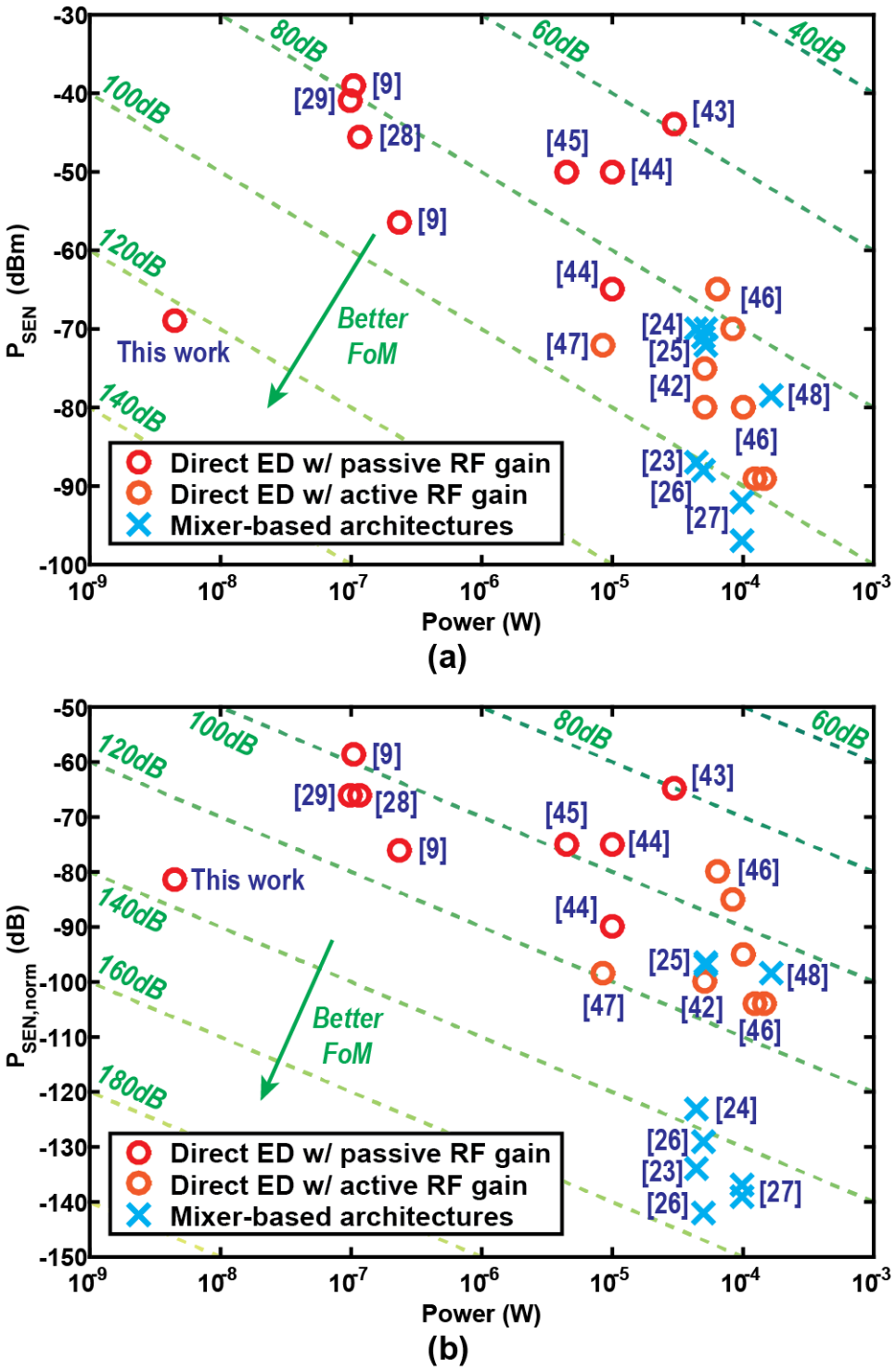


Figure 2.23: (a) Sensitivity vs. Power (FoM_{LAT}); (b) Sensitivity normalized to data rate vs. Power (FoM_{HAT}).

Table 2.1: Comparison With Previously Published State-of-the-Art WuRXs

	[25] JSSC'09	[42] ISSCC'10	[24] ISSCC'11	[28] CICC'13	[27] JSSC'16	[9] ISSCC'16		**This Work**
Technology	90 nm	90 nm	130 nm	130 nm	65 nm	65 nm		**180 nm**
Carrier Frequency	2 GHz	915 MHz	402 MHz	403 MHz	2.4 GHz	2.4 GHz		**113.5 MHz**
Modulation	OOK	OOK	FSK	OOK	OOK	OOK		**OOK**
Supply Voltage	0.5 V	1 V	1 V	1.2/0.5 V	0.5 V	1/0.5 V		**0.4 V**
Digital Correlator	No	No	No	31-bit	No	31-bit		**32-bit**[1]
External Components	BAW filter	L for MN + LNA loading	XTAL + LC MN	XTAL + LC MN	BGA SMD L	XTAL + MN		**Transformer/filter**
Oscillator	Ring osc.	No	Inj-locked osc.	XTAL osc.	LC DCO	XTAL osc.		**Relaxation osc.**
Gain Stage(s)	IF[2]	RF/BB[2]	IF[2]	ED[2]	IF/BB[2]	ED[2]	ED/BB[2]	**TF/ED/BB**
Interferer Rejection	BAW filter	LC MN + LNA loading	LC MN + IF filter	LC MN + correlator	LC MN + N-path filters	Digital processor		**Transformer/filter + correlator**
SIR (dB) @ $\lvert\Delta f\rvert$	> -5 @ 10 MHz[3]	N/A	N/A	$+3.3$ N/A	$-31/-27$ @ 5 MHz[3]	N/A		$\mathbf{-15}$ **@ 5 MHz**[4]
Data Rate	100 kbps	10 kbps	200 kbps	12.5 kbps	10 kbps	8.192 kbps		**0.3 kbps**
Energy/bit	520 pJ	5100 pJ	220 pJ	9.3 pJ	9900 pJ	12.7 pJ	28.8 pJ	**15.0 pJ**
Sensitivity	-72 dBm	-80 dBm	-70 dBm	-45.5 dBm	-97 dBm	-39 dBm	-56.5 dBm	$\mathbf{-69}$ **dBm**[5]
Normalized Sensitivity[6]	-97 dB	-100 dB	-123 dB	-66 dB	-137 dB	-58.6 dB	-76.1 dB	$\mathbf{-81.4}$ **dB**
Power	52 μW	51 μW	44 μW	116 nW	99 μW	104 nW	236 nW	**4.5 nW**

[1] 16-bit code sequence with 2 $\times$ oversampling. [2] The front-end matching network also has modest passive gain.
[3] Measured using CW jammer with signal input power for BER= 10^{-3} + 3 dB.
[4] Measured using CW jammer with signal input power for BER= 10^{-3} + 1 dB.
[5] Defined with less than 10^{-3} missed detection rate.
[6] Calculated by normalizing the sensitivity to data rate using either (2.16) or (2.17) depending on demodulation method.

Chapter 3

Near-Zero-Power Wake-Up Receivers Employing Active and Passive Pseudo-Balun Envelope Detectors

3.1 Introduction

To achieve sub-μW power, WuRX utilizing direct ED based architecture is the only feasible option where the RF signal is directly demodulated via the 2^{nd} order non-linearity of the ED, as discussed in Chapter 2 and depicted in Fig. 3.1(a). An OOK-modulated waveform is first amplified and filtered by a high-Q passive transformer/filter and then rectified by the ED. The ED output is $2\times$ oversampled, digitized, and compared with a voltage reference by a 2-stage regenerative comparator followed by a digital correlator, where the clock is provided by a relaxation oscillator. Once the correlation value between the oversampled code and a programmable code exceeds a programmable threshold, a wake-up signal is generated. In this architecture, conventional EDs with single-ended output are used and need either a reference ladder [8] or a replica ED [29] to serve as the comparator reference voltage, which requires power overhead and/or PVT tuning. Using an RC low-pass filter at the ED output as a dynamic reference is another solution [43], but at the expense of degraded siganl-to-noise-ratio (SNR) due to the burst nature of the wake-up signal. To solve this issue, an active pseudo-balun ED with differential outputs is proposed to flip the comparator state directly and eliminate the voltage reference block, as shown in Fig. 3.1(b) [10]. Moreover, another passive

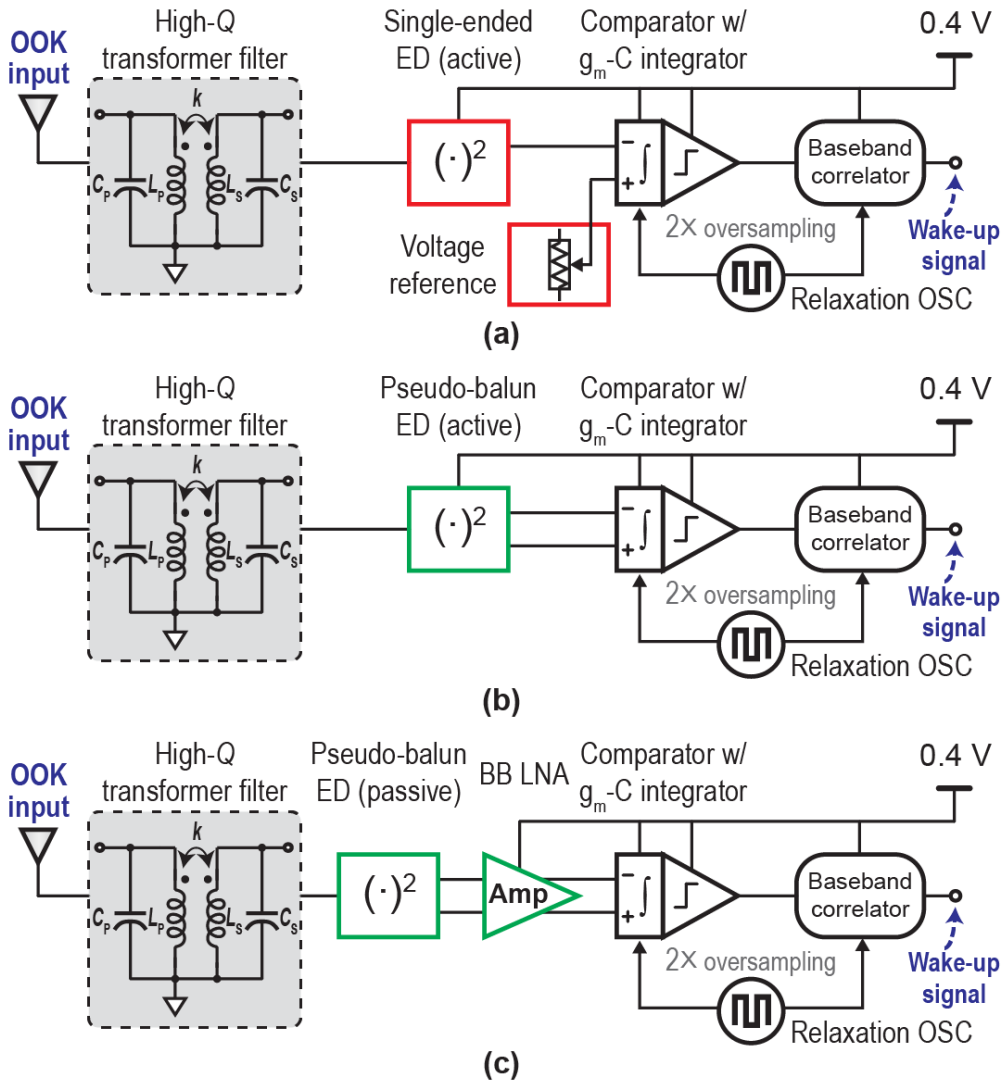


Figure 3.1: WuRX architecture employing: (a) an active ED with single-ended output; (b) an active pseudo-balun ED; (b) a passive pseudo-balun ED with low noise baseband amplifier.

pseudo-balun ED is also proposed, which, when combined with a low noise baseband amplifier, could further improve WuRX sensitivity at minimum extra power expense, as depicted in Fig. 3.1(c) [12].

In addition to architectural improvement, another design target is to operate at a higher carrier frequency, i.e., 400 MHz instead of 100 MHz. As shown in Fig. 3.1, the passive voltage gain A_{V} of the high Q transformer is limited by the effective parallel resistance of secondary coil L_{S} ($R_{\mathrm{S,p}}$) and the ED input resistance (R_{in}). Since

$R_{\mathrm{S,p}} \simeq \omega L_{\mathrm{S}} Q$, larger inductors can achieve larger $R_{\mathrm{S,p}}$; however, to maintain high A_{V} via resonance at 400 MHz with a large inductor, a small ED input capacitance C_{in} is required. Prior work discussed in Chapter 2, which targets LPWAN applications, has achieved excellent sensitivity at nW power levels but was limited to 113.5 MHz, largely because of the low input impedance of the ED [8]. As will be shown shortly, the proposed EDs in this chapter provide higher input resistance, lower input capacitance and higher ED scaling factor k_{ED}. These enhancements not only enable WuRX operation at 400 MHz without significantly compromising power consumption, but also improve sensitivity even when operating at the same FM band as [8]. Moreover, compared to conventional active/passive EDs with single-ended output, both the proposed active and passive pseudo-balun structures provide inherent 1.5 dB sensitivity improvement, which can be used to compensate the A_{V} loss from moving to higher frequency.

The proposed active/passive pseudo-balun EDs were originally presented in [10]/ [12] under 400/100 MHz band, respectively; this chapter provides additional circuit design details and comparison between these two EDs under 400 MHz band. Section 3.2 presents the active design, while the passive design is presented in Section 3.3. Measurement results are presented in Section 3.4, and finally, Section 3.5 concludes this chapter.

3.2 Active Pseudo-Balun Envelope Detector

In prior work, an active ED with dynamic threshold voltage MOSFET (DTMOS) common source (CS) configuration is utilized to boost the 2^{nd} order transconductance g_{m2}, as shown in Fig. 3.2(a) [8]. Since for active ED the transistors size needs to be large enough to minimize the effect of $1/f$ noise at baseband given the low data rate of the WuRX (300 bps), this configuration introduces significant C_{gd} and C_{bd} at the ED input, which is not suitable to enable high transformer gain at 400 MHz. On the other hand, compared to a CS ED, the common gate (CG) ED only has the source connected to the RF input whereas both the gate and bulk nodes are connected to a DC

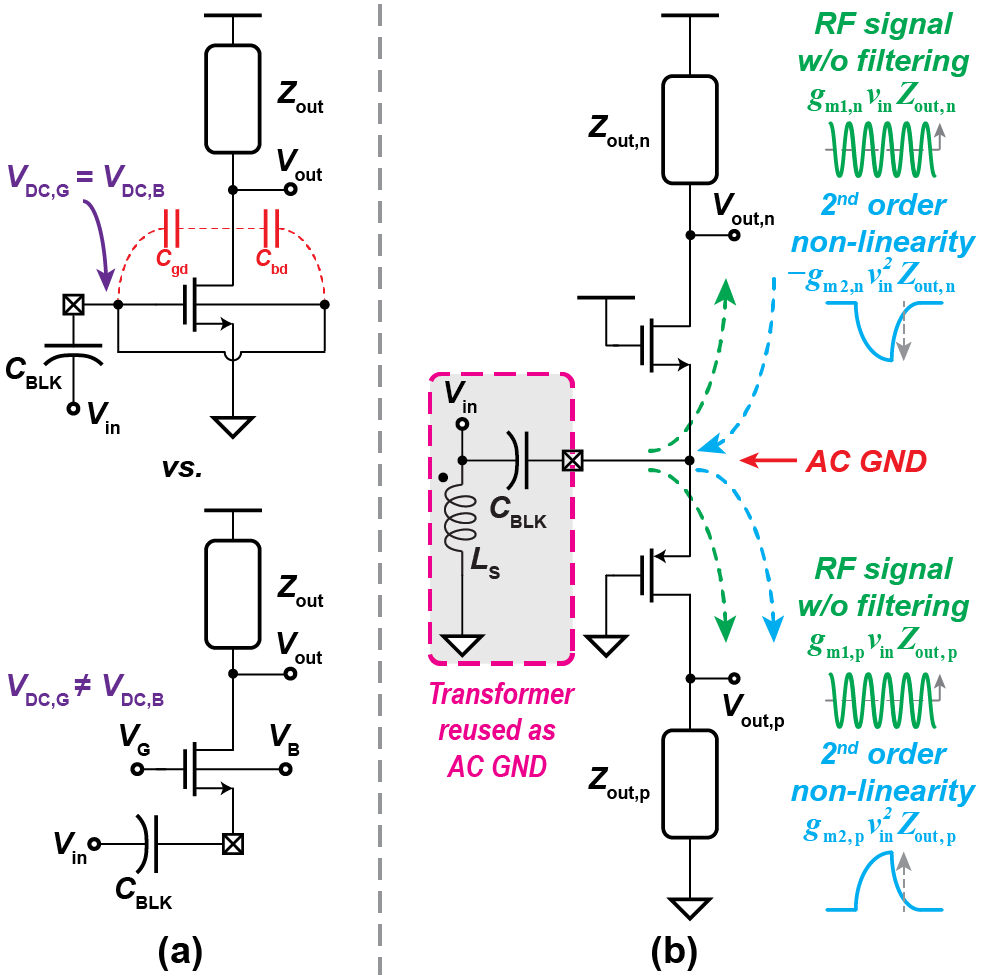


Figure 3.2: (a) Comparison of DTMOS CS and CG EDs; (b) active pseudo-balun current-reuse CG ED operation.

bias voltage, which therefore eliminates the effects of $C_{\rm gd}$ and $C_{\rm bd}$ on the input (Fig. 3.2a). Based on simulation, this configuration reduces input capacitance by 47.5% while still maintaining the 16% $g_{\rm m2}$ improvement of a DTMOS CS design [8]. Moreover, at nA current levels ($\sim$5 nA in this design, which results in $1/g_{\rm m1}$ $\approx$7 MΩ, where $g_{\rm m1}$ is the 1^{st} order transconductance of the transistor), the input resistance of a CG design is comparable with its CS counterpart, and is larger than a CS design with DTMOS configuration because of the elimination of the bulk network connection to the input. In addition, the DC bias voltages for the gate and bulk nodes can be set at different potentials for threshold voltage adjustment and freedom of transistor sizing, whereas for

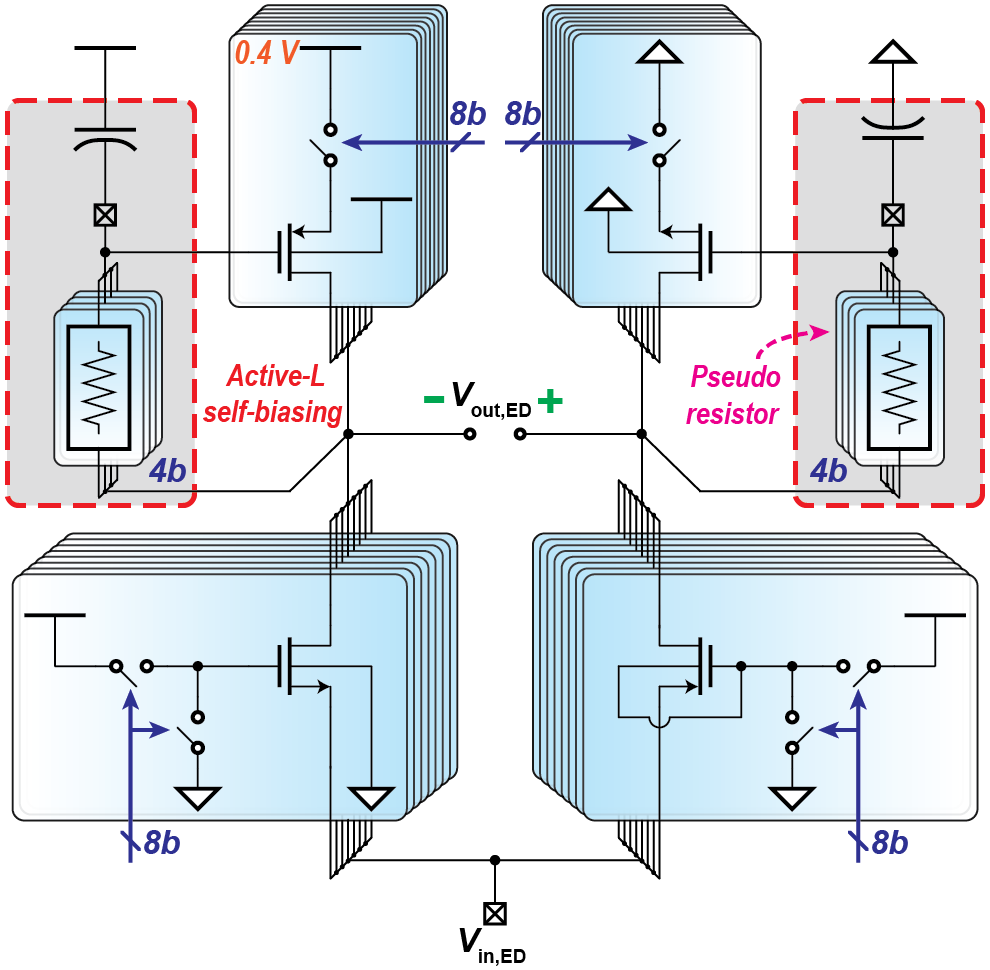


Figure 3.3: Schematic of the proposed active pseudo-balun current-reuse CG DTMOS ED.

a CS architecture an additional off-chip capacitor and bias resistors are then required, leading to extra input capacitance and a noise penalty.

Fig. 3.2(b) depicts the proposed active pseudo-balun ED configuration. Two n- and p-type CG amplifiers are stacked in a current re-use structure to provide single-ended to pseudo-differential conversion, eliminating the need for an explicit reference. The operation of the proposed ED could be verified by deriving the 1^{st} and 2^{nd} order transconductance of the NMOS and PMOS transistors in sub-V_{t} region as shown in the

following:

$$
\begin{aligned}
g_{\mathrm{m1,n}} &= \frac{\partial i_{\mathrm{DS,n}}}{\partial v_{\mathrm{SG,n}}} = \frac{\partial I_{\mathrm{off}} e^{\frac{v_{\mathrm{GS,n}}}{nV_{\mathrm{T}}}}}{\partial v_{\mathrm{SG,n}}} = -\frac{I_{\mathrm{DS,n}}}{nV_{\mathrm{T}}}, \\
g_{\mathrm{m1,p}} &= \frac{\partial i_{\mathrm{SD,p}}}{\partial v_{\mathrm{SG,p}}} = \frac{\partial I_{\mathrm{off}} e^{\frac{v_{\mathrm{SG,p}}}{nV_{\mathrm{T}}}}}{\partial v_{\mathrm{SG,p}}} = \frac{I_{\mathrm{SD,p}}}{nV_{\mathrm{T}}}, \\
g_{\mathrm{m2,n}} &= \frac{\partial^2 i_{\mathrm{DS,n}}}{\partial v_{\mathrm{SG,n}}^2} = \frac{\partial^2 I_{\mathrm{off}} e^{\frac{v_{\mathrm{GS,n}}}{nV_{\mathrm{T}}}}}{\partial v_{\mathrm{SG,n}}^2} = \frac{I_{\mathrm{DS,n}}}{2(nV_{\mathrm{T}})^2}, \\
g_{\mathrm{m2,p}} &= \frac{\partial^2 i_{\mathrm{SD,p}}}{\partial v_{\mathrm{SG,p}}^2} = \frac{\partial^2 I_{\mathrm{off}} e^{\frac{v_{\mathrm{SG,p}}}{nV_{\mathrm{T}}}}}{\partial v_{\mathrm{SG,p}}^2} = \frac{I_{\mathrm{SD,p}}}{2(nV_{\mathrm{T}})^2}.
\end{aligned}
\tag{3.1}
$$

Therefore, based on the polarity in (3.1), the proposed ED acts as a pseudo-balun only to 2^{nd} order non-linearities: linear RF currents flow symmetrically through the n- and p- CG amplifiers to partially cancel at the outputs (and are then further filtered), yet the baseband 2^{nd} order components flow pseudo-differentially with slightly different gains due to the asymmetric loading. Compared to a fully (pseudo)-differential CS design [45], the proposed ED's input is inherently an AC ground because of the transformer and thus no bias circuits (with their additional parasitic capacitance) are required at the input. A fully (pseudo)-differential CG design has also been presented in [49], which was used in a super-regenerative receiver after the voltage-controlled oscillator (VCO) to rectify a differential input signal and thus would require a center-tapped transformer in this design, which results in lower Q and thus lower A_{V} compared to a single-ended design. Moreover, in [49] CG is adopted to achieve higher conversion gain, while in this design CG is adopted to reduce the input node capacitance and maintain the same g_{m2} benefited from the DTMOS CS design as mentioned above.

The proposed current re-use pseudo-balun architecture improves k_{ED} by 66.6% compared to [8], and the WuRX sensitivity by $\sim$1.5 dB (i.e., 2$\times$ signal voltage with 2$\times$ noise power compared to single-ended ED) without a power penalty. The full ED schematic, which is depicted in Fig. 3.3, uses an active-inductor bias technique with MOS-bipolar pseudo-resistor feedback in the load circuits to increase output impedance and therefore k_{ED} [8]. To overcome process variation, all transistors have 8-bit of tun-

ability while the pseudo-resistor cells have 4-bit.

3.3 Passive Pseudo-Balun Envelope Detector

At 400 MHz, active EDs can offer $R_{\rm in}$ >10's of kΩ with wide bandwidths, but suffer from $1/f$ noise [10]. Passive EDs, on the other hand, were historically designed with low-$V_{\rm t}$ devices [50] or with standard high-$V_{\rm t}$ devices along with $V_{\rm t}$-cancellation techniques [51] to maximize power (not voltage) conversion efficiency, which results in a small $R_{\rm in}$. By using high-$V_{\rm t}$ devices at the cost of lower baseband bandwidth ($BW_{\rm BB}$), passive EDs can in fact achieve comparable $R_{\rm in}$ to active EDs, and, most importantly, do not have any $1/f$ noise since there are no DC currents. This permits smaller devices and thus lower $C_{\rm in}$. As such, passive EDs can have higher SNR and enable higher $A_{\rm V}$ compared to active EDs.

Fig. 3.4(a) and 3.4(b) depict conventional and the proposed passive ED unit cells and architectures. Cross-coupled self-mixers [52] rectify a differential input signal and thus require a center-tapped transformer, which results in lower Q and thus lower passive gain compared to a single-ended design. Moreover, biasing is implemented using an extra RC network at the RF node that reduces the ED input impedance. On the other hand, a traditional Dickson rectifier operating in sub-$V_{\rm t}$ [28, 53] can rectify a single-ended input signal, but does not have any tunability and only has a single-ended output, which requires a tunable reference circuit for the comparator. To overcome these issues, as shown in Fig. 3.4(b), a tunable passive pseudo-balun ED architecture is proposed, which is a $2N$-stage rectifier with the middle node connected to a common-mode voltage $V_{\rm CM}$ and the bulk nodes connected to a tunable voltage, $V_{\rm bulk}$, to adjust $V_{\rm t}$ and set the $BW_{\rm BB}$. As such, the baseband AC currents flow in opposite directions relative to ground to form a pseudo-differential output. Compared to the original single-branch N-stage Dickson rectifier, this structure achieves 2$\times$ conversion gain and a 1.5 dB sensitivity improvement under the same input signal level without sacrificing output bandwidth. Although the 2^{nd} branch of the N-stage ED could be connected in parallel with the

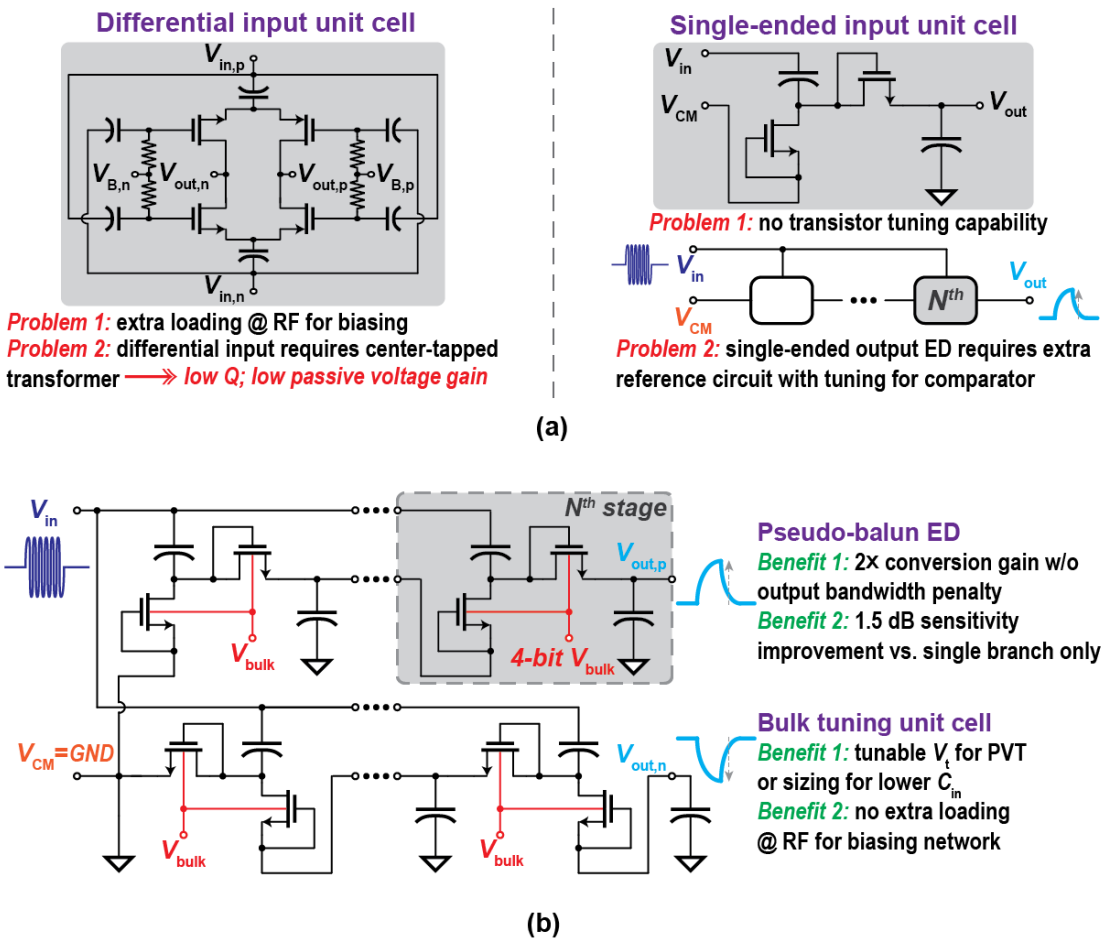


Figure 3.4: (a) Conventional passive ED unit cells and architectures; (b) proposed passive pseudo-balun ED with bulk tuning unit cell.

1^{st} branch without flipping the polarity, this results in the same 1.5 dB improvement in sensitivity, but only half of the conversion gain and is single-ended. $V_{\rm bulk}$ is provided by a diode-connected reference ladder with 4-bit tunability.

To drive a fixed capacitive load from the baseband amplifier, an ED with a large number of stages, N, requires larger transistor widths to maintain the same output bandwidth, and thus has a larger $C_{\rm in}$, which limits the achievable transformer gain. As the transistor width increases, the parasitic capacitor from the ED starts to add on to the fixed capacitive load at the output node, which thus requires $R_{\rm out}$ to decrease further. For the 400 MHz MICS band design, as shown in Fig. 3.5(a), larger transformer passive voltage gain, $A_{\rm V}$, is possible with small N, which has higher $R_{\rm in}$ and lower $C_{\rm in}$.

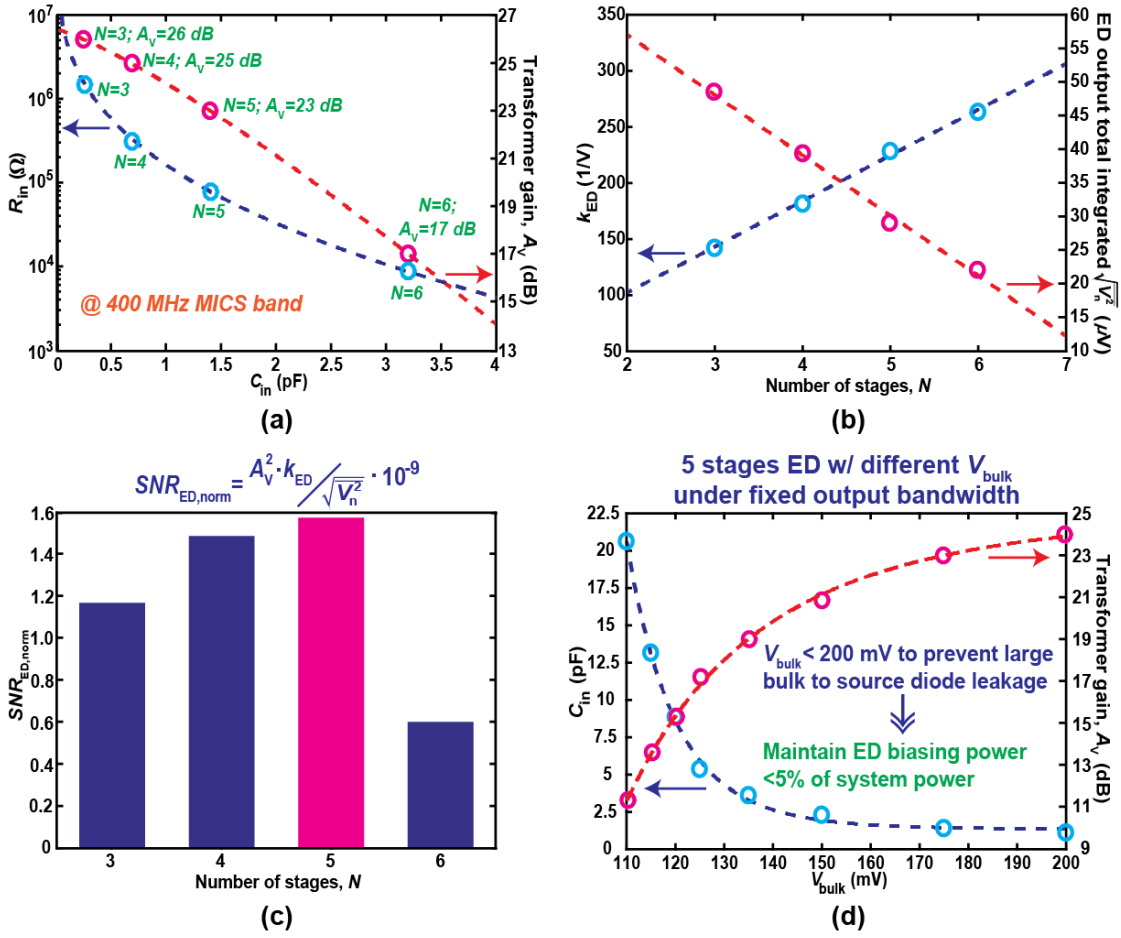


Figure 3.5: Proposed ED tradeoffs with different number of stages, N, under fixed BW_{BB} for 400 MHz operating frequency: (a) R_{in} and A_{V} vs. C_{in}; (b) k_{ED} and $\sqrt{\overline{v_{\mathrm{n}}^2}}$ vs. N; (c) passive ED $SNR_{\mathrm{ED,norm}}$; (d) N=5 stages ED tradeoffs for different V_{bulk}.

However, as shown in Fig. 3.5(b), since the conversion gain and thus ED scaling factor, k_{ED}, are proportional to N, an ED with large N is more suitable for post-ED stage noise suppression. Moreover, since the passive ED noise power density is $4k_{\mathrm{B}}TR_{\mathrm{out}}$, an ED with a larger N has less total integrated noise, $\sqrt{\overline{v_{\mathrm{n}}^2}}$. To find the optimum N, an objective function was developed to compare designs with different N under the same output bandwidth and operating frequency:

$$SNR_{\mathrm{ED,norm}} = \frac{A_{\mathrm{V}}^2 \cdot k_{\mathrm{ED}}}{\sqrt{\overline{v_{\mathrm{n}}^2}}} \cdot 10^{-9}, \tag{3.2}$$

which is essentially the achievable ED output SNR normalized to its input voltage. As shown in Fig. 3.5(c), an optimum value of N=5 was found for the ED operating at 400 MHz using (3.2). Fig. 3.5(d) shows simulation for the N=5 ED $C_{\rm in}$ and the corresponding $A_{\rm V}$ for different $V_{\rm bulk}$. By forward biasing the transistor bulk to source junction diode (<200 mV), $V_{\rm t}$ is reduced and therefore transistors with lower width could be implemented for a given $BW_{\rm BB}$. Thus, the proposed bulk tuning can not only be used to overcome process variation, but can also effectively reduce $C_{\rm in}$ via smaller devices, and therefore maximize the achievable $A_{\rm V}$. Based on simulation, the proposed passive ED achieves 2.3× lower $C_{\rm in}$ and 2.4 dB higher SNR than its active counterpart [10] under the same $BW_{\rm BB}$=33.3 Hz and input signal level while considering ED noise only. The lower $C_{\rm in}$ allows for a larger secondary coil, resulting in 23 dB of passive gain at MICS band, a 4.5 dB improvement over [10]. Moreover, by using a passive ED, most of the power budget can be devoted to the subsequent baseband amplifier to minimize the post-ED circuit noise, as shown in Fig. 3.1(c) [12].

The same design procedure along with (3.2) can be used to optimize the proposed passive pseudo-balun ED for different operating frequency. Fig. 3.6(a) depicts the achievable transformer passive voltage gain $A_{\rm V}$ along with different ED stage num-

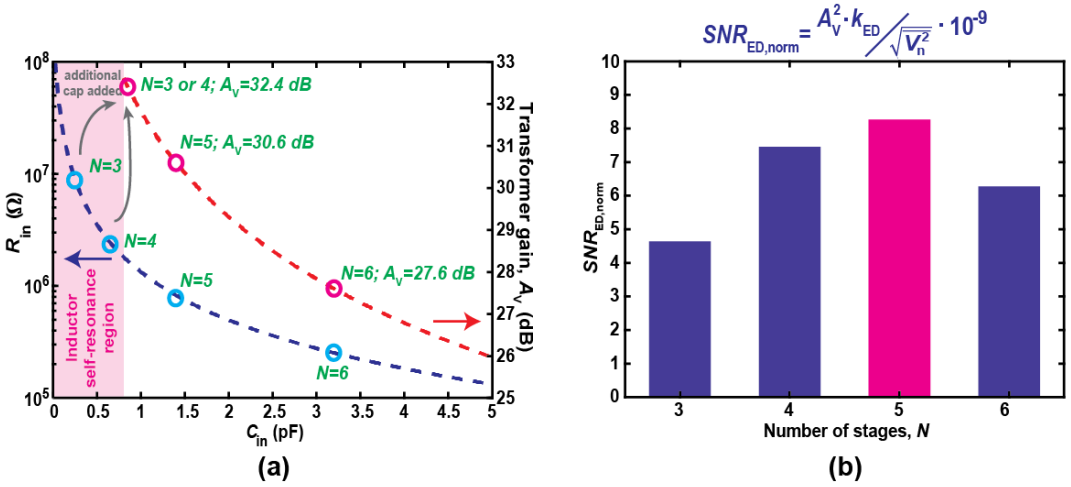


Figure 3.6: Proposed ED tradeoffs with different number of stages, N, under fixed $BW_{\rm BB}$ for 100 MHz operating frequency: (a) $R_{\rm in}$ and $A_{\rm V}$ vs. $C_{\rm in}$; (b) passive ED $SNR_{\rm ED,norm}$.

ber N when operating at 100 MHz FM band. Combined with Fig. 3.5(b), Fig. 3.6(b) shows that an optimum value of N=5 was found for the ED operating at 100 MHz using (3.2), yet with different $SNR_{\mathrm{ED,norm}}$ value compared to Fig. 3.5(c).

3.4 Measurement Results

3.4.1 400 MHz Designs employing Pseudo-Balun Envelope Detectors

The transformer/filter performance is characterized in Fig. 3.7. S_{11} measurements indicate excellent matching across 402–405 MHz for both designs, while the passive voltage gain A_{V}=18.5 dB was measured for the design employing the active pseudo-balun ED and A_{V}=23 dB for the design employing the passive pseudo-balun ED, respectively.

Fig. 3.8(a) and 3.8(b) show the measured power breakdown and transient wave-

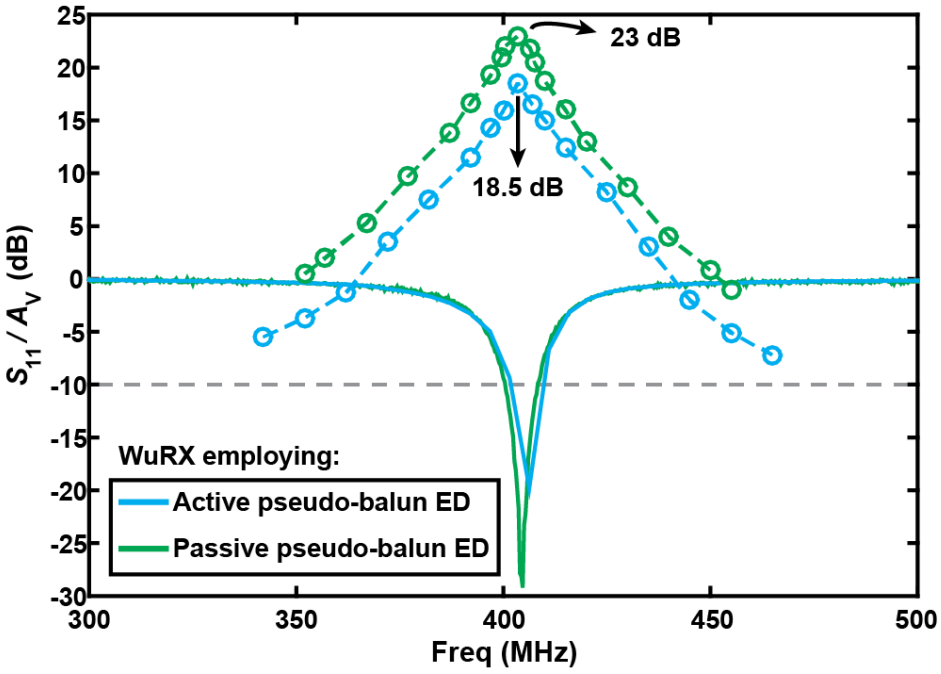


Figure 3.7: Measured transformer S_{11} and A_{V} of the 400 MHz WuRXs.

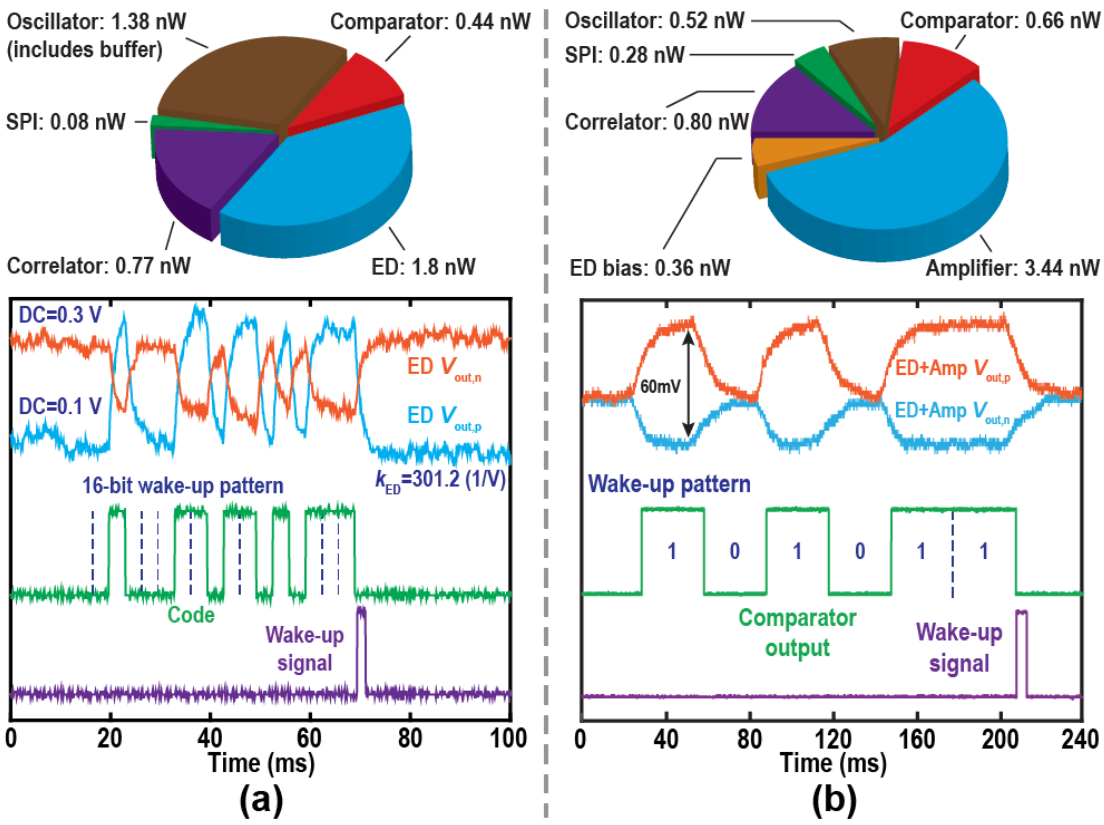


Figure 3.8: System power breakdown and transient waveforms for WuRX employing: (a) an active pseudo-balun ED; (b) a passive pseudo-balun ED.

forms of the two WuRXs. For the active ED version, the total power consumption is 4.5 nW when the ED is set to 1.8 nW and the oscillator is set to provide a 600 Hz clock, while the transient waveforms were measured using a 300 bps 16-bit wake-up pattern under 2× oversampling ratio, which clearly show the pseudo differential outputs of the proposed active ED with k_{ED}=301.2 (1/V). On the other hand, for the passive ED version, the total power consumption is 6.1 nW when the oscillator is set to provide a 200 Hz clock, while the transient waveforms were measured using a 33.3 bps 6-bit wake-up pattern under 6× oversampling ratio, which also verify the pseudo-balun operation of the proposed passive ED with k_{ED}=208.7 (1/V).

Fig. 3.9 shows the waterfall curves for the wake-up signal missed detection rate (MDR) of the two WuRXs. The MDR curves are measured with a false alarm rate of ≈1/hr, and the sensitivity is defined when MDR=10^{-3} is achieved. Measurement

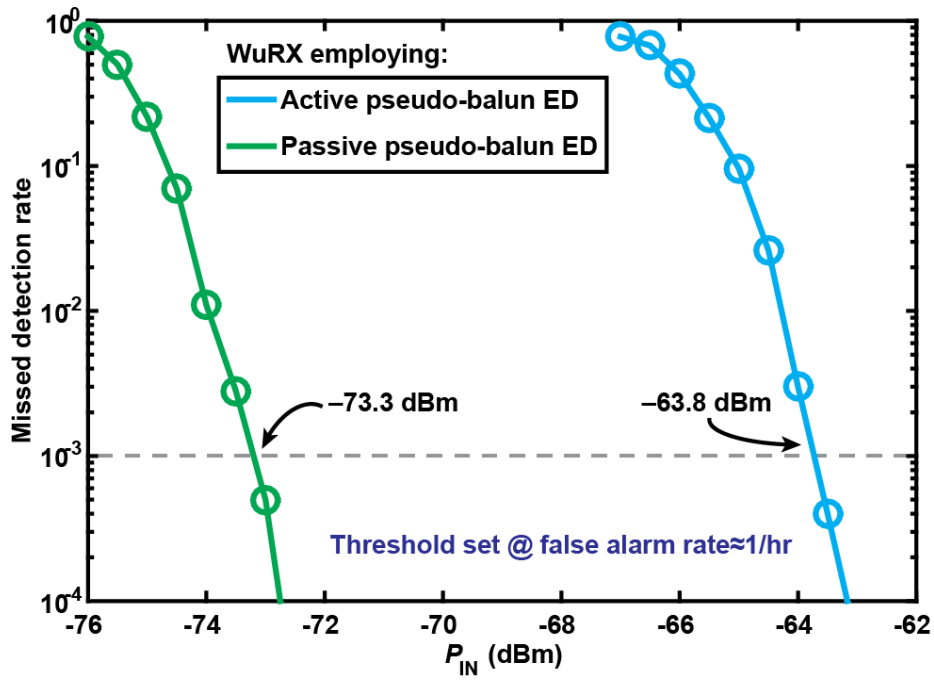


Figure 3.9: MDR waterfall curves of the 400 MHz WuRXs.

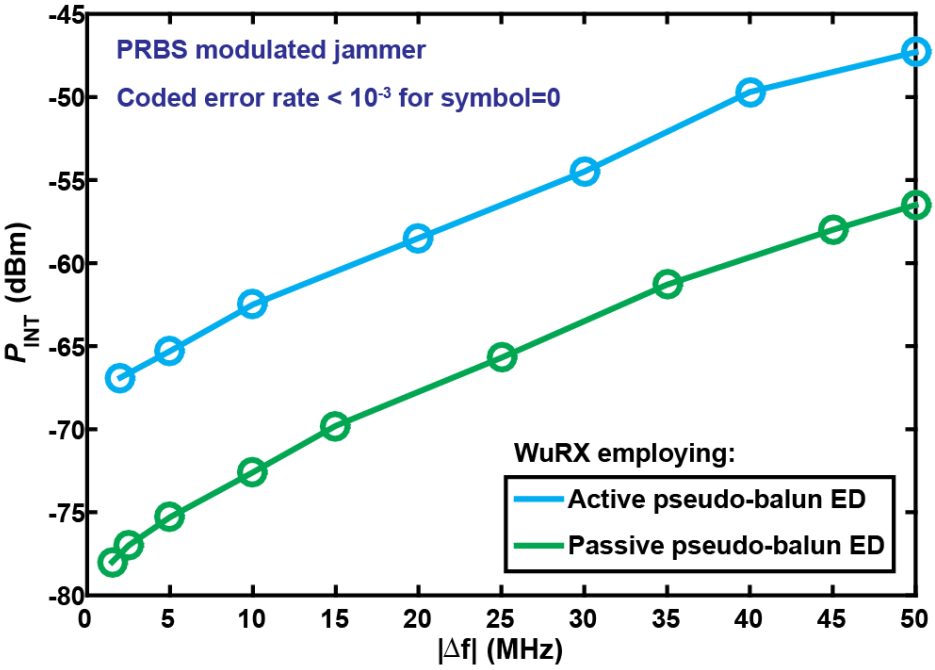


Figure 3.10: Interferer power vs. frequency offset $|\Delta f|$ to carrier frequency for a worst-case PRBS-modulated jammer of the 400 MHz WuRXs.

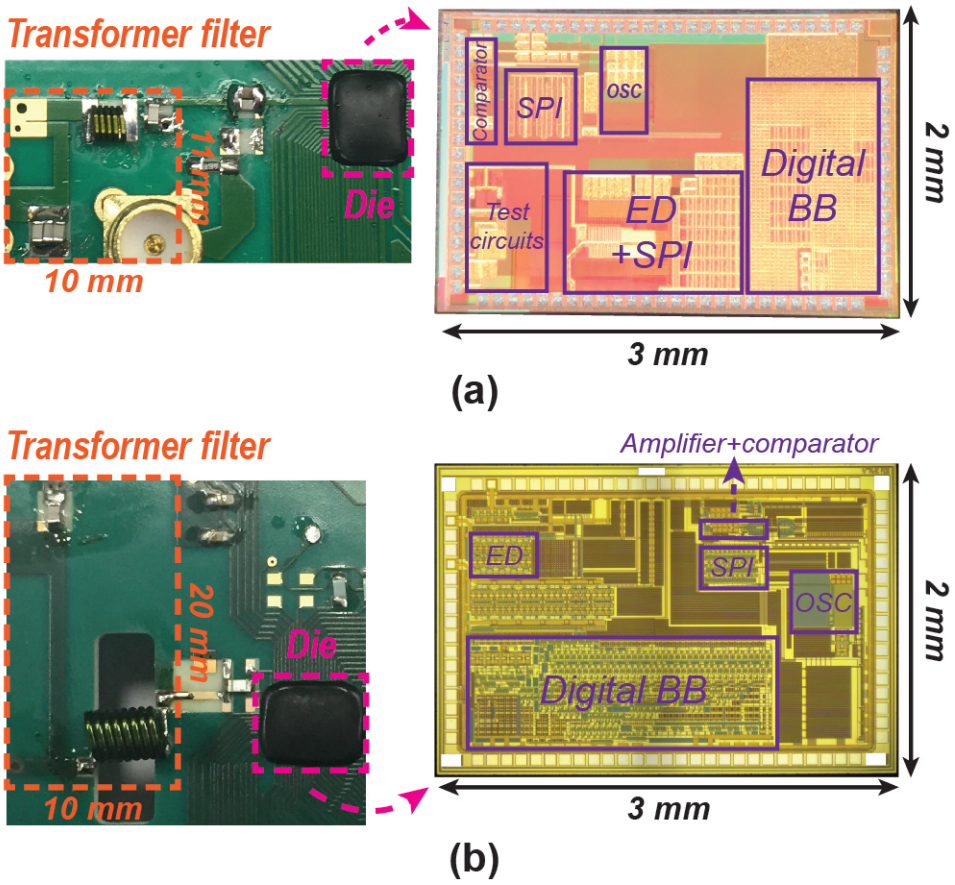


Figure 3.11: Board and die micrographs for 400 MHz designs employing: (a) an active pseudo-balun ED; (b) a passive pseudo-balun ED.

shows that for the active ED version P_{SEN}=−63.8 dBm, while for the passive ED version P_{SEN}=−73.3 dBm. Based on the transformer performance and sensitivity measurement, the sensitivity improvement enabled by the EDs could be verified by comparing to [8], which has P_{SEN}=−69 dBm with A_{V}=25 dB at FM band. For the active ED version comparing to [8], although 6.5 dB passive gain is compromised by moving to MICS band, the proposed pseudo-balun structure restore 1.3 dB, which matches with the analysis. For the passive ED version comparing to the active ED version, the 9.5 dB sensitivity improvement can be segmented into the following: A_{V} improves 4.5 dB enabled by lower ED C_{in}, and another 5 dB is achieved through passive ED plus baseband amplifier SNR improvement over active ED as well as lower BW_{BB}.

Since false alarms will cause unwanted power dissipation in sensor nodes, a

pseudo-random binary sequence (PRBS) modulated jammer at frequency offset Δf to the signal carrier frequency were used to test WuRX performance under interference. Fig. 3.10 depicts the interferer tolerance to maintain a coded error rate less than 10^{-3} for symbol 0 of the two designs (i.e., less than 1 time wake-up per 1000 times incorrect wake-up pattern received). Moreover, a continuous wave (CW) jammer only causes a DC tone at the ED output and therefore is unlikely to cause a false alarm due to the correlator, of which the code-length could be extended to improve interferer resilience further. The die micrographs along with the whole system photographs of the two designs are shown in Fig. 3.11.

3.4.2 100 MHz Design employing Passive Pseudo-Balun Envelope Detector

The same WuRX employing the passive pseudo-balun ED is adopted for the 100 MHz design, and Fig. 3.8(b) shows the measured power breakdown and transient

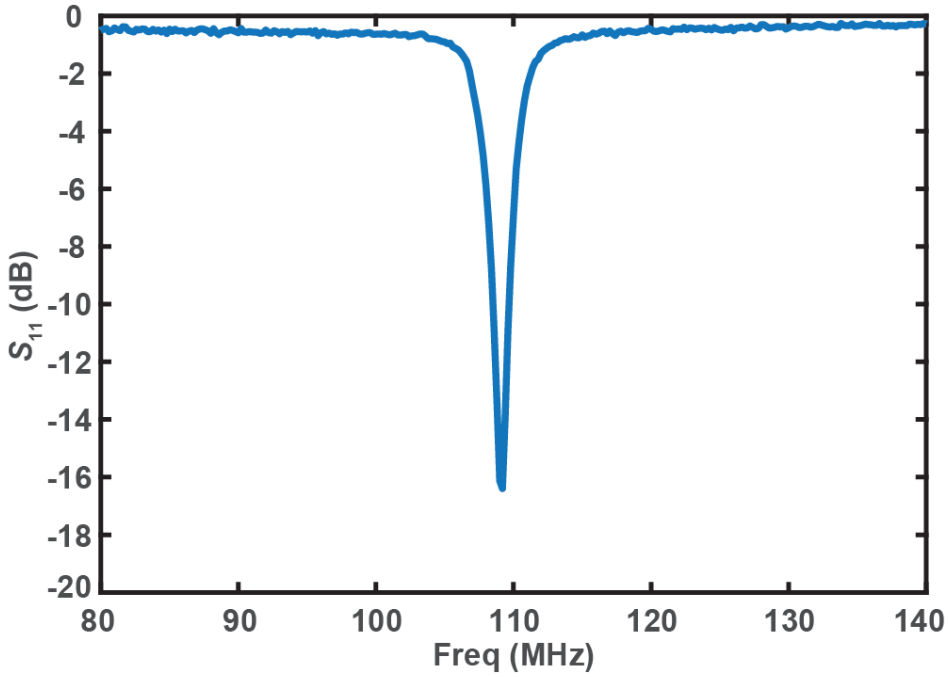


Figure 3.12: Measured transformer S_{11} of the 100 MHz WuRX.

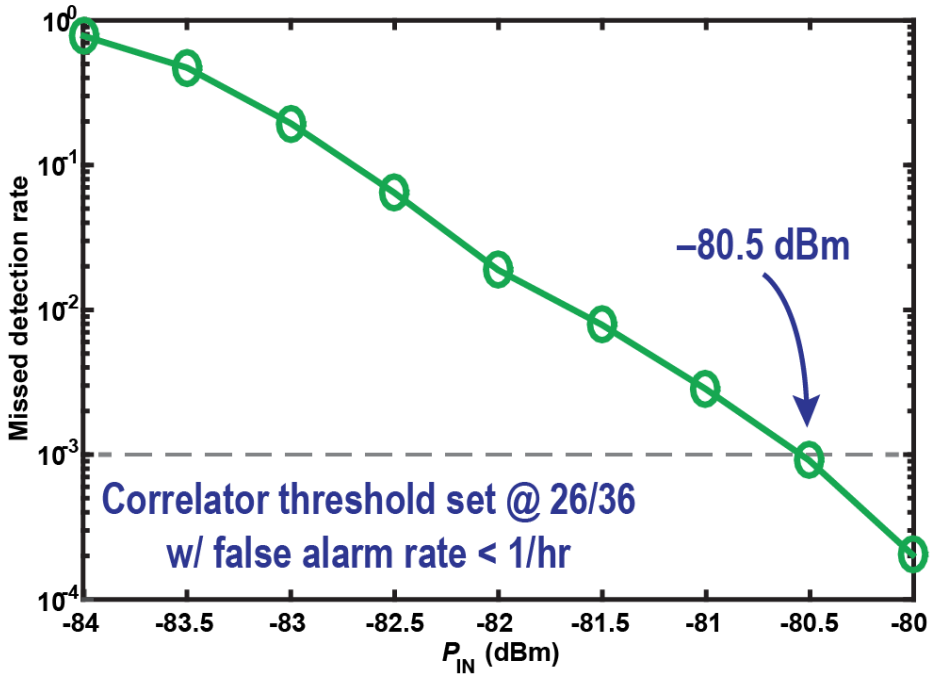


Figure 3.13: MDR waterfall curves of the 100 MHz WuRX.

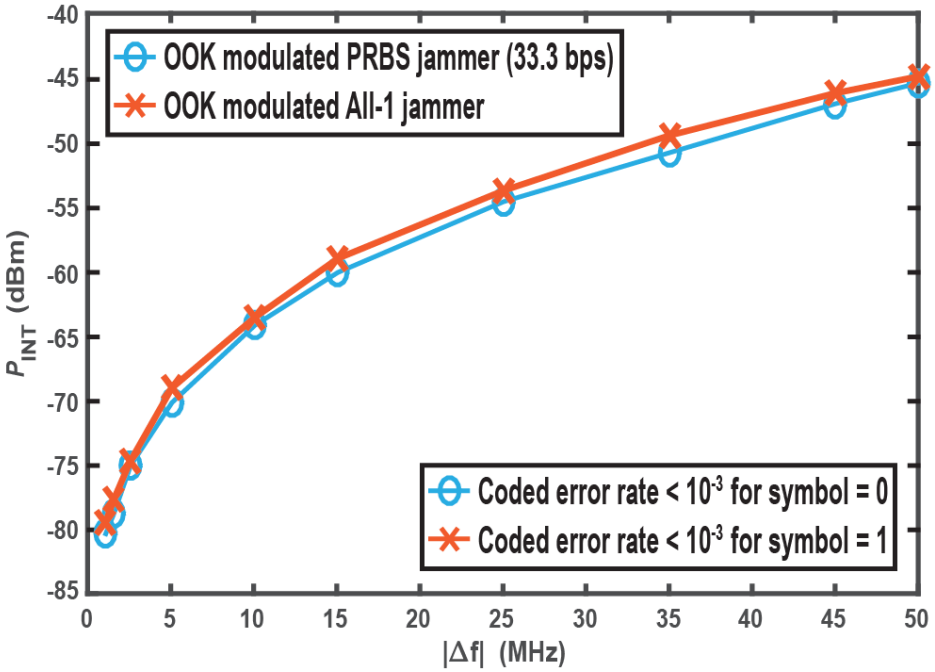


Figure 3.14: Interferer power vs. frequency offset $|\Delta f|$ to carrier frequency for a worst-case PRBS-modulated jammer of the 100 MHz WuRX.

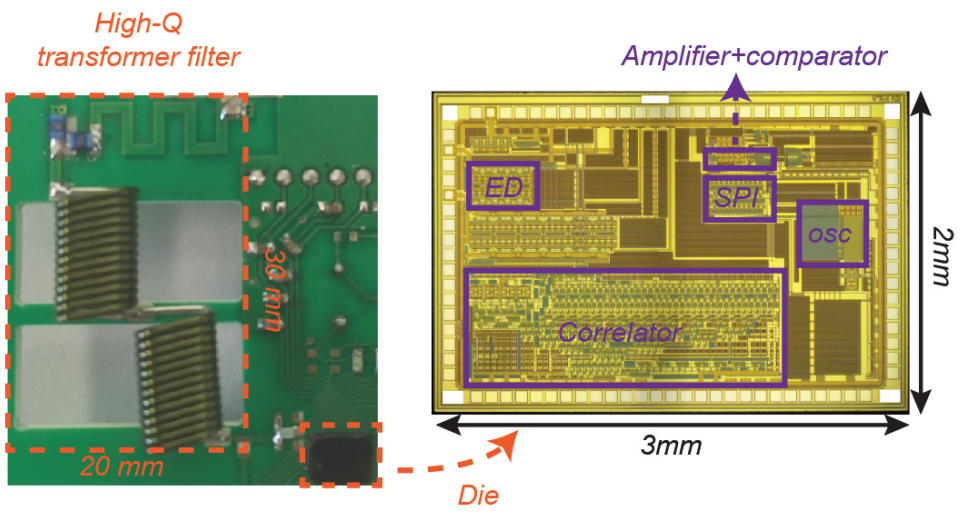


Figure 3.15: Board and die micrographs for the 100 MHz design.

waveforms. The measured transformer A_{V} was 30.6 dB at 109 MHz, and the amplifier gain was 28 dB. Fig. 3.12 shows the measured S_{11}, indicating good matching at 109 MHz. Fig. 3.13 shows missed detection rate (MDR) curves after correlation, where a 0.1% MDR was achieved with random (i.e., unsynchronized) transmission at -80.5 dBm while maintaining a false alarm rate $< 1/\mathrm{hr}$. Part-to-part measurements (n=5) showed that the sensitivity and power were all within 0.5 dB and 0.2 nW, respectively. Fig. 3.14 depicts the interferer tolerance where a 33.3 bps PRBS OOK-modulated jammer was used to characterize the coded error rate for symbol-0 (i.e., false alarms), while an all-1 jammer was used for symbol-1 (i.e., missed detections). The interferer power is defined as the power needed to achieve 0.1% MDR when the signal is 1 dB higher than the sensitivity. A die and PCB photo are shown in Fig. 3.15.

Table 3.1 summarizes the measurement results of the proposed WuRX designs and compares the results to the state-of-the-art sub-300 nW WuRXs. Since longer-bit correlator can provide larger coding gain, while lower data rate (i.e., BW_{BB}) can reduce total integrated noise, both of which improve sensitivity and determine the wake-up latency (L_{WuRX}), to compare state-of-the-art designs, instead of normalizing sensitivity to BW_{BB} [8], here sensitivity is normalized using L_{WuRX} and the proposed WuRX FoM

can be derived as:

$$\begin{aligned} FoM_{\mathrm{WuRX}}(dB) &= -P_{\mathrm{SEN,norm}} - 10\log\frac{P_{\mathrm{dc}}}{1mW} \\ &= -\left(P_{\mathrm{SEN}} + 5\log L_{\mathrm{WuRX}}\right) - 10\log\frac{P_{\mathrm{dc}}}{1mW}, \end{aligned} \tag{3.3}$$

where $P_{\mathrm{SEN,norm}}$ is the normalized sensitivity, P_{dc} is the power consumption, P_{SEN} is the sensitivity in dBm, and $5\log L_{\mathrm{WuRX}}$ is used for non-linear squaring demodulator [8]. While the 400 MHz band design employing the passive pseudo-balun ED achieves FoM_{WuRX}=129.1 dB, the 400 MHz design employing the active pseudo-balun ED achieves a FoM_{WuRX}=123.7 dB with $>3\times$ lower latency. Moreover, the 100 MHz design employing the passive pseudo-balun ED achieves higher FoM_{WuRX}=136.3 dB because of the larger achievable transformer passive gain nature for lower operating frequency.

3.5 Conclusions

In this chapter, two 400 MHz WuRXs that achieve $-63.8/-73.3$ dBm sensitivity while consume only 4.5/6.1 nW in a 0.18 μm CMOS process are presented. Both an active and a passive ED designs with pseudo-balun characteristics were proposed to enable WuRX operation at 400 MHz while improve sensitivity compared to their single-ended counterparts. Moreover, the proposed pseudo-balun structures can eliminate extra voltage reference requirement for the subsequent comparator. Measurement results showed that the WuRX employing the active ED can achieve a communication range of $\sim$100 meters with a wake-up latency of 53.3 ms, while the design employing the passive ED can extend the range further to $\sim$300 meters with a wake-up latency of 180 ms. It should be noted for a WuRX, as long as a reasonable wake-up latency is achieved (e.g., $<$1 second for many low-average throughput applications), the most important metrics are the power consumption and sensitivity. Metrics such as the energy/bit and bandwidth are not as important since a WuRX has, by design, low throughput.

This chapter is based on and mostly a reprint of the following publications: P.-H. P. Wang, H. Jiang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, P. P. Mercier, and D. A. Hall, "A 400 MHz 4.5 nW 63.8 dBm Sensitivity Wake-Up Receiver Employing an Active Pseudo-Balun Envelope Detector," *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, Leuven, Belgium, 2017, pp. 35-38, and P.-H. P. Wang, H. Jiang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, P. P. Mercier, and D. A. Hall, "A 6.1 nW Wake-Up Receiver Achieving -80.5-dBm Sensitivity via a Passive Pseudo-Balun Envelope Detector," *IEEE Solid-State Circuits Letters*, vol. 1, no. 5, pp. 134-137, May 2018. The dissertation author is the primary author of these materials, and co-authors have approved the use of the material for this dissertation.

Table 3.1: Performance Comparison of State-of-the-Art Sub-300 Nanowatt WuRXs

	[54] ISSCC'18	[8] JSSC'18	[28] CICC'13	[52] CICC'17	[53] ISSCC'18	**400 MHz Designs**		**100 MHz Design**
Technology	65 nm	180 nm	130 nm	130 nm	130 nm	**180 nm**		**180 nm**
Supply Voltage	0.5 V	0.4 V	1.2 / 0.5 V	0.5 V	1.0 / 0.6 V	**0.4 V**		**0.4 V**
Digital Correlator	3∼10-bit	32-bit†	31-bit	11-bit*	8-bit	**32-bit**†	**36-bit***	**36-bit***
External Components	CMUT$^{\circ}$	Transformer filter	XTAL+LC MN	LC MN	LC MN	**Transformer filter**		**Transformer filter**
Clock	Relaxation osc.	Relaxation osc.	XTAL osc.	No	Ring osc.	**Relaxation osc.**		**Relaxation osc.**
Passive RF Gain	N.R.$^{\diamond}$	25 dB	5 dB	27 dB$^{\triangleleft}$	N.R.$^{\diamond\dagger}$	**18.5 dB**	**23 dB**	**30.6 dB**
Demodulator Type	Active CS-CG single-ended ED	Active CS single-ended ED	Passive Dickson single-ended ED	Passive self-mixer	Passive Dickson single-ended ED	**Active CG pseudo-balun ED**	**Passive Dickson pseudo-balun ED**	**Passive Dickson pseudo-balun ED**
Carrier Frequency	57 kHz	113.5 MHz	403 MHz	550 MHz	433 MHz	**405 MHz**		**109 MHz**
Wake-up Latency	8.9∼29.8 ms	53.3 ms	2.48 ms	27.5 μs	$>$80 ms$^{\triangleright}$	**53.3 ms**	**180 ms**	**180 ms**
Sensitivity	$-$60.1 dBm$^{\wr}$	$-$69 dBm	$-$45.5 dBm	$-$56.4 dBm	$-$71 dBm	**$-$63.8 dBm**	**$-$73.3 dBm**	**$-$80.5 dBm**
Normalized Sensitivity‡	$-$68.5 dB$^{\wr}$	$-$75.4 dB	$-$58.5 dB	$-$79.2 dB	$-$76.5 dB	**$-$70.2 dB**	**$-$77 dB**	**$-$84.2 dB**
Power Consumption	8 nW	4.5 nW	116 nW	222 nW	7.6 nW	**4.5 nW**	**6.1 nW**	**6.1 nW**
$\boldsymbol{FoM_{\mathrm{WuRX}}}$	119.5 dB	128.9 dB	97.9 dB	115.7 dB	127.7 dB	**123.7 dB**	**129.1 dB**	**136.3 dB**

†16-bit code sequence with 2$\times$ oversampling. *Off-chip and not in the power budget.
*6-bit code sequence with 6$\times$ oversampling. $^{\circ}$Capacitive micromachined ultrasonic transducer.
$^{\diamond}$Not reported. $^{\triangleleft}$Assuming off-chip inductors with a Q of infinity. †27 dB at 151.8 MHz; not reported at 433 MHz.
$^{\triangleright}$Half clock cycle value not provided. $^{\wr}$7-bit wake-up pattern is used for measurement.
$^{\ddagger}P_{\mathrm{SEN,norm}} = P_{\mathrm{SEN}} + 5\log L_{\mathrm{WuRX}}$, where 5 log is used for non-linear squaring demodulator [8].

Chapter 4

An Interference-Resilient BLE-Compatible Wake-Up Receiver Employing Single-Die Multi-Channel FBAR-Based Filtering and a 4-Dimensional Wake-Up Signature

4.1 Introduction

Wireless communication circuits often dominate the power consumption of small battery-powered devices used in applications like the Internet of Things (IoT), wearables, smart homes, and beyond. A large fraction of this power comes from node-to-hub or node-to-node networking requirements, especially when such devices communicate with low average throughput [6, 7]. There are three main ways to establish networking in such applications [7]:

1. *Synchronous:* The most conventional approach involves periodic transmissions between radios to maintain network synchronization. However, turning on radios for synchronization, even when there is no data to transmit (as is often the case in low-average throughput scenarios) is wasteful.

2. *Pseudo-synchronous:* Instead of adhering to a schedule set by a precision local reference, it is possible to wake-up the radio only when needed (i.e., asyn-

chronously), and have the transmitter repeat synchronization packets until both nodes synchronize. This trades off power consumption for increased network latency.

3. *Asynchronous:* Rather than use the main radio to periodically look for synchronization packets, it is possible to design a separate wake-up receiver (WuRX) that continuously monitors the RF spectrum for a pre-specified wake-up signature. Once received, the WuRX will wake-up the main radio to perform on-demand high instantaneous throughput communication.

Properly designed WuRXs can help to reduce the overall power consumption of wireless communications, particularly in low-average throughput scenarios where periodic wake-on events otherwise consume significant energy. To be pragmatic, most WuRXs must abide by the following requirements:

1. *Low power consumption*: Since the WuRX is always on while the main radio is in deep sleep mode, the WuRX can easily become the power bottleneck of the entire system.

2. *Good sensitivity*: The WuRX should ideally offer the same (or better) sensitivity as the main radio. Otherwise, communication distance and therefore network deployment strategies would be limited by the radio with the worst sensitivity.

3. *Interference resiliency*: WuRXs need to wake-up reliably, ideally with little-to-no false alarms. High interference resiliency is therefore required to maintain reliability, especially in congested bands.

4. *Standards compatibility*: The main idea of WuRXs is to offer an attractive low-power means to establish an initial handshake between radios. If the WuRX is not compatible with any standard, then additional custom hardware is required, which adds cost and complicates deployment strategies. Ideally, no changes to existing wireless infrastructure would be required with a fully standards-compatible WuRX.

The easiest way to achieve low-power operation is to utilize low-complexity modulation schemes such as on-off-keying (OOK) or frequency-shift-keying (FSK) operating with low data rates, as these modulation schemes eliminate the need for precision frequency synthesizers, while low data rates enable a low noise bandwidth for high sensitivity even without active RF gain [8, 10, 12, 13, 24, 25, 27–29, 42, 53, 55]. However, most popular radio standards do not natively support such modulation schemes and/or data rates. In addition, most prior work in this area relied on simple energy-detection architectures that, while enabling achievement of very low power, have difficult operating robustly in the presence of interferers.

To solve the first issue, prior work has reported the idea of back-channel (BC) communication, where signals are generated by a standard-compliant transmitter, yet encode information in an auxiliary low-complexity and low data rate modality [9]. Solving the second issue requires judicious use of passive high-Q RF filtering, active IF/baseband filtering, and/or frequency-hopping (the latter two of which unfortunately cost power due to the need for an local oscillator (LO)).

This chapter describes a WuRX designed for operation with Bluetooth Low Energy (BLE). Most prior BLE-compatible WuRXs encoded a wake-up signature in the presence (or sequence) of transmitted BLE advertisement packets, and enabled designs that primarily focus to achieve either low power [9], low latency [15], high sensitivity [56], or interference-robust frequency diversity [57]. However, achievement of all of these parameters simultaneously had not yet been demonstrated in prior art.

The developed BLE-compatible WuRX achieves -85 dBm sensitivity with 220 μW active power consumption while supporting multi-channel frequency diversity through a combination of high-Q filtering by a bank of FBAR resonators and a frequency-hopped mixer-first RF front-end that responds to a 4-dimensional (4-D) wake-up signature. The proposed 4-D wake-up signature is presented in Section 4.2, while Section 4.3 describes the overall WuRX architecture. Section 4.4 presents circuit implementation details, followed by measurement results in Section 4.5. Finally, Section 4.6 concludes this chapter.

4.2 BLE-Compatible Wake-Up Signature

4.2.1 Overview of BLE-Compatible Wake-up Signatures

The 2.4 GHz ISM band is congested by multiple wireless standards, as shown in Fig. 4.1(a). The BLE standard operates across 40 channels within this band, and modulates signals with Gaussian frequency-shift keying (GFSK) at between 1 Mbps (normal mode) and 125 kbps (low data rate mode in BLE 5.0). To facilitate network synchronization and device pairing, three of the 40 channels are reserved for advertising events: channels 37, 38, and 39, located at 2402, 2426, and 2480 MHz, respectively. A single advertising event consists of the same packet transmitted at all 3 advertising channels consecutively, and takes less than 20 ms at low duty cycle mode or less than 3.75 ms at high duty cycle mode, respectively (Fig. 4.1b). The packet length of a single advertising packet for BLE 4 is around 128∼376 μs, and is extended to 784∼16,320 μs for BLE 5. This paper focuses on the design for the more widely adopted BLE 4 standard for now.

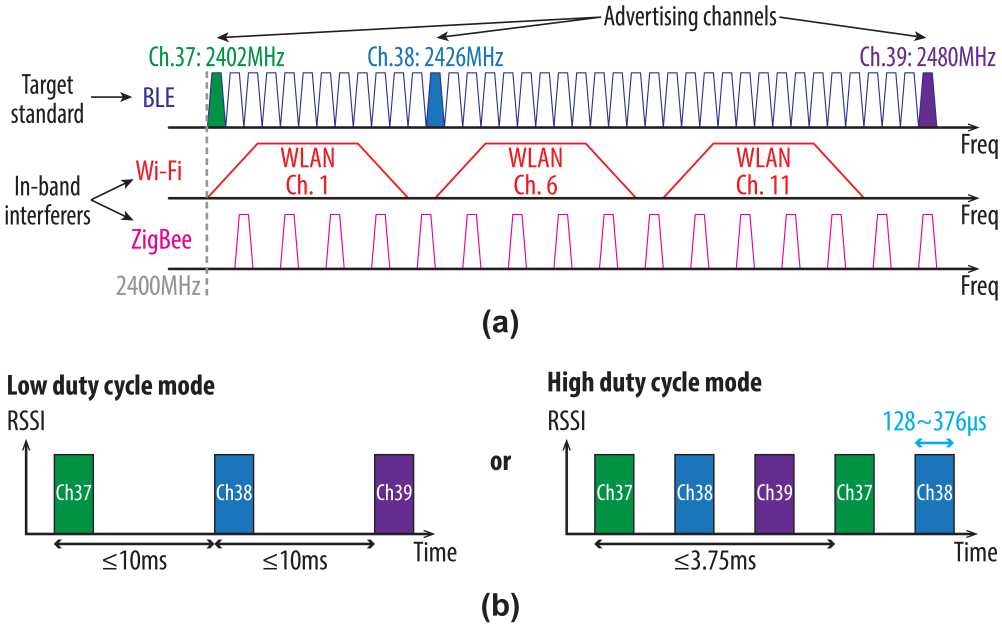


Figure 4.1: BLE standard: (a) channel allocation and (b) advertising event structure.

Since high-data-rate GFSK demodulation is difficult to accomplish at sub-mW power, prior work has suggested using back-channel communication methods to reduce power. A simple way to do this is to have the BLE transmitter simply repeat bits within the advertisement packet to effectively reduce the data rates, as shown in Fig. 4.2(a). For example, bits in an advertisement packet were each repeated 16$\times$ in [56]. This enables a low-latency wake-up scheme. However, building a GFSK demodulator is still difficult to do at sub-mW power levels without compromising frequency accuracy.

Instead of trying to demodulate the GFSK symbols, another form of backchannel communication is to instead detect the energy of an entire packet - where an entire packet forms a logic '1' OOK symbol. This allows for a very low power energy-detecting architecture operating with inherently low bandwidth. An example of this is found in [9], where wake-up information is encoded using the total advertising duration and the interval between the advertising events to create different symbols, as depicted in Fig. 4.2(b). However, this signature is a multi-event message, which has a latency larger than 1 s.

To reduce wake-up latency, another prior-art signature encoded information in two dimensions: 1) the Received Signal Strength Indicator (RSSI) of a single packet, and 2) the length of said packet [15], as shown in Fig. 4.2(c). This approach enables wake-up latency of a single advertising packet (128$\sim$376 μs).

However, both of the above backchannel wake-up signatures do not have any channel frequency differentiation, and are therefore susceptible to nearby interference. To address this issue, a backchannel wake-up signature via detecting the energy of the channel hopping sequence was proposed in [57], a part of which was also independently proposed in [18]. The design in [57] detects the energy at all three advertising channels, and checks if the hopping order matches with a predefined sequence, as depicted in Fig. 4.2(d). This 3-FSK-like modulated signature only requires OOK energy detection at each channel, and can achieve low latency (i.e., 1 advertising event) when operating in the fast-hopping mode, yet with only 27 possible coding combinations within an event.

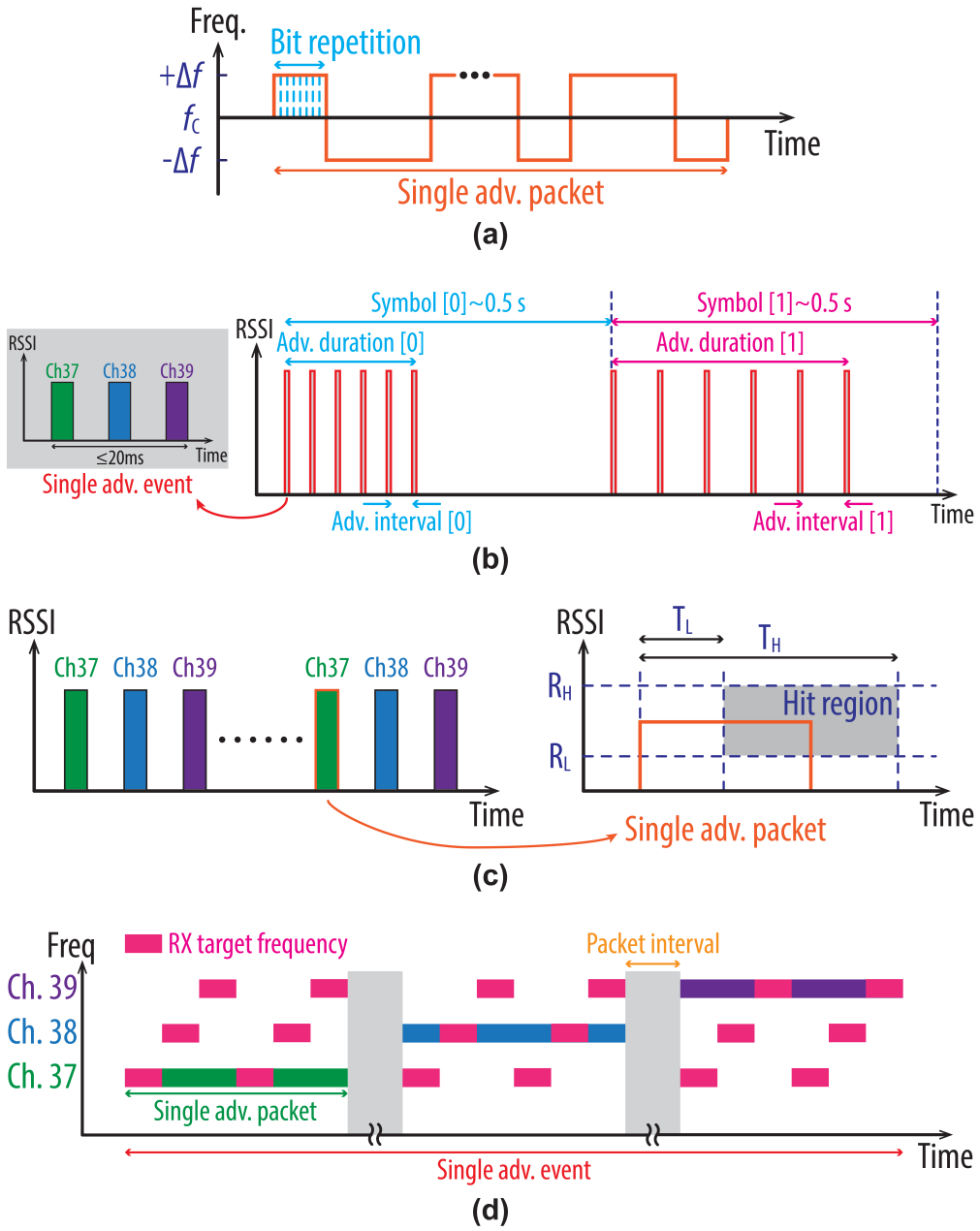
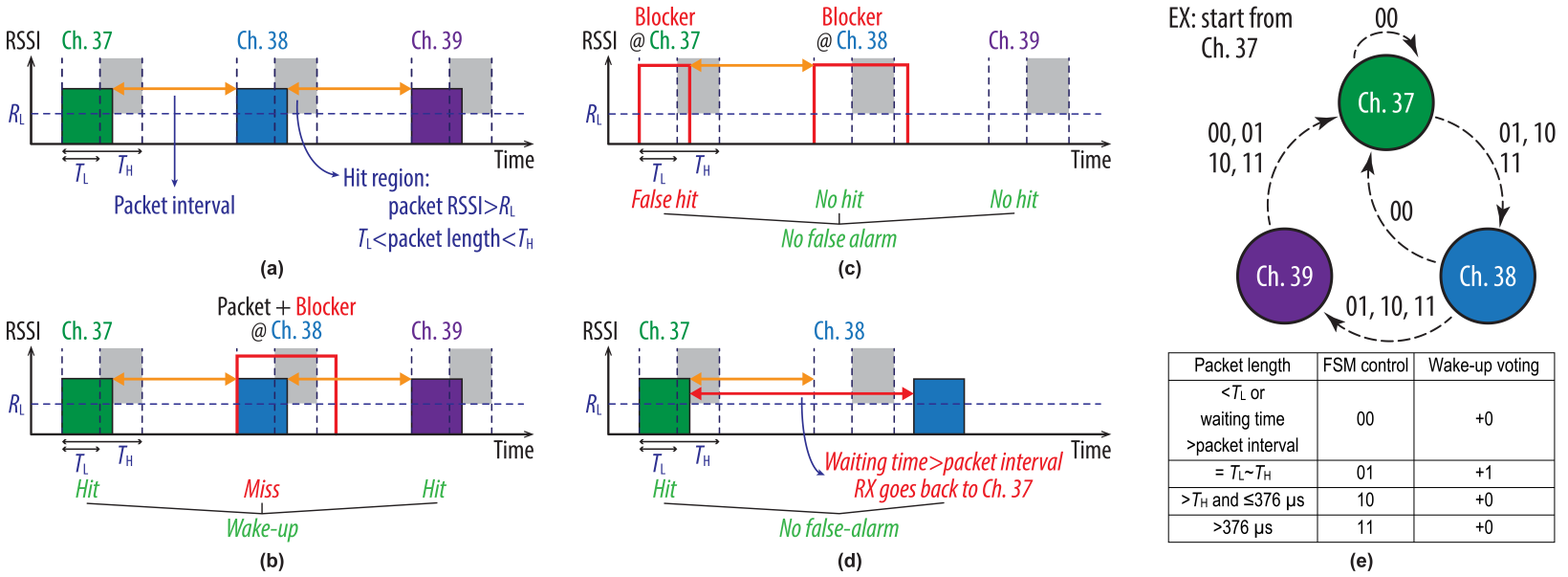


Figure 4.2: Prior-art BLE-compatible wake-up signatures via: (a) direct GFSK modulation with bit repetition; (b) modulating total advertisement duration and the interval between advertising events; (c) detecting single-packet RSSI and packet length; and (d) detecting channel hopping sequence and packet interval.

4.2.2 Proposed 4-Dimensional Wake-Up Signature

Based on the above discussion, there are several knobs that can be used to create a more diverse BLE-compatible wake-up signature. Specifically, this work combines the power threshold and packet length dimensions similar to [15] but without incorporating absolute RSSI, along with the channel hopping and packet interval dimensions [57] to provide four total wake-up signature dimensions [18]. The overall concept is depicted in Fig. 4.3. The main idea here is to make a majority voting decision for the correct packet length while meeting a minimum power threshold at all 3 advertising channels within the correct packet interval. If the signal strength of the received packet is larger than a pre-defined lower bound R_{L}, and the packet length is between the pre-defined lower bound T_{L} and upper bound T_{H}, we say that it generates a hit (Fig. 4.3a). Because of its multi-dimension nature, the proposed wake-up signature can theoretically provide millions of possible distinct signatures within a single advertising event (e.g., with a 1 μs resolution, 128$\sim$376 μs packet length provides 249 different symbols, and up to 10 ms packet intervals provide 10,000 different symbols, which together provide around 2.5 million combinations just from these two dimensions). In practice, however, an 8 μs resolution is chosen in this design by compromising code diversity in order to achieve high sensitivity by limiting baseband bandwidth, and to achieve low power by limiting baseband clock frequency. With 32 different packet lengths and 1206 different packet intervals in this configuration, over 38,000 distinct signatures can still be achieved, which is more than sufficient for most short-range BLE-based networks. This number is derived without considering power threshold in this design, which can help code diversity across sensor nodes by adjusting sensitivity, but not within node diversity without a dedicated RSSI detector like [15]. Although most commercial products hop from channels 37 to 38 and then 39, this is not necessary in the BLE standard or in the presented design. If channel hopping sequence were added, over 230,000 unique signatures are available.

Figure 4.3(b) depicts an example of how the proposed signature can avoid missed



Packet length	FSM control	Wake-up voting
<T_L or waiting time >packet interval	00	+0
= T_L~T_H	01	+1
>T_H and ≤376 μs	10	+0
>376 μs	11	+0

(e)

Figure 4.3: Proposed 4D BLE-compatible wake-up signature: (a) The overall wake-up signature structure. (b) Avoiding missed detection caused by a potential blocker. (c) Avoiding false alarms caused by a potential blocker. (d) Avoiding false alarms caused by signature with the same pulse width but a different packet interval. (e) The majority wake-up voting and channel selection algorithm.

detections caused by blockers. In this example, both the first packet at Ch. 37 and the third packet at Ch. 39 are within the target specifications and generate hits, yet the second packet comes along with a strong blocker that exceeds the hit region and causes a miss. However, thanks to the majority voting algorithm, the WuRX still indicates it is a wake-up event despite the blocker. Another example scenario is shown in Fig. 4.3(c). Assuming there is a blocker at Ch. 37 that makes a false hit, the WuRX then turns to Ch. 38 and then Ch. 39 to check if there are correct packets as well. If there are no hits in both channels, after majority voting no false alarm will occur.

This 4-D signature can also avoid false alarms caused by another signature with the same pulse width but different packet interval, as shown in Fig. 4.3(d). In this example, the first packet at Ch. 37 is a hit, but the second packet at Ch. 38 does not come at the right time - i.e., the waiting time is not within the predefined packet interval. Since it is not the right signature the WuRX is looking for, the receiver goes back to Ch. 37 and no false alarm will occur.

All the above scenarios follow the proposed majority wake-up voting and channel selection algorithm, whose state diagram is shown in Fig. 4.3(e). In this example, the channel selection starts from Ch. 37, although this is just the usual starting channel in commercial products and the channel sequence could be easily changed. If the packet length at the first channel is less than T_{L}, or the waiting time is not within the predefined interval, the finite state machine (FSM) control bits are 00 while the wake-up voting does not count and the WuRX remains at the starting channel (Ch. 37 in this example). If the WuRX detects a packet that is within the hit region, the FSM control bits are 01, which enables wake-up voting to add one and changes the WuRX to the next channel (Ch. 38 in this example). If, on the other hand, a packet with duration larger than T_{H} is detected in the first channel (Ch. 37 in this example), since the WuRX can not distinguish if there is a desired packet buried within a blocker, the WuRX turns to the next channel (Ch. 38) just in case there was indeed a packet buried under the blocker; however, this is not considered a true hit, and the wake-up voting does not count up. At the next channel (Ch. 38 in this example), if no hit is detected, the FSM control bits

are 00, and the WuRX goes back to the first channel (Ch. 37 in this example), and the first packet is determined to be a false hit. However, if the second channel does hit, then the WuRX further turns to the final channel (Ch. 39 in this example). After interrogating all three channels, the majority voting decides whether there is a wake-up event or not. It will be shown later that the proposed 4D wake-up signature, combined with the proposed WuRX architecture and frequency planning, enables the proposed design to achieve low power, high sensitivity, and interference-resiliency.

4.3 Wake-Up Receiver Architecture

4.3.1 Prior-Art BLE-Compatible WuRX Architectures

Due to the growing demand for BLE devices, there has been significant recent work towards developing high performance and low-power BLE transceivers [58–62]. While these designs are great candidates for the main BLE radio, such architectures do not consume sub-mW power, and are thus not well suited as WuRXs. Fortunately, simplified, lower-power architectures can be enabled by incorporating backchannel-based modulations schemes. An overview of prior-art BLE-compatible WuRX architectures based on backchannel communication is shown in Fig. 4.4.

The lowest-power BLE-compatible WuRXs tend to encode information in the energy of entire packets. This enables use of simple energy-detection-based architectures, the simplest of which is shown in Fig. 4.4(a). By removing any active RF amplification and LO generation, and using an envelop detector (ED) to directly convert down to baseband (BB), nW-level powers are achievable in general WuRX applications [8], or specifically for BLE [9, 15]. However, wideband energy detection with limited pre-ED RF filtering implies limited channel selectivity, which causes any nearby interferers to also demodulate to BB. Additionally, wideband demodulators, particularly without significant pre-ED RF gain, also introduce significant noise [32]. For these reasons, prior-art BLE WuRXs using this architecture were limited to sensitivities of -56.5 dBm [9]

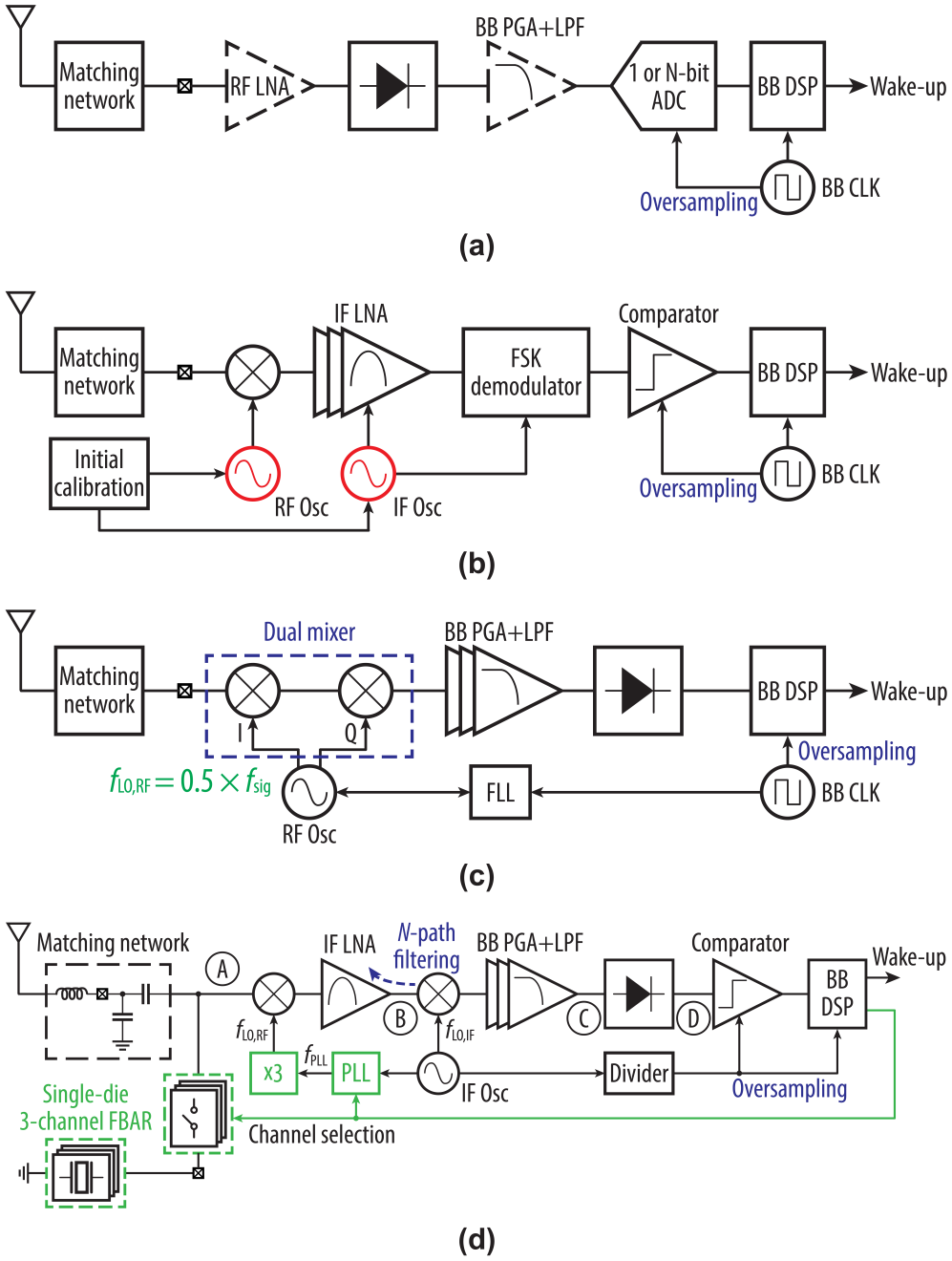


Figure 4.4: Sub-mW BLE-compatible WuRX architectures: (a) direct envelope detection architecture; (b) mixer-first architecture without frequency locked LO; (c) dual mixer-first architecture with frequency locked LO; and (d) proposed mixer-first two-stage heterodyne architecture.

and -58 dBm [15], at powers of 236 nW and 164 μW, respectively.

On the other hand, mixer-based architectures, which normally consume 10s-

to-100s of μW because of LO generation, can achieve high sensitivity and interference resiliency by mixing down the signal to either an intermediate frequency (IF) or BB, thus leveraging more power-efficient amplification as well as sharper multi-stage filtering than at RF. In [56], a mixer-first heterodyne architecture was adopted and achieved a sensitivity of -80 dBm at 230 μW (Fig. 4.4b). However, the LO employed in this design was free-running at a single-channel, and thus could encounter static process variation and frequency drift. Moreover, no image rejection was employed, leading to potentially large interference issues. To save power, another approach utilized a dual mixer-first homodyne architecture with frequency-locked LO that only required the LO frequency to be half of the signal frequency to save power as described in [57] and illustrated in Fig. 4.4(c). Although this design achieved high interference rejection and could operate across multiple different channels, it achieved a sensitivity of -57.5 dBm while consuming 150 μW.

4.3.2 Proposed WuRX Architecture and Frequency Plan

The proposed WuRX employs a two-stage mixer-first heterodyne WuRX architecture, and is shown in Fig. 4.4(d). Here, the matching network first performs an impedance transformation to provide passive voltage gain. An integrated single-pole triple-throw (SP3T) switch is connected to a single-die 3-channel FBAR filter that provides direct BLE advertising channel filtering and, more importantly, image rejection before the first down-conversion. After the first down-conversion, but before the second down-conversion, the IF LNA first provides power-efficient signal amplification (compared to if amplification were instead performed at RF). The IF mixer then performs the second down-conversion and also serves as an inherent N-path filter [27]. After the second down conversion, the BB programmable gain amplifiers (PGAs) with low-pass filters (LPFs) further provide signal amplification and reject both noise and interference to increase the ED output signal-to-noise-ratio (SNR). After the energy detection via the non-linear ED, the ED output is then over-sampled and digitized by the compara-

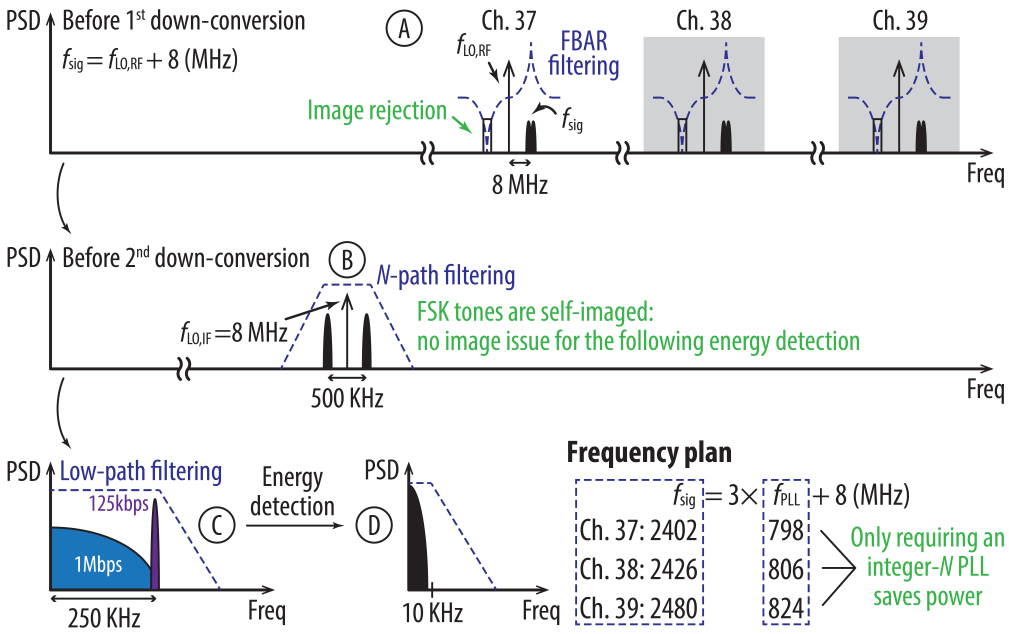


Figure 4.5: Frequency plan and multi-stage filtering of the proposed WuRX.

tor, which serves as a 1-bit analog-to-digital converter (ADC). Finally, the digital BB controls the channel selection sequence for the RF front-ends according to integrated wake-up logic.

The IF LO is generated by an off-chip 8 MHz crystal reference and serves as a global clock. The RF PLL is locked to the IF LO, and then is fed to a frequency-tripler to generate the RF LO. Circuit details of all of these blocks will be explored in the next section.

The frequency plan of the proposed WuRX is depicted in Fig. 4.5. At point A in Fig. 4.5, the signal frequency is 8 MHz higher than the RF LO frequency, and consequently there is an image counterpart at 8 MHz lower than the RF LO frequency. However, the FBAR notch is ideally placed right at the image frequency to provide image rejection. After first down-conversion at point B, the 500 kHz-spaced GFSK signal tones are centered at 8 MHz, and the N-path filter reduces the out-of-band noise and interference. The 8 MHz IF LO then makes the GFSK tones self-image to each other and down-converts the signal without any image issues for energy detection purpose. At point C, the GFSK signal spectrum is mainly decided by the data rate of the employed

BLE standard. For example, at the low data rate setting of 125 kbps in BLE 5.0, the spectrum will look like an FSK signal. The signal is then low pass filtered by the PGAs. Finally at point D, the ED performs the squaring function and low pass filters the packet energy.

Thanks to the careful frequency plan depicted in Fig. 4.5, it is shown that the required RF LO frequency for the three BLE advertising channels at 2402, 2426, and 2480 MHz can be generated in a low-power manner via an integer-N PLL operating at 798, 806, or 824 MHz and locked to a 2 MHz reference (which can be generated via dividing the 8 MHz IF LO by 4) with divider ratios of N=399, 403, and 412, respectively. In this manner, fractional-N synthesis is not required.

4.4 Circuit Implementation

4.4.1 RF LO Generation

According to the proposed frequency plan shown in Fig. 4.5, the RF LO can be generated by a combination of an integer-N PLL and a frequency tripler. Figure 4.6(a) shows the frequency synthesis block diagram. For the integer-N PLL, a standard type-II PLL is adopted and the channel is selected by changing the divider ratio. The voltage controlled oscillator (VCO) is implemented via a ring oscillator that provides the 6 clock phases needed for the subsequent frequency tripler. The frequency tripler is implemented via an AND-gate based edge combiner, which, by feeding in two clocks from the PLL with 120 degrees phase difference, can generate a clock frequency, $f_{\mathrm{LO,RF}}$, that is 3 times higher than the PLL frequency, f_{PLL}. Compared to implementing a 2.4 GHz VCO directly, this approach although does not help reduce the LO buffer power because of the 3 driving paths, rather, it saves the portion of the 800 MHz VCO and PLL divider power by $3\times$, which results in an overall 46% of RF LO power reduction based on simulation. Moreover, compared to LC-VCO-based designs [17, 56], the power consumption of the proposed RF LO generation can be scaled lower with a smaller

geometry process technology. Although LC-VCOs have better phase noise than ring-VCOs, the non-coherent energy detection of entire BLE advertisement packets does not require extremely good phase noise (i.e., -80 dBc/Hz at 1 MHz frequency offset Δf to the carrier frequency is sufficient [63]).

To achieve the desired divider ratio with programmability, an 8-stage Divide-by-2/3 modular N divider [64] is adopted as depicted in Fig. 4.6(b). Although the maximum operating frequency has already been relaxed by 3 times because of the frequency tripler, true single-phase clock (TSPC) based D flip-flops (DFFs) are still required for the first 2 stages of the Divide-by-2/3 cells to ensure sufficient speed because of the low supply voltage (i.e., 0.5 V). The remaining stages using static logic to ensure proper operation at low frequency with low power.

Figure 4.6(c) shows the schematic of the designed ring VCO. To generate the required 6 clock phases, a 3-stage ring oscillator core using pseudo-differential delay cells is implemented, which has better common-mode noise rejection than a single-ended design. The entire ring VCO adopts a current-starved architecture to achieve wide frequency tuning range to combat process variation. However, the resulting VCO gain, K_{VCO}, would be too large especially under a low supply voltage, which is not ideal in terms of design trade-offs between phase noise, reference spur, loop filter capacitor size, and power consumption [65].

To solve this issue, the VCO frequency is controlled by both a coarse tuning section, which provides a set of frequency overlapping curves that cover the entire tuning range, as well as a fine tuning section, which changes the VCO frequency along a certain curve and decides K_{VCO} [65]. For coarse tuning, two binary-weighted 5-bit resistor DACs, which provides a frequency tuning of $\sim$28 MHz/bit on average and covers $\sim$900 MHz, are connected to the virtual supply rails of the ring oscillator core, and are calibrated one time to put the VCO into the desired tuning range initially. For fine tuning, which is part of the PLL loop, a voltage controlled current source feeds the ring oscillator core, and a binary-weighted 6-bit resistor DAC at the source of transistor $M_{\mathrm{N},1}$ linearizes the tuning curve while adjusting K_{VCO} to be 200 kHz/mV in this design that

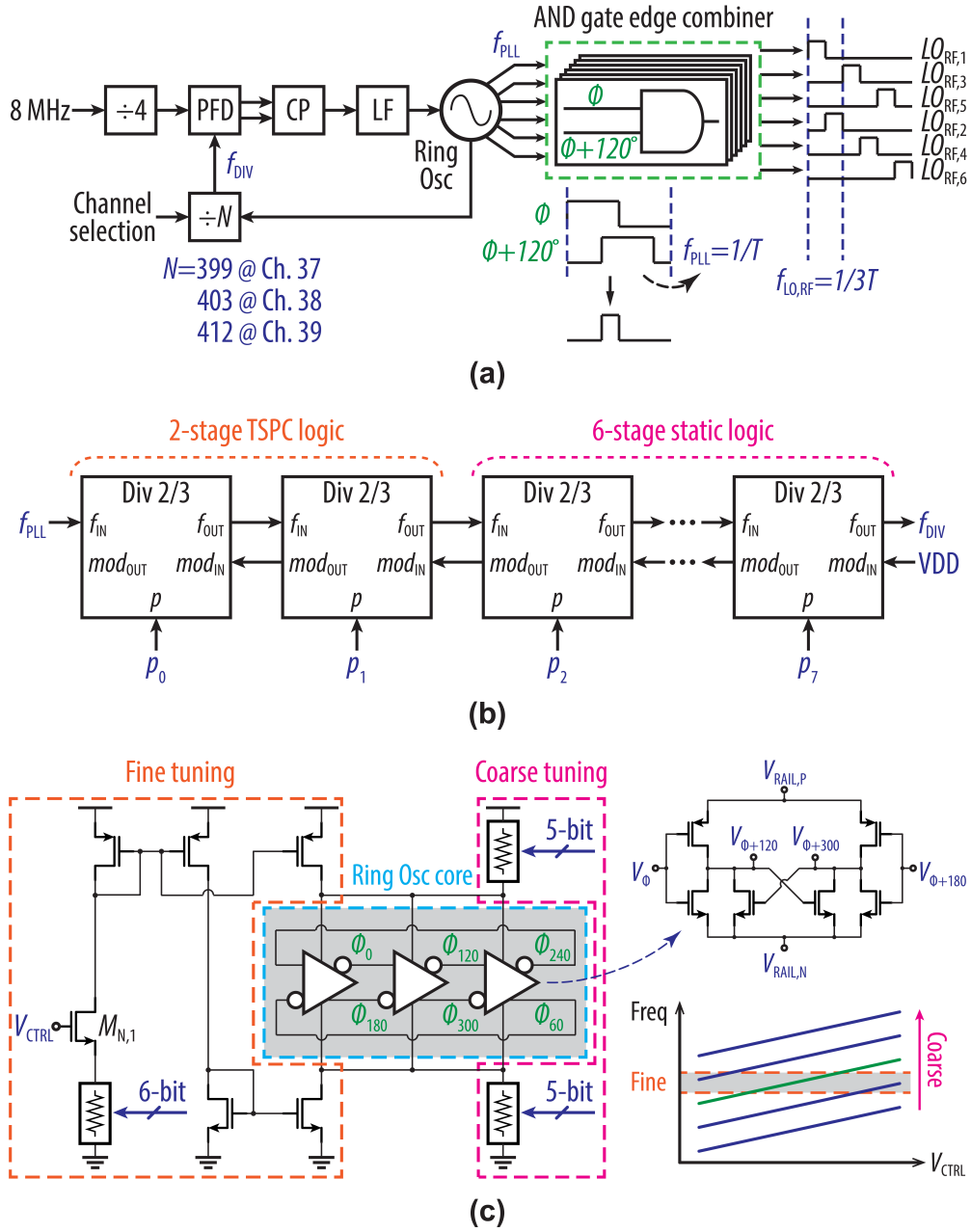


Figure 4.6: Proposed RF LO generation: (a) complete schematic; (b) Divide-by-2/3 modular N divider; and (c) 3-stage pseudo-differential ring VCO with fine and coarse frequency tuning section.

covers 60 MHz of tuning range for single curve with charge pump current source maintaining in saturation region, which is sufficient for the required 26 MHz tuning range from 798∼824 MHz. Moreover, the PLL settling time is ∼22 μs based on simulation,

which is sufficient for the minimum 345 μs packet interval based on the BLE signal generation software available in most commercially available phones.

4.4.2 RF/Analog Signal Chain

The overall RF/analog signal chain is depicted in Fig. 4.7(a). A 0.25 mm^2 FBAR filter that consists of 3 distinctive resonators on a single die is adopted here to provide direct advertising channel filtering. Each FBAR filter has a 3 dB bandwidth of 9.7 MHz and, more importantly, image rejection as discussed in Section 4.3. The FBAR filters have intrinsic quality factors of 1040 considering both parallel and series resonance. The FBAR temperature coefficients are 0.89 ppm/°C, which implies at most 200 kHz of variation across 0$\sim$100 $^{\circ}C$, which is more than sufficient for the non-coherent receiver [66]. Bondwire length variation can alter the center frequency by up to 200 kHz/100 μm based on simulation, which again is within tolerances of the non-coherent architecture.

In order to properly filter, an impedance matching network is placed between the 50 Ω source and the FBAR filter, transforming the effective parallel resonant impedance of the FBAR to look like 50 Ω from the perspective of the source. This matching network also conveniently happens to provide 9 dB of passive voltage gain prior to the mixer. An integrated SP3T switch controlled by the digital BB is connected to the FBAR die to select the desired resonator for the target channel. For this first prototype design, the parallel resonance frequency of the FBAR is made $\sim$12 MHz higher than the target center frequency for each channel to compensate for the capacitance introduced by the pads and switches. The center frequency is then tuned by an on-chip nominally 300 fF varactor that could vary from 100$\sim$500 fF at the bonding interface.

The mixer incorporates both mixing and frequency tripling operating together in one block via a 6-switch passive mixing structure (Fig. 4.6a). The on-resistance value of the RF passive mixer is crucial and is chosen to be 500 Ω in this design to balance the power and noise performance, as a high resistance value will degrade the noise figure (NF), while a low resistance value will enlarge the transistor size and therefore require

a high power LO buffer to drive.

After the first down-conversion, the signal is amplified by an IF LNA, whose schematic is shown in Fig. 4.7(b). A current re-use inverter-based architecture is adopted to combine both the NMOS and PMOS transconductance g_{m}, which effectively doubles the g_{m} and achieve better noise performance for the same current consumption. A feedback resistor R_{F} is used to self-bias the transistors.

The IF signal is then down-converted a second time by a double-balanced passive IF mixer, which also serves as a N-path filter (N=2) load for the IF LNA to filter out unwanted noise and interferers [27]. After the second down-conversion, a 3-stage PGA/LPF provides 27$\sim$45 dB of gain as part of the power threshold setting to condition and filter the 250 kHz down-converted signal. Figure 4.7(c) shows the schematic of a single stage PGA, which consists of a one-hot-coded 3-bit resistor DAC that provides a 3 dB gain step, and two binary-weighted 3-bit capacitor DACs that set the LPF corner frequency. Moreover, instead of using large inter-stage AC-coupling capacitors, a DC-offset cancellation loop is implemented to prevent the 3-stage PGA being saturated by any DC-offset caused by mismatch. At high PGA gain settings, the WuRX sensitivity is limited by the linear amplification portion of the signal chain, which has a NF of 22.6 dB based on simulations. The RF mixer switch and the IF LNA contribute the most noise, accounting for $\sim$43$\%$ and $\sim$50$\%$ of noise, respectively.

After the linear amplification portion of the signal chain, a cross-coupled self-mixing ED shown in Fig. 4.7(d) is designed to rectify a differential signal to a pseudo-differential BB signal, which helps to forgo the need of a precise voltage reference for the following comparator. A two-stage dynamic comparator with 125 kHz clocking frequency is implemented to digitize the ED output signal with a 25$\times$ oversampling ratio for a 200 μs packet. Two 5-bit capacitor DACs are used to set the comparator threshold by providing unbalanced integration time for the differential paths [12], and also serves as part of the power threshold setting (Fig. 4.7e).

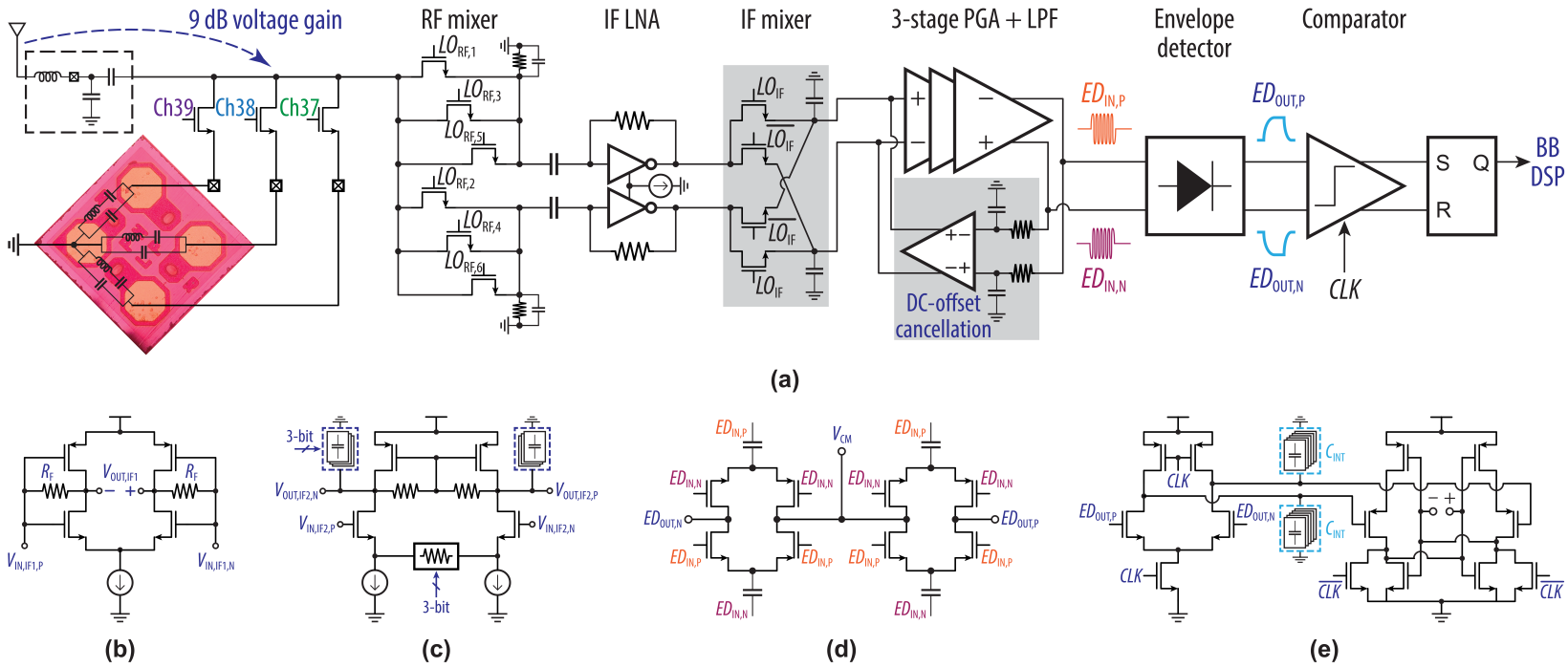


Figure 4.7: Circuit-level implementation of: (a) RF/analog signal chain; (b) IF LNA; (c) single-stage PGA; (d) envelope detector; and (e) comparator.

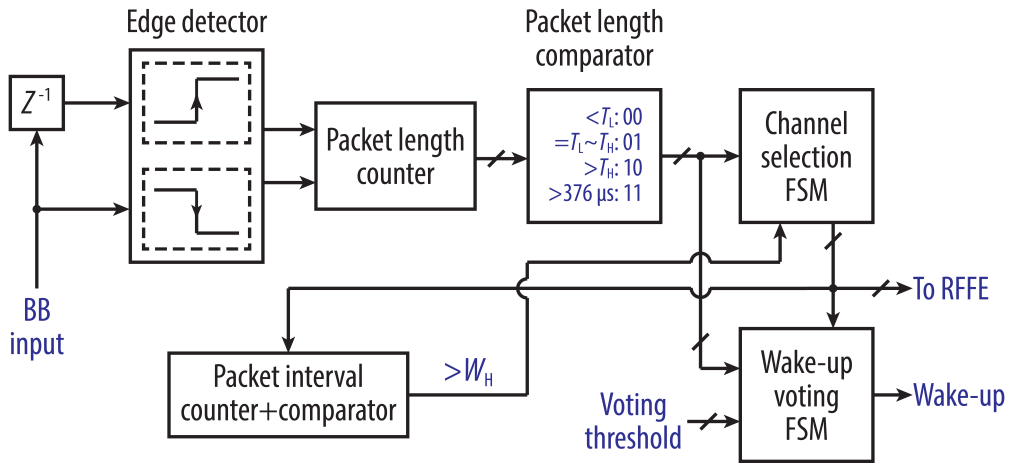


Figure 4.8: Block diagram of the digital baseband.

4.4.3 Digital Baseband

Fig. 4.8 shows the block diagram of the implemented digital BB that follows the proposed algorithm discussed in Section 4.2. An edge detector first compares the input packet with its delayed version to extract the rising and falling edge timing of the packet, which are used to compute the packet length. Some comparator logic then compares the packet length with a pre-defined window $T_{\mathrm{L}} \sim T_{\mathrm{H}}$ to generate a 2-bit control for the channel selection FSM and the wake-up voting FSM. The 2-bit state output of the channel selection FSM controls the RF front-end to receive the desired channel, while providing the current sequencing order for the other blocks. Finally, the wake-up voting FSM generates the wake-up signal after 3-channel scanning and comparison with a pre-defined voting threshold.

Importantly, a packet interval computation is enabled after the first packet is received and causes an FSM state change. If the packet interval is larger than a upper bound duration W_{H} and still no new packet is received, the FSMs rotate back to the initial stage. Therefore, the packet interval computation logic provides another dimension of correlation with the wake-up signature and also prevents the FSMs to be locked in a specific state.

Since a 0.5 V supply is used, the entire digital BB operates in the sub-V_{t} re-

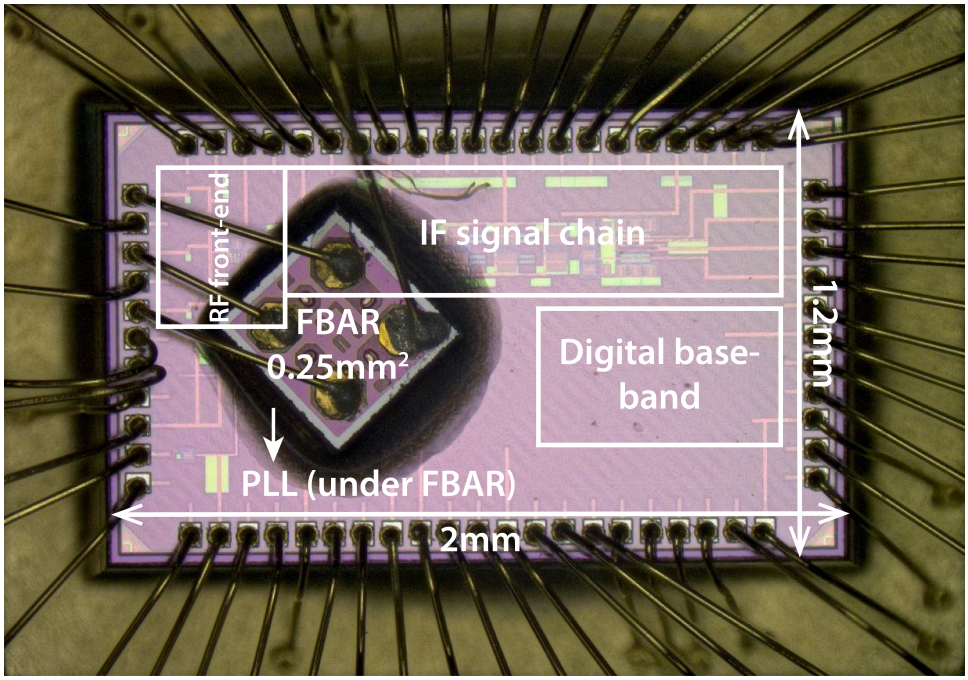


Figure 4.9: Die micrograph of the WuRX employing a single-die 3-channel FBAR die stacked on top of the WuRX die.

gion and therefore all the custom logic gates were designed using only inverters and transmission gates for the highest robustness [41].

4.5 Measurement Results

The proposed BLE-compatible WuRX is fabricated in a 65 nm process, occupying 1.3 mm^2 of core area. The 0.25 mm^2 three-channel FBAR die is mounted on top of the chip and directly wirebonded. All measurements are taken from the wirebonded design. A die and wirebonding photo is shown in Fig. 4.9.

The input return loss of the WuRX is measured across all three advertising channels, i.e., 2402, 2426, and 2480 MHz, in Fig. 4.10. Each channel is individually selectable by the integrated SP3T switch, and all three channels achieve better than -15 dB $|S_{11}|$.

Figure 4.11 shows that the PLL output can be locked to the desired frequencies

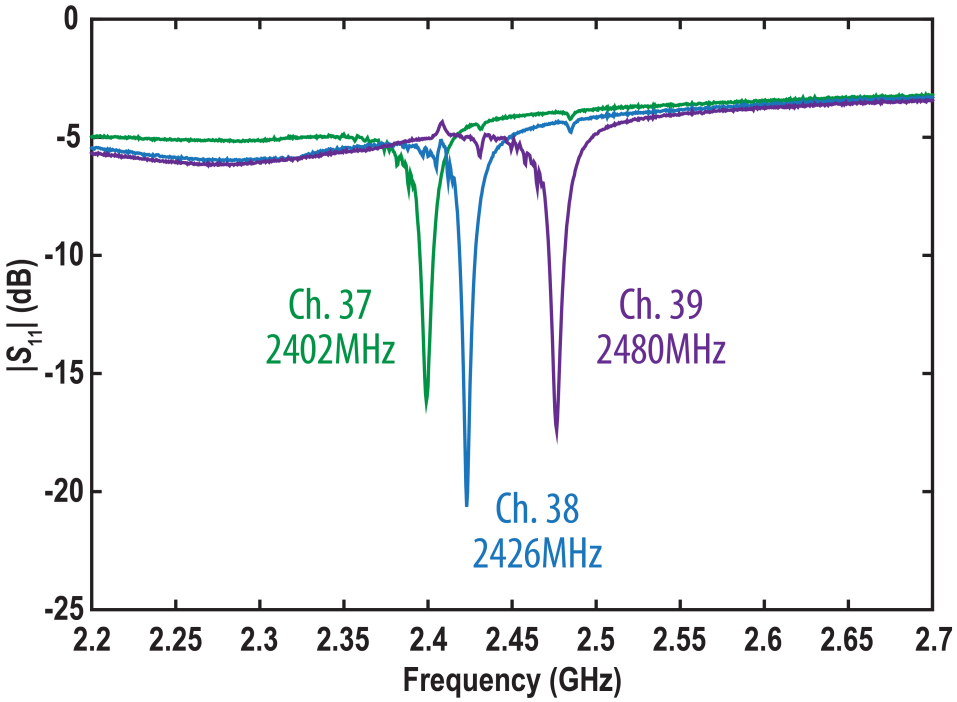


Figure 4.10: Input matching $|S_{11}|$.

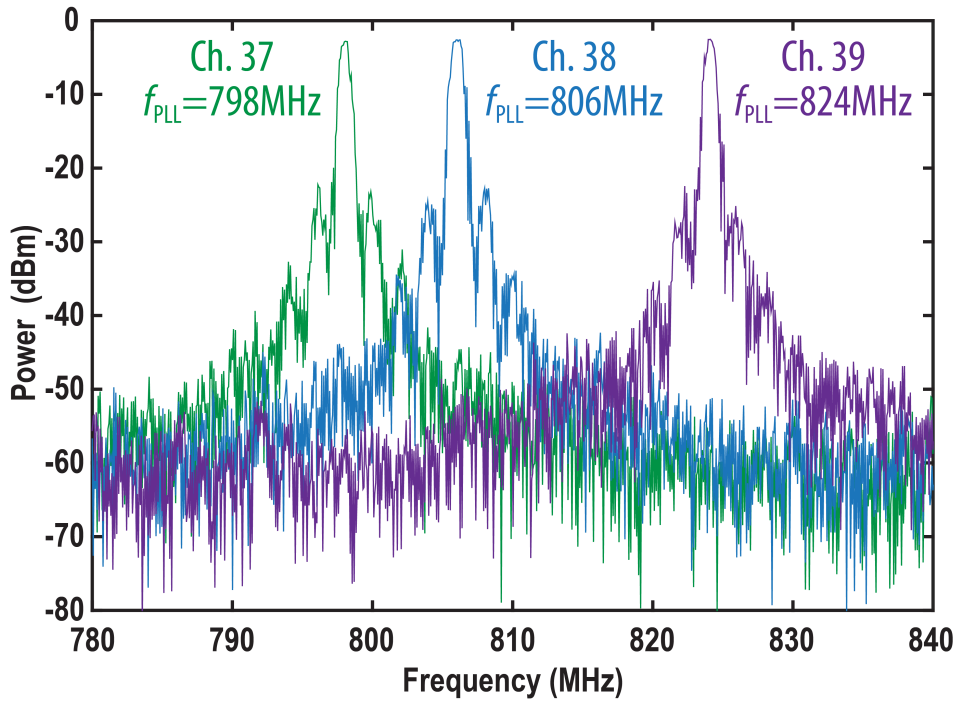
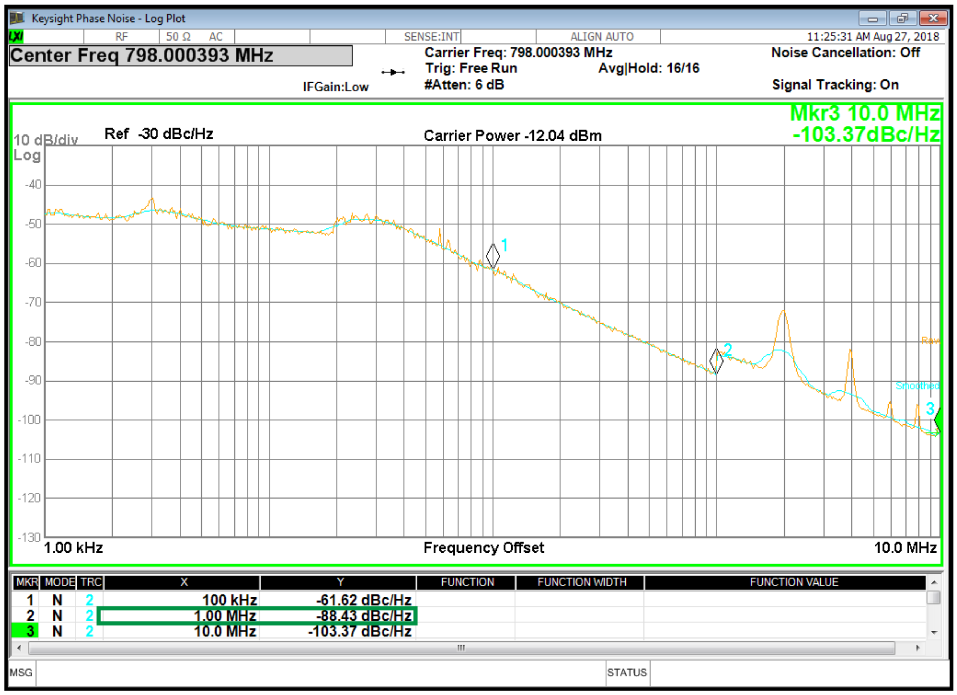


Figure 4.11: PLL output spectrum showing individual locking to three different channel frequencies.



LO phase noise @ 1MHz offset = -88.43 + 20log3 ≈ -79dBc/Hz

Figure 4.12: Measured PLL phase noise.

at 798, 806, and 824 MHz respectively for each advertising channel. The measured PLL output phase noise at 1 MHz $|\Delta f|$ is -88.4 dBc/Hz as shown in Fig. 4.12, which, after the frequency tripler, corresponds to ~ -79 dBc/Hz and is sufficient for a mixer-based OOK-demodulated receiver [63].

Figure 4.13 shows the missed detection ratio (MDR) waterfall curve under single channel operation (i.e., without the benefit from the majority voting mechanism), using asynchronous transmissions and a pseudo-random binary sequence (PRBS) modulated BLE signal. Under these conditions with a total of 10,000 wake-up signals sent at ± 1 dB of sensitivity level, the BLE-compatible WuRX achieved a MDR of 0.1% at -85 dBm with a false alarm rate of < 2/hr. When configured with a slightly higher comparator threshold setting, the chip achieved a sensitivity of -84.5 dBm with no false alarms observed within an hour.

The performance of the proposed WuRX in the presence of interference is char-

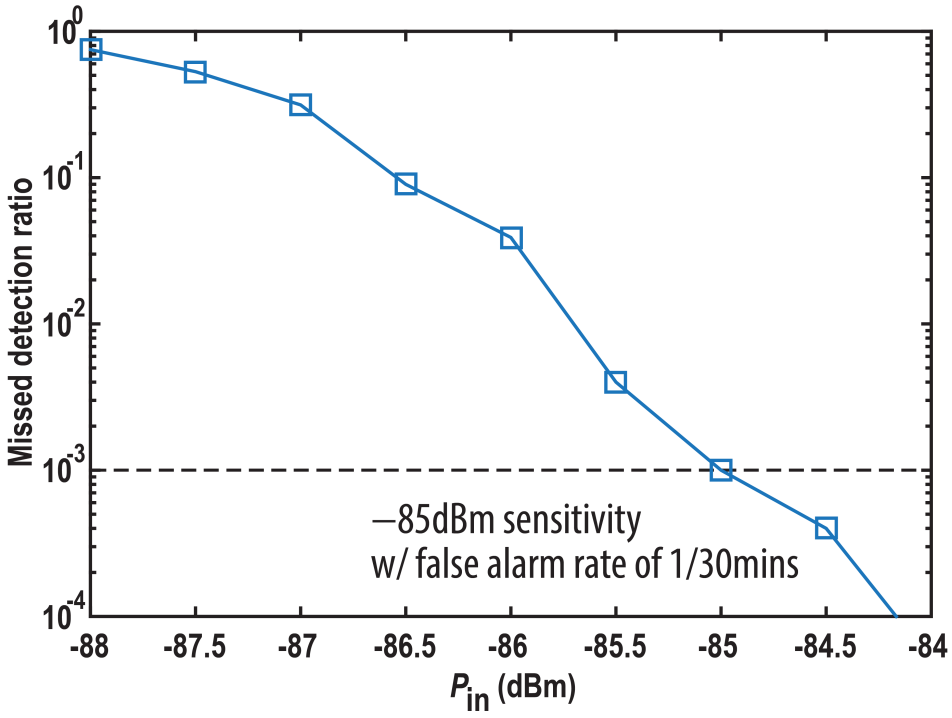


Figure 4.13: MDR waterfall curve for various input power levels.

acterized by the signal-to-interference ratio (SIR) measurements shown in Fig. 4.14, where the interferer power is defined as the power needed to achieve 0.1% MDR when the signal is 3 dB higher than at the nominal sensitivity point. Here, PRBS-modulated BLE and 802.11g Wi-Fi jammers are used throughout all measurements. For single channel operation without frequency-hopping and voting mode enabled, -23 dB SIR at 10 MHz $|\Delta f|$ is achieved, as shown in Fig. 4.14(a). If the FBAR notch was placed at -16 instead of a -27 MHz Δf (due to a fabrication error), the image rejection would have been improved by a further $\sim$10 dB. This can be rectified by properly tuning the FBAR fabrication process.

Figure 4.14(b) shows the SIR improvement when the 3-channel operation with frequency-hopping and voting mode is enabled. The worst case scenario happens when a jammer is present at the same time as the desired wake-up signature and exists throughout the entire advertising event. It should be noted that this worst-case scenario is very unlikely because of packet length limitation from each standard. In this worst-case sce-

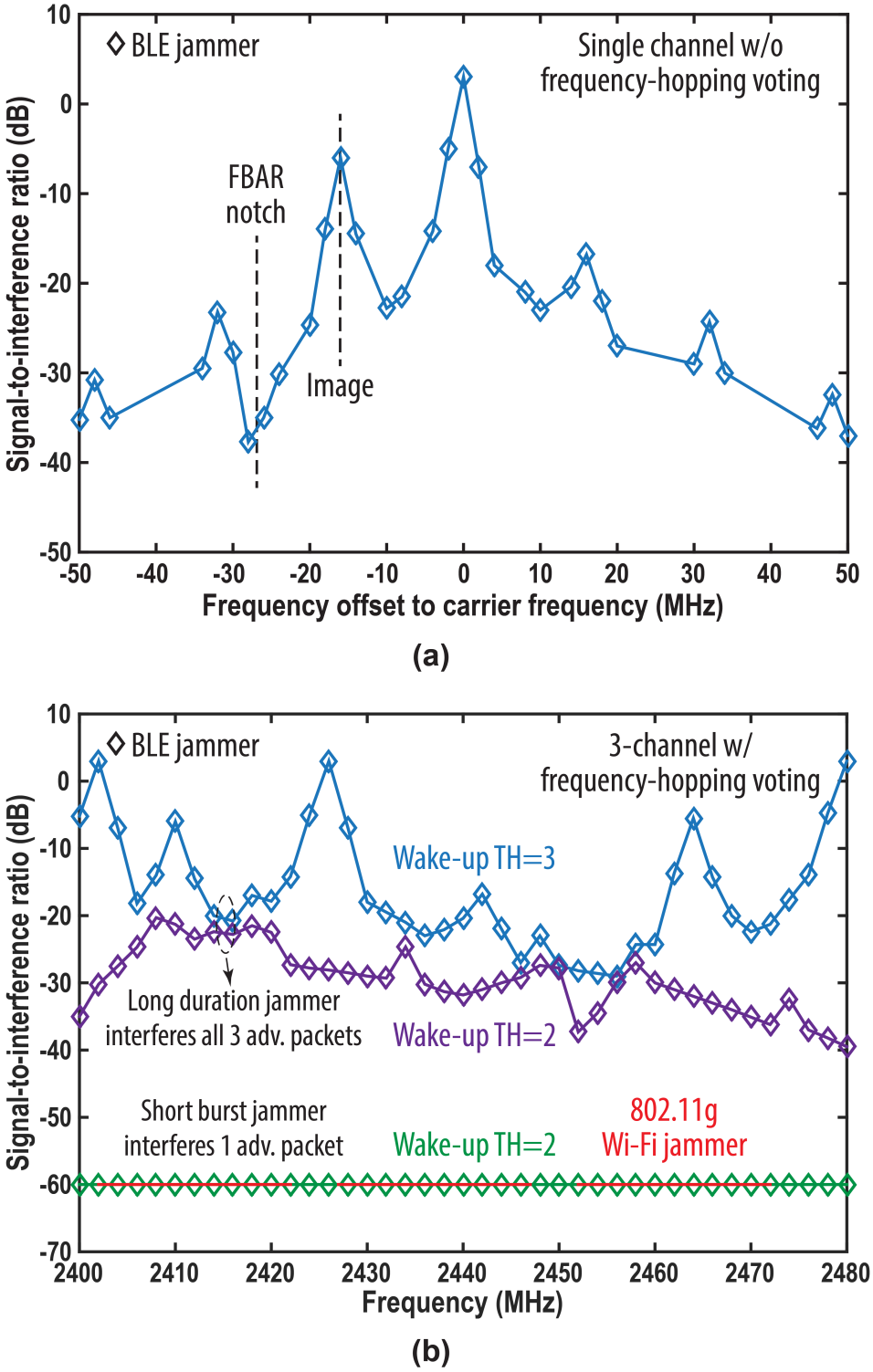


Figure 4.14: SIR measurement under: (a) single-channel operation at Ch. 37; and (b) 3-channel operation.

nario, if the wake-up voting threshold is set to be three (i.e., the voting mechanism is disabled), then the SIR is limited by the most susceptible channel, as shown by the blue curve. However, if the wake-up voting threshold is set to be two, then the SIR improves, especially at the frequency close to the advertising channels as shown by the purple curve. The SIRs of both cases can be further improved from FBAR notch rectification as well. In a more likely scenario where a short burst of jammer packets disrupts one of the three advertising packets, then by setting the wake-up voting threshold to be two, the SIR achieves up to -60 dB throughout the entire band for both BLE and 802.11g Wi-Fi jammers, with that number being artificially limited by test equipment and is in fact likely to be even better in reality.

To verify the proposed WuRX is indeed compatible with real BLE devices and validate a realistic use case, a wireless measurement was taken by connecting the WuRX to an antenna in a normal lab environment and using commercial mobile phones directly as the signal sources, as shown in Fig. 4.15. To validate coding diversity and interference resilience, two BLE advertising sources with different packet lengths were used, and only the signature with the correct packet length can generate a wake-up as depicted in Fig. 4.15(a). To verify the interference combating capability, two phones playing videos over Wi-Fi were placed next to the antenna, while a phone that delivered the BLE advertisement packets was placed upwards of 10 m away (1 m shown for clarity in Fig. 4.15b). As shown on the oscilloscope traces, even though one advertisement packet (in this case, Ch. 38) was corrupted by a Wi-Fi blocker, a wake-up signal was still be generated because of the proposed frequency hopping and voting mechanism. Moreover, to verify the WuRX tendency to create unwanted false alarms, three phones playing videos over Wi-Fi were placed next to the antenna and no false alarms were observed for at least 30 minutes (Fig. 4.15c). Further experiments have been made by maintaining the measurement setup in the normal lab environment with all the Wi-Fi connected devices (e.g., routers) still operating while the comparator threshold was tuned to achieve 0.1 $\%$ MDR when the signal is 3 dB higher than the sensitivity (i.e., for a -82 dBm signal), and no false alarms were observed for at least 24 hours thanks to

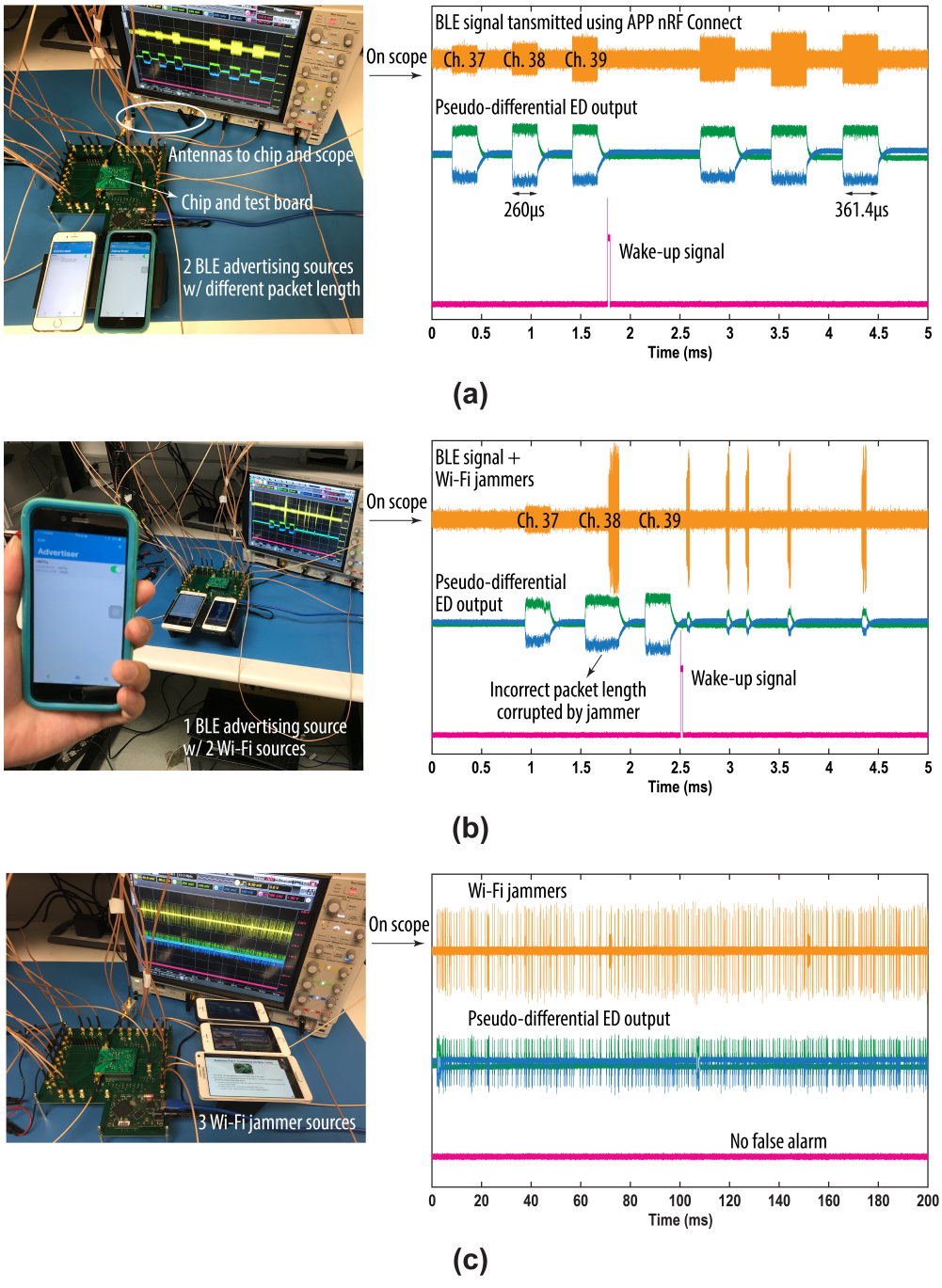


Figure 4.15: Demonstration of correct function using mobile phones by sending: (a) two different BLE advertising packets with different packet lengths to validate coding diversity; (b) one desired BLE packets alongside two proximal Wi-Fi jammers to validate correct wake-up under interference; and (c) three proximal Wi-Fi jammers to validate false alarm performance.

Table 4.1: Power Breakdown of Proposed WuRX

IF LNA	IF PGA	Comparator	PLL + frequency tripler (including LO buffers)	Digital baseband
22.4 μW	22.2 μW	2.7 μW	166.2 μW	6.1 μW

the proposed 4D wake-up signature.

Table 4.1 shows the power breakdown of the WuRX, shows that the entire system consumes 220 μW when operating continuously. Since the power is dominated by the ring-based RF LO generation, which is mainly digital, going to a more scaled process node can help further reduce the power consumption.

Table 4.2 summarizes the measurement results of the proposed WuRX design and compares the results to the state-of-the-art BLE-compatible WuRXs. This work achieves the best sensitivity and FoM among the reported BLE-compatible WuRXs at comparable power consumption, where the FoM takes sensitivity, wake-up latency, as well as power consumption into account and is defined as [8]:

$$\mathrm{FoM(dB)} = -P_{\mathrm{SEN}} + 10\log\frac{1}{Latency} - 10\log\frac{P_{\mathrm{dc}}}{1\mathrm{mW}}, \tag{4.1}$$

Moreover, this work achieves comparable single-channel SIR with [17] while consuming $\sim$6$\times$ lower power. For further sensitivity improvement to match the state-of-art BLE main receiver sensitivity (e.g., $-$95 dBm in [61]), either a low power LNA or larger switches for passive mixer can be adopted at the expense of more power consumption under the same process node.

4.6 Conclusions

This chapter has presented a 0.5 V BLE-compliant WuRX that achieved $-$85 dBm sensitivity while consuming only 220 μW in a 65 nm CMOS process. The proposed design achieved low power and high sensitivity while supporting multi-channel frequency diversity and interference resiliency by: 1) employing a single-die 0.25 mm^2

3-channel FBAR filter for direct filtering of the 3 BLE advertising channels and image rejection; 2) integrating the energy in each advertising channel via a 4D wake-up signature incorporating frequency-hopping majority voting algorithm for low-cost BLE-compliant energy-detection-based demodulation; 3) utilizing a mixer-based two-stage heterodyne receiver that achieves low power while provides multi-stage channel filtering; and 4) implementing a 3-channel LO generator via an ultra-low-power crystal-stabilized ring-oscillator-based integer-N PLL with frequency tripler that achieves sufficient phase noise. Since the power consumption of the proposed design was dominated by the highly digital RF LO generation, advanced process nodes can be leveraged to achieve even lower power and therefore enable new power and area constraint wireless IoT applications.

This chapter is based on and mostly a reprint of the following publications: P.-H. P. Wang and P. P. Mercier, "A 220μW $-$85dBm Sensitivity BLE-Compliant Wake-Up Receiver Achieving $-$60dB SIR via Single-Die Multi-Channel FBAR-Based Filtering and a 4-Dimentional Wake-Up Signature," *IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, Feb. 2019, pp. 440-442, and P.-H. P. Wang and P. P. Mercier, "An Interference-Resilient BLE-Compatible Wake-Up Receiver Employing Single-Die Multi-Channel FBAR-Based Filtering and a 4-D Wake-Up Signature," *IEEE Journal of Solid-State Circuits*, In Press. The dissertation author is the primary author of these materials, and co-authors have approved the use of the material for this dissertation.

Table 4.2: Performance Comparison of State-of-the-Art BLE-Compliant WuRXs

	[9] ISSCC'16	[15] RFIC'17	[56] CICC'18	[57] RFIC'18	[17] JSSC'19	**This Work**	
Technology	65 nm	90 nm	65 nm	65 nm	40 nm	**65 nm**	
Die Area	2.25 mm^2	1.24 mm^2	4 mm^2	1.1 mm^2	1 mm^2	**2.4 mm^2 (1.3 mm^2 core)**	
Supply Voltage	1.0 / 0.5 V	2 V	0.75 V	1.1 / 0.9 V	1.0 / 0.9 V	**0.5 V**	
WuRX Decoding	Interval and duration of adv. events	Packet duration + RSSI	GFSK w/ bit repetition	3-channel hopping sequence + BC symbol correlation		**3-channel voting + packet length + packet interval + power threshold**	
BLE Compatible Frequency Hopping	No	No	No	Yes	Yes	**Yes**	
RF LO Clock	N/A[1]	N/A[1]	LC osc.	Ring osc.	LC osc.	**Ring osc. + freq. tripler**	
Frequency Locking	N/A[1]	N/A[1]	No	FLL	No	**PLL**	
Integrated Digital Baseband	Yes	Yes	Yes	No	Yes	**Yes**	
Adjacent Channel SIR @ 2 MHz @ 10 MHz	N.R.[2]	N.R.[2]	N.R.[2]	-4 dB -20 dB	-10 dB[3] -28 dB[3]	**-6 dB**[4] **-23 dB**[4]	**-60 dB**[5,6] **-60 dB**[5,6]
Power Consumption	236 nW	164 μW[7]	230 μW	150 μW[7]	1200 μW[7]	**220 μW**[7]	
Wake-Up Latency	Multi-adv. events $\sim$2 s	1 adv. packet $\sim$100 μs	1 adv. packet $\sim$200 μs	1 adv. event 1.47 ms[5]	1 adv. event 1.47 ms[5]	**1 adv. packet $\sim$200 μs**[4]	**1 adv. event 1.47 ms**[5]
Sensitivity	-56.5 dBm @ MDR=10^{-3}	-58 dBm @ MDR=10^{-2}	-80 dBm @ BER=10^{-3}	-57.5 dBm @ BER=10^{-3}	-82.2 dBm @ BER=10^{-3}	**-85 dBm @ MDR=10^{-3}**	
False Alarms Per Hour @ Sensitivity	N.R.[2]	$<$6/hr	$<$2/hr[8]	N.R.[2]	N.R.[2]	**$<$2/hr**	
Normalized Sensitivity[9]	-53.5 dB	-98 dB	-117 dB	-85.8 dB	-110.5 dB	**-122 dB**[4]	**-113.3 dB**[5]
FoM	89.3 dB	105.9 dB	123.4 dB	94.1 dB	109.7 dB	**128.6 dB**[4]	**119.9 dB**[5]

[1] Not applicable.
[2] Not reported.
[3] < -32 dB across band when frequency hopping is enabled.
[4] Single channel operation w/o frequency hopping mode enabled.
[5] 3-channel operation w/ frequency hopping mode enabled; BLE advertising event UUID=0x180D is used here for example.
[6] Under the condition of 1 advertising packet being jammed.
[7] Crystal reference power is not included.
[8] Under the setting for a 166 kbps bit rate with a 38-bit correlation threshold, which yields a sensitivity of -82 dBm @ MDR=10^{-2}.
[9] $P_{\mathrm{SEN,norm}}(\mathrm{dB}) = P_{\mathrm{SEN}} - 10\log\frac{1}{Latency}$.

Chapter 5

A Dual-Mode Wi-Fi/BLE Wake-Up Receiver

5.1 Introduction

As discussed in Chapter 4, a pragmatic and immediately deployable WuRX should feature sensitivity and interference resiliency as good as the main radio, while consuming low power with or without duty-cycling, while being compatible the main radio it needs to work with. Since Wi-Fi and BLE are the two most popular radio standards for IoT, wearable, and smart home devices, a receiver that is compatible with both can potentially enable a wide range of new energy-constrained applications at low cost.

This chapter demonstrates a WuRX that is compatible with both Wi-Fi and BLE radios. The developed dual-mode wake-up receiver achieves $-92/-90.3$ dBm sensitivity with a latency-configurable power consumption of 4.4-352μW, all while supporting multi-channel frequency diversity through a combination of a carefully architected frequency plan that supports BLE advertisement channel hopping or a proposed subcarrier-based within-channel Wi-Fi frequency hopping, a carefully crafted frequency down-conversion plan that enables low power receiver architecture, and an on-chip image rejection filter for full on-chip integration. The proposed design was originally presented in [22]; this chapter provides significant additional wake-up signature and receiver architecture analysis, circuit implementation details, as well as additional measurement results. The proposed dual-mode frequency plan and enhanced 4-D wake-up signature is presented in Section 5.2, while Section 5.3 describes the overall WuRX architecture.

Section 5.4 presents circuit implementation details, followed by measurement results in Section 5.5. Finally, Section 5.6 concludes this chapter.

5.2 Wi-Fi / BLE Standard Compatible Wake-Up Signature

5.2.1 Overview of Prior-art Wi-Fi/BLE Standard Compatible Wake-up Signatures

Wi-Fi and BLE both operate in the 2.4 GHz ISM band, which is a highly congested band with many devices operating simultaneously. Thus, good interference resiliency is a must when operating in this band. In part because of the need for high-linearity and careful filtering, and in part due to the complex and high data rate modulation schemes utilized in Wi-Fi and BLE, it is difficult for conventional receiver designs to operate at low (e.g., sub-mW) power levels while achieving good sensitivity. For example, Wi-Fi and BLE use modulation schemes like 256-QAM OFDM or frequency-hopped GFSK, which require complex demodulators with low phase noise local oscillators (LOs), filters, and/or digital signal processors. When coupled with high-linearity front-ends and high data rates, achievement of low-power, especially at good sensitivity levels, is exceedingly difficult.

Since most low-power radios tend to utilize simple, low-complexity modulation schemes like on-off keying (OOK) or binary frequency shift keying (BFSK) [6], a potentially effectual way to reduce the power demands of a Wi-Fi or BLE-compatible WuRX is to make the otherwise complex modulation scheme look like a lower complexity scheme at a lower data rate. This concept, called back-channel communication, has enable many excellent low-power, yet standards-compatible receivers [9, 14–19, 21, 22].

Wi-Fi Compatible Back-channel Wake-up Signatures

As depicted in Fig. 5.1(a), baseline Wi-Fi starting with IEEE 802.11g and onward communicates in one of three primary channels: 1, 6, and 11, located at 2412, 2437, 2462 MHz, respectively. Each channel occupies 20 MHz of bandwidth during baseline operation. Within each channel, 52 OFDM subcarriers are enabled, and modulation ranging from BPSK to 256-QAM is embedded on each sub-carrier with a 4 μs symbol duration. To make this OFDM waveform appear to be lower complexity, prior work has suggested a multi-subcarrier OOK (MC-OOK) approach, where the middle 13 OFDM subcarriers (occupying $\sim$4 MHz of signal bandwidth) are turned on and off within a single 20 MHz Wi-Fi channel (within the standards-imposed peak-to-average power ratios) for OOK symbols 1 and symbol 0, respectively [16, 19, 21]. This method effectively reduces the receiving signal bandwidth and demodulation complexity, to the point where energy-detection architectures can be employed; this enables a low power wake-up receiver architecture. However, due to single-channel operation without frequency diversity, the achievable interference resilience relies solely on the linearity and filtering inside the wake-up receiver itself, which may not be sufficient for truly robust operation at low power levels.

BLE Compatible Back-channel Wake-up Signatures

As also depicted in Fig. 5.1(a), BLE operates across 40 channels, with three of them (Ch. 37, 38, and 39 located at 2402, 2426, and 2480 MHz, respectively) dedicated for advertising events to establish node-to-node initial handshaking. The modulation for each channel is nominally Gaussian frequency-shift keying (GFSK) at a 1 Mbps data rate. A single advertising event consists of three consecutively transmitted packets at each of the three advertising channels. A single advertising event takes less than 20 ms, and a single advertising packet length is between 128$\sim$376 μs.

Since the transmission of advertisement packets is required by the standard, and since the properties of the advertisement packets are well defined, most prior-art BLE-

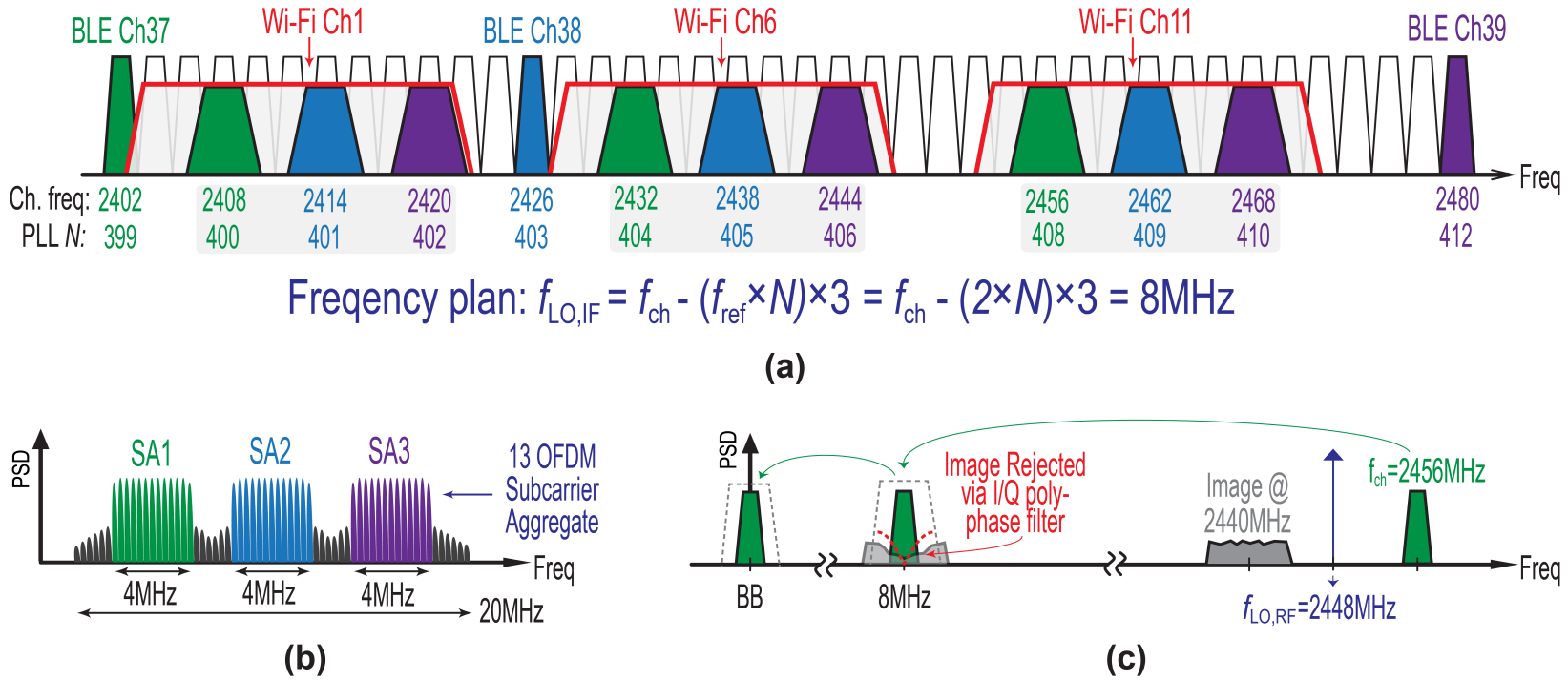


Figure 5.1: (a) proposed frequency plan for BLE/Wi-Fi dual-mode operation; (b) proposed dynamic subcarrier aggregation for Wi-Fi mode; and (c) complete down-conversion flow using OFDM SA1 at Wi-Fi Ch. 11 as an example.

compatible WuRX perform OOK-like energy detection to detect the presence of either multiple advertising events [9], the RSSI and duration of a single channel packet [15], or the frequency hopping sequence [17, 18]. In particular, the work in [18] proposed a 4-dimensional wake-up signature that looked at the RSSI, the packet duration, the inter-packet interval, and the frequency hopping pattern to improve coding diversity and interference resilience.

5.2.2 Proposed Dual-mode compatible Frequency Plan and Enhanced 4-D Wake-Up Signature

Although Wi-Fi and BLE operate with completely different modulation formats, it is possible to architect a back-channel modulation scheme that can use a similar frequency plan to enable reuse of underlying hardware. The overall plan is depicted in Fig. 5.1(a). For BLE, the plan follows the same approach as in [18], where each of the three advertisement channels are down converted in a time-sequenced manner to an 8 MHz IF via an LO generated by a 2 MHz-reference integer-N PLL followed by a frequency tripler. As abovementioned, the frequency-hopped nature of this approach imparts excellent interference resiliency for reception of BLE wake-up events in typical congested environments.

For Wi-Fi reception, one possibility is to use the same 4 MHz-wide MC-OOK signals as in prior-work, so long as the selected sub-carriers are centered at a frequency compatible with the integer-N arithmetic of PLL used in the BLE mode. However, if a BLE (or any other type of) interferer is present nearby, the resulting Wi-Fi-compatible WuRX will not have any frequency diversity, and thus the interference performance will be limited by the linearity and/or on-chip filter sharpness.

To include frequency diversity in a manner that is compatible with the integer-N-based BLE plan, this work proposes a dynamic subcarrier aggregation technique, shown in Fig. 5.1(b), which treats a group of 13 OFDM subcarriers as a subcarrier-aggregate (SA), and this aggregate of 13 subcarriers hops between three different frequency loca-

tions within a single 20 MHz Wi-Fi channel. By carefully selecting the center frequency of each dynamic SA, which may not be the same relative subcarrier locations amongst all three Wi-Fi channels, the integer-N-based BLE frequency plan can be directly re-used for three Wi-Fi channels (1, 6, and 11) simply by using different values of N as indicated in Fig. 5.1(a). This enables dual-mode operation with the same underlying WuRX hardware, all while supporting frequency diversity. The proposed dynamic SA-based back-channel modulation scheme can be enabled with commodity Wi-Fi hardware with a simple firmware modification. Note, however, that since the spacing between SA center frequencies is smaller in a single Wi-Fi channel than the spacing between BLE advertisement channels, the benefits of frequency diversity of the Wi-Fi mode is less than the benefits derived in BLE mode. This will be seen in the corresponding measurements results section.

Fig. 5.1(c) depicts the down-conversion flow using SA1 at Wi-Fi Ch. 11 as an example. Here, SA1, which is located at 2456 MHz, is down converted to an 8 MHz IF by an LO at 2448 MHz, generated from a 2 MHz reference multiplied by $N = 408$ and then again by the frequency tripler. Unlike [18], which required off-chip image rejection filtering, in this case an IQ LO is generated, and the image is rejected fully on-chip via a passive IQ mixer followed by a polyphase filter, which will be described in more detail in the following section.

To further improve the interference resiliency for potential jammers which may occur in between BLE packets or dynamic SA transmissions, an enhanced 4-dimensional wake-up detection scheme is proposed compared to [18]. Since the evaluation period of the incoming packet in [18] covers the entire packet interval to ensure no missed packets, an in-band blocker that occurs before the desired packet might incorrectly trigger the digital finite-state machine, as depicted in Fig. 5.2(a). To solve this issue, this work proposes a packet interval gating logic technique that gates the digital baseband input to prevent blockers, which may show up right in the middle of the packet interval, from potentially initiating an erroneous state transition. Moreover, this gating window, W_{L}, is programmable based on the desired wake-up signature, as depicted in Fig. 5.2(b).

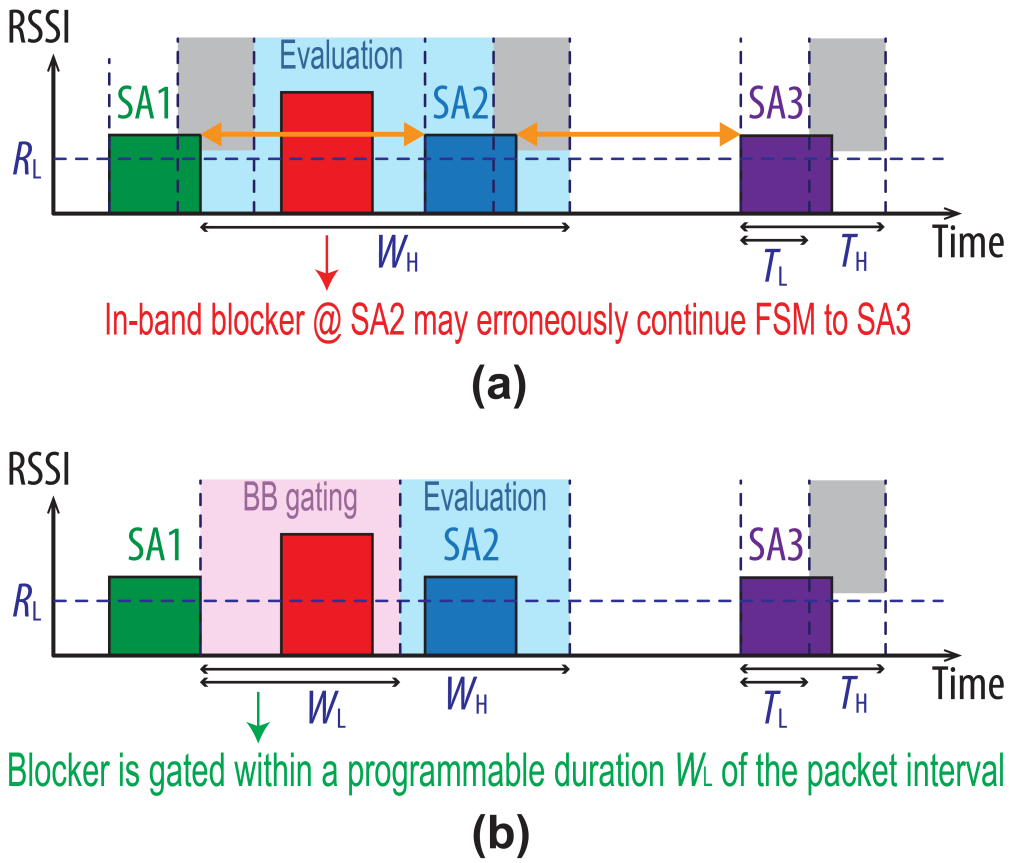


Figure 5.2: 4-dimensional wake-up signature: (a) with evaluation period of the incoming packet covers the entire packet interval; and (b) with proposed packet interval gating period for in-band blocker rejection enhancement.

5.3 Wake-Up Receiver Architecture

5.3.1 Overview of WuRX Architectures

Direct Energy Detection Architecture

The simplest possible back-channel-based modulation encodes information via the presence, or lack thereof, of packets (BLE) or subcarrier aggregates (Wi-Fi). Ignoring frequency hopping, the simplest possible receiver architecture is thus a simple direct energy-detector, as shown in Fig. 5.3(a). Here, an envelop detector (ED) is used to directly down-convert RF signals to baseband (BB) via a non-linear squaring function. Depending on sensitivity and power needs, an optional low noise amplifier (LNA) can be

included. If the LNA is not included, it is possible for this approach to reach the nW-to-μW level for general WuRX applications [8–13]. However, wideband energy detection with limited pre-ED RF filtering implies limited channel selectivity, which causes any nearby interferers to also demodulate to baseband. Moreover, since the ED's conversion gain depends on the square of its input voltage, the output signal-to-noise ratio is typically poor without sufficient pre-ED RF gain [32]. Thus, good sensitivity can only be achieved by burning power to increase pre-ED RF gain via one or more LNAs, or by shrinking baseband bandwidth to values well below what is possible by back-channel standards-compliant signaling. For example, some of the nW-level WuRXs achieve sensitivities better than -80 dBm sensitivity, but do so with a very narrow baseband bandwidths (e.g., 1-100 Hz). In contrast, energy detection of the longest possible BLE advertisement packet requires 376 μs, or a baseband bandwidth greater than $\sim$3 kHz, with much higher bandwidth required for Wi-Fi, even with back-channel approaches. This increased noise bandwidth limits the sensitivities of such direct energy detecting architectures in prior work to -56.5 dBm at 236 nW [9] and -58 dBm at 164 μW [15] for BLE, and -42.5 dBm at 2.8 μW [14] for Wi-Fi.

Mixer-based Zero-IF Architecture

The two major downsides of the direct-ED approach relate to the lack of filtering at RF, which limits channel selectivity and interference resiliency, and the lack of pre-ED gain, which can only occur at power-expensive RF frequencies in this approach. To simultaneously address both of these issues, a mixer can be used to translate incident RF energy to a lower frequency, where it is both easy and power efficient to filter and amplify the signal prior to energy detection. This, however, requires the generation of an LO, which must be accomplished through a phase-locked loop (PLL) or a frequency-locked loop (FLL). Either way, the power of LO generation tends to dominate the power consumption of such approaches, placing them in a distinctly higher category than direct-ED-based approaches. Nevertheless, it is a necessary trade-off to

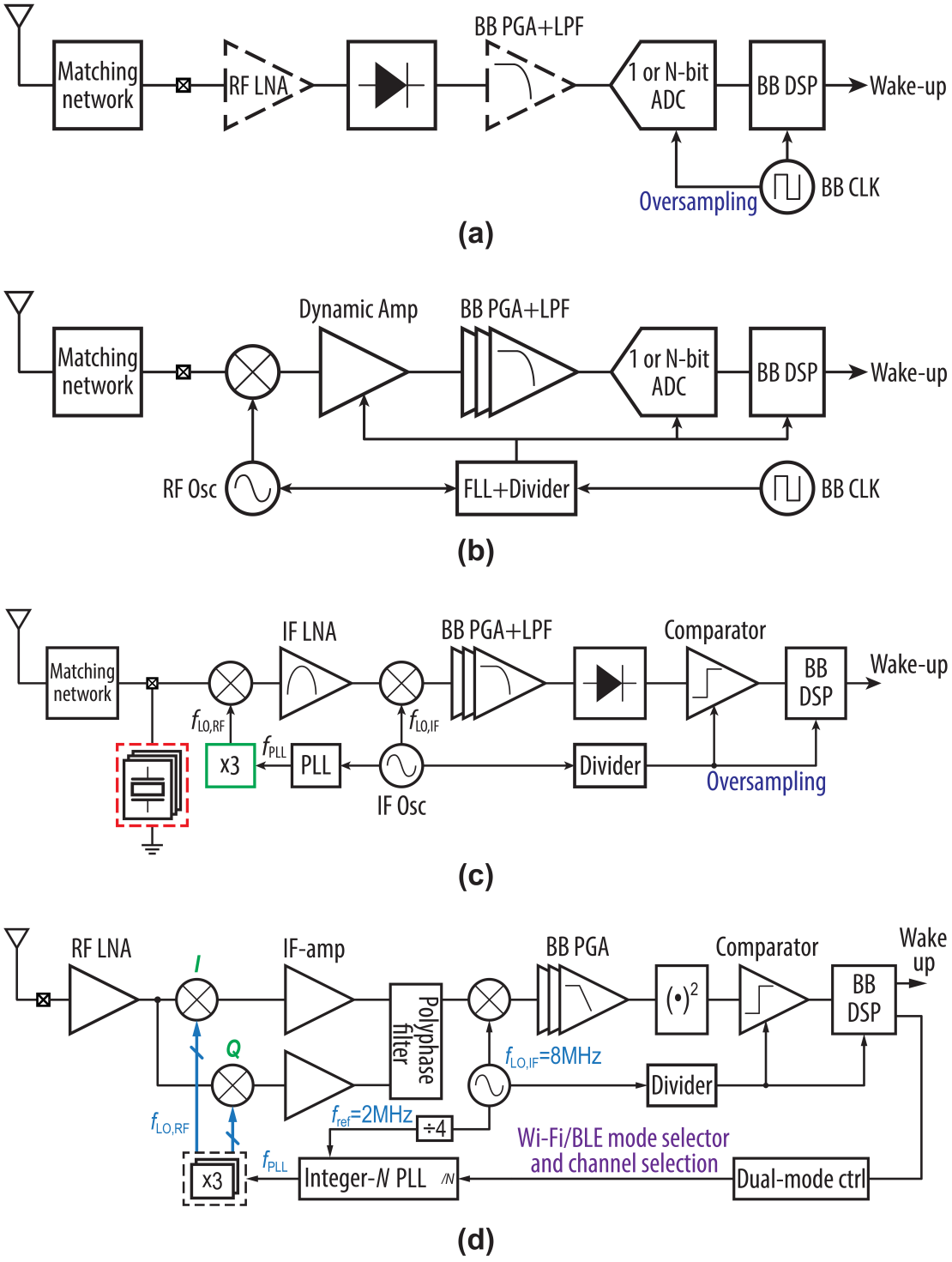


Figure 5.3: Sub-mW standard-compatible WuRX architectures: (a) direct envelope detection architecture; (b) mixer-first zero-IF architecture; (c) mixer-first heterodyne architecture; and (d) proposed mixer-based zero 2^{nd}-IF heterodyne architecture with dual-mode control.

achieve the requisite selectivity, interference robustness, and sensitivity specifications at standards-compatible back-channel bandwidths.

Most prior-art Wi-Fi-compatible WuRXs utilize a mixer-first zero-IF architecture, as shown in Fig. 5.3(b) [16, 19, 21]. In this approach, the front-end RF LNA is removed to save power. Instead, the incident RF signal is, after an on-chip matching network, fed to a passive mixer, which down-converts the signal to baseband for filtering and amplification. To achieve high sensitivity, low passive mixer switch resistance is required, which inevitably increases switch size and therefore passive mixer driver power. This further increases the LO generation and driving power requirement, especially given the 2.4 GHz frequency this occurs at.

Although this architecture does consume more power than a direct-ED approach, such receivers can still achieve sub-mW power and high sensitivity, with performance generally being better in a more scaled CMOS process where dynamic switching power is low. For example in [16], a sensitivity of -72 dBm is achieved for 173 μW of power in 14 nm FinFET technology for Wi-Fi. However, since the signal bandwidth is purposely reduced for a wake-up receiver, the sensitivity of this zero-IF approach is then limited by the post-mixer stage $1/f$ noise [16]. In [19], a dynamic amplifier with low $1/f$ noise is proposed to address this issue, which enables a design that achieves a sensitivity of -92.4 dBm under 340 μW of power in 28 nm, again for Wi-Fi.

Since the phase noise of the RF LO only needs to be around -80 dBc/Hz to not degrade the achievable sensitivity [63], ring oscillator-based LOs are typically employed, as they consume less power than an equivalent LC VCO. In addition, frequency synthesis can be accomplished via an FLL instead of a PLL to save power. Interestingly, however, phase noise still limits the signal-to-interference ratio (SIR) because of reciprocal mixing. Thus, further SIR improvements can be achieved by employing an LC oscillator as a trade-off with power. For example, in [21] a sensitivity of -92.6 dBm with 16.6 dB better SIR compared to [19] is achieved under 495 μW of power in 28 nm for Wi-Fi. While this approach may work well for Wi-Fi back-channel communication, which has a larger signal bandwidth, careful re-design would be required when

translating to lower bandwidths required by BLE to combat not only the more relatively important $1/f$ noise, but also possible FLL frequency fluctuation, in order to properly demodulate the wake-up signal without sensitivity degradation.

Mixer-based IF Heterodyne Architecture

To deal with $1/f$ noise issues that will come into play due to lower BLE bandwidths, a mixer-first heterodyne architecture can be adopted, which adds amplification at an IF away from the $1/f$ noise corner frequency [18]. This approach is shown in Fig. 5.3c). The design in [18], achieves a sensitivity of -85 dBm for 220 μW of power in 65 nm in part by operating the RF LO at one-third of the signal frequency (with a frequency multiplier) and using a 0.5 V supply voltage. Moreover, a PLL instead of a FLL is adopted, which guarantees the frequency stability for low bandwidth signal demodulation. It also achieves interference-resiliency without the use of an LC oscillator when operating under the proposed 3-channel frequency-hopping voting mode. However, without IQ RF LO signals, this prior-art requires a custom off-chip single-die 3-channel FBAR filter for image rejection. Although this off-chip image rejection approach is suitable for BLE applications which requires a single FBAR die only, it can not be operated under Wi-Fi mode without the use of multiple multi-channel FBAR die. For this reason, a new approach is needed to support dual-mode Wi-Fi/BLE operation.

5.3.2 Proposed Mixer-Based Zero 2^{nd} IF WuRX Architecture

The proposed WuRX employs a mixer-based zero 2^{nd}-IF heterodyne architecture, and is shown in Fig. 5.3(d). Before the 1^{st} down-conversion, a matching network and current-reuse LNA provides 18 dB of RF gain, which provides sensitivity improvement over prior-art mixer-first architecture that have only $\sim$9 dB of passive voltage gain [18]. This comes at the cost of an additional 75 μW of power. After amplification, I/Q passive mixers are used to down-convert to the first IF at 8 MHz, where IF

amplifiers can power-efficiently amplify the signal. A passive poly-phase filter can then be employed for image rejection without the need of an off-chip image rejection filter. After the second down conversion, a programmable-gain baseband amplifier with a built-in low-pass filter further provides signal amplification and further rejects both noise and interferers to increase the envelope detector output SNR. The envelope detector then provides a squaring function for energy detection purposes. The envelope detector's output is then oversampled and digitized by the comparator, which serves as a 1-bit analog-to-digital converter (ADC). The digital baseband finally determines the wake-up and, along with the BLE/Wi-Fi dual-mode control logic, controls the channel selection for the RF front-end.

The IF LO is generated by an off-chip 8 MHz crystal reference and serves as a global clock. The RF PLL is locked to the IF LO, and then is fed to a frequency-tripler to generate the RF LO. Circuit details of all of these blocks are discussed in detail in the next section.

5.4 Circuit Implementation

5.4.1 RF LO Generation

Based on the proposed frequency plan shown in Fig. 5.1, the LO is generated via an integer-N PLL. A standard type-II PLL is adopted, as shown in Fig. 5.4(a), where the BLE channel or Wi-Fi SA is selected by changing the divider ratio, which is controlled by a dual-mode control logic based on a finite-state machine.

Since the receiver is performing non-coherent energy detection, good phase noise is not required for proper demodulation (though reasonably good phase noise is required to minimize reciprocal mixing issues), and thus a ring-oscillator can be employed as the VCO. As depicted in Fig. 5.4(a), an $\sim$800 MHz ring VCO is employed to save power, while the 2.4 GHz band LOs are generated via an AND-based frequency-tripling edge combiner, which is the same strategy adopted in [18]. Unlike [18], however, I/Q

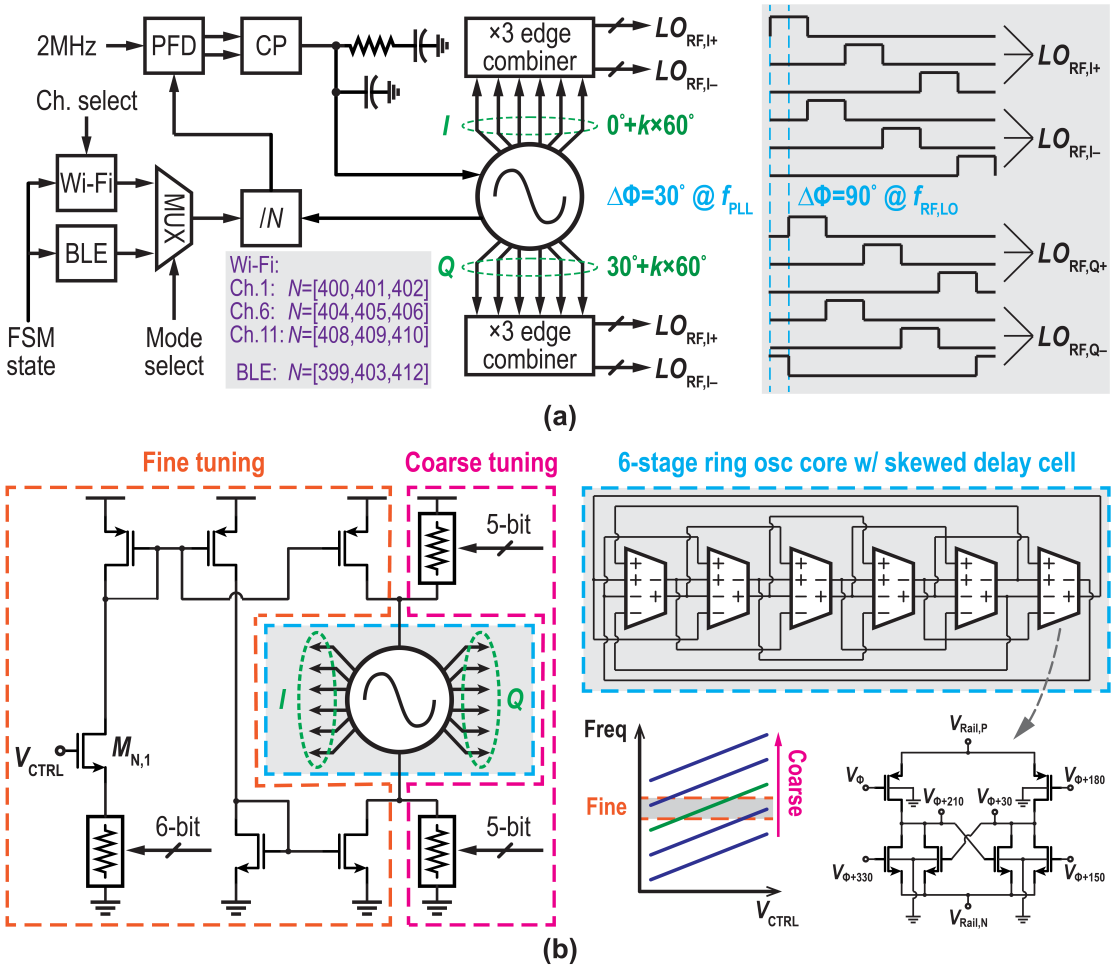


Figure 5.4: Schematic of: (a) PLL with dual mode control logic and proposed IQ generation; (b) 6-stage 12-phase ring VCO with skewed delay cell and fine/course frequency tuning.

RF LO signals are generated here to enable the on-chip image rejection filter. To generate these I/Q LOs, two sets of 6-phase clocks with 30° separation are required, which, after the frequency tripler, can result in the desired I/Q RF LO signals at 2.4 GHz with 90° phase separation, as depicted in Fig. 5.4(a).

To generate the required two sets of 6-phase clocks (i.e., 12 LO phases), one possibility is to design a 12-stage single-ended ring oscillator. However, this is challenging to do at 800 MHz at 0.5 V (selected for low power reasons) in the employed 65 nm process. Instead, a differential 6-stage ring oscillator with skewed delay cells is adopted, where the skew delay cells can effectively boost the achievable oscillating frequency

under the 0.5 V supply [67]. The VCO and the delay cells are shown in Fig. 5.4(b). Here, the PMOS bodies in the skewed delay cells are grounded to improve conductance, thereby reducing transistor size and thus CV^2 power. Since the supply voltage is only 0.5 V, there are no issues with substrate diodes turning on. To ensure PLL stability, both coarse and fine tuning paths are used to control the K_{VCO} to be 320 kHz/mV in this design while still maintaining a large frequency tuning range to overcome PVT [18].

The PLL settling time is $\sim$13.7 μs based on simulations, which is sufficient for the minimum 345 μs packet interval based on the BLE signal generation software available in most commercially available phones.

5.4.2 RF/Analog Signal Chain

The overall RF/analog signal chain is depicted in Fig. 5.5. First, in order to effectively increase the wake-up receiver sensitivity compared to [18], a high gain LNA is employed before the passive mixer. This comes with a cost of 75 μW in (measured) power overhead. The employed LNA achieves a simulated gain of 18 dB and a noise figure of 4 dB by using feedback capacitor C_{F} instead of a resistive feedback component to realize the input matching [68], all while using a current-reuse architecture and moderate-inversion biasing to increase gain efficiency under same current consumption.

After the LNA, the signal is then fed to the RF passive mixer. As part of the tripler and on-chip image rejection circuit, each I/Q RF LO drives a 2-phase 6-switch passive mixer, which downconverts the signal to the 8 MHz IF. The I/Q IF signals are then amplified separately, fed to a polyphase filter, and then summed to achieve image rejection.

The IF mixer then downconverts the IF signal to baseband. After this second down-conversion, in a similar manner to [18], a 3-stage PGA/LPF provides gain in 3 dB steps as part of the power threshold setting to condition and filter the down-converted signal. Additionally, a DC-offset cancellation loop is implemented to prevent the 3-stage PGA being saturated by any DC-offset caused by mismatch, which avoids the use

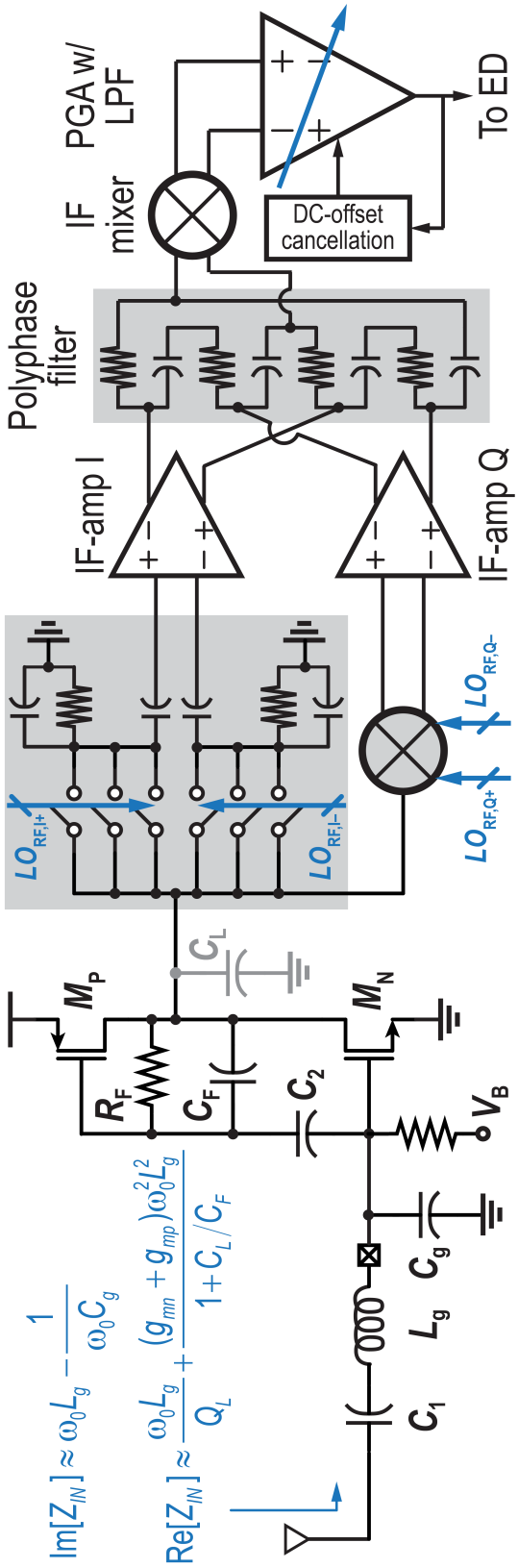


Figure 5.5: Schematic of the wake-up receiver signal chain.

of large AC-coupling caps between each stage of the PGA. At high PGA gain settings, the WuRX sensitivity is limited by this pre-ED linear amplification portion of the signal chain, which has a noise figure of 16 dB based on simulations.

5.4.3 Digital Baseband

Fig. 5.6 shows the block diagram of the on-chip digital baseband, where an edge detector first compares the input signal with a delayed version to extract the rising and falling edge timing of the packet (BLE) or dynamic SA (Wi-Fi), which are used to compute the packet/SA length. The measured packet/SA length is then compared to a pre-defined window, $T_{\mathrm{L}} \sim T_{\mathrm{H}}$, to generate a 2-bit control for the channel selection finite state machine (FSM) and the wake-up voting FSM. The 2-bit state output of the channel selection FSM controls the RF front-end to the desired channel/SA center frequency, while providing the current sequencing order for the other blocks. Finally, the wake-up voting FSM generates the wake-up signal after 3-channel scanning and comparison with a pre-defined voting threshold.

A packet interval computation is enabled after the first packet/SA is received and causes an FSM state change. If the packet interval is larger than an upper bound duration, W_{H}, and still no new packet is received, the FSMs rotate back to the initial

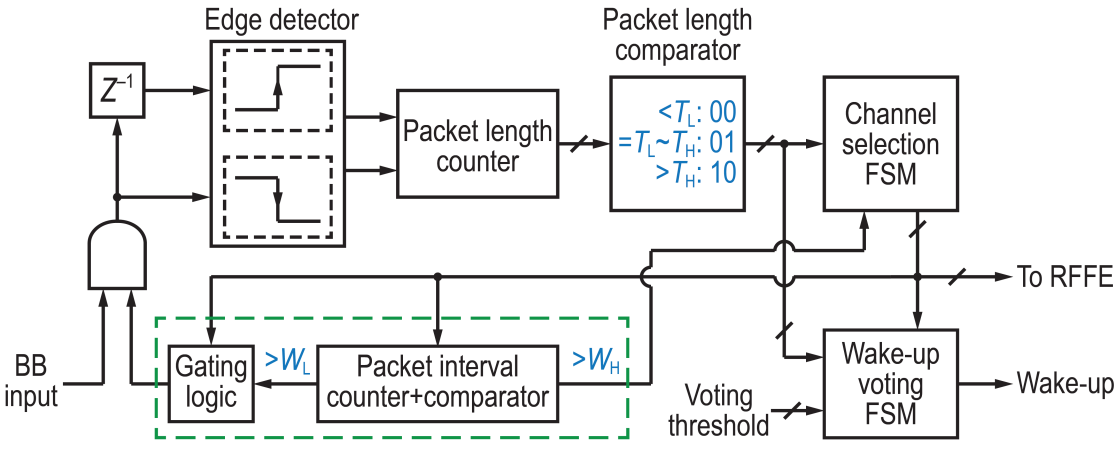


Figure 5.6: Block diagram of the digital baseband.

stage. Unlike [18], where the entire between-packet interval is evaluated, here an additional packet interval gating logic is implemented to gate out the digital baseband for a programmable window, W_{L}, to prevent blockers that may occur right in the middle of the packet interval from potentially initiating an erroneous state transition, as discussed in Section 5.2.

5.5 Measurement Results

The proposed dual-mode BLE/Wi-Fi wake-up receiver is fabricated in a 65 nm process, occupying 0.6 mm^2 of core area. A die photo is shown in Fig. 5.7.

Fig. 5.8(a) shows the measured $|S_{11}|$, which demonstrates that the proposed wake-up receiver is well-matched across the 2.4 GHz ISM band. As shown in Fig. 5.8(b), the wake-up receiver achieves a sensitivity of -92/-90.3 dBm for BLE/Wi-Fi modes, as measured by a missed detection rate of 10^{-3} under a false-alarm rate of $<$1/hr.

To verify the proposed wake-up receiver performance with interference under

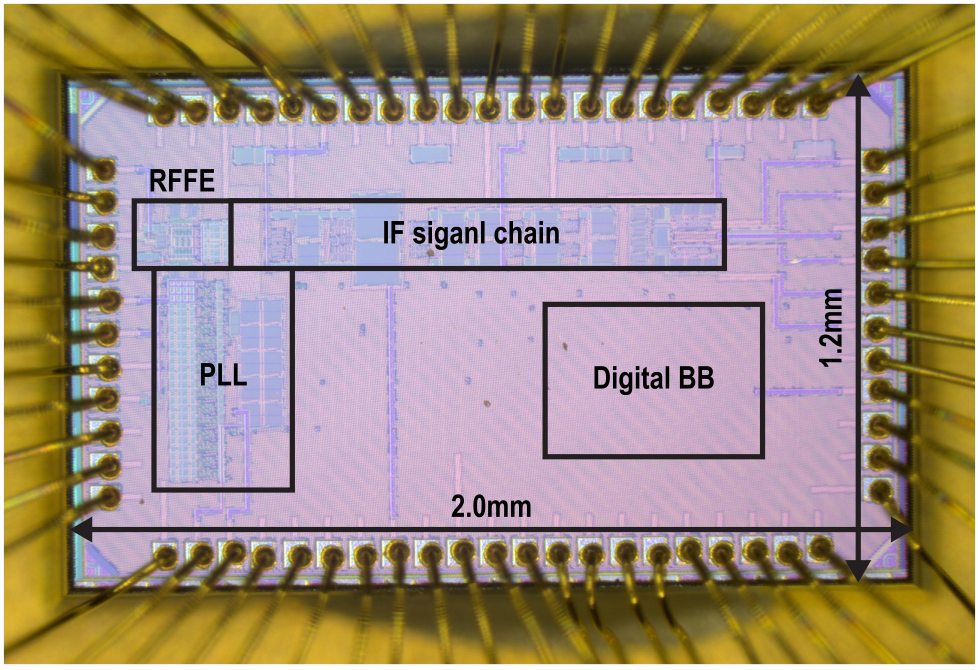


Figure 5.7: Micrograph of the wake-up receiver die.

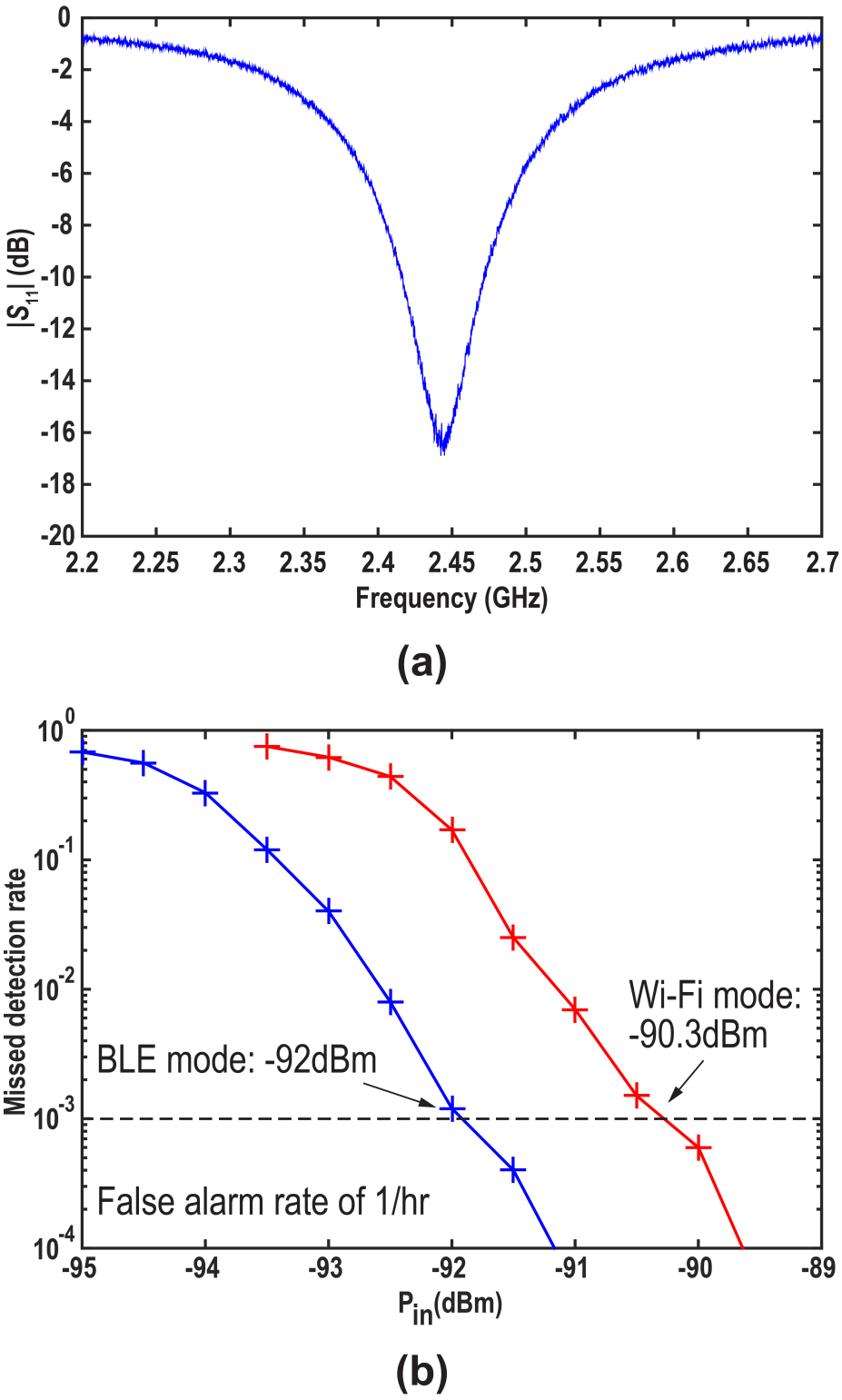
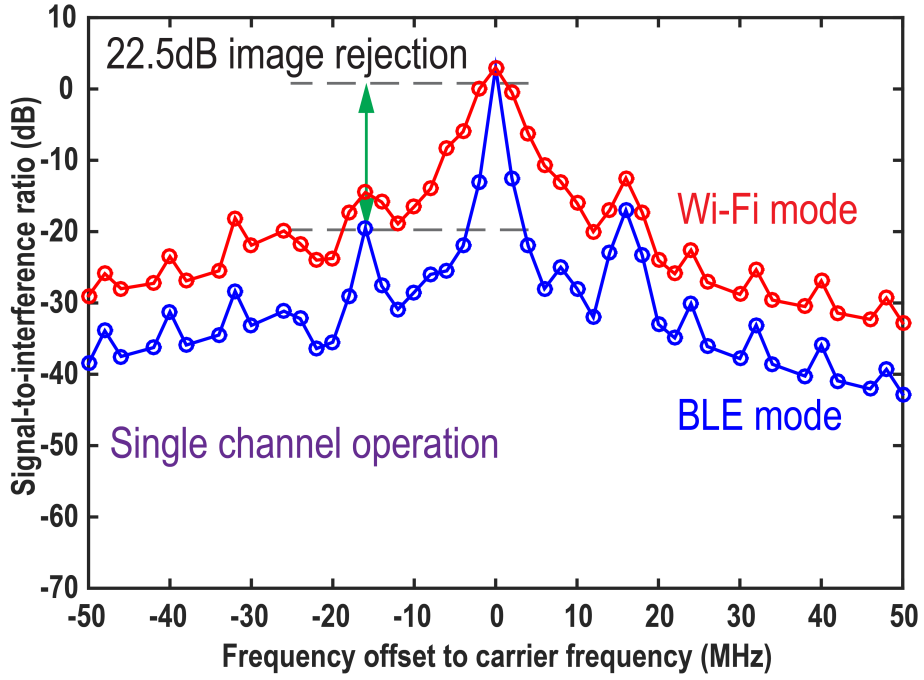
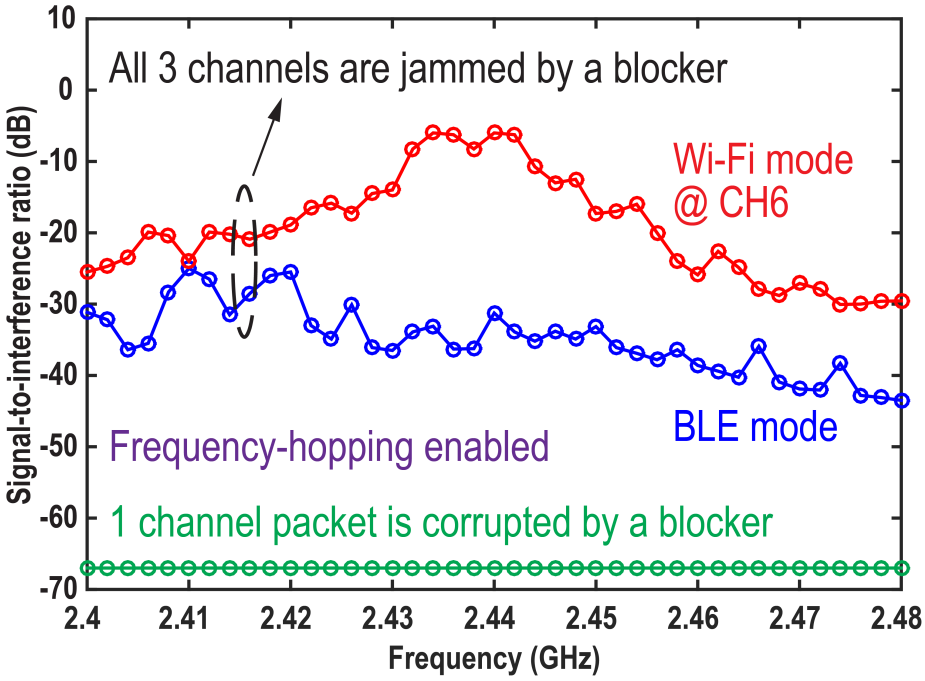


Figure 5.8: Measurement results of: (a) $|S_{11}|$; (b) missed detection rate waterfall curve.



(a)



(b)

Figure 5.9: Measurement results of signal-to-interference ratio: (a) without frequency hopping enabled; (b) with frequency hopping enabled.

practical operation, BLE-modulated jammers are used for signal-to-interference ratio (SIR) measurements. When the wake-up receiver is operating under a single-channel mode without the frequency-hopping voting scheme enabled, the on-chip image rejection and heterodyne structure enables a SIR of -28.5/-21.7 dB at a 10/24 MHz offsets, together with an image rejection of 22.5/17.5 dB for BLE/Wi-Fi modes. These measurements are shown in Fig. 5.9(a). When the frequency-hopping voting scheme is enabled, up to -67 dB SIR (limited by test equipment) is achieved for a normal short-burst jammer that corrupts one of the packets/SAs. This is shown by the green curve in 5.9(b). Moreover, for the extreme and much more rare case where a blocker exists throughout 3-channel operation at just the right time intervals, the SIR is limited by the 2nd most susceptible channel, as shown by the blue and red curves in 5.9(b) for BLE and Wi-Fi modes, respectively. It is also shown that under this extreme case, BLE mode has better SIR across band compared to Wi-Fi mode because of the larger frequency hopping channels separation. However, this is an exceptionally rare case and is unlikely to occur in practice except for intentionally nefarious jammers.

Fig. 5.10 shows measured wireless transient waveforms of the wake-up receiver operating in a realistic lab environment to demonstrate the effectiveness of the proposed wake-up signature processing algorithms. For the first experiment, shown in Fig. 5.10(a), the on-chip digital baseband of the proposed wake-up receiver is programmed to a voting threshold of three (i.e., all three signatures - packets in BLE or SAs in Wi-Fi - must be collected in order to trigger a wake-up event) in order to demonstrate the voting algorithm in the most aggressive false-alarm-avoidance setting. The first transmitted waveform has the expected three signatures with appropriate lengths and at appropriate inter-signature-intervals, and thus a wake-up event is generated. The second transmission in Fig. 5.10(a) utilizes a shorter inter-signature-interval than the receiver is programmed for. Thanks to the proposed input gating logic, most of the second signature's energy is not counted, which means it does not trigger the FSM to move to the next frequency, and thus instead the FSM reverts back to searching at the first frequency without a false alarm. The third transmission in Fig. 5.10(a) uses a longer

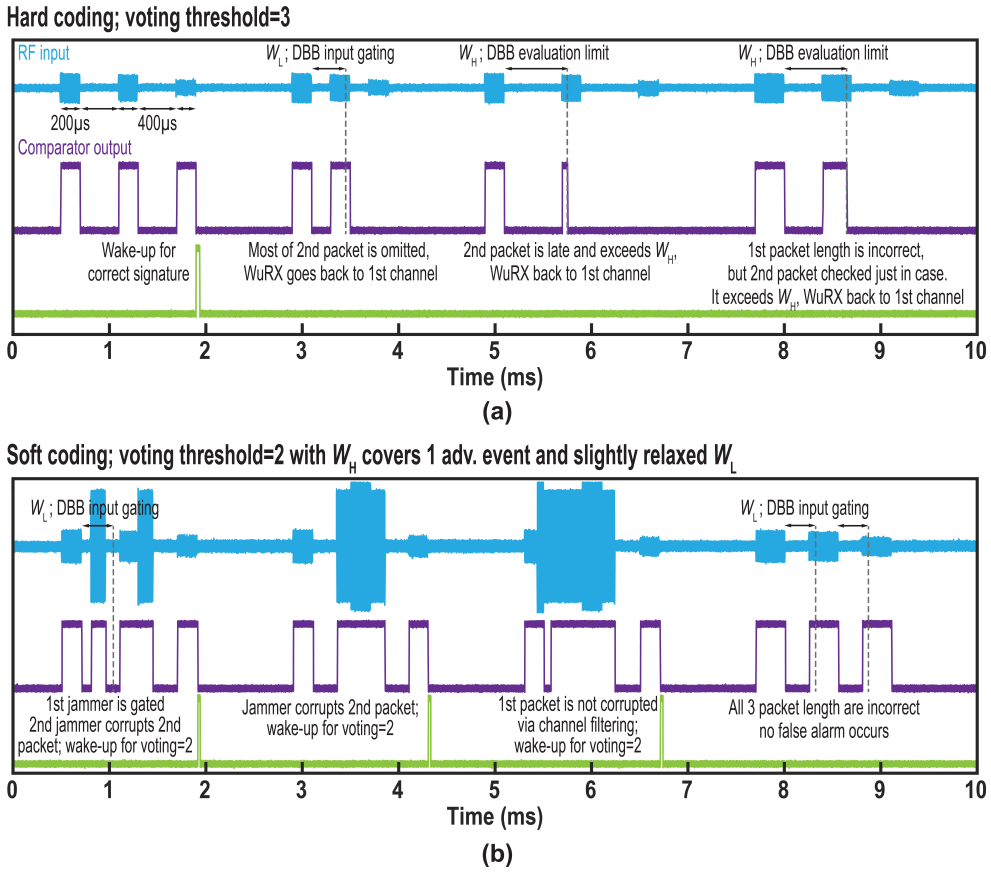


Figure 5.10: Measured transient waveforms under wireless operation in a realistic lab setting for: (a) different signatures under hard coding; (b) interferers under soft coding.

inter-signature-interval. Here, since the second packet comes in late and exceeds the packet evaluation limit, W_{H}, the wake-up receiver also goes back to the first frequency and no false alarms occur. Finally, the fourth transmission in Fig. 5.10(a) uses a slightly longer signature length. Here, the receiver detects something at frequency 1, and although the signature length is incorrect, the wake-up receiver will still move to the second frequency to scan just in case the first signature was correct, but corrupted by jammers. However, since the second signature length in this example is also incorrect, no false alarms are generated.

For the second experiment, shown in Fig. 5.10(b), interfering Wi-Fi/BLE sources are placed right next to the receive antenna, and the on-chip digital baseband of the proposed wake-up receiver is programmed with a voting threshold of two to demonstrate

Table 5.1: Power Breakdown of Proposed wake-up receiver

LNA	IF AMP	IF PGA	Comparator	Digital baseband	RF LO generation
76.5 μW	36.9 μW	21.7 μW	2.2 μW	3.8 μW	211.2 μW

that the proposed wake-up receiver is interference-resilient while still be able to trigger correct wake-ups. In the first transmission, two in-band jammer packets are received simultaneously with the correct three signatures. Fortunately, the first jammer packet occurs within the digital baseband gating window, and thus it will not affect the wake-up signature processing algorithm. Although the second jammer packet occurs within the second wake-up signature period and therefore corrupts it, the first and third signatures are received correctly, and thus a correct wake-up event is triggered thanks to the majority voting algorithm. Similarly, in the second transmission a large and long jammer completely blocks the second signature; however, thanks to the majority voting algorithm, a correct wake-up event is generated. For the third transmission, where a longer jammer occurs across two wake-up signature periods, the built-in multi-stage filtering of the wake-up receiver makes it such that only the second signature is corrupted, and thus a correct wake-up event is still triggered. Finally, the fourth transmission again shows that a wrong wake-up signature, in this case with longer signature durations, will still not cause any false alarms under this majority voting setting because of the packet length counter.

Table 5.1 shows the power breakdown of the wake-up receiver. During continuous operation, the wake-up receiver consumes 352 μW, for a wake-up latency of 1.47 ms. Since 60% of the consumed power is in the LO generation, it is expected that the active mode power of this design can be significantly reduced by scaling to a smaller CMOS technology node. Importantly, however, by duty-cycling the wake-up receiver via a power-gating transistor, power can be traded-off for wake-up latency, which is desirable in many emerging applications; measurements as low as 4.4 μW have been achieved for a wake-up latency of 1 s.

Table 5.2: Performance Comparison of State-of-the-Art Mixer-Based Standard-Compatible WuRXs

	[16] JSSC'18	[17] JSSC'19		[18] ISSCC'19	[19] VLSI'19	[21] JSSC'20	**This Work**	
Wireless Standard	Wi-Fi	BLE		BLE	Wi-Fi	Wi-Fi	**Wi-Fi + BLE**	
Technology	14 nm	65 nm	45 nm	65 nm	28 nm	28 nm	**65 nm**	
Area	0.19 mm^2	1.1 mm^2	1 mm^2	1.3 mm^2	0.1 mm^2	0.18 mm^2	**0.6 mm^2**	
Supply Voltage	0.95 V	1.1 / 0.9 V	1.0 / 0.9 V	0.5 V	0.9 / 0.6 V	0.9 / 0.6 V	**0.5 V**	
Wake-Up Signature	Multi-subcarrier OOK	Frequency-hopped advertising channels		4-D signature with freq.-hopped advertising channels	Multi-subcarrier OOK	Multi-subcarrier OOK	**Wi-Fi Enhanced 4-D signature with freq.-hopped subcarrier aggregation**	**BLE Enhanced 4-D signature with freq.-hopped advertising channels**
RF LO Clock	Ring osc.	Ring osc.	*LC* osc.	Ring osc. + freq. tripler	Ring osc.	*LC* osc.	**Ring osc. + freq. tripler**	
LO Stabilization	XO + FLL	XO + FLL	None	XO + PLL	XO + FLL	XO + FLL	**XO + PLL**	
On-Chip Digital BB	Yes	No	Yes	Yes	Yes	Yes	**Yes**	
SIR	−20 dB @ 25 MHz	−4 / −11 dB @ 2 / 3 MHz	−10 / −15 dB[1] @ 2 / 3 MHz	−6 / −23 dB^2 @ 2 / 10 MHz −60 $dB^{3,4}$ across band	−32.4 dB @ 25 MHz	−49 dB @ 25 MHz	**Wi-Fi −21.7 dB^2 @ 24 MHz −67 $dB^{3,4}$ across band**	**BLE −12.5 dB^2 @ 2 MHz −67 $dB^{3,4}$ across band**
Total Power	173 μW	150 μW	1200 μW	220 μW	340 μW	495 μW	**4.4 μW^5 / 352 μW^6**	
Wake-Up Latency and/or Bit Rate	62.5 kbps	1 ms / 112.5 kbps	1 ms / 250 kbps	200 μs^2 or 1.47 ms^3	62.5 / 250 kbps	62.5 kbps	**1 $s^{3,5}$ or 1.47 $ms^{3,6}$**	
Wake-up operation	Data bits	Data bits	Data bits	Wake-up only	Data bits	Data bits	**Wake-up only**	
Sensitivity	−72 dBm @ BER=10^{-3}	−57.5 dBm @ BER=10^{-3}	−82.2 dBm @ BER=10^{-3}	−85 dBm @ MDR=10^{-3}	−92.4 dBm @ PER=10^{-1}	−92.6 dBm @ PER=10^{-1}	**Wi-Fi −90.3 dBm @ MDR=10^{-3}**	**BLE −92 dBm @ MDR=10^{-3}**
False Alarms Rate @ Sensitivity	N.R.[7]	N.R.[7]	N.R.[7]	<2/hr	N.R.[7]	N.R.[7]	**<1/hr**	

[1] $<$ −32 dB across band when frequency hopping is enabled.
[2] Single channel operation w/o frequency hopping mode enabled.
[3] 3-channel operation w/ frequency hopping mode enabled.
[4] Under the condition of 1 packet being jammed.
[5] WuRX in duty-cycle mode with 1.25% duty-cycle ratio.
[6] WuRX in always-on mode.
[7] Not reported.

Table 5.2 show that the proposed wake-up receiver achieves state-of-the-art sensitivity and SIR amongst BLE wake-up receivers, and comparable sensitivity and continuous mode power to state-of-the-art Wi-Fi wake-up receivers, yet with improved SIR thanks to frequency hopping. In addition, it is the only dual-mode standards-compatible wake-up receiver.

5.6 Conclusions

This chapter presented a fully-integrated dual-mode BLE/Wi-Fi wake-up receiver that achieved $-92/-90.3$ dBm sensitivity at low, latency-configurable power consumption (4.4-352μW) by: 1) exploiting frequency hopping, either via within-channel OFDM dynamic subcarrier aggregation (Wi-Fi) or via advertisement channels (BLE) to achieve interference resiliency; 2) carefully planning the location of OFDM subcarrier aggregates (SAs) or BLE advertisement channels with integer-N arithmetic to enable a low-power IF down-conversion plan for both standards via an integer-N PLL; 3) employing a 6-stage 12-phase skew-delayed ring oscillator that generates IQ LOs at low power, while also enabling image rejection without an off-chip filter; 4) implementing a moderate-inversion current re-use LNA to improve sensitivity with a small power overhead; and 5) modifying the 4D wake-up logic with packet interval gating to improve interference resiliency. Since the power consumption of the proposed design was dominated by the highly digital RF LO generation, implementation in an advanced process node can potentially further lower the power. Even at the current power level, especially with duty-cycling enabled, the power of the presented wake-up receiver was measured to be significantly lower than conventional main radios, and yet the wake-up receiver could achieve similar sensitivity and interference resiliency as baseline Wi-Fi/BLE radios. As a result, the presented design could potentially help enable new wireless IoT applications, particularly those that have low average throughput requirements.

This chapter is based on and mostly a reprint of the following publications: P.-H. P. Wang and P. P. Mercier, "A 4.4μW $-92/-90.3$dBm Sensitivity Dual-Mode BLE/Wi-

Fi Wake-up Receiver," *IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, Jun. 2020, pp. 1-2, and P.-H. P. Wang and P. P. Mercier, "A Dual-Mode Wi-Fi/BLE Wake-Up Receiver," *IEEE Journal of Solid-State Circuits*, Under Review. The dissertation author is the primary author of these materials, and co-authors have approved the use of the material for this dissertation.

Chapter 6

Conclusion

6.1 Thesis Summary

In this thesis, WuRX designs targeting ultra-low-power and high sensitivity for different usage scenarios have been investigated. To achieve these goals, circuit-level, architecture-level, and communication-protocol-level techniques have been proposed, which are summarized in the following.

Chapter 2 presents the design of a WuRX that both improves sensitivity and reduces power over prior art through a multi-faceted design featuring an impedance transformation network with a large passive voltage gain, an active envelope detector with high input impedance to facilitate large passive voltage gain, a low-power precision comparator, and a low-leakage digital baseband correlator. Implemented in a 180 nm SOI CMOS process using DTMOS devices, the OOK-modulated WuRX operates at 113.5 MHz and achieves a sensitivity of -69 dBm, while consuming just 4.5 nW from a 0.4 V supply.

Chapter 3 presents an active and a passive ED designs with pseudo-balun characteristics, both of which enable WuRX operation at 400 MHz while improving sensitivity compared to their single-ended counterparts. Moreover, the proposed pseudo-balun structures can eliminate extra voltage reference requirement for the subsequent comparator. Both implemented in a 180 nm CMOS process, the WuRX employing the active ED can achieve a sensitivity of -63.8 dBm with a wake-up latency of 53.3 ms and consume only 4.5 nW, while the design employing the passive ED can achieve a sensitivity of -73.3 dBm with a wake-up latency of 180 ms and consume only 6.1 nW.

Chapter 4 presents a BLE compatible WuRX that simultaneously achieves low power, high sensitivity, and interference-resiliency. Interference resilience is achieved by detecting a 4-dimensional wake-up signature based on the hopping pattern from BLE-compliant advertising events, while low-power and high-sensitivity are achieved by filtering each advertising channel via a single-die 3-channel FBAR filter, and down-converting packet energy via a designed integer-N frequency plan. Implemented in 65 nm CMOS, the proposed WuRX achieves a sensitivity of -85 dBm and a SIR of -60 dB, while consuming 220 μW from a 0.5 V supply.

Chapter 5 presents a dual-mode WuRX compatible with both BLE and Wi-Fi transmitters. The proposed WuRX achieves state-of-the-art power (as low as 4.4 μW through a latency-power duty-cycled trade-off), sensitivity (as low as -92 dBm), and interference resilience (SIR=-67 dB) via a carefully architected frequency plan that supports BLE advertisement channel hopping or a proposed subcarrier-based within-channel Wi-Fi frequency hopping scheme, a carefully crafted frequency down conversion plan that enables low power receiver architecture via integer-N arithmetic, and an on-chip image rejection filter for full on-chip integration. The proposed design is implemented in a 65-nm CMOS process and operates from a 0.5-V supply.

6.2 Future Directions

As a result, the presented WuRXs could help reduce power consumption and extend system lifetime for IoT devices, particularly those that have low-to-medium average throughput requirements. On top of that, opportunities for further enhancement can also be explored. For instance, LPWAN WuRXs presented in Chapter 2 and Chapter 3 target to be used with the always-on WuRX communication protocol, and therefore adopt the direct envelope detection architecture for near-zero power consumption, which inevitably limits the interference-resiliency and channelization. To enhance interference-resiliency, prior work has proposed a 2-tone envelope detection scheme, which modulates the data onto two separate carrier tones located within the WuRX front-end band-

width with a predefined frequency offset [69]. After the squaring function from ED, the target signal is then located at IF, which not only can be easily filtered in low power manners, but also can prevent coincidence with blockers that are down-converted to DC after ED. This technique can actually be further extended to achieve channelization if an additional IF PLL and tunable IF filter are employed. For this to work, this 2-tone envelope detection scheme would require custom transmitters and new communication protocols, which might provide a great opportunity for emerging LPWAN standards. On the other hand, BLE/Wi-Fi standard-compatible WuRXs presented in Chapter 4 and Chapter 5 target superb interference-resiliency in order to work within the congested 2.4 GHz ISM band, and therefore adopt the mixer-based architecture, which inevitably requires higher power consumption. Fortunately, since the power consumption of the proposed designs were dominated by the highly digital RF LO generation, advanced process nodes can be leveraged to achieve even lower power.

On a broader subject, for wireless sensor nodes, other than reducing the average power required for node-to-node network establishment or spectrum sensing, reducing the peak power required for transmission is also of interest, as most of IoT devices powered by miniature batteries or energy harvesters could not provide sufficient peak power for conventional transmitters. Instead of building an active modulator and transmitter, backscatter communication, where an incident wave to an antenna sees a time-varying impedance profile that creates a modulated reflected signal, can be an effective solution to reduce the peak power requirement [70]. Moreover, recent research has demonstrated a backscatter integrated circuit that can communicate directly with commodity Wi-Fi transceivers with 10s of meters of communication range [14, 71]. All of these technological progress could potentially help enable new classes of power and area constraint wireless IoT applications, and lead us to a true wireless world.

Appendix A

Noise and Sensitivity Analysis for Direct Envelope Detection Based Receiver Architecture

A.1 Theoretical Sensitivity Analysis

Envelope detectors are non-linear elements. Unlike linear mixers used for down-conversion, the squaring operation of EDs converts pre-ED noise down to baseband via two mechanisms: self-mixing of noise, and noise convolved with the input signal. If an ED can be modeled as a squaring operation as $y = k_{\mathrm{ED}} \cdot x^2$, where k_{ED} is the ED scaling factor with 1/V in unit, then the sensitivity of a direct ED system can be given by [32]:

$$P_{\mathrm{SEN}} = \underbrace{\frac{20\sqrt{\overline{v_{\mathrm{n,eq}}^2} SNR_{\mathrm{min}}}}{k_{\mathrm{ED}} A_{\mathrm{V}}^2}}_{1} + \underbrace{4k_{\mathrm{B}} T SNR_{\mathrm{min}} BW_{\mathrm{BB}} F_{\mathrm{FE}}}_{2} + \underbrace{2k_{\mathrm{B}} T F_{\mathrm{FE}} \sqrt{4BW_{\mathrm{BB}}^2 SNR_{\mathrm{min}}^2 + BW_{\mathrm{RF}} BW_{\mathrm{BB}} SNR_{\mathrm{min}}}}_{2}, \tag{A.1}$$

where $\sqrt{\overline{v_{\mathrm{n,eq}}^2}}$ is the total integrated baseband noise (e.g., ED and comparator noise referred to the output of the ED), SNR_{min} is the minimum SNR required for demodulation (e.g., 11 dB for OOK at a BER of 10^{-3} using optimal matched filter [72]), A_{V} is the voltage gain before the ED, BW_{BB} is the baseband bandwidth, BW_{RF} is the RF (or IF in a mixer-based architecture) bandwidth, F_{FE} is the noise factor of all RF and/or IF

components, k_{B} is Boltzmann's constant, and T is temperature.

Part 1 of this expression is the baseband noise, while part 2 is the RF (and/or IF) pre-ED noise that is eventually mixed to baseband via the ED. If the WuRX has sufficient gain at RF/IF such that the baseband noise is small relative to RF/IF noise (i.e., part 1 is negligible), and if RF/IF bandwidth is large, then sensitivity is dominated by self-mixing noise and is given by:

$$P_{\mathrm{SEN,N^2}} = 2k_{\mathrm{B}}T \cdot F_{\mathrm{FE}}\sqrt{BW_{\mathrm{RF}}BW_{\mathrm{BB}}SNR_{\mathrm{min}}}. \tag{A.2}$$

If, on the other hand, gain is large and BW_{RF} is small, then sensitivity is dominated by convolution noise and is given by:

$$P_{\mathrm{SEN,SN}} = 8k_{\mathrm{B}}T \cdot F_{\mathrm{FE}}BW_{\mathrm{BB}}SNR_{\mathrm{min}}. \tag{A.3}$$

The discerning frequency between these two cases is given by:

$$BW_{\mathrm{COR}} = 16BW_{\mathrm{BB}}SNR_{\mathrm{min}}, \tag{A.4}$$

as illustrated in Fig. A.1(a) for OOK modulation at various data rates, assuming 0 dB noise figure of all RF/IF blocks. It is thus important for ED systems with large pre-ED gain to limit RF (or IF) bandwidth prior to envelope detection not only for interference purposes, but also for noise purposes.

However, the above analysis assumes baseband noise is negligible, which is generally not true for receivers with limited pre-ED gain. Unfortunately, achieving high gain at RF requires undesirably large power (e.g., $\sim$100 μW at 2.4 GHz and $\sim$1 μW at 100 MHz for 15 dB gain in 0.18 μm CMOS). While achieving gain at IF is much more energy-efficient, it requires an LO and mixer, which also requires more power than desired in ultra-low-power WuRX applications. Thus, most ultra-low-power WuRXs often forgo active gain before the ED, and thus sensitivity will be predominantly limited by baseband noise, as illustrated in Fig. A.1(b). Since sensitivity is inversely related to

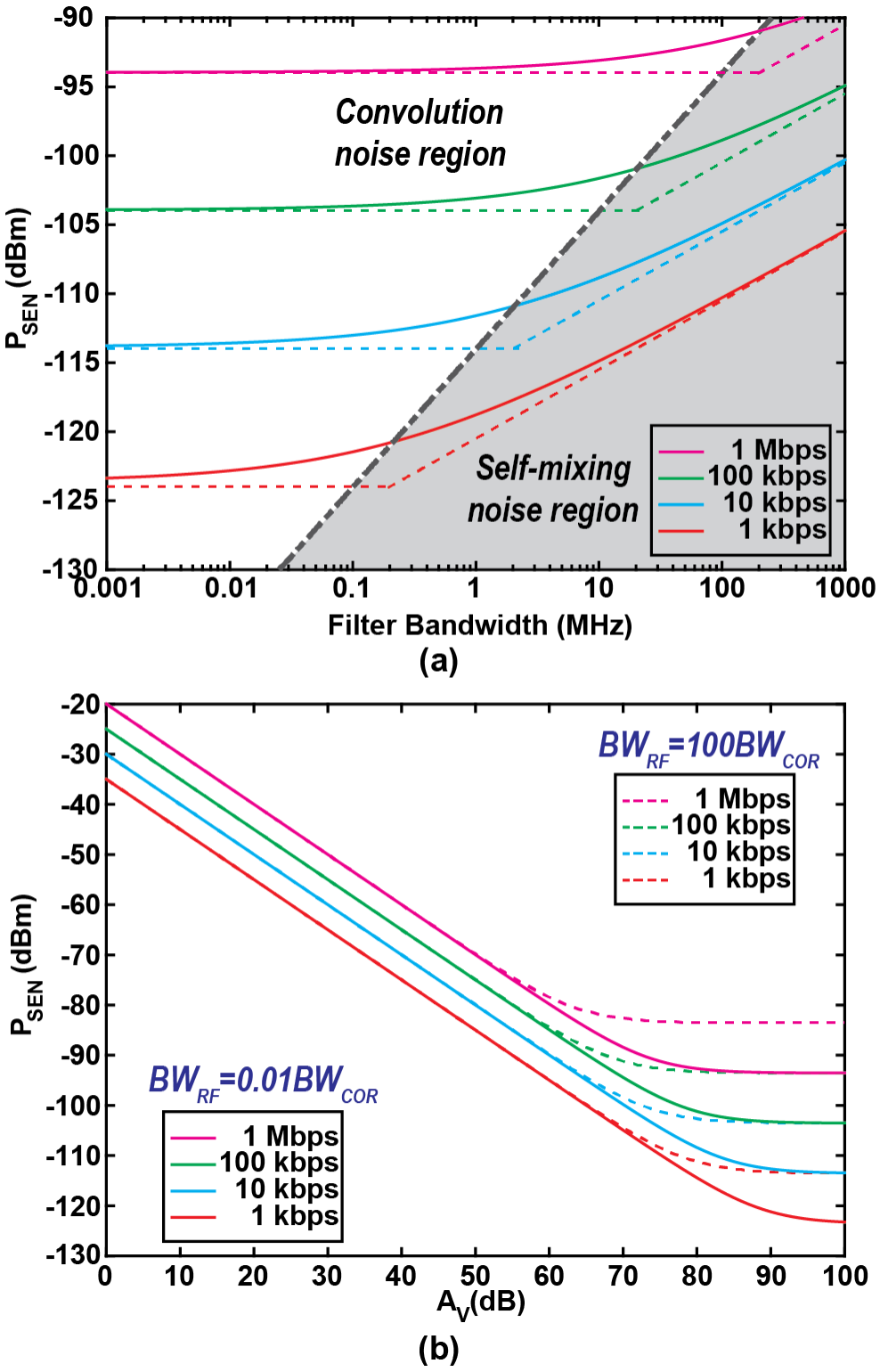
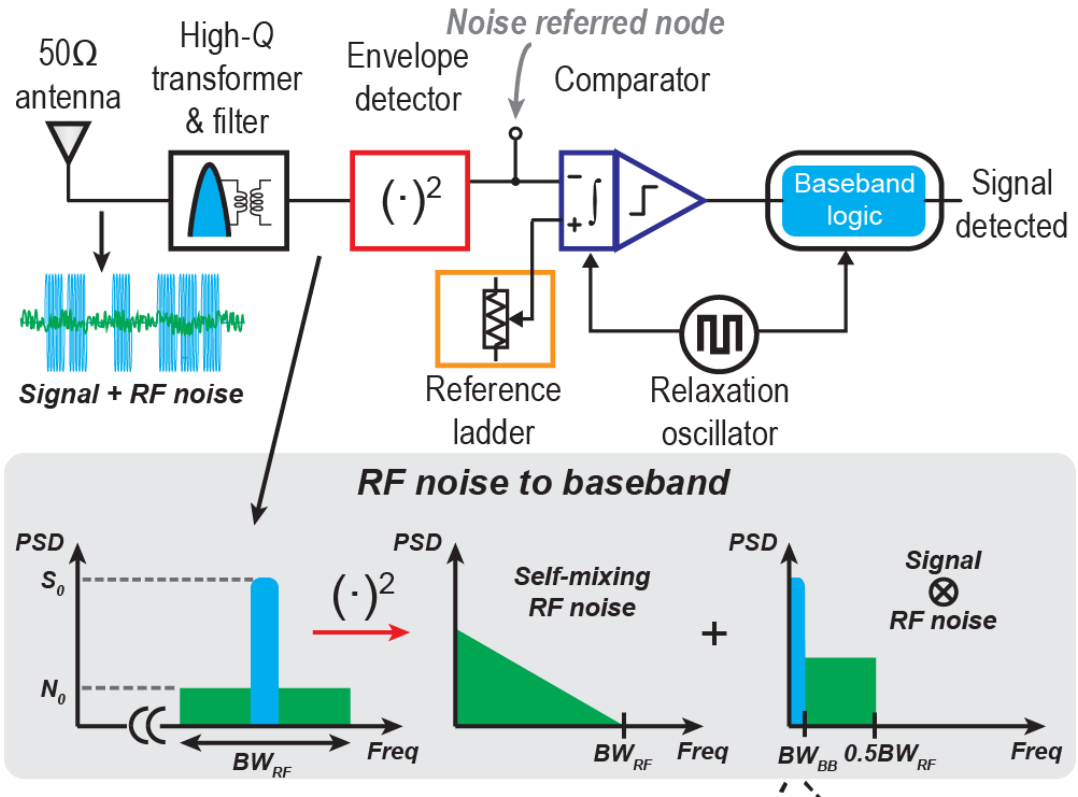


Figure A.1: (a) Sensitivity vs. frond-end filter bandwidth (assuming BB noise negligible); (b) sensitivity vs. front-end gain (assuming BB noise dominates).

the square of the RF/IF voltage gain, most ultra-low-power direct ED WuRXs strive to achieve as much passive voltage gain in the matching network as possible.

A.2 Theory Verification via Measurement

In this section, we revisit the sensitivity equation for direct envelope detection architectures, shown in eq. (A.1), and combine it with noise of each circuit blocks from measurement of the design in Chapter 2 to verify the sensitivity results. Because of the 300 Hz baseband bandwidth, the noise measurement for ED and reference ladder is done using Keysight 35670A dynamic signal analyzer, which is particularly designed for frequency of interest from DC-102.4 kHz, while the noise for comparator is measured using method described in Section V. Fig. A.2 shows the summary of the noise performance from each source, including total integrated noise voltage referred at ED output node, sensitivity limitation, and noise spectrum. Since the baseband circuit noise is dominant, the value for the negligible RF noise, i.e. self-mixing noise and convolution noise, is computed directly using eq. (A.2) and eq. (A.3) with BW_{RF} =1.9 MHz and F_{FE} =1 because of all passive pre-ED circuits. Moreover, the minimum SNR required for our proposed WuRX to achieve BER = 10^{-3} is ∼15.82 dB, which is computed using the Marcum Q-function from BER = $Q_{\mathrm{M}}(0.5\sqrt{SNR_{\mathrm{min}}})$ for OOK modulation. Since the sensitivity from eq. (A.1) is defined for BER = 10^{-3}, all the sensitivity limitation shown here are subtracted by 4 dB to take coding gain into account, and another 2.5 dB in terms of average power. For all the power setting, the estimated sensitivities are only ∼1.5 dB off than the measurement results, which indicates that the proposed WuRX design matches with theory well.



WuRX parameter

Power consumption	4.5 nW	9.5 nW	66.4 nW
Passive voltage gain	25 dB	24.4 dB	21.4 dB
ED scaling factor k_{ED}	180.8	728.0	2840
Measured sensitivity	-69.0 dBm	-71.5 dBm	-73.5 dBm

Measured integrated noise voltage and sensitivity limitation

Noise source	Integrated noise voltage @ ED output (μV)			Sensitivity limitation of each noise source (dBm)		
Signal ⊗ RF noise	N/A			-126.7		
Self-mixing RF noise	N/A			-122.1		
ED noise	151.6	339.4	417.5	-71.3	-73.3	-75.3
Comparator noise	95			-73.4	-78.8	-81.7
Ref. ladder noise	67			-74.9	-80.3	-83.2
Estimated total noise	191.0	358.8	433.4	-70.3	-73.0	-75.1

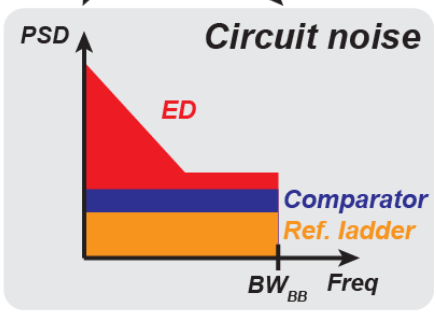


Figure A.2: Noise performance summary of each noise source.

References

[1] "New gsma study: Operators must look beyond connectivity to increase share of $1.1 trillion iot revenue opportunity," GSM Association, London, England, UK, May 2018. [Online]. Available: https://www.gsma.com/newsroom/press-release/new-gsma-study-operators-must-look-beyond-connectivity-to-increase-share

[2] "Powering the iot revolution," Libelium, Zaragoza, Spain, Jul. 2017. [Online]. Available: http://libelium.com/downloads/training/webinar_iot_management_07_11_2017.pdf

[3] X. Wang, P.-H. P. Wang, Y. Cao, and P. P. Mercier, "A 0.6V 75nW all-CMOS temperature sensor with 1.67m°C/mV supply sensitivity," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 9, pp. 2274–2283, Sep. 2017.

[4] H. Wang and P. P. Mercier, "Near-zero-power temperature sensing via tunneling currents through complementary metal-oxide-semiconductor transistors," *Scientific Reports*, vol. 7, no. 4427, Jun. 2017.

[5] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, New Jersey, USA: Prentice Hall Press, 2011.

[6] P. P. Mercier and A. P. Chandrakasan, *Ultra-Low-Power Short-Range Radios*. New York, NY, USA: Springer International, 2015.

[7] E.-Y. Lin, J. Rabaey, and A. Wolisz, "Power-efficient rendezvous schemes for dense wireless sensor networks," in *Proc. IEEE Int. Conf. Communications*, vol. 7, Jun. 2004, pp. 3769–3776.

[8] P.-H. P. Wang, H. Jiang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, P. P. Mercier, and D. A. Hall, "A near-zero-power wake-up receiver achieving -69-dBm sensitivity," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1640–1652, Jun. 2018.

[9] N. E. Roberts, K. Craig, A. Shrivastava, S. N. Wooters, Y. Shakhsheer, B. H. Calhoun, and D. D. Wentzloff, "A 236 nW -56.5 dBm sensitivity bluetooth low-energy wakeup receiver with energy harvesting in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2016, pp. 450–451.

[10] P.-H. P. Wang, H. Jiang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, P. P. Mercier, and D. A. Hall, "A 400 MHz 4.5 nW -63.8 dBm sensitivity wake-up receiver employing an active pseudo-balun envelope detector," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 35–38.

[11] J. Moody, P. Bassirian, A. Roy, N. Li, S. Pancrazio, N. S. Barker, B. H. Calhoun, and S. M. Bowers, "Interference robust detector-first near-zero power wake-up receiver," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2149–2162, Aug. 2019.

[12] P.-H. P. Wang, H. Jiang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, P. P. Mercier, and D. A. Hall, "A 6.1-nW wake-up receiver achieving -80.5-dBm sensitivity via a passive pseudo-balun envelope detector," *IEEE Solid-State Circuits Letters*, vol. 1, no. 5, pp. 134–137, May 2018.

[13] V. Mangal and P. R. Kinget, "A wake-up receiver with a multi-stage self-mixer and with enhanced sensitivity when using an interferer as local oscillator," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 808–820, Mar. 2019.

[14] P.-H. P. Wang, C. Zhang, H. Yang, D. Bharadia, and P. P. Mercier, "A 28μW IoT tag that can communicate with commodity WiFi transceivers via a single-side-band QPSK backscatter communication technique," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 312–314.

[15] M. Ding, P. Zhang, C. Lu, Y. Zhang, S. Traferro, G.-J. van Schaik, Y.-H. Liu, J. Huijts, C. Bachmann, G. Dolmans, and K. Philips, "A 2.4GHz BLE-compliant fully-integrated wakeup receiver for latency-critical IoT applications using a 2-dimensional wakeup pattern in 90nm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, May 2017, pp. 168–171.

[16] E. Alpman, A. Khairi, R. Dorrance, M. Park, V. S. Somayazulu, J. R. Foerster, A. Ravi, J. Paramesh, and S. Pellerano, "802.11g/n compliant fully integrated wake-up receiver with -72-dbm sensitivity in 14-nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1411–1422, May 2018.

[17] A. Alghaihab, Y. Shi, J. Breiholz, H. Kim, B. H. Calhoun, and D. D. Wentzloff, "Enhanced interference rejection Bluetooth Low-Energy back-channel receiver with LO frequency hopping," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 2019–2027, Jul. 2019.

[18] P.-H. P. Wang and P. P. Mercier, "A 220μW -85dBm sensitivity BLE-compliant wake-up receiver achieving -60dB SIR via single-die multi-channel FBAR-based filtering and a 4-dimentional wake-up signature," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 440–442.

[19] R. Dorrance, R. Liu, K. A. Beevi, D. Dasalukunte, M. A. S. Lopez, V. Kristem, S. Azizi, and B. Carlton, "An ultra-low power, fully integrated wake-up receiver and digital baseband with all-digital impairment correction and -92.4dbm sensitivity for 802.11ba," in *IEEE Symposium on VLSI Circuits*, Jun. 2019, pp. C80–C81.

[20] P.-H. P. Wang and P. P. Mercier, "An interference-resilient BLE-compatible wake-up receiver employing single-die multi-channel FBAR-based filtering and a 4-dimensional wake-up signature," *IEEE J. Solid-State Circuits*, In Press.

[21] R. Liu, A. Beevi K.T., R. Dorrance, D. Dasalukunte, V. Kristem, M. A. Santana Lopez, A. W. Min, S. Azizi, M. Park, and B. R. Carlton, "An 802.11ba-based wake-up radio receiver with Wi-Fi transceiver integration," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1151–1164, May 2020.

[22] P.-H. P. Wang and P. P. Mercier, "A 4.4μW $-92/-90.3$dbm sensitivity dual-mode BLE/Wi-Fi wake-up receiver," in *IEEE Symposium on VLSI Circuits*, 2020, pp. 1–2.

[23] T. Abe, T. Morie, K. Satou, D. Nomasaki, S. Nakamura, Y. Horiuchi, and K. Imamura, "An ultra-low-power 2-step wake-up receiver for IEEE 802.15.4g wireless sensor networks," in *IEEE Symp. VLSI Circuits Dig.*, Jun. 2014, pp. 1–2.

[24] J. Pandey, J. Shi, and B. Otis, "A 120 μW MICS/ISM-band FSK receiver with a 44 μW low-power mode based on injection-locking and 9x frequency multiplication," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 460–462.

[25] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 μW wake-up receiver with -72 dBm sensitivity using an uncertain-IF architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.

[26] C. Bryant and H. Sjőland, "A 2.45 GHz, 50 μW wake-up receiver frontend with -88 dBm sensitivity and 250 kbps data rate," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 235–238.

[27] C. Salazar, A. Cathelin, A. Kaiser, and J. Rabaey, "A 2.4 GHz interferer-resilient wake-up receiver using a dual-IF multi-stage N-path architecture," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2091–2105, Sep. 2016.

[28] S. Oh, N. E. Roberts, and D. D. Wentzloff, "A 116 nW multi-band wake-up receiver with 31-bit correlator and interference rejection," in *Proc. IEEE Custom Integrated Circuits Conf.*, Sep. 2013, pp. 1–4.

[29] N. E. Roberts and D. D. Wentzloff, "A 98 nW wake-up radio for wireless body area networks," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Jun. 2012, pp. 373–376.

[30] H. Jiang, P.-H. P. Wang, L. Gao, P. Sen, Y.-H. Kim, G. M. Rebeiz, D. A. Hall, and P. P. Mercier, "A 4.5nW wake-up radio with -69dBm sensitivity," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 416–417.

[31] P. M. Nadeau, A. Paidimarri, P. P. Mercier, and A. P. Chandrakasan, "Multi-channel 180pJ/bit 2.4GHz FBAR-based receiver," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Jun. 2012, pp. 381–384.

[32] X. Huang, G. Dolmans, H. de Groot, and J. R. Long, "Noise and sensitivity in RF envelope detection receivers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 10, pp. 637–641, Oct. 2013.

[33] K. Entesari and G. M. Rebeiz, "A differential, 4-bit, 6.5-10 GHz RF MEMS tunable filter," *IEEE Trans. on Microwave Theory and Techniques*, vol. 53, no. 3, pp. 1103–1110, Mar. 2005.

[34] "Square air core inductors 1515SQ 2222SQ 2929SQ," Coilcraft, Inc., Cary, IL, USA, Oct. 2015. [Online]. Available: http://www.coilcraft.com/pdfs/1515sq.pdf

[35] J.-S. Hong, *Microstrip Filters for RF/Microwave Applications*, 2nd ed. Hoboken, NJ, USA: Wiley, 2011.

[36] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, Oct. 2012.

[37] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI," *IEEE Trans. on Electron Devices*, vol. 44, no. 3, pp. 414–422, Mar. 1997.

[38] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, "A 1.1 nW energy-harvesting system with 544 pW quiescent power for next-generation implants," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2812–2824, Dec. 2014.

[39] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.

[40] P. P. Mercier and A. P. Chandrakasan, "A supply-rail-coupled eTextiles transceiver for body-area networks," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1284–1295, Jun. 2011.

[41] A. Wang and A. P. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[42] X. Huang, S. Rampu, X. Wang, G. Dolmans, and H. de Groot, "A 2.4 GHz/915 MHz 51 μW wake-up receiver with offset and noise suppression," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 222–224.

[43] J. Choi, K. Lee, S.-O. Yun, S.-G. Lee, and J. Ko, "An interference-aware 5.8GHz wake-up radio for ETCS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 446–447.

[44] K.-W. Cheng, X. Liu, and M. Je, "A 2.4/5.8 GHz 10 μW wake-up receiver with -65/-50 dBm sensitivity using direct active RF detection," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2012, pp. 337–340.

[45] S.-E. Chen, C.-L. Yang, and K.-W. Cheng, "A 4.5 μW 2.4 GHz wake-up receiver based on complementary current-reuse RF detector," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2015, pp. 1214–1217.

[46] X. Huang, P. Harpe, G. Dolmans, and H. de Groot, "A 915MHz ultra-low power wake-up receiver with scalable performance and power consumption," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2011, pp. 543–546.

[47] D.-Y. Yoon, C.-J. Jeong, J. Cartwright, H.-Y. Kang, S.-K. Han, N.-S. Kim, D.-S. Ha, and S.-G. Lee, "A new approach to low-power and low-latency wake-up receiver system for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2405–2419, Oct. 2012.

[48] S. Moazzeni, M. Sawan, and G. E. R. Cowan, "An ultra-low-power energy-efficient dual-mode wake-up receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 517–526, Feb. 2015.

[49] B. van Liempd, M. Vidojkovic, M. Lont, C. Zhou, P. Harpe, D. Milosevic, and G. Dolmans, "A 3μW fully-differential RF envelope detector for ultra-low power receivers," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2012, pp. 1496–1499.

[50] P. T. Theilmann, C. D. Presti, D. Kelly, and P. M. Asbeck, "Near zero turn-on voltage high-efficiency UHF RFID rectifier in silicon-on-sapphire CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, May 2010, pp. 105–108.

[51] S. Mandal and R. Sarpeshkar, "Low-power CMOS rectifier design for RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 6, pp. 1177–1188, Jun. 2007.

[52] V. Mangal and P. R. Kinget, "An ultra-low-power wake-up receiver with voltage-multiplying self-mixer and interferer-enhanced sensitivity," in *Proc. IEEE Custom Integrated Circuits Conf.*, Apr. 2017, pp. 1–4.

[53] J. Moody, P. Bassirian, A. Roy, N. Li, S. Pancrazio, N. S. Barker, B. H. Calhoun, and S. M. Bowers, "A -76dBm 7.4nW wakeup radio with automatic offset compensation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 452–454.

[54] A. S. Rekhi and A. Arbabian, "A 14.5mm^2 8nW $-$59.7dBm-sensitivity ultrasonic wake-up receiver for power-, area-, and interference-constrained applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 454–456.

[55] V. Mangal and P. R. Kinget, "A 0.42nW 434MHz -79.1dBm wake-Up receiver with a time-domain integrator," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 438–440.

[56] M. R. Abdelhamid, A. Paidimarri, and A. P. Chandrakasan, "A $-$80dBm BLE-compliant, FSK wake-up receiver with system and within-bit dutycycling for scalable power and latency," in *Proc. IEEE Custom Integrated Circuits Conf.*, Apr. 2018, pp. 1–4.

[57] A. Alghaihab, J. Breiholz, H. Kim, B. Calhoun, and D. D. Wentzloff, "A 150 μW -57.5 dBm-sensitivity Bluetooth Low-Energy back-channel receiver with LO frequency hopping," in *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, Jun. 2018, pp. 324–327.

[58] Y.-H. Liu, C. Bachmann, X. Wang, Y. Zhang, A. Ba, B. Busze, M. Ding, P. Harpe, G.-J. van Schaik, G. Selimis, H. Giesen, J. Gloudemans, A. Sbai, L. Huang, H. Kato, G. Dolmans, K. Philips, and H. de Groot, "A 3.7mW-RX 4.4mW-TX fully integrated Bluetooth Low-Energy/IEEE802.15.4/proprietary SoC with an ADPLL-based fast frequency offset compensation in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 236–237.

[59] A. Sai, H. Okuni, T. T. Ta, S. Kondo, T. Tokairin, M. Furuta, and T. Itakura, "A 5.5 mW ADPLL-based receiver with a hybrid loop interference rejection for BLE application in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3125–3136, Dec. 2016.

[60] F.-W. Kuo, S. B. Ferreira, H.-N. R. Chen, L.-C. Cho, C.-P. Jou, F.-L. Hsueh, I. Madadi, M. Tohidian, M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "A Bluetooth Low-Energy transceiver with 3.7-mW all-digital transmitter, 2.75-mW high-IF discrete-time receiver, and TX/RX switchable on-chip matching network," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1144–1162, Apr. 2017.

[61] M. Ding, X. Wang, P. Zhang, Y. He, S. Traferro, K. Shibata, M. Song, H. Korpela, K. Ueda, Y.-H. Liu, C. Bachmann, and K. Philips, "A 0.8V 0.8mm^2 Bluetooth 5/BLE digital-intensive transceiver with a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 446–448.

[62] H. Liu, Z. Sun, D. Tang, H. Huang, T. Kaneko, Z. Chen, W. Deng, R. Wu, and K. Okada, "A DPLL-centric Bluetooth Low-Energy transceiver with a 2.3-mW interference-tolerant hybrid-loop receiver in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3672–3687, Dec. 2018.

[63] A. M. Alghaihab, H. Kim, and D. D. Wentzloff, "Analysis of circuit noise and non-ideal filtering impact on energy detection based ultra-low-power radios performance," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 12, pp. 1924–1928, Dec. 2018.

[64] C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli, and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-$/mu$m CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1039–1045, Jul. 2000.

[65] T.-H. Lin and Y.-J. Lai, "An agile VCO frequency calibration technique for a 10-GHz CMOS PLL," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 340–349, Feb. 2007.

[66] K. Wang, L. Qiu, J. Koo, R. Ruby, and B. Otis, "Design of 1.8-mW PLL-free 2.4-GHz receiver utilizing temperature-compensated FBAR resonator," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1628–1639, Jun. 2018.

[67] C.-H. Park and B. Kim, "A low-noise, 900-MHz VCO in 0.6-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 586–591, May 1999.

[68] M. Silva-Pereira, J. T. de Sousa, J. C. Freire, and J. C. Vaz, "A 1.7-mW -92-dbm sensitivity low-IF receiver in 0.13-μm CMOS for Bluetooth LE applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 1, pp. 332–346, Jan. 2019.

[69] X. Huang, A. Ba, P. Harpe, G. Dolmans, H. de Groot, and J. R. Long, "A 915 MHz, ultra-low power 2-tone transceiver with enhanced interference resilience," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3197–3207, 2012.

[70] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μw minimum RF input power," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.

[71] P. H. P. Wang, C. Zhang, H. Yang, M. Dunna, D. Bharadia, and P. P. Mercier, "A low-power backscatter modulation system communicating across tens of meters with standards-compliant Wi-Fi transceivers," *IEEE J. Solid-State Circuits*, vol. 55, no. 11, pp. 2959–2969, Nov. 2020.

[72] L. W. Couch, II, *Digital and Analog Communication Systems*, 4th ed. Upper Saddle River, NJ, USA: Prentice Hall PTR, 1992.