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High-precision phase detection in femtosecond timing and synchronization system for TXGLS

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Abstract

High-precision phase detection is critical to the timing and synchronization system for particle accelerators. A live calibration signal is introduced to femtosecond-level phase detection in order to measure the relative phase jitter between a reference wave and a radio frequency (RF) signal, and compensate for the cable electrical length drift due to the thermal variation effect. Non-IQ sampling and 2-stage cascaded integrator-comb filters are integrated into the field-programmable gate array-based digital signal processing to reduce spectrum aliasing and suppress noise. Fine adjustment of hardware components has been made to ensure the isolation between different signals and the linearity over the full-range power level. We have achieved a 6.3 fs root mean square timing jitter for a 2856 MHz RF signal in a single channel, compared to the theoretical limit of 5.1 fs for the current hardware component.

Keywords: phase detection, calibration signal, digital signal processing, timing jitter

(Some figures may appear in colour only in the online journal)

1. Introduction

The low level radio frequency (LLRF) control system is an essential part of particle accelerators [1, 2], and femtosecond-level timing and synchronization (T&S) have a significant impact on the light source facility [3, 4]. In a large-scale particle accelerator, a stabilized radio frequency (RF) signal is distributed as a phase reference over fiber links or coaxial cables, while a receiver at the end station reconstructs the reference signal and synchronizes an RF cavity or a laser resonator to the reference wave [5]. The LLRF controller stabilizes the linear particle accelerator (Linac) RF phase and the optical cavity length by feedback controlling the klystron and piezo, maintaining the jitter between end stations at tens-of-fs level [6, 7].

RF phase detection systems must fulfill high demands on precision and stability to meet the goals of state-of-the-art

femtosecond-level synchronization in modern particle accelerators, especially x-ray light sources such as the Linac Coherent Light Source-II (LCLS-II), x-ray free-electron laser (XFEL) and Tsinghua x-ray gamma light source (TXGLS) [8, 9]. Physically, the RF signal is picked up by the cavity directional coupler in the Linac tunnel, while the receiver chassis containing the LLRF digital controller is located in the klystron gallery to avoid noise and radiation. Synchronization to a reference wave is always corrupted by a phase detection error originating in the electrical length of the cable (between the Linac tunnel and the klystron gallery) due to the thermal variation effect. In modern particle accelerators, it is common to compensate for the phase drift with active methods such as piezo stretchers and temperature controllers [10–12], which can be detailedly implemented in different ways, i.e. cooling water [13] and proportional-integral-derivative

Figure 1. Schematic of high-precision phase detection system.

(PID) temperature controllers [14]. Instead of controlling the ambient temperature, the technique reported here employs a time-multiplexed calibration signal to correct the phase drift along the cable. This fully digital phase detection system has a high precision to meet the femtosecond-level requirement and will ultimately reduce the timing jitter in the T&S system.

2. Theoretical description of high-precision phase detection

2.1. Calibration signal

In the control system of a particle accelerator, one has to detect the phase information and obtain the phase difference between the reference (**REF**) and the signal (**SIG**) with a high precision in order to synchronize **SIG** to **REF** at the femtosecond level. The schematic of the high-precision phase detection system is shown in figure 1. To mitigate the thermal variation effect during the propagation, **REF** and **SIG** are picked up respectively at point G and point H, which are physically close to the device under control (DUC). Cables (from point C to D, from point E to F) between the DUC and the digital signal processing (DSP) board undergo environmental perturbations, resulting in the phase drift. A live calibration signal is introduced to the high-precision phase measurement to compensate for the cable electrical length drift. Once synthesized in an field-programmable gate array (FPGA), the calibration signal (**CAL**) is sent out through a digital-to-analog converter (DAC) and propagates through the cable from point A to B. At point B, it is split into two parts leading to the **REF** channel and the **SIG** channel respectively. The power combiner at point C (or E) is used for combining **REF** (or **SIG**) with the split calibration signal. Then the split calibration signals co-propagate with **REF** from point C to D, as well as with **SIG** from point E to F. Calibration signals **CAL1** and **CAL2** contain information as to the phase shifts each has encountered along its path (from point C to D, or from point E to F).

We can derive simplified equations to characterize propagations of **REF**, **SIG**, **CAL1** and **CAL2** through cables. Given ϕ as the signal phase of interest, measurable signal phase Φ seen at each analog-to-digital converter (ADC) channel can be

$$\Phi_{\text{REF}} = \phi_{\text{REF}} + \phi_{t_1}, \quad (1a)$$

$$\Phi_{\text{SIG}} = \phi_{\text{SIG}} + \phi_{t_2}. \quad (1b)$$

The calibration signals measured by each ADC channel are

$$\Phi_{\text{CAL1}} = \phi_{\text{CAL}} + \phi_{t_0} + \phi_{t_01} + \phi_{t_1}, \quad (2a)$$

$$\Phi_{\text{CAL2}} = \phi_{\text{CAL}} + \phi_{t_0} + \phi_{t_02} + \phi_{t_2}. \quad (2b)$$

The phase delay ϕ_{t_0} is not critical here, since it can be eliminated by the differential calculation. In order to cancel delay changes of ϕ_{t_1} and ϕ_{t_2} , calibration signals (**CAL1** and **CAL2**) with delay information could be used to obtain the desired phase difference between **REF** and **SIG**:

$$\phi_{\text{REF}} - \phi_{\text{SIG}} = (\Phi_{\text{REF}} - \Phi_{\text{CAL1}}) - (\Phi_{\text{SIG}} - \Phi_{\text{CAL2}}) + (\phi_{t_01} - \phi_{t_02}). \quad (3)$$

Cable lengths of calibration signals should match to keep $(\phi_{t_01} - \phi_{t_02})$ as a constant value in spite of the temperature variation. The phase delay on the path BC-BE-GC-HE can not be canceled, so we put them in a temperature stabilized box to keep their phase delay variations as small as possible.

The RF phase is detected at an intermediate frequency (IF) which is created by mixing the RF signal with a local oscillator (LO) signal, resulting in a signal at the beat frequency. An analog front-end circuit down-converts the RF signal to IF (24 MHz) for signal processing, and up-converts the calibration signal to RF signal frequency (2856 MHz) for signal combining. Because the phase noise of LO signal is common to both channels, it is cancelled in the phase measurement process by design. The use of the down-converter stage improves the phase detection accuracy and extends the phase detection frequency up to tens of GHz.

The calibration signal is time-multiplexed with **REF** or **SIG** in order to calibrate out the variation of the cable. Since **REF** is a continuous wave (CW) which can not be turned off in our system, Φ_{REF} can represent the **REF** phase seen by the ADC when **CAL1** is off. The phase of **CAL1** can not be detected directly so that we have to extract the phase information from **REF_CAL** which is the combination of **REF** and **CAL1** when **CAL1** is on. We could obtain Φ_{CAL1} with **CAL1** being the vector difference between **REF_CAL** and **REF**. In the particle accelerator system, **SIG** may be a pulse signal rather than a continuous wave. This case is simpler because **SIG** and **CAL2** can be separated inherently in the time domain. Therefore, Φ_{SIG} and Φ_{CAL2} will be detected directly.

Noise reduction is an essential requirement of the high-precision phase detection system. We investigate the phase fluctuation $\Delta\Phi$ using the phasor diagram shown in figure 2. Supposing the root mean square (RMS) noise measured by the ADC is constant, a greater amplitude leads to a smaller phase fluctuation. Therefore, we should maximize the signal amplitude in **REF**, **SIG** and **CAL** channels.

2.2. Digital signal processing algorithm

The high-precision phase detection in the femtosecond-level T&S system implies ultra low noise. The broadband (white) noise is minimized by the proper selection of low noise components, while the low-frequency noise is suppressed by the feedback control loop. The RF (or laser) phase measurement

Figure 2. Phasor diagram of phase fluctuation. (a) Phase fluctuation of **REF**. (b) Phase fluctuation of **CAL**.

Figure 3. Architecture of 2-stage CIC filter.

is implemented by heterodyning it to an IF which is further mixed to the baseband digitally. In the digital RF system, the waveform is usually represented in the form of a complex vector (phasor), commonly described with its in-phase (I) and quadrature (Q) components. While IQ sampling of an IF waveform has useful properties and is easy to understand, it aliases distortion terms onto the fundamental frequency. Non-IQ sampling, which changes the phase shift between samples to something close to, but not exactly 90° , keeps most of the advantages of IQ sampling while permitting distortion terms to be characterized and filtered out digitally [15]. For a non-IQ sampling process, the IF frequency f_{IF} and the sample rate f_s are related by

$$\frac{f_{IF}}{f_s} = \frac{M}{N}, \quad M, N \in \mathbb{N}^+. \quad (4)$$

In the T&S system of TXGLS, f_{IF}/f_s is 4/17 which means 17 samples over four cycles.

The I and Q components can be treated as the Cartesian coordinates implying the amplitude and phase information of the original signal. Mixers and low pass filters (LPF) are employed for IQ demodulation. The split input signal is mixed with two LO signals (which have a 90° phase shift between them) respectively, followed by LPFs removing the high frequency mixing products [16]. The mixer LO port is used to select the spectrum line to be measured. Ideally, only when the input signal and LO signal have the same frequency, LPFs can obtain the DC (direct current) IQ outputs. The LPF is implemented by a cascaded integrator-comb (CIC) filter and takes N samples averaging in the non-IQ process

$$I = \frac{2}{N} \sum_{n=1}^N y_n \cdot \cos(n\theta), \quad (5a)$$

$$Q = \frac{2}{N} \sum_{n=1}^N y_n \cdot \sin(n\theta), \quad (5b)$$

where $\theta = 2\pi M/N$.

The CIC digital filter, which utilizes only addition and subtraction, and requires no multiplication operations, is an efficient and economical implementation in the FPGA, with characteristics of low pass frequency and linear phase response [17]. Leveraging of the fast processing and real-time performance provided by the FPGA, the CIC filter is often embedded in the T&S system as moving-average digital processing for noise suppression [18]. The CIC filter contains integrators which are simply accumulators and combs which subtract a delayed input sample from the current accumulation. A 2-stage CIC filter is included in our feedback loop to improve the anti-aliasing and image-rejection performance. We obtained this 2-stage CIC architecture by cascading two identical moving average filters, then rearranging the sections to place all integrators first and all combs last, as shown in figure 3. Since combs and integrators are linear time invariant (LTI) systems, we are permitted to swap the order of integrators and combs. A decimator with a sample rate change factor R is built into the architecture to reduce the computational complexity of the narrowband low pass filtering. We put the comb section on the side of the filter operating at the lower sample rate to reduce the data storage requirement. Regarding our 2-stage CIC filter, the sample rate change R is equal to the differential delay D in the comb section. The differential delay D , which must be an integer multiple of N , means that D samples are averaged in the first stage and D^2 samples are averaged in the second stage. Since a larger D indicates noise reduction but higher latency, we have to trade off between the noise suppression and the loop delay.

Figure 4. The 2-stage CIC filter behavior in the time domain. Each circle represents a $x(n)$ input sample. Indexes of samples from left to right are in ascending order, while samples along the longitudinal direction share the same index. The dashed yellow rectangle and the dashed green triangle represent outputs of the first and the second integrators respectively. The decimator picks up only one in every D samples (D is assumed to be 3 in this diagram). The output of the first comb takes the shape of the trapezoid drawn in continuous blue. The second comb subtracts the smaller trapezoid from the next bigger trapezoid, yielding $y_{C2}(m)$ which is in the shape of the continuous red parallelogram.

It is common and easy to describe the 2-stage CIC filter in the frequency domain as

$$H(z) = H_I^2(z) \cdot H_C^2(z) = \left(\frac{1 - z^{-D}}{1 - z^{-1}} \right)^2, \quad (6)$$

where $H(z)$, $H_I(z)$ and $H_C(z)$ are transfer functions of the CIC filter, the integrator and the comb respectively. If we evaluate the transfer function $H(z)$ on the unit circle of z -plane, the DC gain of the CIC filter can be obtained by setting $z = e^{j2\pi f}$, yielding

$$G_{CIC} = \lim_{f \rightarrow 0} |H(e^{j2\pi f})| = D^2. \quad (7)$$

We can also investigate the 2-stage CIC filter behavior in the time domain, as shown in figure 4. Let $x(n)$ be the input

samples to the CIC filter. The input $x(n)$ is accumulated twice in the integrator section as depicted in

$$y_{I1}(n) = \sum_{k=1}^n x(k) \quad (8)$$

and

$$y_{I2}(n) = \sum_{k=1}^n y_{I1}(k) = \sum_{k=1}^n \sum_{i=1}^k x(i), \quad (9)$$

where $y_{I1}(n)$ and $y_{I2}(n)$ are outputs of the first and the second integrators. The decimator picks up only one in every D samples, resulting in

$$y_{dec}(m) = y_{I2}(mD - D + 1), \quad (10)$$

Figure 5. Experimental setup.

where $y_{\text{dec}}(m)$ is the decimator output. Later, a 2-stage subtraction is applied to the decimated result in the comb section:

$$y_{C_1}(m) = y_{\text{dec}}(m+1) - y_{\text{dec}}(m) = \sum_{k=mD-D+2}^{mD+1} \sum_{i=1}^k x(i), \quad (11)$$

$$y_{C_2}(m) = y_{C_1}(m+1) - y_{C_1}(m) = \sum_{k=mD+D+2}^{mD+D+1} \sum_{i=k-D+1}^k x(i), \quad (12)$$

where $y_{C_1}(m)$ and $y_{C_2}(m)$ are outputs of the first and the second combs. The final output $y_{C_2}(m)$ of the 2-stage CIC filter is the sum of D^2 correlated samples in the time domain, as shown in figure 4. For correlated variables, the variance of the mean is

$$\sigma^2 = \text{Var}(\bar{X}) = \frac{1}{n^2} \left[\sum_{i=1}^n \text{Var}(X_i) + 2 \sum_{1 \leq i < j \leq n} \text{Cov}(X_i, X_j) \right], \quad (13)$$

where Var and Cov denote the variance and the covariance of the random variable X respectively. Let σ_{raw} and σ_{CIC} be standard deviations of the CIC input and output data. According to (13), we can conclude that the 2-stage CIC filter has a noise suppression ratio

$$\eta = \frac{\sigma_{\text{CIC}}}{\sigma_{\text{raw}}} = \frac{\sqrt{D^2 + 2C(D, 2) + 4 \sum_{j=2}^{D-1} C(j, 2)}}{D^2}, \quad (14)$$

where $C(n, k)$ is the combination in combinatorics which means selecting k elements from a collection of n elements.

With I/Q components averaged by two CIC filters, a coordinate rotation digital computer (CORDIC) module extracts the amplitude and phase of the signal [19]. The CORDIC algorithm is implemented as a rectangular-to-polar conversion module due to the efficiency of calculating inverse trigonometric functions in the FPGA [20]. It is necessary to note that a CORDIC engine has an intrinsic gain α of about 1.64676, for a large number of stages. To achieve a higher accuracy in the FPGA, the I and Q components are shifted together to make their MSBs (most significant bit) not all zero. The shift does not affect the phase calculation, but for the amplitude calculation, we need to shift it back afterward. In the high-precision phase detection system, the DC gain is

$$G = \frac{\alpha D^2}{2}, \quad (15)$$

ignoring the shift effect.

3. Experimental demonstration of high-precision phase detection

In the experimental configuration shown in figure 5, an LLRF46 board [21] synthesizes **REF** and **CAL**, then drives two DACs to output them respectively, followed by a splitter combining them into a time-multiplexed signal to be measured by an ADC. Since down-conversion and up-conversion do not introduce the phase noise, the heterodying processing is omitted in the experiment. The experiment is demonstrated at 24 MHz which is equal to IF. Based on the described theory, amplifiers are employed to maximize the signal amplitude in order to reduce the phase noise. Amplifiers and attenuators are cascaded in the loop to enhance the isolation and suppress the crosstalk.

3.1. Isolation and linearity measurement

The high-precision phase detection system requires the isolation between different signals and the linearity over the full-range power level. To quantify the isolation in the case of continuous wave, one can maintain **CAL** constant and vary the phase of **REF** over 2π at a certain amplitude, while observing the IQ plane graph of **REF_CAL**, as shown in figure 6. The IQ curve is fitted with an ellipse, which is characterized by the eccentricity e . If **REF** is in a high isolation from **CAL**, the IQ curve of **REF_CAL** is close to a circle, which indicates a homogeneous noise performance over the whole phase cycle. The linearity measurement consists of scanning the whole power level (varying amplitudes of **REF** and **CAL**) and observing the eccentricity of **REF_CAL**. It is important to note that the operating point of the amplifier has to be maintained far below the 1 dB compression point in the linear region to mitigate the non-linearity and the distortion. As shown in figure 7, we have achieved a 0.019 eccentricity which demonstrates a good isolation and linearity over the full-range power level both in **REF** and **CAL** channels.

Figure 6. IQ circles of *REF* and *REF_CAL*.

Figure 7. Eccentricities of *REF_CAL* IQ ellipses over the full-range power level both in *REF* and *CAL* channels.

3.2. Timing jitter measurement

We can quantify the timing jitter of the high-precision phase detection system with the experimental configuration shown in figure 5. Applying a ramp of amplitude value in the FPGA and observing the resulting phase timing jitter accordingly demonstrate that a greater amplitude leads to a smaller phase fluctuation both in *REF* and *CAL* channels, as shown in figure 8.

If A is the signal amplitude measured by the ADC and f is the RF frequency of the main accelerator in TXGLS, the RMS timing jitter σ can be obtained according to

$$\sigma = \frac{FS}{2\sqrt{2}} \cdot 10^{-\frac{SNR-NF}{20}} \cdot \eta \cdot \sqrt{2} \cdot \frac{1}{A} \cdot \frac{1}{2\pi f}, \quad (16)$$

where FS and SNR are the full-scale counts and the signal-to-noise ratio of the ADC, NF is the noise figure of the amplifier. The LTC2255 is embedded in the LLRF46 board as the ADC. Note that the LTC2255 is a 14-bit ADC, the FS is $2^{14} = 16384$ least significant bits (LSBs). The reference voltage of the LTC2255 is set relatively low to increase sensitivity, which also degrades the SNR. The SNR of the ADC is 68.6 dB in our case, which is corresponding to 11.1 bits ENOB (effective number of bits). The low noise amplifier introduces a 2.9 dB

Figure 8. Phase timing jitter versus normalized amplitude.

Figure 9. Phase error measurement for a single channel.

NF to our system. By setting differential delay $D = 85$ in the 2-stage CIC filter, the noise suppression ratio η is 0.089 according to (14). It is also necessary to know that the IQ demodulation produces a factor of $\sqrt{2}$ in the phase noise estimation. Since one channel ADC monitors the vector sum of **REF** and **CAL1**, each signal (**REF** and **CAL1**) accounts for half of the full-scale amplitude. The FS is the peak-to-peak quantized amplitude in counts, so the maximum A is $2^{14}/4 = 4096$ LSBs. This is also the case for **SIG** and **CAL2** in another ADC channel. Considering that the RF frequency is $f = 2856$ MHz in TXGLS, the RMS timing jitter limit is 5.1 fs for a single channel in theory according to (16). Figure 9 illustrates the phase error measurement in the **REF** channel. We have achieved a 6.3 fs RMS timing jitter for a 2856 MHz RF signal in a single channel, which almost reaches the theoretical limit for the current hardware component.

In the case of the continuous wave, the timing jitter in the **REF** channel is $\sigma_{\text{REF}} = 5.1$ fs, but Φ_{CAL1} can not be obtained directly. Provided that **REF** and **CAL1** interfere constructively, the amplitude of **REF_CAL** is $2A$,

yielding $\sigma_{\text{CAL1}} = \sqrt{1^2 + (1/2)^2} \cdot \sigma_{\text{REF}} = 5.7$ fs. If **SIG** is a pulse wave, timing jitter values of **SIG** and **CAL2** are $\sigma_{\text{SIG}} = \sigma_{\text{CAL2}} = 5.1$ fs. According to (3), the ultimate timing jitter limit of $(\Phi_{\text{REF}} - \Phi_{\text{SIG}})$ can be obtained by

$$\sigma_J = \sqrt{\sigma_{\text{REF}}^2 + \sigma_{\text{CAL1}}^2 + \sigma_{\text{SIG}}^2 + \sigma_{\text{CAL2}}^2}, \quad (17)$$

which is 10.5 fs in our phase detection system.

With the high-precision phase detection system fully implemented in TXGLS, 48.2 fs RMS timing jitter has been demonstrated between the mode-locked laser oscillator and the RF reference signal [22].

4. Conclusion

In summary, a high-precision phase detection technique has been developed by using a live calibration signal to measure the relative phase jitter and compensate for the thermal effect at a receiver. Non-IQ sampling and 2-stage CIC filters are employed in the digital signal processing to reduce spectrum aliasing and suppress noise respectively. Hardware component adjustment is optimized to ensure the isolation between different channels and the linearity over the full-range power level. A 6.3 fs RMS timing jitter in a single channel has been demonstrated in the T&S system, compared to the theoretical limit of 5.1 fs for the current hardware component.

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