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High-Transition Temperature Superconducting Digital Electronics With Helium Ion Irradiated Junctions

A Dissertation submitted in partial satisfaction
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by

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I dedicate my dissertation work to all my family members. Especially, to my dearest parents, who support me all along with no doubt.

ABSTRACT OF THE DISSERTATION

High-Transition Temperature Superconducting Digital Electronics With Helium Ion Irradiated Junctions

by

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University of California, Riverside, March 2022
Dr. Shane A. Cybart, Chairperson

Superconducting digital logic electronics based on Josephson junctions is established as the ultra-fast speed and ultra-low power consumption microelectronics device. Significant progress has been made in the development of superconducting digital circuit based on low-T_C superconductors. Rapid single flux quantum (RSFQ) logic has been experimentally demonstrated to operate up to 770 GHz clock frequency with a bit-error rate close to the measurement limit. The power consumption is extremely low in such high-frequency operation, about three orders of magnitude less than that of CMOS logic. The energy dissipation of Quantum flux parametron (QFP) has been reduced to the order of 10^{-21} Joules per transition. However, low T_C digital circuit requires more complicated cryogenic systems to operate below liquid helium temperature (sub-kelvin temperatures). An effort has been made to develop high T_C digital circuits for operation above nitrogen temperatures. Further development is needed to solve a number of problems. In order to enable circuit functionalities and complexities required for computing, a very large-scale integration of superconducting circuit is needed. Comparing to the typical CMOS circuit integration scale,

due to the physical limitations on the size of superconducting logic cells made by traditional fabrication process, the present superconducting integrated circuit density is several orders of magnitude lower [1].

The realization of using focused helium ion beam (FHIB) to write an over-damped Josephson junction on the material of yttrium barium copper oxide (YBCO) [2] will further extend the digital logic technology to high T_C superconductors and allow the circuit be tested at liquid helium temperature, which will also make the integration with nitrogen-cooled circuits easier. Furthermore, a multilayer process is presently used to make Josephson junction, which is complicated and limit the scale of the circuit. The ion irradiation technology makes the circuits simpler. It is possible to fabricate nano scale circuit, allows to design more complex circuit and solve the challenge of large-scale integration. In this dissertation, we show the simulations and measurements of some basic RSFQ cells made by high T_c materials, with which can monitor the propagation of signal and prove the logic function of the chip fabricated by FHIB technology. In the future, we will continue the prospects for a further increase of the operation temperature and implementation of complex digital circuit.

Contents

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Chapter 1

Introduction

1.1 Superconducting Electronics

Superconductivity was discovered by Dutch physicist Heike Kamerlingh Onnes in 1911 in Leiden when he was studying the resistance of solid mercury at cryogenic temperatures [3]. It is a phenomenon that in certain materials, the electrical resistance vanishes and magnetic fields are expelled when the temperature is lowered than a characteristic critical temperature T_C. Great efforts have been devoted to finding out the quantum mechanical mystery of superconductivity. In 1933, Meissner and Ochsenfeld discovered the Meissner effect, the phenomenon that the applied magnetic fields are expelled from superconductors [4]. In 1935, Fritz and Heinz London devised the London equation and used it to explain the Meissner effect, which was the first theoretical model for superconductivity [5]. Anther important step occurred in 1950s: the phenomenological Ginzburg–Landau theory (1950) [6] and the microscopic BCS theory (1957) [7]. The phenomenological Ginzburg–Landau theory successfully explained the macroscopic properties of superconductors and predicted the

two categories of superconductors: Type I and Type II. The BCS theory was proposed by Bardeen, Cooper and Schrieffer, which was a microscopic theory and explained the superconducting current as a superfluid of cooper pairs. Cooper pair is a pair of attractive electrons bounded together and mediated by the exchange of phonons. In 1962, Josephson established the Josephson effect that a supercurrent can flow through two superconductors separated by a thin insulating layer [8]. IBM had fabricated the first Josephson junction within a few years [9]. In 1983, Bell Labs successfully made a niobium/aluminum oxide Josephson junction with a more reliable and easier fabrication technology.

Superconducting digital electronics started from the invention of cryotron, a simple switching device developed by Buck in 1954 [10]. The cryotron utilized the transition from the superconducting state to the normal state by the magnetic field which can destroy the superconductivity. Due to the transition was caused by a thermal effect, the switching speed was low. In 1967, with the prediction of the superconducting tunneling effect by Josephson and experimental demonstration of the Josephson effect by Anderson and Rowell, Matisoo proposed a switching device based on Josephson tunnel junctions, called latching logic gate [11] [12]. In order to reset the logic gate from resistive state to the superconducting state, the device should be AC powered. The switching delays were about 10 ps [13], which were much shorter than the switching time of semiconductor devices at that time. However, with increasing the frequency of the AC power, the punch-through probability would also increase and cause the failures in the logic operation. In order to overcome the disadvantage of latching logic, a new logic operation had been proposed in 1985, which used a single flux quantum (SFQ) as an information carrier. The first logic system utilizing SFQ pulses

propagating in the circuit was called resistive SFQ logic, proposed by the researchers from Moscow State University [14]. The circuit consisted by overdamped Josephson junctions and used small resistors for connecting gate to gate. In order to improve the speed and energy efficiency, the researchers used superconducting wires and Josephson junctions to replace the resistors and named the new system rapid SFQ (RSFQ) [15]. The RSFQ circuit had a wider operating margin, lower bit error and higher operating frequencies, up to the order of 100 GHz [16]. The systems based on SFQ have been developed recently, such as the application in the reversible computing, neuromorphic computing and quantum computing. Reversible computing has been proposed to achieve if there is no reductions in information entropy during a logic operation. The adiabatic superconducting device with adiabatic switching operations is a good candidate for a logically and physically reversible gate, which bit energy can be close to the order of thermal limitation k_BT [17]. A natural neuromorphic technology utilizes SFQ circuit to mimic neural systems with quantized SFQ pulses and superconducting transmission lines resembling action potentials and axons generated by biological neurons, respectively [18]. In superconducting quantum computing system, SFQ circuit can be used for generating microwave pulse with the time resolution of sub-ns, precisely controlling the qubit state and adequately detecting the output microwave at the same temperature stage as qubits. [19].

1.2 Limitation

The motivated efforts toward development of superconducting device is that the superconducting digital circuit is believed to be fastest speed and lowest power consumption.

This circuit will contribute to the future type computing, like reversible computing and quantum computing. Also, Superconducting device is sensitive to the magnetic field which can use as magnetic flux signal detector.

Superconducting electronics has already contributed significantly to the needs of our society. It has the potential to play a major role as a key technology in the future. However, superconducting low T_C devices need cooling to quite low temperatures. Difficulty arises in transitioning these signals through large temperature gradients for connection to semiconductor components. For practical applications, a cast of important support electronics is needed to connect these low temperature quantum devices to our classical worlds.

Therefore, we try to make a high T_C digital circuit which don't demand stringent requirements for a cryocooler system and allow the device to operate at a higher temperature. Moreover, the voltage state resistances of high-T_C superconducting devices are more suitable for impedance matching to semiconductors than the resistance of traditional low-T_C superconducting devices. We apply a simpler technology to fabricate the Josephson junction: Focus Helium Ion Beam (FHIB), which can make a Josephson junction with a high current density. This technology can also scale down the size of junction and use for making large scale integrated circuit in the future. Improvement in this technology would also help to meet expectations in the superconducting electronics concerning size and integration into existing frame works of the telecommunication industry.

1.3 High T_c Superconductivity

High T_C superconductors are a kind of materials that behave as superconductors with critical temperatures greater than the boiling point of liquid nitrogen. In 1986, Bednorz and Muller discovered superconductivity in lanthanum barium copper oxide (LBCO) [20], a lanthanum-based cuprate perovskite material, which had a transition temperature of 35 K. Soon after that, it was found that replacing the lanthanum with yttrium (yttrium barium copper oxide) would raise the critical temperature above 90 K [21]. Fig. 1.1 is the experimental resistance and temperature characteristics of a 35 nm Yttrium barium copper oxide (YBCO) thin film. The transition temperature is about 94 K. YBCO is a cuprate superconductor, which crystallizes in a layered orthorhombic distorted perovskite structure. As shown in Fig. 1.2, the material is consisted by 3 stacks of perovskite in a unit cell with deficient oxygen. YBCO is very sensitive to the oxygen order in the crystal lattice which can be altered by light ion irradiation. Due to ion irradiation would cause displacement of atoms in the crystal structures or carrier concentration would change from excess of oxygen vacancies, it can use to modify the materials and make a Josephson junction. Our group has demonstrated that Josephson junctions can be fabricated on epitaxial YBCO thin films by utilizing FHIB [2]. Moreoever, comparing to other high T_C superconducting materials, YBCO is relatively easy to grow through Sputtering. The critical temperature and current density are also high enough for our experiments.

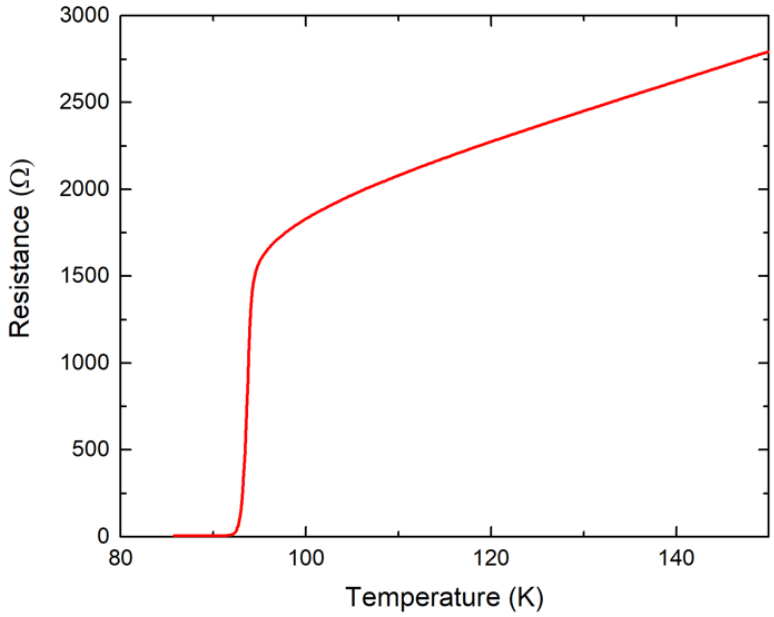

Figure 1.1: The resistance and temperature characteristics of a YBCO thin film.

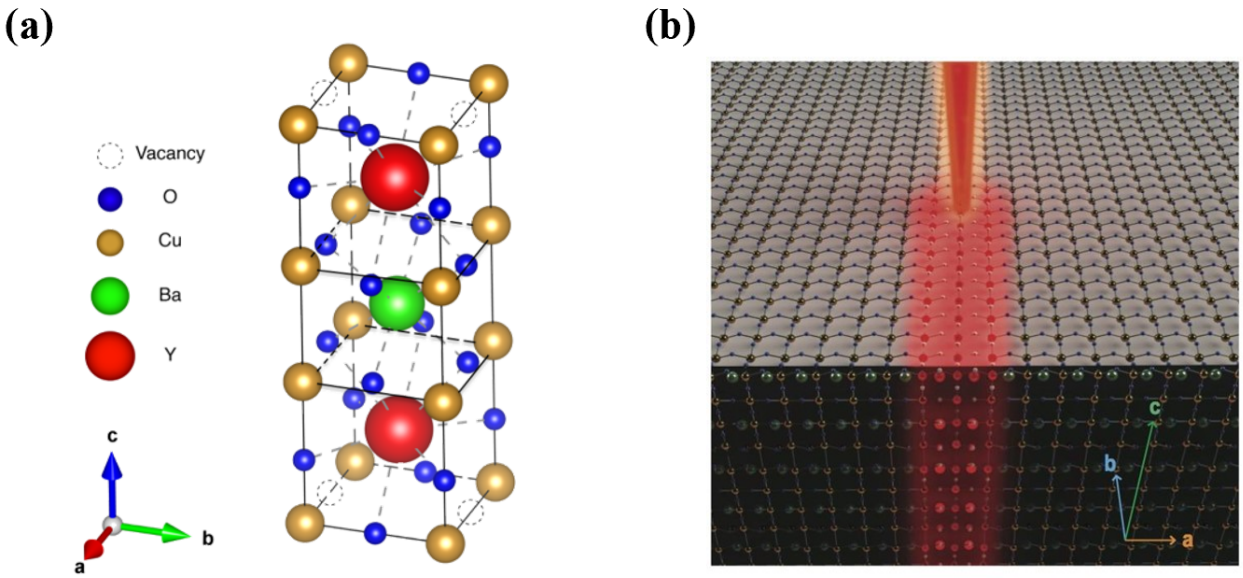

Figure 1.2: The crystal structure of YBCO and scaled model of focused helium ion beam interacting with an YBCO crystal. [2].

1.4 Josephson junction

A Josephson junction is one that consists of two superconductors weakly coupled by a thin barrier, shown in Fig. 1.3. It can experience quantum mechanical tunneling of electron cooper pairs through the barrier without breaking up the pairs, which is an important feature of a superconductor. The behavior of a cooper pair on each side of the tunnel barrier can be expressed by a wave function. The cooper pair tunneling across the junction and the wave function coupling between two superconductor are described by the Josephson effect. The Josephson effect is the phenomenon of supercurrent flowing across the barrier without any voltage applied. The coherence of the wave function is responsible for two Josephson effects: first is the weak-link current-phase relation (DC Josephson effect) and the second is the superconducting phase evolution equation (AC Josephson effect). Two relations are used to describe the dynamics of these two Josephson effects.

The DC Josephson effect is related to a direct current crossing the junction without any external electromagnetic field applied, which is the result from Josephson tunneling. The DC Josephson current is proportional to the sine of Josephson phase. The Josephson phase is the phase difference across the junction. In this case, the Josephson phase is a constant over the time due to the absence of a voltage and the supercurrent flowing through the junction is a direct current. Critical current I_C is the maximum current to sustain the superconducting states. The DC Josephson current takes values below the critical current.

$$I = I_C sin(\phi_1 - \phi_2), \tag{1.1}$$

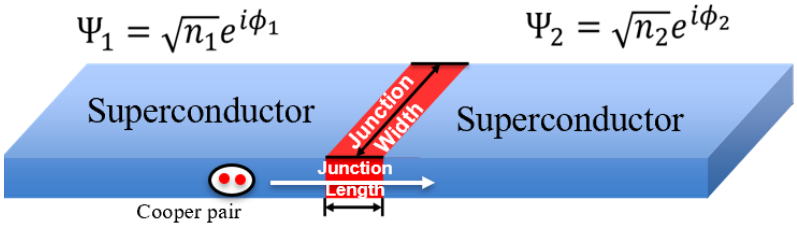

Figure 1.3: The schematics diagram of a Josephson junction.

In the AC Josephson effect, a fixed voltage is applied across the junction and results in linearly varying Josephson phase φ in accordance with time. Due to the modulation of Josephson phase, a sinusoidal alternating current with an amplitude of I_c is generated. The oscillation frequency is proportional to the applied voltage: $f = \frac{2e}{\hbar}V$. Depending on this feature, a Josephson junction can be used as a voltage-to-frequency converter. The maximum applied voltage is limited by the energy gap, which is the minimum energy required to break the Cooper pairs apart to quasiparticles excitation.

$$\frac{d\varphi}{dt} = \frac{2eV}{\hbar}, \tag{1.2}$$

Fig. 1.4 is an example of current-voltage characteristics of a Josephson junction. The junction will change to a voltage state with a resistance R_N when the applied current is larger than the critical current. $I_C R_N$ product is theoretically related to the energy gap.

When a perpendicular magnetic flux applied to the junction, the critical current will be periodically modulated with the flux quanta in a sinc function reminiscent of the optical Fraunhofer diffraction pattern shown in Fig. 1.5. Fraunhofer diffraction pattern

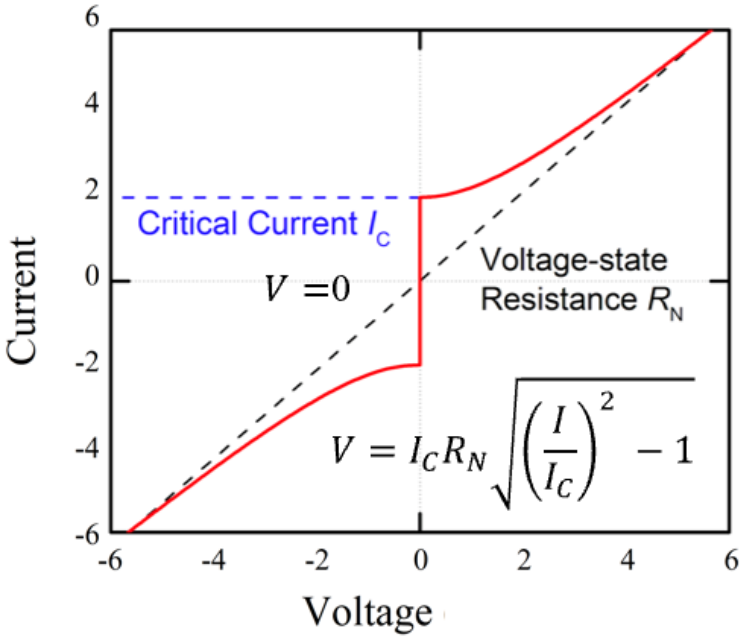

Figure 1.4: The current-voltage characteristic of a Josephson junction.

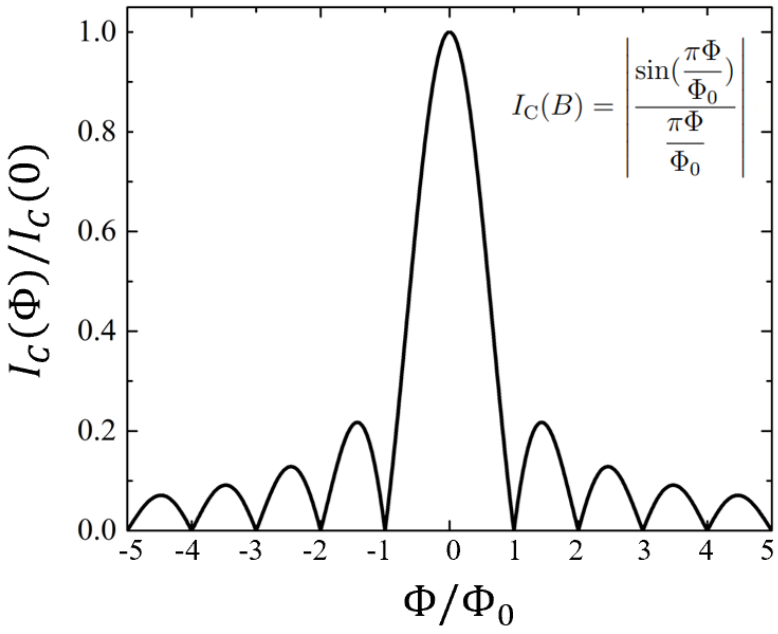

Figure 1.5: The Fraunhofer diffraction pattern of a Josephson junction.

shows the maximum Josephson current in a single Josephson junction.

1.4.1 Resistively Shunted Junction Model

The current-voltage characteristics and the dynamics of a Josephson junction can be described using the semiclassical resistively capacitively shunted junction (RCSJ) model. When the current through the Josephson junction goes above critical current (I_c), the junction becomes resistive. Cooper pairs are not the only charge carries that can tunnel through a junction. It is possible for a cooper pair to break up onto electron quasi-particles, which tunnel through the junction and recombine as a cooper pair on the other side. When these electrons tunnel through a junction, the process is resistive with a resistance R_N. According to the AC impedance of an actual junction, it is also capacitive. These processes can be modelled by the RCSJ model shown in Fig. 1.6. In this model, an ideal junction is placed in parallel with a resistor and a capacitor. 1.3 is obtained by simplifying the previous Josephson current function with this model and the Stewart-McCumber parameter β_C is got from this equation.

The current can be expressed by the voltage and the phase difference across the junction:

$$I = C\frac{dV}{dt} + I_C sin\varphi + \frac{V}{R_N}, \tag{1.3}$$

According to the superconducting phase evolution equation 1.2, the expression for the current becomes:

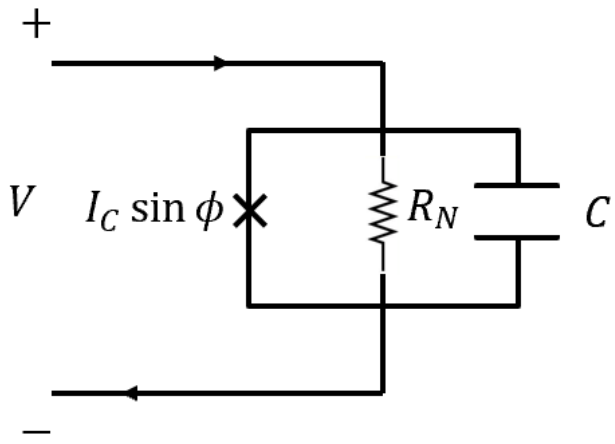

Figure 1.6: The RCSJ model for a Josephson junction. C is the effective capacitance and R the effective resistance of the junction.

$$I = sin\varphi + \frac{d\varphi}{d\theta} + \beta_C \frac{d^2\varphi}{d\theta^2}, \tag{1.4}$$

$$\theta = \frac{2e}{\hbar} I_C R_N t \tag{1.5}$$

$$\beta_C = \frac{2\pi I_C {R_N}^2 C}{\Phi_0}, \tag{1.6}$$

The constant β_C is the damping factor. Fig. 1.7 shows the experimental current–voltage characteristic of two different types of junctions. When $\beta_C > 1$, the junction is underdamped junction. An underdamped junction will show hysteresis in the current-voltage curve. When $\beta_C < 1$, the junction is overdamped junction and the current-voltage curve is nonhysteretic. When $\beta_C = 1$, the junction is critical junction. The digital circuit require an overdamped or critically damped junction.

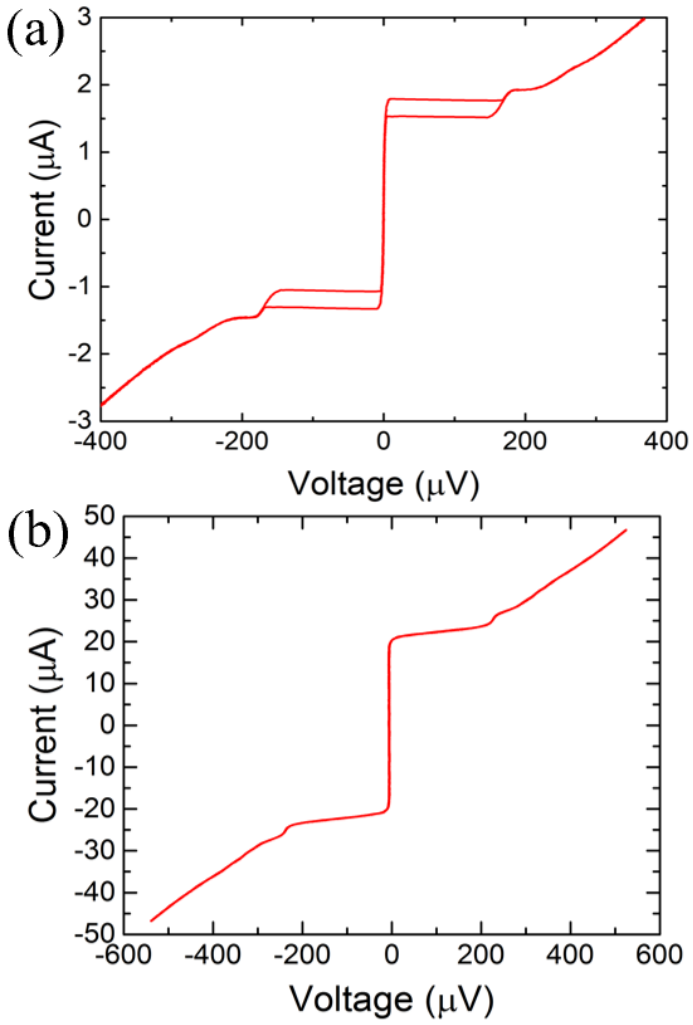

Figure 1.7: (a) A hysteretic current–voltage characteristic for an underdamped junction. (b) A non-hysteretic current–voltage characteristic for an overdamped junction.

1.4.2 Focused Helium Beam Irradiated Josephson Junctions

The junction is patterning by Focus Helium Ion Beam (FHIB) direct writing technology. Ion irradiation has strong effects on the high T_c superconductors. It causes displacement of atoms in the crystal structures or carrier concentration changes from excess of oxygen vacancies. The helium ion beam is finely focused to 0.75±0.25 nm from a gas filed ion source. YBCO lattice can be converted from superconducting to insulating at an irradiation dose $> 10^{15}\ ions/cm^2$. A moderate ion dose of $\sim 10^{16}\ He^+/cm^2$ is applied to create a very narrow insulating barrier for YBCO junction. As a result, an in-plane superconducting-insulating-superconducting (SIS) junction can be obtained by this direct ion irradiation. As a heavy dose results in a lower Josephson junction critical current, in this dissertation, an ion dose between $1.75 \times 10^{16}\ He^+/cm^2$ and $2.75 \times 10^{16}\ He^+/cm^2$ is used to modulated a critical current from 70 μA to 140 μA.

Our group have successfully fabricated a nanoscale Josephson junction by FHIB with confining the irradiated region to sub-10-nm dimensions. The junction was demonstrated with insulating tunnel barrier, no excess current and high resistance. The Fig. 1.8 (c) shows the experimental current-voltage characteristic of a S-I-S junction over a large range of temperature, which voltage state resistance R_N increases with the temperature cooling down. The non-hysteresis current-voltage curve also proves that the junction is overdamped, which is suitable for the digital circuit.

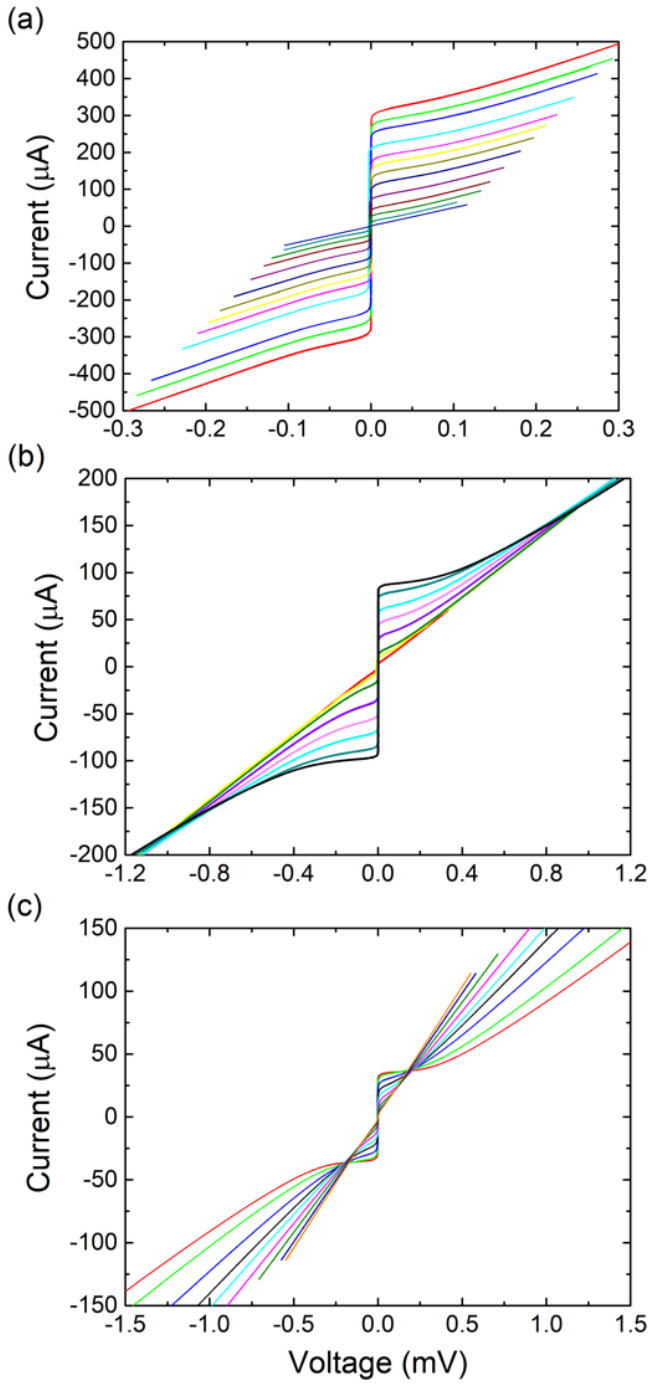

Figure 1.8: Current-voltage characteristics of 4 μm-width junctions with barrier being (a) a metal, (b) in the middle of metal-insulator transition, and (c) an insulator with temperatures ranging from 4.2 K to 45 K. In (b) the resistance is a constant $R \approx 6$ over 40K.

1.5 Superconducting digital circuit

Superconducting logic circuits are built on the properties of superconductors: zero resistance superconducting wires, flux quantization and ultrafast junction switching to encode, process and transfer data. The circuits are made by active junction and passive inductances, resistances, transformers and transmission lines.

Superconducting digital circuits are based on the properties of superconductivity and Josephson junction. The main property of superconducting circuits is related to the dynamics of magnetic flux in the circuits, which has manifested itself in macroscopic quantum state: magnetic-flux quantization in units of $\Phi_0 = h/2e$ (fluxon). In 1961, the effect of flux quantization was experimentally observed by Deaver and Fairbank [22]. They proved that the flux through a superconducting loop was quantized: $\Phi = n\Phi_0$.

Flux quantization plays an important role in the superconducting digital circuits. The current circulating around a closed superconducting loop with inductance will maintain a magnetic flux of $n\Phi_0$, which can use as a digital storage element. If the loop contains N Josephson junctions, the flux through a loop becomes:

$$\Phi + \frac{\Phi_0}{2\pi} \sum_{i=1}^{N} \varphi_i = n\Phi_0, \tag{1.7}$$

Due to the junction switching, the value of n is changed. The junction acts as a controllable valve that permits flux quanta to leak out or be pumped into a superconducting loop. One flux quantum changing would cause a 2π switching in the Josephson phase. From the function 1.2, the corresponding voltage across the junction produces a pulse with a quantized area of $\int V dt = \Phi_0$, which is named as a single flux quantum (SFQ). The pulse

width and amplitude is determined by the parameters of the Josephson junctions, which can be as narrow as 1 ps with an amplitude of about $2I_C R_N$. The switching energy per pulse is on the order of $I_C \Phi_0$, which is much lower power consumption than other technologies. The use of narrow SFQ pulses forms the basis of rapid SFQ logic (RSFQ), the fastest digital circuit that has been developed worldwide, which has been demonstrated with a speed in excess of 750 GHz [23].

Chapter 2

He-FIB Directly-Written Josephson Junctions

2.1 Ion Irradiation Effect

Several YBCObased Josephson junctions technologies have been studied, such as grain boundary [24], bicrystal junction [25], step-edge junctions [26] and c-axis sandwich junctions [27] with multiple-layer structures. However, ceramic copper-oxide superconductor is difficult to fabricate high quality multilayer. It's been known that ion irradiation can affect the material properties of YBCO and even cause the material transition from a superconductor to an insulator. A new technology is the Focused Helium Ion beam (FHIB) direct-writing, achieved by a Carl Zeiss Orion Plus helium ion microscope. Instead of using electron beam, our group use a novel FHIB junction technology to simply the junction fabrication process.

Helium ion beam has a much smaller diffraction effect, and with an atomically sharp tungsten tip, only three atoms at the topmost, which is usually called trimmer. The helium ion beam is already focused from its source. Those two key features make the beam a spot size about a quarter nanometer to half nanometer, which is about 30 times smaller than gallium based focused ion beam. As shown in Fig. 1.2 (b), an ion beam propagates through the thin film and leaves a very narrow damage track. With increasing ion dose, the resistivity increases and critical temperature decreases. YBCO lattice can be converted from superconducting to insulating at a high irradiation dose. Therefore, a moderate ion dose is applied to create a very narrow tunnel barrier for YBCO junction and a heavy dose is used to create insulating region.

2.2 $YBa_2Cu_3O_{7-\delta}$ He-FIB Junctions

Based on the effect of ion disorder, our group use FHIB to irradiate YBCO film and create a planar junction by direct writing technology with amazing properties. The disorder caused by helium ion can change the YBCO from superconductor to normal metal, or insulator. The Josephson junction is obtained by the ion irradiation, which consists of two superconductors separated by a very thin insulator. Jopseson junction can sustain a certain supercurrent without any voltage applied and then switch to a tunnel resistance under a high voltage bias, like the theoretical RCSJ model shows.

As shown in the Fig. 2.1, the helium ion microscope gets its ions from the gas field ion source. A high voltage is applied to atomically sharp tungsten tip and form the trimmer. The surrounding helium gas will be ionized by the large electrical field around

the trimmer. A series of electromagnetic lenses are used to narrow and control a helium ion beam to the nano scale, which can be used to locally disorder the desired region on the YBCO film. The spot size of the ion beam is only 0.5 nm. It can create disorder in a few nanometer wide range and scale down the junction to 2-3 nm. Performance is determined by the current and voltage characteristic, shown in Fig. 2.2. The critical current is about 35 μA and the normal state resistance is about 10 Ω.

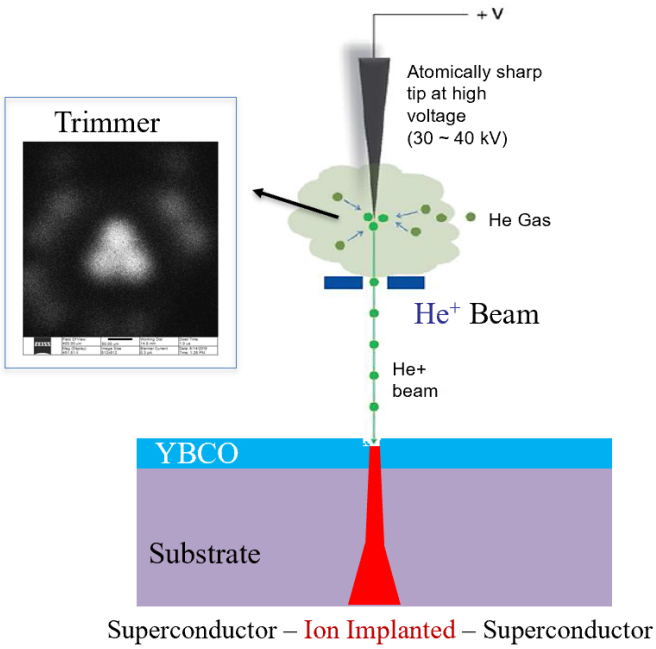

Figure 2.1: The schematics diagram of Josephson junction written by FHIB.

Conductivity is measured by increasing the voltage bias to a non linearity of the tunnel junction current-voltage curve region and capturing a high frequency dither in a Lock-in Amplifier. The spike in the middle of Fig. 2.3 is correspond to the suppercurrent at zero voltage. The peak position reveals the superconducting energy gap.

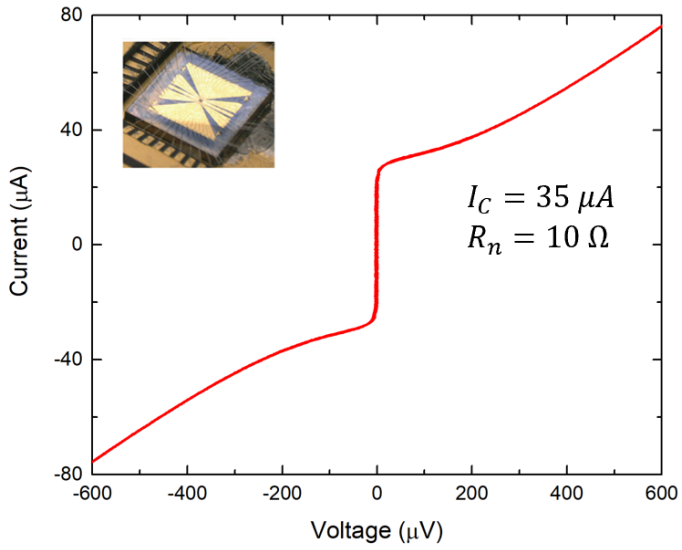

Figure 2.2: The current-voltage characteristic of a directly written Josephson Junction.

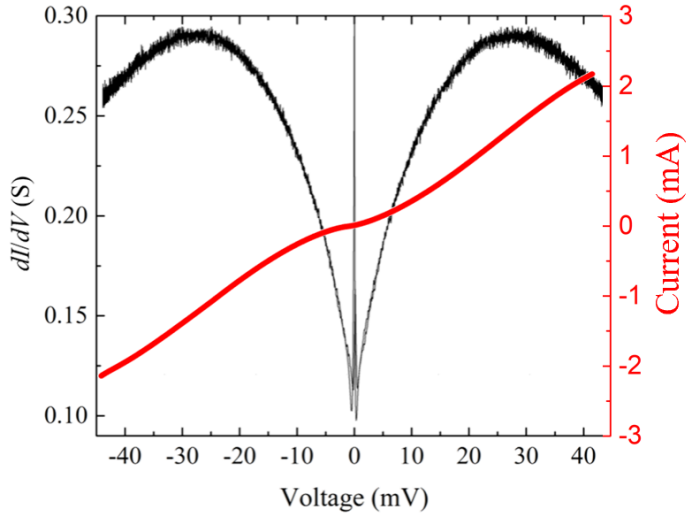

Figure 2.3: The conductance-voltage characteristic of a directly written Josephson Junction measured at a non linearity IV region.

A perpendicular magnetic field is applied to get the critical current magnetic field characteristic of a Josephson junction, which is Fraunhofer-like pattern. Fig. 2.4 shows the experiment result of a critical current modulated by the external magnetic field. The oscillation period is changed by the junction width. Narrow junction has a wider oscillation period. The maximum critical current would be obtained at zero applied field. But if a Josephson junction traps environment magnetic flux during the cooling process, the maximum critical current would deviate from zero field and appear at a non-zero magnetic filed.

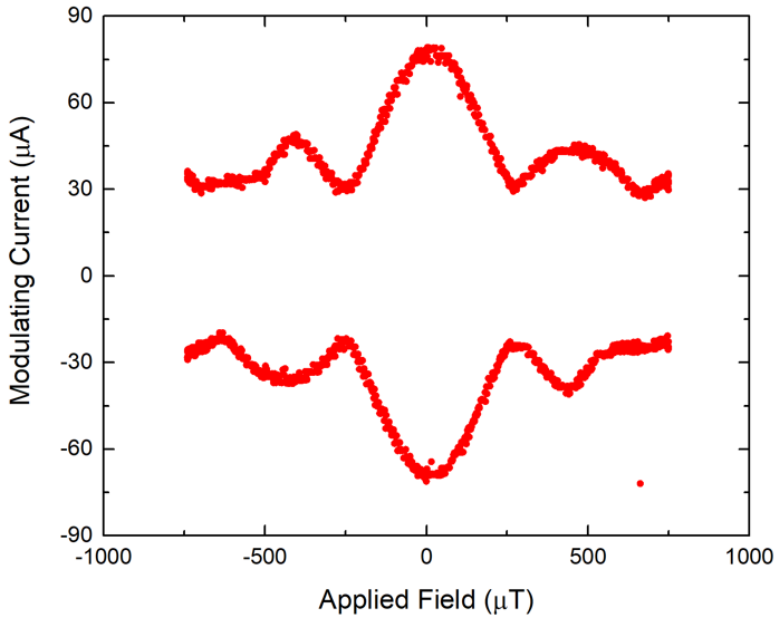

Figure 2.4: The Fraunhofer diffraction pattern of a directly written Josephson Junction.

The experiment results shown from Fig. 2.2 to Fig. 2.4 demonstrate that the FHIB technology has the ability to fabricate a planar junction with a perfect quality.

As mentioned in the Chapter 1, the junction consists of two superconductors cou-

pled by a weak link. The weak link can consist of a thin insulating barrier (known as a superconductor–insulator–superconductor junction, or S-I-S) or a short section of non-superconducting metal (S-N-S). With different dosages, the Josephson junction can be tuned from Superconductor-Normal-superconductor to superconductor-insulator-superconductor junction. Fig. 2.5 is a comparison of SNS and SIS junction as a function of temperatures. When the dosage is light, SNS junction is obtained. Reducing the temperature, the resistance at voltage state also decreases, which is expected for a metallic barrier. When the dosage is large enough, SIS junction is obtained and the resistance increases with lowering temperature, which is expected for an insulator barrier. In the application of digital logic gates, SIS junction is used due to its lower excess current and larger $I_C R_N$ product.

To test our planar ion-irradiated Josephson junctions for the nanoscale application, an experiment to measure a junction with width from 4 μm down to 50 nm has been devised. Fig. 2.6 shows a directly written nano junction. A 4 μm YBCO wire was narrowed down to nm by two insulating barriers, which restricted current to a nanowire. A Josephson junction was inserted in the middle of the wire with a lower dose. Fig. 2.7 is the results for different width junctions. The critical current is proportional to the width while the resistance is inversely proportional with the width. All of the junctions have a similar $I_C R_N$ product of about 400 μV. The constant $I_C R_N$ product implies the material properties remaining the same and no thermal damage.

This new technology provides an improvement in patterning high T_C superconductors and enables fabrication of high density nano scale superconducting circuits and

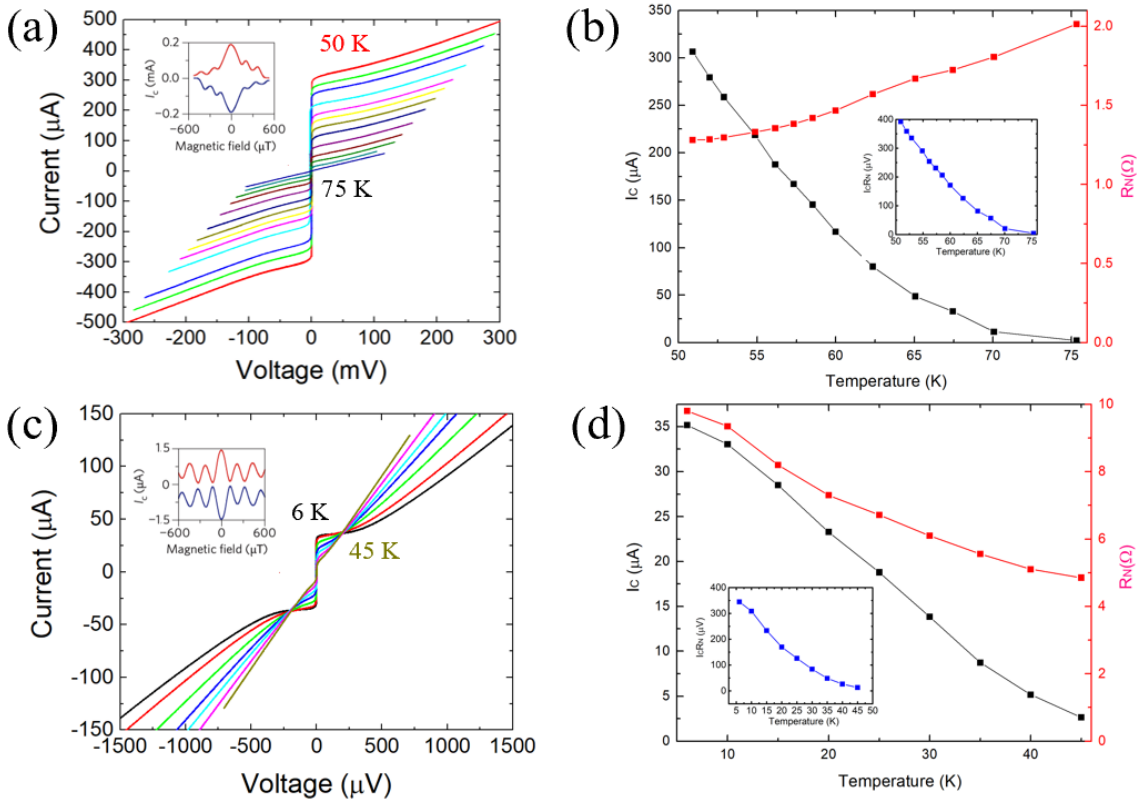

Figure 2.5: (a) The current-voltage characteristics for a SNS junction at different temperature. (b) The corresponding temperature dependence of I_C (left axis) and R_N (right axis) for this SNS junction. (c) The current-voltage characteristics for a SIS junction at different temperatures. (d) The corresponding temperature dependence of I_C (left axis) and R_N (right axis) for this SIS junction. The insert figure shows the temperature dependence $I_C R_N$ products.

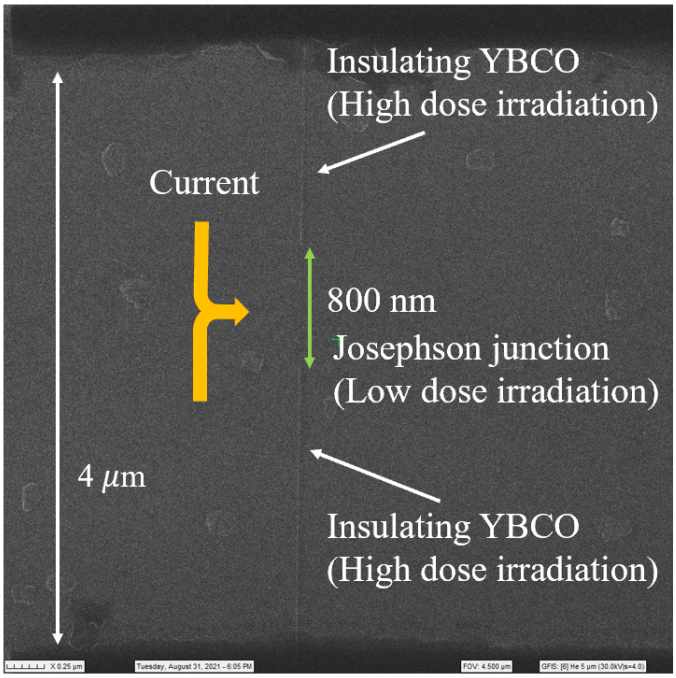

Figure 2.6: Helium ion microscope image of a 800 nm junction.

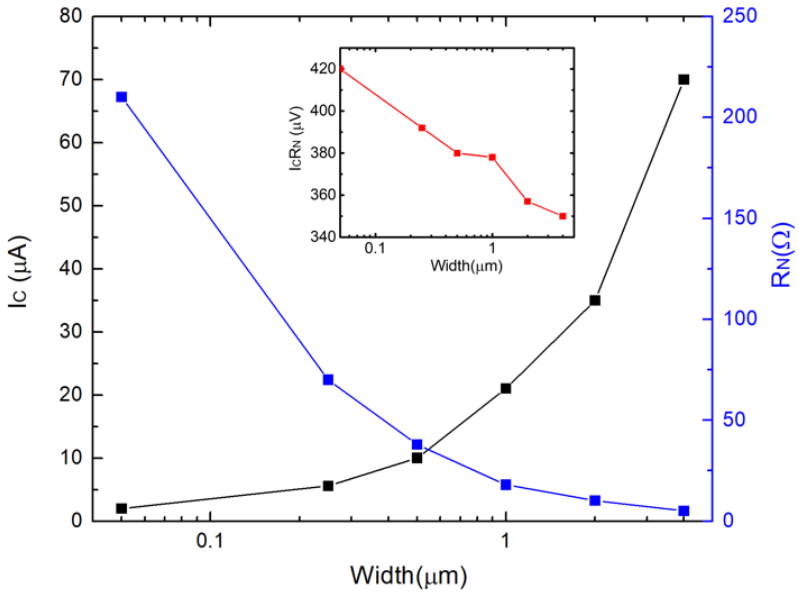

Figure 2.7: The width dependent critical current I_C (left axis) and normal state resistance R_N (right axis) of the directly written planar junctions.

interconnects.

2.3 NbN He-FIB Junctions

Moving on from the application of FHIB technology on the high T_C superconductor, we also investigated the application of FHIB to the low T_C superconductor. As shown in the Fig. 2.8, we zapped 10 nm NbN microstrip on silicon substrate with $\approx 1 \times 10^{20}$ He^+/cm^2 and successfully made junctions out of it. Fig. 2.9 - 2.11 are the primary results of a NbN zapped junction. In Fig. 2.9, the second transition temperature at 7.8 K indicates the existence of a zapped Josephson junction. The current-voltage characteristics are obtained by 4-point measurement. At 4.2 K, the critical current is about 8 μA and the normal state resistance is about 10 Ω. Fig. 2.11 shows the Fraunhofer diffraction pattern of a directly written NbN Josephson junction. The phenomenon of magnetic field dependent critical current demonstrates this zapped NbN junction works.

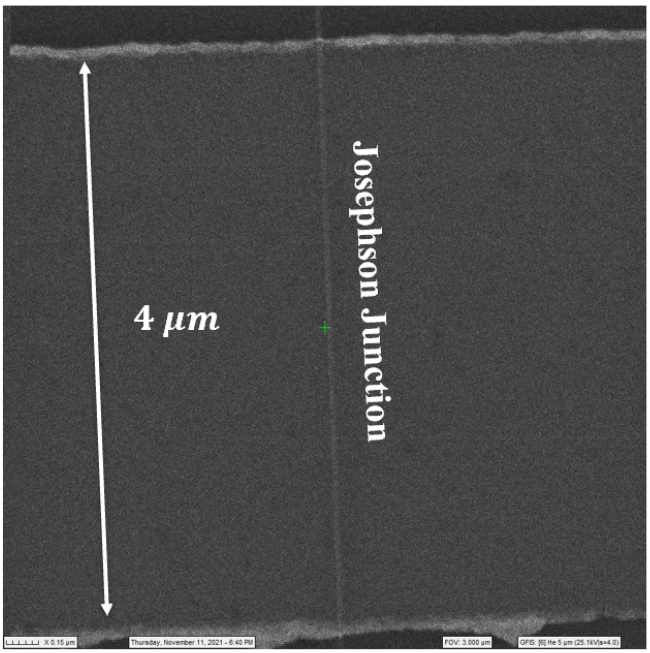

Figure 2.8: Helium ion microscope image of a NbN junction.

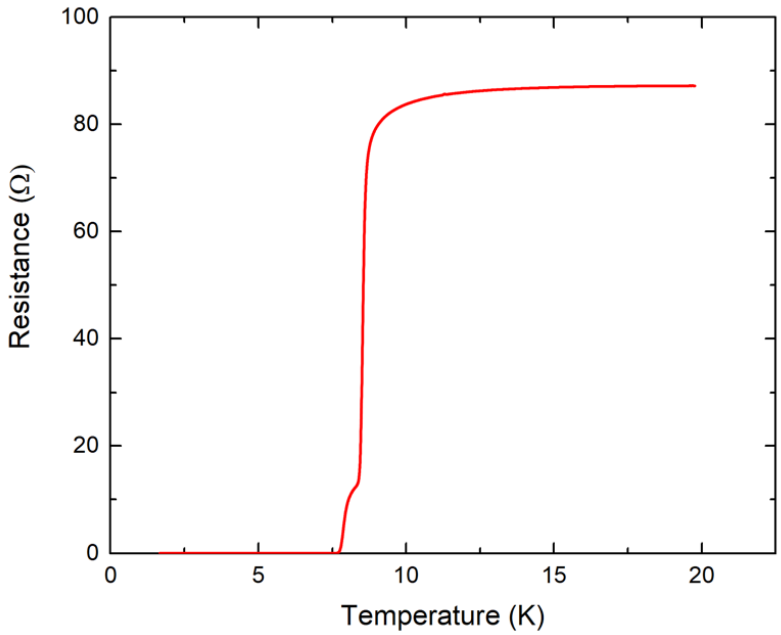

Figure 2.9: The resistance and temperature characteristic of a NbN thin film with a junction irradiated by the FHIB.

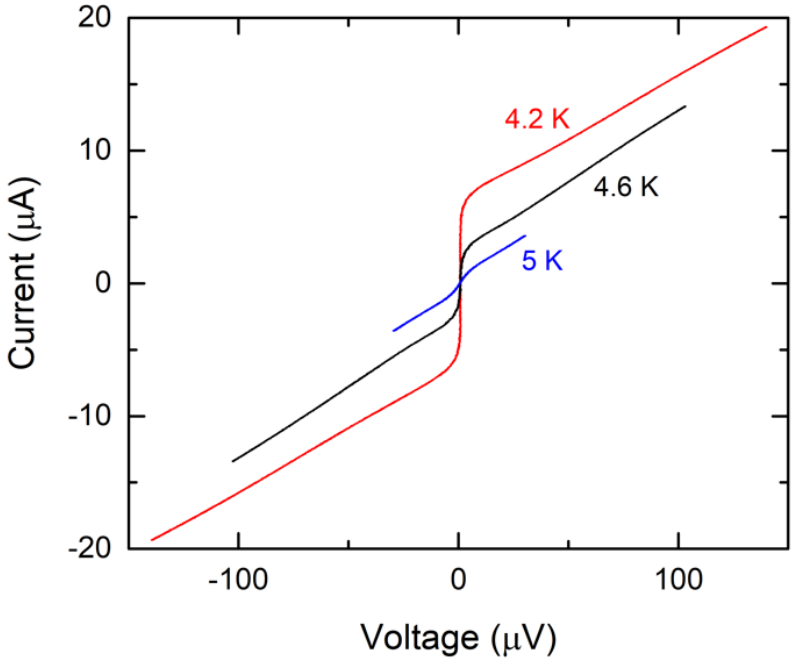

Figure 2.10: The current-voltage characteristics for a NbN irradiated junction at three different temperatures.

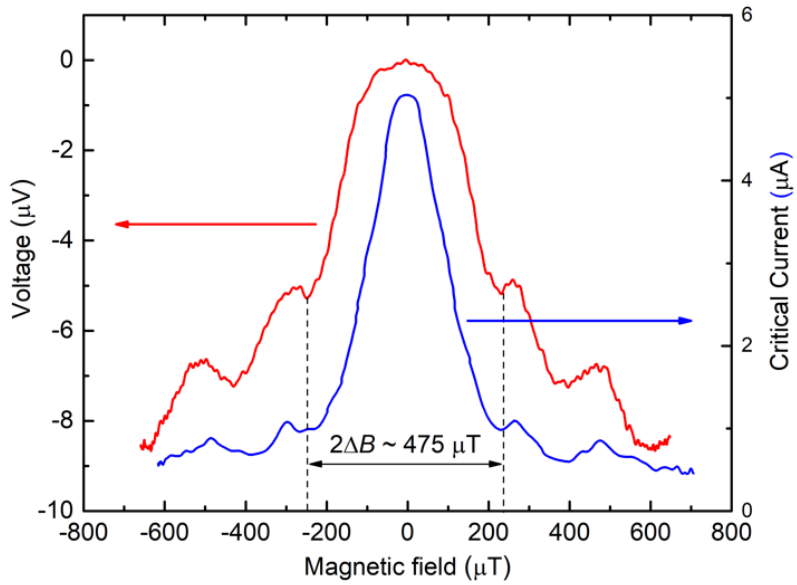

Figure 2.11: The characteristics of voltage (left axis) and critical current (right axis) vs. magnetic filed for a NbN irradiated junction.

Chapter 3

Inductance Investigation

3.1 Motivation

Superconducting computing provides a promising high performance, energy-efficient alternative to conventional computing, where power and cooling for large-scale computing systems are drastically becoming unmanageable problems- especially for centralized supercomputers and data centers. With the advantages of wide temperature operation and low cost of cooling, high critical temperature (T_C) superconductors could revolutionize future systems. The computing speed and energy cost per bit of superconducting circuits depend strongly on their inductance. Therefore, critical factors affecting the performance of superconducting devices include precise design and control of the inductance. Additionally, technological improvements in the growth patterning and the interconnection of multiple layers can further optimize the inductance of more complex digital circuits [28–30].

Recent innovations in high-quality and reproducible YBCO devices fabricated by focused helium ion beam (FHIB) irradiation [2, 31–34] could aid in the development of

high-T_C superconducting digital circuits. However, the beam energy of the FHIB is not high enough to penetrate thick films, unlike the prior-art of masked ion beam irradiated junctions [35]. Therefore, FHIB junctions are only suitable in the films with thicknesses much less than the penetration depth λ_0 ~150 nm [36]. This is particularly important because the inductance is dependant on the two dimensional penetration depth, which rapidly increases with decreasing film thickness t, $\lambda_\perp = \lambda_L^2/t$.

In previous work [37–40], the total sheet inductance of YBCO can be reduced to just ~1 pH/□ with the addition of a ground plane. However, these demonstrations utilize 300 nm to 400 nm thick dielectric layers and 200 nm to 300 nm thick counter electrodes. These structures had thicknesses larger than their penetration depth, which merits the study of the inductive properties of thinner films where kinetic inductance dominates. Therefore, in this work we experimentally measured the geometric and kinetic inductance of commercially grown single and double layer YBCO thin films grown by reactive coevaporation [41] onto sapphire wafers with thicknesses much less than their penetration depth.

3.2 Fabrication

Single and multilayer films of YBCO were grown on r-plane sapphire buffered with 20 nm of CeO_2 by Ceraco GmbH, with thicknesses much less than the penetration depth of YBCO. The single-layer film was 35 nm thick. The multilayer structure consisted of two superconducting layers separated by an insulator with the following thicknesses: 35 nm YBCO, 75 nm CeO_2 and 135 nm YBCO (from top to bottom). The insulating layer should be thick enough to prevent the leakage current from flowing through the pinholes in the

CeO_2. The total thickness needs to be kept to under 300 nm in order to ensure the film stability and to prevent cracking from happening during the deposition process. A 200-nm thick gold electrode was evaporated in-situ to make electrical contacts. In previous work, we detailed the synthesis of these multilayer films and verified that the two superconducting layers were isolated from one another with no pin-hole shorts through the CeO_2 insulator [42]. The lithography procedure is shown in Fig. 3.1.

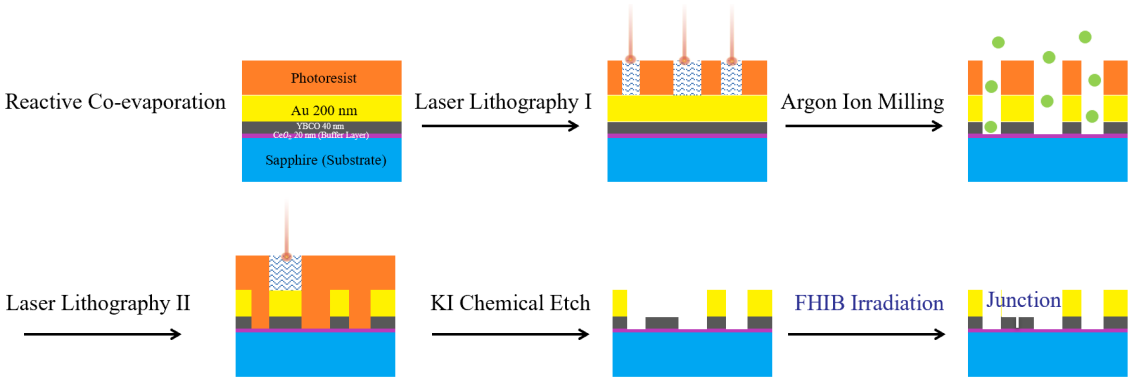

Figure 3.1: The process of fabrication.

3.3 Measurements

To investigate the sheet inductance (inductance per square), we utilized SQUIDs with electrodes for direct current injection into the SQUID loop [43]. In these devices, inductance can be accurately determined by measuring the SQUIDs' magnetic field response to the injection current [44]. We fabricated several direct-inject SQUIDs in the upper layer of the multilayer sample as well as in a second single layer sample using a fabrication method

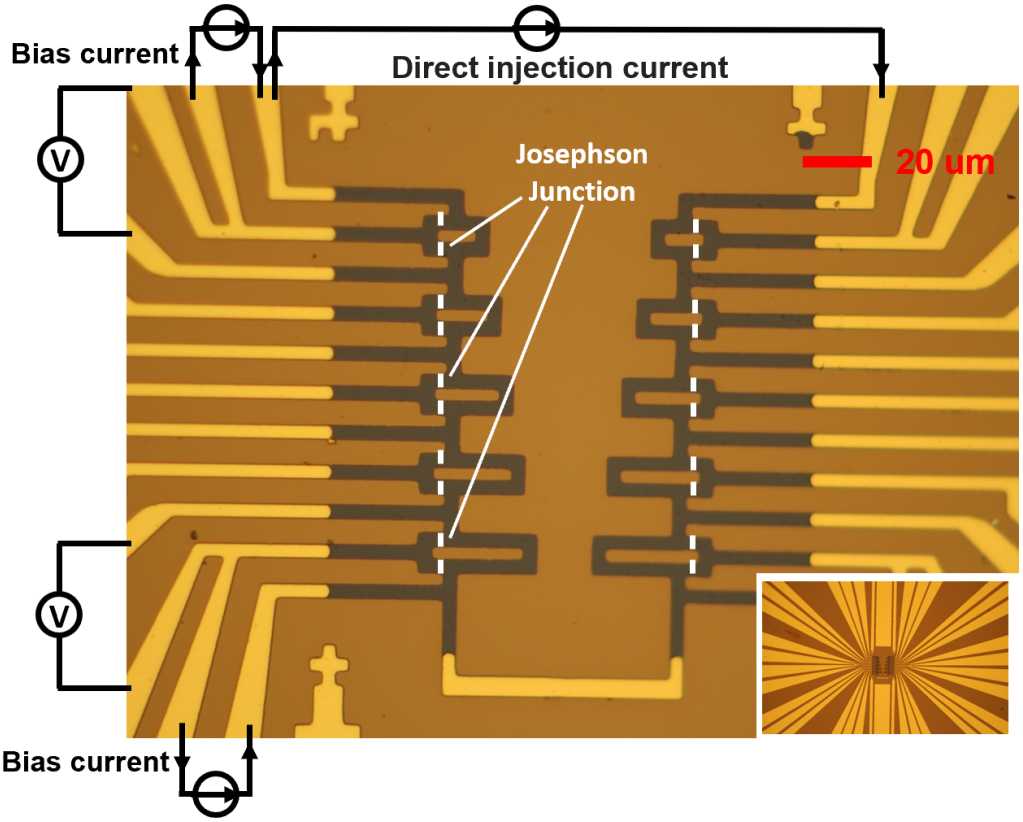

Figure 3.2: The optical microscopic photograph of YBCO SQUIDs fabricated from the multilayer film. The center dark area is the exposed top YBCO pattern, where the gold electrode layer was chemically etched away. The solid white lines represent the Josephson Junctions, which are directly written on the exposed top YBCO layer by the helium ion irradiation. The design is a symmetrical pattern. From top to down, the five SQUID loops have 5, 7, 9, 11 and 13 squares of inductance in common with the direct inject control line.

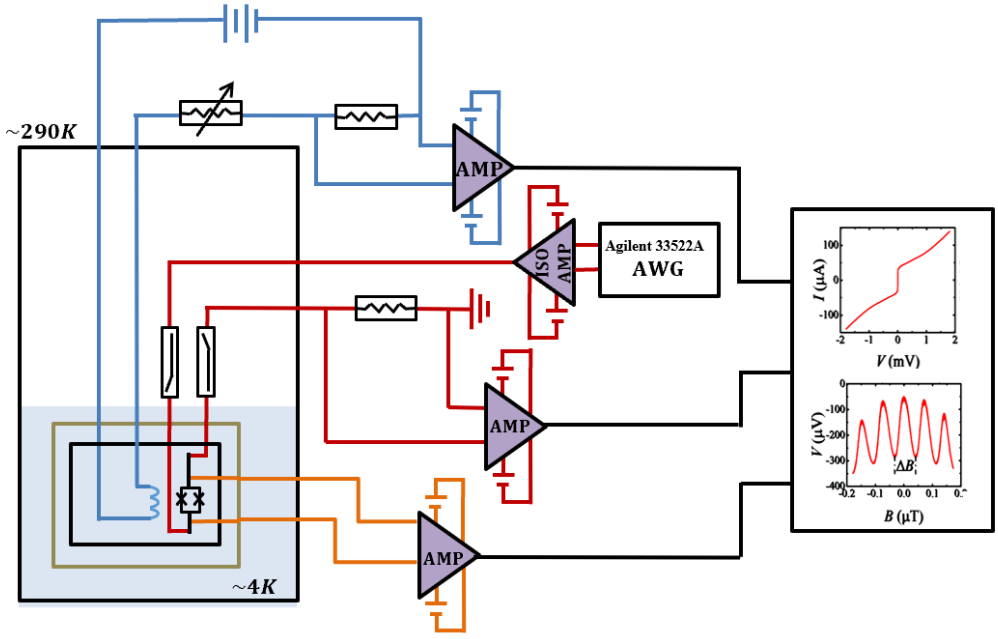

Figure 3.3: The schematic of measurement system.

detailed in previous work [45, 46]. In Fig. 3.2, the multilayer SQUID chip is shown. The area of the SQUID loop can be defined as the area of a single square times the number of squares that make up the loop. In our design, the SQUIDs have different areas of the loops with different numbers of squares: 5, 7, 9, 11 and 13, to accurately determine the sheet inductance of the material. The chips were created using laser lithography and argon ion milling in order to pattern the large-scale electrodes into both the gold and the top YBCO layer. Since there is no return current flowing through the ground plane on the bottom, the undesirable influence of magnetic fields induced by the bias currents and the ground return currents can be neglected in this situation. Subsequently, Josephson junctions were written using a Zeiss Orion Plus helium ion microscope applying dosages of about 8×10^{16} He^+/cm^2 to modify portions of the superconducting film into insulating lines that form Josephson

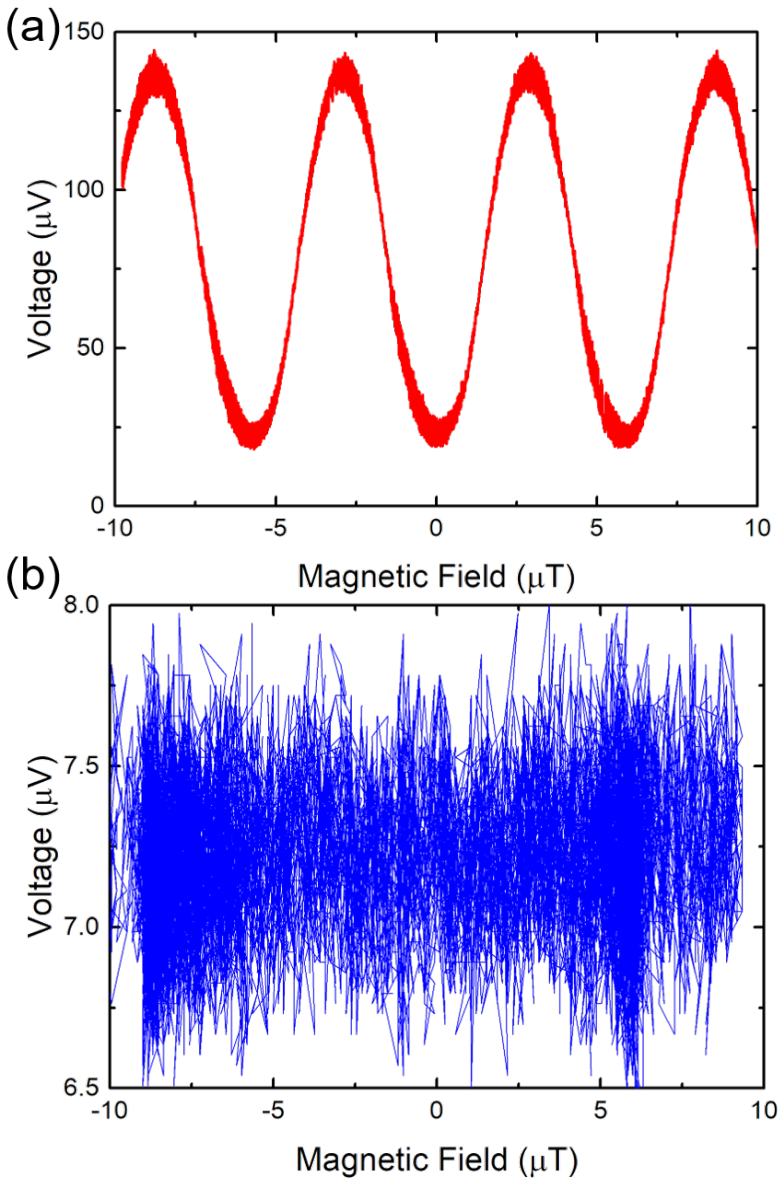

Figure 3.4: Voltage external magnetic filed characteristics for (a) single layer thin film SQUID with 135 μV modulation amplitude and (b) SQUID on multilayer film with ground plane with no voltage-external magnetic field response.

junctions [2].

The chip is wire bonded to a copper plate carrier with a diode for accurate monitoring of the local temperature of the chip. The chip carrier is mounted in an evacuated dip probe and cooled in a liquid helium Dewar with magnetic shielding for electrical measurements. As shown in Fig **??**, the cryoperm shield probe is immersed in liquid helium Dewar. The test signal is generated by an Agilent arbitrary waveform generator. Low noise Preamplifiers are used to readout the output signals. A 100 Ω resistance is in serial to calculate the current flowing through the device. A copper coil is attached to the back of the chip holder for applying an external magnetic field. In order to reduce the noise, the coil is powered by the battery. The data was recorded by a National Instruments analog to digital converter connected to a PC.

Each device was individually tested by DC biasing above the critical current (297.8 μA and 122.8 μA, respectively, for the single layer and multilayer SQUID at 4.2 K) and measuring the voltage-magnetic field (V-B) characteristics with an external magnetic field applied normal to the substrate from the backside of the sample. Fig. 3.4 (a) shows the V-B plot for the single layer device with a large modulation voltage amplitude of 135 μV. In contrast, Fig. 3.4 (b) shows the multilayer device with no detectable modulation. This demonstrates that the ground plane is superconducting and that it is sufficiently shielding the SQUIDs from the applied field.

Next, we measured the voltage response of the SQUID by injecting a current through the common injection line. The voltage modulation of the SQUIDs as a function of injection current (V-I_L) are shown in Fig. 3.5 (a) and (b) for the single layer and for the

multilayer, respectively. Both chips were operated over a large temperature range from 4 to 60 K. At 4.2 K, the modulation amplitudes were 60 μV for the single layer and 110 μV for the multilayer SQUID chip.

3.4 Results and Discussion

By comparing the magnetic field periods from the external field ΔB to the periodicity in current from the injection line I_L, we can accurately determine the injection inductance L_I and the sheet inductance $L_{\mathrm{S}} = L_I/N$, where N is the number of squares of material. The inductance value of the SQUID loop is determined from $L = \Phi_0/\Delta B$. Using a linear fit shown in Fig. 3.6, the sheet inductance is obtained from the inductance plotted against the lengths of the square loops. At the lowest temperatures, we found L_S to be 6.2 $\pm$ 0.2 pH/$\square$ and 4.3 $\pm$ 0.4 pH/$\square$ for the single and multilayer films, respectively. This demonstrates that the ground plane in the multilayer device reduces the sheet inductance by almost a factor of two.

The thickness of the patterned YBCO layer (35 nm) is thin compared to the penetration depth of a magnetic field into the superconductor. The total inductance is mainly contributed by the kinetic inductance and geometric inductance. To differentiate between the contributions from the geometric and kinetic inductance, we measured the dependence of the sheet inductance on temperature (Fig. 3.7). The data is fitted using a model of *d*-wave superconductors with impurity scattering [47] - [48]:

$$L_{\mathrm{s}} = L_{\mathrm{g}} + L_{\mathrm{k}}(0)/[1 - (T/T_{\mathrm{C}})^2], \tag{3.1}$$

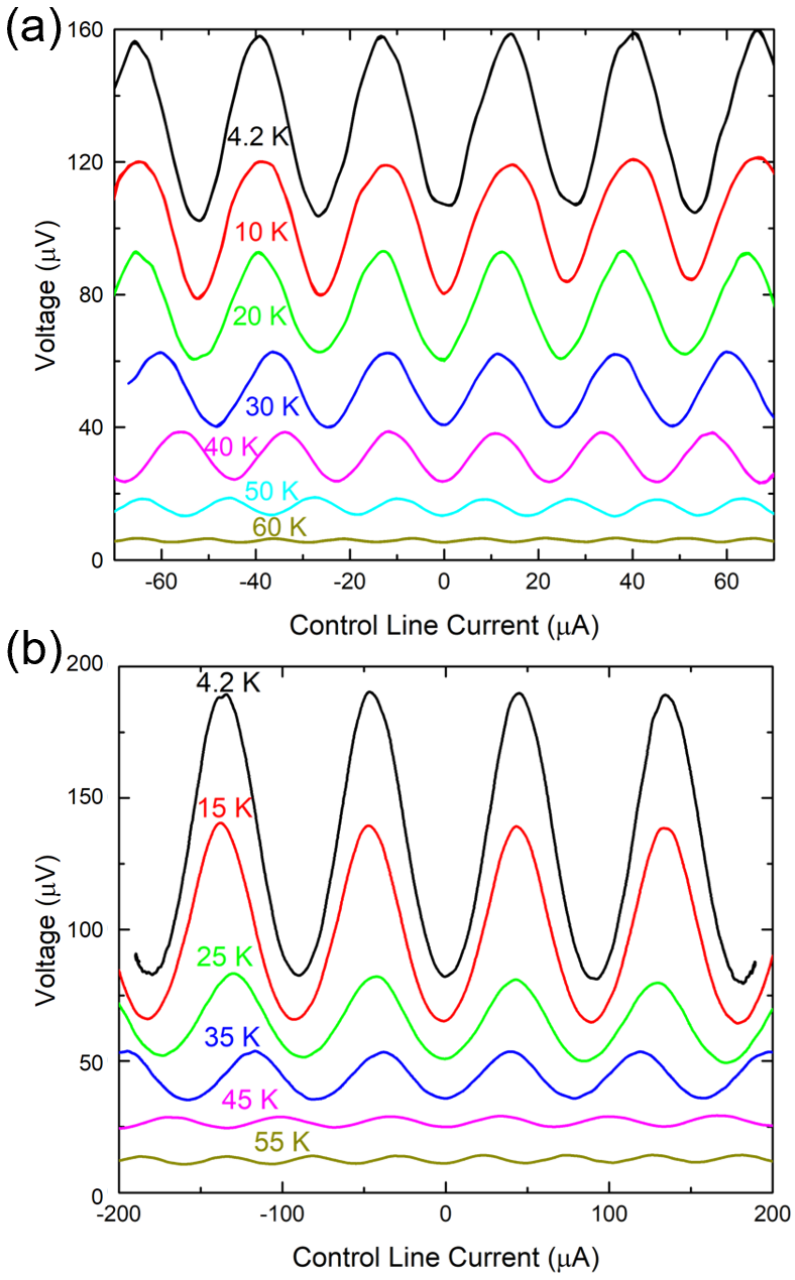

Figure 3.5: Representative (a) single layer and (b) multilayer SQUID voltage - injection current characteristics (V-I_L) for several temperatures. The voltage modulation curves are all offsetting by ~ 10 μV for clarity.

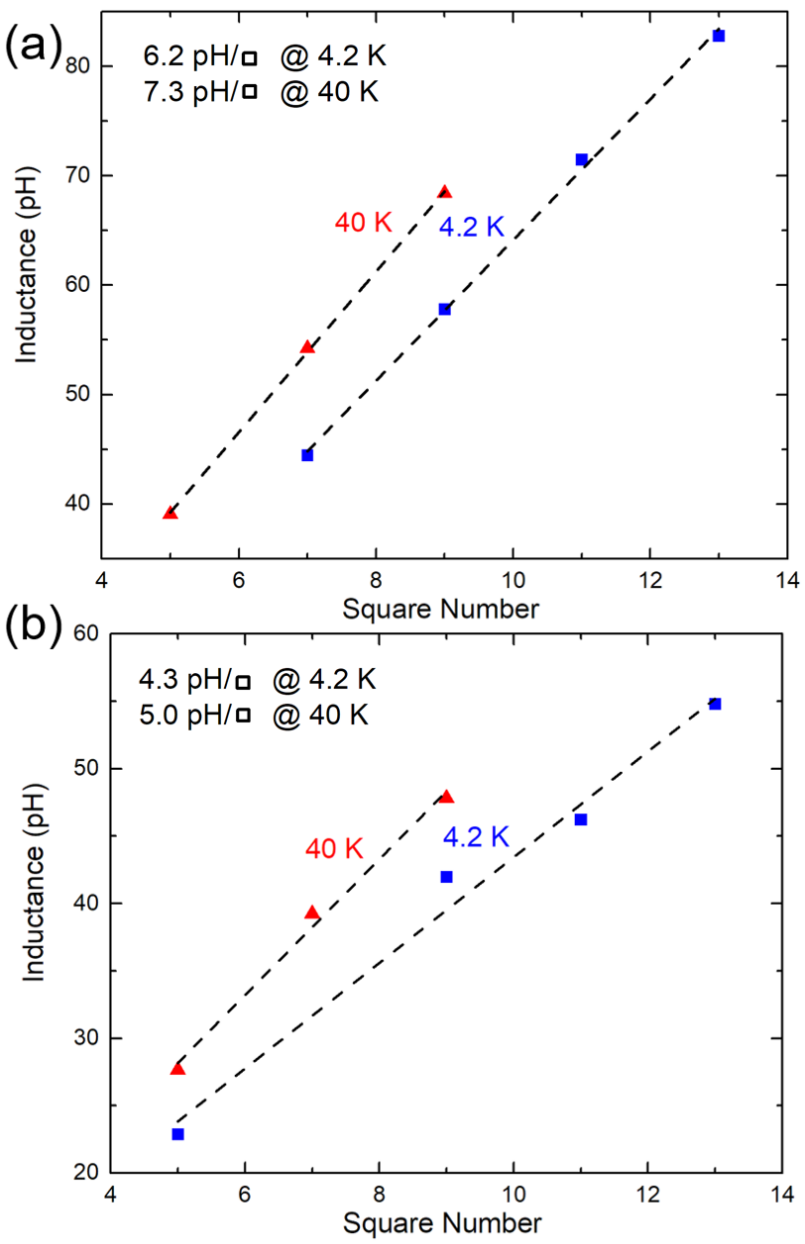

Figure 3.6: The relationship of length in numbers of squares and SQUID loop inductance for (a) single and (b) multilayer films at low and high temperature. The slope is the sheet inductance.

where L_g is the geometric inductance, L_k is the dependence of kinetic inductance on temperature, $L_k(0)$ is the value at 0 K, and T_C is the YBCO transition temperature. From a resistivity vs temperature measurement, we found the T_C taken at zero resistance for the single layer YBCO film, as well as for the top YBCO layer in the multilayer structure. The T_C values were found to be 79 K and 82 K, respectively.

Fig. 3.7 shows the dependence of inductance L_s on temperature was plotted against $[1-(T/T_C)^2]^{-1}$, linearly fitted to Eq. (6.1). From the fit we found the inductance properties of the single and multilayer devices. The geometric inductances L_g are 2.0 ± 0.2 pH/□ and 0.1 ± 0.4 pH/□, respectively, while the 0 K kinetic inductance L_k are 4.1 ± 0.2 pH/□ and 4.3 ± 0.4 pH/□. As shown in Fig. 3.7, the geometric inductance of the multilayer is much smaller than that of the single layer device, indicating that the ground plane can significantly reduce the contribution of the geometric inductance and effectively reduce the total sheet inductance with no detectable change in the kinetic inductance. As the geometric inductance refers to the magnetic energy stored within the film, the elimination of geometric inductance indicates the shielding effect from the ground plane. Moreover, the reduction of geometric inductance allows for higher device frequency of operation.

The magnitude of the temperature dependent kinetic inductance is determined by the film thickness and is proportional to the the penetration depth [49], $L_k/\square=\mu_0\lambda(T)^2/t$, where $\lambda(T)=\lambda(0)/\sqrt{[1-(T/T_C)^2]}$. The kinetic inductance becomes constant when there is no change in the penetration depth at low temperatures. For the inductance of the multilayer device, the kinetic inductance dominates, which leads to the inductance becoming constant at low temperatures. It is also responsible for the appearance of an upturn in the plot

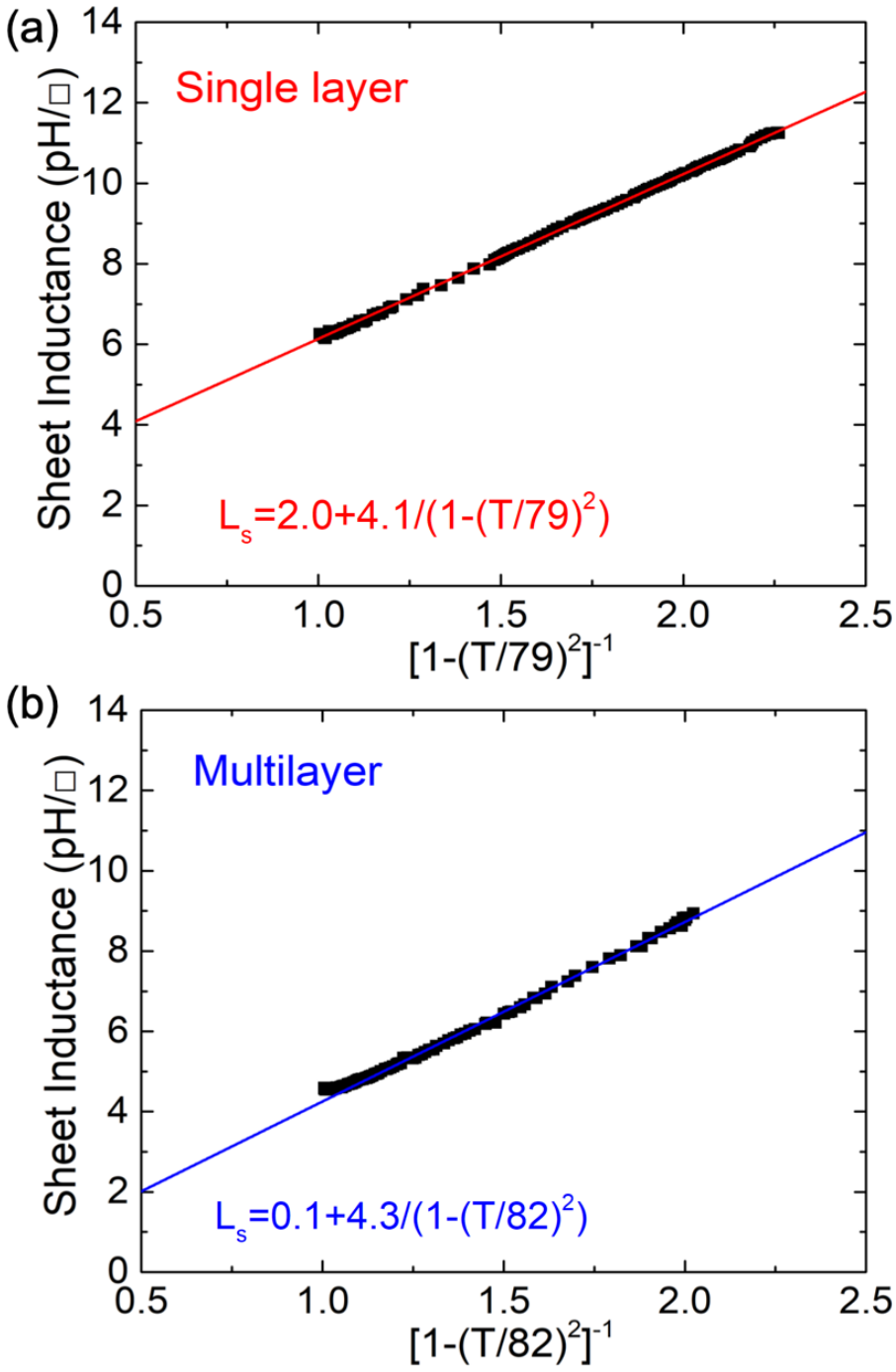

Figure 3.7: The relationship between inductance $L_{\rm s}$ and $[1-(T/T_{\rm C})^2]^{-1}$. Black squares are the measurement data. The solid curve is the result of the fit.

of Fig. 3.7 (b) at low temperatures. From the kinetic inductance, the penetration depth can be estimated to be about 290 nm. Due to uncertainties in the measurement of the film thickness, the calculated penetration depth may be larger than the actual value. The kinetic inductance responds to the superconducting state and the nondissipative kinetic energy of the supercurrent [50]. The addition of a ground plane dose not induce more energy dissipation to the device and eliminates the magnetic energy stored within the film.

3.5 Conclusion

In this work, we investigated the inductance properties of YBCO single and multilayer films grown commercially on large area wafers with thickness less than the penetration depth. The presence of a superconducting ground plane in the multilayer film substantially reduces the geometric component of the sheet inductance. This significantly relaxes circuit design constraints for single flux quanta device components requiring small inductance such as adiabatic quantum flux paramtrons [51]. Furthermore, we showed that the ground plane can serve as an environmental magnetic shielding layer for SQUID devices. This could aid SQUID [52, 53] or Josephson array [54] based applications for magnetically noisy environments.

3.6 Acknowledgement

Chapter 3 has been submitted for publication of the material as it appears in Cai H, Li H, Cho EY, Cybart SA, Inductance of YBa $_2$ Cu $_3$ O $_{7-\delta}$ Thin-Films With and Without Superconducting Ground Planes. IEEE Transactions on Applied Superconductivity. 2020

Jun 3;30(7):1-5. The dissertation author was the primary investigator and author of this paper.

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Chapter 4

High T_C Nanoscale Superconducting Quantum Interference Devices

4.1 Introduction

Superconducting Quantum Interference Device (SQUID) is well-known as one of most sensitive magnetometry. As shown in the Fig. 4.1, a SQUID consists of two parallel Josephson junctions connected in a superconducting loop. A bias current is applied to send cooper pairs tunneling through the junctions. A fundamental property of a superconducting ring is that the magnetic flux trapped in the loop is quantized in units of flux quantum. Only in multiples of flux quantum are allowed to exist in the loop.

SQUID functions as magnetic flux to voltage converter. The magnetic field applied

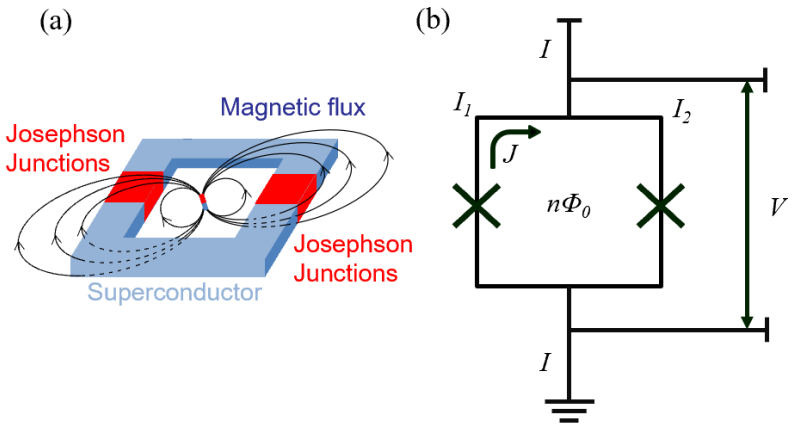

Figure 4.1: (a) The schematics diagram of a SQUID. (b) The equivalent circuit of a SQUID.

to the loop will change the phase difference across each of two junctions, which will affect the critical current of the SQUID. Fig. 4.2 (a) shows two current-voltage curves under different applied magnetic field. The critical current is periodically suppressed by the magnetic field. Due to the oscillation of critical current, the voltage is modified by the magnetic flux. One period of voltage variation corresponds to an increase of one flux quantum. The Fig. 4.2 (b) is the voltage variation for steadily increasing magnetic field. The modulation amplitude is determined by the $I_C R_N$ product.

4.2 Nano-SQUID fabricated by FHIB

The idea of shrinking the size of Josephson junction and the superconducting loop is proposed to get a smaller junction capacitance, larger resistance and smaller loop inductance, which allows to explore quantum limited sensitivity of a SQUID with a lower flux noise. NanoSQUID is sensitive enough to detect even a flip of a single electron spin. For example, it can use to detect single nanoparticle, or reading out the state of each spin-

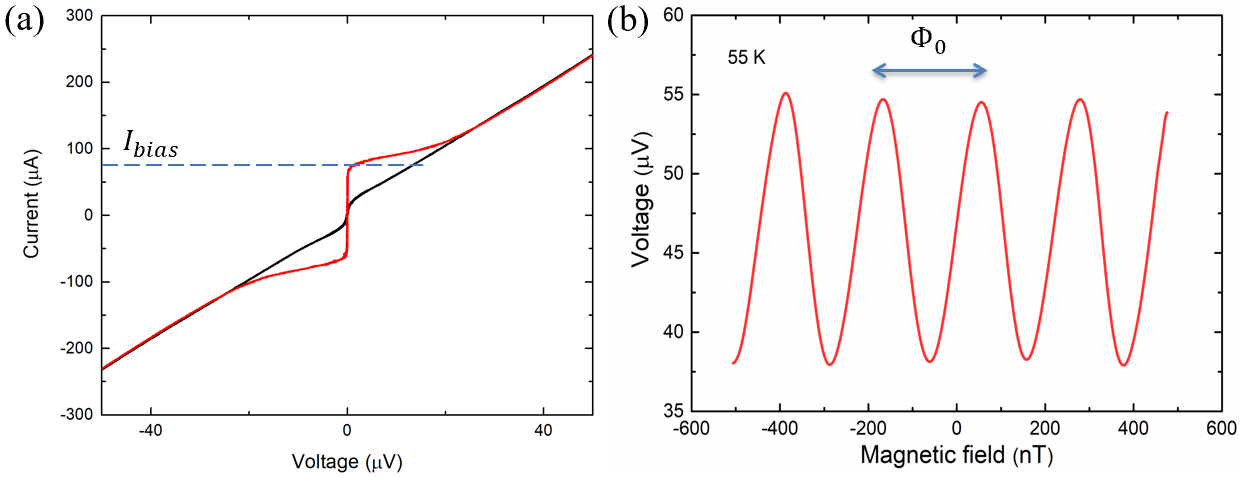

Figure 4.2: (a) The current-voltage characteristics and (b) voltage - magnetic field Characteristic of a SQUID.

based quantum bit individually other than collectively. In order to make a strong coupling, the size of a SQUID requires to be comparable to the size of the nanoparticle. Moreover, scaling down the size of the nano-SQUID can allow for cramming more devices into multiple SQUIDs circuits to customize the impedance and voltage output of transimpedance amplifiers.

4.2.1 Sample fabrication

The helium ion beam technology has the capability to do sub-10 nm nanofabrication. Therefore, we propose a novel method of patterning superconducting circuits by local modification of the superconducting material electrical properties with ion irradiation. Instead of etching away any materials, an insulating barrier is created by disorder in the material, which minimizes the damage from fabricating a nanoscale circuit. No mask is needed in the fabrication process. Two junctions and SQUID loop are made at the same

step by the self-aligned direct-writing process, which results in a fast run fabrication process with high yield.

In our experiment, the devices were directly patterned by this ion beam without any mask. Fig. 4.3 (b) is a helium ion microscope image of a nano-SQUIDs with a 400 nm × 400 nm SQUID loop and two 200 nm-width junctions. The black areas are insulating region, irradiated with heavy dose. An area irradiation is performed to make an insulating hole. In order to fabricate a nano junction, firstly, a heavily irradiation is used to make a nanowire. Then a light irradiation is applied to the nanowire to make a YBCO tunnel junction, Due to the nano-SQUID loop is too small, it is hard to inductively couple magnetic flux into a nano-SQUID. However, the coupling strength is inversely proportional to the distance. In the design, a control line is placed only a few nanometers away from the SQUID, which results in a strong coupling. This control line is defined by heavy dose-irradiated insulating pathway, which separates the control line and nano-SQUID. Magnetic flux produced by the control current flowing through the path will be effectively locally coupled to the nano-SQUIDs.

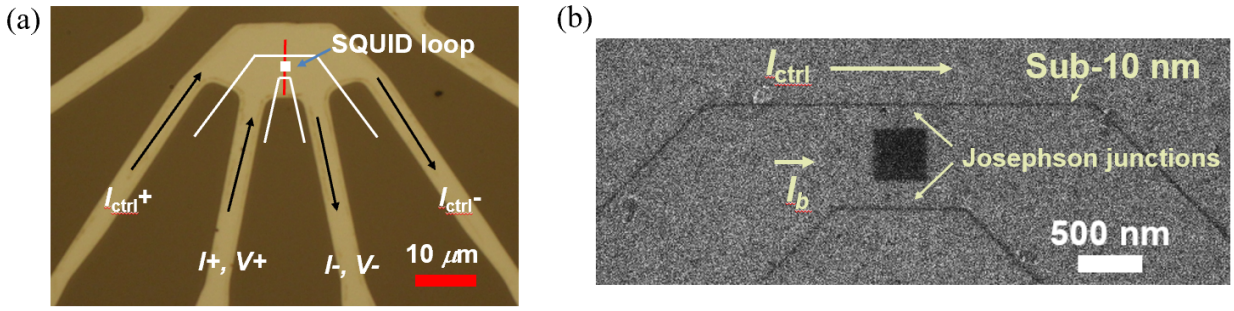

Figure 4.3: (a) The optical microscopic and (b) helium ion microscope image of a 400 nm^2 nano-SQUID.

Fig. 4.4 shows 2D and 3D AFM images of the nano-SQUID. The bright yellow parts are written by heavy dose for converting the material to insulator. Helium ions penetrate the YBCO thin film and collect in the substrate. Accumulation of helium cause bubbles in the substrate that mechanically raise the film.

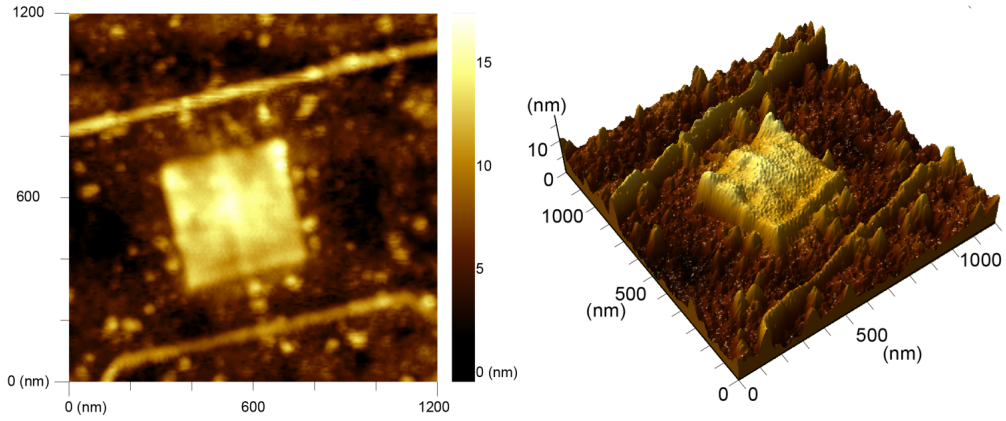

Figure 4.4: Atomic Force Microscope image of the YBCO nano-SQUID.

4.2.2 Electrical transport measurement

The device is DC biased slightly over critical current and a control current is swept through the control line to generated a magnetic field. Fig. 4.5 is the voltage response to the control current at different bias current. Apparently, it is the characteristic behavior of a SQUID.

In order to investigate the dependence of the voltage on the control current, a series of nano-SQUIDs with the square loop sizes ranging from 900 nm down to 100 nm were fabricated. In Fig. 4.6, the curves on y-axis were offset to avoid overlap in the figure.

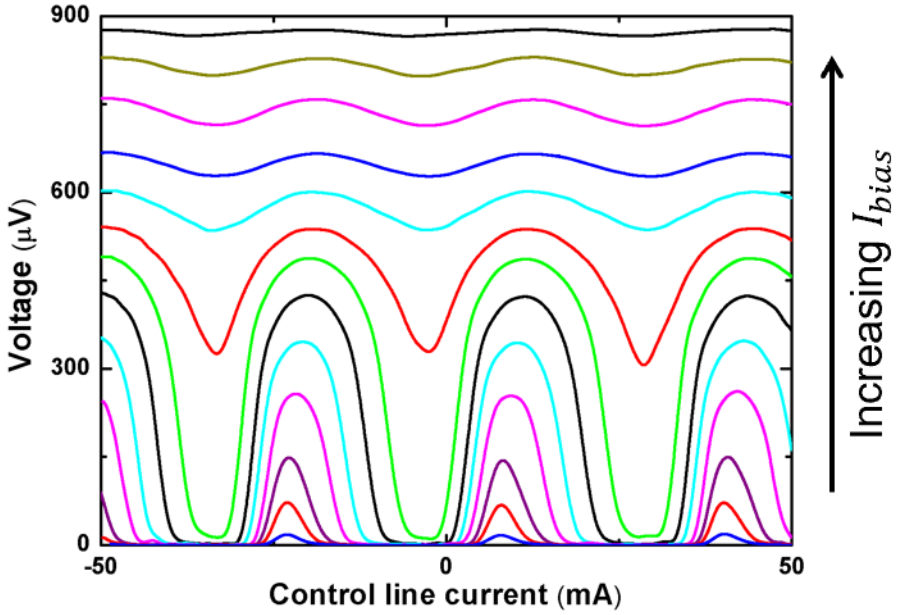

Figure 4.5: The voltage and magnetic current modulation of a 400 nm^2 nano-SQUID at a series of bias currents.

The mutual inductance between the control line and nano-SQUID can be obtained from the oscillation period, which shows positive relation with the loop size. In order to calculate the magnetic effective area, an external magnetic field is applied to the nano-SQUID. From the oscillation period of the voltage-external magnetic field characteristic, effective flux capture area can be obtained. The effective magnetic capture areas of all these nano-SQUIDs scale down from $\sim$4 μm^2 to $\sim$ 0.28 μm^2, following a square law of the square SQUID loop sizes. Therefore, not only the physics size of our device is in nanoscale, the magnetic effective area is also in nanoscale.

Continuously, we trimmed down the loop size to tens of nanometers for higher sensitivity and higher integrated density. Current - Voltage curves in Fig. 4.7 show no excess current and large $I_C R_N$ product. Both current-voltage characteristics reveal high-quality

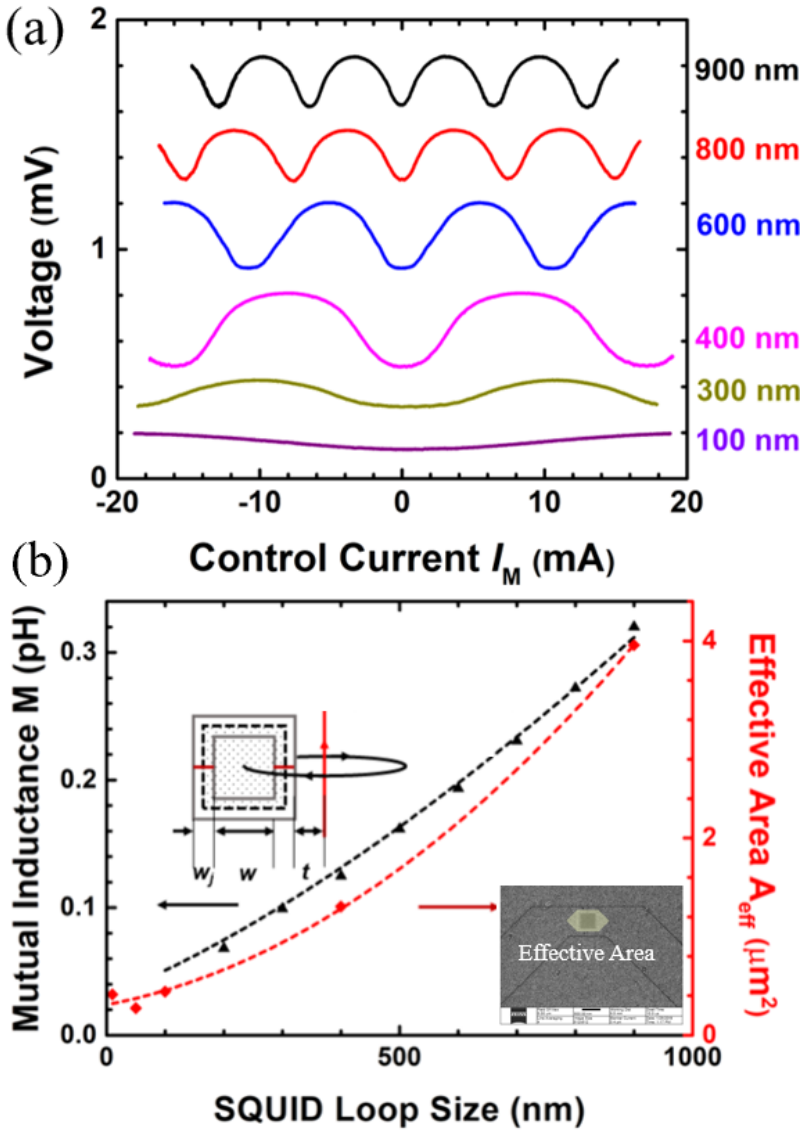

Figure 4.6: The voltage and magnetic current modulations of a series of nano-SQUIDs with varying loop size at 4.2 K. All these nano-SQUIDs have similar 200 nm junctions.

of Josephson tunnel junctions with insulating barriers. Compared to the previous several hundreds of nanometers nano-SQUIDs, even better characteristics in tens of nanometers nano-SQUIDs were observed due to a smaller inductance and a spot of high-quality film.

A Quantum Design Physical Property Measurement System (PPMS) is required to provide a strong enough magnetic field for the voltage - magnetic field modulation measurement. When nano-SQUID is statically biased, the voltage of the nano-SQUID is modulated by the magnetic field generated by the superconducting coil in the PPMS. The nano-SQUIDs exhibit ~ 0.8 mV and ~ 0.5 mV output voltages respectively, shown in Fig. 4.8, which are very high for a single SQUID output. The modulation voltage is still ~ 200 μV at 40 K.

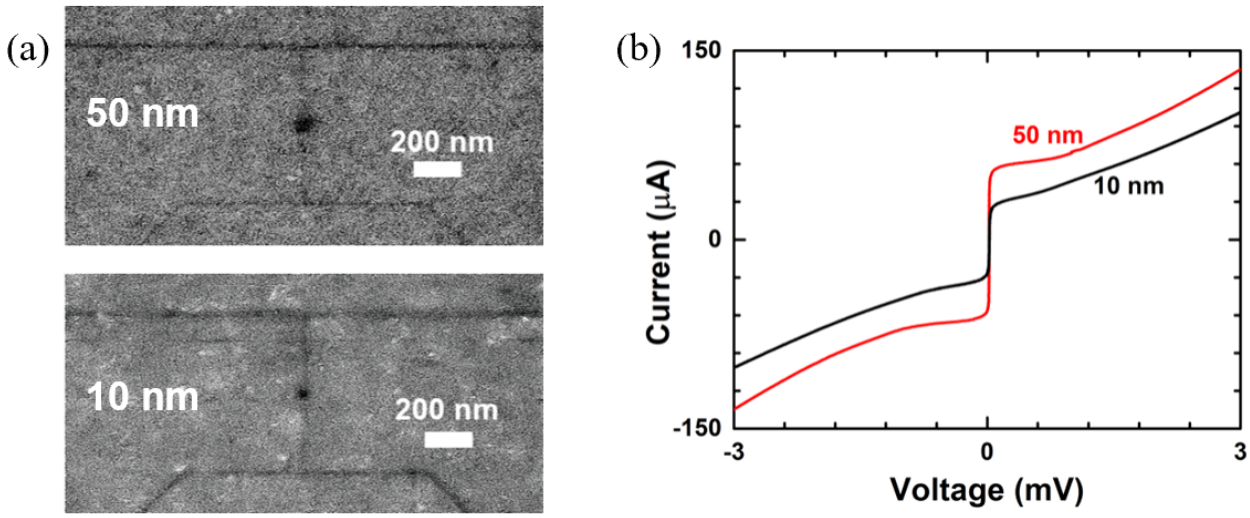

Figure 4.7: (a) Helium Ion Microscope images of a 10 nm^2 and a 50 nm^2 nano-SQUIDs. (b) the current-voltage characteristics for a 10 nm^2 and a 50 nm^2 nano-SQUID.

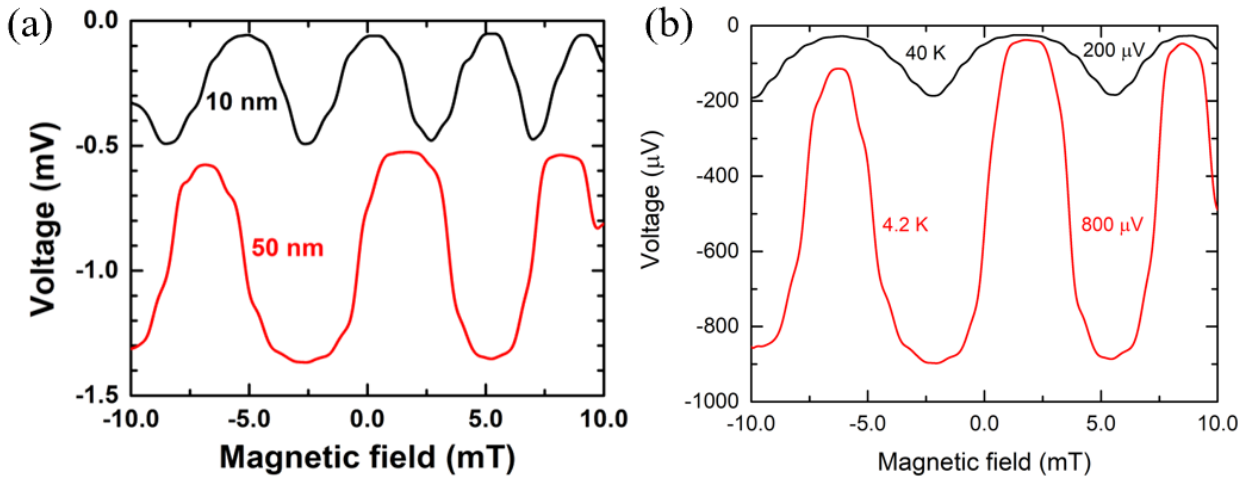

Figure 4.8: (a) The voltage - magnetic field characteristics for a 10 nm^2 and a 50 nm^2 nano-SQUID. (b) The voltage - magnetic field characteristics for a 50 nm^2 nano-SQUIDs at two different temperatures.

4.3 Nano-SQUID Transimpedance Amplifier

Considering the factors of coupling strength and output voltage, the optimal square SQUID loop size was found to be ∼400 nm. A set of temperature dependent current-voltage and voltage-magnetic field characteristics are plotted in Fig. 4.9. The electrical transport results exhibit a very high output voltage and a very wide working temperature range from 4.2K up to 50K. From I-V characteristics, nearly temperature independent normal resistance is observed. Meanwhile, ∼ 0.5 mV modulation voltage is observed in the V-B characteristics at low temperature. This large amplitude and wide operating temperature range show the capability of applications in high Tc digital logic. For example, it can be used as output drivers.

Fig. 4.10 shows the Operation of the nano-SQUID as a transimpedance amplifier. An 3 mA input current is pulsed through the control line and generates an output voltage

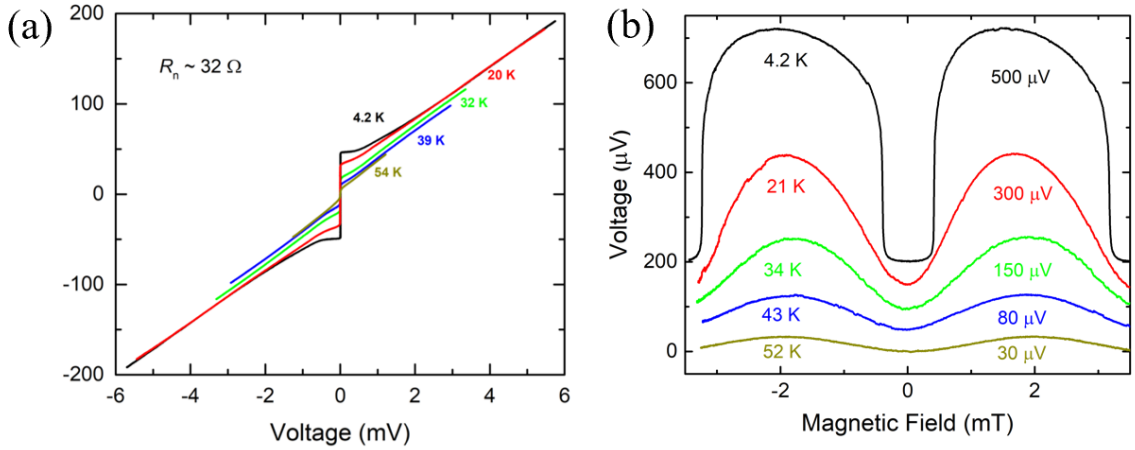

Figure 4.9: (a) The current - voltage characteristics and (b) voltage - magnetic field characteristics for a 400 nm^2 nano-SQUID with 200 nm-width junctions at different temperatures.

pulse of 0.35 mV with a transimpedance of 0.1 Ω.

In order to measure the noise characteristics of the nano-SQUID transimpedance amplifier, the whole system was placed in a radio frequency shield room. Battery powered amplifiers, low pass filters at low temperature, a niobium sheild can and three layers of mu-metal shield cans were used to reduced the external noise. The output voltage was recorded and analyzed by HP noise spectrum analyzer. The flux noise spectrum was measured by an open loop using a small signal method at optimal sensitive flux bias point. As shown in Fig. 4.11 red spectrum, large 1/f noise appears at this sensitive working point, which dominant the noise up to 100 kHz. The black curve is the background noise of the measurement system including the pre-amplifier. The flux noise at 1 kHz is $\sim 2\ \mu\Phi_0/\sqrt{Hz}$. $S_\Phi{}^{\frac{1}{2}}$ at 100 kHz is $\sim 0.3\ \mu\Phi_0/\sqrt{Hz}$.

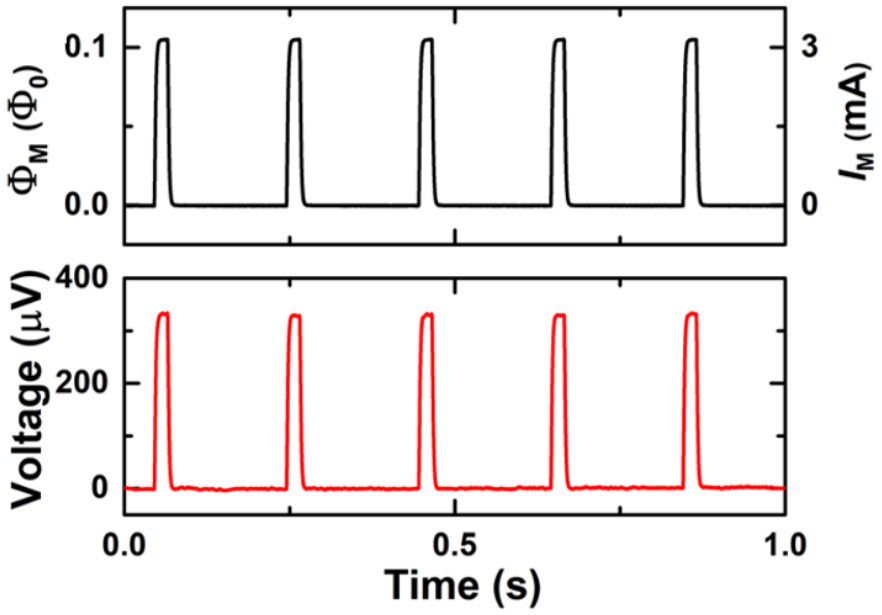

Figure 4.10: The Operation of a nano-SQUID as a transimpedance amplifier.

4.4 Nano-SQUIDs Array

These small patterns are an advance in scaling down the size of nano-SQUIDs. However, the inductive coupling strength between the integrated control line and nano-SQUID is still too weak for operation as a transimpedance amplifier. Our further studies in this effort focused on multiple 400-nm^2 nano-SQUIDs in series or in parallel, which exhibited the best combination of output voltage and inductive coupling between the control line and the nano-SQUIDs. Moreover, the voltage modulation and $I_C R_N$ product have a strong positive relation. From Fig. 4.12, the more nano-SQUIDs in series, the higher normal resistance will be obtained, which result in a larger output voltage. The critical current of the nano-SQUID array is nearly independent from the number in series.

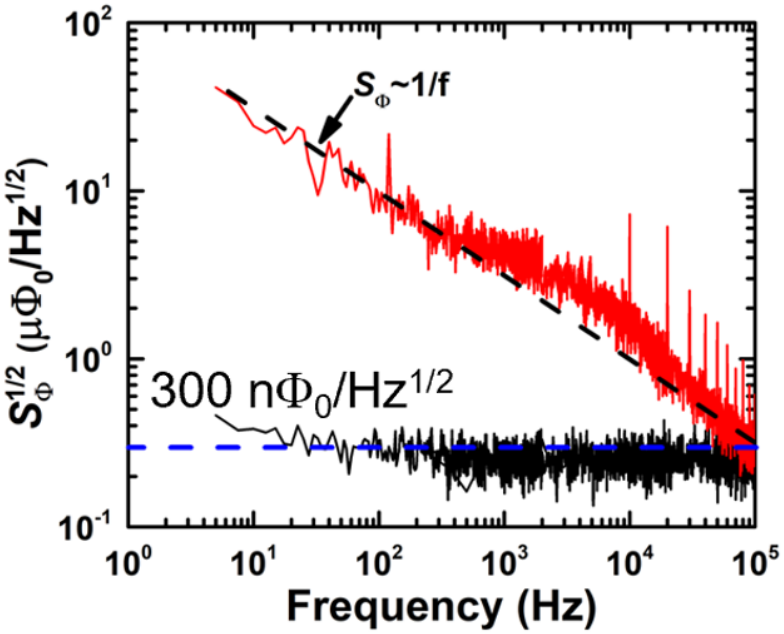

Figure 4.11: Flux noise spectrum $S_\Phi{}^{\frac{1}{2}}$ measured at a optimal working point without flux-locked loop electronics and bias reversal. The red noise is measured at the magnetic flux bias of -0.13Φ_0.

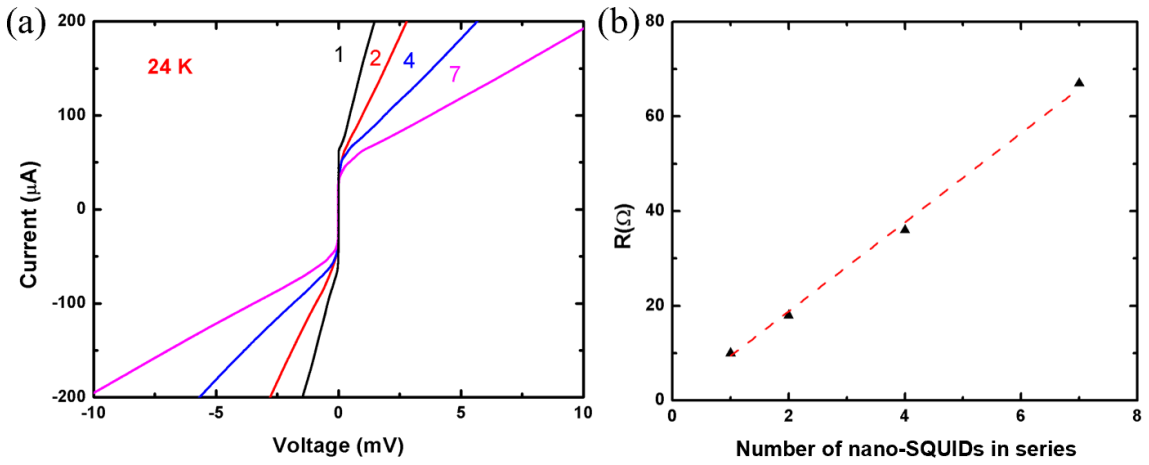

Figure 4.12: (a) The current - voltage characteristics of different number of nano-SQUIDs in series. (b) The relation between the normal resistance and number of nano-SQUIDs in series.

Fig. 4.13 shows a three-nanoSQUID in series and a three nanoSQUID in parallel. The circuit is directly patterned by helium ion beam. As shown in Fig. 4.14, mV voltage swings are observed with a wide operating temperature.

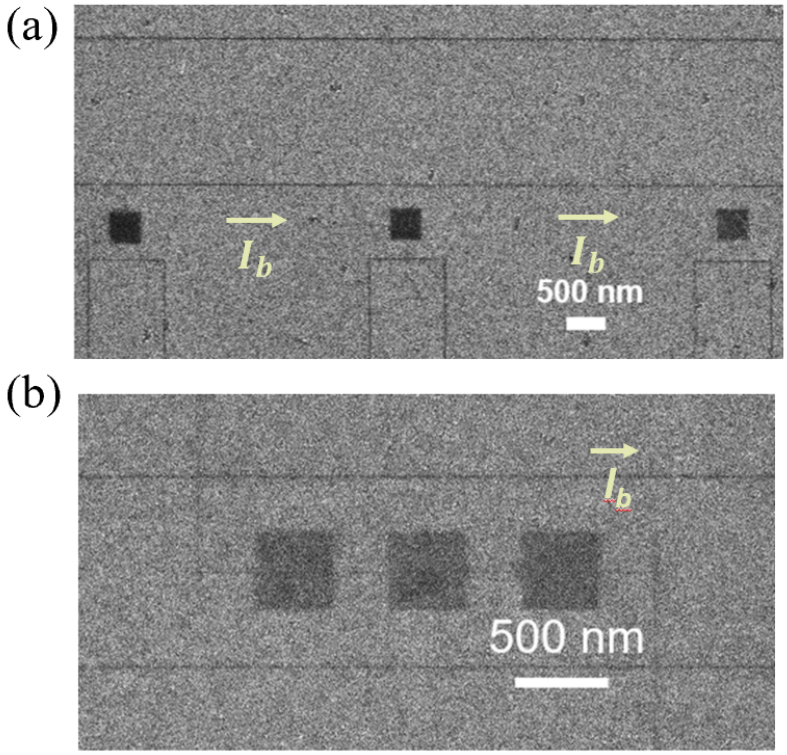

Figure 4.13: Helium Ion Microscope images of (a) three Nano-SQUIDs in series and (b) three Nano-SQUIDs in parallel.

4.5 Acknowledgement

Chapter 4, in part, has been submitted for publication of the material as it appears in Li, H., Cai, H., Cho, E.Y., McCoy, S.J., Wang, Y.T., LeFebvre, J.C., Zhou, Y.W. and Cybart, S.A., 2020. High-transition-temperature nanoscale superconducting quantum

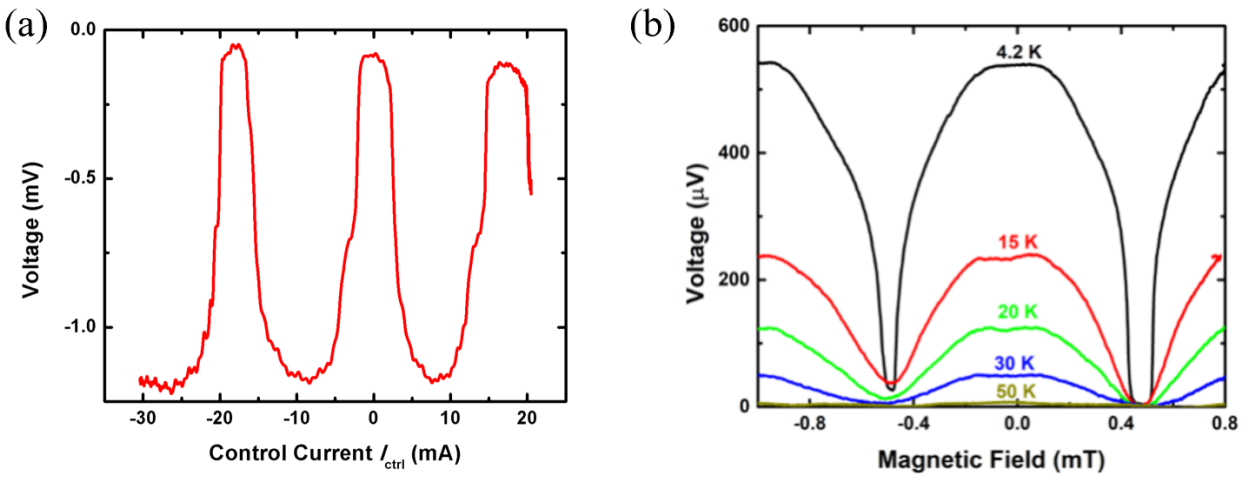

Figure 4.14: (a) The voltage - magnetic current modulation of three Nano-SQUIDs in series. (b) The voltage - magnetic field modulation of three Nano-SQUIDs in parallel.

interference devices directly written with a focused helium ion beam. Applied Physics Letters, 116(7), p.070601.

Chapter 5

High T_C Single Flux Quantum Flip Flop

5.1 Introduction

Superconducting single flux quantum (SFQ) logic circuits based on Josephson junctions have found applications in memory, mixers, digital sensor readouts, switches for routers, and high-speed computing [55], [56]. SFQ devices have low power consumption and the capability to operate at high-speed. These capabilities make SFQ prime candidates for next-generation electronics.

Most superconducting digital circuits are composed of niobium, it has a relatively large isotropic energy gap, which enables a very high operation frequency, reported as high as 770 GHz [23]. Unfortunately, the operating temperature, 4 K, of niobium-based chips, requires high power cryogenic cooling systems. To reduce size, weight, and power of

SFQ systems, researchers have been working on development of high-transition temperature superconducting (HTS) digital circuits [57], [58], [59], which can combine high operation speed and low power consumption with a higher temperature of operation. In addition, the advantages of a non-hysteretic current-voltage characteristic and no requirement for external shunting resistance, which is necessary for niobium tunnel junctions, make HTS digital circuits more appealing. Moreover, in low T_C RSFQ circuits, a resistor network is used to supply dc bias currents for the RSFQ circuits and shunting resistances are used to modify β_C value and make critical damped junctions. These resistors generate the static energy dissipation, which is ten times larger than the dynamic energy dissipation generated by the operation. While, in high T_C RSFQ circuits, the circuits don't require these resistors, which reduce the static energy dissipation and can be used in future energy efficient high-end computing systems. Moreover, the typical energy gap of high T_C superconducting material is larger than that of low T_C superconducting, which indicates a higher operating frequency.

However, HTS materials are much more difficult to synthesize and process than niobium, therefore HTS SFQ circuit processes are very primitive in comparison to niobium. In previous work, circuits were based on YBCO bi-crystal grain boundary or ramp-edge junctions with multiple circuit layers [60], [61], [28]. The fabrication process and reproducibility of HTS multi-layer junctions were complicated by the requirement that the layers must be grown epitaxialy. Moreover, large-scale integration has been technologically challenging to realize, predominately due to large deviations in junction properties. In an effort to simplify the fabrication process, a HTS SFQ was made by direct electron beam writing [62]. This work demonstrated the excellent properties of direct-write junctions, particularly in

the layout and design process, because junctions can be freely placed and are not required to be oriented along a specific direction or on a bi-crystal. Unfortunately junctions formed with electron beam irradiation are weak-link superconductor-normal metal-superconductor (SNS) junctions, with very low figures of merit ($I_C R_N$), which leads to very high bit error rates. The recent development of Josephson junctions directly written into HTS films by gas field ion sources motivates a new class of digital HTS devices with stronger Josephson barriers and improved control on device properties [2], [32], [33]. In this work, a basic SFQ Reset-Set flip-flop (RSFF) was fabricated in a single layer YBCO film by focused helium ion beam irradiation to characterize the potential of helium ion junctions for digital circuits.

5.2 Experimental

5.2.1 RSFF Design and Operation

RSFF circuit properties are related to the dynamics of quantized magnetic flux stored in superconducting loops in units of $\Phi_0 = h/2e$. When a current pulse enters the junction and exceeds the junction critical current a phase slip of 2π (across the junction) occurs and the flux quantum is passed to an adjacent loop. The duration of the phase slip is on the order of picoseconds, which allows for high speed flux propagation and an operating frequency of the circuit to reach as high as hundreds of GHz. The parameter $\beta_{\mathrm{L}} = (2\pi L I_{\mathrm{C}})/\Phi_0$ describes the circuit's dynamic behavior. Specifically, β_{L} determines the number of flux quanta that may be stored in a superconducting loop. Adjusting the loop inductance and the critical current of junction allows the number of flux quanta stored in the loop to be restricted for different purposes. The loop inductance is estimated by the

geometric structure and the sheet inductance. The sheet inductance of our YBCO films are discussed in detail in prior work [44], [29], [63].

A schematic illustrating our layout for fabrication of a helium ion RSFF device is shown in Fig. 5.1. We utilize the same approach previously used for electron beam junctions [62]. RSFF is a three-terminal circuit: "Set" port, "Reset" port and readout SQUID. The circuit includes two DC to SFQ converters (DC/SFQ) for injecting "Set" and "Reset" SFQ pulses, two Josephson transmission lines (JTL) for SFQ pulse transmission, an SFQ storage loop for storing information and an inductively coupled superconducting quantum interference device (SQUID) for readout of signal. DC/SFQ consists of an inductance and a two-junction interferometer. When an input current injects the circuit, the current across J7 (or J8) is larger than its critical current and produces an SFQ pulse forward to the JTL. JTL is a series of two-junction interferometers connected together with DC biased in parallel. The bias current is about 75% of the critical current, which is close enough to allow a junction to be triggered by a coming SFQ pulse. In order to carry an SFQ pulse from one junction to the next, the loop $\beta_L/2\pi$ is about 0.5 and cannot store any flux quantum. The SFQ pulse is transmitted through the JTL until the pulse arrives at the edge of the JTL and enters the storage loop. The storage loop consists of an inductance and a two-junction interferometer. In order to store a single SFQ pulse, the loop $\beta_L/2\pi$ is about 1.5, which allows the loop have two stable states: 1 flux quantum and non-flux quantum. Switching between these two states can be realized by trapping or releasing a flux quantum in the loop. The storage loop can receive a signal from "Set" or "Reset" port, respectively. Depending on the source of the input pulse, the loop will switch its state

and realize flip-flop. J1 is pre-biased. When an input SFQ pulse from "Set" port arrives on J1, a 2π-leap of the Josephson phase will be induced across the J1 and a positive SFQ pulse will be injected into the storage loop. This positive SFQ pulse causes a clock-wise current circulating in the loop, which will become a bias current for J2. No more SFQ pulse will be allowed to enter the loop after the storage loop has been set. The SFQ pulse from "Reset" side cannot trigger J2 until the storage loop has a flux quantum and J2 has been biased. When the SFQ pulse from "Reset" side triggers J2, a negative SFQ pulse will be injected into the loop, which will suppress the previous clockwise circulating current and release the flux quantum off the loop. When the flux quantum is released, the bias current distribution returns to the initial state and the interferometer is reset. This flip-flop process can be monitored by the readout SQUID. According to the positive or negative SFQ pulse from "Set" or "Reset" port, a voltage output pulse will be generated by the SQUID. When an SFQ pulse enters from the the "Set" port, the circulating current in the storage loop will change the magnetic bias applied to the SQUID loop then the SQUID will produce an output voltage. When the storage flux quantum is released off the loop, the readout SQUID will return to the initial state. The voltage pulse width is controlled by the time difference between "Set" and "Reset" pulse.

5.2.2 Simulation

Circuit simulation was performed using WRspice software to verify proper operation and optimization of the parameters. The parameters involved in the simulation were chosen close to the experimental values observed in the YBCO based films and junctions.

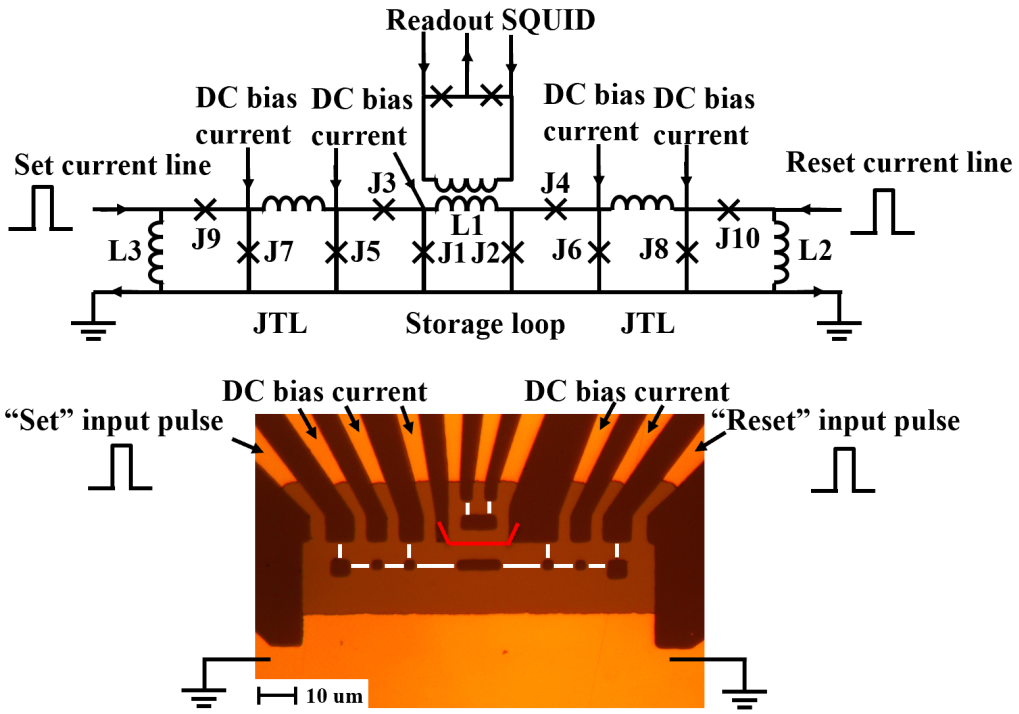

Figure 5.1: The RSFF device. (a) The circuit schematics diagram of the device. (b) The optical microscopic photograph of the device. The center orange area is the exposed YBCO pattern, where the gold electrode layer was chemically etched away. The solid white lines represent the Josephson Junctions, which are directly written on the exposed top YBCO layer by the helium ion irradiation. The red line is the insulating line written by a much higher irradiation dose, which divides the SQUID from the storage loop.

WRspice includes an intrinsic Josephson junction model, which contains parameters for the description of junction properties. In order to avoid unwanted non-return-to-zero effects from hysteretic current–voltage characteristics, SFQ circuit is based on overdamped junction with a non-hysteretic current–voltage characteristics. Due to β_C of an overdamped junction lower than 1, the junction capacitance and shunt resistance should be small. However, too small β_C will reduce the operating speed. Therefore, we choose the junction parameter close to the critical damping regime. Here the junction capacitance was set to 1.14 pF, the shunt resistance was set to 1 Ω, the critical currents of the junctions in the JTL and storage loop were set to 100 μA, the normal state resistance was set to 5.49 Ω. J3 and J4 are the buffer junctions, which isolate the two input signals and output signals and ensure that the signal transmission is unidirectional. When the direction of the signal is forward propagation, the buffer junctions are in the superconducting state. While the signal reverses propagation path, the buffer junctions change to the resistive state and block the transmission. In order to realize a single transmission, the critical currents of the buffer junctions should be smaller than the other junctions in the circuit. Here we set the critical currents of the buffer junctions to be 75% smaller than the other junctions (75 μA). The inductance in the JTL used for coupling to the neighbor junction was 6 pH. The inductance in the DC/SFQ converter is 8 pH and the inductance in the storage loop was 25 pH. The mutual inductance between the storage loop and Readout SQUID was 2.82 pH.

Fig. 5.2 shows the simulation results with a 5 GHz input pulse. The first and third traces are the DC input at "Set" and "Reset" ports. The second and fourth are the SFQ pulses converted from a DC pulse and transmitted in the JTL. The last trace is the

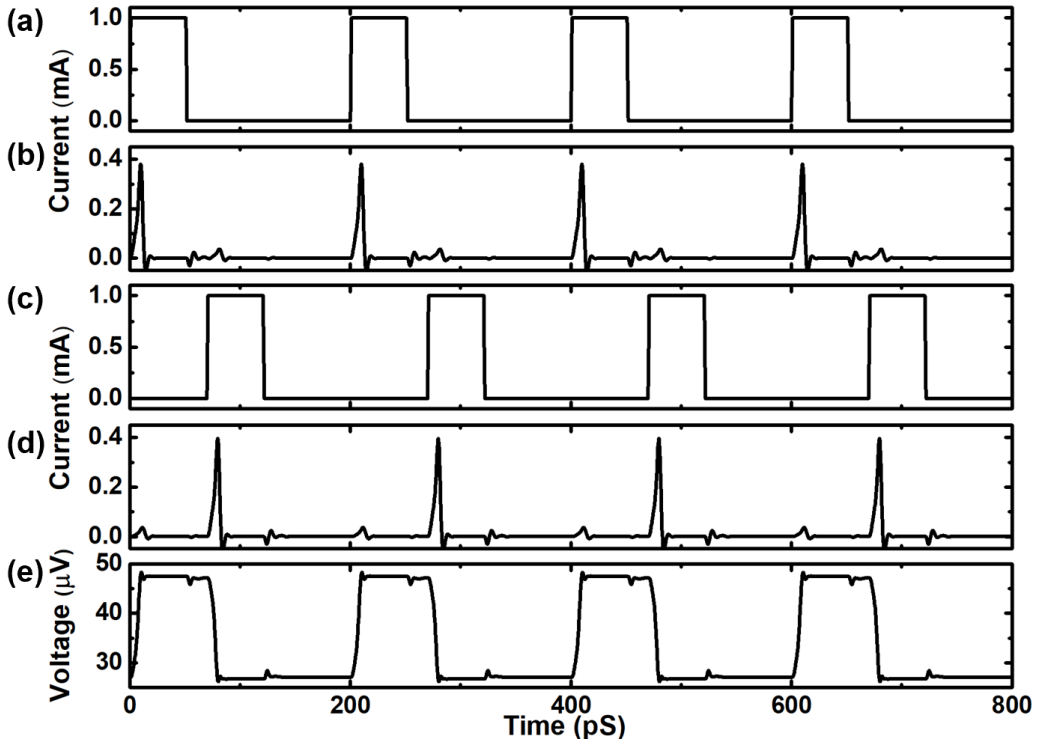

Figure 5.2: The operation of the circuit, simulated by WRspice. (a) Input DC "Set" pulse. (b) SFQ pulse generated by J7, converted from DC "Set" pulse. (c) Input DC "Reset" pulse. (d) SFQ pulse generated by J8, converted from DC "Reset" pulse. (e) Output DC pulse, readout by inductively coupled SQUID.

voltage output from the readout SQUID. The simulation shows that the input DC signal produces a magnetic flux through the inductance of the DC/SFQ converter front end. The SFQ pulse transmits through the JTL to toggle the RS flip flop. The storage loop changes state upon receiving an SFQ pulse and requires an external reset signal to revert back to the default state. Until a "Reset" signal was applied, the stored flux quantum was released and it continues to the next logic gate. The state of the storage loop was probed by an inductively coupled readout SQUID. When the storage loop holds a flux quantum, it causes a supercurrent to circulate through the loop. Magnetic field is generated by this circulating current and detected by the SQUID.

5.2.3 Device Fabrication

A 35 nm YBCO film with a top 200 nm gold layer was patterned into bridges and electrodes by photolithography and argon ion milling as shown in the photograph displayed in Fig. 1b. Using a Zeiss Orion Plus focused helium ion beam (He-FIB), junctions were directly written into the film with an irradiation dose of about 8×10^{16} He^{+}/cm^{2}. The irradiation converted narrow portions of the superconducting film into insulating lines that form the Josephson tunnel barriers. By changing helium ion beam dosages, the junction critical current can be modified. After the fabrication, the current-voltage characteristic of a typical junction and the SQUID magnetic flux-voltage characteristics were measured to find out the critical current and the flux bias point. The $I_C R_N$ product was $\sim$500 μV. The amplitude of the SQUID voltage modulation was $\sim$480 μV. Furthermore, we observed very little excess current, which was desirable for digital circuits.

5.2.4 Test and Measurement

The device was cooled in a liquid helium Dewar to ∼20 K and shielded from magnetic field by a cylindrical μ-metal inner vacuum can. The temperature can be regulated in the range from 4 K to 77 K. DC bias was applied from a 1.5 V battery in series with a 20 kΩ resistor to decrease the voltage noise. The standard error in I_C of He-FIB YBCO Josephson junctions is estimated to be 25% [46], [54]. We calculated the bit error rate by using WRspice, which takes thermal noise into account utilizing the Monte Carlo method. The bias margin is defined as the bias region in which the bit error rate is smaller than 1×10^{-10}. The bias margin is estimated to be $\sim$ 16.8% at 20 K with fixed I_C to 100 μA for all the junctions in the circuit, while it reduced to $\sim$ 6.9% when the above parameter spread considered. In the experiment, we applied 75 μA as the bias current. The two input pulses were generated by an arbitrary function generator with an activated synchronization mode on dual signal channels. The flip-flop process can be detected with the measurement of the voltage across the readout SQUID. The readout SQUID was biased nearly above the SQUID critical current I_C and tuned to a flux bias point with high sensitivity to the magnetic flux (maximum the transfer factor $dV/d\Phi_x$). The amplitude of the output voltage was determined by the SQUID voltage modulation under the on-chip magnetic field from the circulating current in the parallel RS storage loop. Fig. 5.3 shows the test result, which is consistent with our simulations. Compared to previous single layer YBCO SFQ circuits which junctions are made by direct electron beam writing [62], we get a 10 times larger output voltage because of the larger junction $I_C R_n$ products associated with helium ion Josephson junctions. Our circuit was only characterized at low frequency (a few Hz),

due to the experiment setup with twisted pairs and RC filters, though it can operate at higher frequency (up to GHz) as simulation results indicates. The high frequency signal requires to be transmitted from a microwave setup through an ultra-low loss coaxial cable or rectangular waveguide. Higher speed testing is expected in the future with upgraded measurement platform.

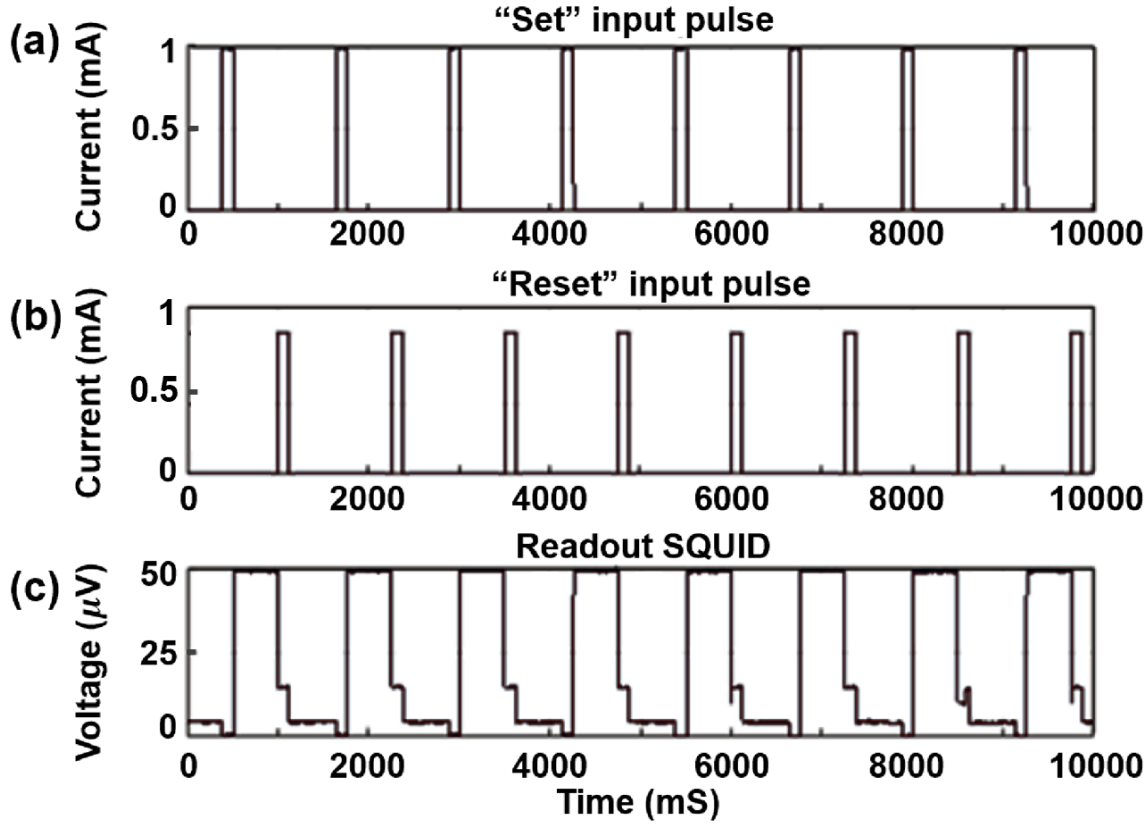

Figure 5.3: The operation of the RS flip-flop device, presented in the time domain. (a) Input DC "Set" pulse. (b) Input DC "Reset" pulse. (c) Output voltage pulse, detected by SQUID.

5.3 Discussion of results

From the simulation in Fig. 5.2, it is expected that one "Reset" pulse should cause the readout SQUID to detect a 1-step output. However, from the experimental data shown in Fig. 5.3, the "Reset" pulse causes the detection of a 2-step output, with a minor step at 0.015 mV and a major step at 0.05 mV. The minor step seen in the experimental data shown in Fig. 5.3 could arise from a larger inductance in the storage loop than that of the simulated value, which causes $\beta_L/2\pi$ to be larger than 2 and allows for multi-flux injection. In order to investigate the probability of multi-flux injecting into the storage loop, a large storage loop of inductance 50 pH has been simulated and shown in Fig. **??**. In this simulation, $\beta_L/2\pi$ is about 2.4, so two flux quantum can be stored in the storage loop. When two SFQ pulses enter the loop, the arriving "Reset" pulse can release one flux quantum and produce an output pulse with half amplitude. From the simulation, even though the storage loop can store two flux quantum at the same time, one "Reset" pulse cannot cause an output pulse with 2-step in the readout SQUID. The readout SQUID will only produce a 2-step output voltage after two "Set" pulses have been injected and both "Reset" pulses have arrived. However, in our experiment, only one "Set" pulse is applied and the output voltage returns to 0 V after a single "Reset" pulse. The simulation demonstrates that the 2-step output in our device is not caused by too large of a storage loop inductance.

A reasonable explanation for the emergence of the steps in the experimental output not seen in the simulation could be that the input current directly couples to the readout SQUID and changes its magnetic flux bias, causing a noise step in the output signal. The minor step in the output voltage pulse is caused by the mutual inductance between the

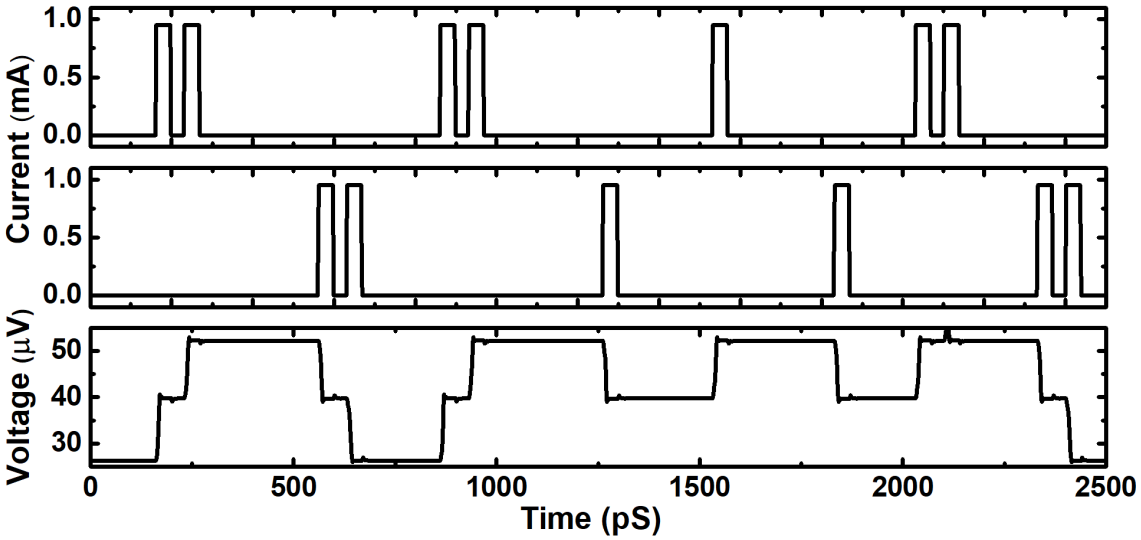

Figure 5.4: The simulation of the circuit with larger storage loop inductance by WRspice. (a) Input DC "Set" pulse. (b) Input DC "Reset" pulse. (c) Output DC pulse, readout by inductively coupled SQUID.

input current line and the SQUID. This mutual inductance is much smaller than the mutual inductance between the storage loop and the SQUID, inducing a small flux signal which the SQUID is able to detect. However, the magnitude of this detected noise signal is much smaller than that of the signal output by the storage loop, and therefore is inconsequential to device operation. As shown in Fig. 5.3, the direct coupling between the input current and readout SQUIDs appeared in the form of the minor steps in the output voltage sequence, which suggested the direct coupling did not dominate the results. Regardless of the change of the "Set" pulse, the output signal will continue to exist until the "Reset" pulse arrives. While the minor step strongly relies on the change of "set" pulse or "Reset" pulse. Therefore, the possibility of an output caused by the direct coupling between input current and readout SQUID can be neglected as well.

To firmly confirm the functionality of the circuit, we have neglected alternative in-

terpretations such as multi-flux quantum injecting into the storage loop and direct coupling between the input current and readout SQUID. Another possibility is the input current direct coupling to the storage loop. Leaking along the JTL, the input current may produce a flux quantum and directly couple to the storage loop, which then readout by the SQUID. In order to neglect this possibility, the magnetic flux and voltage characteristics have been measured to find out the input current level for one fluxon. From this test, it shows that in order to produce one flux quantum in the loop, the input current should be higher than 4 mA. In our experiment, the input current is much smaller than 4 mA, which is not large enough to directly induce a flux quantum in the storage loop. Threshold current experiments are needed for further clarification by comparing the results with that of the simulations in the future, although we ran many numerical simulations to exclude the possibility of sneaking current to the storage loop by using WRspice.

5.4 Conclusion

We have successfully demonstrated an HTS helium ion Josephson junction SFQ device. To obtain the highest operating temperature and speed with lowest bit error rates, in future work, it will be essential to continuously increase the critical current density beyond what we have demonstrated. The error rate is proportional to $\exp^{(I_{th}/I_C)}$. I_{th} is the current scale of thermal fluctuation, which is related to the thermal excited noise. At present, the device is tested at ~20 K. In this temperature, the critical currents of junctions in the circuits are much larger than the current scale of thermal fluctuation. In the future, if the device is operated at a higher temperature, the increasing of operating

temperature requires a proportional increase of I_C. Higher critical current can also increase the signal-to-noise ratio, thus lower bit error rates. The maximum speed of RSFQ devices scales roughly as square-root of J_C [23]. To raise the current, we will use thick films for the circuit. The thick films have good qualities and less defects, which can further increase the current density. The higher critical density can improve the operation speed. Additionally, the sheet inductance (especially the contribution from the geometric inductance) will also reduce in the thicker film, which will make the design requirement for low inductance much easier. With thicker film, one can get lower sheet inductance and higher I_C), thus higher operation speed and lower bit error rates. The thickness of the film is currently a limitation for the He-FIB JJs technology in general. Very thin films are required to ensure that the irradiation is even throughout the depth of the film. In the future, higher ion beam voltages could allow for thicker films, and therefore larger values of critical current. Furthermore, other types of superconducting digital circuits, with smaller critical current requirements, such as Quantum Flux Paramatrons (QFP) [64], [65] could be better suited for this process. Overall, we have shown that this junction fabrication technology is particularly useful in applications requiring flexibility in layout, scalable circuit features and elevated operation temperatures.

5.5 Acknowledgement

Chapter 5 has been submitted for publication of the material as it appears in Cai H, Li H, Cho EY, LeFebvre JC, Cybart SA. YBa $_2$ Cu $_3$ O $_{7-\delta}$ Single Flux Quantum Flip Flop Directly Written With a Focused Helium Ion Beam. IEEE Transactions on

Applied Superconductivity. 2021 Apr 1;31(5):1-5. The dissertation author was the primary investigator and author of this paper.

Chapter 6

High T_c Quantum Flux Parametron

6.1 Introduction

Energy efficiency is becoming more and more important to the current high operational rate supercomputer, as ever more powerful machines consume ever more energy. The power consumption of an exascale computer with complementary metal-oxide-semiconductor (CMOS) circuits will be more than 100 MW [66]. The reduction of power consumption generated by logic circuits is essential for future high performance computers. The past few years have been a dramatic increase in the interest in new superconducting circuit. High operation speed and low power consumption may allow the superconducting circuits to outperform traditional semiconductor logic. A major cause of this trend has undoubtedly been the push towards achieving reversible computing and practical superconducting quantum computers [67] − [68]. Superconducting digital circuits have shown outstanding performances in fast processing and adiabatic computing.

Quantum flux parametron (QFP) is an extremely energy efficient logic device,

which reduces the energy consumption of computing systems and is an attractive candidate to realize future reversible logic gates. The energy dissipation of QFP is 1000 times smaller than that of CMOS circuits. The bit energy of QFP is expected to be of the order of k_BT by adiabatic operation. Niobium-based adiabatic QFP logic gates have been investigated and discussed [51]− [64]. In their studies, the bit energy would be 20% of thermal energy at 4.2 K [69], which is much smaller than other superconducting digital circuits. An AC bias current is supplied to drive the QFP gates though microwave cables. However, niobium-based chips require high power cryogenic cooling systems. Also, the microwave interconnections between external room temperature AC signal generator and the chip placed on a 4.2 K cryo-system will cause heat inflow and reflection losses in the microwave cables, which limits the sufficient performance of the QFP gates. Motivated by this reasoning, here we have proposed a QFP circuit based on high transition temperature (T_C) superconductor (HTS) materials, which have the possibility to operate at liquid nitrogen temperature with simple crycoolers.

Most HTS junctions are intrinsically self-shunted junctions, which decrease lay-out complexity. Moreover, these HTS junctions have larger energy gaps than those of low transition temperature superconductor junctions. The higher I_CR_N product leads to an increase of the operating frequency. $YBa_2Cu_3O_{7-\delta}$ (YBCO) is the most commonly studied high transition temperature (T_C) superconducting material. Several YBCO−based Josephson junctions technologies have been studied, including bicrystal grain boundary, step-edge junctions and c-axis sandwich junctions with multiple-layer structures [60], [61], [28]. However, it's difficult to fabricate high quality HTS multilayer. The variations resulting from

the fabrication process limit the complexity of feasible circuits, which require a low spread of junction parameters. Recently, ion−irradiated junction technology has been studied which shows the ability to pattern Josephson junctions in monolayer with excellent uniformity [2]− [33] and has potential to build a high-density large-scale architecture with nano structure directly writing [70]. This technology simplify fabrication processes and improve the performance of HTS circuit. In this chapter, we fabricated a HTS QFP in a single layer YBCO film by focused helium ion beam (FHIB) irradiation. Superconductor−insulator metal−superconductor (SIS) junctions are formed with FHIB irradiation to obtain a higher characteristic voltage and lower bit error rates.

6.2 Experimental

6.2.1 Operation principle of QFP logic

QFP logic operates with an extremely low bit energy per switching event due to no requirement of DC bias currents and zero static power consumption. The minimum switching energy can be close to $k_B T \ln 2$, which is known as the Landauer limit. The equivalent circuit of a QFP is shown in Fig. 6.1. It is composed of two symmetric rf superconducting quantum interference devices (SQUIDs) shared a same inductive load L_{Load}, and powered and clocked by an AC excitation current I_{ex}. An excitation current line is set close to the two superconducting loop and magnetically couples with the two loop inductors. When excitation current I_{ex} flows through the excitation current line and generates $0.5\phi_0$ excitation magnetic flux to each superconducting loop via magnetic coupling, the QFP is activated. A small input current I_{in} flows through input line to the inductive load. I_{in} is bidirec-

tional and determines which logic state the gate switches. Either junction J_L or J_R will switch depending on the polarity of I_{in}. As a result, depending on the direction of I_{in}, an SFQ is stored in either left superconducting loop or right superconducting loop. As the magnetic flux inside a superconducting loop increases from 0 to $0.5\phi_0$, the QFP potential energy evolves from a single well to a double well, which is the fundamental requirement for encoding and storing binary logic states in the QFP. Output current I_{out} is generated through L_{Load} due to junction is switched and an SFQ is held in the loop. The polarity of I_{out} represents the logic state of the QFP. The output current I_{out} flowed from the ground to the superconducting loop with an SFQ in the right loop is taken to be logic state 0 and I_{out} flowed from the superconducting loop to the ground with an SFQ in the left loop is logic state 1. The amplitude of the output current depends on the the L_{Load} and the junction critical current, which is almost independent with the input current amplitude. Ideally, the QFP has ability to amplify any arbitrarily small input current.

The behavior of a QFP gate with quasi-static states can be analyzed from the equilibrium conditions of the circuit Hamiltonian function. Ideal operation of the QFP is obtained when the parameters of the QFP are symmetric: inductances $L_{\text{xL}} = L_{\text{xR}} = L_x$, $L_L = L_R = L$, coupling coefficients $k_L = k_R = k$ and junction critical current $I_{\text{CL}} = I_{\text{CR}} = I_C$. The potential of the QFP included magnetic energy and Josephson energy can be expressed with normalized circuit parameters [71], [72]:

$$U = E_j[\frac{(\phi_x - \phi_-)^2}{\beta_L} + \frac{(\phi_{in} - \phi_+)^2}{\beta_L + 2\beta_q} - 2cos\phi_- cos\phi_+] \tag{6.1}$$

where $E_j = I_C\Phi_0/2\pi$ is the Josephson energy; Φ_0 is the flux quantum; $\phi_- =$

$(\phi_L - \phi_R)/2$ and $\phi_+ = (\phi_L + \phi_R)/2$ represent the logic state of the QFP; ϕ_L and ϕ_R are the phase different across the junction j_L and j_R, respectively; $\phi_x = 2\pi k\sqrt{L_x L} I_x/\Phi_0$ and $\phi_{in} = 2\pi L_q I_{in}/\Phi_0$ are the normalized excitation and input flux; $\beta_L = 2\pi L I_C/\Phi_0$ and $\beta_q = 2\pi L_q I_C/\Phi_0$ are the normalized loop and load inductances, which determine the hysteretic or nonhysteretic nature of the QFP and also determine the dynamic energy dissipation and the profile of the potential energy during a switching event. When β_L and β_q are small, it is possible to realize adiabatic operation, which can potentially reduce the bit energy to the order of thermal energy. The potential energy shape changes periodically between a single-well shape and a double-well shape as the excitation flux increases. When ϕ_x changes from $2\pi n$ to $2\pi(n + \frac{1}{2})$, the potential energy evolves from a single-well shape into a double-well shape, in which case the number of SFQ stored in each superconducting loop becomes different with each other. When ϕ_x changes from $2\pi(n - \frac{1}{2})$ to $2\pi n$, the potential energy evolves from a double-well shape to a single-well shape, in which situation the number of SFQ stored in each superconducting loop is the same. During the activation of the QFP ($\phi_x = 2\pi(n+\frac{1}{2})$), if ϕ_{in} is applied, the potential energy changes to an unbalanced double-well potential, which favors the state with the lowest potential energy. For $\phi_{in} > 0$, the potential minimum appears in the right well resulting in positive ϕ_+ which represents logic 1. For $\phi_{in} < 0$, the left well has the lowest potential resulting in negative ϕ_+ which represents logic 0. For $\phi_{in} = 0$, the logic state is stochastically determined due to the symmetric double-well shape of the potential energy.

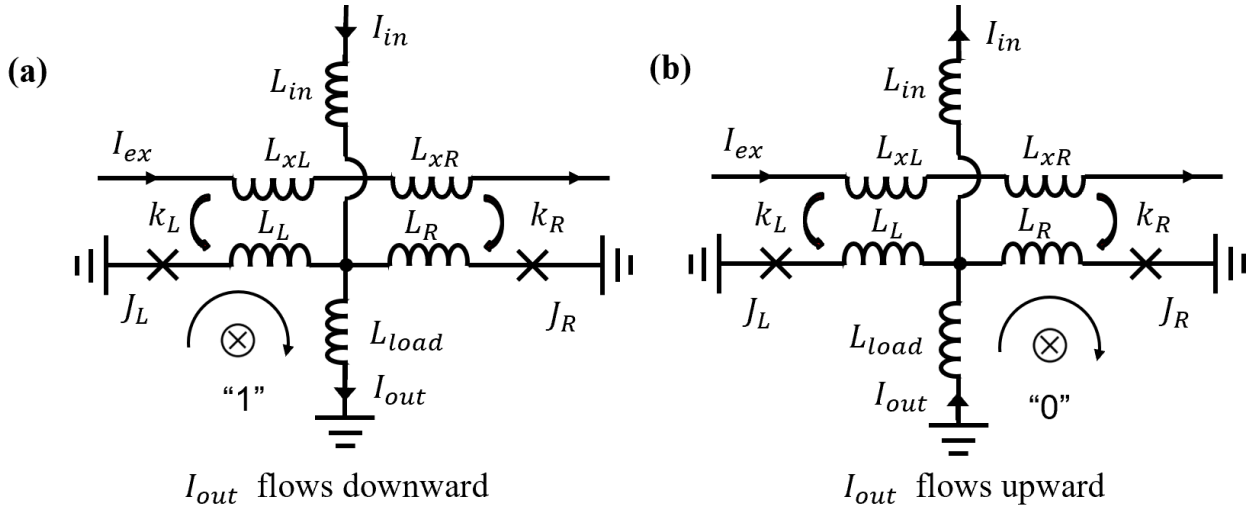

Figure 6.1: Schematic of the QFP circuit. After the circuit is activated, when the input current is positive, the excitation flux will induce a phase flip on j_L and admit an SFQ into the left superconducting loop. A positive current will flow through L_{Load} and QFP is switched to logic 1 state. Conversely, when the input current is negative, J_R will undergo a 2π phase flip and induce an SFQ in the right superconducting loop, a negative current is generated in L_{Load} and QFP is switched to logic 0 state.

6.2.2 Device Fabrication

In this experiment, commercial 40-nm-thick YBCO thin film grown on cerium oxide buffered r-plane sapphire by reactive coevaporation was used. For electrical contacts on YBCO chip, a subsequent 200-nm-thick Au layer was thermally evaporated in-situ. Laser photolithography and Ar ion milling were performed to prepattern large-scale electrodes on both Au and YBCO layers for helium ion irradiation and electric-transport measurements. Following prepatterning, a second photolithography and KI chemical etch were used to remove the Au layer and uncover the intended YBCO area for FHIB direct writing. Helium ion irradiation was accomplished by a Zeiss Orion NanoFab He/Ne ion microscope with 32 keV He^+ ions. The irradiation caused disorder in the YBCO lattice and converted YBCO from superconducting to insulating. A moderate ion dose of

6×10^{16} He^+/cm^2 was applied to create a very narrow insulating barrier for YBCO in-plane superconducting-insulating-superconducting (SIS) junction. Comparing to superconductor-normal metal-superconductor (SNS) junctions, SIS junction has very little excess current and larger damping resistances, which would increase the intrinsic switching speed of the junctions and result in a further reduction in energy dissipation [73]. A heavy dose of 3×10^{17} He^+/cm^2 was used to create a insulating line between adjacent excitation current line and QFP loop. Due to the excitation current line just a few nanometers away from the QFP loop and the magnetic field strength inversely proportional to the distance, a higher coupling coefficient k was obtained. Fig. 6.2 schematically illustrates the circuit schematic and chip optical photograph. In order to avoid unwanted magnetic coupling, a in-plane ground plane is implemented between excitation current line, input current line and readout SQUID. The excitation current line and input current line are nearly vertical. A dc-SQUID biased in the voltage state is used as a current sensor to readout the output current flowing through L_q and generated a large output voltage. The load inductance of the QFP is magenetically coupled to the dc-SQUID and the dc-SQUID exhibits a voltage transition when the QFP switches to "0" or "1" state. The operation point of the dc-SQUID is set to the maximum transfer factor $\mid \frac{dV}{dI_B} \mid$ point (I_B is the magnetic current in the SQUID loop), where is most sensitive to external magnetic current and can continuously and linearly convert the output current of QFP into output voltage.

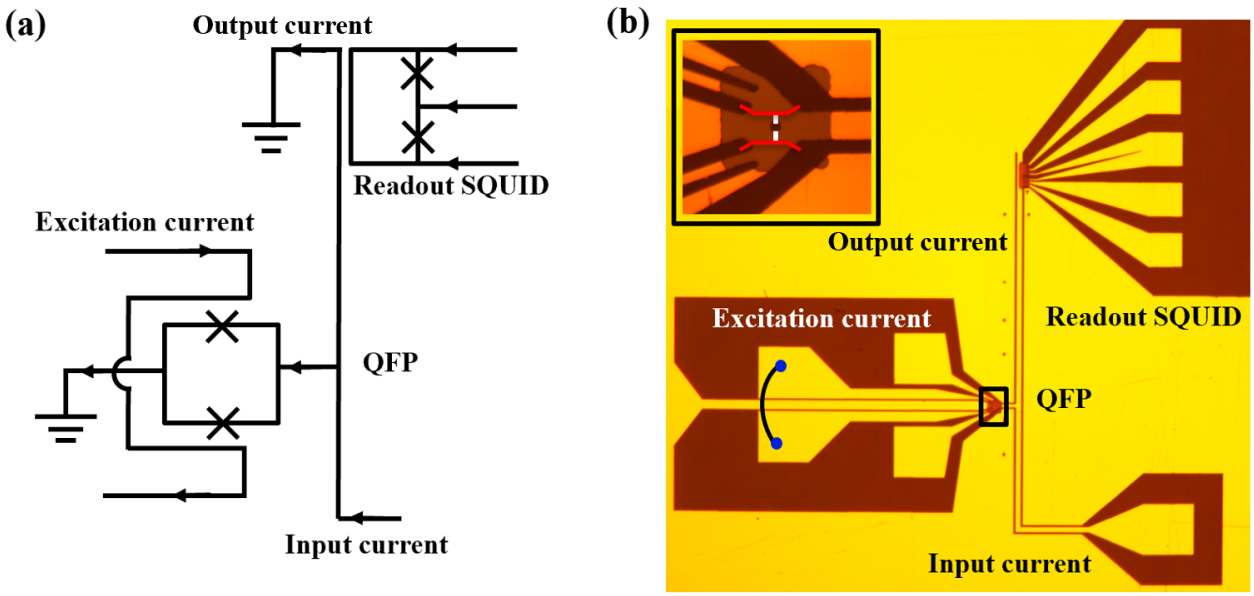

Figure 6.2: The QFP device. (a) The circuit schematics diagram of the device. (b) The optical microscopic photograph of the device. The inset orange area is the exposed YBCO pattern, where the gold electrode layer was chemically etched away. The solid white lines represent the Josephson Junctions, which are directly written on the exposed top YBCO layer by the helium ion irradiation. The red line is the insulating line written by a much higher irradiation dose, which divides the QFP from the excitation current. Two excitation current lines are shorted by wire bonding.

6.2.3 Simulation and Measurement

Fig. 6.3 shows the simulation results for a QFP switching operating using WR-spice. QFP gate is driven by the excitation clock pulses whose amplitude is determined by ϕ_x to produce $0.5\phi_0$ in the QFP loop. The inductance values of L, L_x, $L_{\rm in}$ and $L_{\rm Load}$ are extracted from the circuit layout by InductEx. These inductances define how the potential energy changes and how output current generates during a switching event. Therefore, the inductances should be optimized in terms of the dynamic energy dissipation, the operation margin and the current gain $I_{\rm in}/I_{\rm out}$. In order to decrease the energy dissipation, both β_q and β_L should be small. However, considering to the operation margin, which should not be narrower than $\pm 25\%$ for the gate robustness, β_L requires to be small, whereas β_q requires to be larger than 1.4 [74]. Moreover, as the output current depends on the β_q and a small β_q (below 0.2) results in dramatically reducing output current [51], the $L_{\rm Load}$ should be chosen in accordance with the Josephson junctions critical currents to guarantee a large enough output current and current margin for the practical operations of the logic gates. Therefore, considering all the above, β_L should decrease whereas β_q should make a trade-off between energy consumption, operating margin and current gain. For the high-speed operations, critically damped Josephson junctions with the McCumber parameter $\beta_c \approx 1$ are used in this circuit. The critical currents of Josephson junctions are about 120 μA. A small bidirectional input current $I_{\rm in}$ is set to be $0.3I_{\rm C}$. When the excitation current is activated, QFP gate switches at every cycle of the input current and generates an output current. The different polarity of output current represents the different logic state of the QFP gate. Comparing to the input current, the output current is amplified with a current

gain $I_{\text{in}}/I_{\text{out}}$ about 2.5, which is a which is a feature of QFP gate. The energy dissipation can be evaluated to be approximately 4 aJ per clock cycle at 5 GHz operation by integrating the product of the excitation current and the voltage over time.

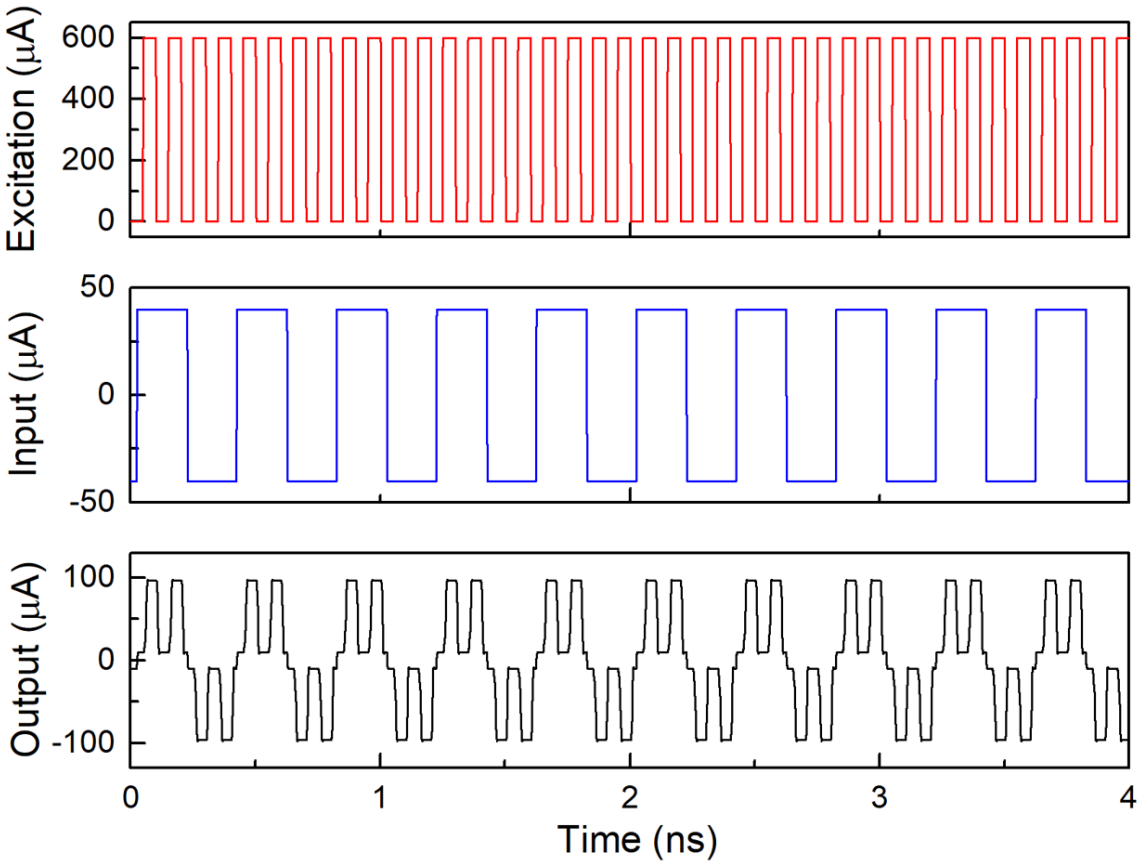

Figure 6.3: Transient analysis of the QFP operating at 5 GHz. $\phi_x/2\pi \approx 0.48$,$I_C \approx 120\mu$A, $I_{ex} = 600\ \mu$A, $I_{in} = 40\ \mu$A, k ≈ 0.4, $\beta_L \approx 1.1$, $\beta_q \approx 3.5$.

After simulation and fabrication, the device was loaded on an evacuated dip probe with three-layer μ-metal magnetic shield vacuum can in a liquid helium Dewar and measured at 25 K. The input and excitation currents were generated by an arbitrary function generator with a 10 kΩ resistor placed at each input terminal to suppress voltage noise from room temperature to low temperature. Low noise battery-powered pre-amplifiers were used

to measure the output voltage. All the instruments and Dewar were in a RF shielded room and connected to a general ground to reduced noise. A low-speed experimental QFP switching operation presented in the time domain were shown in Fig. 6.4. The output voltages from dc-SQUID, which corresponded to the states of QFP gate, were observed when the excitation current was activated and the polarity switched when the input current inverted. Theoretically, the QFP was capable of amplifying an arbitrarily small input current. However, due to the effects of fabrication nonuniformity and noises, in this experiment, we applied an input current of ± 40 μA. The similar transient waveforms between the experiment and the simulation indicated that the circuit operated correctly, where the gate generated an output after the excitation current was activated.

6.3 Discussion of results

A small offset was observed in the output voltage. There are two effects that might induce this offset. One is the parasitic coupling in the actual asymmetrical construction of circuit layout, which will cause the unwanted magnetic coupling between the excitation inductance L_x and load inductance L_{Load} then readout by the dc SQUID. If this parasitic magnetic coupling was not small enough, the excitation current margin would be reduced. In order to investigate the influence of the parasitic coupling, the experiments of voltage magnetic field characteristic were conducted, from which the mutual inductance can be obtained by the relation $M = \phi_0/I_B$. I_B is the period of magnetic current that produces a single flux quantum in the SQUID loop. As shown in Fig.6.5 (a), the parasitic inductance is about 0.04 pH. A 600 μA excitation current will produce about 0.2 μV offset in the output

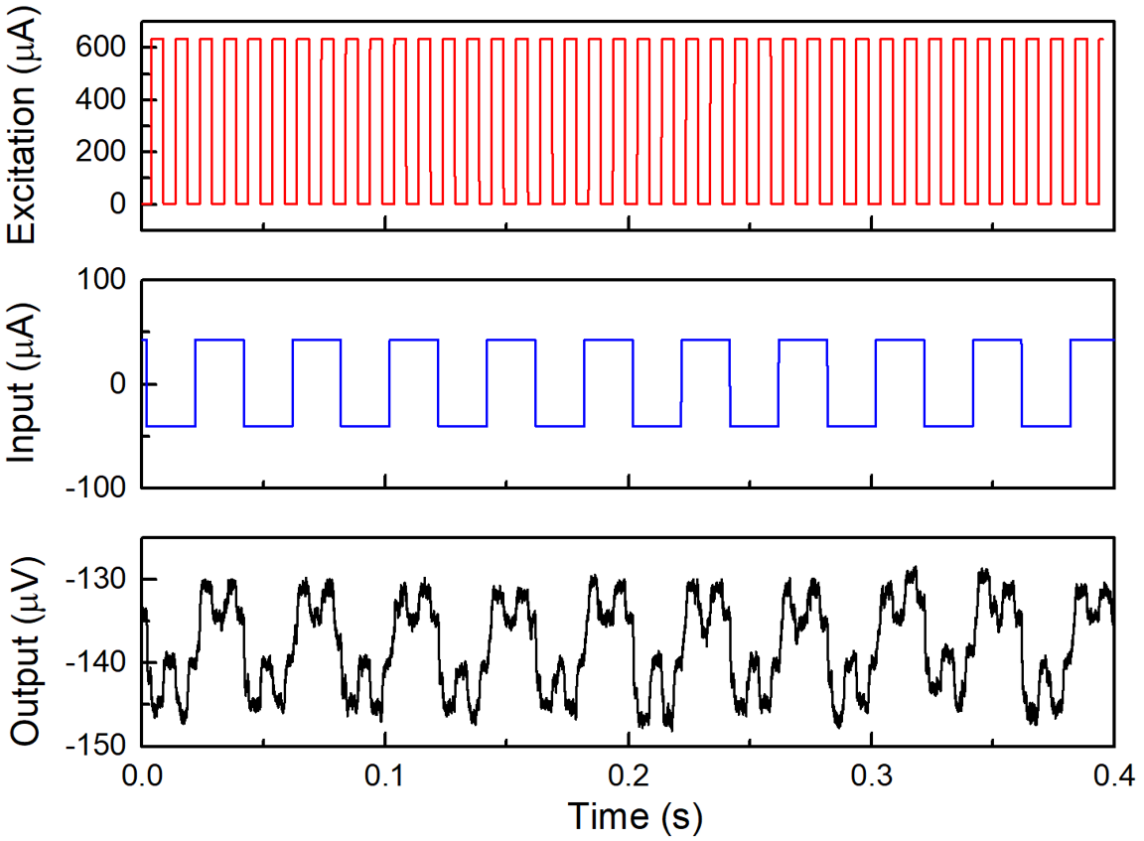

Figure 6.4: The operation of QFP switching gate measured at 25 K. A steady output voltage was observed with 600 μA excitation current and $\pm$40 μA input current at 100 Hz. The circuit parameters were the same as the parameters used in simulation.

voltage. This offset resulted in a ∼0.2 μV different between output voltage amplitude of state "0" and state "1", which is negligibly small. The other effect that would induce an offset in output voltage is the input current. The mutual inductance between the L_q and readout SQUID is about 1.65 pH. As shown in Fig.6.5 (b), a 40 μA (-40 μA) input current will cause a ∼2 μV (-2 μV) offset. This offset corresponds to a ∼4 μV offset between two different polarity pulses in Fig. 6.4. Generally, the input current of QFP gate can be much smaller than 40 μA and the influence of input current will be suppressed. Moreover, from voltage magnetic current characteristics, ∼90 μA is needed to produce a 5 μV modulation, which corresponds to the output current. Therefore, the current gain of QFP gate is about 2.25.

6.4 Voltage Buffer

In addition to the basic operation, QFP gate can work as a voltage buffer. In previous measurement, the readout SQUID is biased at the most magnetic flux sensitive point. When the flux bias moves close to the bottom of the voltage magnetic oscillation, only one direction modulation will generate an output. As shown in the Fig. 6.6, the output only produces when the input current is positive. As this circuit provides either no voltage or a voltage that is same as the input signal, it can used as digital buffer.

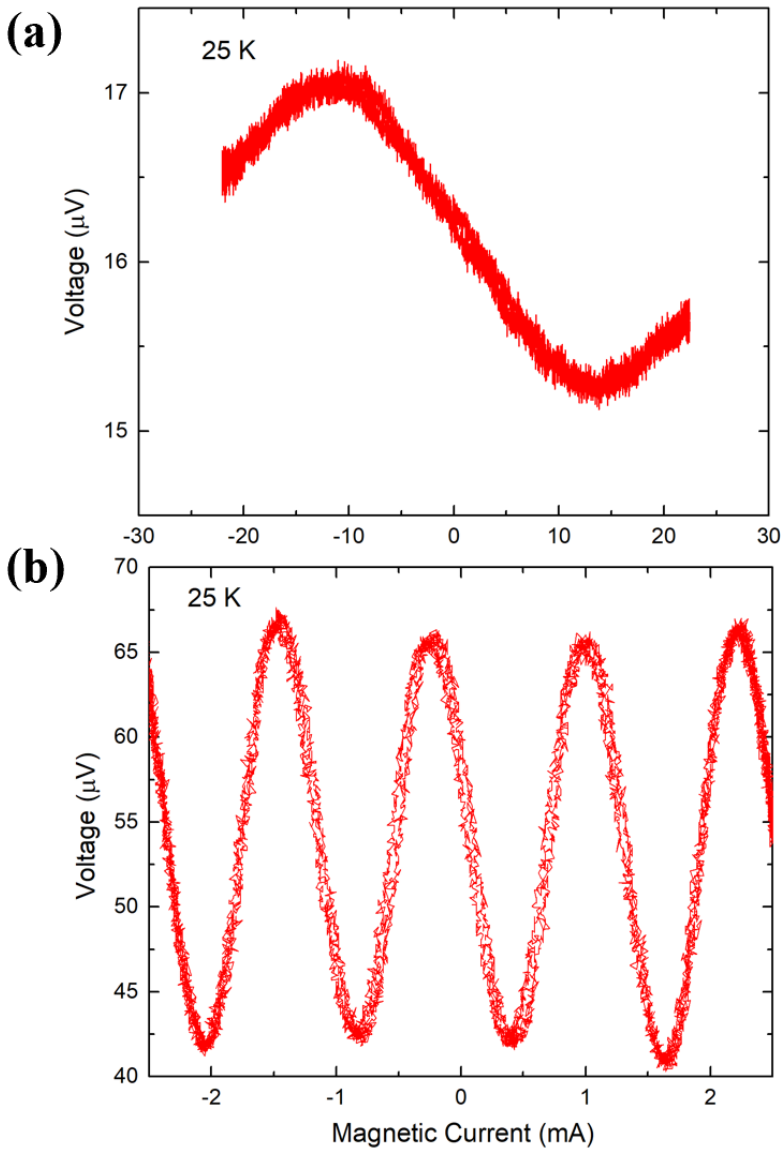

Figure 6.5: Voltage magnetic current characteristics for (a) readout SQUID modulated by the excitation current and (b) readout SQUID directly modulated by the input current.

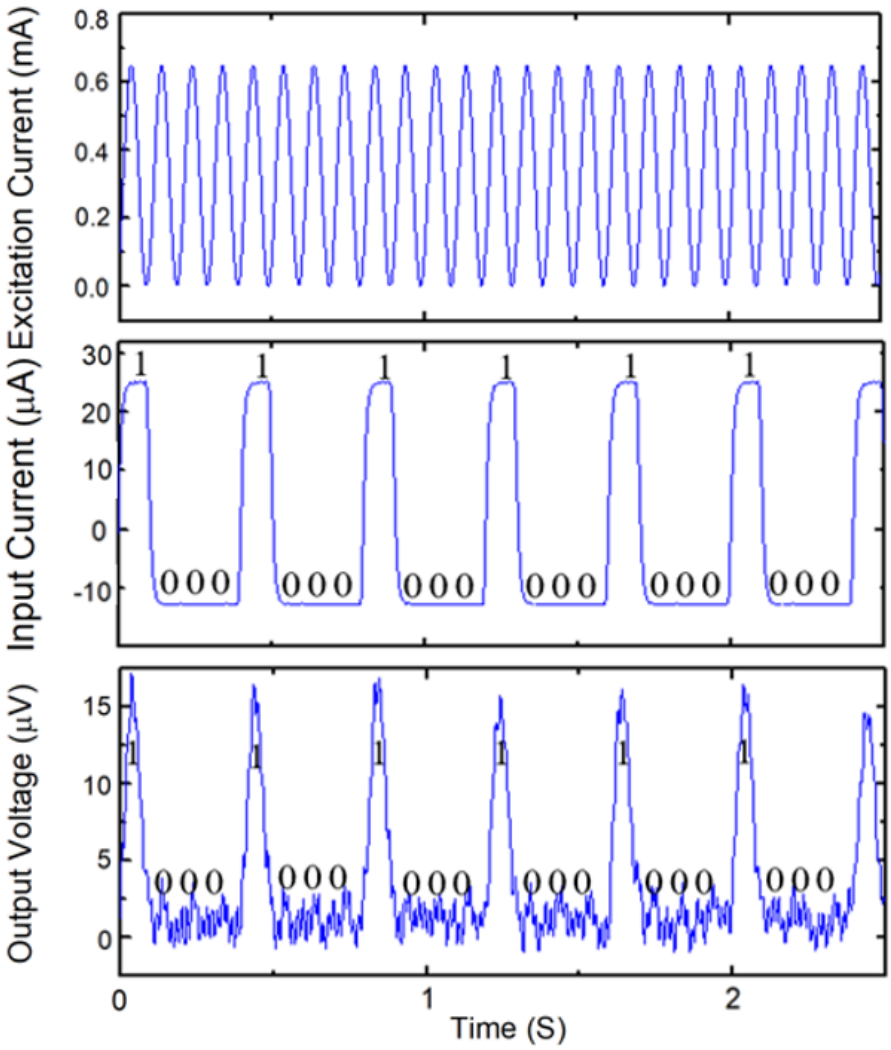

Figure 6.6: The operation of voltage buffer. A steady output voltage was observed only when both excitation current and input current are activated.

6.5 QFP Array

Moving on from a single QFP, a three-stage QFP gate has been developed. The QFP array is driven by three-phase clock pulses whose phases are shifted 90° relative to each other. As shown in the Fig. 6.7 the excitation currents are activated in turn. When the input current is positive, each QFP generates an output current in turn after each excitation current is activated then propagating one-bit information. An output voltage is obtained by readout SQUID when the third clock is in the high state.

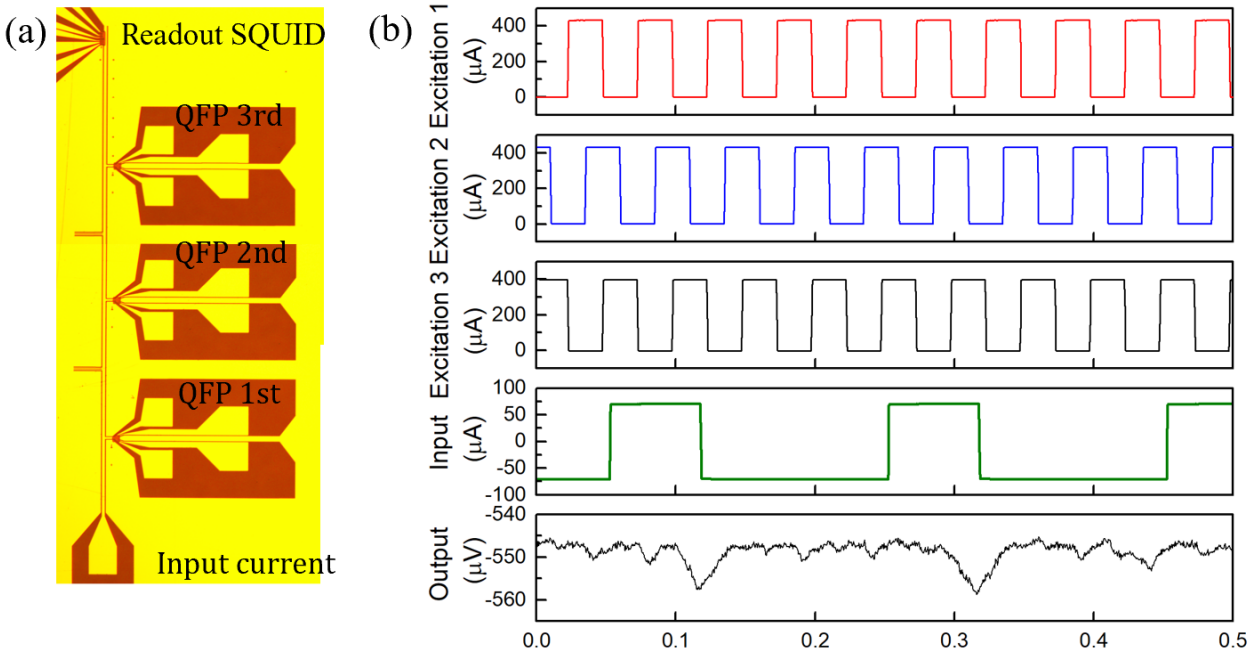

Figure 6.7: (a) The optical microscopic photograph of the three-QFPs array. (b) The operation of the three-QFPs array.

6.6 Conclusion

In conclusion, We have designed and measured a high T_C QFP gate fabricated by the FHIB. The experimental results confirmed the correct switching operation of a QFP gate and the measurement revealed that the offset caused by the parasitic coupling was negligibly small and the QFP gate worked robustly with this small parasitic coupling. In the future, we will focus on decreasing the circuit inductance β_L and β_q, which can dramatically reduce the dynamic switching energy of a single QFP gate. As mentioned before, β_L and β_q are two important parameters, which will define the dynamics energy dissipation, the QFP gate operating margin and the QFP gate operating mode in an adiabatic mode or in a non-adiabatic mode. These two parameters have been precisely investigated and demonstrated in the previous papers [51] [74] that QFP gate had the potential to operate with adiabatic switching by gradually changing the potential energy profile between a single-well shape and a double-well shape so that the logic states can switch quasi-statically. The dynamic energy dissipation of an adiabatic QFP (AQFP) ($\sim$ zJ at 5 GHz operation) is about two orders of magnitude smaller than the dynamic energy dissipation of the original QFP. The bit energy of AQFP is approaching the theoretical thermal limit $k_BT\ln 2$. Comparing to the optimized β_L and β_q [51] ($\beta_L = 0.4$, β_q=1.6), which can maximize the benefit of adiabatic switching with a wider current margin, smaller energy dissipation and higher operating frequency, β_L and β_q used in this chapter are a little bit large, which suppress the current gain and increase the dynamic power consumption. In the future, a thick YBCO film will be used for patterning with a ground plane underneath to decrease the sheet inductance, which results in small enough β_L and β_q that can operate the QFP gates in the fully adiabatic mode.

Moreover, due to the smaller circuit inductances, the influence of the parasitic coupling will be further suppressed. The thick films not only have good qualities and less defects but also increase the critical current densities, which will further improve the junction intrinsic switching speed and logic gate operation speed. Overall, the HTC QFP gate fabricated by FHIB technology is particularly useful in applications requiring lower energy dissipation and higher operation temperature.

Chapter 7

Conclusions

Herein, we have experimentally demonstrated that the technique of FHIB is particularly useful in the application of high T_C digital circuits.

The dissertation began with the Josephson junction irradiated by the FHIB technology and the investigation of sheet inductance in $YBa_2Cu_3O_{7-\delta}$ thin film. The junction characteristics have been experimental demonstrated. The parameter of inductance is another key role in realizing a high-speed, low-power and high-performance superconducting digital logic. We experimentally measured and compared the sheet inductance of $YBa_2Cu_3O_{7-\delta}$ films with and without superconducting ground planes. Specifically, we fabricated several superconducting quantum interference devices from single and multilayer films with different geometries using a focused helium ion beam. Measurements of the device electrical transport properties were analyzed to determine the sheet inductance. Additionally, temperature dependent measurements of the inductance were used in order to separate the contributions from geometric and kinetic inductance. We found that the pres-

ence of a ground plane in our multilayer structure significantly reduces the contribution of the geometric inductance with no detectable change in the kinetic inductance.

Depending on the FHIB junction fabrication technology, the following three chapters present three different types of high T_C devices fabricated by the FHIB. Materials modification of YBCO with focused helium ion irradiation has greatly improved the control of processing oxide superconductive devices. Higher resistances and smaller feature sizes enable novel device geometries. Nanoscale structures created in this manner can be used in to create oxide superconductive electronics. A direct-write nano-SQUID integrated with a strong inductively coupled nanostructured on-chip control line shows a promising low power superconducting transimpedance amplifier. The ability of transimpedance conversion with very large voltage modulations over a wide range of temperatures can use as an output driver for the connection between low temperature superconducting circuits and room temperature CMOS electronics. The coupled control line is much stronger than prior technology and opens up new applications for these devices in superconductive quantum electronics. The inductively coupled readout SQUID used in RSFQ and QFP gates is one of the application based on this strong-coupling technique. High T_C RSFQ logic gates are attractive not only because of their intrinsic high operating frequency but also due to their elevated operation temperatures. In this dissertation, we eliminate bottlenecks in traditional YBCO junction fabrication process and advance the state of the art in circuit fabrication technology that can readily be incorporated into a large-scale integration with nano-scale junctions for future applications. Energy efficiency is another key metric of advancement for the future logic circuit. Adiabatic QFP has the potential to reduce one bit energy dissipation to the

order of the thermal energy and achieve practical reversible logic gates. However, to realize a practical large scale superconducting system, not only low power but also high speed data transfer between cryogenic temperature and room temperature are essential. A promising approach to overcome the low operating temperature is the use of high T_C superconducting material. We implemented a high T_C QFP circuit and demonstrated to operate the gate correctly and reliably at T$\sim$25 K. The possibility of a nano-structure circuit formed by direct focus helium ion beam writing is a promising approach to realize future large-scale integration. RSFQ and QFP have their own advantages and disadvantages. The typical operation frequency of RSFQ gate is much faster than that of QFP gate, whereas the energy dissipation of QFP gate is much lower than RSFQ gate. In order to inherit the advantages of each system and build an ultrahigh speed and extremely low power logic gate, RSFQ and QFP hybrid system is an effective approach that is worth a try in the future.

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