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Transmission Line Based Noise-Canceling LNA Design in 60GHz Communication

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To the love of my life,

Zeqi Wang

To my mom,

Airong Ding

For all their love and support

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This dissertation can not be done without the support of my family, my wife Zeqi Wang, my mother Airong Ding, my father Yongjin Zeng. You are the best family I could ever hope for.

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Abstract

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This dissertation describes a complete design of transmission line based 60GHz low-noise amplifier with noise-canceling technique in bulk CMOS technology. Paper starts with transceiver system review, including building blocks and the importance of LNA noise figure. Existing noise-canceling LNA topologies at sub-6GHz are reviewed. The difficulties of migrating them into 60GHz LNA design is discussed and solution is proposed. Furthermore, transmission line fundamentals are reviewed in detail. Two innovative applications of transmission line, as a voltage dividing feedback path and as input/output impedance transformer, are proposed, both with mathematical derivation and simulation validation. Finally, two 60GHz noise-canceling LNA are designed. The transmission line feedback LNA is designed, utilizing the advantage of transmission line feedback path, noise canceling and derivative superposition. This LNA has very high linearity and lowest noise figure ever recorded in any publications.

Chapter 1 Introduction

1.1 Wireless communication and 5G

In the last few decades, wireless technologies have reshaped our human society in all aspects. People used to make phone calls on telephone at home or at work, and then comes cell phone allowing access for a call anywhere on the planet. People used to surf the internet for news sitting in front of a personal computers with cables connected to an ethernet port, and then comes the WiFi that enable your portable devices that can connect to internet anywhere at your home. People used to take photos on their camera and transferring pictures to computers/internet with USB, and then comes iPhone that you can record whatever you see and publish it on Facebook immediately wherever you see it. The wireless communication has changed the way we live, reformed industrials and increased productivity to a new level. Not only it changed the physical surroundings of our environment, it also reshaped our ideology and imaged existence of things that relate to real condition of existence.

Fig 1.1 The old generation of communication VS the new generation [25]

As the wireless communication technology develops, we are banging on the gate of 5G, the fifth generation of cellular mobile communications. The 5G is a successor of current 4G wireless protocol, aiming at higher data rate, reduced latency, energy saving, cost reduction, higher system capacity and massive device connectivity. These advantages are achievable through 3 major technology upgrades: 1. extreme

densification and offloading, 2. mmWave and 3. Massive MIMO (Multiple Input Multiple Output)[1]:

1. Densification and offloading: A straightforward but effective way to increase network capacity is to make the cells smaller. The smaller the cells are, and denser the base station can be deployed. This deployment eases the competition of end users within the range of same base station and allow each user to have wider spectrum for communication and backhaul.
2. mmWave: Terrestrial wireless systems have largely restricted their operations to the relative slim range of microwave frequencies from several hundred MHz to a few GHz. One the other hand, mmWave frequency, ranging from 30-300GHz and wavelengths are 1-10mm, has the advantage of wider bandwidth and less interference (due to the fact of path loss and small covering range).

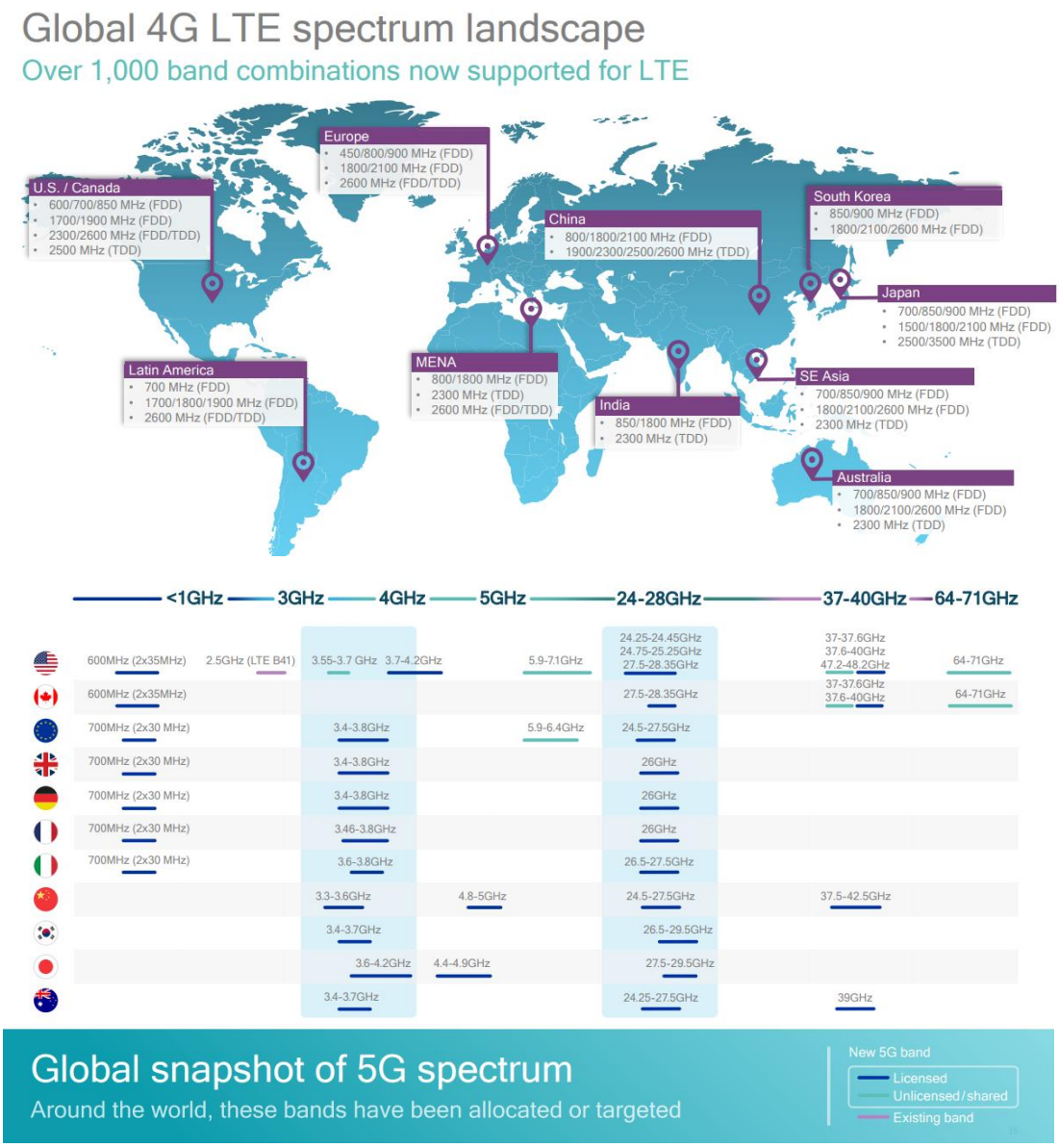


Fig 1.2 Comparison of 4G and 5G spectrum usage[26]

3. Massive MIMO: (also referred to as “Large-Scale MIMO” or “Large-Scale Antenna Systems”) is a form of multiuser MIMO in which the number of antennas at the base station is much larger than the number of devices per signaling resource. Having many more base station antennas than devices

renders the channels to the different devices quasi-orthogonal and very simple spatial multiplexing/de-multiplexing procedures quasioptimal. The favorable action of the law of large numbers smoothens out frequency dependencies in the channel and, altogether, huge gains in spectral efficiency can be attained. Eventually, higher data rate can be achieved with the help of multiple antennas and spatial multiplexing techniques.

Just like the way cell phone and 3/4G communications have done to reshape of society and ideology, the development of 5G will bring out more use cases that will potentially change our human once more. To name a few, the VR (virtual-reality) headset/helmet is causing dizziness of user due to the latency of video VS head movement, which is something can be solved by 5G. The data transmission ability 3G communication boosted the impact of social media companies like Facebook and Twitter, while the improved data speed 4G created live streaming video platform companies like Twitch. Previous hardware innovations proved its ability of creating industrials (especially software companies) from ground, there is no doubt with even more advanced data speed 5G provides there will be more software innovation and companies will be generated.

1.2 60GHz and Beyond

The biggest advantage of mmWave communication is the widen frequency bandwidth, but the frequency spectrum is not free across all frequency range. In the United States, FCC (Federal Communication Commission) allocates 36-40GHz for licensed high-speed microwave data links and 60GHz band for unlicensed short range (1.7km) data links with data throughputs up 2.5Gbit/s. The 71-76, 81-86 and 92-95 GHz bands are also used for point-to-point high-bandwidth communication links. As for the 60GHz frequency, in May 2009, IEEE standard, IEEE 802.11ad protocol, was announced by WiGig (Wireless Gigabit Alliance) (Wikipedia reference here). This protocol was developed from previous IEEE 802.11ac protocol that use 2.4GHz and 5GHz as WiFi protocol. IEEE 802.11ad enable devices operate in the 2.4, 5 and 60GHz band, deliver data transfer rates up to 7Gbit/s. In 2017, IEEE 802.11ay was proposed as a supplementary to IEEE 802.11ad, adding MIMO up to 4 streams and adding four times the bandwidth of previous version. [2]

However, the advantage of 60GHz does not come free. The difficulties of 60GHz frequency communication including strong pathloss, atmospheric and rain absorption, low diffraction around obstacles and penetration through objects, significant phase noise and exorbitant equipment costs. [3]

1. The path loss: if the electrical size of the antenna (i.e., their size measured by the wavelength $\lambda = c/f_c$ where f_c is the carrier frequency) is kept constant, as the frequency increases the antenna shrink and their effective aperture scales with $\lambda^2/4\pi$; then the free space path loss grows with f_c^2. Thus, increasing f_c by an order of magnitude, say from 3 to 30GHz, adds 20dB of power loss regardless of the transmit-receive distance. However, if the antenna aperture at one end of the link is kept constant as the frequency increases, then the free-space pathloss remains unchanged. Further, if both the transmit and receive antenna apertures are held constant, then the free-space pathloss actually *diminishes* with f_c^2: a power gain that would help counter the higher noise floor associated with broader signal bandwidths. Although preserving the electrical size of the antennas is desirable for a number of reasons, maintaining at the same time the aperture is possible utilizing arrays, which aggregate the individual antenna apertures: as the antennas shrink with frequency, progressively more of them must be added within the original area. The main challenge becomes co-phasing these antennas so that they steer and/or collect energy productively. This challenge becomes more pronounced when the channel changes rapidly, for instance due to mobility (whose effect in terms of Doppler shift increases linearly with frequency) or due to rapid alterations in the physical orientation of the devices.

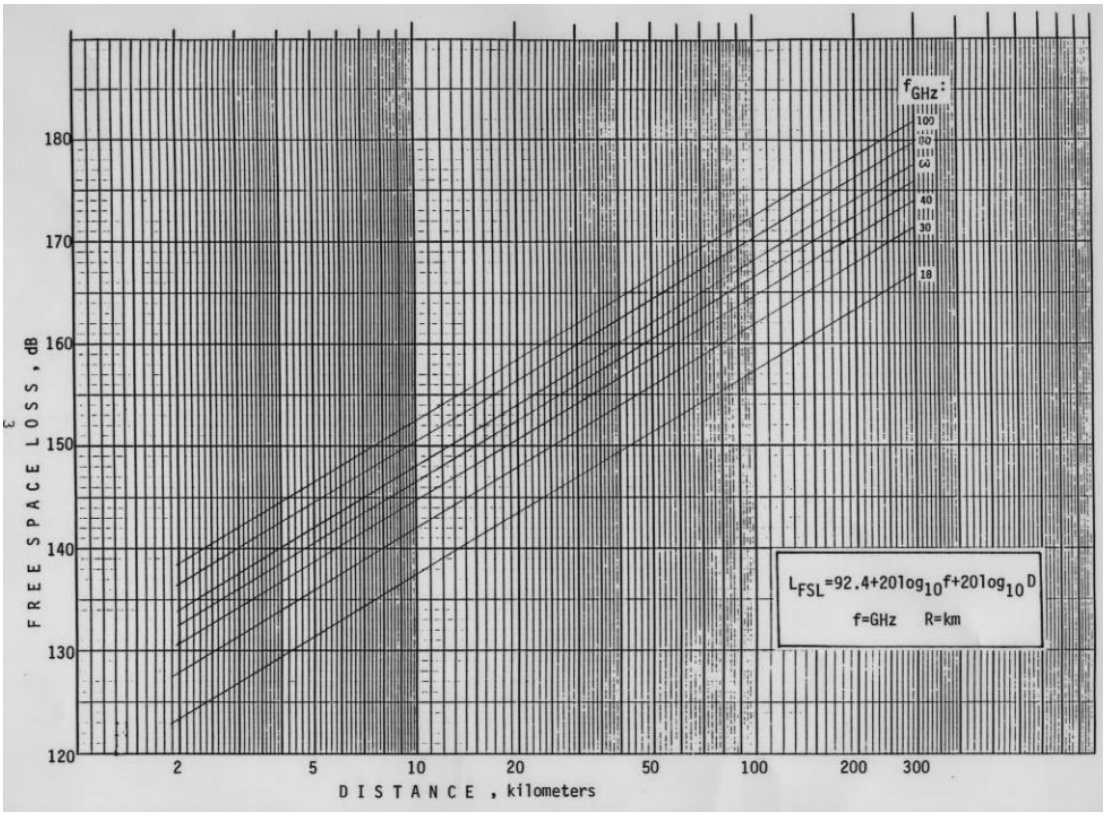


Fig 1.3 Free Space Loss Between Isotropic Antennas[3]

2. Atmosphere and rain absorption: as shown in Fig 1.4, aside path loss from the higher frequency, the atmosphere absorption is different from frequency to frequency. In 60GHz region, there is a huge spike of absorption, which severely restricted the communication range of 60GHz signals. This, however, could be treated as disadvantage or advantage at the same time. The downside is to maintain regular communication and reasonable data speed, more power from transmitter is needed to compensate the absorption. Meanwhile, the good thing is the line-of-sight communication capability is desired as data security being

paramount nowadays in some applications.

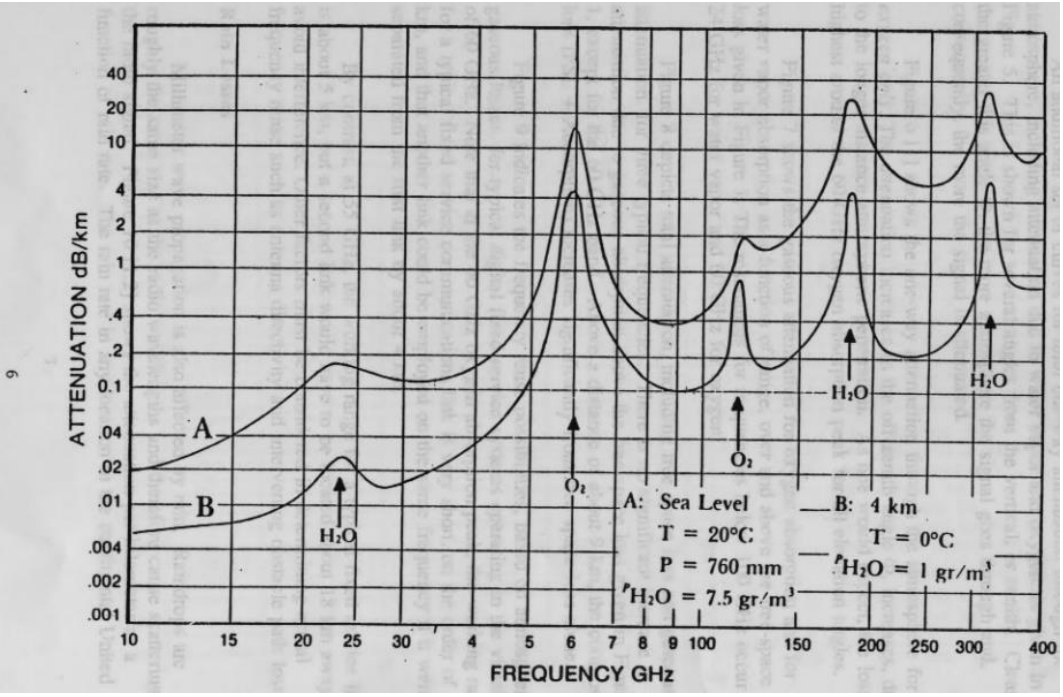


Fig 1.4 Average Atmospheric absorption of mmWave[3]

3. Low diffractions and penetrations:

If there is no line-of-sight (LOS) path between the transmitter and the receiver, the signal may still reach the receiver via reflections from objects in proximity to the receiver, or via diffraction or bending. In general, diffraction is not undesirable. In fact, there are a great percentage of power receiver received is coming from reflections and diffractions. However, due to the short wavelength of mmWave, the reflecting materials are “rougher”, resulting less diffraction power from objects. This effectively increases path loss.

Also, the real world is not free-space and the signal attenuation in gaseous environment is a big issue. As shown below in Fig 1.5, as the frequency goes up (wavelength goes down), the attenuation is growing severe.

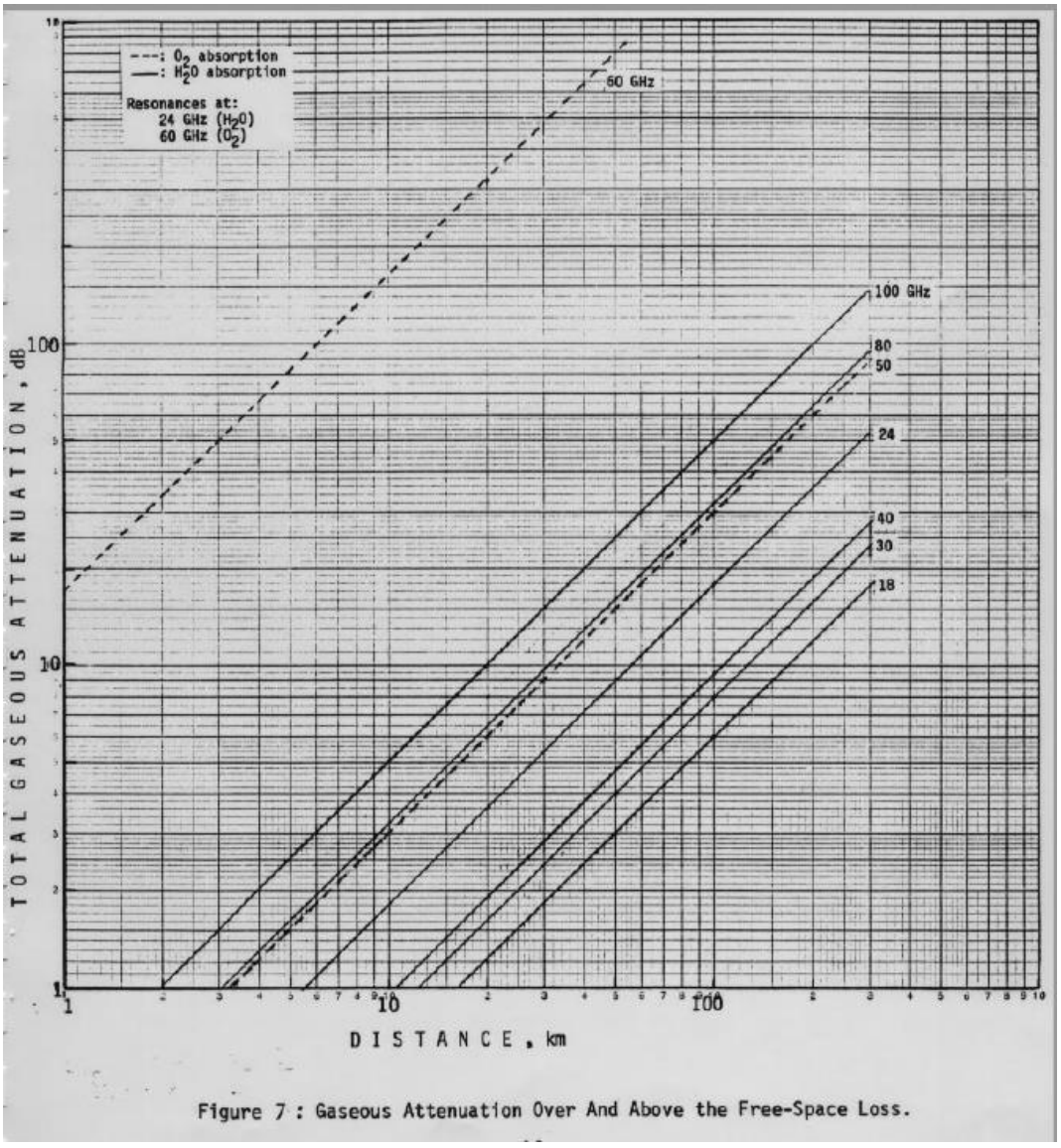


Fig 1.5 Gaseous attenuation over and above the free-space loss.[3]

With those being said, as the mmWave communication become more difficult, there is a need for receiver to have the ability to pick up weaker signals from environment. That, in electrical language, is looking for a receiver to has less noise figure.

1.3 Transmission Line and application in RF circuits

In RF engineering, the transmission line (T-Line) has been widely used when signals (voltage or current) shows their wave nature. As signals frequencies go higher, the normal wire/cable tends to radiate energy along the signal propagation direction. In RF frequency region, especially in this dissertation 60GHz region, the quarter wavelength (an indicator of lumped circuit VS distributed circuit, which is determined by whether the signal is wave or not) is down to 1.25mm, which is a comparable number to circuit size. Therefore, there are a lot of applications of T-Line in RF circuit.

One of the most important application is T-Line impedance matching. Impedance is defined as the ratio of voltage over current, but inside T-Line the voltage/current are constantly changing as the wave propagates. The reason for changing voltage/current is when treating voltage/current as wave, the wave can be either transmitting forward

or reflected backward. The transmitting wave and reflected wave together make the signal as it is at that particular point. This feature is used for impedance matching, which goal is complete transmission with zero reflection. In lumped circuits, people use inductors and capacitors to do impedance matching for maximum transmission. In RF region (discrete circuits), there are growing interests in using T-Line to do impedance matching.

If the T-Line can be used in impedance transformation, can it also be applied in voltage/current transformation? Theoretically, impedance matching is changing the impedance looking into the T-Line, and impedance is defined as voltage over current. Therefore, if impedance is transformed, does that means the voltage is transformed as well? From physics point of view, the voltage along the signal propagation direction, the voltage is transmitting voltage + reflected voltage. That means the voltage is different from point to point along the propagation direction, which is voltage transformation. The theory of “voltage transformation” along T-Line seems reasonable but haven’t been proven. In this dissertation, we will try to prove it’s valid and we will present an application of T-Line “voltage transformation”.

1.4 Current status of 60GHz CMOS RFIC

For a quite long time, mm-Wave circuits have been realized in III-V compound semiconductor technologies, such as GaAs and InP. However, these technologies have low yield and limited integration. They are, generally, intended for professional and military applications for which the cost-factor is not considered. In consumer electronics and in the spirit of IoT, where everything is connected, a lower cost solution is desired. Contrarily to III-V compound semiconductor, CMOS has advantage of being the lowest cost option in volume production and offering high level of integration with RF/analog/digital circuits.

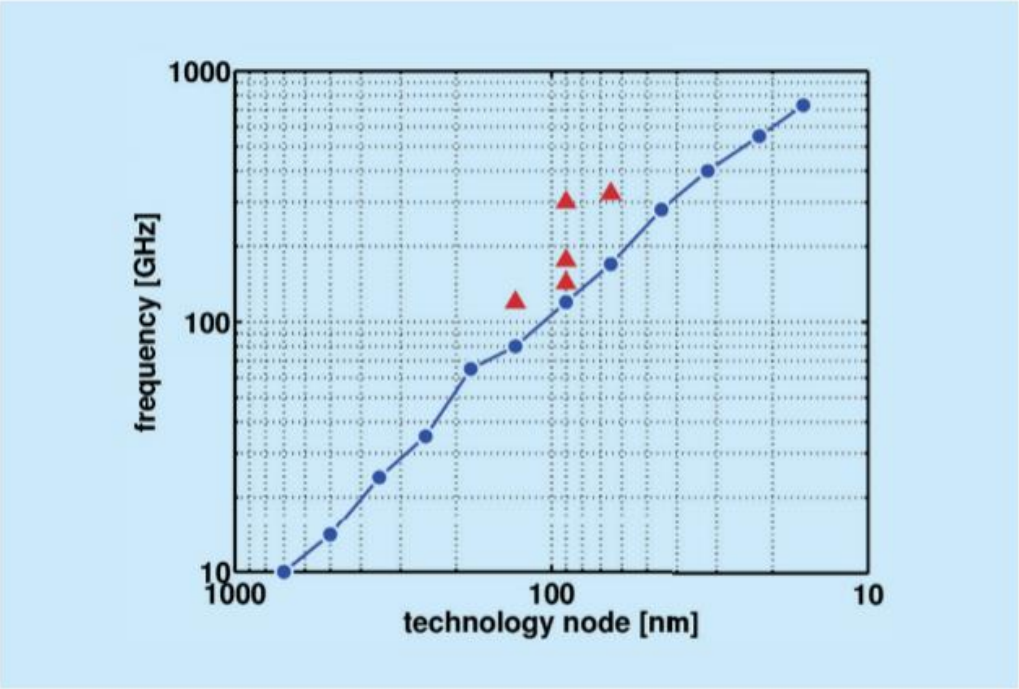


Fig 1.6 The transistor speed improves with the process scaling [Courtesy of Prof. Patrick Reynaert, the triangles represent the 90nm and 65nm transistor fmax] [27]

As shown in Fig 1.6, after following the scaling of the Moore's Law for more than 40 years, the speed of the CMOS transistor is improved significantly. The transistor f_{MAX} in the 90nm and 65nm CMOS is more than 100GHz, offering opportunities in mm-Wave applications. Considerable RF performance at mm-Wave frequencies have been achieved using low-cost CMOS technology [27].

However, the CMOS technology has its own disadvantages as well. The biggest challenges are the low-gain and parasitics. Because the transistors are working close to f_{MAX}, the transistor cannot provide sufficient gain as in lower frequencies. The

parasitics CMOS process has are usually ignored in lower frequencies, but in mm-Wave circuit design it is very destructive. These challenges are further explored, and solutions are provided in this dissertation.

1.5 Outline of the dissertation

In this dissertation, we started with the introduction of 60GHz transceiver architecture in chapter 2, and specifically low-noise amplifier. Transmission line was introduced as a critical passive device in 60GHz LNA. In chapter 3, varies LNA architectures and noise-canceling LNA topologies are presented. The theory of classic noise-canceling is discussed in detail. Chapter 4 starts with a discussion of high frequency limitation of classic noise-canceling theory, then an advanced noise-canceling theory applicable in 60GHz was proposed and discussed. To fulfill the noise-canceling operation, two innovative application of transmission line were proposed and validated. In chapter 5, two noise-canceling LNA were designed, one resistive feedback and one transmission line feedback. Design methodologies were presented and discussed in detail. Simulation results are shown and comparisons of 60GHz LNAs are listed. A conclusion is draw at the end of this dissertation.

Chapter 2 Architecture of Receiver Front End

The receiver is a critical part of a wireless system, responsible for reliably recovering the desired signal from a wide spectrum of transmitting source, interference, and noise. In this section, we will describe how to the receiver front end is composed, from architecture choices to the individual core parts. Detail analysis are discussed, like frequency planning and link budget, to provide a solution in our 60GHz receiver design.

2.1 Frequency planning and Receiver architecture

The first step of RF frequency planning is link budget. A link budget is a signal-power plan for a radio system. It is used to determine a receiver's capabilities under specific operating conditions for the standard specified data rates, ranges, and bit error rates. It accounts for the attenuation of the transmitted signal due to propagation, as well as the antenna gains and feedline and other losses. In a simple equation to define link budget:

Received Power (dB) = Transmitted Power (dB) + Gain (dB) – Losses (dB)

When taking all effective parameters into the equation above, it becomes:

$$P_{RX} = P_{TX} + G_{TX} - L_{TX} - L_{FS} - L_M + G_{RX} - L_{RX}$$

Where:

P_{RX} = received power / tolerable path loss (dBm)

P_{TX} = transmitter output power (dBm)

G_{TX} = transmitter antenna gain (dBi*)

L_{TX} = transmitter losses (connector loss/cable loss) (dB)

L_{FS} = free space path loss** (dB)

L_M = miscellaneous losses (fading margin/body obstacles/etc.) (dB)

G_{RX} = receiver antenna gain (dBi)

L_{RX} = receiver losses (connector loss/cable loss) (dB)

*dBi(isotropic) is the forward gain of an antenna compared with the hypothetical isotropic antenna, which uniformly distributes energy in all directions. Linear polarization of the EM field is assumed unless noted otherwise.

**free space loss is calculated by Friis equation, free of environment obstacles

To get a feeling of how much power is received by receiver, (from reference book mm-Wave communication system) an example of mm-Wave scenario is given as follows: transmission power to Tx antenna is 10dBm, the communication distance is 5m and path loss for 5m is approximately -82dB, the connection losses at Tx and Rx are approximately -15dB each. Tx/Rx antenna gain is 12dBi. To sum up, a receiver

usually requires high gain of 100-120dB to restore the low power received to a level near its original baseband value. This much of gain should be spread over the RF/IF/baseband stages to avoid instabilities and possible oscillation.

Besides the power constraint, the link budget, there are other functions receiver should be able to provide: *selectivity*, in order to receive the desired frequency signal while rejecting adjacent channels, image frequencies and interferences; *isolation*, from the transmitter to avoid saturation of the receiver; *down-conversion*, from the received RF frequency to a lower IF frequency for baseband signal processing.

High gain can be obtained with amplifiers, at RF and IF stages. RF amplifier are responsible to detect and amplify RF signal to proper level for mixing while maintaining reasonable noise figure. The amplifier cost and design difficulty generally increase with frequency. Therefore, IF amplifier can give more gain to meet gain requirements. In principle, selectivity can be achieved by using a narrow bandpass filter at the RF stage of the receiver, but the bandwidth and cutoff requirements for such filter are usually impractical to realize at RF frequencies. It is more effective to achieve selectivity by down converting a relatively wide RF bandwidth around the desired frequency band. Down-conversion can be fulfilled with mixers, along with frequency synthesizer to create a reference frequency.

A RF receiver front-end is the combination of the above circuit blocks. There are two mainstream RF front-end architecture: super-heterodyne architecture and direct-conversion architecture.

The super-heterodyne architecture (as shown in Fig 2.1) is the most popular choice for RF receiver front-end. It consists of: an antenna; an RF bandpass filter first rejects out-of-band signals along with RF signal; a low noise amplifier amplifies RF signal while keeping the noise level as low as possible; an image rejection filter suppresses the image signal at $2w_{LO}$-w_{RF}, which could be overlapped with original RF signal after mixing; a mixer that down converts the signal from RF to intermediate frequency (IF); a channel selection bandpass filter removes unwanted signals, and an IF amplifier before feeding signal to baseband.

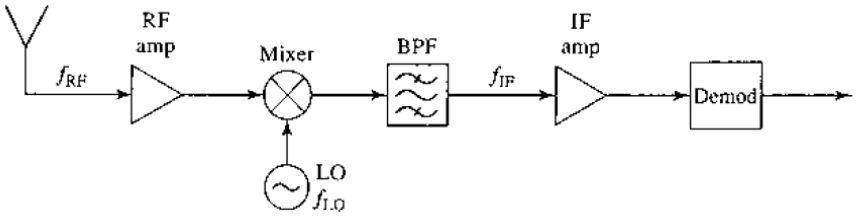


Fig 2.1 Block diagram of a single-conversion superheterodyne receiver [5]

Direct conversion has advantages in intrinsically simple architecture, due to absence of image filtering (as shown in Fig 2.2). Direct conversion receiver is similar to superheterodyne receiver except the local oscillator frequency is set to the same

frequency as the desired RF signal. Therefore, the RF signal is directly converted to baseband. Filter design is also easier, no low-pass filter is needed. In lower frequencies, the direct conversion receiver is preferred due to lower power and lower area cost, making it attractive to monolithic one-chip integration and mobile application devices. However, its drawbacks including higher dynamic range requirements, sensitivity to DC offset and local oscillator leakage back to the antenna. When designing 60GHz receiver, the immature 60GHz circuit technologies have made it more challenging to use the direct conversion architecture. Nevertheless, several results have been made. (reference here, direct conversion 60GHz transceiver)

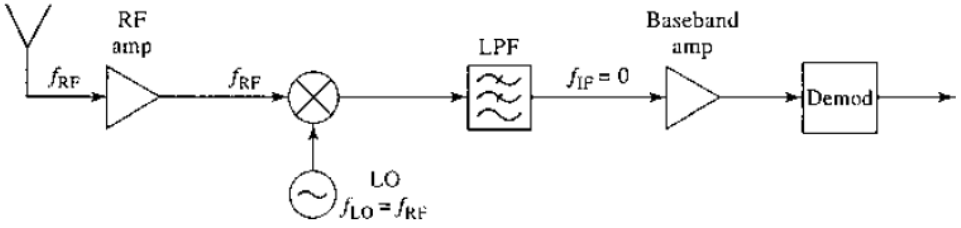


Fig 2.2 Block diagram of a direct-conversion receiver [5]

When designing the system, one of the most basic consideration is dynamic range. The dynamic range is the ability of picking up the weak signals from noise and handling the strong signals without distortion. It is identified by two parameters, noise figure and compression point/interception point.

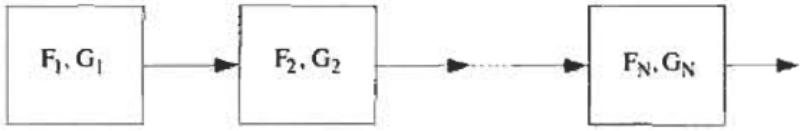


Fig 2.3 Cascaded systems for noise figure computation

For a cascaded system in Fig 2.3, like receiver, the total noise factor is the sum of these individual contributions, given by Friis' formula:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{\prod_{n=1}^{N-1} G_N}$$

Where the F_n denotes the nth stage noise figure and G_n denotes the nth stage gain.

It is clear that the system noise figure is in fact dominated by the noise performance of the first few gain stages. Hence, in trying to achieve a good noise figure, most of the design effort will generally focus on the first few stages. That is why this dissertation prioritizing the importance of noise canceling structure of LNA.

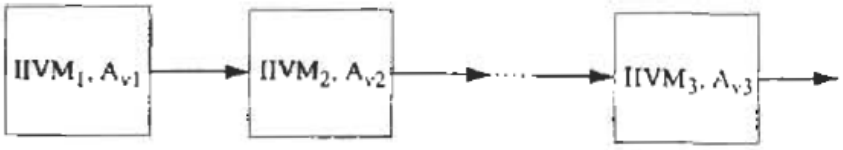


Fig 2.4 Cascaded systems for input intercept calculation

Fig 2.4 Cascaded systems for input intercept calculation

The linearity can be indicated either by 1dB compression point or third-order interception point. Here we use 3rd order interception points to quantize the non-linearity contribution of each stage, as follows:

$$\frac{1}{\mathrm{IIV3}_{tot}^2} = \frac{1}{\mathrm{IIV3}_j^2} + \sum_{j=2}^{n} \left\{ \frac{1}{\mathrm{IIV3}_j^2} \prod_{i=1}^{j-1} A_{vi}^2 \right\}$$

Where $\mathrm{IIV3_n}$ denotes the nth stage 3rd order input intercept voltage and A_{vn} denotes the nth stage voltage gain.

It is clear that for non-linearity, the latter stages have more impact than former stages. It makes sense because the signal is stronger in the latter stages, more prone to distortion.

2.2 Amplifiers and Architectures

As stated in previous section, the main function of receiver is to provide high gain. Regardless of what the receiver architecture is, there is always at least a low-noise amplifier in RF frequency as first stage to separate signal from noise and an IF amplifier to provide very high gain in the loop. In this section, we will review the amplifier design and specifically LNA design in detail.

What makes a good amplifier design? There is no straightforward answer to it. As shown in the Fig 2.5 “Analog Design Octagon”, there are so many parameters need to be considered. Gain is obvious the biggest functionality of an amplifier, especially in 60GHz where the transistor gain is limited. Noise is also very important, especially

for LNA which main responsibility is to provide gain while keep the noise figure low at the first stage of receiver. Linearity is the upper limit of the receiver dynamic range, as we discussed earlier, and the power dissipation determines the application scenario of the amplifier. Such trade-offs are the challenges in the design of high performance amplifiers, requiring intuition and experiences to arrive at an acceptable compromise.

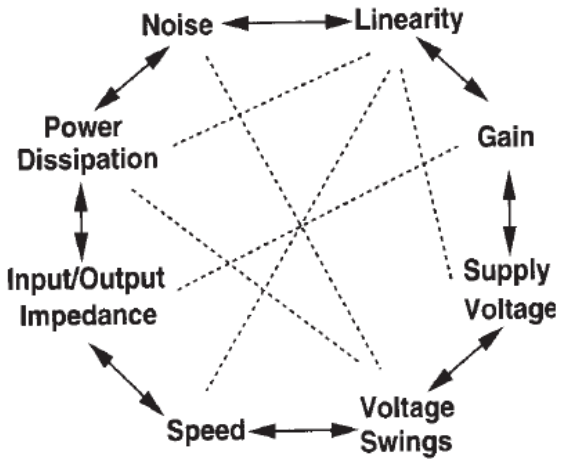


Fig 2.5 Analog Design Octagon [4]

In this sub-chapter 2.2, we start with review on transistor modeling and amplification. Then we review the three single transistor amplifier architectures: common source amplifier (CS); common drain (CD) amplifier (source follower); common gate stage (CG), which we will eventually use CS and CD to make voltage amplifier and source follower. Eventually, cascode topology is reviewed to improve the performance of amplifier.

2.2.1 MOSFET and Amplification in CMOS

In CMOS technology, the amplification is achieved by the transistor NMOS (or PMOS). To understand how the transistor can amplify signals, let's first see how transistor (as shown in Fig 2.6) works:

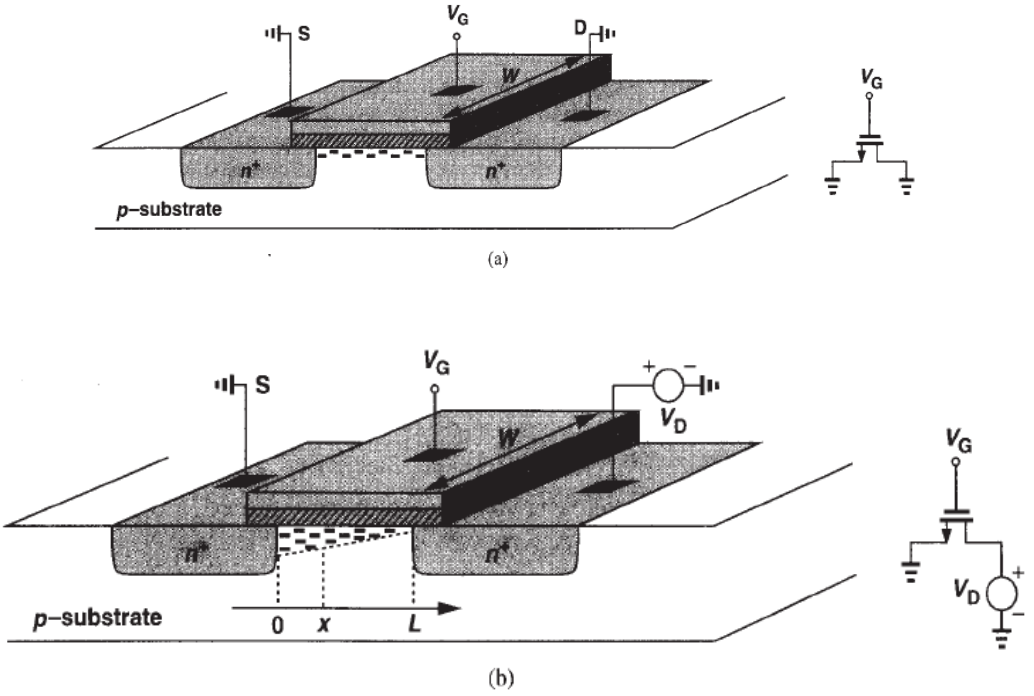


Fig 2.6 a) NMOS transistor; b) NMOS transistor channel with drain biasing [4]

Depending the relationship of Vds and Vgs, the operation of a MOSFET is separated into three different regions: *cut-off region*, *triode region* and *saturation region*. (as shown in Fig 2.7)

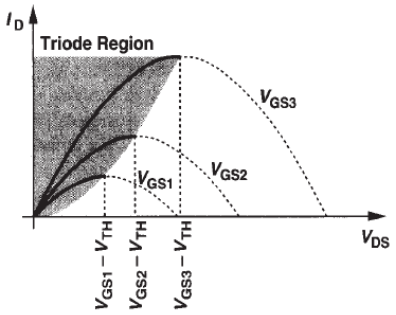


Fig 2.7 Drain current versus drain-source voltage in the triode region [4]

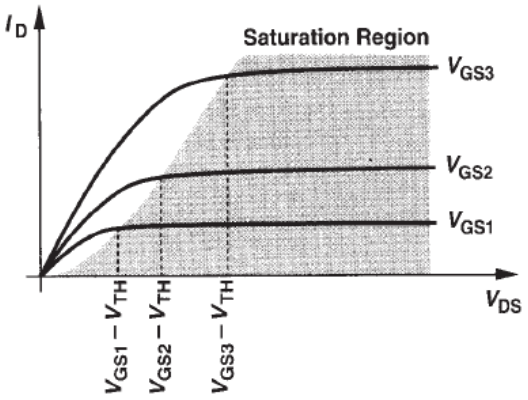


Fig 2.8 Saturation of drain current [4]

When Vgs < Vth (*cut-off region*):

the gate-source voltage Vgs is smaller than the threshold voltage Vth of a transistor, the transistor works at *cut-off region*. There is no inversion under gate oxide and no channel conduction from source to drain. Ideally, there is zero current flow between source and drain, but in practice there is weak inversion with current:

$$I_D \approx I_{D0} e^{\frac{V_{GS}-V_{th}}{nV_T}}$$

where I_D is drain-source current, I_{D0} is current at $V_{GS}=V_{th}$, the thermal voltage $V_T=kT/q$ and the slope factor n.

From expression above, although the change of V_{GS} (as input) can results in variation in I_D (as output), cut-off region is prohibited in amplifier design due to limited I_D. When designing amplifier, always make sure the transistor is turned on, which is Vgs≥Vth.

When $V_{GS} > V_{th}$ and $V_{DS} < V_{GS} - V_{th}$ (*triode region*):

the transistor is turned on, and a channel has been formed between source and drain. The transistor works like a voltage controlled current source, with drain-source voltage as:

$$I_D = \mu_n C_{ox} \frac{W}{L} ((V_{GS} - V_{th}) V_{DS} - \frac{{V_{DS}}^2}{2})$$

where un is the charge-carrier effective mobility, W is the gate width, L is the effective gate length and C_{ox} is the gate oxide capacitance per unit area.

In this region, as shown in the shaded area in Fig 2.7, the slope $\partial(\frac{Ids}{V_{GS}})$ of the graph indicates the power of signal amplification. Assuming the CS stage is connected to a fixed resistor load R, small variation of V_{ds} will generate variation on I_{ds}, and in turn to create voltage variation across load resistor. This amplification can be modeled mathematically by transconductance.

Transconductance, denoted by g_m, is defined as the change in the drain current divided by the change in the gate-source voltage, as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{GS}} = u_n C_{ox} \frac{W}{L} V_{DS}$$

When $V_{GS} > V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$ (*saturation region*):

When the transistor is fully turned on, the channel is fully formed. However, as the voltage V_{DS} exceed $V_{GS} - V_{th}$, which is also called "overdrive voltage", current Ids will not increase infinitely. Instead, channel is *pinched-off*, as shown in Fig 2.9.

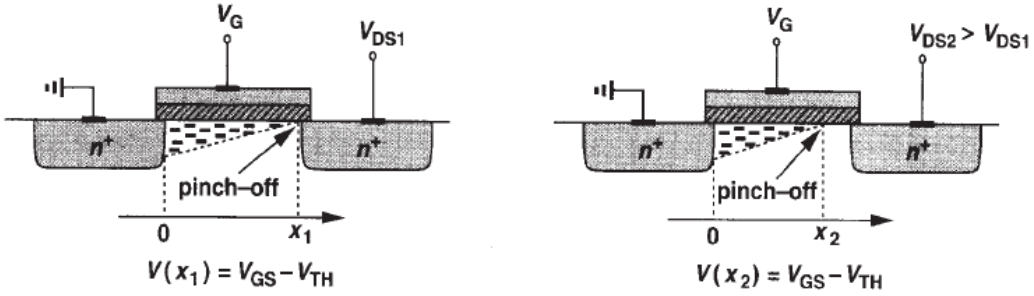


Fig 2.9 Pinch-off behavior [4]

As voltage V_{DS} increases, the effective length drops and maintain a constant current. The drain current is given as:

$$I_{D,max} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

and transconductance can be expressed by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} |_{VDS,const} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

Knowing the MOSFET performance is the first stage in amplifier design. By understanding what the transistor can do, basically as a voltage controlled current source (g_m), we can amplify signals. There are also several secondary effects affecting the performance of transistor, such as body effect, channel length modulation, as well as high frequency modeling of transistor. (Details is discussed in Thomas Lee's book [5]).

2.2.2 Common source amplifiers

The common source amplifier converts variations in its gate-source voltage to a small-signal drain current, which can pass through a resistor to generate an output voltage. As shown in Fig 2.10:

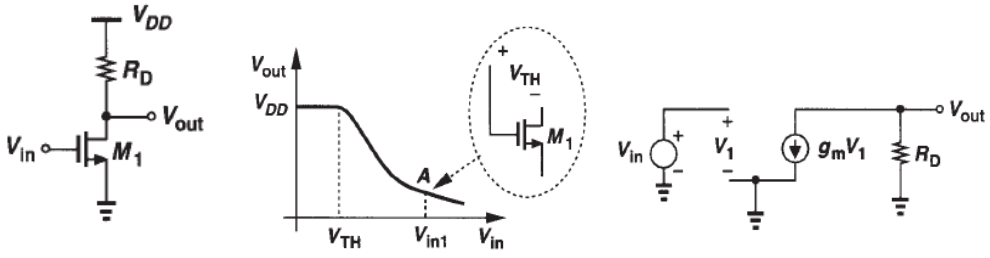


Fig 2.10 a) Common-Source Stage, b) large signal input-output characteristic, c) small-signal model for the saturation region [4]

Assuming transistor in working in saturation region (means Vin are between Vth and Vin1 in Fig 2.10.b), then output Vout and gain Av:

$$V_{out} = V_{DD} - R_D \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2$$

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -R_D \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) = -g_m R_D$$

Common source amplifier is the most common amplifier in analog/RF circuit design. It could provide very good gain and high input impedance. This topology is very well studied that it can easily provide 50ohm input impedance with proper LC circuit, a good linearity with source-degeneration and noise canceling with feedback.

2.2.3 Common drain amplifier.

Common drain amplifier, also known as “buffer” or “unity buffer”, is a voltage buffer that provide unity voltage gain but can drive low-impedance output (contrary to common-source amplifier which gain is proportional to output impedance). A common drain amplifier and its small signal equivalent circuit is draw in Fig 2.11.

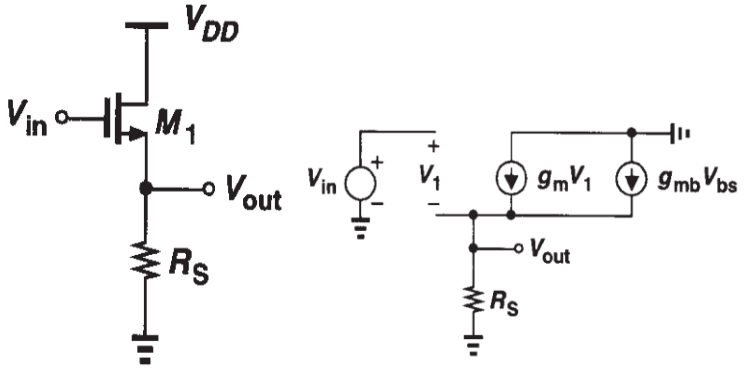


Fig 2.11 a) Common-Drain Stage, b) small-signal model for the saturation region [4]

Again, assuming the transistor is working in saturation region,

$$V_{out} = R_S \times \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{in} - V_{TH} - V_{out})^2$$

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = \frac{g_m R_S}{1 + (g_m + g_{mb})R_S}$$

Since common drain amplifier exhibit unity gain, high input impedance and a moderate output impedance, it is often used as the output stage of common source amplifier.

2.3 Low Noise Amplifier

Low Noise Amplifier (LNA) is typically the first stage of a receiver. Its main function is to provide enough gain to overcome the noise of subsequent stages (such as a mixer). The signal entering the LNA is usually very weak and mixed with noises. From Friis' Formula, we know the first few stages of the receiver will dominate its overall NF. Therefore, LNA plays a critical role in providing this gain while adding as little noise as possible. In this section, we will go over the LNA performance metrics, design methodology and one of the most common LNA topology, the shunt-series LNA. The shunt-series LNA topology will be adopted in this dissertation LNA design.

2.3.1 Performances and performance metrics

Aside from providing gain and minimizing noise, LNA should also accommodate large signals without distortion, good impedance matching to previous stage and following stage, and limited power consumption and area cost based on application scenario. Knowing what we are expecting from LNA, below are the metrics that define performance:

1. ***Gain***: gain is a measurement of the ability to amplify signal. It is measured by Scattering parameters S21. S-parameters are usually expressed on logarithmic scale in term of decibel (dB).
2. ***Noise:*** Noise is defined by noise figure (NF), as shown below:

$$NF = 10\log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right) = SNR_{in,dB} - SNR_{out,dB}$$

   it is the degradation of signal to noise ratio at input vs at output. It is also expressed in dB. NF defines the lower limit of LNA dynamic range. The smaller the NF is, the better LNA can retrieve data from noisy inputs, which requires less discrepancy of signal from noise floor.
3. ***Linearity:*** Linearity of LNA defines the upper limit of LNA dynamic range. It is the maximum input power level of the input signal without distortion in waveform (which is information). There are two commonly used measures of linearity: 1-dB compression point (P_{1dB}) and input referred third order intercept point (IIP3). P_{1dB} is defined as the input power that causes a 1dB drop in the linear gain due to

device saturation. IIP3 is defined as the input power at which the amplitude of the third-order intermodulation (IM3) term is equal to the amplitude of the linear fundamental term. (Worth mentioning here IIP3 is a purely mathematical concept based on the assumption that the nonlinearity of an LNA could be modeled using lower order polynomial, and it is usually higher than the actual max linear input).

4. ***Input impedance and output impedance:*** they are the impedance looking into the LNA from input side and output side. Impedance matching refers to the requirements that an LNA should present a specific impedance (e.g, 50Ω) to the input and output load. The impedance matching determines the transfer characteristics of the LNA. Input impedance matching is particularly important if a passive filter precedes the LNA, since the characteristics of many filter are quite sensitive to the quality of the termination. Input/output impedance matching are measured by S11 and S22 parameters by considering an LNA as a two-port network.
5. ***Stability:*** Stability is a criterion that must be considered and satisfied when designing an LNA. Unconditionally stable means the LNA will not oscillate at that frequency with whatever input and output stage. Theoretically, if both input and output impedance have positive real values, in other words is the reflected power is always less the incident power, the LNA will be unconditionally stable.

Mathematically, unconditional stable is when both equations below are satisfied at the same time:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} > 1$$

$$B_1 = 1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2 > 0$$

where $\Delta = S_{11}S_{22} + S_{12}S_{21}$

Above are five major specs people paying attention to when design/select a LNA. There are also other general specs people worth noticing, like power and area consumption etc.

2.3.2 LNA topologies: power match versus noise match

Systematically analysis LNA, we can treat LNA as a 2-port black box with equivalent voltage noise sources $\underline{e_n}$, current noise source $\underline{i_n}$ and a noiseless 2-port box, as shown in Fig 2.12 below,

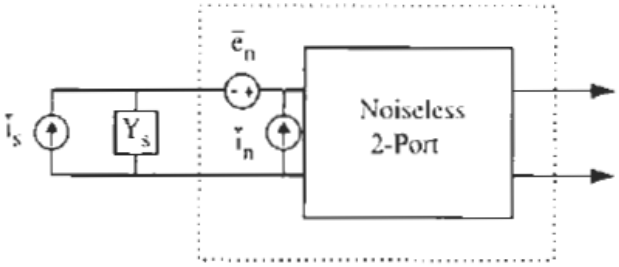


Fig 2.12 Equivalent noise model of a two-port network [5]

and the system noise factor F is:

$$F = F_{min} + \frac{R_n}{G_s}[(G_s - G_{opt})^2 + (B_s - B_{opt})^2]$$

where *Rn, Gs, Bs*, and *Gu* are four noise parameters of the system.

In LNA application, the chief noise sources are drain-source current noise and gate-source current noise. Converting them into equivalent noise model above and solve for four noise parameters. The detailed 2-port analysis is in Thomas Lee's Book Chapter Eleven[5]. Here, to understand the logic of LNA design, we list 2-port analysis conclusion in Table 2-1,

Table 2-1 Summary of intrinsic MOSFET two-port noise parameters

Parameter	Expression
Gs	*~0*
Bs	$\omega C_{gs}(1 - \alpha\lvert c\rvert\sqrt{\frac{\delta}{5\gamma}})$
Rn	$\frac{\gamma g_{d0}}{g_m^2} = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m}$
Gu	$\frac{\delta\omega^2 C_{gs}^2(1 - \lvert c\rvert^2)}{5g_{d0}}$

Where α is the substitution:

$$\alpha = \frac{g_m}{g_{d0}}$$

and correlation coefficient *c*:

$$c \equiv \frac{\overline{\iota_{ng}\cdot\iota_{nd}^*}}{\sqrt{\overline{\iota_{ng}^2}\,\overline{\iota_{nd}^2}}}.$$

To minimize noise factor, we should satisfy:

$$B_{opt} = -B_c = -\omega C_{gs}(1 - \alpha|c|\sqrt{\frac{\delta}{5\gamma}})$$

We can see the optimum source susceptance is essentially inductive in character, except that it has the wrong frequency behavior. On the other hand, for maximum power transfer (minimum power reflection), source impedance should be matched to previous stage output impedance, which in most cases is 50Ω. In short, the 2-port analysis proves the power matching and noise matching design CANNOT be achieved at the same time.

2.3.3 Shunt-Series amplifier and inductively degenerated CS amplifier

There are two commonly used topologies that can provide resistive input impedance, shunt-series amplifier and inductively degenerated common-source amplifier, as shown in Fig 2.13.

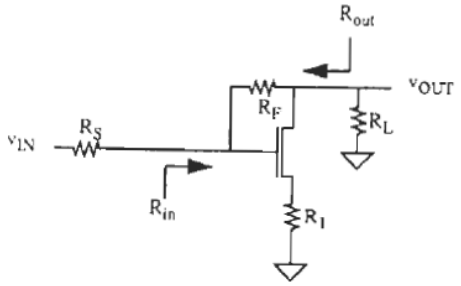


Fig 2.13 Shunt-series amplifier (biasing not shown) [5]

The shunt-series amplifier is very attractive in LNA design primarily because it can provide a relative constancy of input and output impedance over a board frequency range. In Fig 2.12, R_s denotes to the resistance of input source and R_L is the load resistance. Thus, the amplifier core consists of just R_F and R_1.

The gain and input/output resistance at low frequency are given (reference from Thomas Lee Chapter 9):

$$R_{out} \approx R_{in} \approx \frac{R_F}{1 + {R_S}/{R_1}} \approx \frac{R_F}{1 - A_V}$$

where $R=R_L=R_s$. From Equation above, we can conclude that the shunt-series amplifier can provide resistive component to compensate the gate of MOSFET, which is purely capacitive. The gain is ideally $-R_L/R_1$, and with secondary effect it ends like:

$$A_V = \frac{v_{out}}{v_{test}} = -\frac{R_L}{R_1} \cdot \left[\frac{1}{1 + {1}/{g_m R_1}}\right] \cdot \left[\frac{1}{1 + {R_L}/{R_F}}\right] \cdot \left[1 - \frac{1}{g_{m,eff} R_F}\right]$$

$$g_{m,eff} = \frac{g_m}{1 + g_m R_1}$$

From equations above, we can easily design an LNA manipulating R_1 and R_f.

At high frequencies, parasitics must be considered. In general, gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} are the main factor in input impedance. The effective input capacitance is given by:

$$C_{in} \approx \frac{C_{gs}}{g_m R_1} + C_{gd} \frac{|A_V|}{2}$$

and almost in all practical cases, the Miller-augmented C_{gd} dominates.

Still, the resistive component R_{in} and capacitive component C_{in} of input impedance fail to provide 50Ω input impedance to optimize power transfer nor inductive input impedance B_{opt} to optimize noise factor. Therefore, when designing Shunt-Series amplifier, an L-match could be used to transform the resistive component to 50Ω at some nominal frequency. Of the possible types of L-matches, the best choice is usually one that places an inductance in series with the gate and shunt capacitance across the amplifier input, such a network becomes transparent at low frequencies, where no correction is required.

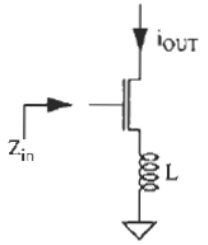


Fig 2.14 Inductively degenerated common source amplifier [5]

The shunt-series amplifier inevitably introduces excess thermal noise from resistor R_1 and R_f. However, there is another method can introduce resistive component to input impedance of a common-source amplifier, that is as shown in Fig 2.14, the inductively degenerated common-source amplifier. The input impedance has the following form:

$$Z_{in} = sL + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}L \approx sL + \frac{1}{sC_{gs}} + \omega_T L$$

where L is ω_T is g_m/C_{gs}. Z_{in} can be treated as a series of RLC network. The resistive component, which should be matched to 50Ω, is directly proportional to the inductance value. The disadvantage, though, is the limited bandwidth. As shown in equation, Zin is only resistive at resonant when $sL = -(\frac{1}{sC_{gs}})$. Luckily, in most applications, narrowband is not only acceptable but desirable. In real applications, L_g, is used in this topology to provide an extra degree of freedom when designing devices parameters, as shown below in Fig 2.15.

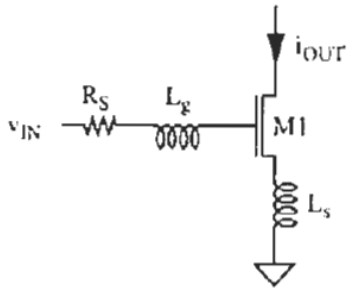


Fig 2.15 Narrowband LNA with inductive source degeneration (biasing not shown) [5]

2.4 Transmission Line

Transmission Line (T-Lines) are an important device for mmWave design. There are two major reasons: 1). At 60GHz, the reactive elements needed for matching networks and resonators become increasingly small, requiring values on the order of 50-250pH. It's becoming impossible to build an inductor with that small inductance.

On the other hand, given the quasi-transverse electromagnetic (quasi-TEM) mode of propagation, T-lines are inherently scalable in length and are capable of realizing precise values of small reactance; 2). Using T-Line has the advantage of using the well-defined ground return path significantly reduces magnetic and electrical field coupling to adjacent structures.

Theoretically, the difference between circuit theory and transmission line theory is the electrical size. Circuit theory assume all components and wires are physically much smaller than the electrical wavelength (aka lumped circuit), while in the transmission line theory everything is a considerable fraction of a wavelength, or many wavelengths (aka distributed circuit). Thus, a transmission line is a distributed-parameter network, where voltages and currents can vary in magnitude and phase over its length while ordinary circuit analysis deals with lumped elements, where voltage and current do not vary appreciably over the physical dimension of the element.

Before we are modeling T-Line, we first have to determine whether T-Line is lumped or distributed component in system. The criterion of distinguish a lumped vs distributed system is:

$$l \ll \lambda$$

Where l is the length of T-line and λ is the wavelength of 60GHz (which is $5\text{mm}/5\times10^{-3}$) (equation here). Therefore, in the circuits we analysis below, T-Line can always be treated as distributed circuit.

As shown in Fig 2.16, a transmission line is often schematically represented as a two-wire line in lumped-element circuit,

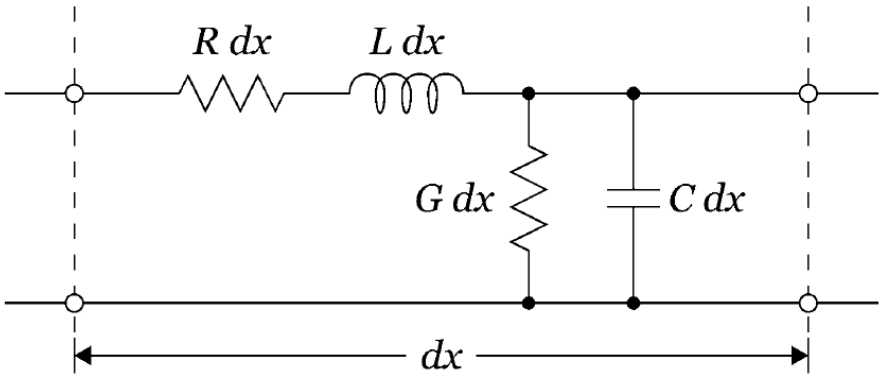


Fig 2.16 Lumped RLC model of infinitesimal transmission-line segment

Where R/L/G/C are per-unit-length quantities defined as:

R = series resistance per unit length, for both conductors, in Ω/m

L = series inductance per unit length, for both conductors, in H/m

G = shunt conductance per unit length, in S/m

C = shunt capacitance per unit length, in F/m

Since the T-Line can be completely characterized by its equivalent frequency-dependent R/L/G/C distributed circuit as shown is Fig 2.16. At 60GHz frequency, they can be modeled as:

$$Z \equiv \sqrt{L/C}$$

$$\lambda \equiv \frac{2\pi}{\omega_0\sqrt{LC}}$$

$$Q_L \equiv \omega_0 L/R$$

$$Q_C \equiv \omega_0 C/G$$

Where Z_0 is intrinsic impedance, Q_L and Q_C are inductive and capacitive quality factor respectively.

In the following sub-chapters, we will first review the T-Line impedance transformation. Then we will review how the smith chart is applied in T-Line impedance transformation. After the background is reviewed, we will analyze how the T-Line impedance transformation is used in LNA input matching with single-stub and double-stub.

2.4.1 The terminated lossless transmission line & impedance transformation

To illustrate how the T-Line can transform impedance, Fig 2.17 shows a lossless transmission line terminated in an arbitrary load impedance Z_L.

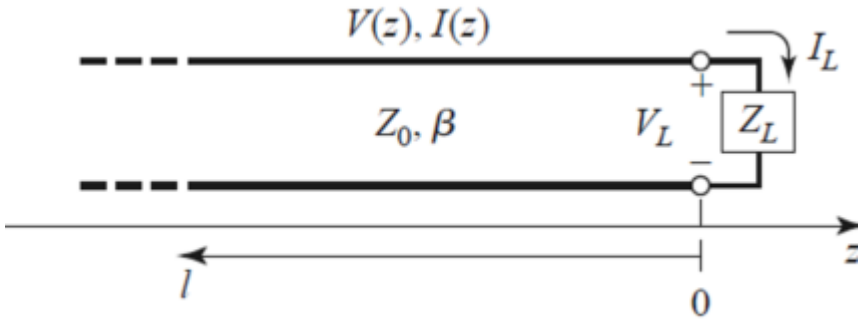


Fig 2.17 A transmission line terminated in a load impedance ZL. [6]

Assuming an incident wave of the form $V_0^+ e^{-j\beta z}$ is generated from a source at $Z<0$. Z_0, the characteristic impedance of transmission line, is the ratio of voltage to current of the traveling wave in that transmission line. However, when the line is terminated in an arbitrary load $Z_L \neq Z0$, then the voltage to current ratio of the load must be forced to Z_L. Then comes the definition of 'reflected voltage wave' $V_0^- e^{j\beta z}$ and 'voltage reflection coefficient' Γ. Assuming the load is at $z=0$, we have following equations;

$$V_{(z)} = V_0^+ e^{-j\beta z} + V_0^- e^{j\beta z}$$

$$I_{(z)} = \frac{V_0^+}{Z_0} e^{-j\beta z} - \frac{V_0^-}{Z_0} e^{j\beta z}$$

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L - Z_0}$$

From the equations above, we know that the voltage and current (both amplitude and phase) on the line are constantly changing, oscillating with relative position to load. Therefore, the impedance seen looking into the T-Line is oscillating with

position. At a distance $l = -z$ from the load, the input impedance seen looking toward the load is:

$$Z_{in} = \frac{V(-l)}{I(-l)} = \frac{V_0^+(e^{j\beta l} + \Gamma e^{-j\beta l})}{V_0^+(e^{j\beta l} - \Gamma e^{-j\beta l})} Z_0 = \frac{1 + \Gamma e^{-2j\beta l}}{1 - \Gamma e^{-2j\beta l}} Z_0$$

A more usable of the equation above is:

$$\begin{aligned} Z_{in}(d) &= Z_0 \frac{(Z_L + Z_0)e^{j\beta d} + (Z_L - Z_0)e^{-j\beta d}}{(Z_L + Z_0)e^{j\beta d} - (Z_L - Z_0)e^{-j\beta d}} \\ &= Z_0 \frac{Z_L \cos\beta d + jZ_0 \sin\beta d}{Z_0 \cos\beta d + jZ_L \sin\beta d} \\ &= Z_0 \frac{Z_L + jZ_0 \tan\beta d}{Z_0 + jZ_L \tan\beta d} \end{aligned}$$

and $\lambda = \frac{2\pi}{\beta}$

Where Z_{in} is the impedance looking into the transmission line, d is the physical length of T-line, β is propagation constant calculate in equation, Z_L is load impedance and Z_0 is the intrinsic impedance of T-Line.

From the equation above, we can conclude that there are three typical cases of using T-Line: 1). T-line is terminated to short circuit; 2). T-Line is terminated to open circuit; 3) T-Line is terminated to a load with length equals to 1/4 wavelength.

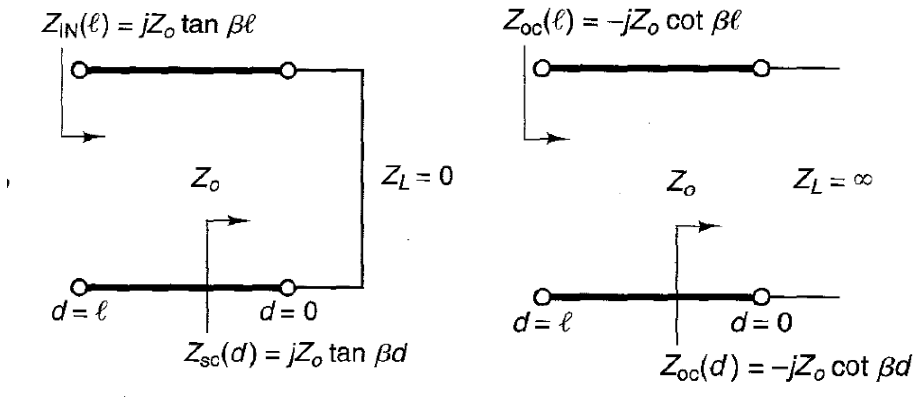


Fig 2.18 from left to right: T-Line terminated into short circuit; T-Line terminated into open circuit [6]

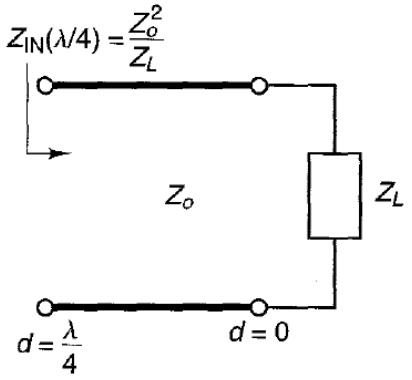


Fig 2.19 quarter-wavelength long T-Line terminated into arbitrary impedance ZL [6]

1) $Z_{SC}(d) = jZ_0 \tan \beta d$

2) $Z_{oc}(d) = -jZ_0 \cot \beta d$

3) $Z_{IN}\left(\lambda/_4\right) = \frac{Z_0^2}{Z_L}$

2.4.2 Smith chart and T-Line impedance tuning

From previous sub-chapter, we know that the impedance looking into a transmission line is not the impedance at the load. The impedance change, with or without T-Line and with different lengths of T-Line, proves to be very useful in RF circuits. For example, people use T-Line to match LNA input impedance[21]. However, in RF circuit design, it's not always the case that the impedance transformation falls into the above three categories. For a T-Line of arbitrary length terminated into an arbitrary load, smith chart proven to be a very useful tool to get correct initial state and correct trend in impedance matching.

Smith chart is based on a polar plot of the voltage reflection coefficient, Γ. Let the reflection coefficient be expressed in magnitude and phase (polar) form as $\Gamma = |\Gamma| e^{j\theta}$. Then the magnitude $|\Gamma|$ is plotted as a radius $(|\Gamma| \leq 1)$ from the center of the chart, and the angle θ $(-180^o \leq \theta \leq 180^o)$ is measured counterclockwise from the right-hand side of horizontal diameter. Any passively realizable $(|\Gamma| \leq 1)$ reflection coefficient can then be plotted as a unique point on the smith chart.

In series T-Line impedance tuning, smith chart can give a quick estimate on how the impedance looking into T-Line will change. This is very helpful in estimating the length of T-Line. To start, plot the nominal impedance on smith chart. The nominal impedance $z_L = Z_L/Z_0$. Then draw an SWR (standing wave ratio) circle through the load impedance point. Reading the reference position of the load on the wavelengths-

toward-generator (WTG) and rotating it towards the reference position of the source impedance, the distance between the starting position and ending position on the WTG is the electrical length of the T-Line. That electrical length would be a good estimate of T-Line to start with, before throwing variables into simulator.

Except for the load terminated into the load, there is another popular method of impedance matching using a single open-circuited or short-circuited length of transmission line (a stub) connected either in parallel or in series with the transmission feed line at a certain distance from the load [6].

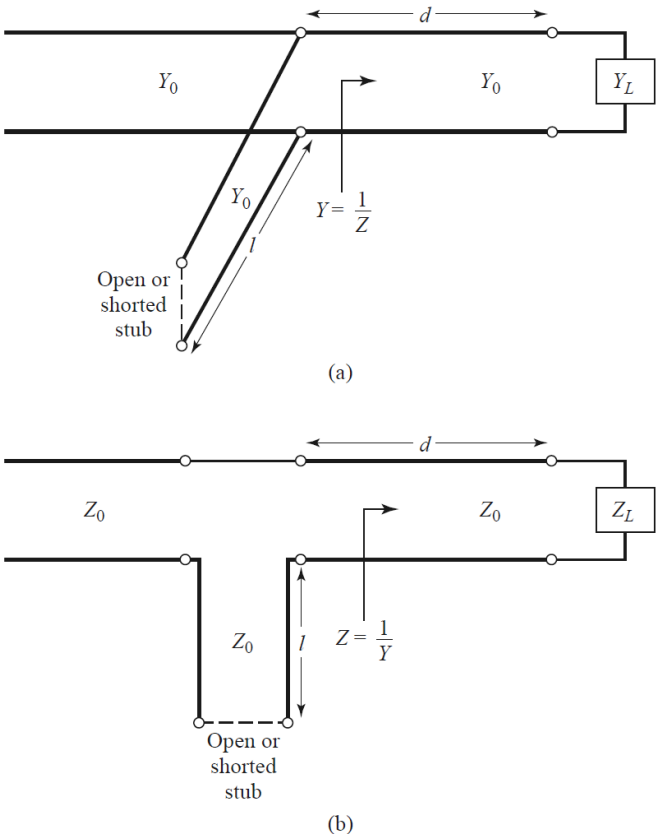


Fig 2.20 Single-stub tuning circuits. (a) shunt stub, (b) series stub [6]

Fig 2.20 shows the forms of single-stub tuning circuits: shunt stub and series stub. When designing an impedance matching circuit, there are two variables that greatly impact the results, distance d from load which changes the real impedance and stub length l which changes imaginary impedance (Eq X and X in previous section shows the open/shorted terminated T-Line can only provide imaginary impedance, or reactance). (characteristic impedance Z_0 is also a factor in changing impedance, but the range of Z_0 permitted in real semiconductor circuit is neglectable when comparing with the electrical length can do to tangent ($tan\beta d$)).

For a shunt stub, the basic idea is to select d so that the admittance, Y, seen looking into the line at distance d from the load is of the form Y_0+jB. Then the stub susceptance is chosen as $-jB$, resulting in matched condition. For the series-stub case, the distance d is selected to that the impedance, Z, seen looking into the line at a distance d from the load is of the form Z_0+jX. Then the stub reactance is chosen as $-jX$, resulting in a matched condition.

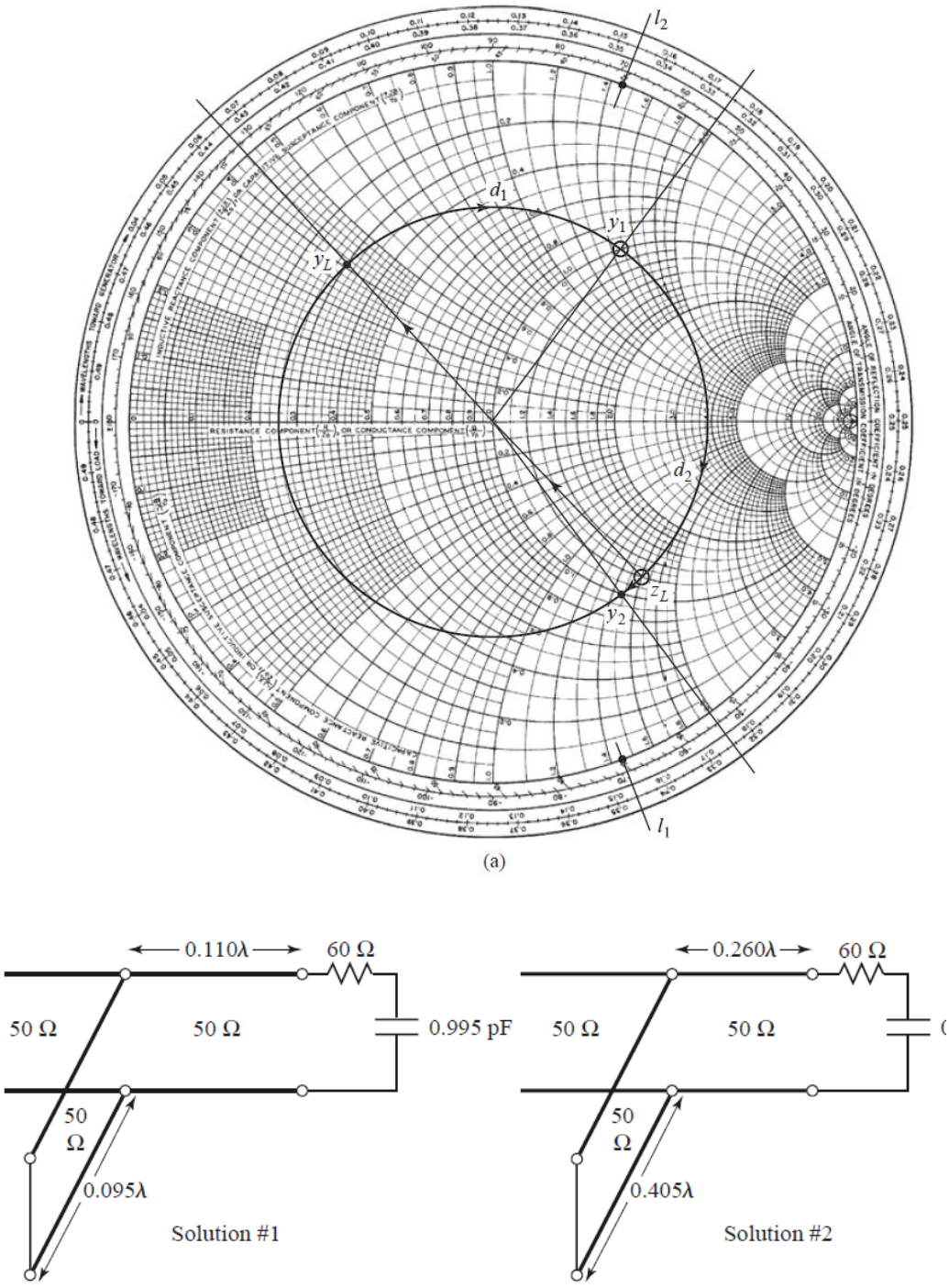


Fig 2.21 example of a). how to use smith chart for the shunt-stub; b). shunt-stub solution [6]

Before we throw everything into simulator, we want to get a feeling on how long the *d* and *l* would be. We will use Fig 2.21 as an example, demonstrating how to estimate *d* and *l* step by step. Instead of showing exactly how to solve this, we vague our single stub is terminated into $A+jB$.

Step 1, transfer the load impedance $A+jB$ to nominal impedance z_L and then to nominal admittance y_L;

Step 2, plot y_L on smith chart;

Step 3, like what we did in series T-Line (it is in fact series T-Line tuning), move y_L on the SWR circuit WTG so it intersects at y_1 with $1+jx$ circle, the electrical distance *d* WTG is the physical distance *d* of series T-Line; (Step 3b, the SWR also intersects with $1+jx$ circle, or any wavelength that is y_1 and y_2 plus half wavelength. However, the shortest possible solution is favorable for better bandwidth.)

Step 4, the shunt T-Line cancels the $+jx$ with $-jx$. If the T-line is terminated with open circuit, the impedance starts from infinite (horizontal axis towards right) on smith chart and rotates WTG to y_1. If the T-line is terminated with short circuit, the impedance starts from zero (horizontal axis towards left) on smith chart and rotates WTG to y_1. The electrical distance *d* WTG is the physical distance *l* of shunt T-Line. Series single-stub works similar to the analysis above. With the analysis above, we can estimate and give an initial value to T-Line and then starts computer calculation.

Such a single-stub tuning circuit is often very convenient because the stub can be fabricated as part of the transmission line media of the circuit, and lumped elements are avoided. Shunt stubs are preferred for microstrip line or stripline, while series stubs are preferred for slotline or coplanar waveguide.

Double-stub:

The single-stub tuner of the previous section is able to match any load impedance (having a positive real part) to a T-Line, but suffers from the disadvantage of requiring a variable length of line between the load and the stub. This is not a problem for a fixed matching circuit, but would probably pose some difficulty if an adjustable tuner was desired. In this case, the *double-stub tuner*, as shown in Fig 2.22, with uses two tuning stubs in fixed positions, can be used.

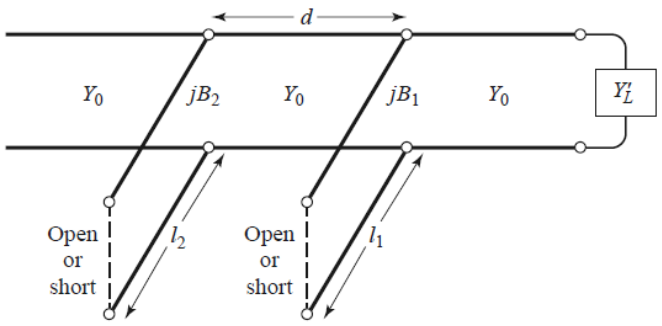


Fig 2.22 double stub tuner [6]

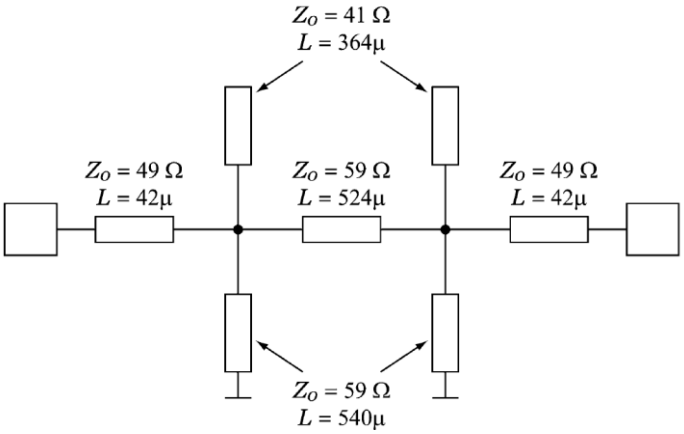


Fig 2.23 example of a double-stub tuner, a CPW filter at 30GHz

Before we move on to impedance matching using transmission line, it is very important what is the estimated impedance T-Line can replace. As shown in equations:

$$Z_{in}(d) = Z_0 \frac{Z_L + jZ_0 \tan \beta d}{Z_0 + jZ_L \tan \beta d}$$

the physical variables are T-line length '*d*' and characteristic impedance Z_0. Since we know the wavelength of 60GHz is 5mm, we can estimate the range of ($tan\beta d$). In this dissertation, the length ranging between 1-200 um, which means ($tan\beta d$) is in the range of (0-1). A realistic characteristic impedance Z_0 is between 3-100Ω.

In respect to the inductance and capacitance, with $(tan\beta d)\ \varepsilon\ (0, 1)$: $jw_L = jZ_0$ $(tan\beta d)$ means the inductance L is 2.5 $\times 10^{-9}$ and higher; $-j\ (1/w_C) = -jZ_0\ (cot\beta d)$ means the capacitance C is basically any value.

In this subsection, we review some basic concept of transmission line and impedance looking into a transmission line. The feature of impedance looking into T-Line can be changed by the T-Line length and characteristic impedance makes impedance transformation possible. This is actually a very common technique nowadays in RF circuit design, mostly used in input/output impedance matching. Single-stub tuner and double-stub tuner were developed by previous scientists to enable a easy way for impedance matching.

2.4.3 Microstrip line VS Waveguide (transmission line in CMOS)

CMOS technology is primarily used for digital circuit application, therefore the typical epi-substrate is low-resistivity bulk silicon. This appears to be a major limitation in multigigahertz applications. Prior works [7] proved microstrip line and coplanar waveguide (CPW) are the best potential choices for constructing an on-chip transmission line.

Microstrip line on silicon is implemented with top-layer metal as signal path, and the bottom-layer metal as ground plane. Fig 2.24 a) shows the effectiveness of the metal shield, with essentially no electric field penetration into the substrate. The shunt loss, G, is therefore due only to the loss tangent of the oxide, yielding a capacitive quality factor, Q_C, of around 30 at mm-Wave frequencies. The biggest drawback to

microstrip lines on standard CMOS is close proximity of the ground plane to signal path (about 4μm). That leads to a very small distributed inductance L and in turn a very small inductive quality factor Q_L.

CPW, on the other hand, is using a top-layer metal signal path surrounded by two adjacent grounds. The signal width, W, can be used to minimize conductor loss, while the signal-to-ground spacing, S, controls the Z_0 and the tradeoff between Q_L and Q_C. Usually, CPW T-Line are preferred over microstrip line due to their considerably higher Q_L compared to microstrip lines. Higher Q_L means higher availability of characteristics impedance Z_0. In the following simulations, we will use the Z_0 as variable. The flexibility of Z_0 can provides better circuit performance. Therefore, CPW is used as T-Line in our dissertation. Prior works have demonstrated Z_0 can varying from 10-90Ω, so we will assume Z_0 can change from 3-100Ω in our design.

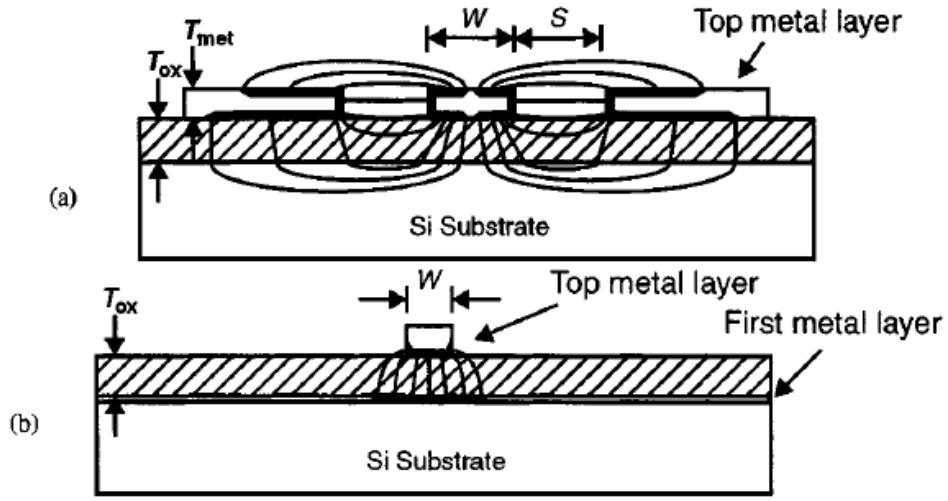


Fig 2.24 Illustration of electric field lines and current distribution due to skin effect in (a) coplanar waveguide (CPW) and (b) microstrip line in CMOS technology.

2.5 Mixers

In receiver architecture, the input signal is at 60GHz and the output signal is at baseband frequency, usually at 2.16GHz which is the bandwidth per channel. Most circuit are linear and time invariant, like LNA and filters, which cannot change the frequency of signal. Mixer, on the other hand, is a linear circuit block depends fundamentally on a purposeful violation of time invariance. Therefore, mixer in receiver architecture provides the frequency transition from RF to baseband

frequency. The frequency transition is realized by multiplication of two signals in time domain as:

$$(A\cos\omega_1 t)(B\cos\omega_2 t) = \frac{AB}{2}[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t]$$

where the output on the right side of equation has new frequencies $\omega_1 - \omega_2$ and $\omega_1 + \omega_2$.

2.5.1 Mixer figure of merits

A good mixer performance is defined by conversion gain, noise figure and linearity and isolation.

Conversion gain is defined as the ratio of the desired IF output to the value of the RF input. For a mixer defined as equation above, the conversion gain is the IF output, $AB/2$, divided by A (assuming A is the RF input and B is the LO input). Hence, the conversion gain is $B/2$, or half of the LO amplitude.

The definition of noise figure, which is signal-to-noise (SNR) at RF input divided by SNR at output. This definition also applies to mixer characteristics. However, due to the presents of image signal, there are two noise figures used in mixer definition, single-sideband noise figure (SSB NF) and double-sideband noise figure (DSB NF). Both SSB and DSB will have the same IF output signal and noise power, but DSB will have double signal power at input end. Therefore, the DSB NF is usually 3dB

lower than SSB NF. To accurately characterize noise performance of mixer, SSB NF should be used, but if stated without any indication whether it is DSB or SSB one may assume that DSB is being quoted [Thomas Lee's book]. From system perspective (Friis equation), the noise performance of mixer is not priority and not as important as LNA. Usually a tolerable SSB NF ranges from 10dB to 15dB.

Linearity and distortion are defined by 1-dB compression point, similar to other circuit components like LNA. However, in mixer distortion may also come from intermodulation distortion (IMD). Assuming two-tune are desired signal ω_{RF1} and potential interferer ω_{RF2} , and third-order are $2\omega_{RF1} \pm \omega_{RF2}$ and $2\omega_{RF2} \pm \omega_{RF1}$. If $2\omega_{RF1} - \omega_{RF2}$ or $2\omega_{RF2} - \omega_{RF1}$ close to desired signal ω_{RF1}, it adds to output signal power but contains dis-proportional information signal. This IMD can be expressed by third-order interception point (as shown in Fig. 2.25).

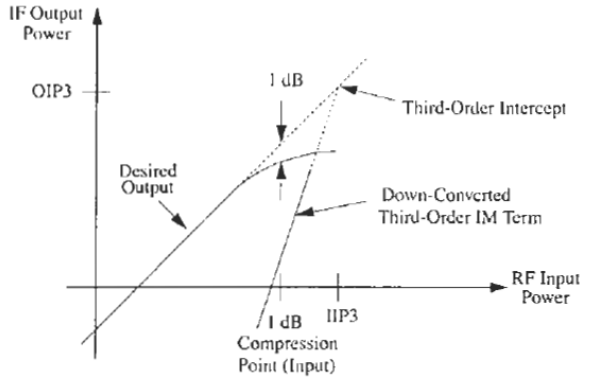


Fig 2.25 Definition of mixer linearity parameters [5]

Since the LO power is usually very large, to provide sufficient conversion gain, the interaction among three ports RF/LO/IF are also very important. That can be measured by S-parameters, like S21, S31 and S32.

2.5.2 Mixer topology

The core question in mixer design is how to provide a multiplication of two signals.

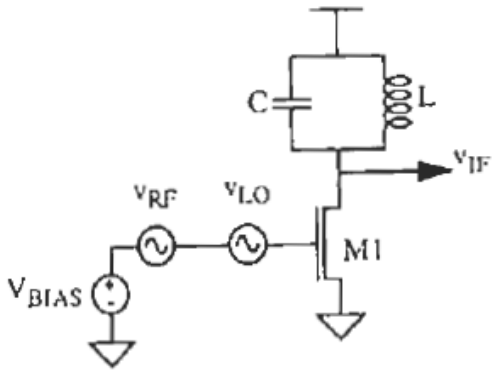


Fig 2.26 Square-law MOSFET mixer (simplified) [5]

One way to realize multiplication is using the square-law of MOSFET, as shown below in Fig 2.26. The input v_{IN} is the sum of RF signal and LO signal.

$$v_{IN} = v_{RF}\cos(w_{RF}t) + v_{LO}\cos(w_{LO}t)$$

and the output v_{OUT} is the sum of three distinct components:

$$v_{OUT} = v_{fund} + v_{square} + v_{cross}$$

where

$$v_{fund} = c_1[v_{RF}\cos(w_{RF}t) + v_{LO}\cos(w_{LO}t)]$$

$$v_{square} = c_2\{[v_{RF}\cos(w_{RF}t)]^2 + [v_{LO}\cos(w_{LO}t)]^2\}$$

$$v_{cross} = 2c_2 v_{RF} v_{LO}[\cos(w_{RF}t)\cos(w_{LO}t)]$$

The advantage of square-law MOSFET is the unwanted signal v_{fund} and v_{square} are all fairly easy to remove by filter. The disadvantage, however, is only long channel devices are square-law MOSFET. In 60GHz applications the use of short channel devices, which are needed to increase f_t, is a must. Short channel devices are more linear as a results of velocity saturation. Therefore, this topology is not preferred in 60GHz mixer design.

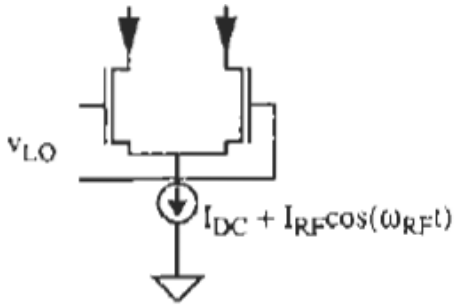


Fig 2.27 Single-balanced mixer [5]

The other method to realize multiplication is multiplier-based mixers. Fig 2.27 shows a way to accomplish multiplier-based mixer design, single-balanced mixer. The RF input feeds into the tail transistor and LO is chosen large enough to alternately switch the tail current from one side to the other. The switch signal, provided by LO, can be expressed in Fourier series:

$$sgn(\cos(w_{LO}t)) = \frac{1}{2} + \frac{2}{\pi}\cos(w_{LO}t) - \frac{2}{3\pi}\cos(3w_{LO}t) + \cdots$$

and we can safely ignore the higher order components, making Eq X to be:

$$sgn(\cos(w_{LO}t)) = \frac{1}{2} + \frac{2}{\pi}\cos(w_{LO}t)$$

with only DC and w_{LO} in frequency domain. The tail current is given as:

$$i_{out}(t) = sgn(\cos(w_{LO}t))\{I_{BIAS} + I_{RF}cosw_{RF}t\}$$

which has the function of $\cos(w_{RF}t) \times \cos(w_{LO}t)$.

As equation above shows the DC component is inevitable in single-balanced mixer. This DC component can be canceled in double-balanced mixer, as known as Gilbert-Cell, as shown Fig 2.28.

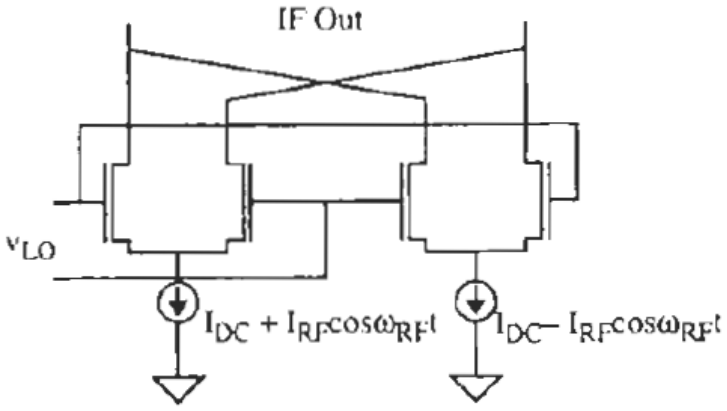


Fig 2.28 Active double-balanced mixer [5]

Summary:

In this chapter, we review the general concepts of receiver and major key blocks that will be needed in receiver design. The review starts from receiver system specs and system design. This step gives us an idea of how each individual component specs would be. Then we reviewed the amplifier and LNA design, which is a special case of amplifier but more focused on power/noise match. This lays the foundation of the future LNA design. After that, T-Line basics is review here in this chapter. In mm-Wave, T-Line is a major and inevitable part of circuit design for impedance matching, filters and etc. At last, to complete receiver design, mixer design is reviewed.

Chapter 3 Noise in LNA and Noise Canceling LNA

The sensitivity of communications systems is limited by noise, and the noise performance is defined by Noise Figure (NF). Recall the definition from Chapter 2, NF is defined as:

$$NF = 10log_{10}(F) = 10log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right) = SNR_{in,dB} - SNR_{out,dB}$$

Where the F is noise factor:

$$F = \frac{SNR_{in}}{SNR_{out}}$$

The noise figure can also be presented as:

$$F = \frac{N_a + kT_0BG}{kT_0BG}$$

where *Na* is noise added in the system, *k* is Boltzmann's constant ($1.38 \times 10^{-23} J/K$), *B* is the amplifier bandwidth in hertz and *G* is the amplifier gain.

From the definition above, the noise factor, or noise figure, is an indicator of how much noise power is added during signal transmission. In this chapter, we will discuss the noise performance of LNA and method to reduce noise figure. First, we will analyze how many noise sources in LNA, and their contributing component. Secondly, the classic noise canceling method is introduced. Lastly, we will discuss the

limitation of classic noise canceling theory, which collapse in high frequencies, and develop an advanced high frequency noise canceling theory in LNA application.

3.1 Noise Model of MOSFET

With the downscaling of channel length into deep-sub-micrometer regime, RF MOSFETs has become good choices for mm-Wave circuit application. There have been several attempts [9] to build models and characterize noise performance of transistor. Before we move on to noise canceling, it is very important to firstly know which noise sources we are dealing with.

In 65-nm CMOS technology process, the equivalent circuit is shown is Fig 3.1. In this detailed extracted noise behavior model of MOSFET transistor, the input resistance R_i and phase delay τ are essential in describing the intrinsic small-signal behavior when operating at close to cutoff frequency (f_t), and the junction capacitance $C_{j,db}$ along with substrate resistance R_b are used to model the RF substrate loss. In addition, the series inductances (L_s, L_d and L_g) are pronounced for the high-frequency operation.

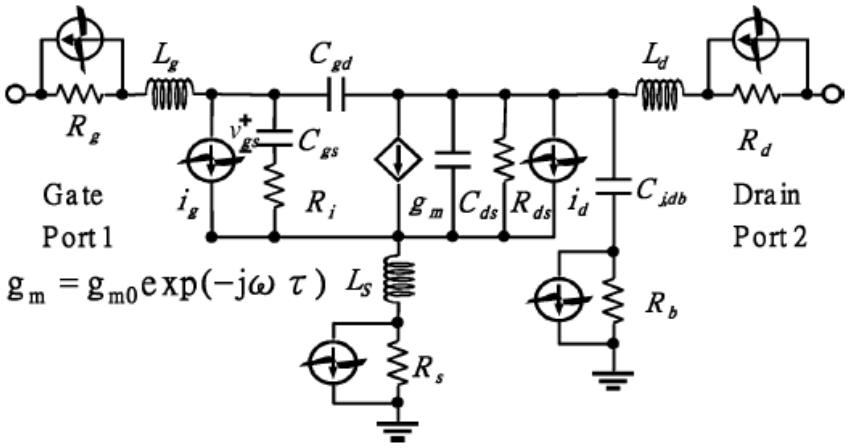
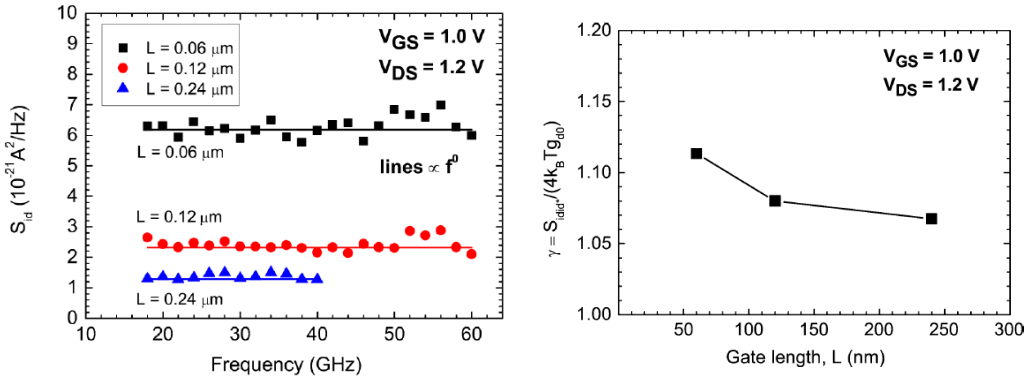


Fig 3.1 RF noise equivalent circuit for bulk MOSFETs. [9]

Detailed experiment and validation are shown in this paper [8]. The conclusion is summarized as follows:



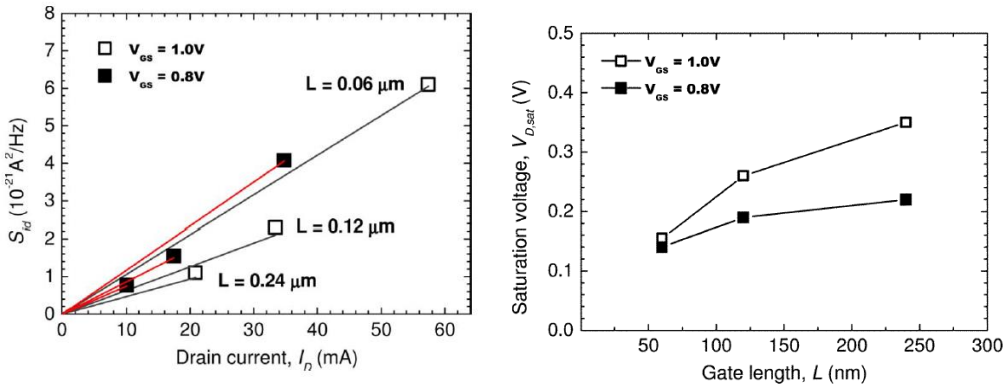


Fig 3.2 a) channel noise versus frequency; b) noise factor γ versus frequency; c) channel noise versus channel length; d) saturation voltage versus channel length [9]

1.) The channel thermal noise (as known as channel noise) is **consistence across all frequencies**;

The channel noise is defined as:

$$S_{id} = 4k_B T \gamma g_{d0}$$

where S_{id} is channel noise denoted as power spectral density ($S_{id} = \frac{i_{nd}^2}{\Delta f}$), k_B is Boltzmann constant, T is the ambient temperature in kelvin, g_{d0} is the channel conductance at zero drain-source voltage, and γ is the noise factor.

2.) The channel noise will increase as the **gate length** reduces;

Channel length modulation is an inevitable phenomenon in 65-nm technology. Therefore, if we take channel length modulation into consideration, the equation X will be rewritten as:

$$S_{id} = 4k_B T I_D \left(\frac{1}{V_{D,sat}} + \frac{\alpha^2 V_{D,sat}}{3V_{GT}^2}\right) \approx \frac{4k_B T I_D}{V_{D,sat}}$$

where I_D is the drain-source current and $V_{D,sat}$ is the drain saturation voltage at which the carriers start to travel with their saturation velocity. I_D and $V_{D,sat}$ increase if we increase channel length L. Therefore, from the equation X and from Fig 3.2 b) we can see the channel noise increases as the channel length reduces.

3.) The channel thermal noise will increase with **drain current** increases;

From both equations above and Fig 3.3 c) we can get this conclusion.

4.) Most importantly, channel noise remains to be the dominate noise source in 60GHz circuits.

The last conclusion is very important because classic noise canceling theories are all targeted to cancel the channel noise. Since the channel noise is still the biggest factor in 60GHz circuits, then the classic noise canceling logistics are still validated.

3.2 Shunt-Series Common Source LNA with Noise Cancellation

In 2004, F. Bruccoleri et. al ([10]-[13]) proposed a wide-band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling, in the hope of minimizing noise figure in low frequency application over a wide frequency band.

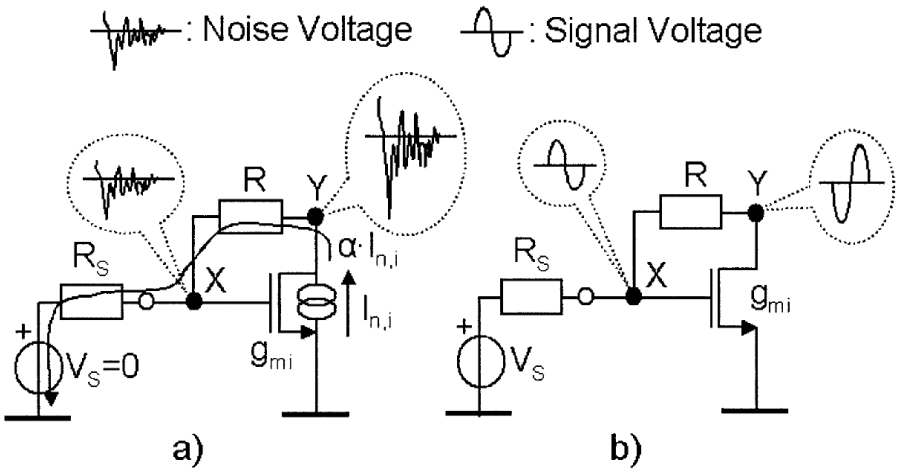


Fig 3.3 Noise Canceling LNA topology and (a) noise, (b) signal voltage at nodes X and Y [11]

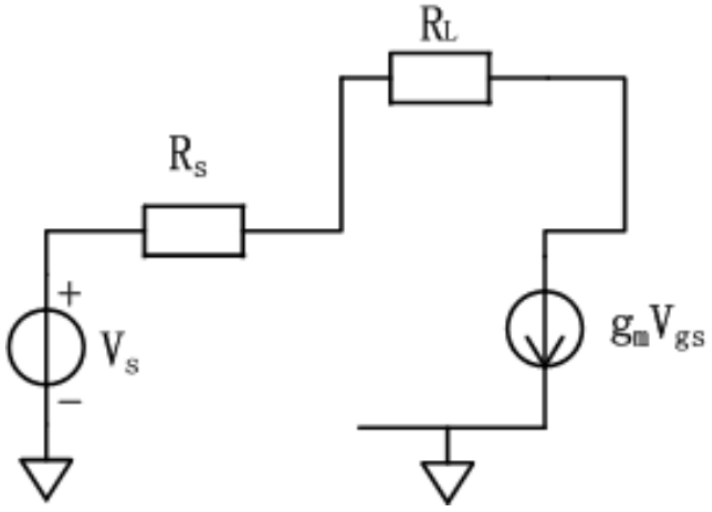


Fig 3.4 Equivalent small signal analysis of Fig 3.3

The noise canceling theory can be illustrated in a behavior model in Fig 3.3, and the equivalent small signal analysis is shown in Fig 3.4. The common source amplifier transistor M_1 is generating an amplified signal from node X to Y, with gain being $1-g_{mi}R_f$, where the g_{mi} is the transconductance of transistor M_1 and R_f is

the feedback resistance. The thermal noise (current) generated by M_1, $i_{n,ds}$, flows out of the transistor and goes from node Y to X. This current noise goes through resistor R and Rs, making noise voltage divided from node Y to X, with a ratio of $V_{n,Y}/V_{n,X} = {}^{R_f + R_S}/_{R_S}$. Give $-g_{mi}R_f > 1$, which is very normal (after all, this is an amplifier we are designing), this noise voltage ratio from node Y to X has an opposite sign of signal gain $1-g_{mi}R_f$. This difference in sign for noise and signal makes it possible to cancel the noise of the matching device, while simultaneously adding the signal contributions constructively.

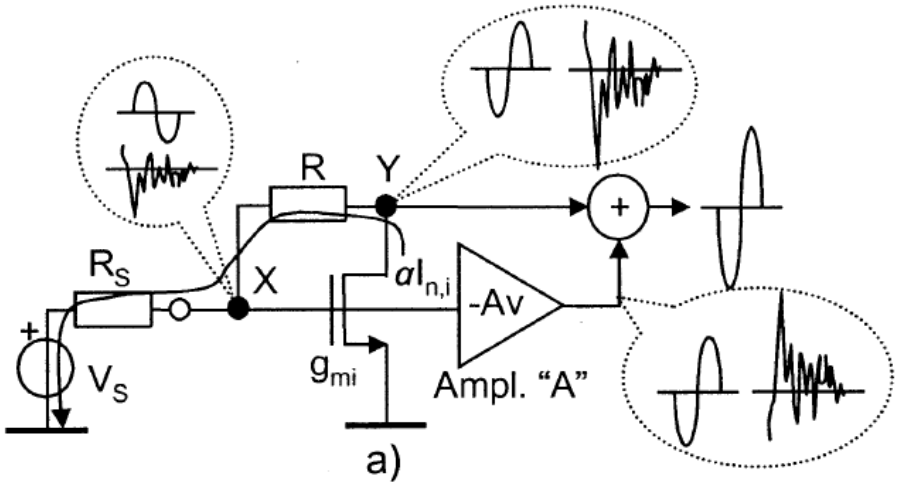


Fig 3.5 Wideband LNA exploiting noise canceling [11]

The noise canceling realization can be achieved by creating a new output, where the voltage at node Y is added to a scaled negative replica of the voltage at node X (as shown in Fig 3.5). A proper value for this scale factor renders noise canceling at the

output node, for the thermal noise originating from the transistor M_1. For simplicity, we can assume:

$$V_{X,n,i} = \alpha(R_s, g_{mi}) \cdot I_{n,i} R_S$$

$$V_{X,n,i} = \alpha(R_s, g_{mi}) \cdot I_{n,i} (R_S + R_f)$$

and making the noise disappear we can make the auxiliary path gain *Av* equal to:

$$A_{v,c} = \frac{V_{Y,n,i}}{V_{X,n,i}} = 1 + \frac{R_f}{R_S}$$

therefore, the overall gain of Fig 3.4 is:

$$A_{VF,c} = \frac{V_{OUT}}{V_X} = 1 - g_{mi} R - A_{v,c}$$
$$= -g_{mi} R - \frac{R_f}{R_S} = -2\frac{R_f}{R_S}$$

However, worth mentioning here is, the key of designing this noise canceling circuit is to find the proper factor value and the proper factor value is not as easy as equation X. The analysis of voltage gain and noise feedback ratio above are greatly simplified. For example, since output Y is not isolated, any load connected to node Y will change the gain of amplifier.

Still, we can draw some conclusion here that will be used in our 60GHz LNA design:

1). Noise canceling depends on the ratio of the source resistance, R_s, and feedback resistance R_f.

2). The cancellation is independent of transconductance, g_{mi}, as it has equally effect on the noise voltage $V_{n,Y}$ and $V_{n,X}$.

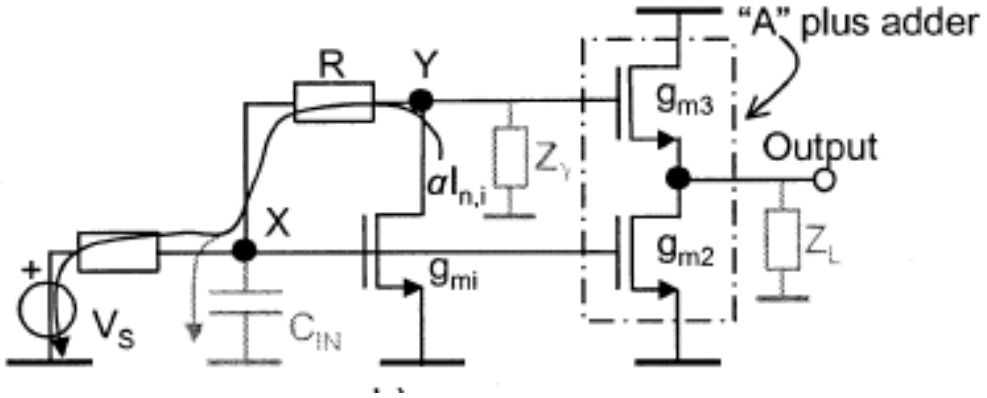


Fig 3.6 Elementary implementation of amplifier A plus adder [11]

To fulfill the logic of Fig 3.4, we can use another common source amplifier M2 as auxiliary amplifier "Av" and common drain amplifier M3 as voltage adder. The complete circuit is draw in Fig 3.6.

3.3 Common Gate LNA with Noise Cancellation

Besides the paper above, there is another topology of noise canceling proposed by Chih-Fan Liao and Shen-Iuan Liu in their paper [14]. That paper, instead of using a common source amplifier, used a common gate amplifier as an example, as shown in the Fig 3.7 below.

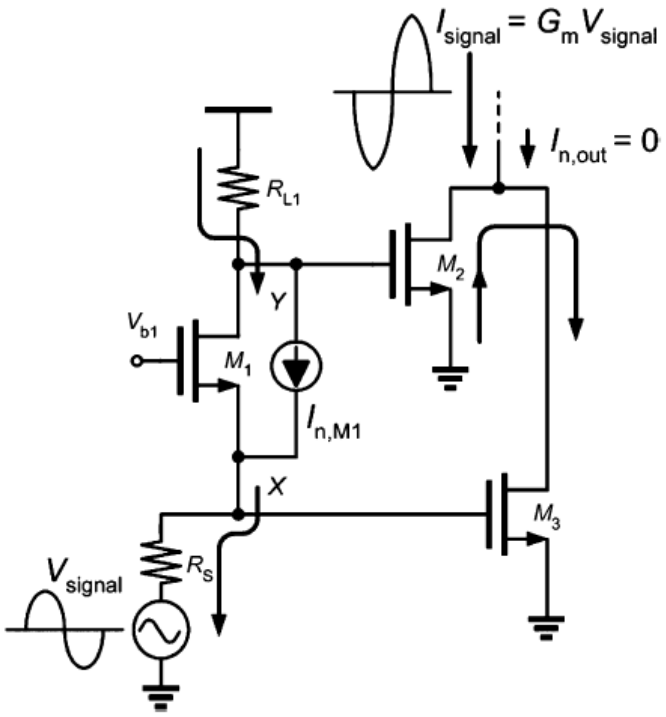


Fig 3.7 Principle of the noise-canceling technique with common gate amplifier [14]

The thermal noise of transistor M1 is modeled as current source $I_{n,M1}$. If we draw a small signal analysis of the topology, we can see the noise voltage V_n is out of phase from $V_{y,n}$ to $V_{x,n}$. The gain of common gate amplifier is gm ($R_L//r_o$), which is a positive gain. The different sign of voltage gain and noise voltage gain creates a possibility of canceling thermal noise and enhancing voltage gain at the same time, just like it was in Common Source Noise Canceling LNA. This topology was reported to be, theoretically, better than CS-NCLNA due to the fact that there is no additional noise introduced in feedback path. Any noise created by the matching devices are modeled

in the $I_{n,M1}$ and will be canceled. Paper [12] provides another method to accomplish the same idea.

3.4 Transformer based Common Source LNA

The common gate Noise Canceling topology is considered to be better than Common Source Noise Canceling in the zero-feedback path noise excitation. To solve the disadvantage of generating noise from feedback resistor R_f, paper [15] provides a novel way to couple signal and noise back to the input. With a transformer (accomplished with L1 and L2) (as shown in Fig 3.8&3.9), the signal and noise at the output of transistor M1 (drain) are coupled back to the input (gate). This topology creates a feedback path that is also free of resistance. However, the performance was not simulated using EM tools, so it's hard to say how it will perform in mmWave region. To my best knowledge, I haven't seen a signal paper on mmWave LNA design with transformer. Not sure if it's the complexity of transformer design in mmWave or it's the EM effect of that transformer on the rest of the circuitry, or both.

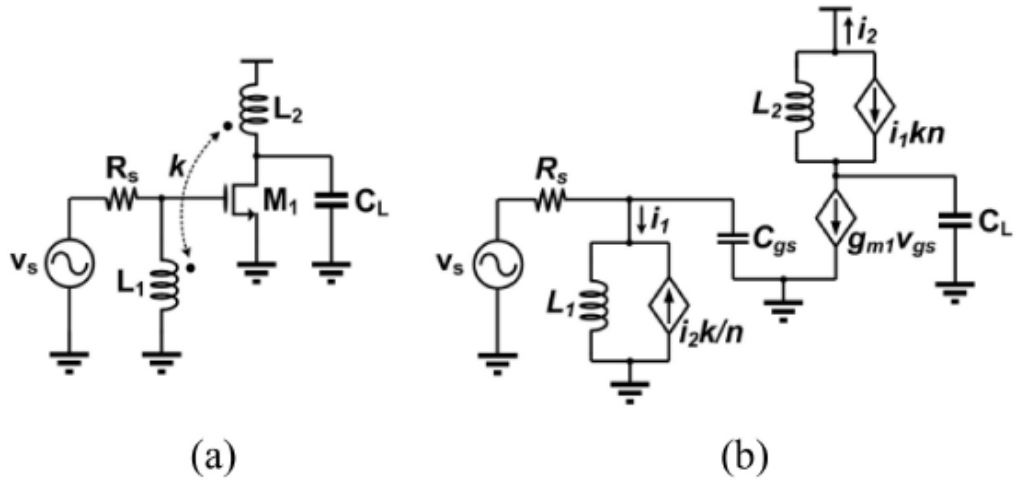


Fig 3.8 Shunt-shunt transformer-feedback LNA: (a) schematic, and (b) a small-signal model [15]

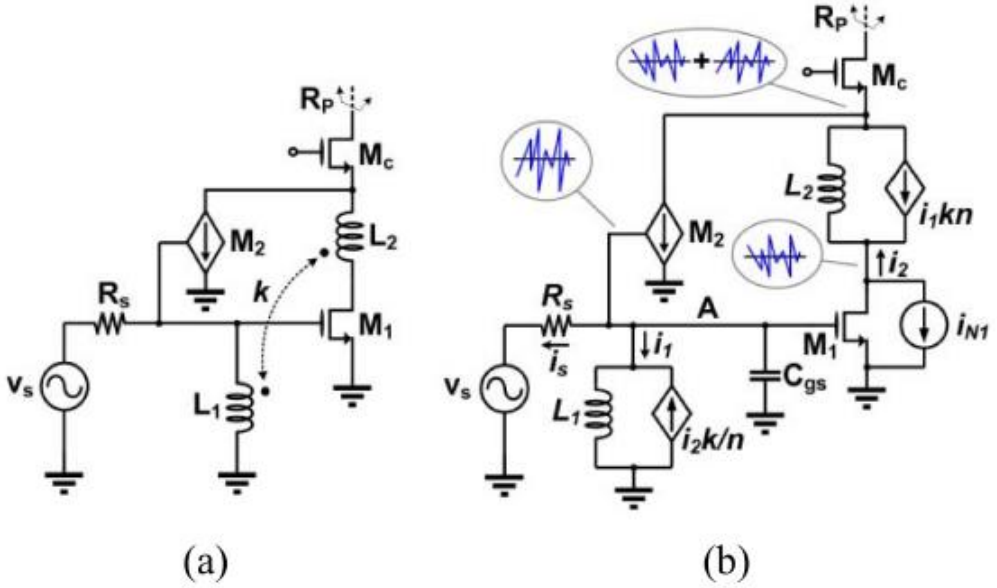


Fig 3.9 Proposed noise cancellation technique: (a) schematic, and (b) a small-signal model [15]

3.5 Transmission Line based Feedback LNA

Apparently, there are other ways to form a “noiseless” feedback path. In general, imaginary impedance is considered as noiseless, like ideal capacitor / inductor / transmission line. Capacitor / inductor are more common in lower frequency applications while transmission line is more common in higher frequencies. In this dissertation, a transmission line based common source amplifier will be proposed and discussed (as shown in Fig 3.10), and a noise-canceling LNA utilizing this type of amplifier will be proposed and validated.

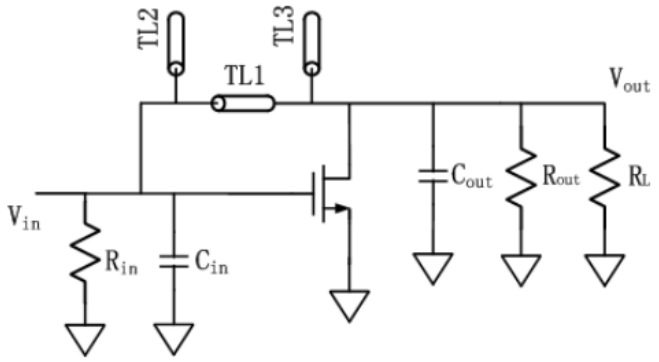


Fig 3.10 Transmission Line based Common Source Amplifier

As will be proved in later chapters, this topology has merits of creating a noise-free feedback path and providing enough degrees of freedom to change the feedback (and feedforward) ratio in both magnitude and phase. However, since transmission line behaves like distributed circuit and the rest of circuit are treated as lumped

circuit, we need special modeling and analysis of how transmission line performs. This will be discussed in Chapter 4.2.

Summary:

In this chapter, well-studied noise canceling were review. The review started with shunt-series common source LNA with noise cancellation. The theory was review in detail because this is the topology as our future NC-LNA foundation. Also reviewed are the CG NC-LNA and transformer-based NC-LNA. Above are three major noise canceling topologies that are published. They are all proven to be very effective in noise reduction. In fact, the logic behind these three papers are the same, creating an architecture that makes the noise and signal have reversed signs. Moreover, it is desirable if the circuit that creates the reversion is noise-free, which are the latter two topologies. In this dissertation, we will focusing on the first topology, shunt-series resistive feedback Common Source Noise Canceling LNA, and push it to mmWave region with a novel topology called transmission line based common source amplifier.

Chapter 4 Noise-Canceling topology in 60GHz

In previous two chapters, basic LNA topologies and noise-canceling LNA topologies are thoroughly introduced. The performance upgrades of Noise-Canceling topologies in sub-6GHz have been shown, but little has been done in mmWave region. There are a lot of difficulties involved, firstly, the modeling of transistor, passive components and even substrate is very complicated due to parasitics; secondly, the gain of a transistor can provide are strongly limited due to the process, which greatly limits the ability of using feedback topology, a critical part of any noise-canceling topology. Now, as the CMOS technology advances, with increased f_t and gain, and as previous researchers developed more accurate MOSFET models in simulators, we can continue developing Noise-Canceling theory in mmWave and verify it in ADS/Cadence.

In this chapter, we will develop two theories that lay the foundation of noise-canceling LNA design at 60GHz, the conjugated impedance and voltage feedback ratio matching, as well as the use of T-Line as a voltage divider for feedback. Firstly, a topology of mmWave noise-cancelling LNA is developed, based on the CS LNA and feedback architecture like discussed before, but included the parasitics effects 60GHz circuitry has. Secondly, as the operating frequency goes into mmWave region,

transmission line becomes a realistic circuit component as the quarter wavelength of 60GHz, 1250μm, is becoming comparable with the size of a chip and can be easily implemented. As we shall see later in this chapter, T-Line has less noise when used as "resistance" and can be modeled/designed more accurately when used as "inductance". Therefore, a T-Line feedback path for voltage dividing purposes is proposed, analyzed and validated.

4.1 Noise canceling limitation and solution in 60GHz

Before we discuss the noise canceling in 60GHz, we first need to review what types of noise we are facing in this frequency region in the technology we use. In chapter 3.1, we have shown the biggest noise source at 60GHz is still the (thermal) channel current noise. In our 65-nm CMOS predictive model [16], simulation results (as in Fig 4.1) proved that for common source amplifier in mm-Wave application, the channel thermal noise, is indeed the most significant noise source in the circuit. From power perspective, the channel thermal noise indicator, MOSFET1.ids, contributes more than 90% of noise power. Therefore, methods can lower this thermal noise will have a great impact on noise performance.

index	port2.NC.name	port2.NC.vnc
freq=55.00 GHz		
0	_total	530.2 pV
1	MOSFET1	530.2 pV
2	MOSFET1.ids	520.8 pV
3	MOSFET1.Rg	52.42 pV
4	MOSFET1.Rbdb	44.50 pV
5	MOSFET1.Rbpb	41.79 pV
6	MOSFET1.flicker	41.66 pV
7	MOSFET1.Rbsb	30.85 pV
8	MOSFET1.Rbpd	24.60 pV
9	MOSFET1.Rbps	7.993 pV
10	MOSFET1.igs	2.862 pV
11	MOSFET1.igd	1.678 pV
12	MOSFET1.igb	629.3 aV

Fig 4.1 Common source amplifier noise contributors

The small signal analysis conducted in previous chapter are all low-frequency/DC equivalent circuit. The capacitors are effectively open circuit and inductors are effectively short circuit. The advantage of low-frequency analysis is one can easily and quickly predict how a circuit will behavior. On the other hand, the disadvantage is that parasitic effects are omitted. The parasitic effect is particular destructive in 60GHz applications.

At higher frequencies, if we take the parasitics into the noise canceling topology, we can redraw the noise canceling LNA as Fig 4.2. C_{IN}, C_Y and C_L are the summing parasitic node capacitors at input/Y/load nodes.

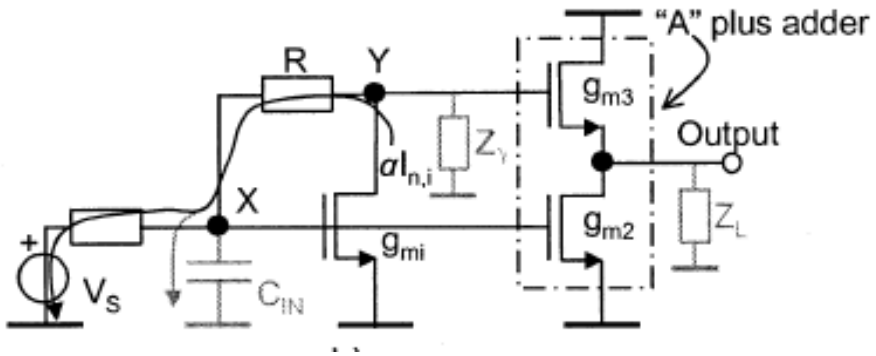


Fig 4.2 high frequency model of NC-LNA [11]

In order to investigate the dominant frequency limitations of noise canceling we can safely assume $C_Y = C_L = 0$, because tehy are not in the feedback path from node Y to X. In Fig 4.2, the C_{IN} is sum effect of gate-source capacitance C_{gs} and gate-drain capacitance $C_{ds,}$ in both transistor M_1 and M_2. The noise current $I_{n,i}$ flows out from transistor M_1 through feedback resistor R_f and 'sees' a complex source impedance $Z_{(s)}$.

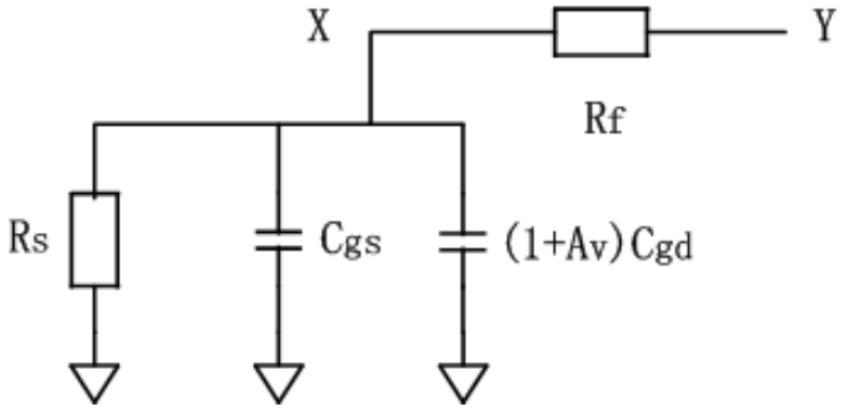


Fig 4.3 the equivalent feedback circuit of noise current from node Y to source

Fig 4.3 shows a simplified feedback path from node Y to X in detail. C_{gs} and C_{gd} is the combination g_s and g_d capacitance. A_v is numerically positive or the absolute value of gain M_1 provides. $(1+A_v)\,C_{gd}$ is the virtual input impedance of transistor M_1 due to Miller effect. From the analysis of noise canceling in pervious chapter, we know that to make noise canceling happens the gain of transistor M_2 provides Av,c is:

$$A_{v,c} = \frac{V_{Y,n,i}}{V_{X,n,i}} = 1 + \frac{R_f}{R_S} \qquad (4.1)$$

At lower frequency, the impedance of C_{gs} and C_{gd} ($\frac{1}{j2\pi f C_{gs}}$ and $\frac{1}{j2\pi f(1+A_{v,c})C_{gd}}$) is large that they are both "open circuit". However, as frequency goes up to 60GHz, both $\frac{1}{j2\pi f C_{gs}}$ and $\frac{1}{j2\pi f(1+A_{v,c})C_{gd}}$ are comparable to R_S. When replacing R_s in equation above, complex impedance $Z_{(S)} = R_f // \frac{1}{j2\pi f C_{gs}} // \frac{1}{j2\pi f(1+A_{v,c})C_{gd}}$ makes equality of Eq 4.1 collapse. Bruccoleri also noticed this high frequency limitation in his paper [12]. He pointed out the mismatch of equation above gets more severe as frequency goes up. From his observation, this mismatch effect with frequency can be modest up to relatively high frequencies because of the low input-node resistance $R_s/2$.

The fact Bruccoleri proved the effectiveness of his noise-canceling theory up to 2GHz gives us confidence in finding a noise-canceling topology at even higher frequency, like 60GHz, as well as drives us to search for an explanation of how the noise-canceling works when it's not operating at DC. Bruccoleri's conclusion that

noise-canceling fails at higher frequency are coming from the real number R_s becomes tue complex value $Z_{(s)}$, while R_f and $A_{v,c}$ remain real. However, neither R_f nor $A_{v,c}$ will remain purely real number as frequency goes up.

On the left side of the equation, $A_{v,c}$, will not be purely real (resistive). In low-frequency analysis, the gain of a common source amplifier is $-g_m R_{load}$. However, as frequency goes higher, R_{load} becomes Z_{load}, where Z_{load} is the combination effect of channel length modulation effective resistor r_0, C_{gd} of transistor M_2 (sometimes referred as current loading effect), C_{gs} of transistor M_3 and load impedance (of the following stage).

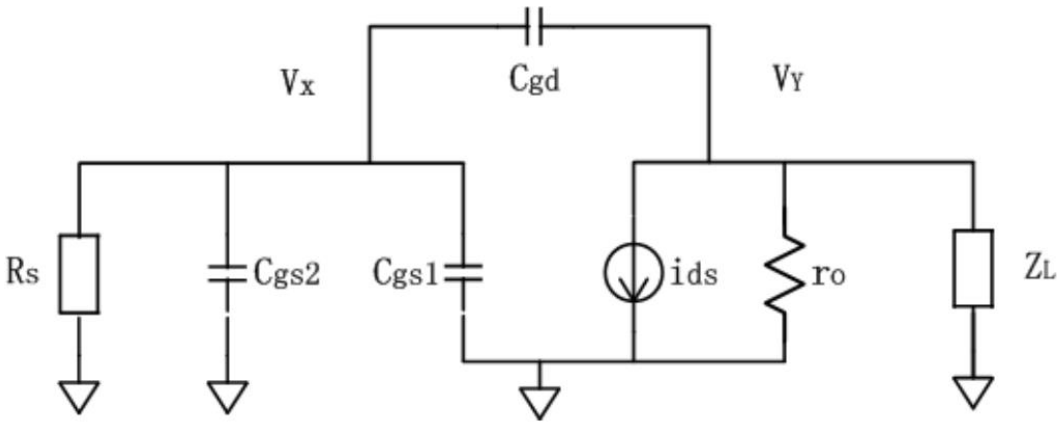


Fig 4.4 the equivalent model of common source amplifier (transistor M2)

From the equivalent circuit above (Fig 4.4), we see that the gain of auxiliary path, $A_{v,c}$, can hardly maintain purely real. Therefore, the left side and right side of

equation 4.1, are both complex value at higher frequencies. However, if the complex gain equals to complex impedance ratio:

$$A_{v,c} = \frac{V_{Y,n,i}}{V_{X,n,i}} = 1 + \frac{R_f}{Z_S} \qquad (4.2)$$

the noise-canceling will still be achievable.

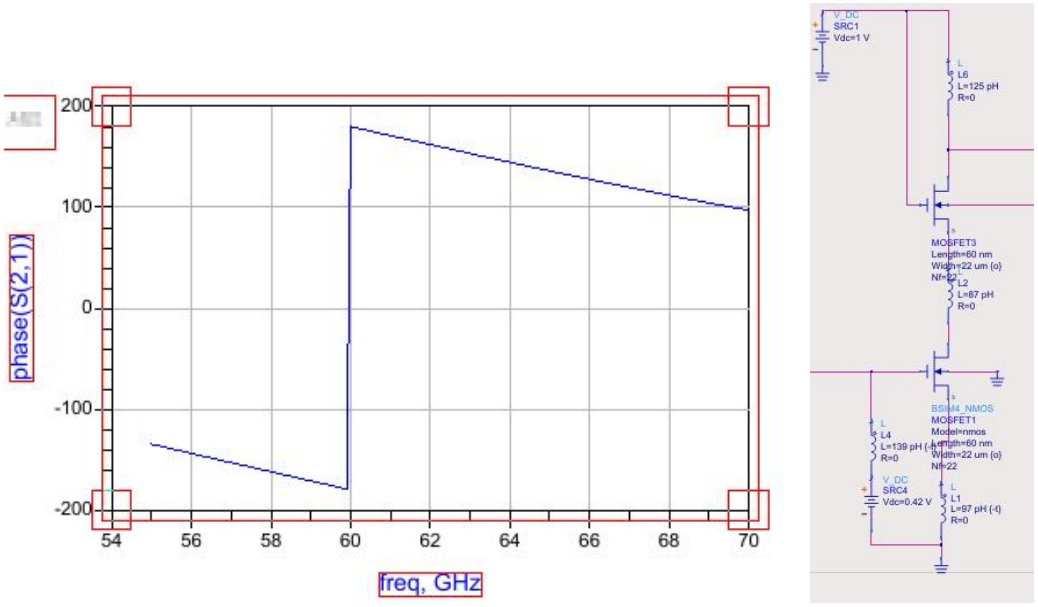


Fig 4.5 Common Source Amplifier S21 phase & testbench

To illustrate the idea of complex gain $A_{v,c}$, in Fig 4.5 is a common source cascode amplifier with inductive load. From the phase plot, we can see the gain doesn't have a constant -180 degree phase (as it would be if $A_{v,c}$ is $-g_m R_{load}$), but a changing phase around -180 degree. (note: the positive phase difference is essentially negative phase shift over -180 degree).

Not only the $A_{v,c}$ and $Z_{(s)}$ in equation above is complex, but also the feedback path, R_f. If we draw a small signal equivalent circuit of transistor M1, as in Fig 4.6, it's clear that the feedback is not purely resistive. In low-frequency analysis, the gate-drain capacitance, C_{gd}, can be treated as open circuit. In the 60GHz range though, the capacitance not only can not be ignored, but load a large portion of AC current from Y to X, in parallel with feedback resistor R_f.

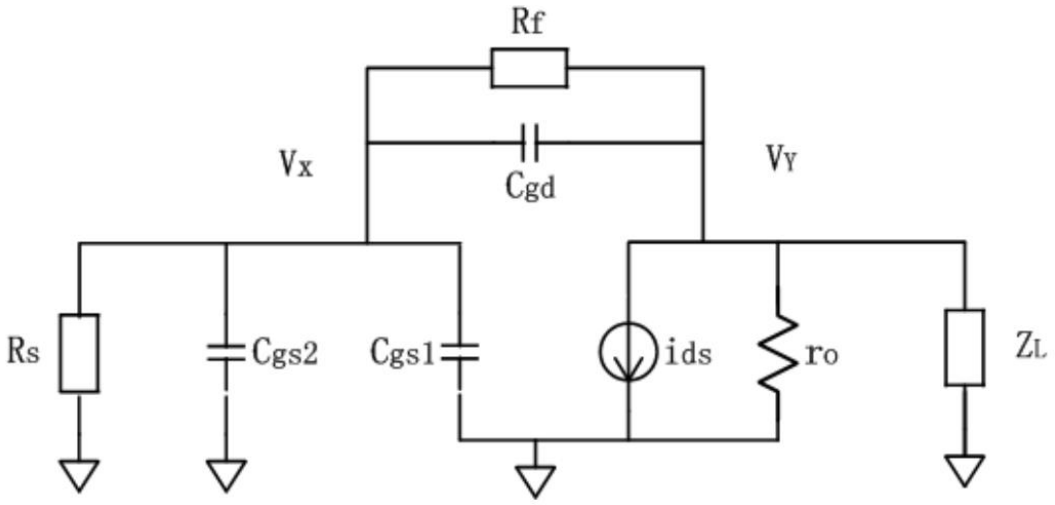


Fig 4.6 the equivalent model of common source amplifier with feedback resistor

To sum up, in LNA circuits, the biggest noise figure contributor, at low-frequency or at high-frequency/mm-Wave frequency, remains to be channel thermal current noise. Therefore, the idea of canceling channel noise to improve noise performance [12] should also be valid at 60GHz application. However, the classic noise canceling theory was developed from low-frequency small signal analysis. The conclusion drew from low-frequency small signal analysis:

$$A_{v,c} = \frac{V_{Y,n,i}}{V_{X,n,i}} = 1 + \frac{R_f}{R_S}$$

is no longer suitable for high frequency circuit.

In reference paper [12], Bruccoleri also pointed out the high frequency limitation of the noise canceling theory. With that being said, he still proved the noise canceling can work up to 2GHz. The author of this dissertation also has two tape-out experiences showing the effectiveness of noise canceling from 1.5-5GHz in previous intern experience at GlobalFoundries with their 22-nm FDSOI technology.

To explain the effectiveness in higher frequencies, new theory was developed and summarized in the equation:

$$A_{v,c} = 1 + \frac{Z_{(f)}}{Z_{(s)}} \qquad (4.3)$$

where $A_{v,c}$ is complex gain, $Z_{(f)}$ and $Z_{(s)}$ are feedback impedance and source impedance respectively.

Furthermore, publications also confirmed: in order to make noise-canceling effective, $A_{v,c}$ doesn't have to be 100% matched to $1 + \frac{R_f}{R_S}$ (or $1 + \frac{Z_{(f)}}{Z_{(s)}}$). This conclusion greatly relaxes the application of noise-canceling LNA and the accuracy needed when designing a feedback voltage ratio.

The Eq 4.3 above seems to be very straightforward. However, the most difficult part in designing 60GHz LNA is to find $A_{v,c}$, $Z_{(f)}$ and $Z_{(s)}$ respectively and match

the equation. We need very accurate models and value of transistor parameters to draw the small signal analysis. Therefore, instead of quantitively match Eq 4.3, we can first qualitatively understand the circuit. Redraw the feedback path from node Y to X in Fig 4.6 as Fig 4.7.

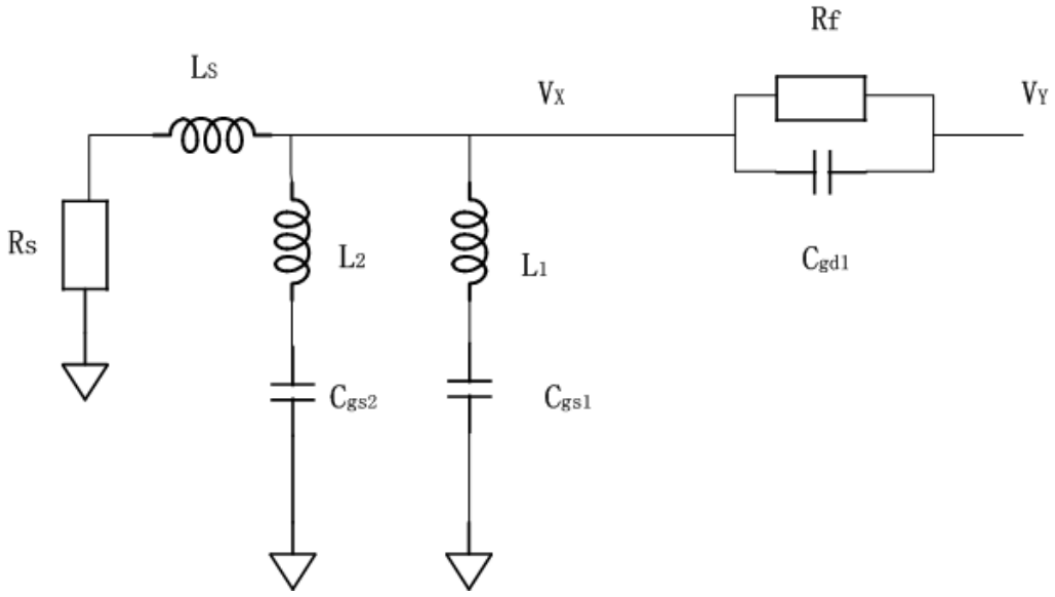


Fig 4.7 the equivalent circuit of Fig 4.6 from node Y to X

Not only the matching of $Z_{(f)}$ and $Z_{(s)}$ is important here, but also the input impedance matching. Looking into the node X, the R_f and C_{gd} are also part of input impedance network. Therefore, to maintain a good input impedance matching and keep equation 4.3 valid, we should provide an extra degree of freedom. To provide that flexibility, L_s, connecting from source to X, and L_1/L_2 connecting from X to gate of transistor M_1 and M_2 are added to the circuit respectively. To get a quantitative

solution to devices parameters, the rest can be done by simulation software like ADS or Cadence.

4.2 T-Line's ability of impedance transformation and voltage dividing

As the frequency goes up and the wavelength goes down, the T-Line has been adopted in RFIC/MMIC designs, in impedance matching network and filters. As we discussed in chapter 2, the fundamental theory behind impedance transformation concerns wave reflection at impedance discontinuities. Since we know the T-Line has the property of changing impedance, and it doesn't generate significant noise, we are motivated to see if we can use transmission line in 60GHz Noise Canceling LNA.

There are two extra motivations for use of T-Line at 60GHz: to design more accurate impedance matching circuitry; and to achieve a feedback voltage ratio that satisfies the noise-canceling requirement. First, for 60GHz impedance matching, the inductance for the lumped LC impedance matching can become so small that is not arcuately available in a 65nm CMOS technology, whereas the T-Line fabrication can be more accurate and reliable. Secondly, in the previous circuit simulations, we noticed that in order to get a better noise canceling, the feedback resistance tends to be high, and that resistor will generate thermal noise in the feedback path which

cannot be canceled. If a T-Line can be substituted, it will introduce minimal excess noise.

We propose using T-Line as feedback path for following reasons: 1. T-Line has been widely used as impedance transformation tool in mmWaves; 2. The reason T-Line being used for impedance transformation is the impedance looking into the T-Line is different from the real load impedance, and the impedance varies with length/characteristic impedance changes; 3. The theory behind the point 2 is the voltage along the T-Line at different geometry point is the superposition of wave feed forward and wave feed backward; 4. The addition/subtraction of wave (which essential is signal) makes the voltage at the input of T-Line and across load impedance different, and by carefully design, the voltage ratio can be controlled; 5. A controllable voltage ratio is “voltage divider”.

To see if it can work, recall the basic principle of Transmission Line in chapter 2.4.

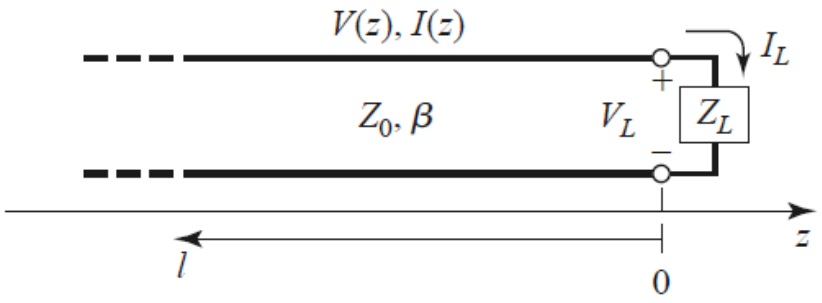


Fig 4.8 A transmission line terminated in a load impedance ZL. [6]

A transmission line terminated in an arbitrary load impedance Z_L is illustrated in Fig 4.8. We know that the voltage along the transmission line is constantly changing, with the sum being:

$$V_{(z)} = V_0^+ e^{-j\beta z} + V_0^- e^{j\beta z}$$

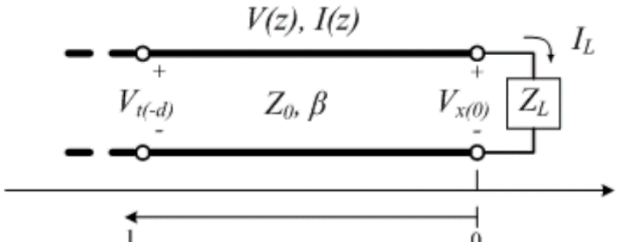


Fig 4.9 Superposition of incident and reflected wave in T-Line

and reflection coefficient Γ is defined as:

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L - Z_0}$$

Usually, we want the reflection coefficient Γ to be zero, meaning there is no voltage reflected, which is achieved by impedance matching. In impedance matching is widely used to deliver maximum power from source to load. However, in our

"voltage divider" application, the zero-reflection feature is not desired. Instead, we want some architecture to realize $(V_Y/V_X) = A_{v.c}$ (the gain of auxiliary amplifier). In other word, we want not a zero reflection, but a reflection so that overall that the overall voltage is at the input/output end of transmission line satisfies $(V_Y/V_X) = A_{v.c}$, with zero phase shift.

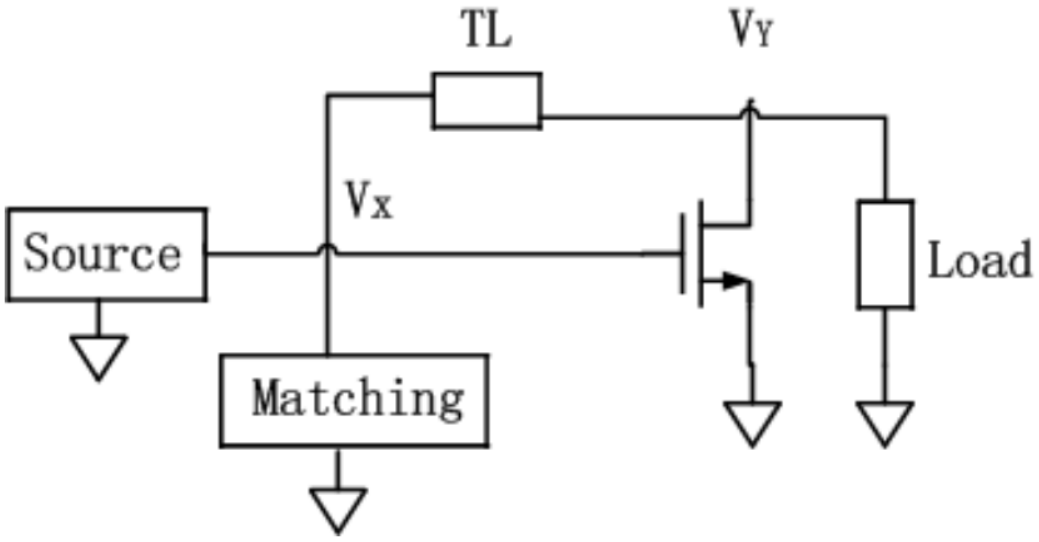


Fig 4.10 the conceptual schematic of the Noise-Canceling LNA with T-Line feedback at mmWave, first stage only

Assuming V_Y is the incident wave V_0^+ at far end and V_X is the voltage V_L seen at the load 'Z_L' when distance $z = 0$. The 'Z_L' in NCLNA is the network of source impedance and matching network impedance in combination. In this application, the maximum power deliver is not prioritized, instead some magnitude of reflected voltage wave is allowed and necessary. Worth mentioning here is the voltage $V_{(Z)}$ can

be both real and complex values. This satisfies the requirements we proposed in chapter 4.1 on complex auxiliary gain.

From the derivation above, we know that the voltages at the two ends of the T-Line is different, that difference is exploited in this dissertation to replace the complex feedback signal path (complex voltage divider). To show the “voltage dividing” feature of T-Line, first the theory proposed above is tested and verified by circuit simulator.

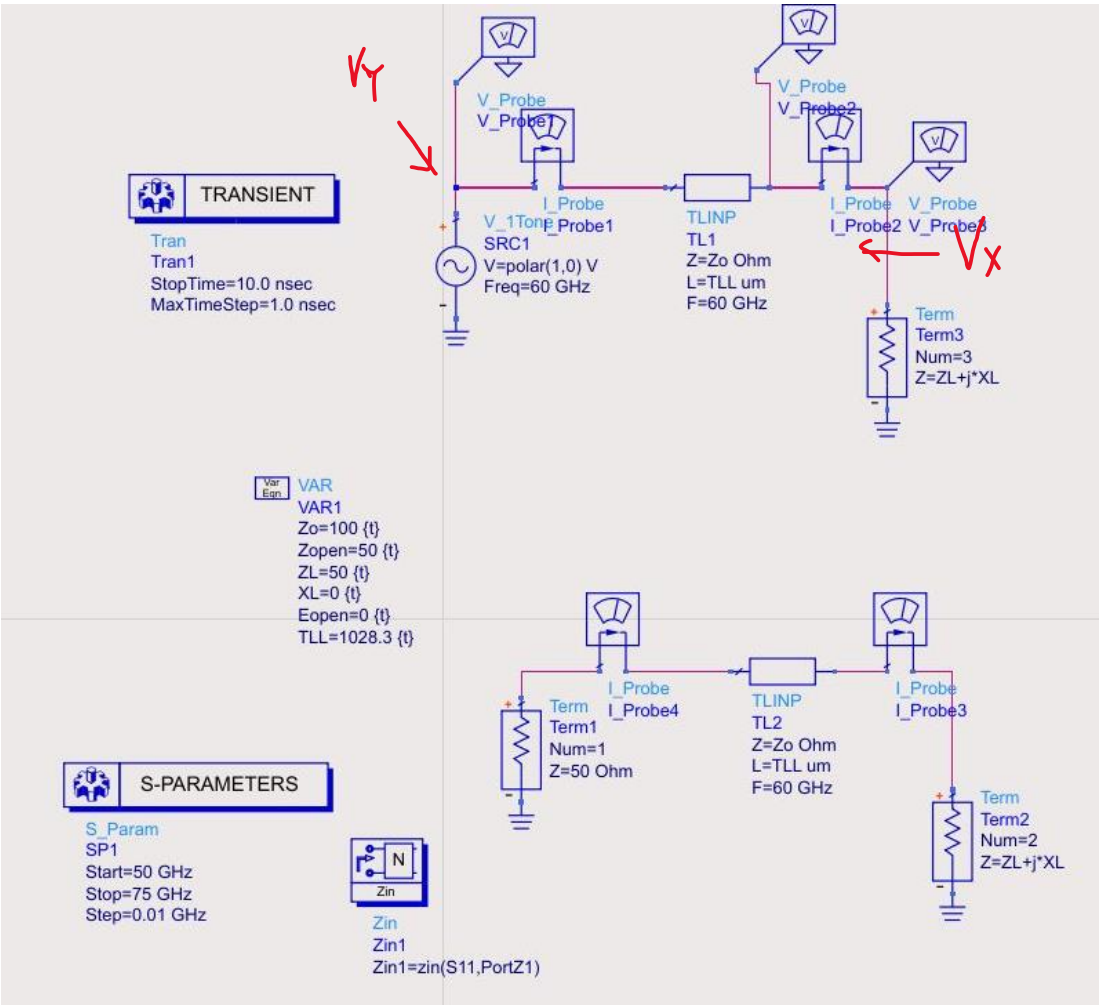


Fig 4.11 testbench of "voltage divider" feature of T-Line

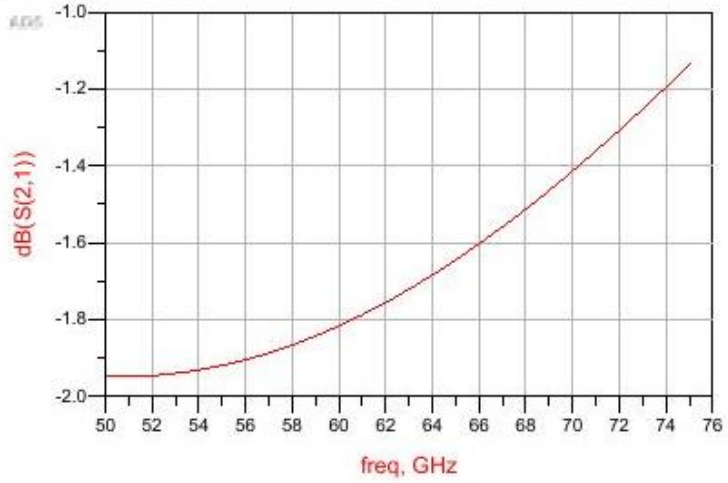
The feasibility of using transmission lines is first explored using ADS. Fig 4.11 shows a schematic of the test circuit of the idea "voltage dividing". The figure shows two identical circuits of a source '*Term 1*', a transmission line '*TL1/2*' and load impedance '*Term 2&3*'. The top half is the 'transient simulation' and bottom half is 's-parameter simulation'. (the reason for dividing into two parts is the time-domain 'transient simulation' in ADS cannot take complex impedance for 'Term 2').

From ‘transient simulation’, we measure the transient voltages at the left side of the T-Line and right side of the T-Line. To make the following expression easier, we assume the voltage at input end ‘V_Y’ and voltage at output end ‘V_X’. From ‘s-parameter simulation’, we measure: 1). The impedance Z_{in} (magnitude and phase) looking into the network of T-line in series of Z_{load}; 2). The voltage gain from ‘*Term 1*’ to ‘*Term* 2’ S21 (magnitude and phase).

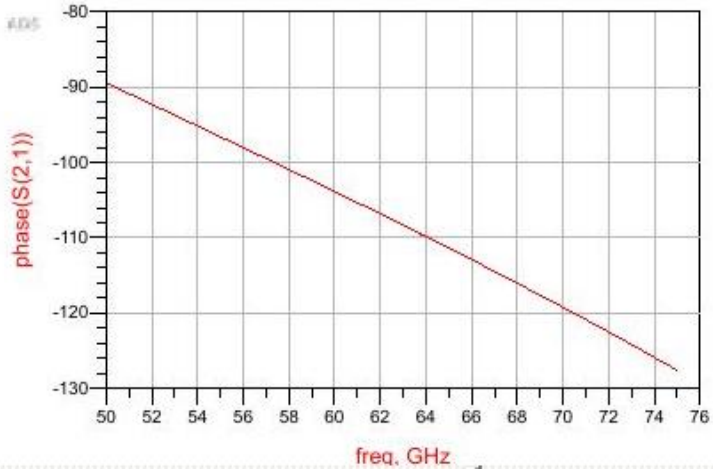
The source impedance is set to be 50Ω and load impedance is set to be variable complex impedance (Z_L+jX_L). The T-Line ‘*TL1/2*’ has two degrees of freedom, intrinsic impedance z = Z_0 (ohm) and length L = *TLL* (μm).

If we give an arbitrary number, say Z_0 = 100Ω, *TLL* = 1000μm, Z_L+jX_L = 50+j0Ω, the results are plotted as below in Fig 4.12. From the graph we can read the V_Y is a small portion of V_X with some degrees of phase shift. The impedance looking into T-Line (as shown in Fig 4.13) is not 50+j0Ω as well, it’s a varying complex impedance whose magnitude and phase change with time.

voltage gain S21 in dB (0 means same voltage from input to output, negative means Vx<VY)



negative means output is ahead of input



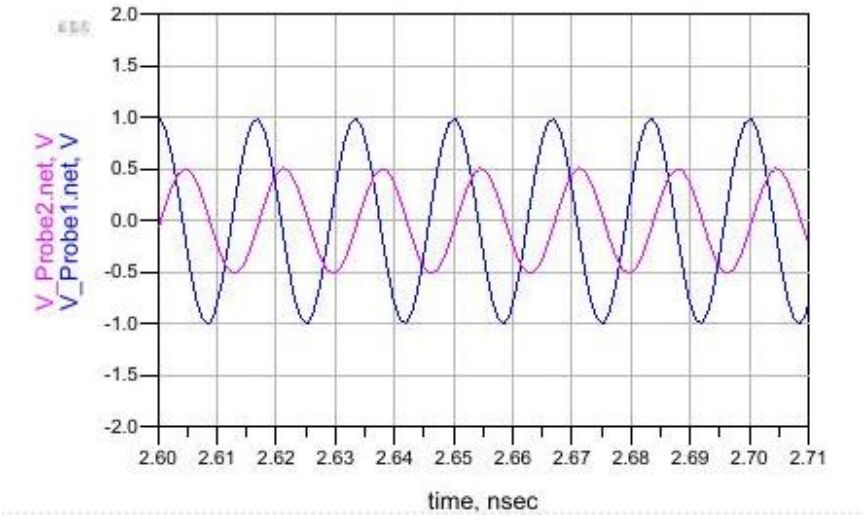
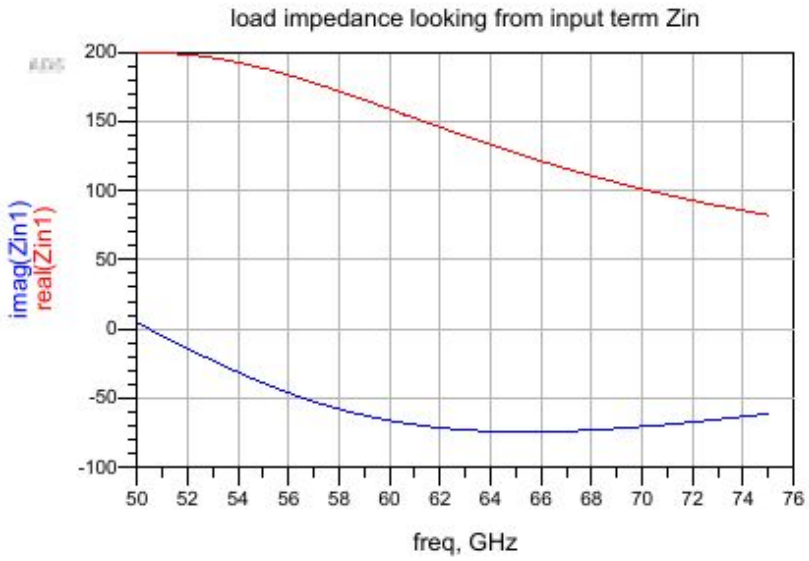


Fig 4.12 simulation results of testbench shown in Fig 4.11. S(2,1) phase and magnitude are shown, transient of “VY” and “VX”


load impedance looking from input term Zin
imag(Zin1)
real(Zin1)
200
150
100
50
0
-50
-100
50 52 54 56 58 60 62 64 66 68 70 72 74 76
freq, GHz

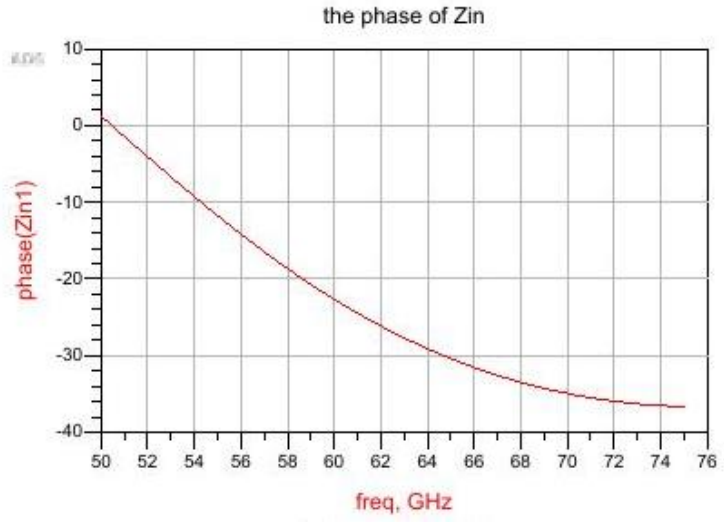

the phase of Zin
phase(Zin1)
10
0
-10
-20
-30
-40
50 52 54 56 58 60 62 64 66 68 70 72 74 76
freq, GHz

Fig 4.13 input impedance looking into T-Line in frequency domain

If we tune the circuit, with the help of shunt stubs matching (as shown in Fig 4.14), we can get to a stage that (V_Y / V_X) are in the range of (0, 1) and in phase. This shows that at least for some specific conditions both input and output voltage can be in phase with different values ("voltage dividing").

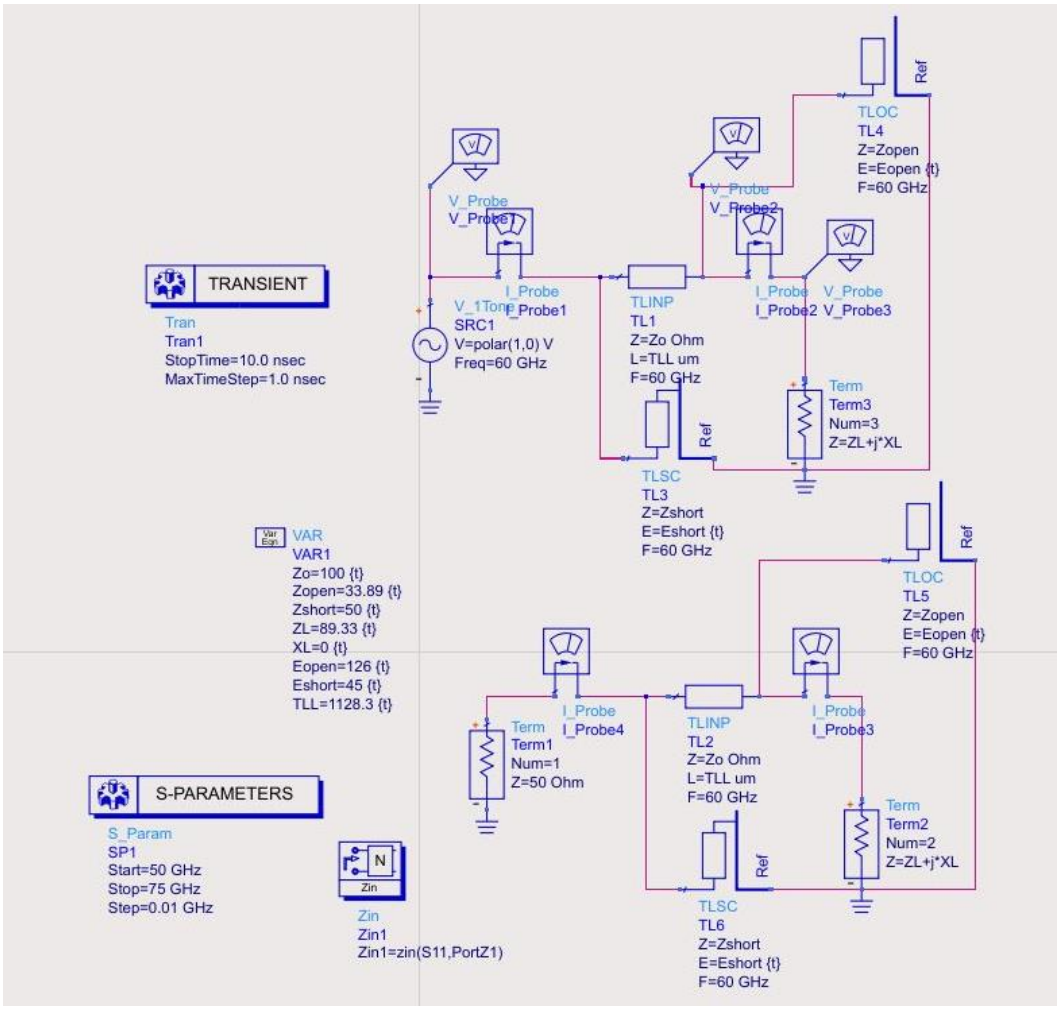
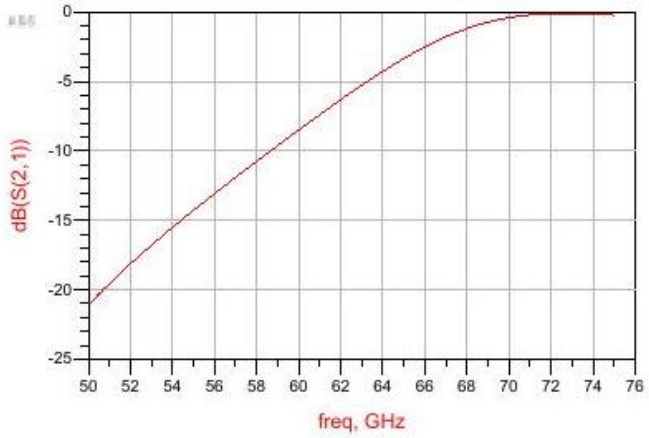


Fig 4.14 testbench of tuned “voltage divider” T-Line

voltage gain S21 in dB (0 means same voltage from input to output, negative means Vx<VY)



negative means output is ahead of input

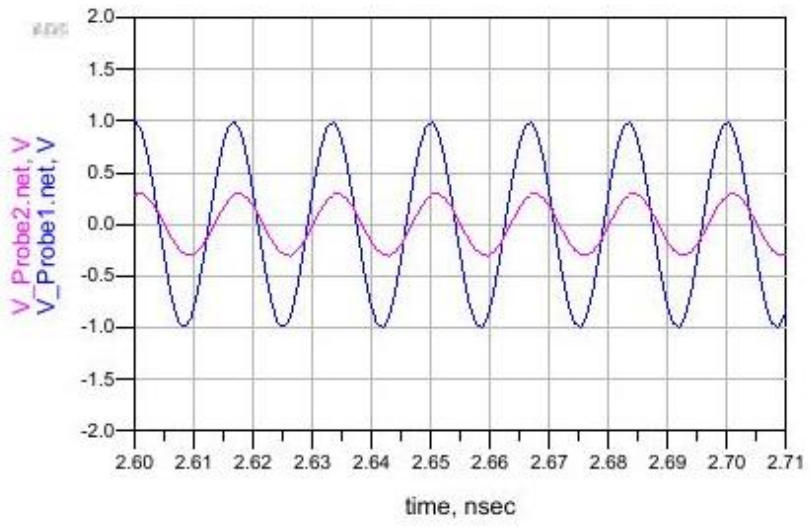


Fig 4.15 simulation results of testbench shown in Fig 4.14. S(2,1) phase and magnitude are shown, transient of "VY" and "VX"

In the noise canceling theory, the essence of noise canceling is to create a feedback path that bring both thermal noise ($i_{n,d}$) and amplified signal from V_Y to V_X, with V_Y/V_X = the amplification the auxiliary path provides. The simulation above shows one example: in 60GHz frequency region, where we can use a carefully matched T-Line to accomplish the 'voltage dividing' results. The advantage of using T-Line dividing the voltage over resistive feedback, or complex feedback contains resistor, is the thermal noise created by the feedback path is neglectable. The noise canceling topology only cancels the thermal noise generated by amplification transistor M1. To demonstrate how much noise the feedback resistor generates, Fig

4.16 illustrates a resistive feedback Noise-Canceling LNA simulation results. The total noise voltage is 1.04nV and noise voltage from the feedback resistor is 456pV. From power point of view, noise power from the feedback resistor is 20% of the whole LNA. On the contrary, in T-Line feedback Noise Canceling LNA the T-Line only (Fig 4.17) generates 120pV noise voltage and that is only 1% of the total noise power.

index	port2.NC.name	port2.NC.vnc
freq=55.00 GHz		
0	total	1.040 nV
1	MOSFET1	665.8 pV
2	MOSFET1.ids	659.3 pV
3	MOSFET1.flicker	66.23 pV
4	MOSFET1.Rg	55.37 pV
5	MOSFET1.Rbpb	24.49 pV
6	MOSFET1.Rbdb	16.69 pV
7	MOSFET1.Rbpd	14.90 pV
8	MOSFET1.Rbsb	7.119 pV
9	MOSFET1.Rbps	7.024 pV
10	MOSFET1.igs	3.743 pV
11	MOSFET1.igd	2.445 pV
12	MOSFET1.igb	1.430 fV
13	MOSFET3	551.8 pV
14	MOSFET3.ids	547.4 pV
15	MOSFET3.flicker	56.48 pV
16	MOSFET3.Rbpb	28.36 pV
17	MOSFET3.Rg	18.28 pV
18	MOSFET3.Rbsb	16.35 pV
19	MOSFET3.Rbps	12.76 pV
20	MOSFET3.Rbpd	8.196 pV
21	MOSFET3.Rbdb	8.184 pV
22	MOSFET3.igs	1.589 pV
23	MOSFET3.igd	1.046 pV
24	MOSFET3.igb	1.649 fV
25	R11	455.9 pV
26	MOSFET4	301.6 pV
27	MOSFET4.ids	292.4 pV
28	MOSFET4.flicker	72.74 pV
29	MOSFET4.Rbpb	7.479 pV
30	MOSFET4.Rbdb	6.290 pV
31	MOSFET4.Rg	5.082 pV
32	MOSFET4.Rbpd	5.027 pV
33	MOSFET4.Rbsb	2.432 pV
34	MOSFET4.Rbps	2.406 pV
35	MOSFET4.igd	1.017 pV
36	MOSFET4.igs	384.0 fV
37	MOSFET4.igb	46.11 aV
38	MOSFET2	181.0 pV
39	MOSFET2.ids	179.8 pV
40	MOSFET2.Rbpb	11.07 pV

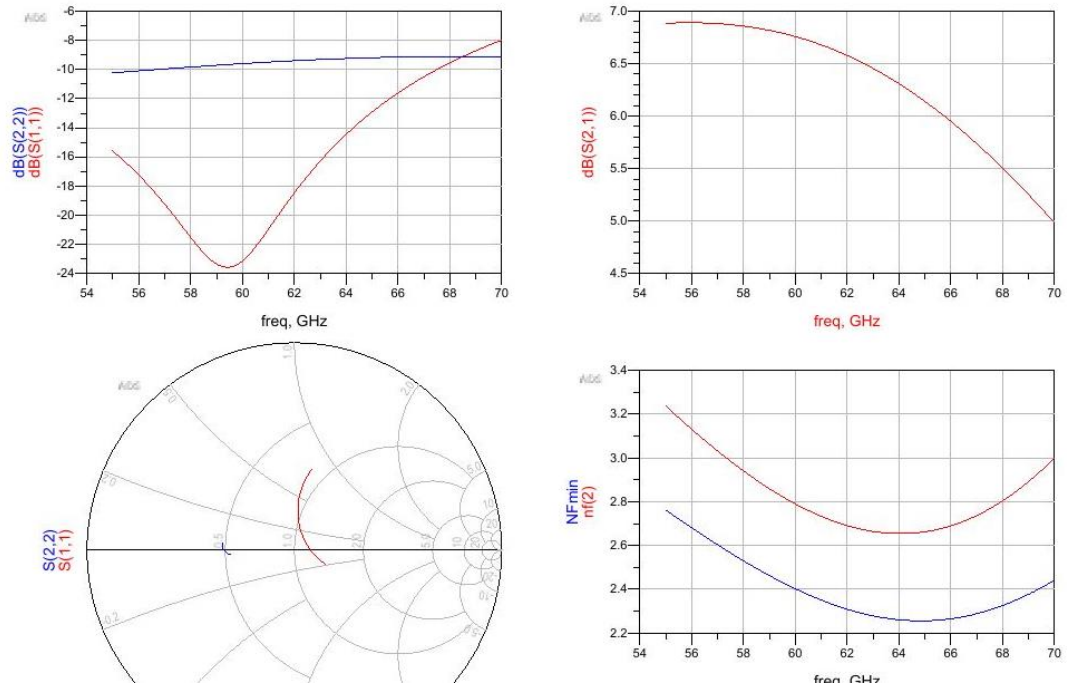


Fig 4.16 simulation results of resistive feedback Noise-Canceling LNA, noise contributors and

S11/S22/S21/NF

index	port2.NC.name	port2.NC.vnc
freq=55.00 GHz		
0	_total	1.192 nV
1	MOSFET2	890.8 pV
2	MOSFET2.ids	881.7 pV
3	MOSFET2.Rg	95.27 pV
4	MOSFET2.flicker	66.37 pV
5	MOSFET2.Rbpb	33.29 pV
6	MOSFET2.Rbdb	28.24 pV
7	MOSFET2.Rbpd	24.15 pV
8	MOSFET2.Rbps	9.614 pV
9	MOSFET2.Rbsb	9.610 pV
10	MOSFET2.igs	3.731 pV
11	MOSFET2.igd	2.222 pV
12	MOSFET2.igb	1.046 fV
13	MOSFET4	600.6 pV
14	MOSFET4.ids	597.6 pV
15	MOSFET4.flicker	37.74 pV
16	MOSFET4.Rbdb	28.68 pV
17	MOSFET4.Rbpd	24.41 pV
18	MOSFET4.Rbsb	20.54 pV
19	MOSFET4.Rbps	16.67 pV
20	MOSFET4.Rbpb	7.491 pV
21	MOSFET4.igs	1.810 pV
22	MOSFET4.igd	1.553 pV
23	MOSFET4.Rg	683.0 fV
24	MOSFET4.igb	3.691 aV
25	MOSFET6	370.1 pV
26	MOSFET6.ids	368.0 pV
27	MOSFET6.flicker	34.18 pV
28	MOSFET6.Rg	13.34 pV
29	MOSFET6.Rbpb	7.857 pV
30	MOSFET6.Rbsb	6.980 pV
31	MOSFET6.Rbps	5.392 pV
32	MOSFET6.Rbpd	2.268 pV
33	MOSFET6.Rbdb	2.268 pV
34	MOSFET6.igd	103.6 fV
35	MOSFET6.igs	17.07 fV
36	MOSFET6.igb	14.43 fV
37	MOSFET3	283.0 pV
38	MOSFET3.ids	278.9 pV
39	MOSFET3.flicker	47.88 pV
40	MOSFET3.Rbpb	2.410 pV
41	MOSFET3.Rbsb	1.448 pV
42	MOSFET3.Rbps	1.160 pV
43	MOSFET3.Rg	699.6 fV
44	MOSFET3.Rbpd	695.8 fV
45	MOSFET3.Rbdb	695.8 fV
46	MOSFET3.igs	647.4 fV
47	MOSFET3.igd	5.860 aV
48	MOSFET3.igb	1.525 aV
49	MOSFET5	212.2 pV
50	MOSFET5.ids	210.8 pV
51	MOSFET5.flicker	21.09 pV
52	MOSFET5.Rg	10.57 pV
53	MOSFET5.Rbpb	4.559 pV
54	MOSFET5.Rbsb	3.855 pV
55	MOSFET5.Rbps	2.931 pV
56	MOSFET5.Rbpd	1.316 pV
57	MOSFET5.Rbdb	1.316 pV
58	MOSFET5.igd	103.0 fV
59	MOSFET5.igb	17.45 fV
60	MOSFET5.igs	0.07794E-18V
61	TL18	47.84 pV
62	TL19	43.15 pV
63	TL15	20.72 pV
64	TL17	8.138 pV
65	TL12	1.248 pV
66	MOSFET1.flicker	[illegible]

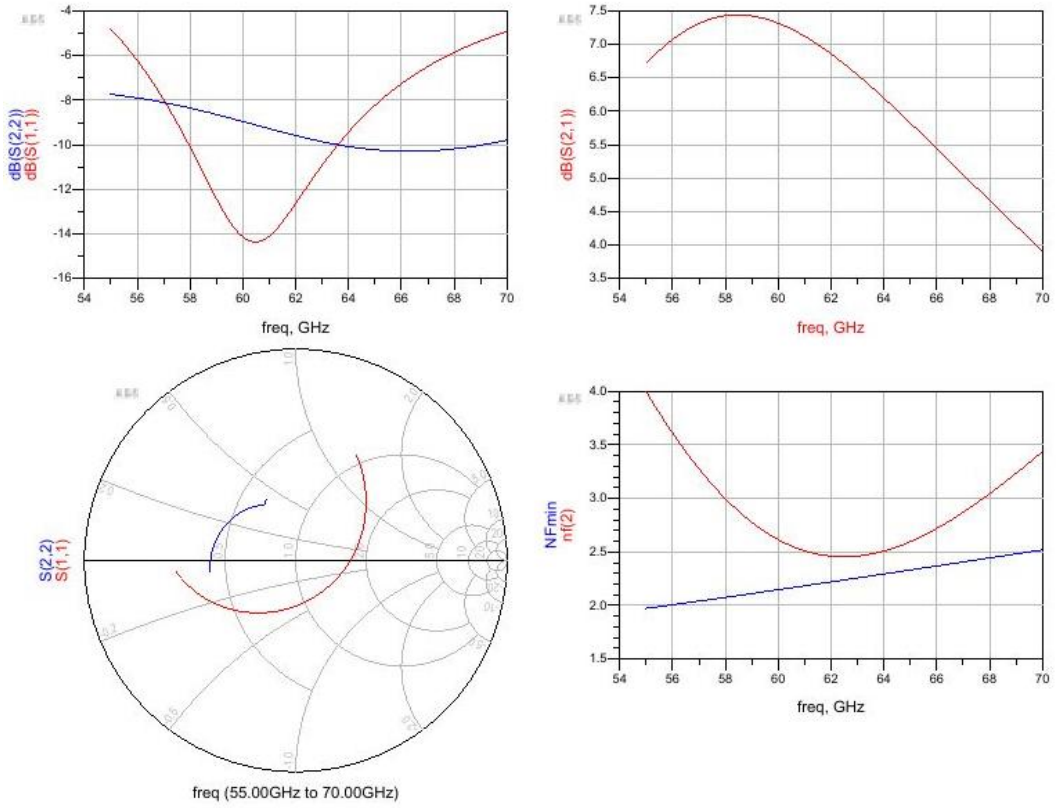


Fig 4.17 simulation results of T-Line feedback Noise-Canceling LNA, noise contributors and S11/S22/S21/NF

4.3 Generalization of T-Line Voltage Dividing

Knowing the T-Line can be used as voltage divider, the next step is to find a way to design the T-Lines to make the voltage ratio match the auxiliary path gain:

$$(V_Y/V_X) = A_{v.c}$$

In this section, a mathematical way of calculating the T-Line feedback ratio is developed, as a guidance of how to set property parameter of T-Line feedback structure.

Let's look at Fig 4.9 again, there is incident wave $V_0^+ e^{-j\beta z}$ and reflected wave $V_0^- e^{j\beta z}$ coexisting at the same time. The voltage seen at each point on the transmission line is the combination effect of both incident wave and reflected wave:

$$V_{(z)} = V_0^+ e^{-j\beta z} + V_0^- e^{j\beta z} \qquad (4.1)$$

where z is the distance from load/transmission line intersection. Let's assume the V_X is when $z = 0$ and V_Y is at $z = -d$. Now we can write V_X and V_Y as:

$$V_{X(0)} = V_0^+ e^{-j\beta 0} + V_0^- e^{j\beta 0} = V_0^+ + V_0^- \qquad (4.2)$$

$$V_{Y(-d)} = V_0^+ e^{j\beta d} + V_0^- e^{-j\beta d} \qquad (4.3)$$

by definition, reflection coefficient Γ is:

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad (4.4)$$

where Z_L is the load impedance and Z_0 is the characteristic impedance of transmission line. Take Eq 4.4 back to 4.2 and 4.3:

$$V_{X(0)} = V_0^+ + V_0^- = V_0^+(1 + \Gamma) \qquad (4.5)$$

$$V_{Y(-d)} = V_0^+ e^{j\beta d} + V_0^- e^{-j\beta d} = V_0^+[\cos(\beta d)\,(1 + \Gamma) + j\sin(\beta d)(1 - \Gamma)] \qquad (4.6)$$

Therefore, we can write the ratio of (V_Y/V_X) as:

$$A_{V,C} = {V_{Y(-d)}}/{V_{X(0)}} = \frac{\cos(\beta d)\,(1+\Gamma) + jsin(\beta d)(1-\Gamma)}{(1+\Gamma)}$$
$$= \cos(\beta d) + jsin(\beta d)\frac{Z_0}{Z_L} \qquad (4.7)$$

From Eq 4.7, we can see draw the conclusion: When feed the voltage from one end of transmission line to the other, the voltage ratio could be any complex, where real term $\epsilon(0,1)$ and imaginary term $\epsilon\left(0,\frac{Z_0}{Z_L}\right)$. The absolute value of ${V_{Y(-d)}}/{V_{X(0)}}$, could be any number from 0 to infinite.

The magnitude and phase of the voltage ratio in Eq4.7 can be rewritten as:

$$Magnitude = \sqrt{cos^2(\beta d) + sin^2(\beta d)\cdot\frac{Z_0^2}{Z_L^2}} = \sqrt{1 + [sin^2(\beta d)\cdot(\frac{Z_0^2}{Z_L^2} - 1)]} \quad (4.7.b)$$

$$Phase = \tan^{-1}\left[\frac{sin(\beta d)\cdot\frac{Z_0}{Z_L}}{\cos(\beta d)}\right]$$
$$= \tan^{-1}\left[tan(\beta d)\cdot\frac{Z_0}{Z_L}\right] \qquad (4.7.c)$$

From this can be seen that a simple transmission line cannot supply a voltage ratio that is in phase unless $\frac{Z_0}{Z_L} = 0$, a condition that is not practical useful. Therefore, more degree of freedom of impedance matching and voltage feedback ratio is desired, meaning more complicated transmission line structure are needed.

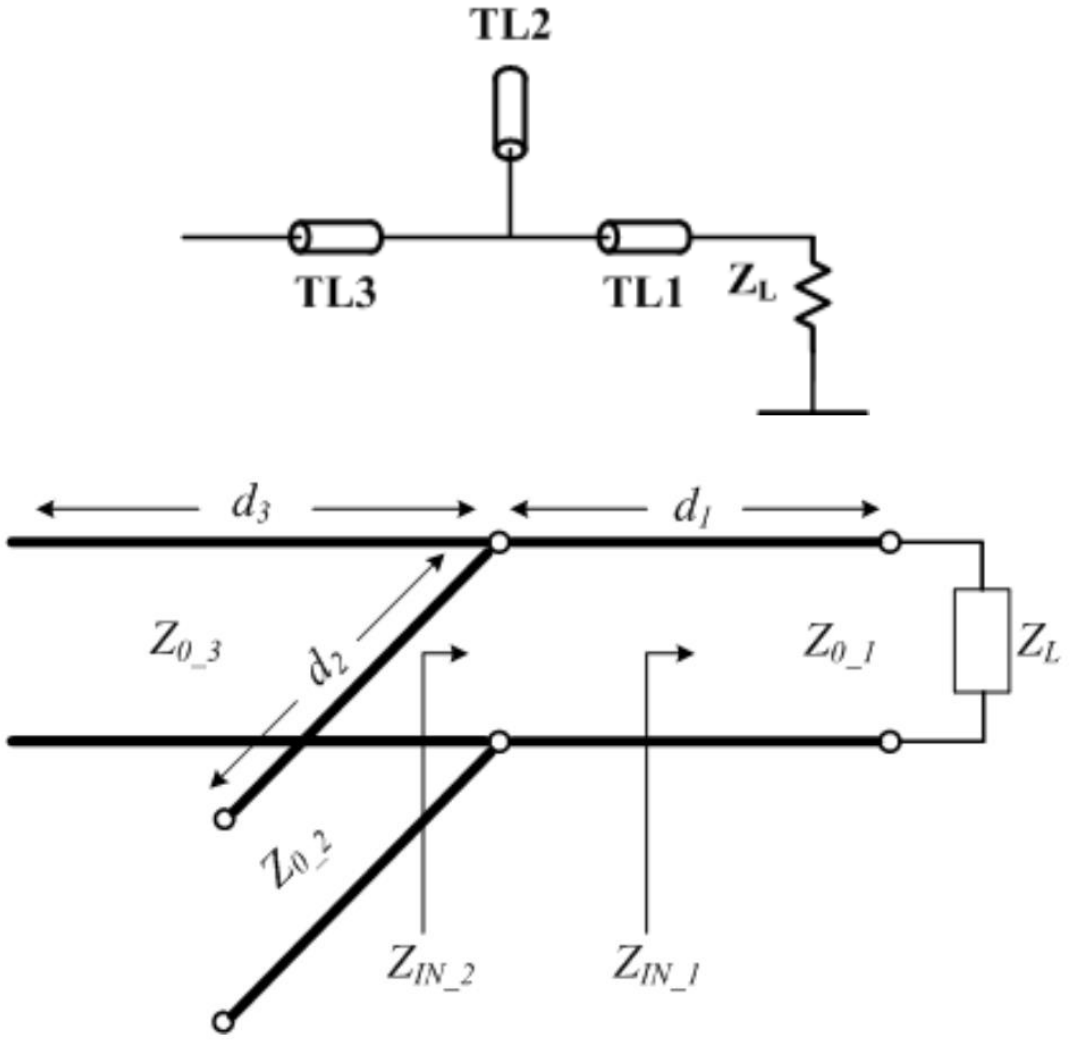


Fig 4.18 series-shunt-series T-Line terminated into a load

As shown in Fig 4.18, a series-shunt-series T-Line structure is terminated into a load Z_L. This type of structure can be analyzed by dividing it to a two pieces cascade system: 1). A transmission line TL1 terminated into load Z_L, which obey the analysis of Eq 4.5-4.7; 2). A shunt stub transmission line TL2 in parallel with (TL1+Z_L), as an

impedance transformer; 3). A transmission line TL3 terminated into a new load described by 1) and 2).

As we discussed, subsystem 1) obeys the analysis of Eq 4.5-4.7, rewritten as:

$$V_{[X\_1](0)} = V_{0\_1}^{+}(1 + \Gamma_1) \tag{4.8}$$

$$\Gamma_1 = \frac{V_{0\_1}^{-}}{V_{0\_1}^{+}} = \frac{Z_L - Z_{0\_1}}{Z_L + Z_{0\_1}} \tag{4.9}$$

$$V_{[Y\_1](-d_1)} = V_{0\_1}^{+}[\cos(\beta d_1)\,(1 + \Gamma_1) + jsin(\beta d_1)(1 - \Gamma_1)] \tag{4.10}$$

$$V_{[Y\_1](-d_1)} \Big/ V_{[X\_1](0)} = \cos(\beta d_1) + jsin(\beta d_1)\frac{Z_{0\_1}}{Z_L} \tag{4.11}$$

where $V_{[X\_1](0)}$ is the voltage at the intersection of load impedance Z_L and transmission line TL1. The $V_{[Y\_1](-d_1)}$ is the voltage at the far end of transmission line TL1 where d_1 distance away from load Z_L. The $V_{0\_1}^{+}$ is the incident wave inside of transmission line TL1. Γ_1 is the reflection coefficient of TL1 and load Z_L.

The subsystem 2), shunt stub in parallel with (TL1+Z_L). Assuming it's an open shunt stub, the impedance of the shunt stub is:

$$Z_{OC}(d_2) = -jZ_{0\_2}\cot\beta d_2 \tag{4.12}$$

and the impedance looking into the shunt stub in parallel with (TL1+Z_L) is:

$$Z_{IN\_2} = Z_{IN_1} // Z_{OC}(d_2) \tag{4.13}$$

where Z_{IN_1}, the impedance looking into (TL1+Z_L) is:

$$Z_{IN\_1} = Z_{0\_1}\frac{Z_L + jZ_{0\_1}\tan\beta d_1}{Z_{0\_1} + jZ_L\tan\beta d_1} \tag{4.14}$$

Therefore, we can rewrite Z_{IN_2} as:

$$Z_{IN\_2} = Z_{IN_1} // Z_{OC}(d_2) = [Z_{0_1} \frac{Z_L + jZ_{0_1} \tan \beta d_1}{Z_{0_1} + jZ_L \tan \beta d_1}] // [-jZ_{0\_2} \cot \beta d_2] \quad (4.15)$$

These are the impedance transformations discussed previous.

Now for the subsystem 3), since there is impedance discontinuity from subsystem 3 to subsystem 2, there are (voltage) wave reflections as well, the voltage at the intersection of subsystem 2 and 3 is:

$$V_{[X\_3](0)} = V_{0\_3}^{+}(1 + \Gamma_2) \quad (4.16)$$

where $V_{0\_3}^{+}$ is the incident wave in transmission line TL3. Although there is impedance discontinuity at the intersection of TL1 and TL3, the voltage is not. Therefore, we have:

$$V_{[X\_3](0)} = V_{[Y\_1](-d_1)} = V_{0\_1}^{+}[\cos(\beta d_1)\,(1 + \Gamma_1) + jsin(\beta d_1)(1 - \Gamma_1)] \quad (4.17)$$

now that we know:

$$V_{[Y\_3](-d_3)} = V_{0\_3}^{+}[\cos(\beta d_3)\,(1 + \Gamma_2) + jsin(\beta d_3)(1 - \Gamma_2)] \quad (4.18)$$

where Γ_2 is:

$$\Gamma_2 = \frac{Z_{IN\_2} - Z_{0\_1}}{Z_{IN\_2} + Z_{0\_1}} \quad (4.19)$$

Now we can write the voltage dividing ratio of two ends of transmission line TL3 as follows:

$$V_{[Y\_3](-d_3)} \Big/ V_{[X\_3](0)} = \cos(\beta d_3) + jsin(\beta d_3) \frac{Z_{0\_3}}{Z_{IN\_2}} \quad (4.20)$$

Therefore, we can combine the equations above and fine a solution for the voltage dividing ratio of $V_{[Y\_3](-d_3)}/V_{[X\_1](0)}$ as follows:

$$V_{[Y\_3](-d_3)}/V_{[X\_1](0)} = V_{[Y\_3](-d_3)}/V_{[X\_3](0)} \cdot V_{[Y\_1](-d_1)}/V_{[X_1](0)} \qquad (4.21)$$

With the assumption stated in Eq 4.17.

Therefore, the conclusion is, for a series-shunt-series transmission line structure, the voltage ratio at two ends is:

$$V_{[Y\_3](-d_3)}/V_{[X\_1](0)} = [\cos(\beta d_1) + jsin(\beta d_1)\frac{Z_{0\_1}}{Z_L}] \cdot [\cos(\beta d_3) + jsin(\beta d_3)\frac{Z_{0\_3}}{Z_{IN\_2}}]$$

This equation will be call cascade transmission line voltage dividing equation for future references.

By dividing complex transmission line structures into cascade of series T-Line terminated into “new load impedances”, voltage dividing analysis can be applied to any T-Line structure a feedback LNA might need.

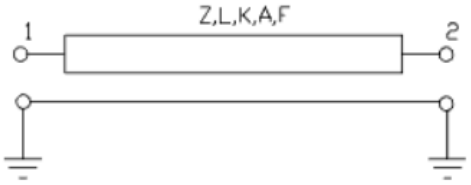
4.5 Noise of Transmission Line

There are, of course, nothing comes without any resistance. The merits of using T-Line to replace the feedback resistor is based on the idea that a T-Line in fact

creates less noise. Intuitively comparing with a resistive feedback, which needs to be 500-1KΩ and usually realized by polysilicon (high resistivity material), the T-Line, made of metal, has less resistance. To prove the effectiveness of noise reduction T-Line has over regular resistor, let's first analyze the model of T-Line we use. In the 65nm predictive model, there is no transmission line modeling. The T-Line model we used in our design is the default model in ADS library [reference here]. In that model, the transmission line is defined as shown in Fig 4.19.

Symbol

Illustration



Parameters

Name	Description	Units	Default
Z	Characteristic impedance	Ohm	50.0
L	Physical length	mil	1000.0
K	Effective dielectric constant	None	2.1
A	Attenuation	dB/meter	0.0001
F	Frequency for scaling attenuation	GHz	1
TanD	Dielectric loss tangent	None	0.0002
Mur	Relative permeability	None	1
TanM	Magnetic loss tangent	None	0
Sigma	Dielectric conductivity (leakage)	Siemens/m	0
Temp	Physical temperature	°C	None

Fig 4.19 T-Line model in ADS library

T-Line parameters above can be split into two categories: a). the design variables that can be easily implemented in schematic/layout design; b). the technology variables that are predetermined by the type of technology/PDK. The variables in category a includes the characteristic impedance Z (usually called Z_0, in other parts of

this thesis), and physical length L. The length and width of T-Line together will determine the characteristic impedance Z_0. The definition of characteristic impedance Z_0 is, however, unclear of whether it is lossy or lossless T-Line in ADS. The definition of lossy T-Line is:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

and lossless T-Line is as defined in Chapter 2.4:

$$Z \equiv \sqrt{L/C}$$

The technology variables define the four types of loss T-Line carries:

1) The loss due to metal conductivity;
2) The loss due to dielectric loss tangent;
3) The loss due to conductivity of dielectric;
4) The loss due to radiation.

The loss due to metal conductivity is considered to be the main source of T-Line. It is originated from DC sheet resistance and skin effect. DC sheet resistance is due to the conductivity of T-Line material the metal itself. The skin effect is the tendency of an AC current to become distributed within a conductor such that the current density is largest near the surface of the conductor and decreases with greater depths in the conductor. The skin effect causes effective resistance of the conductor to increases at

higher frequencies due to the reducing effective cross-section of conductor. The skin effect induced resistance can be modeled as:

$$R_{RFSH} = (\frac{\omega\mu_0\mu_R}{2\sigma})^{\frac{1}{2}} = (\frac{\pi f\mu_0\mu_R}{\sigma})^{\frac{1}{2}}$$

where we can see it is proportional to the square-root frequency. In combination, the loss of metal conductivity in modeled by parameter A (Attenuation) above. This loss is similar to the loss resistor creates, with same properties of thermal noise.

The dielectric tangent loss quantifies a dielectric material's inherent dissipation of electromagnetic energy. It can be parameterized in terms of either the loss angle ***δ*** or the corresponding loss tangent ***tan δ***, as shown in figure below:

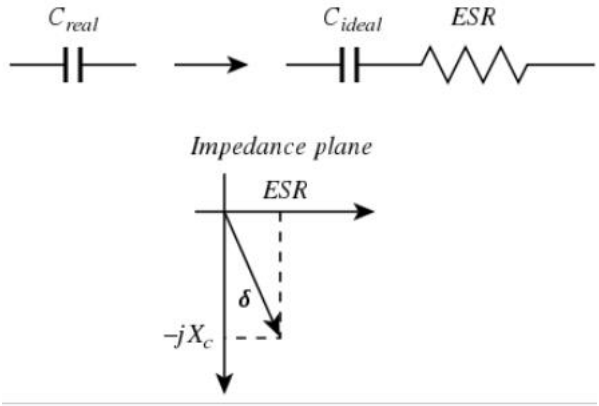


Fig 4.20 the modeling of dielectric loss tangent for a dielectric material

worth mentioning here is, the ESR, equivalent series resistance, here means it's not a real resistor in the theory. It is not really creating thermal noise. It is just a model to present how much energy is converted into heat.

The conductivity of dielectric material, or the leakage. This is often to be "impossible", as the default value to be set to zero. Therefore, although it is creating thermal noise in the circuit, we can safely ignore it.

The radiation, like the dielectric tangent loss, are electromagnetic energy losses as well.

As we discussed above, the reason we use transmission line is not to transform total energy from Y to X, it is for the purpose of transfer signal (or energy) from Y to X with some voltage ratio. That voltage ratio, always smaller than 1, itself indicates the energy loss in tolerable in our design. Therefore, the only loss really matters is the conductivity loss, and the effect is proportional only to the square-root of frequency.

In conclusion, the losses of T-Line create that are disruptive in LNA design is only the sheet resistance and skin depth losses, which are weak functions of frequency. The small noise resistance of transmission line means that its available power $P_{AY} = kT$ is not effectively coupled to the source or load. Therefore, it's safe to say T-Line will be much less noisy replacing feedback resistor.

Summary:

The biggest noise contributor of 60GHz CMOS LNA was shown to be the thermal noise of the amplification transistor, and the noise-canceling is effective in canceling thermal noise of transistor. However, the classic noise canceling theory, although proven can work in up to several gigahertz, is facing model and equation failure in traditional DC small signal analysis. To solve the high frequency limitation, especially in 60GHz, this chapter proposed two architectures, complex feedback path (feedback path with real and imaginary impedance) and transmission line feedback path. Then a transmission line voltage divider is proposed and analyzed, in order to build a noise-canceling LNA. The voltage dividing ratio is derived and simulated in ADS. Finally, the noise model and analysis of transmission line itself is reviewed. In the next chapter, 60GHz noise canceling LNA with complex feedback and transmission line feedback path will be built and tested.

Chapter 5 60GHz NC-LNA circuit design

In this chapter, we will design a Noise-Canceling LNA that works at 60GHz. The theory was based on reference [12] and to rephrase here, the addition of two Common-Source amplifier with one CS amplifier has a feedback path, as shown in Fig 5.1.

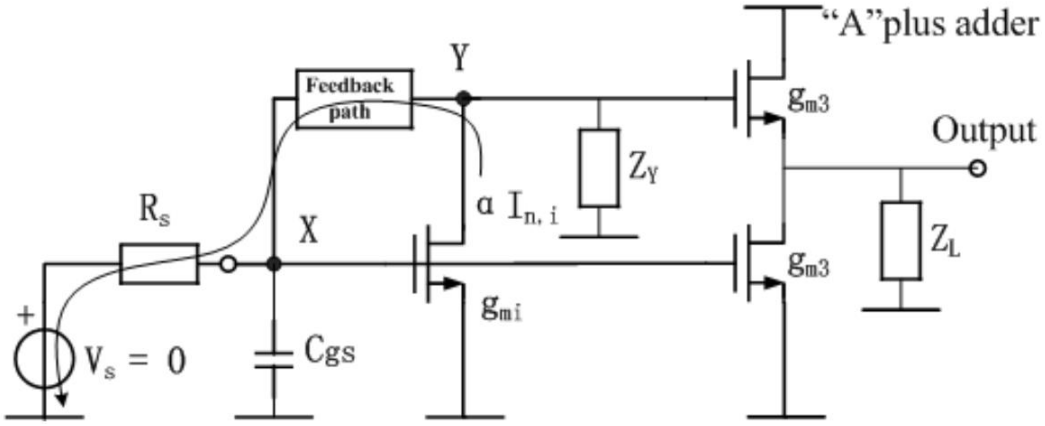


Fig 5.1 conceptual schematic of noise canceling LNA @ 60GHz

This chapter will start with common-source amplifier design and more specifically, the shunt feedback common-source amplifier design. Design starts with analysis of low-frequency models but then incorporates the difference of higher-frequency and lower-frequency modeling. A T-Line based shunt feedback common-source amplifier design is proposed in 60GHz frequency range. Next, a noise-canceling LNA with resistive feedback is presented, as a continuation / supplementation of classic noise-canceling theory. Then, the T-Line based NCLNA is

introduced and design steps are analyzed, and simulation results are presented. Finally, for better LNA linearity, derivative superposition [17] is incorporated in the design.

5.1 Shunt Feedback Common-Source Amplifier

The first step of designing a good NC-LNA is to design good Shunt-Series amplifier, at higher frequency. This involves more detailed considerations than at lower frequencies. When the operation frequency is approaching the device (65nm CMOS technology) frequency limits, the effect of ever-present parasitic capacitance and inductances can impose serious constraints on achievable performance. Therefore, the design gets much harder. Our goal is to get the best gain out of limited 65nm CMOS technology can provide, with good input/output matching. The noise, however, is less important in both amplifier designs because they will be canceled anyway.

The modeling of parasitic capacitance is very complicated, usually relying on not only designer's experiences but more importantly on the fabrication company's modeling expertise. Moreover, the modeling may vary a lot from technology to technology. Therefore, this section instead of trying to be accurate on every detail, we

will make reasonable approximation and focus on comparisons from lower frequency modeling to higher frequency modeling, ignoring (partially) the parasitics and focusing on active and passive devices themselves. A good way to validate our analysis is by analogy between the low frequency and high frequency models. Finally, all analysis will be validated by ADS simulation.

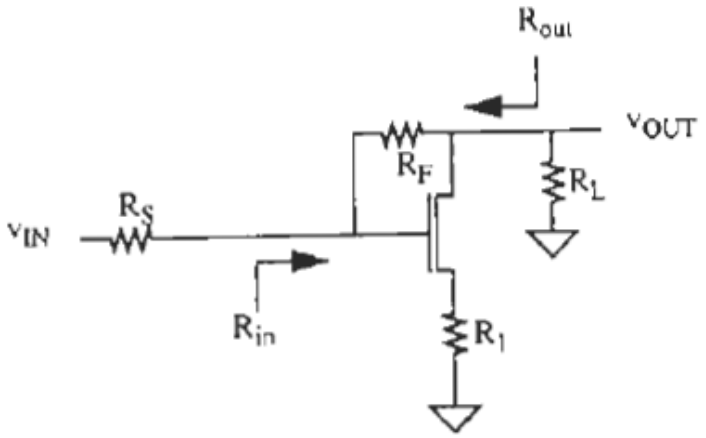


Fig 5.2 Classic source degeneration shunt-series amp schematic [5]

The basic amplifier we chose to use is the shunt-series feedback amplifier (as Thomas Lee called in his book) as shown in Fig 5.2. The shunt feedback is the use of drain-gate feedback resistor and the series feedback is the use of source degeneration (also a form of feedback) resistor.

The technique of source degeneration, inductive or resistive, is widely used in LNA design. For resistive source degeneration, used at low frequency (as shown in Fig 5.2) and inductive source degeneration, used at high frequency, Fig 5.3 is very

important to understand their functions and properties. As in Thomas Lee's book [5], in the shunt-series amplifier, resistive source degeneration is used to provide good linearity, making the effective gain:

$$G_m = \frac{g_m}{1 + g_m R_1}$$

As drawn in Fig 5.2. If we assume the source degeneration R_1 is large comparing with $1/g_m$, making the effective $g_m = {}^{1}/_{R_1}$. Then based on Miller Effect, the input impedance Rin:

$$R_{in} = \frac{R_F}{1 - A_V} \approx \frac{R_F}{1 + {}^{R_L}/_{R_1}}$$

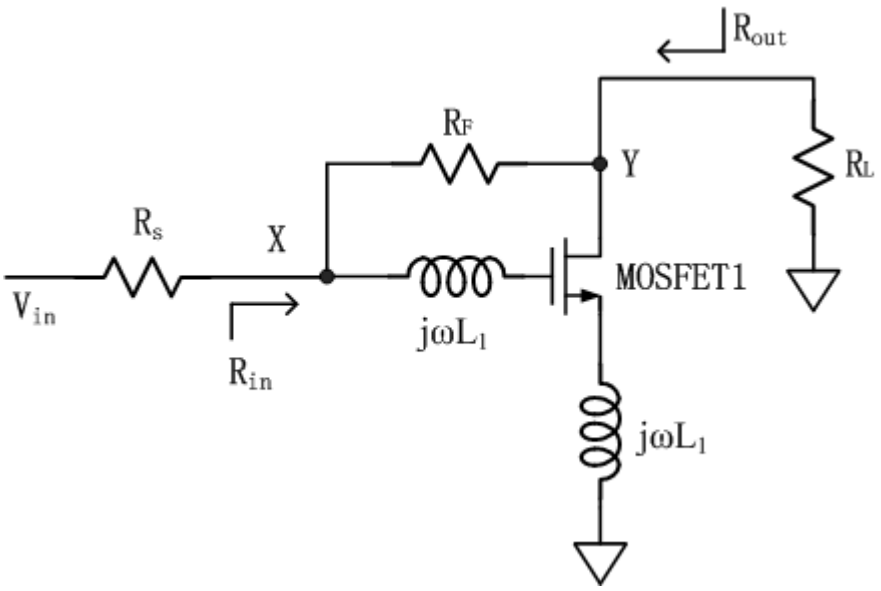


Fig 5.3 inductive source degeneration amplifier schematic at 60GHz

At 60GHz, we can redraw the shunt-series amplifier as shown in Fig 5.3:

a). the Miller Effect now must take gate-drain capacitance into account (rewrite $R_F = (R_F || \frac{1}{j\omega C_{gd}})$);

b). gate of transistor is no longer an open circuit, becoming (old R_{in} || (source matching L + C_{gs} + source degeneration L));

c). the gain is changed from R_L/R_1 (as discussed later);

d). the source degeneration resistor, R_1, becomes complex as $j\omega L_S$.

Therefore, we can rewrite the input impedance as:

$$R_{in} \approx \frac{R_F}{1 + R_L/R_1} \approx (\frac{R_F // \frac{1}{j\omega C_{gd}}}{1 + A_V}) \ // \ (j\omega L_1 + \frac{1}{j\omega C_{gs}} + j\omega L_s)$$

The equation above is not accurate, parasitics are not considered at all and other effects like substrate are all ignored. However, the equation above indicates that the methods to determine R_{in} remains the same and proper combinations of R_F, L_s and L_1 can be found to match a transistor (C_{gd}, C_{gs}) to a 50 ohm input.

Similarly, the output impedance is:

$$R_{out} = \frac{R_F + R_S}{1 + R_s/R_1} \approx \frac{R_F}{1 + R_s/R_1}$$

The input/output impedance are typically matched to 50ohms, making:

$$R_{out} \approx R_{in} \approx \frac{R_F}{1 + R_L/R_1} \approx \frac{R_F}{1 - A_V}$$

Also, in[5], the gain is given in the form of:

$$A_V = \frac{v_{out}}{v_{test}} = -\frac{R_L}{R_1} \cdot \left[\frac{1}{1 + {}^{1}/_{g_m R_1}}\right] \cdot \left[\frac{1}{1 + {}^{R_L}/_{R_F}}\right] \cdot \left[1 - \frac{1}{g_{m,eff} R_F}\right]$$

where the gain A_V is expressed in the form of ideal gain multiplied by several non-ideal factors.

1. The first term $-\frac{R_L}{R_1}$ is the ideal gain. At 60GHz, R_1 is not a resistor anymore, but instead an inductor $j\omega L_s$. Low frequency gain has a minus sign "-" indicating -180^o phase shift while in higher frequency the -180^o phase shift is still valid but the $\frac{R_L}{j\omega L_s}$ will introduce more phase shift.
2. The second term reflects the influence of finite transconductance. Due to the relative value of ${}^{1}/_{g_m} \ll R_1$ is not valid anymore, $\left[\frac{1}{1+{}^{1}/_{g_m R_1}}\right]$ is used to model the effect of finite transconductance on gain. At 60GHz, ${}^{1}/_{g_m} \ll j\omega L_S$ is not valid as well so the finite transconductance coefficient $\left[\frac{1}{1+{}^{1}/_{g_m j\omega L_S}}\right]$ should be considered.
3. The third term indicates how much the feedback resistor R_F is loading R_L. The feedback resistor creates a secondary current path (the transistor is basically a voltage controlled current source) ground. This reduces gain, with a coefficient

$\left[\frac{1}{1+{R_L}/{R_F}}\right]$. At 60GHz, the load resistance is replaced with load impedance Z_L. We can rewrite the coefficient as $\left[\frac{1}{1+{R_L}/{(R_F//\frac{1}{j\omega C_{gd}})}}\right]$.

4. The last term shows the effects the feedback resistor has on gain by creating a feedforward path directly from input to output. The input signal sees a direct signal path from Gate of transistor to Drain through the R_F, reducing the gain. The effect is represented by coefficient $\left[1-\frac{1}{g_{m,eff}R_F}\right]$ where $g_{m,eff}$ is the effective transconductance. At 60GHz, although the value of $g_{m,eff}$ might be different, the equation remains valid.

Now we can rewrite the gain as:

$$A_V=\frac{v_{out}}{v_{test}}=-\frac{R_L}{j\omega L_s}\cdot\left[\frac{1}{1+{1}/{g_m j\omega L_S}}\right]\cdot\left[\frac{1}{1+{R_L}/{(R_F//\frac{1}{j\omega C_{gd}})}}\right]\cdot\left[1-\frac{1}{g_{m,eff}(R_F//\frac{1}{j\omega C_{gd}})}\right]$$

The analysis above was based on the DC small signal analysis of the series-shunt amplifier and modified for high frequencies. The analysis ignores all parasitics which

are critical to mmWave circuit design. However, it serves as guide for how to design a series-shunt amplifier at 60GHz, and as a reference of how to set parameters in simulation and gives guidance on how to change parameters to achieve the desired performance.

5.2 T-Line based Feedback LNA at 60GHz

The shunt-series amplifier is a core part of noise-canceling LNA, valuable for providing gain as well as a path that transfers the thermal noise, generated in the common source transistor, from Drain back to Gate with a ratio of $\frac{R_S}{R_S+R_F}$ (<1). In this section, now that we know that the T-Line can provide voltage transformation that can do the job of $\frac{R_S}{R_S+R_F}$ (discussed in chapter 4), we will derive and validate the theory of transmission line based LNA, including gain/input/output impedance.

To understand theory better, we use components as simple as possible, as shown below in Fig 5.4, the transistor is replaced with Voltage Controlled Current Source (VCCS) with transconductance g_m; transmission line model is picked from ADS default library with two variables, characteristic impedance Z0 and length d. Also, the finite channel modulation effect and source degeneration inductor is removed to simplify the mathematical derivation.

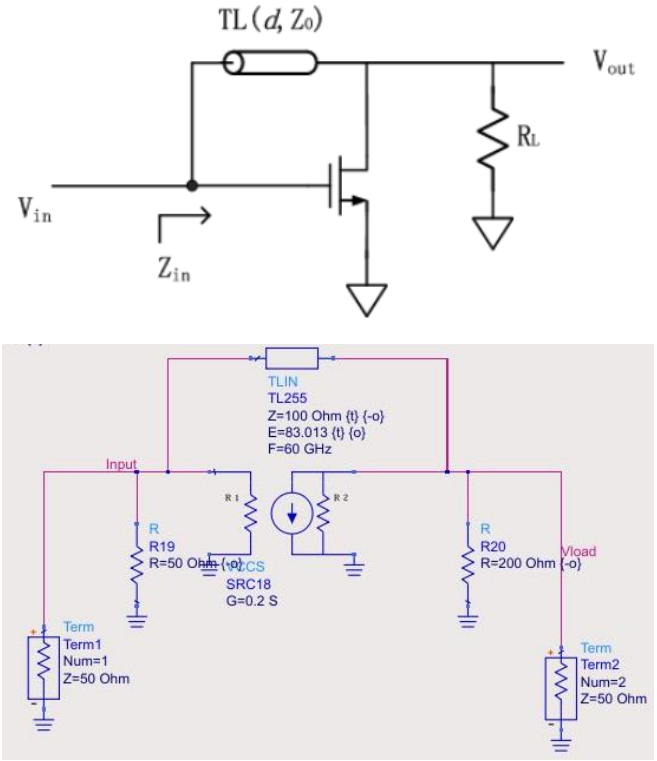


Fig 5.4 Amplifier with T-Line feedback 1). Conceptual topology; b). ADS schematic

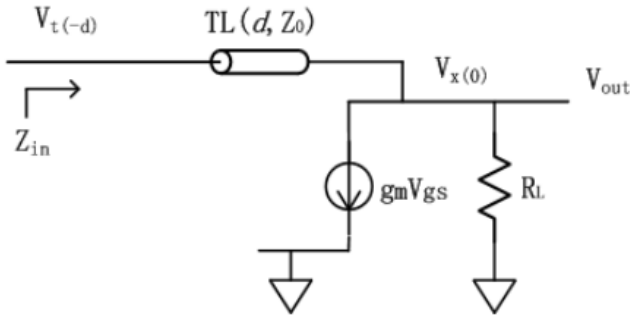


Fig 5.5 Input impedance calculation equivalent circuit

The input impedance calculation can be derived as shown in Fig 5.5, :

1. The input impedance looking into transmission line is given as:

$$Z_{in} = \frac{V_{t(-d)}}{I_{t(-d)}} = \frac{V_0^+(e^{j\beta d} + \Gamma e^{-j\beta d})}{V_0^+(e^{j\beta d} - \Gamma e^{-j\beta d})} Z_0 = \frac{1 + \Gamma e^{-2j\beta d}}{1 - \Gamma e^{-2j\beta d}} Z_0$$

where the $V_{t(-d)}$ and $I_{t(-d)}$ is the voltage and current at the left side of transmission line respectively. Reflection coefficient Γ is given as

$$\Gamma = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Worth mentioning here the Z_L is not the load impedance (resistance) R_L, but R_L in parallel with the VCCS ($g_m V_{gs}$), as shown:

$$Z_L = \frac{V_{X(0)}}{\frac{V_{X(0)}}{R_L} + g_m V_{t(-d)}}$$

where $V_{X(0)}$ is the voltage at the right-side of transmission line. Since $V_{X(0)}$ and $V_{t(-d)}$ are related as:

$$V_{x(0)} = V_0^+\left(e^{j\beta d} + \Gamma e^{-j\beta d}\right) = V_0^+(1 + \Gamma)$$

We have:

$$Z_L = \frac{V_{X(0)}}{\frac{V_{X(0)}}{R_L} + g_m V_{t(-d)}} = \frac{(1 + \Gamma)}{\frac{(1 + \Gamma)}{R_L} + g_m(e^{j\beta d} + \Gamma e^{-j\beta d})}$$

and Reflection coefficient Γ could be rewrite as:

$$Z_L = \frac{(1 + \Gamma)}{(1 - \Gamma)} Z_0$$

$$\Gamma = \frac{\frac{1}{Z_0} - \frac{1}{R_L} - g_m e^{j\beta d}}{\frac{1}{Z_0} + \frac{1}{R_L} + g_m e^{-j\beta d}}$$

In summary, the input impedance of transmission line based amplifier, as shown in Fig 5.5, is

$$Z_{in} = \frac{1 + \Gamma e^{-2j\beta d}}{1 - \Gamma e^{-2j\beta d}} Z_0$$

where

$$\Gamma = \frac{\frac{1}{Z_0} - \frac{1}{R_L} - g_m e^{j\beta d}}{\frac{1}{Z_0} + \frac{1}{R_L} + g_m e^{-j\beta d}}$$

2. The gain of resistive shunt-series amplifier:

   Before we derive gain equation, let's first put the simplified gain equation for resistive feedback amplifier again, as:

$$gain = A_v = \frac{V_{out}}{V_{in}} = -g_m \frac{R_F R_L}{R_F + R_L} + \frac{R_L}{R_F + R_L}$$

   Similarly, transmission line based feedback amplifier gain can be expressed as:

$$A_V = A_{Vgm} + A_{FF}$$

   where A_{Vgm} is the gain from VCCS and A_{FF} is the feedforward gain.

   Next, is to figure out A_{Vgm} and A_{FF} separately.

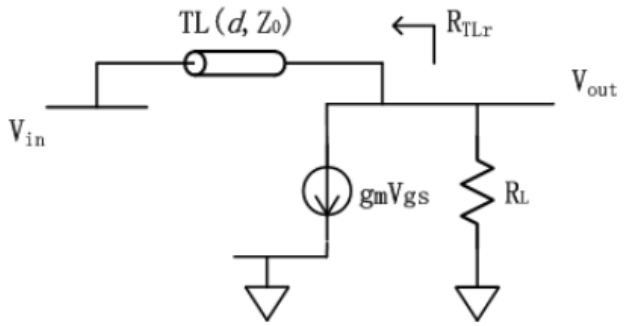


Fig 5.6 Input impedance calculation equivalent circuit

a). A_{Vgm} is generated by the VCCS sees the impedance of load impedance R_L in parallel with impedance from the transmission line back to source:

$$A_{Vgm} = -g_m(R_{TLr}//R_L)$$

and the impedance looking from the right side of transmission line backward to source, expressed by R_{TLr}, (T-Line right), based on Pozar's theory is given as:

$$R_{TLr} = Z_0 \frac{Z_S + jZ_0 \tan \beta d}{Z_0 + jZ_S \tan \beta d}$$

where Z_S is source impedance.

b). Feedforward gain A_{FF} is the voltage ratio from the left side of transmission line to the right side of transmission line. Detailed derivation is explained in Chapter 4.2, and the conclusion here is:

$$A_{FF} = {V_{x(0)}}\Big/{V_{t(-d)}} = \frac{V_0^+[(1+\Gamma_L)]}{V_0^+[\cos(\beta d)\,(1+\Gamma_L) + jsin(\beta d)(1-\Gamma_L)]}$$

where Γ_L, the reflection coefficient looking from left side of transmission line to the right side (load side) of transmission line is given:

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$$

clean up the equation above we have:

$$A_{FF} = {V_{x(0)}}/{V_{t(-d)}} = \frac{Z_L}{Z_L \cos(\beta d) + jZ_0 sin(\beta d)}$$

Combining equations above we have the overall gain as

$$A_v = -g_m(R_{TLr} // R_L) + \frac{Z_L}{Z_L \cos(\beta d) + jZ_0 sin(\beta d)}$$

3. Output impedance of transmission line feedback

The output impedance equivalent circuit is draw as below in Fig 5.6. The output impedance is calculated when a test voltage is applied to Vout, and test current is given as: (load impedance R_L is ignore for now, as it is just another impedance in parallel with Z_{out})

$$I_{test} = g_m V'_{gs} + I_{tline}$$

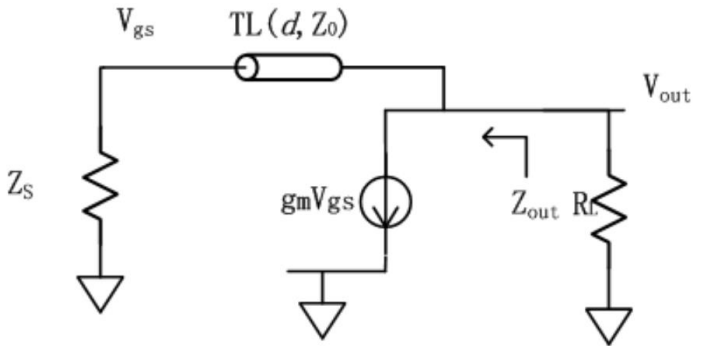


Fig 5.6 Output Impedance Equivalent Circuit

The current flow through VCCS is controlled by the voltage at the left side of transmission line (aka the gate of transistor), and V'_{gs} is given as:

$$V'_{gs} = V'_{x(0)} = V_0^+(1+\Gamma_S) = \frac{V_{test}(1+\Gamma_S)}{(e^{j\beta d} + \Gamma e^{-j\beta d})}$$

where source reflection coefficient Γ_S, is given as:

$$\Gamma_S = \frac{Z_s - Z_0}{Z_s + Z_0}$$

The current flow through transmission line is given by Pozar's theory:

$$I_{tline} = \frac{V_0^+}{Z_0}(e^{j\beta d} + \Gamma_S e^{-j\beta d})$$

Therefore, the output impedance is given by:

$$Z_{out} = \frac{V_{test}}{I_{test}} = \frac{1}{\frac{g_m \times (1+\Gamma_S)}{e^{j\beta d} + \Gamma_S e^{-j\beta d}} + \frac{e^{j\beta d} - \Gamma_S e^{-j\beta d}}{(e^{j\beta d} + \Gamma_S e^{-j\beta d})Z_0}}$$

In the input/output impedance matching analysis above, we treat T-Line, terminated into any arbitrary load, as an ordinary resistor that can be placed in parallel with any lumped circuit components.

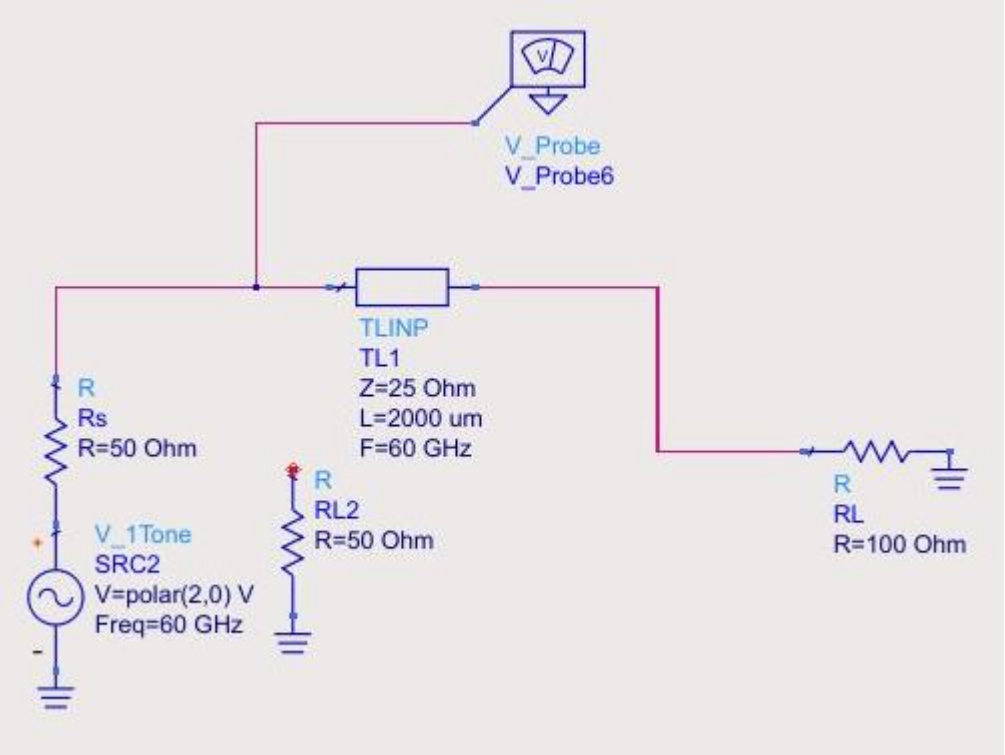


Fig 5.7 Test bench of T-Line in parallel with resistor

To verify a lossy transmission line was placed before load impedance $R_L = 100\Omega$. The source is an ideal voltage source generating 2V peak-to-peak voltage and a $R_s = 50\Omega$ was place in series with it to act as source resistance. Carefully set transmission line to find a spot that voltage looking into T-Line is 1V, which means looking into the T-Line, $Z_{in}(d) = 50\Omega$, as shown in Fig 5.6 left. When $R_{L2} = 50\Omega$ was connected into the circuit, the voltage measured at V_probe is 0.698, which means the impedance (magnitude) looking into T-Line the system is now 25Ω, which = $Z_{in}(d)//R_{L2}$. Furthermore, the fact of peak voltages for both circuits are at the same time means there is no phase shift in the parallel circuit.

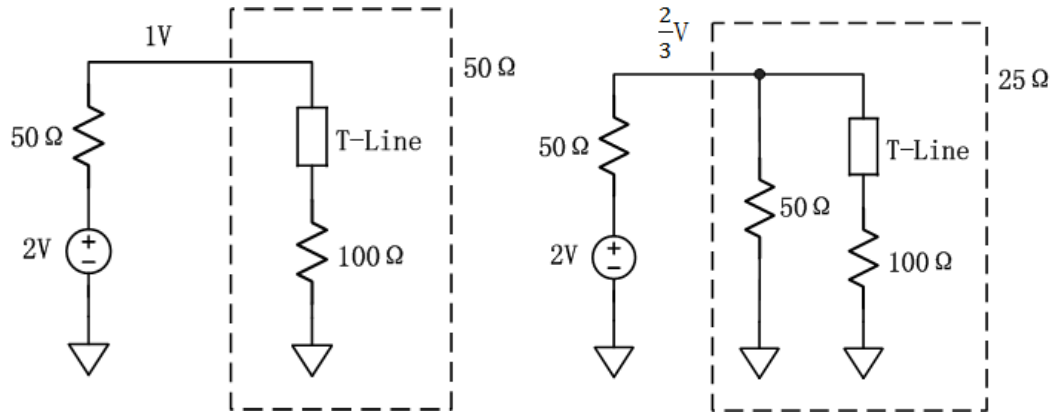


Fig 5.5 left: equivalent circuit without R_L2; right: equivalent circuit with R_L2

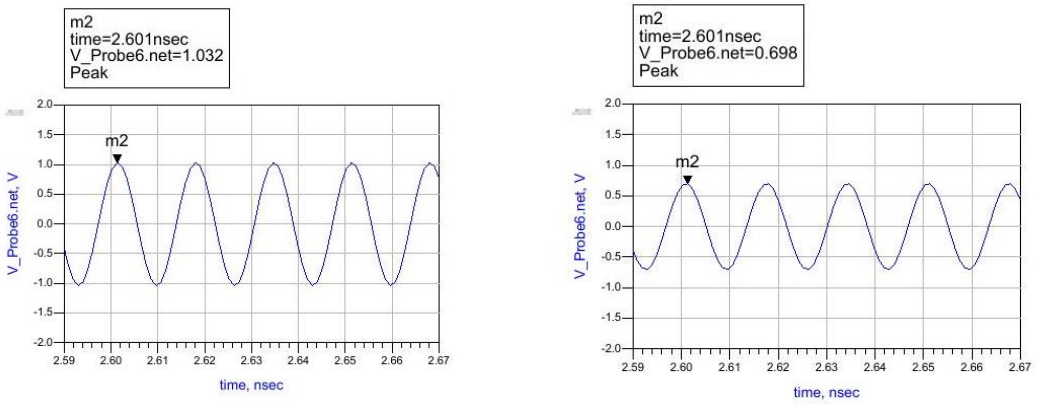


Fig 5.6 left: transient voltage measured at V_probe without R_L2; right: transient voltage measured at V_probe with R_L2

The conclusion is a transmission line, terminated in an arbitrary load impedance, will transform load impedance Z_{load} into the impedance looking into the transmission $Z_{in}(d)$.When put them in parallel with other resistor or impedance Z_R, the new impedance looking into the whole system is $Z_{in}(d)//Z_R$. This is the basis of T-Line based shunt-series amplifier analysis above. For future reference, “T-Line parallel impedance” will describe this feature.

The derivation of gain / input impedance / output impedance is calculated in Matlab (script attached in appendix) and verified versus ADS simulation results. To illustrate the gain, impedance and noise performance of a transmission line based feedback amplifier, we use the simple circuits as shown in Fig 5.4 b).

Voltage Controlled Current Source (VCCS) act as transistor with transconductance =0.2. For resistive case, the feedback resistor is set to be 200Ω and for transmission line case the feedback transmission line is set to have characteristic impedance =100Ω and electrical wavelength = 83degree. A 50Ω resistor is added as input noise source and a 200Ω resistor is added as output noise source.

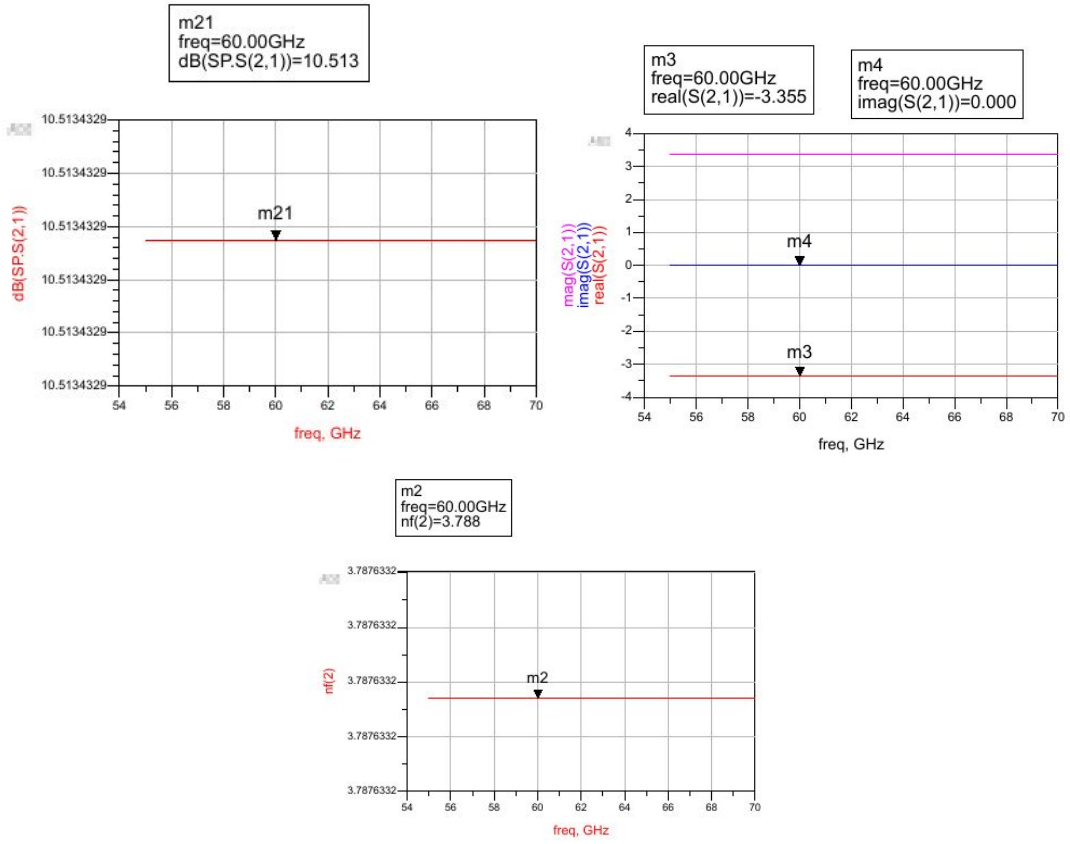


Fig 5.8. Resistive feedback, a) gain in dB; b) gain in Mag and Real/Img part; c) NF

The resistive feedback amplifier gain and noise figure from 55-70GHz are roughly |S21|=10.5 dB and the noise Figure (NF) is 3.788. . Replacing the feedback resistor with transmission line and adjusting it for for the same gain at 60GHz, we have following results shown in Fig 5.9:

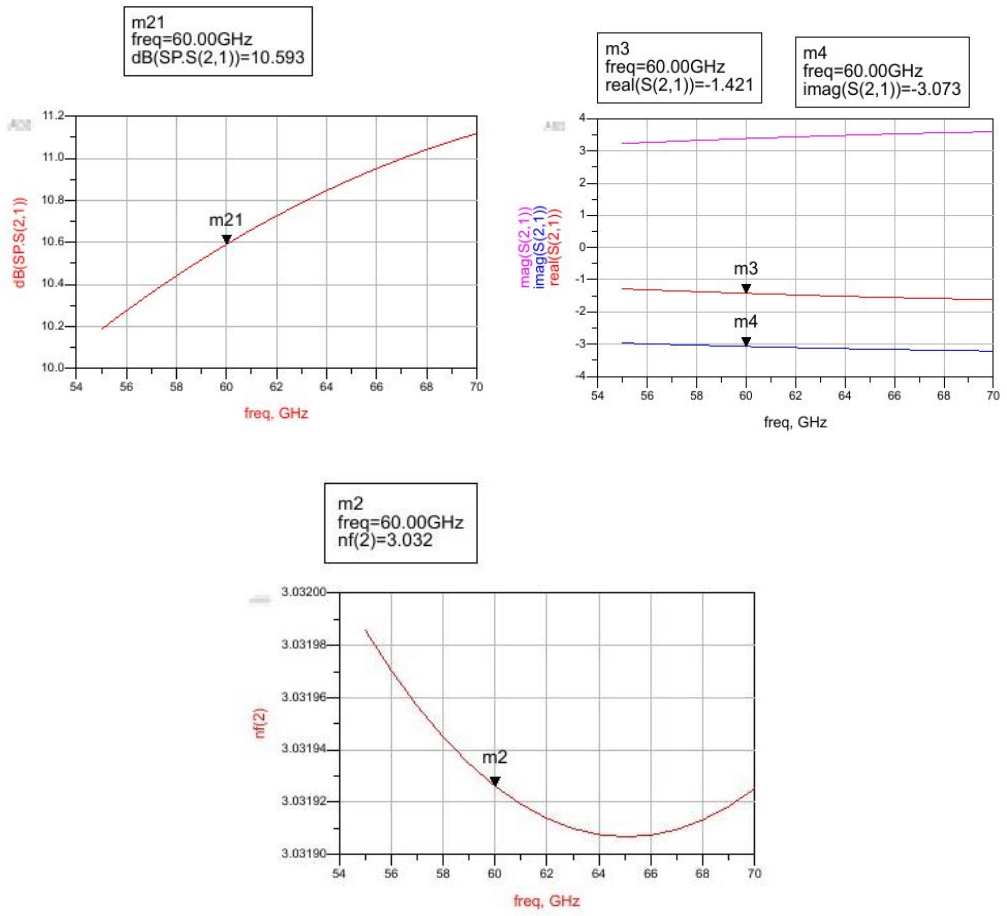


Fig 5.9. For transmission line feedback, a) gain in dB; b) gain in Mag and Real/Img part; c) NF

Taking all the variables back to the equations above we can have all the matching results as ploted in Fig 5.8 and Fig 5.9.

5.3 Transmission Line based Common Source LNA in 60GHz

Based on the conceptual model and derivation proposed in Chapter 5.2, we proceed to a real circuit design with transmission line feedback.

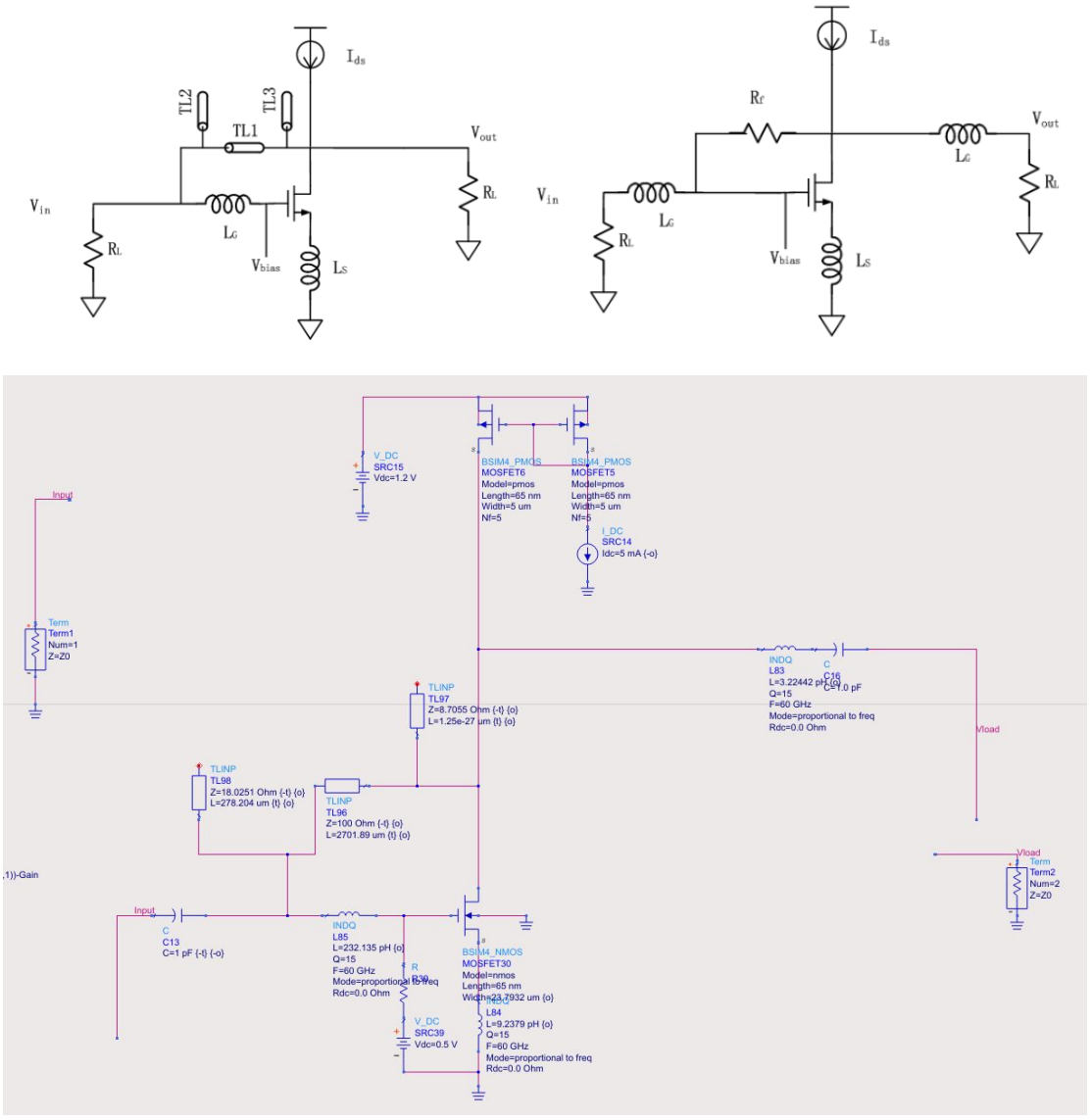
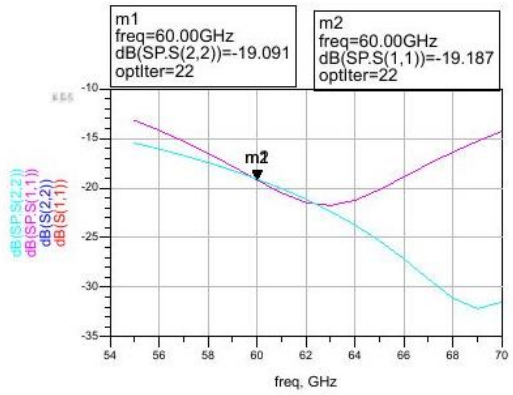


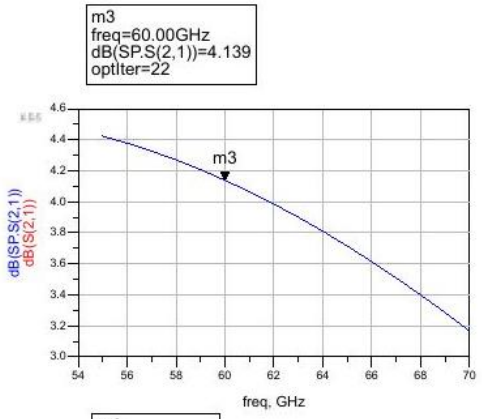
Fig 5.10 a). conceptual design of transmission line / resistor based feedback common source amplifier at 60GHz, and b). schematic in ADS

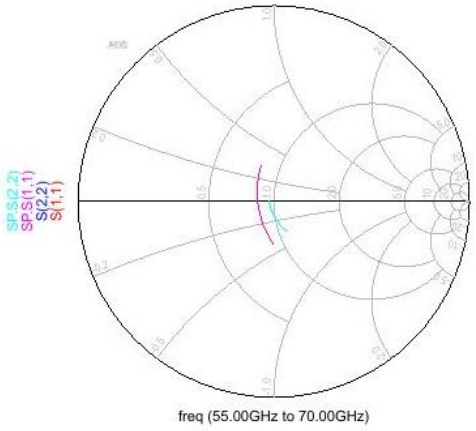
Fig 5.10 shows both the conceptual design and schematic captured in ADS.

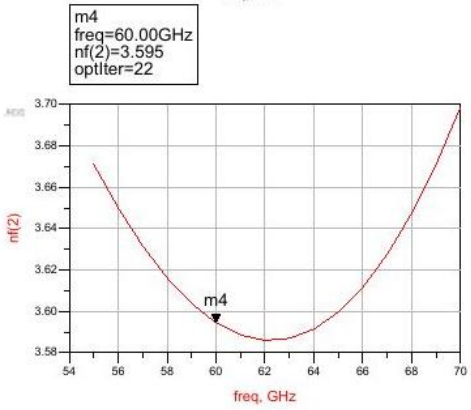
Experiment in this section is designed to compare the NF improvement of LNA of the

T-Line implementation relative to resistive implementations at same gain. To make a fair comparison, both transistors (in resistive feedback and in t-line feedback) are set with same length / width and same DC biasing condition. Drain current in both transistors are the same as they are provided by the same current mirror. The amplifier topology is the same as they both are common source amplifier with inductive source degeneration. Also, since NF is related to gain, and higher gain in general provides better NF, both amplifiers are designed for the same gain.


m1
freq=60.00GHz
dB(SP.S(2,2))=-19.091
optIter=22
m2
freq=60.00GHz
dB(SP.S(1,1))=-19.187
optIter=22
m2
dB(SP.S(2,2))
dB(SP.S(1,1))
dB(S(2,2))
dB(S(1,1))
freq, GHz


m3
freq=60.00GHz
dB(SP.S(2,1))=4.139
optIter=22
m3
dB(SP.S(2,1))
dB(S(2,1))
freq, GHz


SP.S(2,2)
SP.S(1,1)
S(2,2)
S(1,1)
freq (55.00GHz to 70.00GHz)


m4
freq=60.00GHz
nf(2)=3.595
optIter=22
m4
nf(2)
freq, GHz

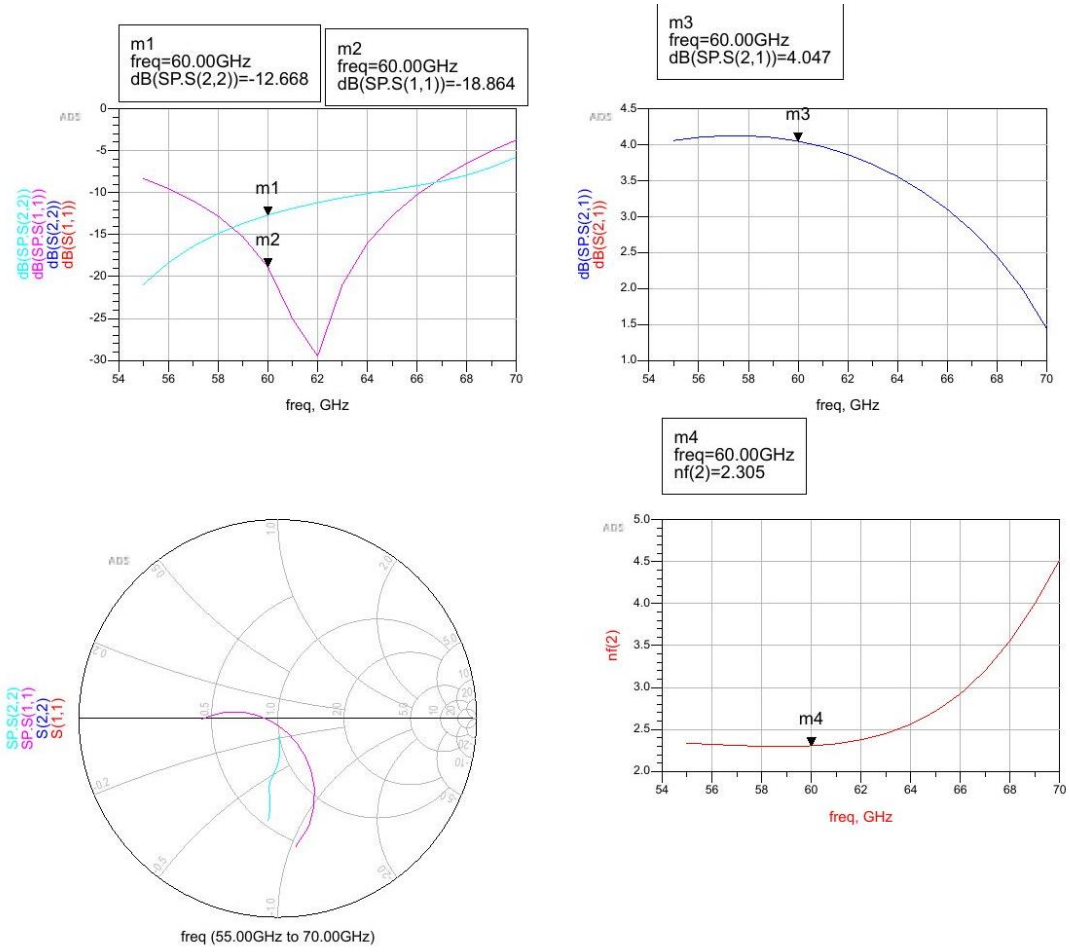


Fig 5.11 simulation results comparison of a) resistive; b) t-line based feedback LNA

Simulation results are summarized as in table below:

Amp Type	S21 dB	NF dB	S11 dB	S22 dB
Resistive	4.139	3.595	-19.091	-19.091
T-Line	4.047	2.305	-18.864	-12.668

At the same gain, t-line based feedback amplifier has less noise and lower NF than its resistive counterpart, since it removes the noise source in feedback path.

With a single stage LNA designed above, we proceed to a complete 3-stage LNA design, to facilitate comparison with 60GHz amplifiers reported in literature and to compare with our own noise canceling LNA. Gain / transistor size constraints are removed, and biasing conditions are optimized for better performance. A 3-stage topology is adopted to achieve a roughly 20dB gain. Additional inter-stage impedance matching is used and results are shown below in Fig 5.12.

As simulation results show, a 20.8dB max gain is achieved at 60GHz, minimum achievable NF is 3.08dB, input/output are reasonably well matched and both source and load stability circle is out of Smith Chart unity circle, meaning it is unconditionally stable.

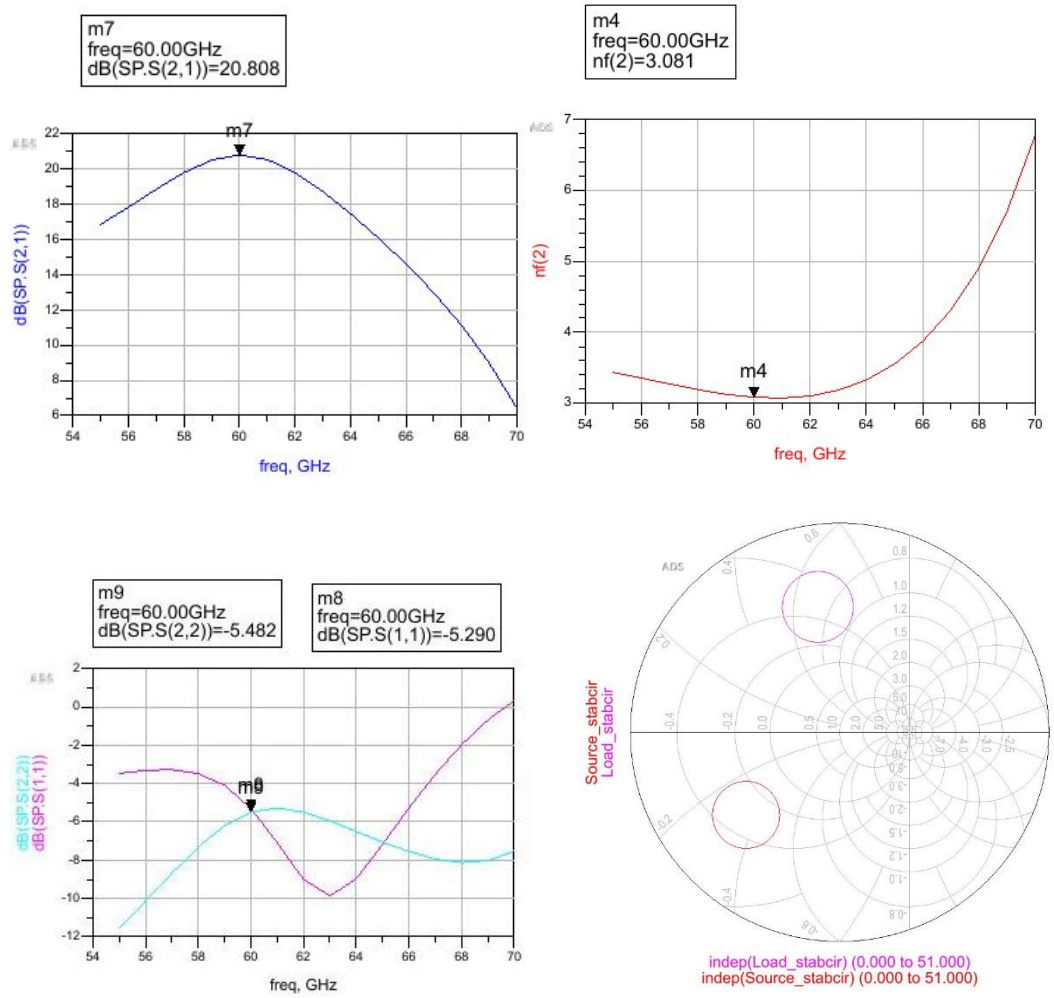


Fig 5.12 Optimized 3-stage t-line feedback LNA simulation results, a) gain; b) NF; c) S11&S22; d) stability circle

5.4 NC-LNA in 60GHz

Now that the common source amplifier and shunt-series amplifier design are reviewed and analyzed, the next step is to put the two amplifiers together in a Noise-

Canceling topology. The NC-LNA design is intended to provide ultra-low NF for 60GHz communications. (Different parts of the world have different unlicensed bands for 60GHz communication usage, but in general the frequency of operation is all within 57-66GHz range.) The following targets are required to make a good LNA within 57-66GHz:

1) signal bandwidth is at least 2.16GHz for one channel;

2) voltage gain $S21 \geq 14dB$, that is ${V_{out}}/{V_{in}} \geq 5$;

3) input/output impedance matched to 50Ω;

4) NF as low as possible. ($NF < 3dB$)

In the following design procedure, we will start with single stage NC-LNA design, and then work towards three-stage cascade NC-LNA. From system design point of view, first stages have more significant impact on system NF while linearity is a priority in latter stages. Therefore, when designing the first stage LNA, we always want to minimized noise figure. When designing latter stages, we can trade noise performance for gain and linearity.

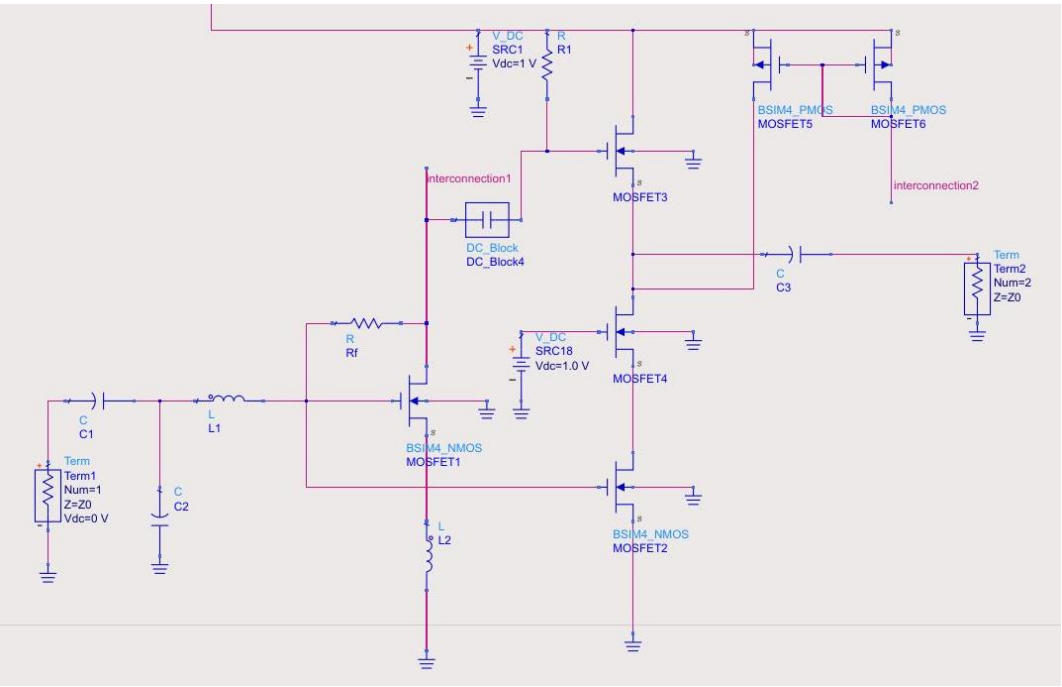


Fig 5.10 schematic of the 60GHz noise canceling CMOS LNA

Fig. 5.10 shows the 60GHz noise canceling CMOS LNA schematic. Refer to the concept circuit (Fig 5.1): transistor MOSFET1 is a common source amplifier; transistor MOSFET2, together with MOSFET4 forms a cascode amplifier. This is the auxiliary amplification path that proves gain $A_{v,c}$; transistor MOSFET3 is a source follower and voltage combiner that passes the amplified signal from MOSFET1 and combines it with the amplified signal from MOSFET2. Resistor R_f is the feedback resistor that provides a path for noise current back to the source. Inductor L_1, capacitor C_2 and source degeneration inductor L_2 are for input impedance matching purpose. In the schematic, the wires named “interconnection 1” and “interconnection

2” are connected to current mirrors, providing realistic biasing current for transistor MOSFET1 and MOSFET2 respectively. (current mirror not shown in schematic)

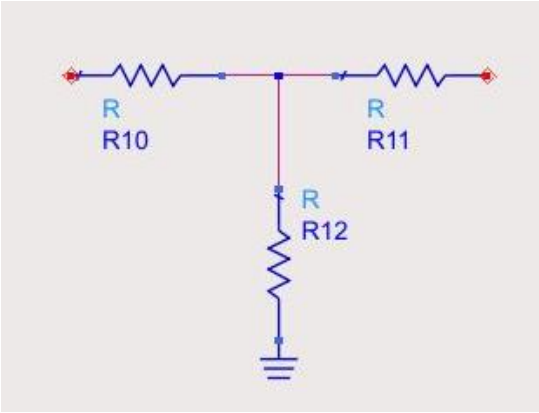


Fig 5.7 A better feedback network with less amount of total resistance[4]

In the course of design, we noticed that the resistor R_f became very large. A large resistor value is impractical, not only because it may consume a lot of area, but it also introduces large parasitic capacitance that is unwanted and unpredictable. Therefore, the feedback R_f is replaced with a resistor network configuration as Fig 5.9. This configuration can provide an effective resistance larger than three individual resistance combined.

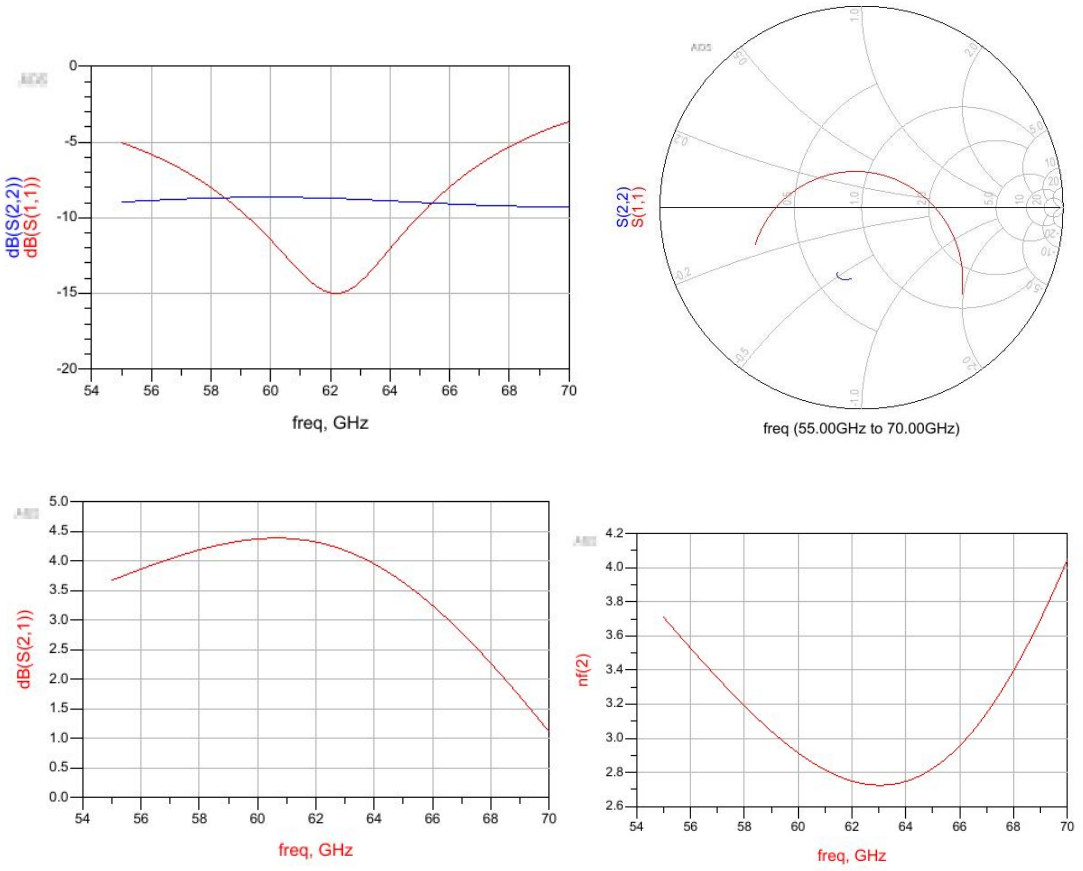


Fig 5.8 a) input/output impedance matching S11 and S22, b) S11 and S22 in smith chart, c) power gain S21, d) NF.

Fig. 5.10 shows the performance S11/S22/S21/NF of the LNA designed above. This LNA has 4dB of gain over a 7GHz bandwidth, a peak gain of 4.4dB at 60GHz with input/output impedance that are reasonably well matched. The NF is as low as 2.8dB, and below 3.4dB across all required frequency bands.

Stability is a necessary condition for an LNA. In theory, oscillation will occur when either input or output impedance has a negative real part. This would then imply

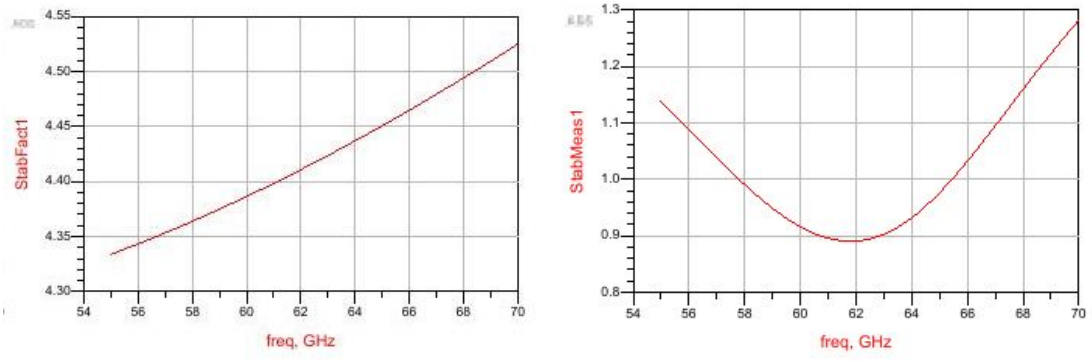
that $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$. In ADS software, the reflection coefficient $|\Gamma_{in}|$ and $|\Gamma_{out}|$ is not easy to plot. Instead, ADS use a simpler $K - \Delta$ test, where it can be shown that a device will be unconditionally stable if it satisfies Rollet's condition, defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

along with the auxiliary condition that:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

are simultaneously satisfied. These two conditions are necessary and sufficient for unconditional stability and are easy to plot in ADS. The necessary and sufficient conditions for unconditional stability are the stability factor is greater than unity and the stability measure is positive. Stability factor and stability measure are imbedded in function "StabFact" and "StabMeas" respectively. The results are plotted in Fig 5.11. These plots show the LNA is unconditionally stable.



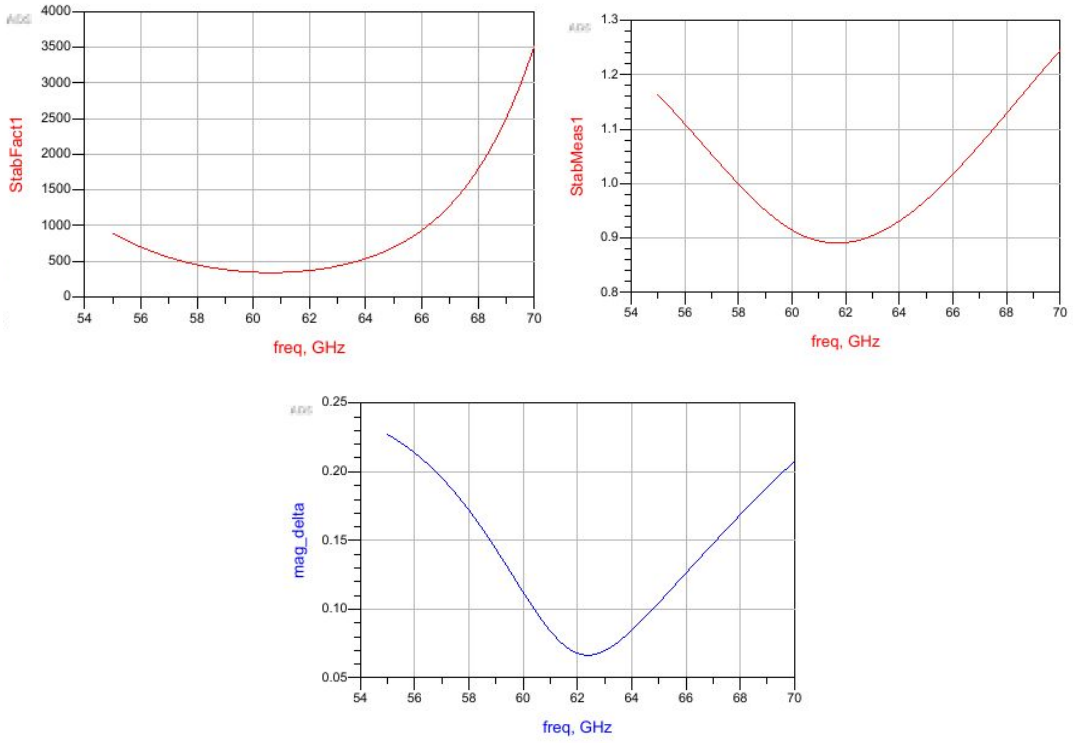


Fig 5.9 LNA simulation results: a) stability factor K, b) stability measure, c) delta|Δ|

The linearity is characterized by the 1dB compression point. As the input power increases, the output power (blue curve) cannot increase linearly along with input power. When the gain (red curve) drops by 1dB, the frequency corresponding to it is called the 1-dB compression point. In our single stage LNA design, the 1-dB compression point occurs when input is -14dBm.

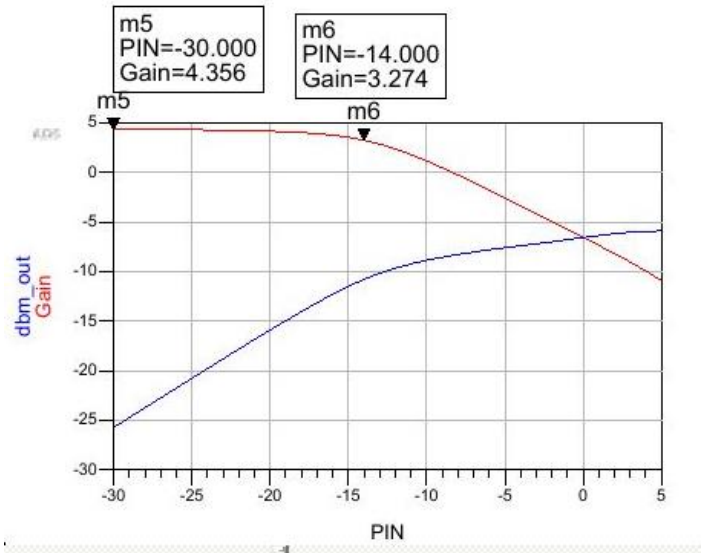


Fig 5.10 1dB compression point of 60GHz NCLNA

For a 3-stage cascade LNA system, the design principles are summarized below:

1). The former stages have more significant impact on system noise figure;

2). The latter stages have more significant impact on system linearity;

3). Mismatched peak gain for narrow-band circuits can provide an overall flat gain (wide-band applications), at the expense of lower gain.

With the above guidelines, a cascade Noise-Canceling LNA is designed, and results are shown below in Fig 5.13:

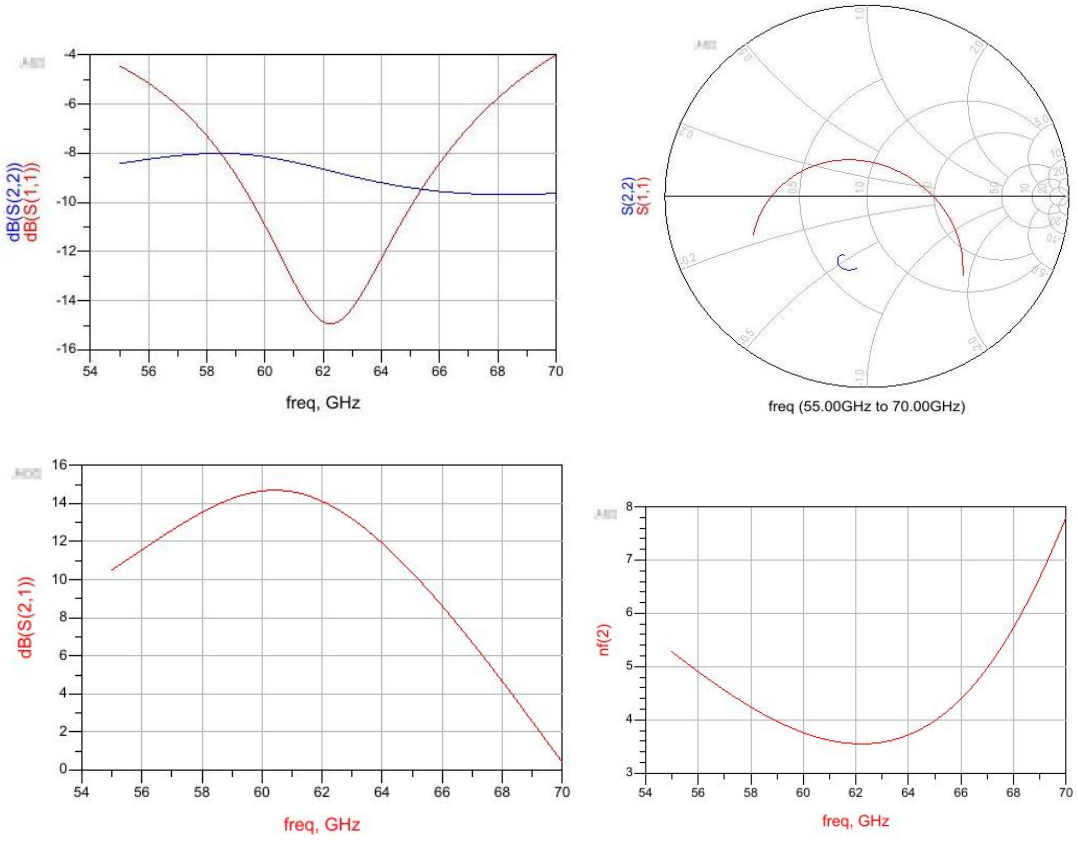


Fig 5.11 a) input/output impedance matching S11 and S22, b) S11 and S22 in smith chart, c) power gain S21, d) NF.

Fig. 5.13 shows the S-parameters simulation results of 3-stages NCLNA. This LNA have 14.7dB peak gain at 60GHz, and -1dB bandwidth wider than 3GHz. The minimum NF recorded is 3.4dB, and below 4dB over 6GHz frequency range.

Also, the linearity and stability tests were done in ADS. From results in Fig 5.14 and Fig 5.15, the amplifier is unconditionally stable with a 1dB compression input referred power level = -25dBm.

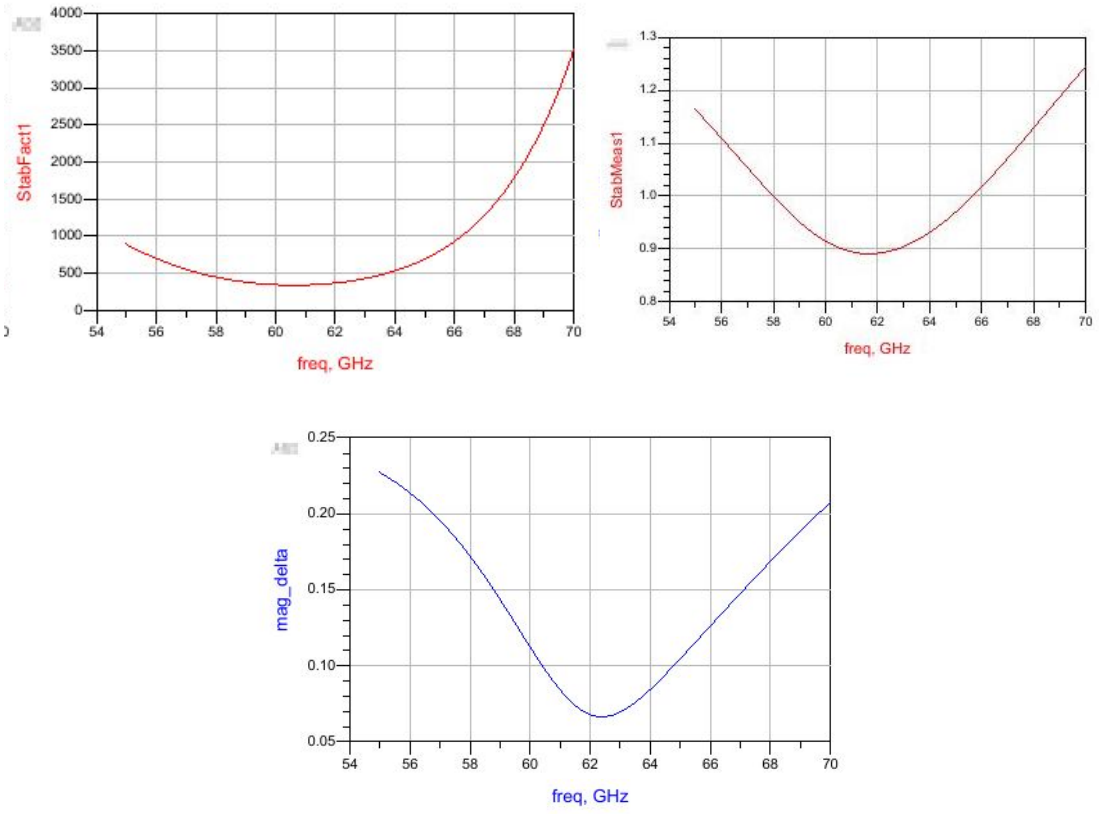


Fig 5.12 3-stages LNA simulation results: a) stability factor K, b) stability measure, c) delta|Δ|

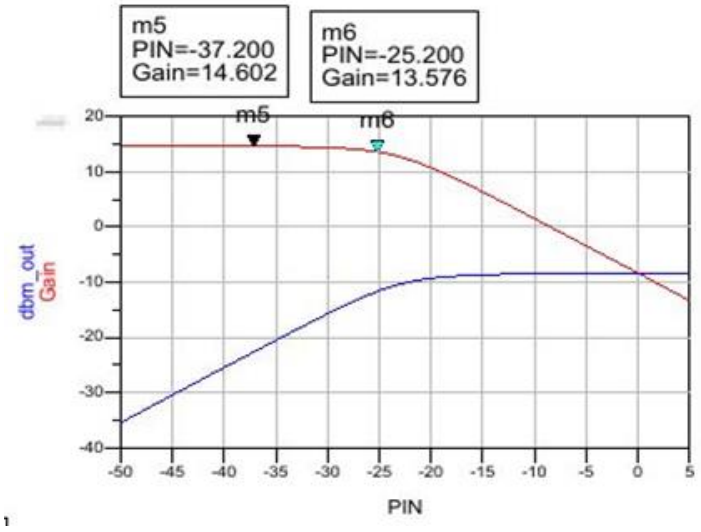
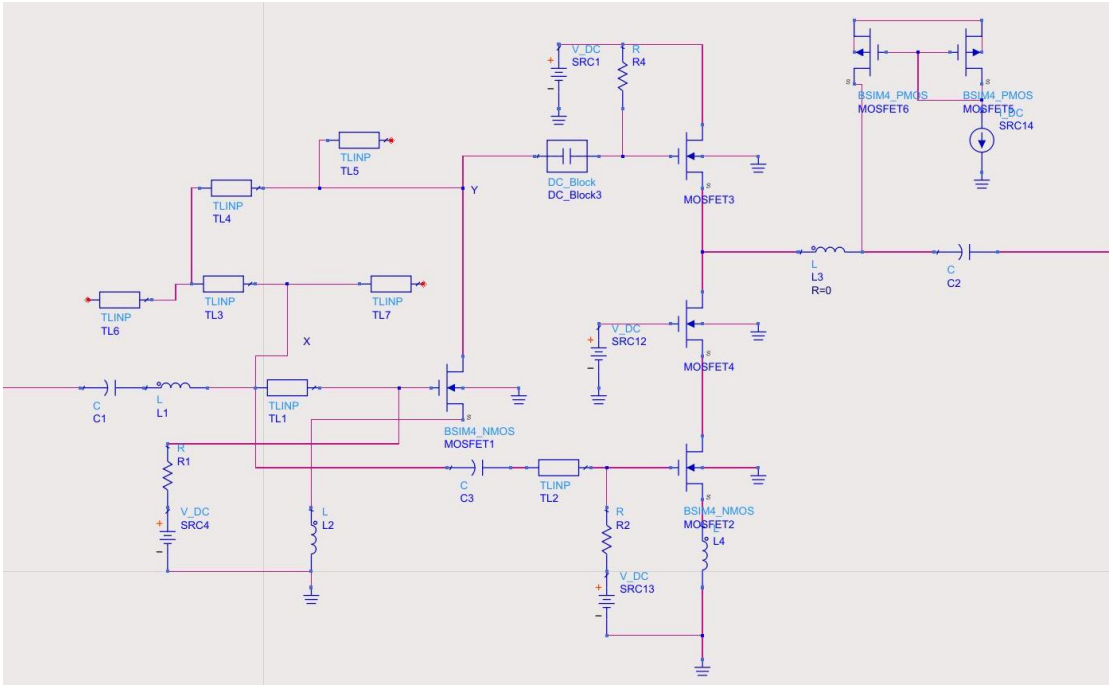


Fig 5.13 1dB compression point of 60GHz 3-stages NCLNA

5.5 Improved NC LNA with T-Line Feedback

As discussed in previous chapter, the transmission line can be a useful tool in providing impedance transformation and feedback voltage dividing. In the noise canceling LNA with transmission line design, as shown in Fig. 5.16 below:



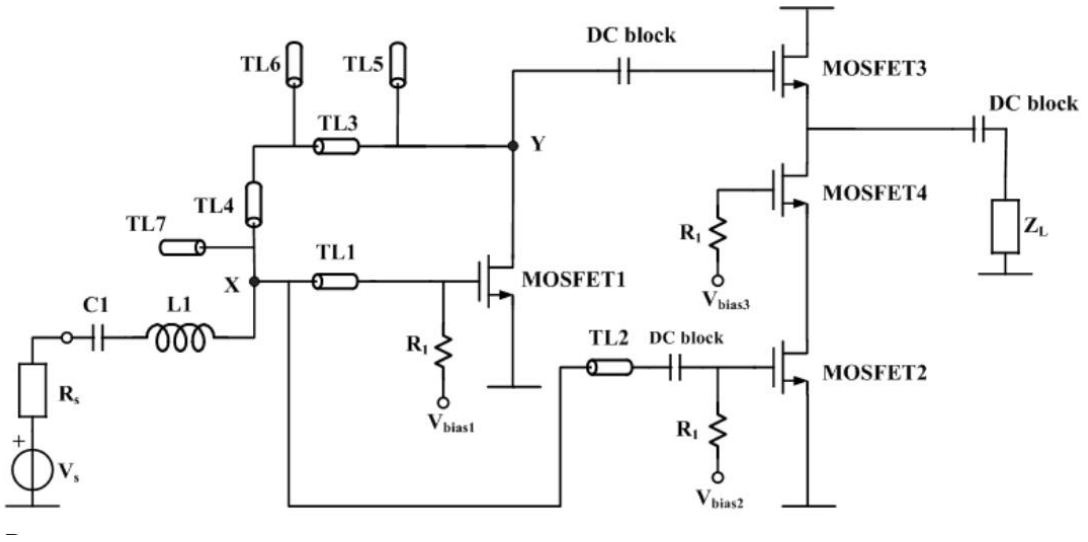


Fig 5.14 60GHz NC-LNA with T-Line feedback A). the schematic view; B). the conceptual view

For the transmission line TL1 and TL2 are connected to transistor MOSFET1 and MOSFET2 to provide n impedance match. T-Line TL3 and TL4 creates a feedback path for both high frequency signals and noise. At low frequencies, the T-Line behaves as short. (can be shown by the equation below. When frequency is very low, wavelength is very high and $tan\beta d \approx 0$, impedance looking into the T-Line $Z_{IN} \approx Z_0 \frac{Z_L}{Z_0} = Z_L$).

$$Z_{in}(d) = Z_0 \frac{(Z_L + Z_0)e^{j\beta d} + (Z_L - Z_0)e^{-j\beta d}}{(Z_L + Z_0)e^{j\beta d} - (Z_L - Z_0)e^{-j\beta d}}$$
$$= Z_0 \frac{Z_L \cos\beta d + jZ_0 \sin\beta d}{Z_0 \cos\beta d + jZ_L \sin\beta d}$$
$$= Z_0 \frac{Z_L + jZ_0 \tan\beta d}{Z_0 + jZ_L \tan\beta d}$$

TL1, TL3 and TL4 provides a bias path for MOSFET1 from gate to drain. With $V_{gs} = V_{ds} = V_{bias1}$, the transistor is guaranteed to operate in saturation region. The drain-

source current, I_{ds}, transconductance, g_m, are all determined by V_g/ , V_s/ , V_d of the transistor.

On the other hand, T-Line TL3 and TL4 at high frequencies (60GHz) will provide the "voltage dividing" and impedance transformation features in the LNA. As discussed in chapter 4, the voltage from Y through T-Line to X is "divided". While it is possible to find a match of $\frac{V_y}{V_x} = A_{v,c}$ with only T-Line TL3 and TL4, TL5, TL6 and TL7 (shunt-stubs) are used to provide extra degrees of freedom in reaching proper $\frac{V_y}{V_x}$.

In real LNA design, not only the feedback ratio has to be considered, but also the input impedance. The input impedance in this case is the impedance looking into both TL1, TL2 and feedback path, $Z_{(in)1}$, $Z_{(in)2}$ and $Z_{(in)fb}$ respectively. The total input impedance is therefore $Z_{(in)1}//Z_{(in)2}//Z_{(in)fb}$. (this was derived at the end of subchapter 5.2).

Satisfying both:

$$\frac{V_y}{V_x} = A_{v,c}$$

$$Z_{(in)1}//Z_{(in)2}//Z_{(in)fb} = 50\Omega$$

is not easy, but can be accomplished by most circuit simulation software. What's needed is to carefully modify the T-Line length and characteristic impedance to find an optimum point to satisfy both equations above.

For a single stage Noise Canceling LNA with transmission line feedback (as shown in Fig. 5.16), simulations results are shown below in Fig. 5.17. From 57-66GHz, the maximum gain is 7.34dB; noise figure NF is well below 3dB over the entire range and can get as low as 2.37dB. Input/output impedance matching is reasonably good.

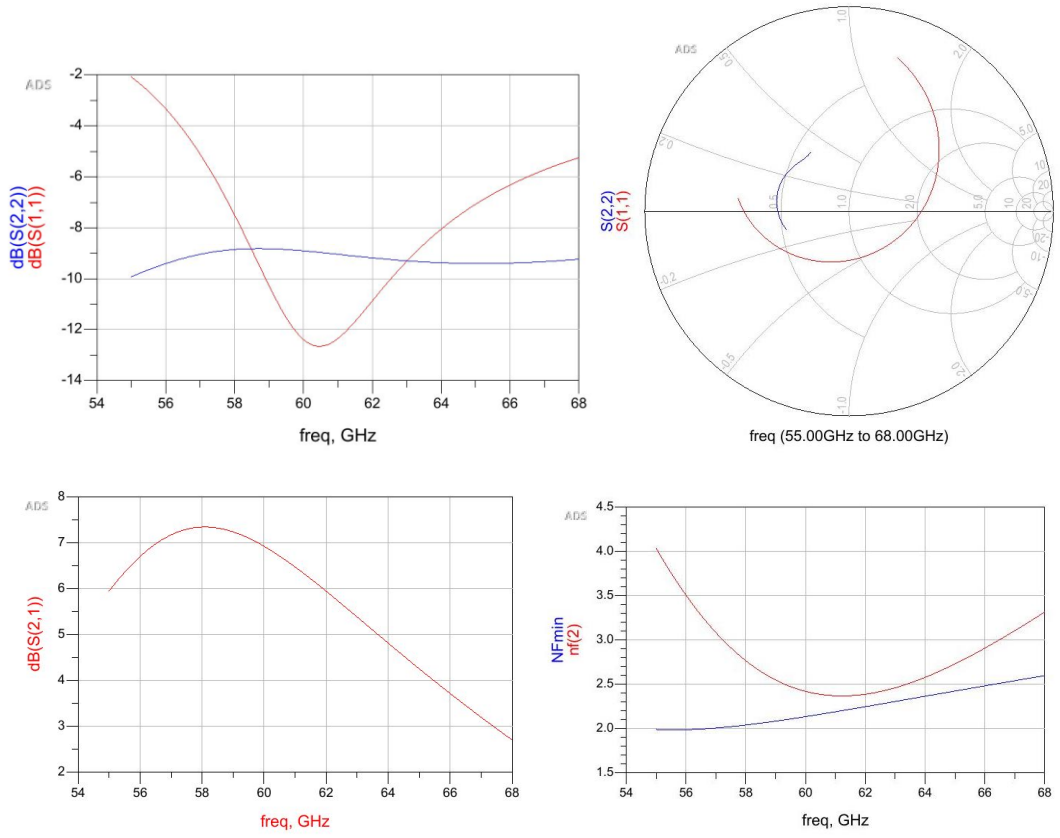


Fig 5.15 a) S11&S22 in dB; b) S11&S22 in Smith Chart; c) gain S21 in dB; d) NF and NFmin in dB

The 1-dB compression point is shown below. The gain droped 1 dB at input power = -17dB.

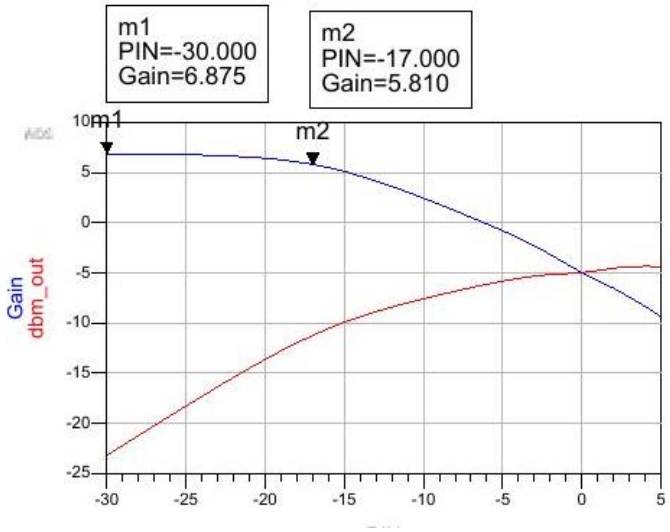


Fig 5.16 1dB compression point of single stage NCLNA with T-Line feedback

The stability factor "StabFact" is greater than unity and stability measure "StabMeas" is positive showing that the LNA is unconditionally stable, as shown in Fig. 5.19.

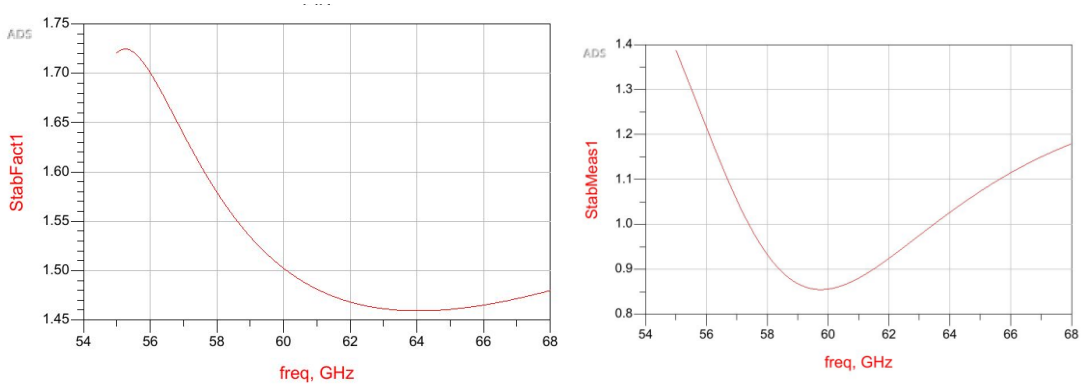


Fig 5.17 a) stability factor "StabFact"; b) stability measure "StabMeas"

The 1-dB compression point is significantly lower than comparable results, shown in following section. To improve linearity, the concept of derivative superposition [17] is introduced here.

In a common source configuration, the drain-source current can be expanded as below:

$$i_d(V_{gs}) = g_m V_{gs} + g_m{}' V_{gs} + g_m{}'' V_{gs} + \cdots$$

where g_m, $g_m{}'$ and $g_m{}''$ are transconductance and higher order coefficients. As shown in Fig 5.20, if we model the transconductance separately as individual voltage (Vgs) controlled current source, the collective effect of g_m, $g_m{}'$ and $g_m{}''$ then will determine the gain and output voltage of CS amplifier, which will affect 1-dB compression point.

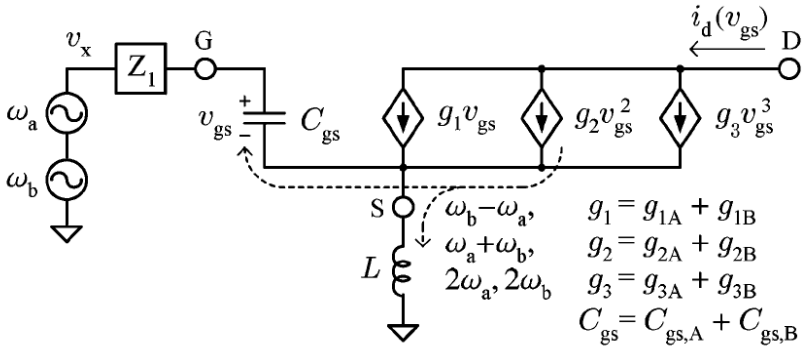


Fig 5.18 the small-signal nonlinear equivalent circuit of the CS amplifier [17]

The 3rd-order intercept point (IP3) is another indicator of how linear the circuit is. In the Fig 5.20, through the source degeneration inductor Ls, the RF signal is coupled back to gate. That will create unwanted signals like $2\omega_a$-ω_b, $2\omega_b$-ω_a that can not be filtered out. Therefore, the magnitude of $g_m{}''$ is very important to IP3. Its effect can

also be characterized as third-order intermodulation distortion (IMD_3), which determines IIP_3.

The basic ideal of derivative superposition to rectify the non-linearity issue in an amplifier by using two signal paths with g_m'' at different sign along both paths so as to cancel each other out. As shown below in Fig 5.21, when the biasing condition and transistor width changes, g_m'' changes from positive to zero to negative. This variation of g_m'' provides an opportunity to cancel out if there are two parallel CS amplifiers.

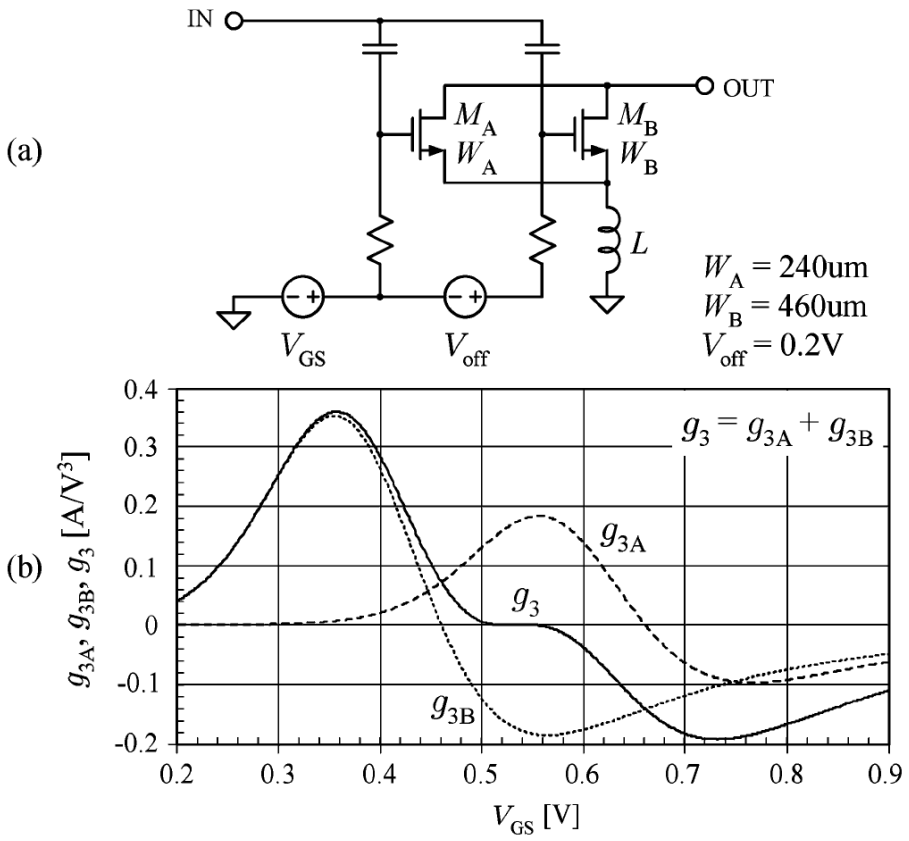


Fig 5.191 Derivative Superposition a). conceptrual schematic and b). g_m g_m''

g_m'' plot

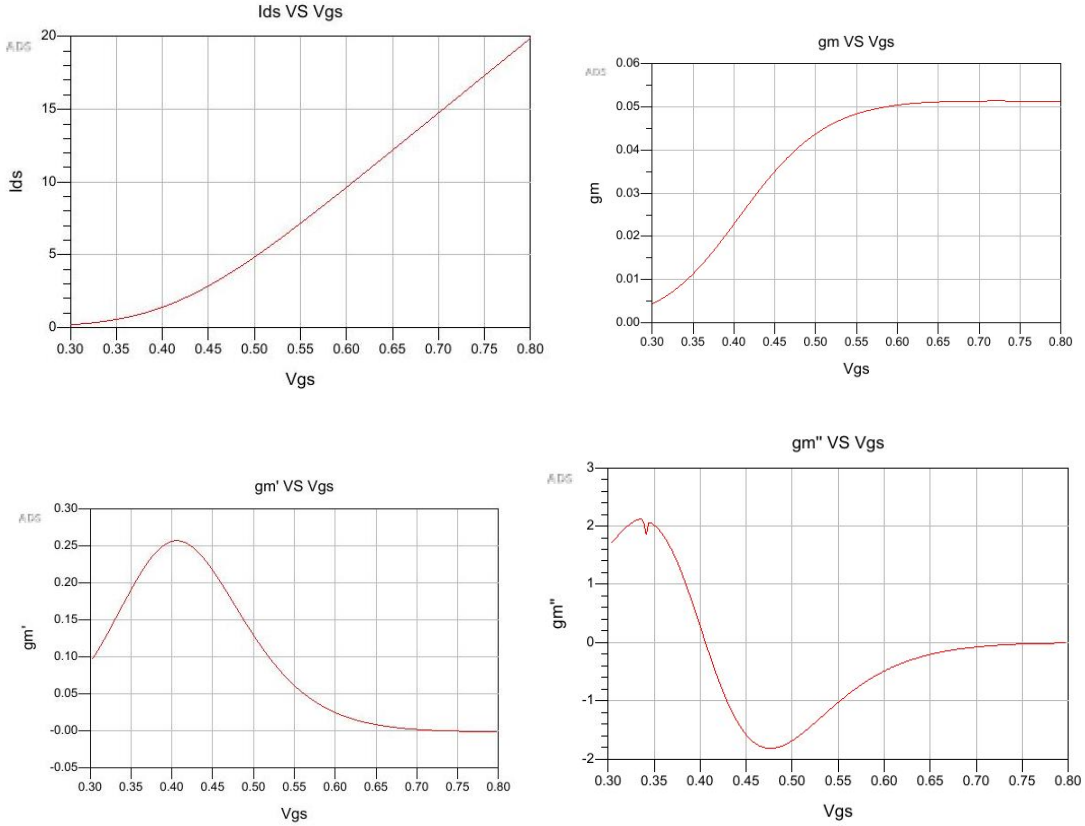


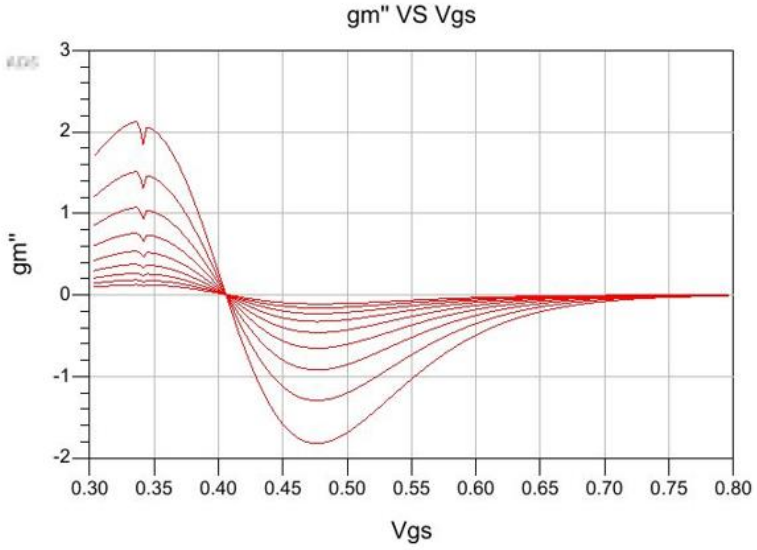
Fig 5.202 transconductance and higher order coefficients of CS amplifier

Fig 5.22 shows the transconductance and higher order transconductance coefficient of the CS amplifier M1 in our design. Because we have been biasing both transistor M1 and M2 at 500mV, we see the g_m'' of both transistors are near the negative maximum. The negative g_m'' in combined makes the third-order distortion large and reduces the linearity of the LNA.

In fact, noise-canceling LNAs are particularly suitable for derivative superposition in two ways:

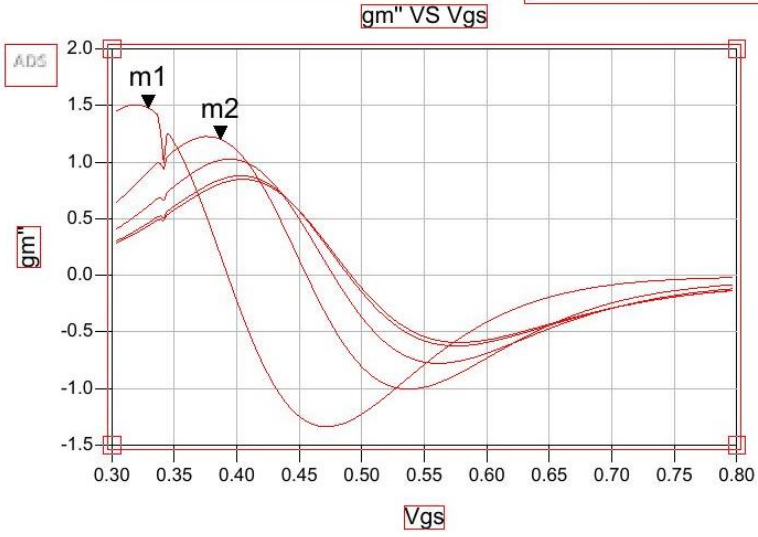
1) The derivative superposition architecture needs two parallel CS transistors (two signal paths) to cancel g_m''. The noise canceling LNA naturally uses the same structure.
2) The way to match g_m'' and noise-canceling can co-exist very well because they can be provided by different parameters. In both applications, there is one branch is designed to cancel the g_m'' noise on the other branch has, without disturbing the gain and g_m on that branch. That branch is sometimes called auxiliary branch because there is no stringent requirement to achieve a specific gain. In derivative superposition, we manipulate the width/length/Vgs of the auxiliary path transistor to match g_m''. In the noise-canceling circuit, we have the luxury of either matching noise feedback ratio to auxiliary gain or vise versa, we can match noise by only changing parameters in main branch and feedback path to provide sufficient noise canceling. Therefore, naturally derivative superposition and noise canceling LNA are very compatible.

To get a sense of how the derivative superposition should be applied in our noise-canceling circuit, we first study how the design variables length/width/Vgs/Vds affect g_m'', as shown in Fig 5.23 below:



m1
Vgs2=0.329
diff(diff(diff(I_Probe2.i)))=1.482
L=65.000

m2
Vgs2=0.387
diff(diff(diff(I_Probe2.i)))=1.204
L=85.000



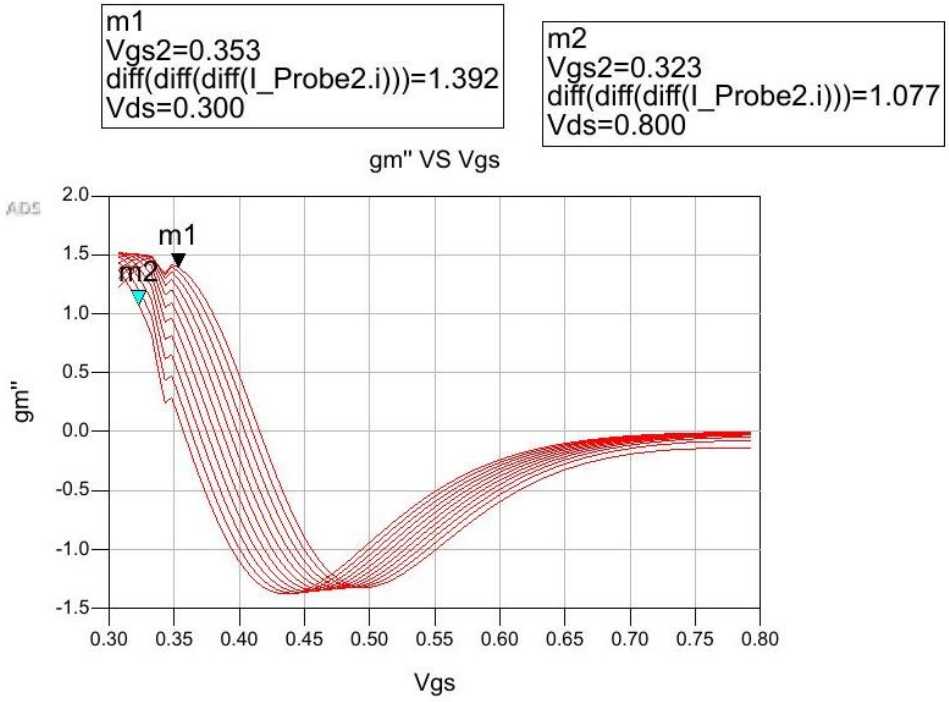


Fig 5.213 sweep width when length/Vds are fixed; b). sweep length when width/Vds are fixed; c). sweep Vds when width/length are fixed.

Out of the four parameters, length and Vds are less effective, increasing g_m'', but at the cost of increased noise. The variation of Vds has a limited effect in terms of reducing g_m'' at a given Vgs. Therefore, we focus on setting proper bias (Vgs) and width.

Although at roughly 400mV both g_m'' are close to zero, we can't bias both transistors at that voltage, due to the fact that at 400mV the transistor are in weak inversion. The threshold voltage of 65nm NMOS is in the range of 350mV to 400mV. The transistor can only provide limited gain and bandwidth in weak inversion region.

Therefore, the only solution is biasing the main path Vgs > 600mV, to provide gain and minimize g_m''. The auxiliary path transistor is set to < 400mV to provide the negative g_m'' component. Then carefully modify transistor width to closely match the magnitude of g_m'' from both transistors.

The derivative superposition noise-canceling LNA was designed as shown in Fig 5.23. Since we are independently biasing both transistor, one extra capacitance is added to seperately biasing the auxiliary path. After careful re-design the parameters of the circuit, the performance of single stage derivative superposition noise-canceling LNA are shown in Fig 5.24.

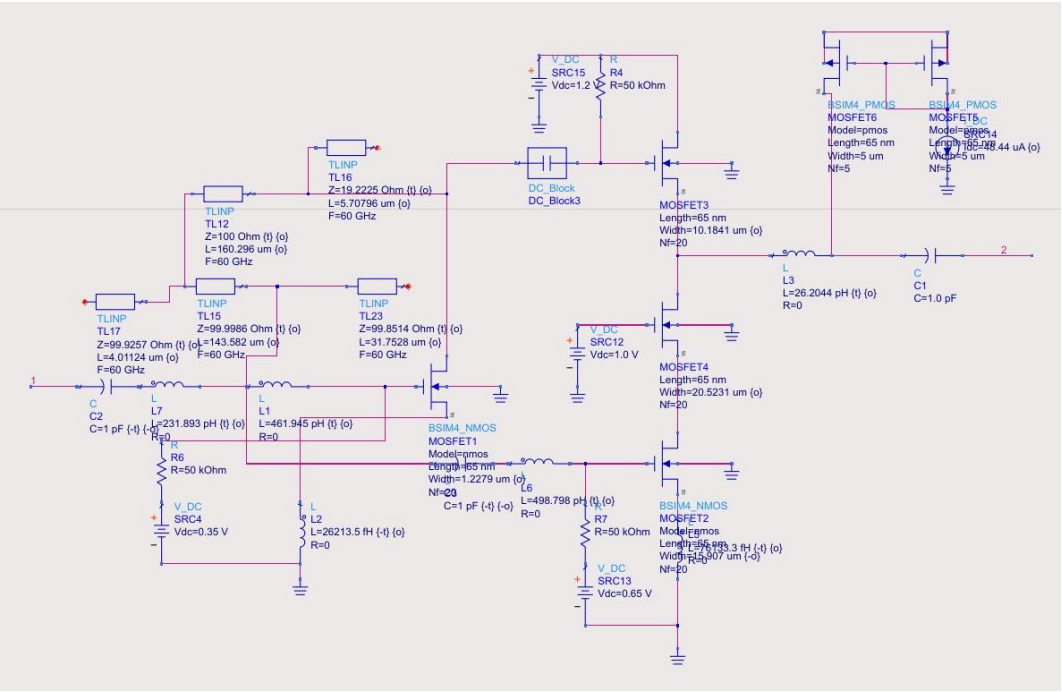


Fig 5.224 the derivative superposition Noise-Canceling LNA

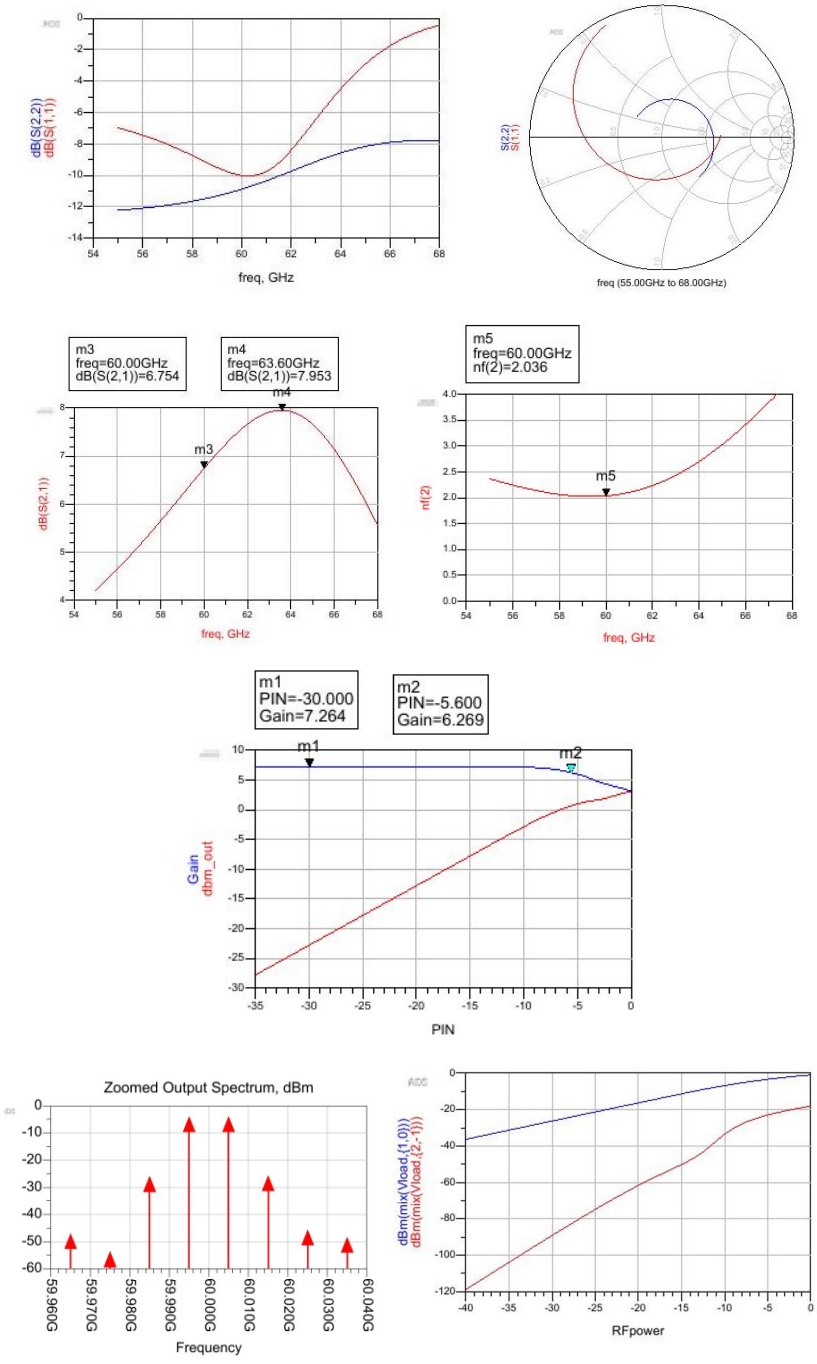


Fig 5.235 the performance of LNA in Fig 5.23: a). S11 and S22 in dB; b). S11 and S22 in smith chart; c). gain S21; d). NF and NFmin; e). 1-dB compression point; f). 3rd order harmonics in dBm; g). IP3.

Fig 5.25 shows simulation results of a single stage Noise Canceling LNA with transmission line feedback (as shown in Fig. 5.24). From 57-66GHz, the maximum gain is 7.95dB; noise figure NF is well below 3dB over the entire range and can get as low as 2.04dB. Input/output impedance matching is reasonably good. The 1-dB compression point is now -5.6dBm (input referred, or +1.1dBm output referred 1-dB compression point).

To summarize the methodology for designing a 60GHz noise-canceling LNA with transmission line feedback, and its changes from the way we were designing traditional LNA:

1). Make a Common Source amplifier, MOSFET1, with drain and gate biased at same DC voltage, terminated into a source follower MOSFET3. Optimize transistor width/length to max g_{m1}.

2). Create auxiliary Common Source amplifier MOSFET2 and cascode transistor MOSFET4. MOSFET2 is set to an satisfy the "derivative superposition", where requiring MOSFET2 $g''_{m2} = -g''_{m1}$, to maximize linearity of system.

3). Connect gate and drain of transistor with T-Line feedback. The feedback path could be series-shunt-series stubs, shunt-series-shunt stubs or more complicated topologies like series-shunt-series-shunt-series shown in example design. The goal of

this feedback, as discussed above, is to provide voltage dividing from $V_Y/V_X = A_{V,C}$, where $A_{V,C}$ is the gain of MOSFET2.

4). Input impedance match by providing either LC or T-Line to gate of transistor MOSFET1&MOSFET2 independently.

5). Refine the voltage dividing ratio after step 4 by changing feedback T-Line lengths. The alternative is to change $A_{V,C}$ of MOSFET2 to match the new V_Y/V_X. Track s-parameter and NF while doing this refinement.

For a 3-stage LNA, with guideline of system LNA design in Chapter 5.2, we construct the cascade LNA like Fig. 5.26. The major change from the single stage LNA is inter-stage output/input impedance matching, and latter stages prioritize gain over noise.

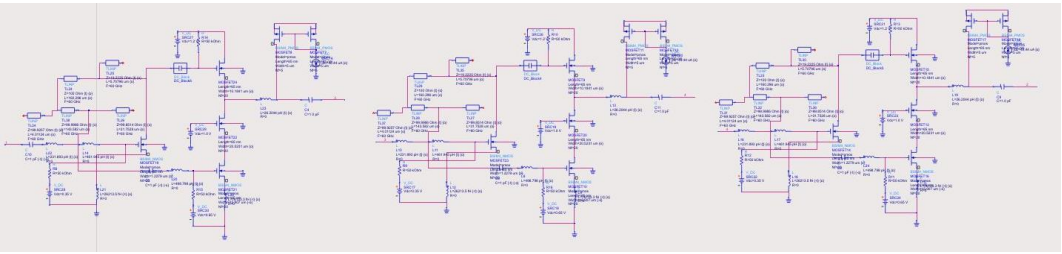


Fig 5.246 schematic of 3-stage NCLNA with T-Line feedback

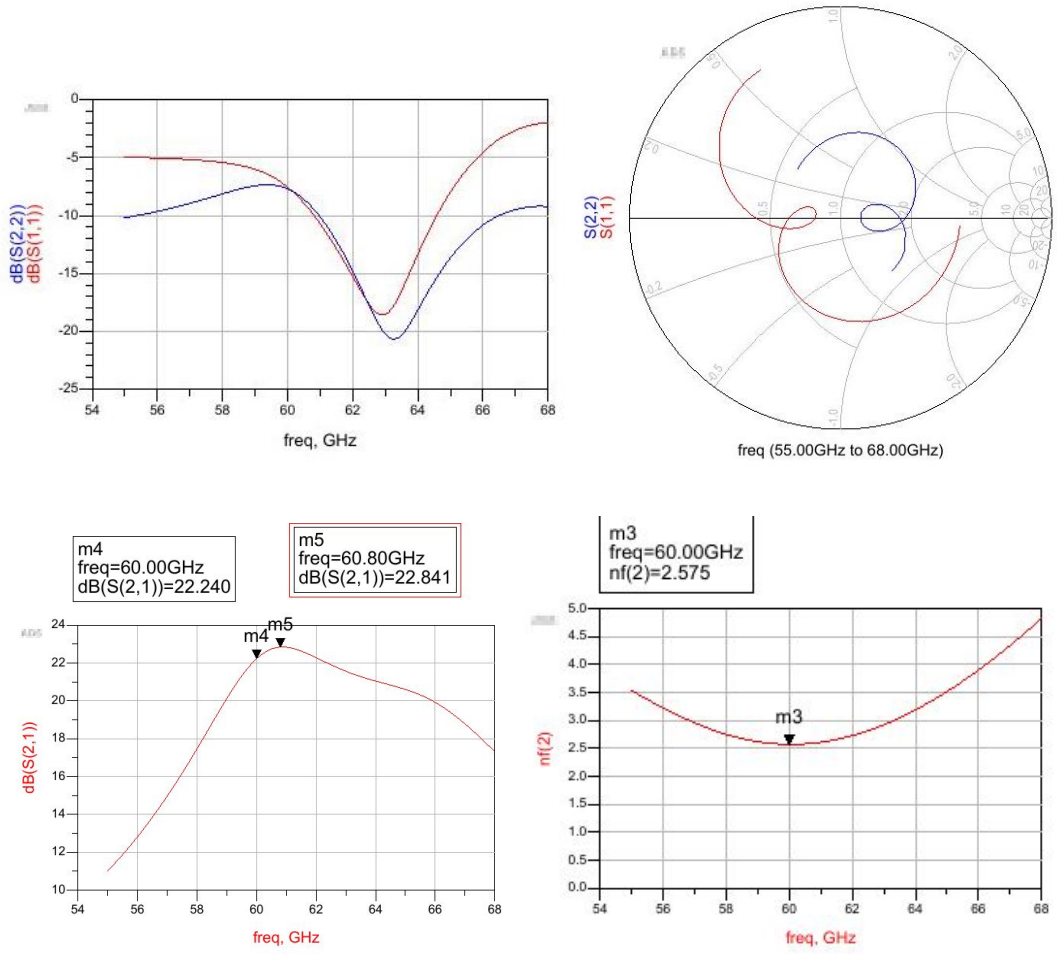


Fig 5.257 a) S11&S22 in dB; b) S11&S22 in Smith Chart; c) gain S21 in dB; d) NF and NFmin in dB

Simulation results are shown above in Fig. 5.27. In the operation frequencies from 57-66GHz, the gain is well over 16dB with peak gain at 22.8dB; noise figure is below 3.5dB with minimum NF at 2.58dB. Input/output impedance is reasonable matched.

Fig. 5.28 shows the stability criteria of the LNA. Once again, the stability factor "StabFact" is greater than unity and stability measure "StabMeas" is positive showing the LNA is unconditionally stable

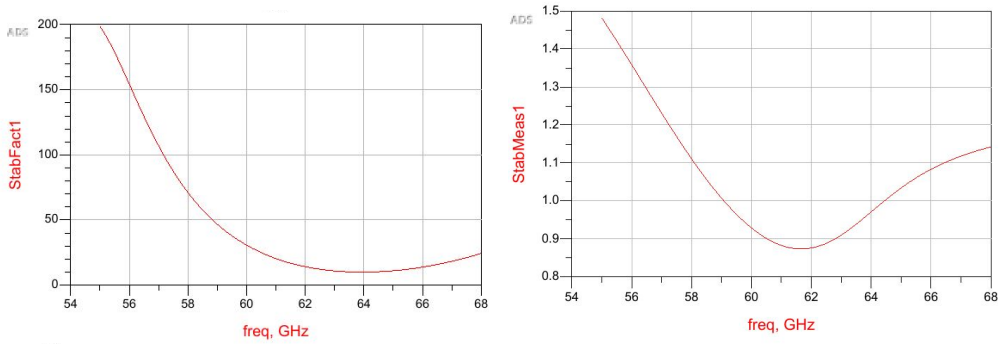


Fig 5.268 a) stability factor "StabFact"; b) stability measure "StabMeas"

Linearity is shown below in the 1-dB compression point plot. The gain dropped 1 dB at an input power = -21dBm. The output referred 1-dB compression point at 1.24dBm.

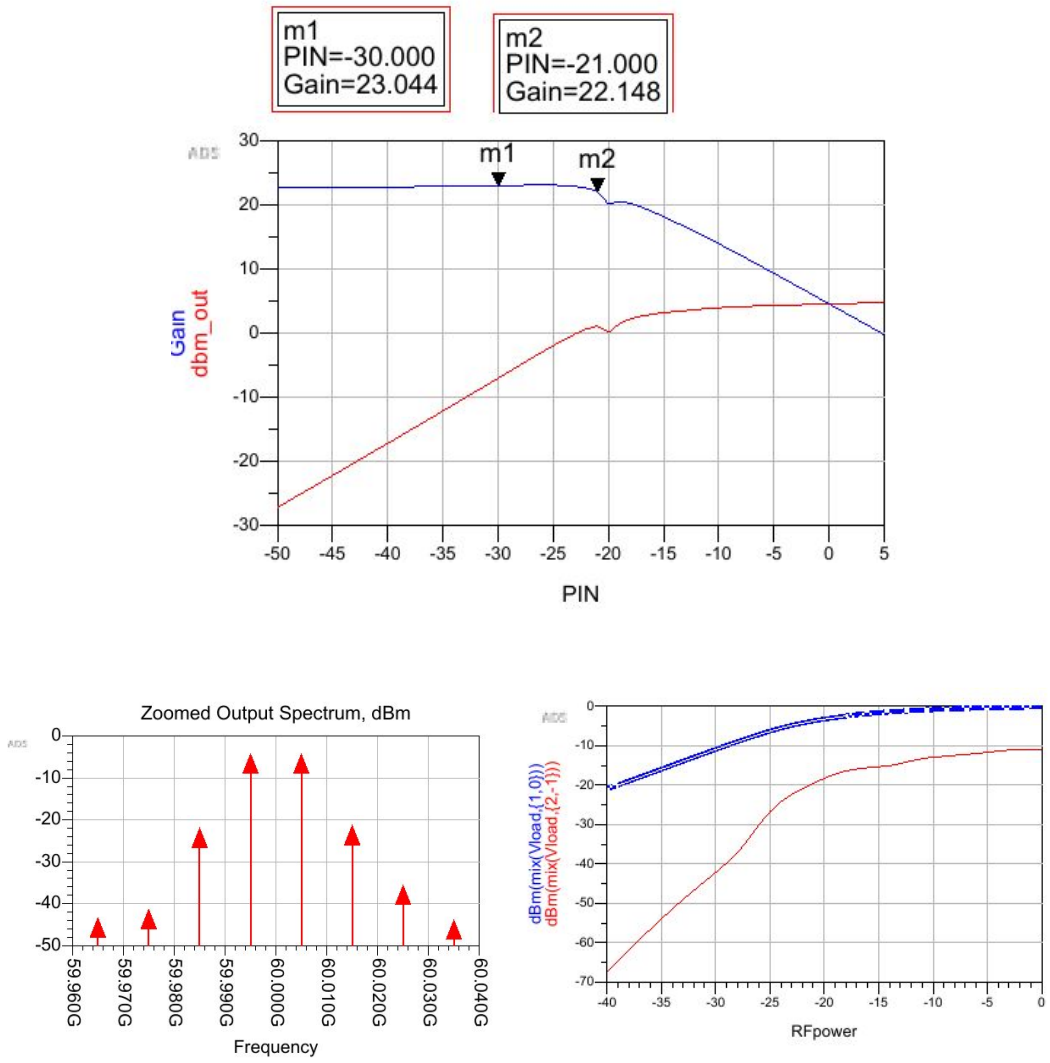


Fig 5.279 3-stages NCLNA with T-Line feedback: a). 1-dB compression point; b). 3rd order harmonics in dBm; c). IP3

For the LNA, power and area consumption are also very important. There are two DC power sources feeding power into the system, the biasing voltage source for MOSFET1 gate, which is also responsible for providing the DC biasing current for

MOSFET1 I_{ds}, and the DC biasing current for MOSFET2/3/4 I_{ds}. The total current provided for 3 stages results in a power consumption of 9.6mW.

To summarize my design simulation results, and to highlights the key improvement from a resistive feedback LNA to a T-Line feedback LNA, a table is presented below:

	Gain S21 (dB)	NF (dB)	1dB compression point (output referred)
1-stage Resistive	4.4	2.8	-9.6
3-stage Resistive	14.7	3.4	-10
1-stage T-Line	7.95	2.04	+1.1
3-stage T-Line	22.84	2.58	+1.24

5.6 Results and comparison

In the following table, a detailed comparison of reported 60GHz low-noise amplifiers is presented. Among all specs, our design has second highest gain, second best linearity and the lowest recorded NF. Our NF is significantly from the next best value by over 30%.

Ref	Tech [nm]	Freq [GHz]	Max Gain [dB]	P-1dB [dBm]	min NF [dB]	Vdd [V]	Power [mW]	Technology
[1]	65	56	22.4	-3.4	4.5	1.5	16.8	2 cascode
[1]	65	56	18.7	-6.5	5.2	1.0	8.5	2 cascode
[2]	65	60	23	-3.5	4	1.25	8	3 CS TF+CF*
[3]	65	59	16.2	-4.85	3.8	1	8.3	3 CS+CPW
[4]	65	60	20.6	-8.4	4.9	1.2	33.6	TL based
[4]	65	60	18	-5	4.0	1.2	28.8	Inductor based
[5]	65	60	15	-6	5.9	1.5	31	4 cascode
[6]	65	60	22.3 (19.3)	2.7	6.1	1.2	35	differential
[7]	65	61.2	18.9	-22.3	6.06	1.8	45	3 cascode
This work	65	60	20.8	**	3.08	1.2	14	3 T-Line FB
This work	65	60	22.84	1.24*	2.57	1.2	9.6	3 NC T-Line FB

a. TF+CF = transformer + capacitive feedback

b. Derivative Superposition

Summary:

In this chapter, two Noise Canceling LNA were designed to investigate the practicality of the ideas proposed, the noise-canceling at 60GHz and the T-Line constructed feedback path. We started with the fundamentals of the design of a NC-LNA, including how to design CS amplifiers and shunt-feedback amplifiers. Specifically, the theory of designing a shunt-feedback amplifier with a T-Line was analyzed mathematically. Secondly, a Noise Canceling LNA with resistive feedback is designed for comparison. The source impedance is carefully matched to satisfy the noise canceling condition. Simulation results show the effectiveness of complex feedback path noise canceling LNA. Finally, a novel topology using a transmission line as feedback path to design noise canceling LNA is presented, providing noise figure improvement lower than any NF ever get reported.

Chapter 6 Future works

In low-gigahertz communications, there are numerous publications of architecture innovations to improve the performance of circuitry. Like the noise-canceling topology we discussed in our paper, the NC-LNA traded off gain and power consumption for lower noise-figures and less distortion. This trade-off was not possible in 130nm/180nm CMOS technologies, as the ft and fmax of transistor are limited and no luxury of gain can be afforded at 60GHz (mmWave frequencies). However, as the silicon technologies keeps advancing, those advanced topologies could be revisited in newer technologies and might make an impact.

The high frequency and small wavelength of mmWave drive traditional lumped circuitry towards the use of distributed elements. For example, as other publications have mentioned, using transmission line to do impedance matching gives more accurate modeling of passive devices and reduces complexity of matching. In this dissertation, based on the wave feedforward and reflection theory, we came up with voltage dividing feature that suits feedback voltage dividing, which conventionally is accomplished by resistors in series in lumped circuit realizations. Applying distributed elements to lumped circuit would be interesting and likely full of potential improvement for high frequency operations.

An obvious next step is to fabricate and test circuits using these approaches.

Chapter 7 Conclusion

In this dissertation, a complete design of a 60GHz transmission line feedback low-noise amplifier has been presented. It was designed using 65nm CMOS technology and simulated in ADS. This noise-canceling LNA has advantages of very high linearity and lowest noise figure ever reported by all existing 60GHz CMOS LNAs.

The idea of using noise-canceling topology in 60GHz comes from existing noise-canceling publications in sub-6GHz. This dissertation started with reviewing sub-6GHz noise-canceling LNA design. Specifically, common-source cascode amplifier and shunt-series feedback amplifier design are reviewed in detail as both of them are core blocks of the noise-canceling topology been adopted.

Due to the natural of limited gain CMOS can provide for 60GHz, there haven't been too much publications of feedback amplifier examples in 60GHz. This dissertation designed and simulated two shunt-series feedback LNAs, one with a resistor feedback path and one with transmission line feedback path. The transmission line feedback path is favored since it creates a feedback path without adding any additional noise. Both LNA works very well as foundation for noise-canceling LNA.

In the process of designing transmission line feedback path, two innovative applications of transmission line have been proposed and validated: 1). to use transmission line as voltage dividing component; 2). to use transmission line as impedance transformation for input/output impedance matching purposes. Both applications are analyzed and mathematically derived from distributed system fundamental equations and verified in circuit simulators. Guidance for the design of transmission lines to fulfill those applications are proposed and simulated.

Finally, a transmission line feedback noise-canceling LNA in 60GHz was presented. In pursuit for a better linearity, a combination of noise-canceling and derivative superposition was proposed. Eventually, a noise-canceling LNA working at 60GHz, with 22.84dB gain, 2.57dB noise figure and 1.24dBm output-referred 1-dB compression point, was designed and simulated. The noise performance is significantly superior than other LNAs published.

Chapter 8 Appendix

Chapter 5.2 gives the gain / input impedance / output impedance derivation. Here, the Matlab script used for evaluation is shown in the section below.

For a series-shunt-series transmission line, the voltage ratio is calculated in Matlab script as:

```
% voltage ratio calculator


% d1 = -pi-0.1: pi/100: pi-0.1;

d1 = 0.4611*pi

beta = 1

Z0_1 = 100

Z0_3 = 100

ZL = 50


voltage_ratio_1 = cos(beta*d1)+i*sin(beta*d1)*(Z0_1/ZL)


Zin_1 = Z0_1 * ((ZL+i*Z0_1*tan(beta*d1))./(Z0_1+i*ZL*tan(beta*d1)))
```

```
% with a shunt stub at load

Z0_2 = 100

d2 = 0.4611*pi

% d2 = -pi-0.1: pi/100: pi-0.1

Zin_2 = (-i*ZL*Z0_2*cot(beta*d2)) ./ (ZL-i*Z0_2*cot(beta*d2))


d3 = 0.4611*pi

% d3 = -pi-0.1: pi/100: pi-0.1;


voltage_ratio_2 = cos(beta*d3)+i*sin(beta*d3).*(Z0_3./Zin_2)


voltage_ratio = voltage_ratio_1.*voltage_ratio_2


result1 = real (voltage_ratio)

result2 = imag (voltage_ratio)


figure

plot(d3, result1)
```

figure

plot(d3, result2)

For input impedance is calculated as:

gm = 0.2

Rf = 200

Rl = 40

Z0 = 100

beta = 0.4611*pi

d = 1

% gamma = (Zl-Z0)/(Zl+Z0)

gamma = ((1/Z0)-(1/Rl)-gm*exp(i*beta*d))/((1/Z0)+(1/Rl)+gm*exp(-i*beta*d))

% Zl = (1+gamma)/(((1+gamma)/Rl)+gm(exp(i*beta*d)+gamma*exp(-i*beta*d)))

For output impedance is calculated as:

Z0 = 100

RL = 50

Rs = 50

```
Rf = 200

Zs = 50

gm = 0.2

beta = 0.4611*pi

d = 1

gamma = (Zs-Z0)/(Zs+Z0)


% variable definition


% resistive case

Vgs = Rs/(Rf+Rs)

Zout_resistive = 1/((1/RL) + gm*(Rs/(Rf+Rs)) + 1/(Rf+Rs))


% transmission line case

Zout_t_line = 1 / ( (gm*(1+gamma)) / (exp(i*beta*d)+gamma*exp(-i*beta*d)) +

(exp(i*beta*d)-gamma*exp(-i*beta*d))/((exp(i*beta*d)+gamma*exp(-

i*beta*d))*Z0) )


% Vgs = (Vx)
```

% result = Vx/(Ztlr +gm*Vgs)

Amplifier gain equation is given as:

% resistive gain equations:

gm = 0.2

Rf = 200

RL = 40

ZL = 200

% ZL = 40

Rs1= 50

Rs = 50

Z0 = 100

beta = 0.8

% beta = 0.4611*pi

d = 1

```
amp_gain = - gm * ((Rf*RL) / (Rf + RL)) + RL / (Rf + RL)

input_impedance_FB = 1/(gm+(-gm+1/Rf)*(Rf/(Rf+RL)))

input_impedance_1 = (input_impedance_FB * Rs1)/(input_impedance_FB + Rs1)

Mag_S21 = ( (input_impedance_1 / (input_impedance_1 + Rs)) / 0.5 ) * amp_gain

% Ken_Gain = - gm * (((Rf+Rs)*RL) / ((Rf+Rs) + RL)) + RL / ((Rf+Rs) + RL)

% transmission line gain

gamma = ((1/Z0)-(1/RL)-gm*exp(i*beta*d))/((1/Z0)+(1/RL)+gm*exp(-i*beta*d))

input_impedance_tline = ((1+gamma*exp(-2*i*beta*d))/(1- gamma*exp(-
2*i*beta*d)))*Z0

input_impedance_2 = (input_impedance_tline * Rs1) / (input_impedance_tline +
Rs1)
```

```
Ztlr = Z0 * ((25+i*Z0*tan(beta*d))/(Z0+i*25*tan(beta*d)))    % 25= 50//50 here

vccs_gain = -gm * ( (RL*Ztlr) / (RL + Ztlr) )

feedforward_gain = 1 / (cos(beta*d)+ i*sin(beta*d)*Z0/ZL)

amp_gain_tline = (vccs_gain) + (feedforward_gain)

S21_tline = ( (input_impedance_2 / (input_impedance_2 + Rs)) / 0.5 ) *
amp_gain_tline

Mag_S21_tline = abs(S21_tline)
```

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