UNIVERSITY OF CALIFORNIA SAN DIEGO

Advances in Millimeter-wave Phased-Array Systems, RFICs and Cross-Point Switch Matrices

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Professor Daniel Sievenpiper

2020

The dissertation of Yaochen Wang is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2020

DEDICATION

To my family

EPIGRAPH

Man proposes, God disposes.

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Chapter 2, in partly, is a reprint of the material as it appears in: Yaochen Wang, Thomas Phelps, Kerim Kibaroglu, M. Sayginer, Qian Ma and Gabriel M. Rebeiz, "28 GHz 5G-Based Phased-Arrays for UAV Detection and Automotive Traffic-Monitoring Radars," 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, 2018, pp. 895-898

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Chapter 4 is, in partly, has been published in: Yaochen Wang, Hyunchul Chung, Qian Ma and Gabriel M. Rebeiz, "A 57.5-65.5 GHz Phased-Array Transmit Beamformer in 45 nm CMOS SOI with 5 dBm and 6.1% Linear PAE for 400 MBaud 64-QAM Waveforms",*IEEE Trans. Microw. Theory Techn.*

Chapter 5 is, in partly, will be submitted for publication of the material as it may appear in: Yaochen Wang, Yang Yang and Gabriel M. Rebeiz, "A Low-Power 30-Gbps 16×16 Active Cross-Point Switch Matrix in 45-nm CMOS SOI",*IEEE J. Solid-State Circuits*

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PUBLICATIONS

Yaochen Wang, Thomas Phelps, Kerim Kibaroglu, Mustafa Sayginer, Qian Ma, Gabriel M. Rebeiz, "28 GHz 5G-based phased-arrays for UAV detection and automotive traffic-monitoring radars", 2018 IEEE MTT-S International Microwave Symposium, Philadelphia, Pennsylvania, USA, Jun. 2018

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Yaochen Wang, Yang Yang, Gabriel M. Rebeiz, "A 30-Gbps 16$\times$16 Active Cross-Point Switch Matrix in 45-nm SOI CMOS", *IEEE J. Solid-State Circuits*

Bhaskara Rupakula, Ahmed Nafe, Samet Zihir, Yaochen Wang, Tsu-Wei Lin, Gabriel M. Rebeiz, "63.5–65.5 GHz Transmit/Receive Phased-Array Communication Link With 0.5–2 Gb/s at 100–800 m and +/- 50 degree Scan Angles". *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 9, pp. 4108-4120, Jun. 2018

ABSTRACT OF THE DISSERTATION

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by

Yaochen Wang

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2020

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With the technical revolution on hardware and software of communication system, the fifth generation mobile communication systems (5G) is followed into the spotlight. In the 5G era, the frequency band will be in millimeter-wave region (24-60 GHz) and the available bandwidth can be the unthinkable in the 4G age. As a result, the data rate in the coming future can arrive >100 times higher than what we have currently employed. Its feature on high data rate and low delay will bring the significant improvement on the associated industries, such as autonomous vehicle, Internet-of-Tings (IoT)...

However, the mm-wave signals also bring the more challenge on the 5G system design

of the mobile and base station. It will suffer from the high atmospheric absorption in the communication, which is the dominant limitation on the long-distance communication in 5G. Therefore, it is essential to develop the 5G communication system and mm-wave ICs to overcome the physical limitation of mm-wave. The research projects in this dissertation, in consequence, focus on communication system design and mm-wave ICs for 5G. Also, it shows the advanced high data-rate ICs for IoT, which will be implemented of 5G era.

Chapter 1

Introduction

1.1 Background

The upcoming fifth-generation(5G) era utilizes millimeter-wave with the frequency band of 24 to 60 GHz. The usage of mm-wave bring the possibility of wider bandwidth, high data rate and low delay in the 5G era. Actually, it has been shown experimentally in numerous studies that the mm-wave communication system can support up to tens of Gb/s data rate, compared with hundreds of Mb/s at most in the forth generation (4G), due to the significant increment of the bandwidth. It could revolutionize many areas and the way we live and bring the major improvements on autonomous vehicle, Internet-of-Things (IoT), low-latency remote medical monitoring and cloud computing.

Due to mm-wave's high atmospheric attenuation in the air, the dominant challenge on 5G commercialization is the transmission distance of the mm-wave communication system. Therefore, the beam-forming technology is one of the research hotspots and it can focus the signal power on the scannable beams to improve the SNR and communication distance in the mm-wave region. Due to the wavelength of < 1 mm, more antenna elements can be integrated in the small devices to build the phased arrays to implement the beam-forming and overcome the free space

loss at the mm-wave band. In additional, the interference of adjacent cells can be reduced due to the focused beam. In the coming future, the phased arrays will be applied on the based stations and customer edge devices in 5G.

5G commercialization also proposes high requirements in the device and design perspective point of view. With the development of the semiconductors, the SiGe HBT (silicon-germanium hetero-junction bipolar transistor) and bulk, SOI(silicon-on-insulator), FDSOI (fully depleted SOI), and CMOS FET (complementary metal-oxidesemiconductor field effect transistor) can provide the good RF performance (f_t and f_{max} of $>$ 200 GHz). However, the gain/power efficiency is significantly worse than the lower frequency circuit (such as $\sim$2 GHz in 4G era). Therefore, the 5G circuit designer should propose the innovation of the circuit topology and system architecture to remedy the limitation of the device at the high frequency.

With the growth of 5G communication, the potential of cloud computing has been noticed and all the data can be stored and processed in the cloud when the high data rate and low latency communication come true. The customer edge device can be smaller and more power-efficient, which just need to achieve the the feature of visualization. The communication circuit with high speed between various severs inside the cloud computing network is another field of research nowadays. Tens of Gbps data rate of wire-line communication also brings the new challenge on the circuit design.

1.2 Motivation

The implementation of phased array on the hardware can realize the potential in many applications, such as target detection and monitoring. These functions can be achieved on the same phased arrays and there is no additional cost due to no changing on the hardware and just changing on the software and waveforms.

In the mm-wave circuit design of next generation communication systems, the low effi-

ciency and low linear output power of previous beam-forming chips are the dominant limitation in system design. The former can cause the inevitable high power consumption and heat generation. The latter can limit the radiated power and maximum communication distance. Thus, there is pressing need on finding the solution on these two issues from circuit design and system architecture.

Furthermore, the transmitting(Tx) and receiving(Rx) phase arrays can be built with close proximity in the base stations. The leakage from Tx array to Rx array can saturate the Rx system and affect its performance. Hence, the high linearity circuit is high demand to avoid this issue, especially on the down-conversion mixer.

Due to the growing amount of data traffic in both long-haul and short-haul communication networks, high-speed non-blocking cross-point switches have attracted a lot of interest in the past few years. This versatile circuit, which can connect any input port (N) to any output port (M), is essential for reconfiguring the networks both at the server level and between a cluster of servers. In large switch matrices, line amplifiers are used between the different row/column cells to act as isolators between the switching cells. This requires a lot of DC power, and switch matrices are known to be highly inefficient.

1.3 Thesis Overview

This thesis presents the system design in the 5G communication and fully integrated mm-wave circuits for phased arrays and high data rate communication circuit.

Chapter 2 presents the multi-function 5G base station designs which can not only provide the high data rate communication but also show the feasibility of the UAV detection and automotive traffic-monitoring on the same phase arrays. A long-distance and high-resolution FMCW radar system has been achieved using 28 GHz and 60 GHz 5G phased-arrays. As shown in the measurements, the 5G based radar system can detect a small UAV at a range greater than 250 m

and 110 m distance, respectively.

Chapter 3 presents a low-power, high-gain, high-linearity phased-array transmit (Tx) beamformer chip in 45 nm RFSOI process. An architecture employing a power amplifier with neutralization, a 180° active phase shifter and 11/22/45/90° passive phase shifters results in high linearity and low power consumption. The measured gain is 22 dB with a 3-dB bandwidth of 57.5-65.5 GHz and an OP_{1dB} and OP_{sat} of 7.5-10 dBm and 9.5-11.5 dBm at 57-64 GHz, respectively. A peak power added efficiency (PAE) of 14.6% and 17.6% at 60 GHz is achieved at P_{1dB} and P_{sat}, respectively. The measured RMS phase and gain errors are $< 4°$ and < 0.7 dB at 57-64 GHz, respectively. The beamformer chip also has 14 dB gain control with less than 2.8 dB drop in the OP_{1dB}. Complex modulation measurements using a 400 MBaud 64-QAM waveform show an error vector magnitude (EVM) of 5% (-26 dB) at an average power 5 dBm and with a DC power consumption of only 52 mW, resulting in a linear PAE of 6.1%. Also, 18-20 Gbps data rates are demonstrated with an EVM $< 5\%$ (64-QAM) and $< 9\%$ (16-QAM) at 60 GHz. To author's knowledge, this work achieves state-of-the-art linearity and efficiency for 60 GHz communication systems.

Chapter 4 presents a high linearity 60 GHz mixer designed in GF8HP 0.12 μm SiGe BiCMOS technology and its flip-chip packaging is achieved on the low cost PCB. The LO structure can be selected for doubler path and thru path by SPDTs for various applications. And the mixer design is based on the double balanced passive mixer with adjustable bias voltage control to compensate the transistors mismatch. Optimization on the transistor and its layout has resulted in the around -13.5 dB conversion loss in 55-67 GHz with 0 dBm LO driving power. With assembled on the low cost RF board, the mixer board can reach around -18 dB conversion loss with < 45 dBm LO leakage shown at the RF port. The IIP3 measurement is limited by the measurement setup and IIP3 of this proposed mixer board should be > 24 dBm, which is the highest known to-date.

Chapter 5 presents a 30 Gbps 16x16 switch matrix in 45nm CMOS technology, with

a three-stage buffer-based active switch as the row/column switching core. The row and column loaded transmission lines and termination resistors are optimized for low-power and high-frequency performance, and with high isolation between channels. The 16×16 switch matrix operates at 30 Gbps signal with an average peak-to-peak jitter of 6.6 ps and >0.52 V eye height over the different paths, and consumes 16-17 mW per path (0.55 pJ/bit) at 30 Gbps. Simulations indicate that the switch matrix can operate at 64 Gbps with minor variation in the termination resistors. Also, the design can be scaled to 64×64 (and larger) switch matrices with virtually no change in any circuitry. Application areas are in non-blocking cross-point switch matrices data routing at the server level or multi-processor level. To the author's knowledge, this work represents the lowest power consumption to-date for any switch matrix design.

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Chapter 2

28 GHz/ 64GHz 5G-Based Phased-Arrays for UAV Detection and Automotive Traffic-Monitoring Radars

2.1 Introduction

The introduction of phased-arrays into 5G base stations will not only enable the next generation of cellular communication with Gbps data rates, but can also result in base stations with interesting capabilities that were not possible before. The narrow, steerable beam of a phased-array allows the base-stations to also be used as an FMCW radar system with no additional resources on the RF front-end. This is especially true with 256-element 4x4 MIMO, or 128-element 2x2 MIMO, or 64-element horizontaly-polarized and 64-element verticaly-polarized 5G arrays. In this case, one array (typically 64-elements) would be used as a Tx-only system in FMCW radar mode, and the other array (typically 64-elements) would be used as an Rx-only system. This capability would allow for the detection of UAVs in urban environments and even automotive traffic monitoring at road intersections. The potential therefore exists for one base sta-tion to

Figure 2.1: A single phased-array serving multiple functions.

act not only as a communication site, but as a power-ful radar sensor in a network of devices that could deliver a multitude of functions (Fig. 2.1). In order to demonstrate the versatility of the 5G Tx/Rx phased-arrays, we designed an FMCW radar incorporating standard 5G Tx/Rx arrays employed as FMCW transmitters and receivers(Fig. 2.2). Small UAV detection was easily possible up to 250 meters with 28 GHz arrays and 110 meters with 64 GHz arrays.

2.2 28 GHz Phased-Arrays for 5G communication and UAV detection

2.2.1 28 GHz FMCW SYSTEM DESIGN

The 28 GHz FMCW radar employs 64-element phased-arrays designed for 5G communications (Fig. 2.3) [1]. At 30 GHz, the elements are spaced 0.5λ in the horizontal direction and 0.63λ in the vertical direction. This allows the array to scan without grating lobes up to ±50° in azimuth and ±25° in elevation. In the Tx mode, the 5G arrays provide an EIRP of 50-52 dBm at Psat with an antenna gain, $G_{Tx} = G_{Rx} = 22.5$ dB (the antenna gain includes antenna loss and

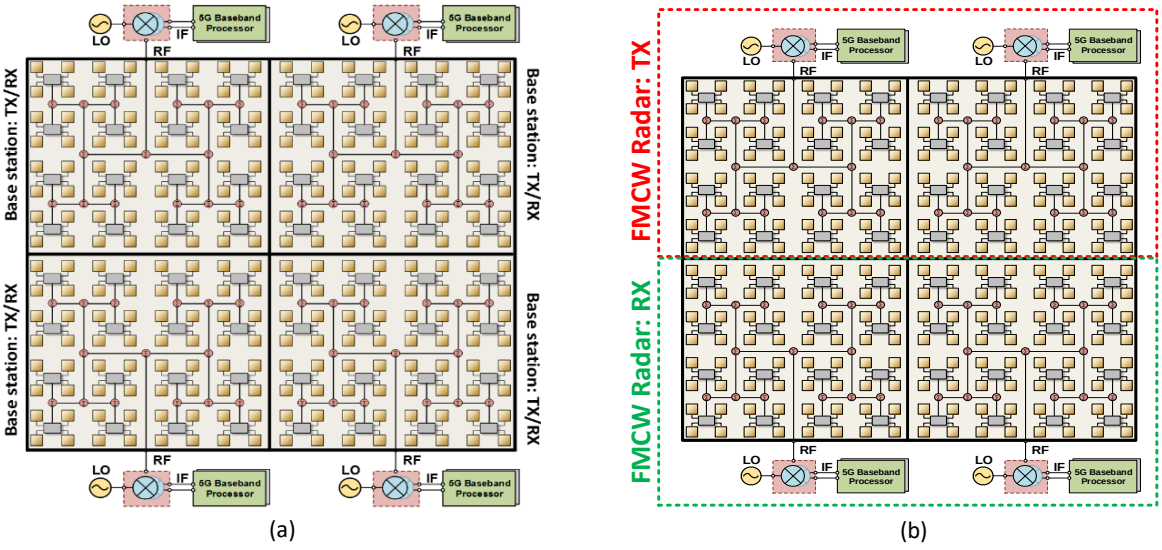

Figure 2.2: 2x64-elements phased-arrays used as a (a) 2x2 MIMO or (b) an FMCW radar system.

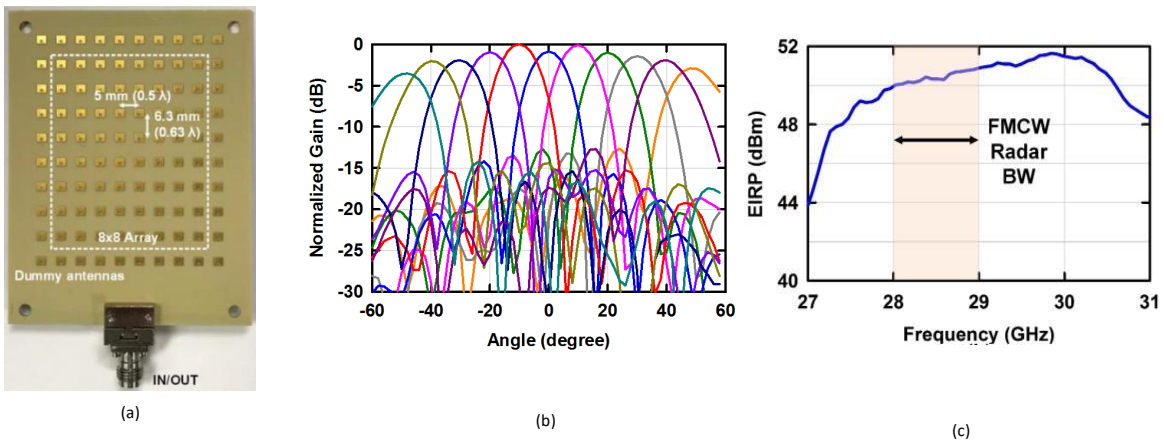

Figure 2.3: (a) 5G 64-element phased-array used in FMCW radar system. (b) Measured array EIRP at Psat. (c) Measured array patterns at scan angles from -50° to 50° in the azimuth plane.

impedance mis-match). In the Rx mode, the 5G array has a system noise figure of 6.5 dB up to the transceiver. An FMCW radar system operates by transmitting a signal that changes linearly in frequency over a frequency span $\triangle$f in a time interval T_b, as shown in Fig. 2.6. When the FMCW signal is scattered off a target and returns to the receiver, the target range (ie, travel time) translates to a difference frequency be-tween the transmitted and received signals (f_b), and can be found using a simple de-modulator (mixer) and an FFT func-tion at baseband. The FMCW radar system block diagram and equipment used are shown in Fig. 2.5. A frequency span ($\triangle$f) of 1 GHz and a pulse time (T_b) 10 μs was selected. The fast pulse time is chosen so that multiple FMCW radar measurements can be done in different beams within the 1 ms 5G timeframe, thus allowing for a wide scan volume. These values also set the unambiguous radar range (R_{max}) to 1.5 km as given by [2]:

$$R_{max} = \frac{cT_b}{2} \tag{2.1}$$

and a range resolution ($\triangle$R) of 0.15 m, as given by [2]:

$$\triangle R = \frac{c}{2 \triangle f} \tag{2.2}$$

The radar equation is used to calculate the received signal power as:

$$P_R = \frac{P_{Tx} G_{Tx} G_{Rx} \lambda^2 \sigma}{(4\pi)^3 R^4} \tag{2.3}$$

where λ is the free-space wavelength, R is the range between radar system and target, and σ is the radar target cross section. We approximated the UAV radar cross section as 0.05 m^2 (based on private communications with US National Labs).

For a range R=250 m at 28.5 GHz, the total loss, L is:

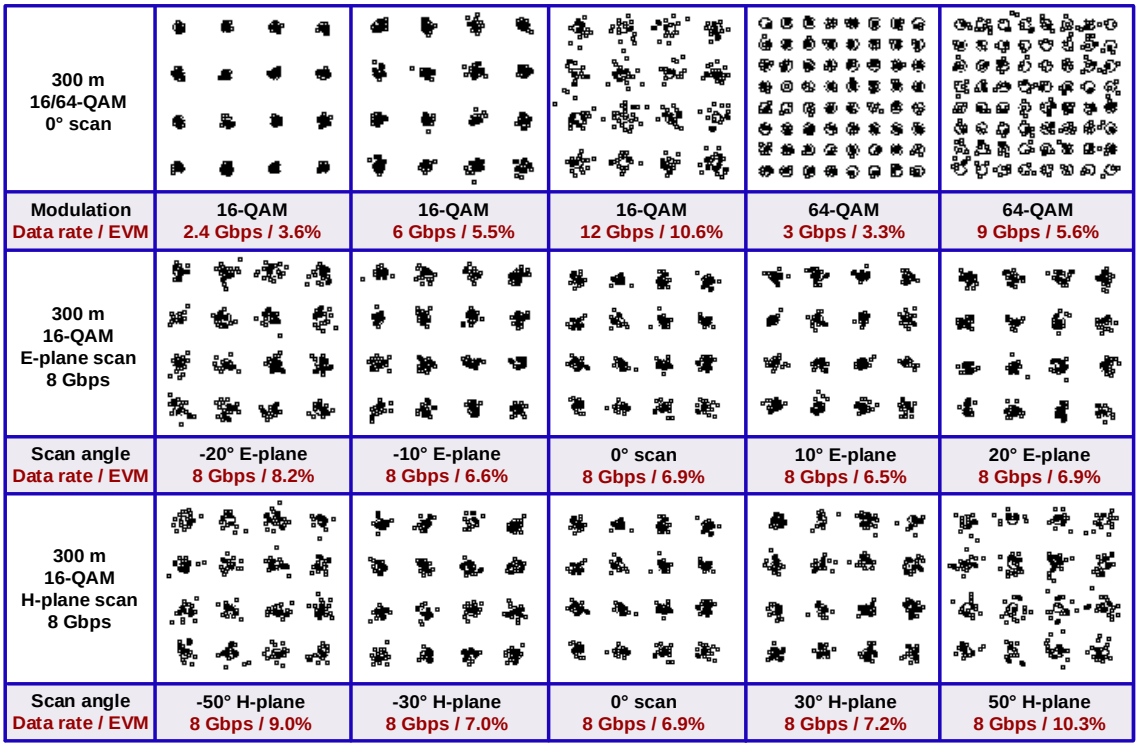

Figure 2.4: Data communication with this proposed arrays as the MIMO system.

$$L = 10log(\frac{\lambda^2\sigma}{(4\pi)^3R^4}) = -181.5\ dB \tag{2.4}$$

Based on 4.1, the received power at 250 m at the antenna aperture is:

$$P_{R\_250m} = P_{Tx} + G_{Tx} + L + G_{Rx} = -109\ dBm \tag{2.5}$$

where EIRP = $P_{Tx} + G_{Tx}$. The Tx chain is based on an arbitrary waveform generator which produces the linear frequency sweep at an IF of 4-5 GHz. It is upconverted to 28-29 GHz and amplified before being split to the transmit array (15 dBm) and to act as the LO for the Rx path. The power delivered to the phased-array is enough to operate the Tx mode phased-array with an EIRP of 50 dBm. In the Rx chain, the signal is first received by the phased array, then fed

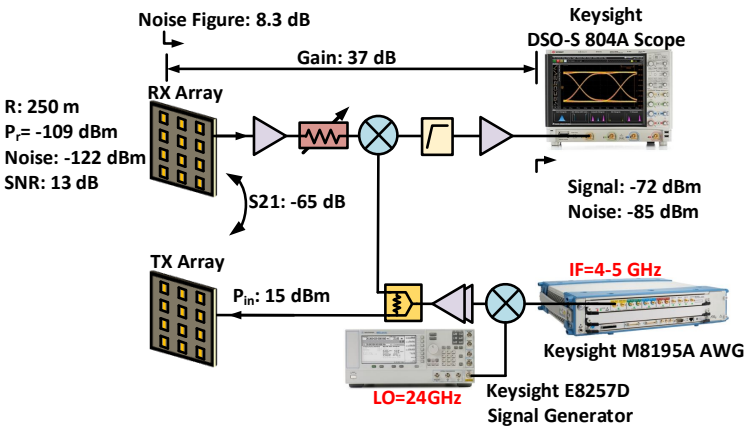

Figure 2.5: FMCW radar diagram and equipment used.

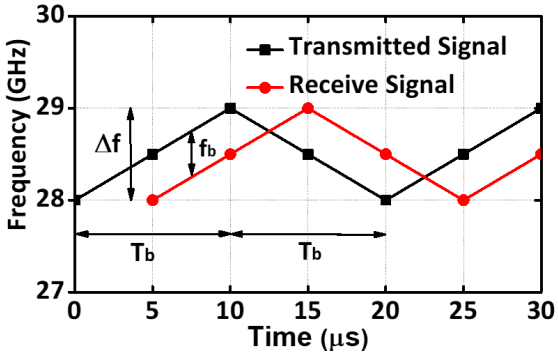

Figure 2.6: FMCW waveform example.

into an additional low noise amplifier to compensate for the cable and mixer loss. The received signal is mixed with the transmitted FMCW waveform and the resulting baseband signal is passed by a DC block and amplified at 0.05-500 MHz before entering the DSO scope. A limitation in long-range FMCW systems is the Tx to Rx isolation. In this case, an absorber is placed between the Tx and Rx phased-arrays, and the measured isolation (S_{21}) is 65 dB at 28-30 GHz (Fig. 2.7(b)). Therefore, the received leakage power is:

$$P_{R\_Leakage} = P_{In\_Tx} + S_{21} = -50\ dBm \tag{2.6}$$

and is 59 dB larger than the received radar signal for R = 250 m. An attenuator is therefore used in Fig. 2.5a before the mixer to ensure that the leakage power is less than -35 dBm. This is lower than the mixer IP_{1dB} and does not saturate the IF amplifier and DSO scope. At the DSO scope, the expected leakage power is:

$$P_{DSO\_Leakage} = P_{R\_Leakage} + G_{Rx} = -23\ dBm \tag{2.7}$$

where the gain of the Rx path (G_{Rx}) is 27 dB from the Rx array output port to the DSO scope input. The total gain including the phased-array electronic gain, and all other blocks shown in Fig. 2.5(a) is 37 dB. The total system noise figure is simulated to be 8.3 dB including the DSO scope NF (30 dB). The system noise is -122 dBm at the antenna for a baseband integration bandwidth of 20 kHz (equivalent to 5 FMCW ramps).

2.2.2 28 GHz RADAR MEASUREMENTS

To test the FMCW system, we assembled the radar in an open area to reduce the clutter, and used a DJI Phantom 3 as the UAV target (Fig. 2.8). The response of the FMCW radar when the drone is at different ranges is shown in Fig. 2.9. In Fig. 6d, we can clearly see a tone at 168 MHz, which corresponds to R = 252 m. The measured power at the DSO scope is -72.6 dB, which

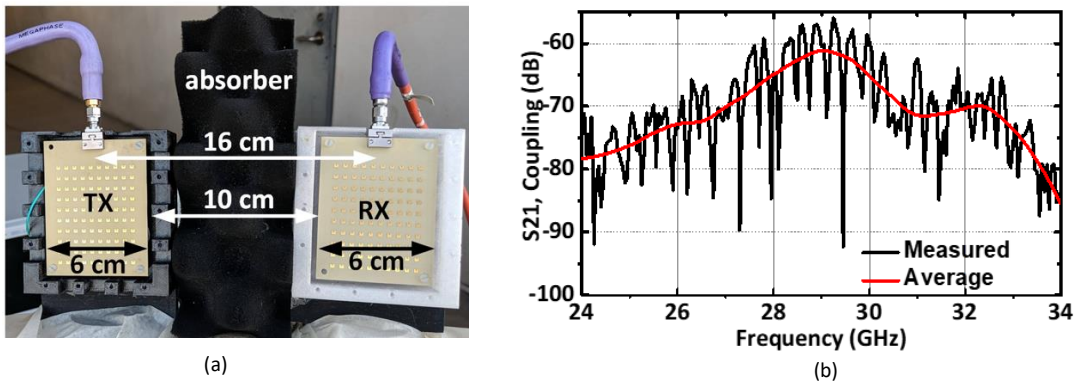

Figure 2.7: (a) Tx and Rx 5G arrays with middle absorber. (b) Measured cou-pling from the Tx to the Rx ports.

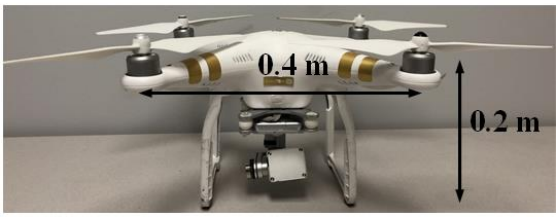

Figure 2.8: DJI Phantom 3 SE.

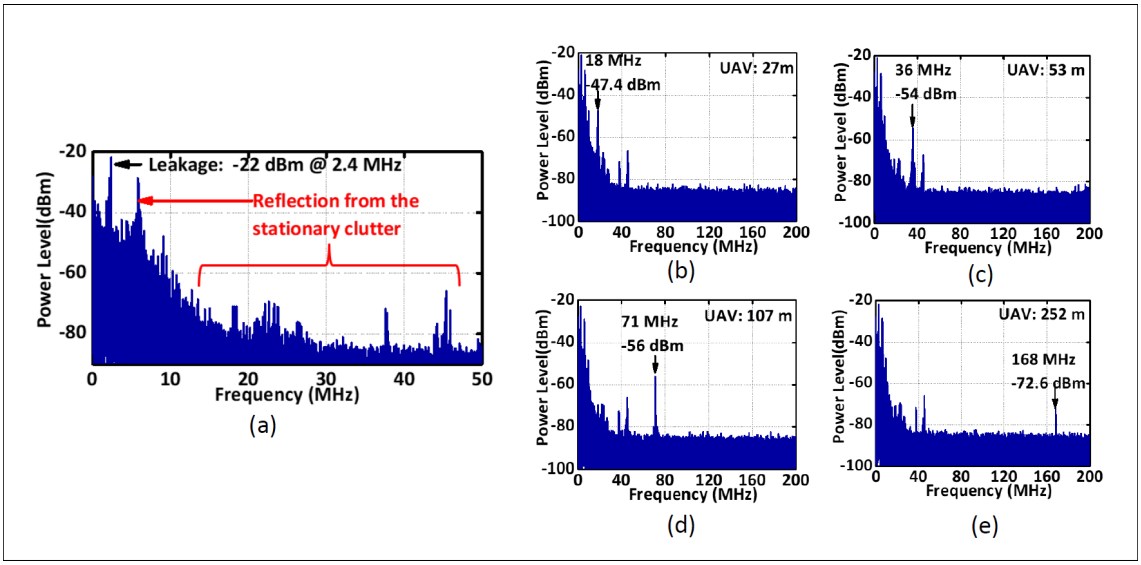

Figure 2.9: (a) Measured power spectrum density at close range;(b)-(e)Measured signals for target detection at different distances.

agrees well with simulations (-109 dBm +37 dB) and results in a SNR $>=$ 13.5 dB. Additionally, one can clearly see the Tx to Rx leakage with a received power of -22 dBm at 2.4 MHz (this is equivalent to 1.5 m of delay due to the cables between the Tx and Rx array and mixer). Any target at a range above 10 meters is above the leakage frequency and is easily detectable (Fig. 2.9a). The few spikes that remain constant in Fig. 2.9 are due to stationary clutter providing reflections, and can be removed using DSP and difference methods. Another important benefit of phased-arrays is that the narrow beam allows the radar system to track in angle as well as distance. The 3-dB beam-width of the 64-element 5G arrays is 12°. To demonstrate this, we hovered the drone in a single location at a range of 42 m and scanned the array from -15° to 15°. As shown in Fig. 2.10, the signal drops by 10 dB at 8° beam scan. This confirms that the 5G array provides the angular resolution as given by its antenna beamwidth.

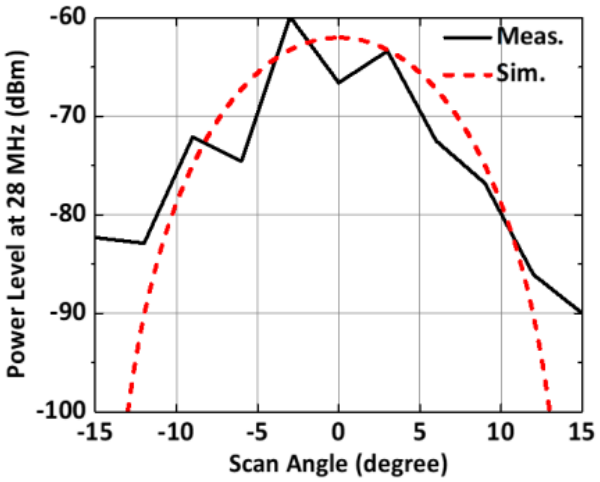

Figure 2.10: Power detected from a target at 42 meters vs phased-array scan angle.

2.3 64 GHz Phased-Arrays for 5G communication and UAV detection

2.3.1 64 GHz FMCW Radar Design

Millimeter-wave 5G base stations at 28 GHz and 60 GHz are planned to be widely used for Gbps communications. Benefited by the beam-forming technology, the 5G base stations provide a narrow and scannable beam due to the use of phased-array technology. This brings the possibility of using 5G base stations as FMCW radar systems without additional hardware, by using one panel as a Tx array alone and one panel as a Rx array alone. As a result, the 5G base stations can operate as a multi-function system, where for 97-98% of the working time, the base station is used for high data-rate communications and, for 2-3% of the time, it can operate as an FMCW radar to detect UAVs and automotive traffic. There are several advantages and disadvantages for 60 GHz 5G systems (as opposed to 28 GHz systems) when used for FMCW radars. A main advantage is the capability to synthesize very narrow beams (3-4° beamwidth)

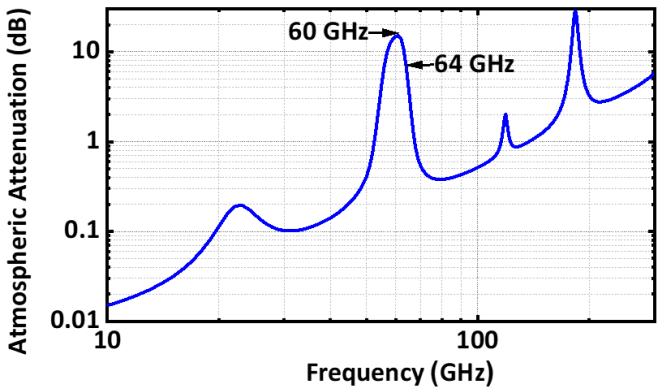

Figure 2.11: Atmospheric attenuation vs frequency.

using a physically small array, which improves target angular resolution. However, the main disadvantage is the atmospheric attenuation which is 5-15 dB/km at 58-64 GHz, and a 1 km radar range would incur 10-30 dB of additional propagation loss. Therefore, the 60 GHz base stations are most probably going to be used in the 100-300 meter radar detection range, which is enough for dense urban areas. Also, perhaps another advantage to using 60-64 GHz base-stations is that base-stations will have a low probability of interferences due to the high atmospheric attenuation. The center frequency of the proposed radar system is selected as 64 GHz, which has an atmospheric attenuation of 6 dB/km rather than 15 dB/km at 60 GHz (Fig. 2.11). This work shows that a small UAV with an RCS of 0.01 m^2 can be detected using a 5G phased array at up to 200 m with high signal-to-noise ratio.

2.3.2 64 GHz Phased-Array Antenna

The 64 GHz FMCW radar employs a 62.5-65.5 GHz 1-dimensional (1-D) phased array designed for 5G communications (Fig. 2.12(a)). The array is based on 32 channels with 0.54λ spacing at 64.5 GHz and each channel is composed of an eight-element series-fed microstrip patch array. The array spacing allows for a scan angle of ±50° without grating lobes in the

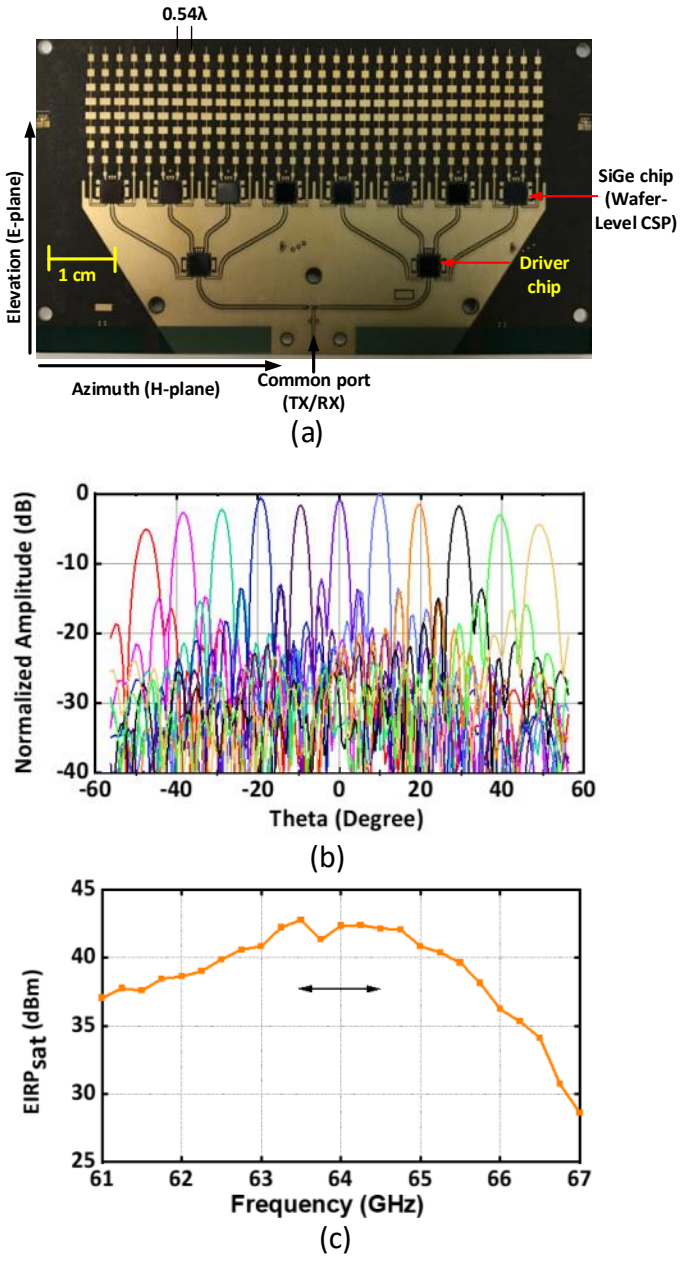

Figure 2.12: (a) 5G 32-channel phased array used in FMCW radar system. (b) Measured EIRP at Psat. (c) Measured array pattern at scan angle from -50° to 50° in the azimuth plane.

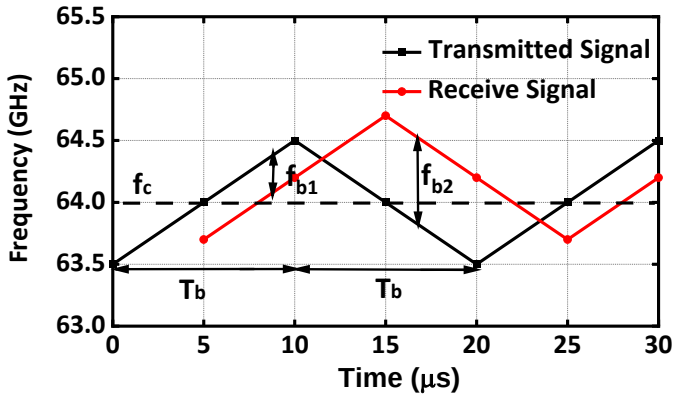

Figure 2.13: FMCW waveform: Transmitted and receive signals, with doppler effects.

azimuth plane, and the beamwidth is 2.9° at broadside and increases to 4.4° at the maximum scan angle. The antenna array size is 2.7 × 9.2 cm^2, providing an antenna gain $G_{Tx} = G_{Rx}$ = 29.4 dB (the antenna gain includes antenna loss and transmission line loss to the chips). In the Tx mode, the measured $EIRP_{sat}$ is 42-43 dBm at 64±0.5 GHz at broadside, and drops by 3-3.5 dB at 50° scan angles. In the Rx mode, the system noise figure is 7.6 dB and with an electronic gain of 23.5 dB [3]. The entire array consumes 7 W in the Tx mode and 4.5 W in the Rx mode. The 32-element phased-array has been used in 2 Gbps communication links at 300 meters, and was also able to achieve 250 Mbps links at 800 meters, over all scan angles. These are detailed in [4].

2.3.3 64 GHz FMCW Radar System Performance

In an FMCW radar system, the transmitted signal has a linear-variation with frequency, with a frequency span △f in a time interval T_b. The reflected signal from the target is detected by the Rx phased array and mixed with the transmitted signal. The beat frequency f_b between the transmitted and received signals is proportional with the target distance (R) and equal to the round-trip delay multiplied with frequency sweep rate. The simulated performance of a 64 GHz radar system is summarized in Table 2.1. With a frequency span (△f) of 1 GHz and a pulse time (T_b) of 10 μs, the unambiguous radar range (R_{max}) is 1.5 km:

Table 2.1: Power detected from a target at 42 meters vs phased-array scan angle.

EIRP	41-42 dBm
$G_{Tx\_Attenna}$	29.4 dB
$G_{Rx\_Attenna}$	29.4 dB
NF_{system}	10 dB
Δf (or Range Resolution)	1 GHz (15 cm)
T_b (or Unamb. Range)	10 µs (1.5 kms)
σ	0.01 m^2
Atmospheric attenuation at 64 GHz	6 dB/km
Integration Time	1 ms
Doppler Resolution	2.3 m/s
SNR at 100 meters	23.7 dB
SNR at 200 meters	10.4 dB
SNR at 300 meters	2.2 dB

$$R_{max} = \frac{cT_b}{2} \tag{2.8}$$

and the range resolution ($\triangle$R) is 0.15 m, as given by:

$$\triangle R = \frac{c}{2 \triangle f} \tag{2.9}$$

If the target is moving, due to doppler effect, the received signal will show a frequency offset (Fig. 2.13). The two beating frequency f_{b1} and f_{b2} can be used to calculate the target distance (R) and the velocity (v_{target}) by:

$$f_b = \frac{2R}{c} \times \frac{\triangle f}{T_b} \tag{2.10}$$

$$f_D = \frac{2v_{target}}{\lambda} \tag{2.11}$$

$$f_{b1} = f_b - f_D \tag{2.12}$$

$$f_{b2} = f_b + f_D \tag{2.13}$$

The doppler resolution ($\triangle\ v_{target}$) of this system is given by:

$$\triangle\ v_{target} = \frac{c}{2f_c \times T_b \times N} = 2.3\ m/s \tag{2.14}$$

where N is the number of ramp functions in resolution period (N=100 for the calculation above, resulting in an integration time of 1ms). Assuming a target distance of 110 m and a radar cross section (σ) of around 0.01 m^2 (based on private communications with US National Labs), the space loss factor is calculated as:

$$L = 10log(\frac{\lambda^2\sigma}{(4\pi)^3R^4}) = -181\ dB \tag{2.15}$$

The received signal is calculated as [5]:

$$P_{scope\_110m} = P_{Tx} + G_{Tx\_antenna} + L + L_{atm\_loss} + G_{Rx\_antenna} + G_{Rx\_path} = -71\ dBm \tag{2.16}$$

where EIRP=$P_{Tx} + G_{Tx\_anttena}$, L_{atm_loss} is the atmospheric loss (at 6 dB/km$\times$2R). $G_{Rx\_anttena}$ is the Rx antenna gain (29.4 dB) and G_{Rx_path} (40.5 dB) is the electronic gain from the antenna port to the IF port. The measured noise at the IF receiver is calculated as:

$$P_{Noise\_Scope} = 10log(KTF \times \frac{1}{IntegrationTime}) + G_{Rx\_path} = -93.5\ dBm/Hz \tag{2.17}$$

where F = 10 dB and is the receiver noise figure referenced to the antenna port, and a 1 ms of integration time is used. This means that an SNR of 22 dB is available at 110 m range. Fig. 2.16 presents the simulated FMCW radar system SNR versus target distance. The system

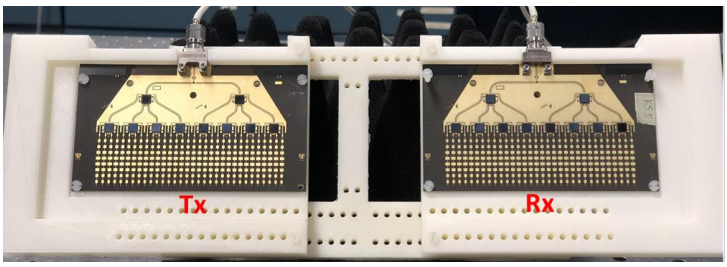

Figure 2.14: Tx and Rx arrays used in FMCW radar system.

simulations show that this simple radar system, based on commercial 5G phased-arrays with 42 dBm EIRP, can detect a UAV at over 200 m with a SNR >10 dB. If operation at 60 GHz is desired, the detection range drops from 210 m to 180 m due to the added atmospheric loss. Note that Fig. 2.16 presents simulations at normal incidence and the range will drop to $0.7R_{max}$ at 50° scan angles due to the drop-in antenna gain by 3-dB in the Tx and Rx modes. However, one can increase the integration time to 4-5 ms at the wide scan angles to compensate for the signal loss. In general, a detection range of 200 m is achievable with such arrays over all scan angles. The 64 GHz radar results in a beamwidth of 2° at broadside ($G_{Tx} \times G_{Rx}$) and 3.1° at 50° scan angle, and can locate a target within a very narrow angular resolution without multi-phase signal processing. This means that the entire 1-D space can be covered in 50 beam-steps, each with an average of 2 ms integration time, and the entire search can be completed in 100 ms. The 12° beamwidth in the elevation plane is enough to cover a 42 m vertical height at 200 m, and $\pm$ 4° of additional scanning in the elevation plane can be obtained using a different center frequency (63 or 65 GHz instead of 64 GHz). This is possible due to the traveling-wave nature of the series-fed 8-element microstrip antenna array.

2.3.4 Hardware Implementation

The 64 GHz radar is designed using a UCSD up and down-converter mixer (Fig. 2.15). In the Tx mode, the up-converter mixer contains an embedded doubler and an LO of 29.75 GHz

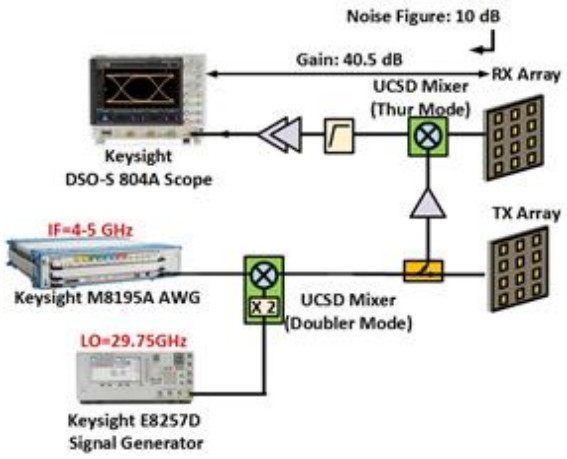

Figure 2.15: FMCW radar system and equipment used.

is used. The IF is obtained using a high-speed Keysight M8195A arbitrary wave generator and is swept from 4-5 GHz. This results in an FMCW waveform at 63.5-64.5 GHz, and an image at 54.5-55.5 GHz (which is not radiated by the array, or even passed by the E-band amplifier). The LO leakage at 59.5 GHz is optimized to be -45 dBm, and has no effect on the system. The upconverted signal is passed by a 10 dB coupler and a drive amplifier to act as the LO for the Rx array. The FMCW radar is a standard IF-based system based on Keysight equipment for experimental demonstration. In actual systems, the transmit and receive chains can be replaced by commercial transceivers from Infineon or ADI [6].

2.3.5 64 GHz FMCW Radar Measurement

To test this 64 GHz FMCW radar system, a UAV detection experiment was performed in open area to reduce clutters. The target is selected as DJI Phantom 3. A short ramp rate of 10 µs is used to push the IF high in frequency and make it easy to use with the equipment (a ramp rate of 100-200 µs could also be used, but the IF would be at 3.5-7 MHz). When the distance between

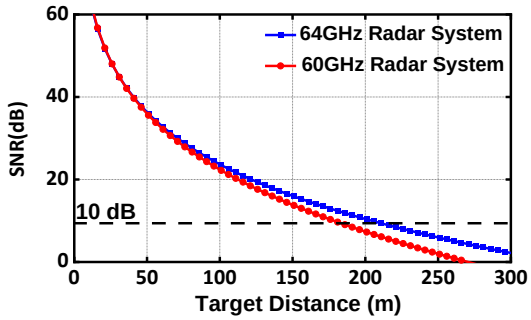

Figure 2.16: Calculated SNR vs. target distance (see Table I for system details).

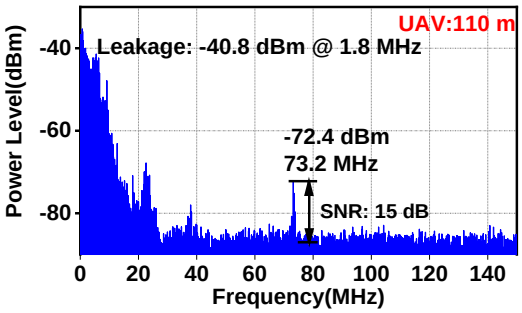

Figure 2.17: Measured signal for UAV detection at a range of 110 m.

the target and radar system is 110 m, a received IF signal can be clearly seen at 79 MHz with -72.4 dBm of power, matching very well with the simulated power level. The measured noise floor is -88 dBm/Hz, which is higher than calculated value of -93.5 dBm/Hz (assuming 10 dB Rx system noise figure) due to the noise from the DSO scope. The measured SNR is greater than 15 dB at R=110 m. Note that there is a direct leakage path from the transmit array to the receive array which shows up at a very close IF (1.8 MHz). However, this is handled by the receive chain with no saturation and shows up at the DSO scope at -41 dBm. The other signals are clutters from the building edges (the setup was on a building on the 6th floor next to large walls). Still, the 110 m UAV signal is clearly seen at 73.2 MHz and proves that 5G phased arrays can be used for UAV detection.

2.4 Conclusion

A long-distance and high-resolution FMCW radar system has been achieved using 28 GHz and 60 GHz 5G phased-arrays. As shown in the measurements, the 5G based radar system can detect a small UAV at a range greater than 250 m and 110 m distance, respectively. This shows the potential of 5G base stations for UAV detection and automotive traffic-monitoring.

2.5 Acknowledgment

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Chapter 2, in part, is a reprint of the material as it appears in: H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A packaged 0.01−26 GHz single-chip SiGe reflectometer for two-port vector network analyzers", *IEEE International Microwave Symposium (IMS)*, June, HI, 2017, pp. 1259-1261. The dissertation author was the primary investigator and author of this paper.

Chapter 2 is also, in full, has been submitted for publication of the material as it may appear in: H. Chung, Q. Ma, M. Sayginer, and G. M. Rebeiz, "A packaged 0.01−26 GHz single-chip SiGe reflectometer for two-port vector network analyzers", *IEEE Trans. Microw. Theory Techn.*, submitted. The dissertation author was the primary investigator and author of this paper.

Chapter 3

A 57.5-65.5 GHz Phased-Array Transmit Beamformer in 45 nm CMOS SOI with 5 dBm and 6.1% Linear PAE for 400 MBaud 64-QAM Waveforms

3.1 Introduction

Due to the growing amount of data usage in high-definition video and virtual reality applications, the 60 GHz frequency band has received a lot of interest in the past few years with the WiGig IEEE 802.11ad standard, as reported in [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19]. The primary advantage of 60 GHz is the capability to synthesize narrow beams (3-6° beamwidths) using a physically small array [7], [8], which significantly improves the antenna gain and reduces interference from adjacent cells for small-scale communication equipment. However, due to high path-loss and atmospheric attenuation in the ISM band (57-64 GHz), a large array (256 elements in [9]) and high output power in [10] are needed to realize

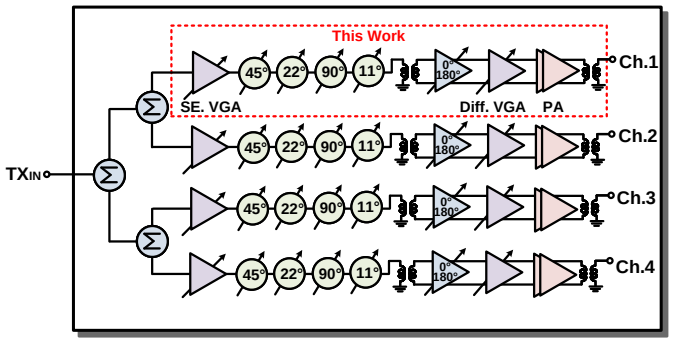

Figure 3.1: Block diagram of a 60 GHz 4-channel phased-array beamformer chip.

a high EIRP and long-distance links. This inevitably leads to the issues of power consumption and heat dissipation [8]. Therefore, building a high-linearity transmit channel with low power consumption is an important precondition for the widespread adoption of 60 GHz communication links.

In this paper, a high linearity and low DC power transmit (Tx) beamformer chip is demonstrated using the 45 nm RFSOI process (Fig. 5.1). The channel is designed using both active and passive phase shifters and considers the trade off between power and insertion loss. A cascode power amplifier with neutralization is designed for improved linearity and efficiency. Optimization of the system structure and related circuits have resulted in a high linearity and low DC power Tx beamformer chip with state-of-the-art performance.

3.2 Phased Array Tx Channel Design

3.2.1 Technology

The phased-array Tx beamformer chip is designed in the GlobalFoundries 45-nm RFSOI process with thick metals (LD=4.1 μm, OB=3 μm, OA=3 μm), and leads to a high inductor Q with simulated values of 30-35 at 60 GHz (Fig. 5.2(a)). The NFET provides an NF_{min} of 0.8 dB at 60 GHz and an associated f_T of 180-200 GHz (referenced to the top metal) at a bias current

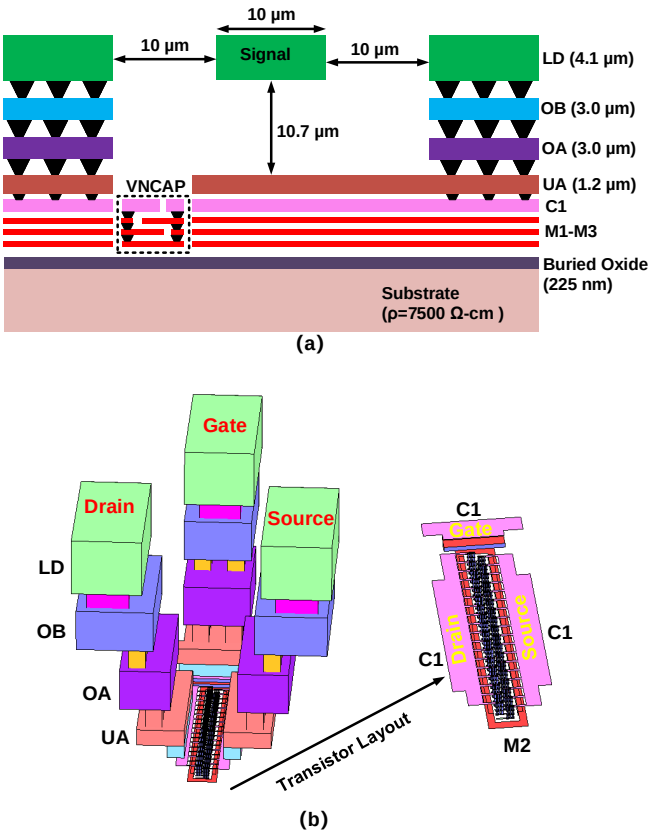

Figure 3.2: (a) Cross section of GlobalFoundries 45 nm CMOS RFSOI metal back-end; (b) layout of a W=20×1 μm transistor up to LD and C1.

of 0.15–0.2 mA/μm. A double-gate contact is employed to reduce the gate resistance and a relaxed pitch layout is chosen to reduce the parasitic capacitance (Fig. 5.2(b)) [20]. The coplanar waveguide (CPW) 50 Ω transmission line with a signal line width of 10 μm and a gap of 10 μm has measured loss of 0.8 dB/mm at 60 GHz [18].

3.2.2 Variable Gain Amplifier Design

The transmit channel consists of a single-ended VGA with a maximum gain of 7 dB and a NF of 6 dB, and a 1-bit gain control of 7 dB (Fig. 5.1 and Fig. 3.3(a)). This is followed by a 4-bit phase shifter all in single-ended mode and is done to reduce the area on the chip. The single-ended VGA reduces the transmit system noise figure and eases the differential gain lineup

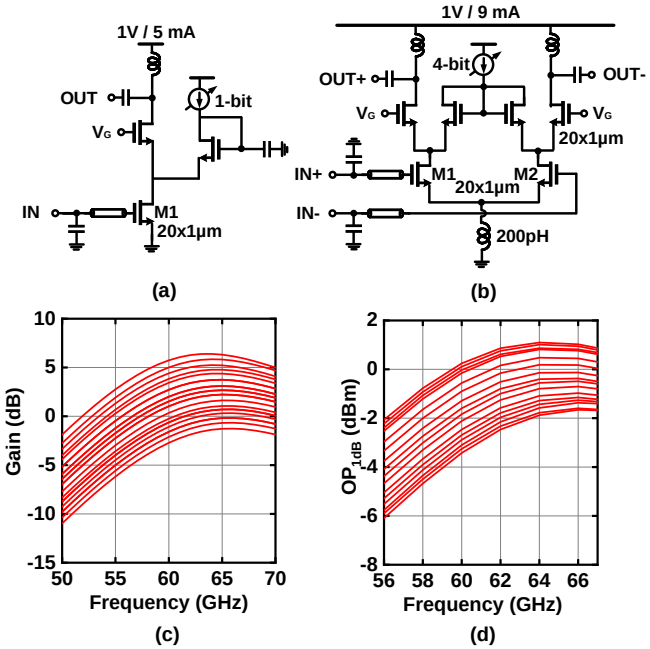

Figure 3.3: Schematic of (a) single-ended VGA and (b) differential VGA; (c) simulated gain and (d) simulated OP_1dB for the differential VGA.

after the balun. The differential VGA has a maximum gain of 7 dB and 4-bit of gain control with 0.5-dB steps (Fig. 3.3(b),(c)). A tail inductor (j75Ω @60 GHz) is used to provide >10 dB common-mode rejection (CMRR) as [18]. The VGA input impedance varies a bit with gain control, and the phase response of the passive phase shifter is sensitive to its load impedance. Therefore, a 0/180° active phase shifter is used between the passive phase shifter cells and the VGA, and provides a near-constant impedance for both phase states (see Fig. 5.1 for block line-up). The VGA also acts as a driver to the PA, and this poses an issue with current steering. Note that current steering results in VGA OP_{1dB} reduction versus gain drop (Fig. 3.3(d)) [21]. Therefore, the VGA and PA lineup are co-designed so that the VGA can still drive the PA even if set at its low gain states (OP_{1dB} of -2 to -3 dBm).

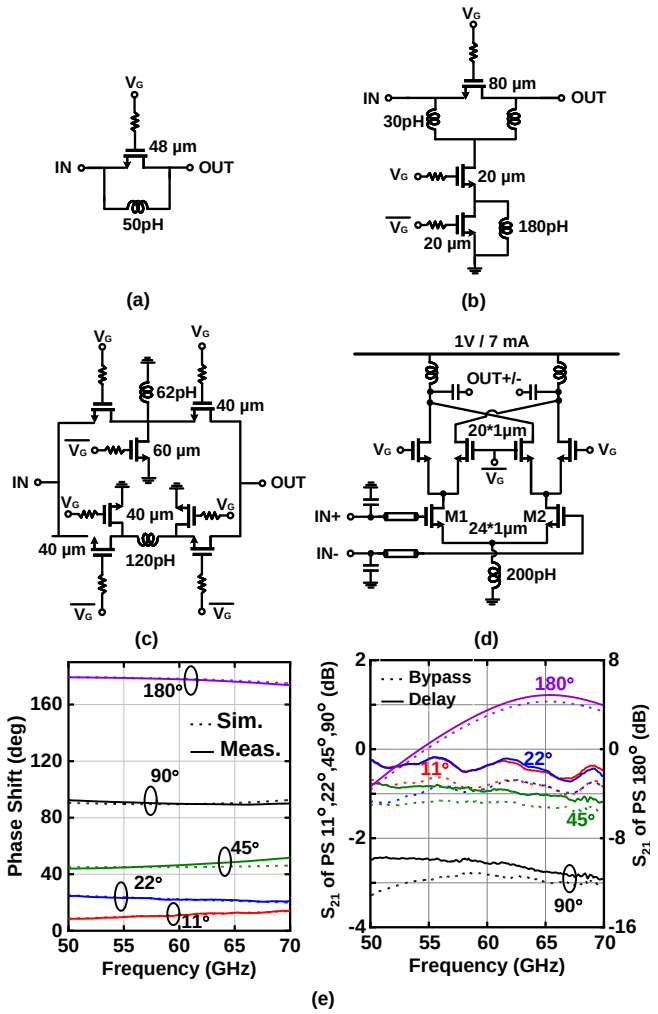

Figure 3.4: (a) 11° phase shifter; (b) 22°/45° phase shifter; (c) 90° phase shifter; (d) active 180° phase shifter; (e) measured phase shifts and S_{21} of the 11°, 22°, 45°, 90° and 180° phase shifters.

3.2.3 Phase Shifter Design

The 11°, 22°, 45° and 90° cells are passive phase shifters are designed and consume ~ 0 mW. The 180° cell is an active phase shifter and compensates the insertion loss of the passive topology. A passive balun (1 dB loss) is used between the single-ended cells and the differential cells.

Fig. 3.4(a) presents the 11° phase shifters which consists of a series switch with a parallel inductor [], [**?**]. The phase shift occurs when the transistor is off and its source and drain

capacitance become a CLC impedance-matched phase-shifting circuit. The measured insertion loss is 0.4 and 0.9 dB in the bypass and phase-delay state at 60 GHz and S_{nn} <-20 dB. Fig. 3.4(b) presents the 22° and 45° phase shifters which are based on switched LC-networks [**?**], [**?**]. The additional shunt transistor with 20 μm device provides a constant phase shifter over a wide frequency to minimize the RMS phase error [**?**]. The measured average insertion loss is ∼0.7 and ∼1 dB for the 22° and 45° cells at 60 GHz, respectively. The 90° phase shifter is based on a switched low-pass/high-pass circuit (Fig. 3.4(c)) [**?**]. Note that there are no stand-alone capacitors in the circuit, as these are present when the transitors are switched off. The SPDT switches are series-shunt designs for high isolation and the cell results in ∼2.6 dB insertion loss. All passive phase shifters are optimized to have a low variation in their loss (±0.3 dB) between the bypass-state and the phase-delay state so as to ensure a low RMS gain error. The simulated output P_{1dB} of these passive phase shifter is >10 dBm at 60 GHz and does not limit the system linearity.

The active 180° phase shifter provides 3-5 dB gain, with a measured amplitude and phase imbalance of < 0.6 dB and 5°, respectively (Fig. 3.4(d)). The measured active phase shifter OP_{1dB} is -2 dBm at 60 GHz and also does not affect the system linearity. The measured phase shifts and insertion loss versus frequency for the individual cells are shown in Fig. 3.4(e). Excellent agreement between simulations and measurements is achieved due to the full electromagnetic analysis of the inductors and transistor connections using ANSYS HFSS. The complete phase-shifter, with the active and passive components, is nearly gain-neutral having an aggregate gain of -2 dB to -0.5 dB at 60-65 GHz including the balun loss, and consumes only 7 mW of DC power.

3.2.4 Power Amplifier With Neutralization

The power amplifier is based on a two-stage differential cascode topology (Fig. 3.5(a)). In the first stage, the transistors are biased in class-A to achieve high power gain, and a 1 V supply is used for high efficiency. A tail inductor provides >10 dB of common-mode rejection and lowers

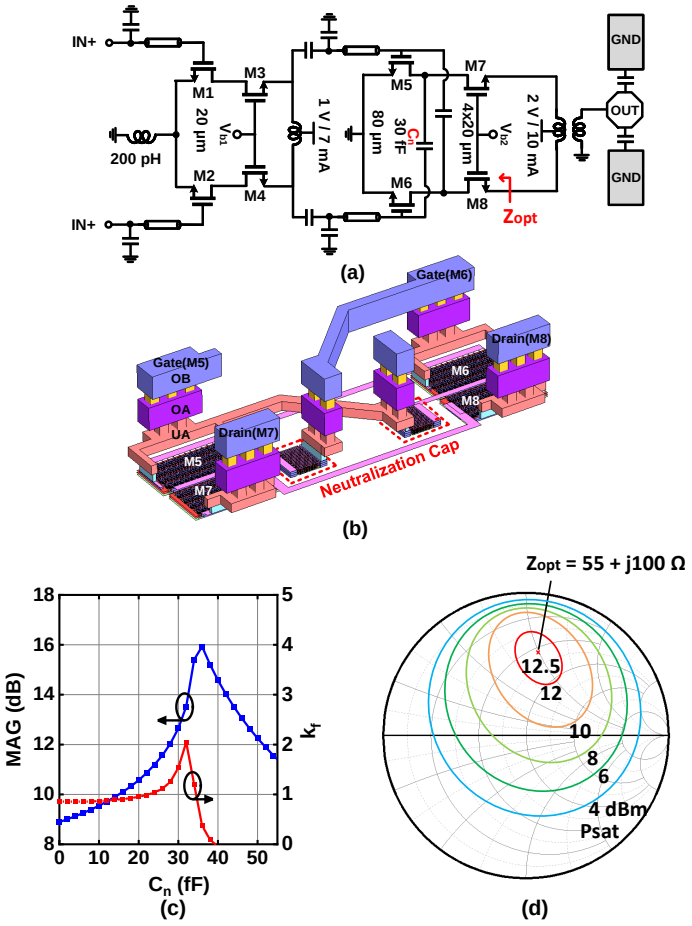

Figure 3.5: (a) Schematic of two-stage cascode power amplifier with neutralization; (b) 3D view of neutralization capacitor layout; (c) MAG and k_f of cascode differential pair versus C_n at 60 GHz and (d) simulated load-pull of the second stage for C_n=30 fF (Smith chart Zo=100 Ω); (e) V_{DS} for M5 and M7 at 60 GHz at OP_{1dB}; (f) layout of transformer-balun, co-simulated with the output GSG pad.

the risk of common-mode oscillation in the PA.

The second stage uses a 2 V supply voltage with the transistors biased in class-AB for high output power and efficiency. However, class-AB designs result in low gain, and this necessitates a higher power from previous stages, and intensifies the design challenges on the first stage with a 1 V supply voltage. Therefore, the common source transistors are neutralized by equivalent negative capacitances (C_n) to lower the effective gate-to-drain capacitance (C_{gd}). As is well know, C_{gd} limits the power gain and leads to poor reverse isolation. The neutralization technique is implemented by cross-connecting two capacitors C_n between the drain and gate terminal of the

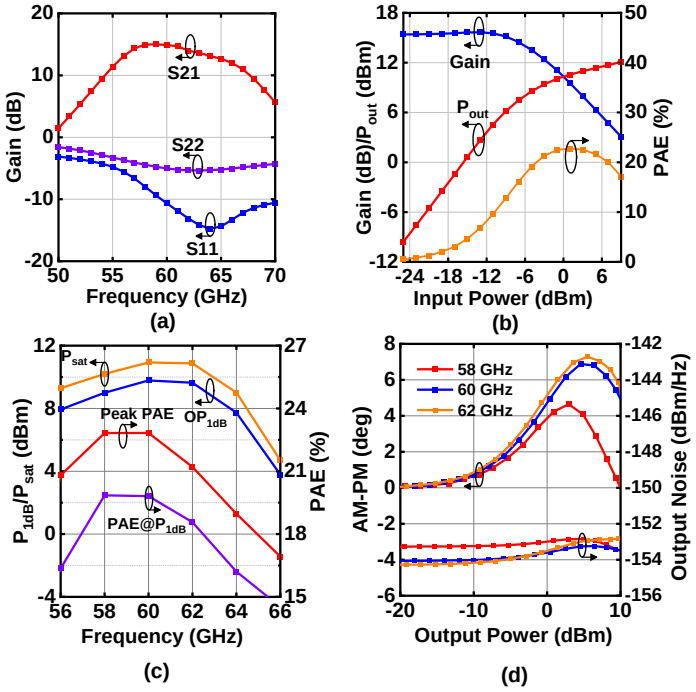

Figure 3.6: (a) Simulated S-parameters for the two-stage PA; (b) simulated gain, output power and PAE versus input power at 60 GHz; (c) simulated P_{1dB}, P_{sat} and PAE versus frequency; (d) AM-PM versus input power.

differential stage (Fig. 3.5(b)) [**?**]. The maximum available gain and stability at 60 GHz for the cascode stage with neutralization is shown in Fig. 3.5(c). The maximum MAG of 16 dB is achieved when Cn is 36 fF, however, kf is nearly equal to 1, which is marginal for stability. Therefore, a C_n of 30 fF is used to take into account any process variation ($\pm$ 20%).

The entire cascode structure in Fig. 3.5(b) is simulated using Integrand Software EMX and takes into account the capacitance and the inductive connections between the transistors. A load-pull analysis is also done at the drain nodes of M7/M8 and a P_{sat} of 12.5 dBm is achieved at an optimal load impedance of Z_{opt}=55+j100 Ω at 60 GHz and a PAE of 28% for an ideal matching network (Fig. 3.5(d)). The V_{DS} waveforms for M5 and M7 are presented in Fig. 3.5(e) and are lower than the break-down voltage of the 45RFSOI transistors. The output matching network is then co-designed with the transformer-balun and GSG pad capacitance and no extra matching network is required (Fig. 3.5(f)). The balun has a k=0.7 at 60 GHz and is designed

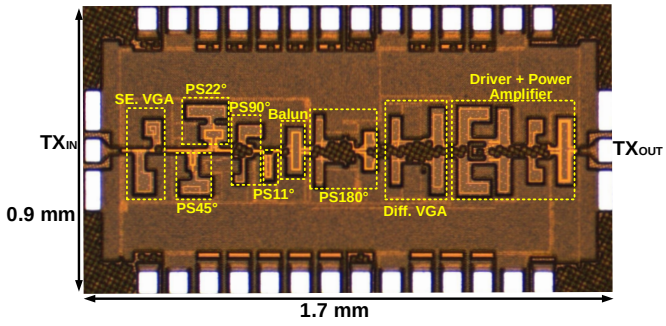

Figure 3.7: Microphotograph of the 60 GHz Tx channel chip in 45nm CMOS SOI.

using the OA and OB thick-metal layers and introduces 0.8-1 dB loss at 56-66 GHz, but provides an equivalent shunt inductance which is used for output matching, and an additional 20 dB of CMRR thus improving stability when packaged [**?**].

The two-stage PA results in a simulated power gain $>$ 15 dB with a 3-dB bandwidth of 56-65 GHz and a NF of 5 dB at 57-65 GHz. Fig. 3.6(b) presents the simulated gain, output power and PAE at 60 GHz. The PAE at P_{1dB} is 20% and the peak PAE is 22%, including the balun loss. The PA maintains high output power and efficiency at 57-64 GHz, with a mimimum OP_{1dB} of 9 dBm and a PAE of 17% (Fig. 3.6(c)). A gain expansion of $<$ 0.5 dB is present due to the self bias of the class-AB amplifier, with an AM-PM response of $<$ 7° and output noise power of $<$ -153 dBm/Hz at OP_{1dB} (Fig. 3.6(d)). Note that the current from the 2 V supply increases from 10 mA at small-signal to 20 mA at P_{1dB}. The IP_{1dB} is always less than -4 dBm and the PA can be driven by the VGA, even under mid-gain states. This will be shown in the measurement section.

The entire channel, shown in Fig. 1, has a simulated gain of 23.5 dB at 60 GHz with a 3-dB bandwidth of 57-65 GHz and an IP_{1dB} of -15.5 to -11 dBm. Two power supplies are used, 1 V for all stages and phase shifters and 2 V for the last stage, resulting in a channel PAE of 15-19 % at 60 GHz, for P_{1dB} to P_{sat} operation. The simulated NF is 7.5 dB at 60 GHz, and the output noise is -143 dBm/Hz at P_{1dB}. For a 1 GHz bandwidth and an output power of 5 dBm (backoff of 5 dB from P_{1dB}), the transmit SNR is 58 dB, which is the highest known to-date.

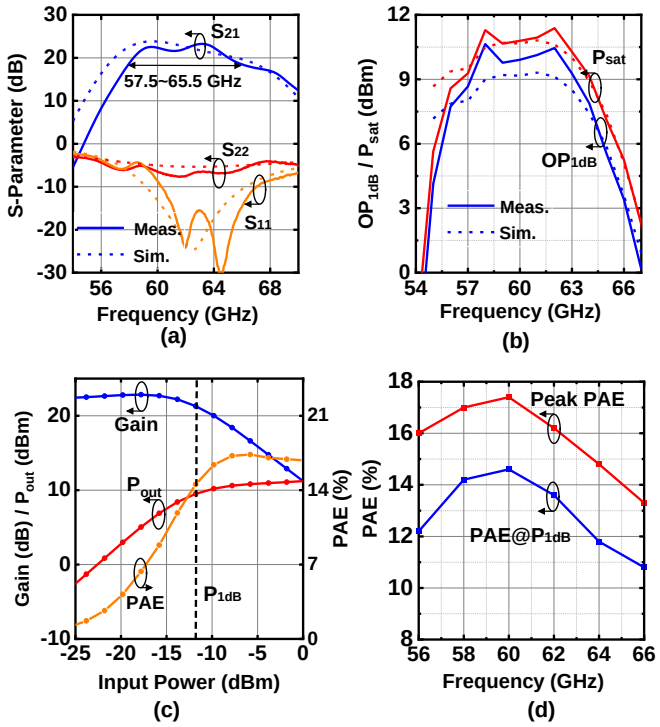

Figure 3.8: Measured (a) S-parameters; (b) OP_{1dB} and P_{sat}; (c) gain, output power and PAE at 60 GHz and (d) PAE at P_{1dB} and peak PAE at max gain state.

3.3 Tx Channel Chip Measurements

Fig. 5.14 presents a microphotograph of the transmit channel with a chip area of 0.9 mm $\times$ 1.7 mm, and an active area of 0.35 $\times$ 1.45 mm. Note the ground plane used around the single-ended VGA and phase shifter to reduce any ground plane inductance. All measurements are performed using GSG probes and a Keysight N5247B network analyzer (PNA-X), which calibrates the cable loss up to the probe tips. The chip consumes 48 mW in the small-signal regime, and 67 mW at P_{1dB}.

Fig. 3.8(a) presents the measured and simulated S-parameters. The measured gain is $>$ 19 dB at 57.5-65.5 GHz with a peak of 22 dB at 63 GHz. The measured S_{11} is $<$ -9 dB at 59-67 GHz and S_{12} is $<$ -60 dB over the entire band. The OP_{1dB} is $>$ 9 dBm at 57-63 GHz and P_{sat} is $>$ 10.5 dBm (Fig. 3.8(b)). Removing the 0.5-1 dB peaks at 58 GHz and 62 GHz which could be

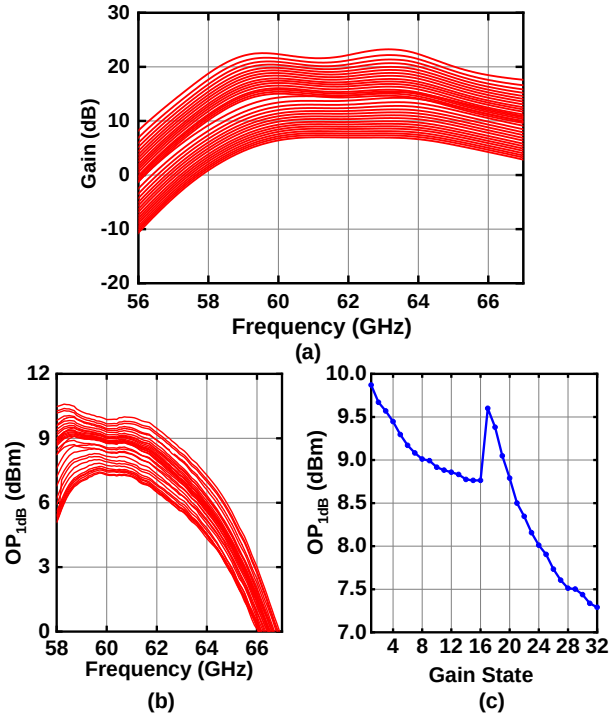

Figure 3.9: Measured 5-bit gain control with (a) channel gain; (b) OP_{1dB}; (c) OP_{1dB} at 60 GHz versus gain state over 14 dB gain control.

due to standing waves in the measurement setup or power-detector calibration, the peak OP_{1dB} at P_{sat} occur at 60-62 GHz and are 10 dBm and 11.5 dBm, respectively, with a corresponding PAE of 14.6% and 17.6%.

The measured channel gain versus 5-bit control results in 14-dB range with 0.5 dB gain steps, < 0.8 dB maximum gain step, and a phase variation of $< \pm 6°$ over the gain control range at 58-65 GHz (Fig. 9(a)). Gain state 16 is realized with the lowest gain of the differential VGA and the high-gain mode of the single-ended VGA. However, gain state 17 is achieved with the highest gain of the differential VGA and the low-gain mode of the single-ended VGA. The differential VGA can deliver more power to the PA, which causes the variation in OP_{1dB} between these two adjacent gain states. The OP_{1dB} is $>$4 dBm at 58-64 GHz, even with 14 dB of gain control (Fig. 9(b)). In particular, for the first 21 gain states with 10 dB gain control, the OP_{1dB} can be kept $>$ 8.5 dBm at 60 GHz (Fig. 3.9(c)). This is important for calibration in large phased-arrays where

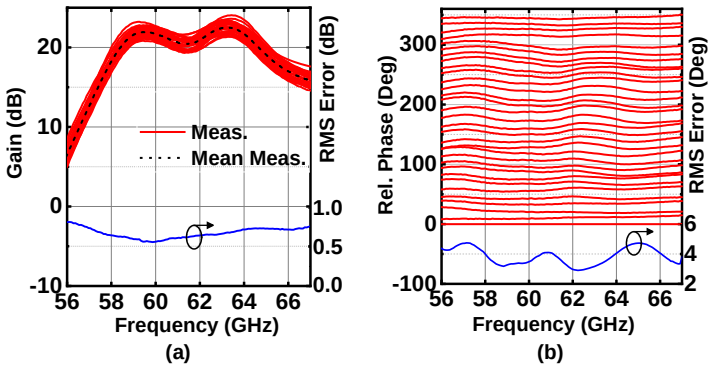

Figure 3.10: Measured 5-bit phase shifters with (a) gain and RMS gain error; (b) normalized phase and RMS phase error.

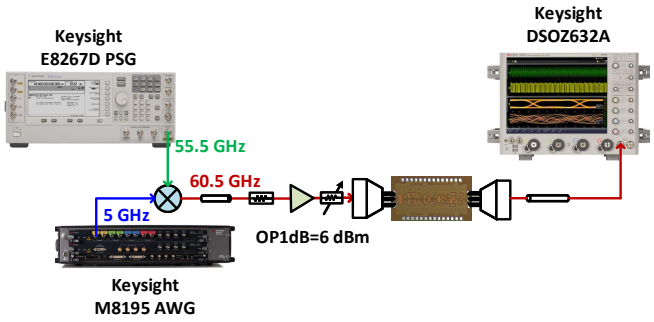

Figure 3.11: Setup for complex modulation and EVM measurements at a center frequency of 60.5 GHz.

3-4 dB from the VGA range may be used to equalize the difference between the channels.

The 5-bit phase shifter response is shown in Fig. 3.10, with a gain variation of ±1 dB at 57-65 GHz, resulting in an RMS gain error of 0.7 dB (Fig. 3.10(a)). The measured RMS phase error is 4-5° at 56-67 GHz (Fig. 3.10(b)).

3.4 EVM Measurements

Complex modulation measurements are performed on the 60 GHz phased-array Tx beamformer chip with the setup shown in Fig. 3.11. A Kesight M8195 arbitrary waveform generator (AWG) is used to generate 16-QAM and 64-QAM waveforms with an IF centered

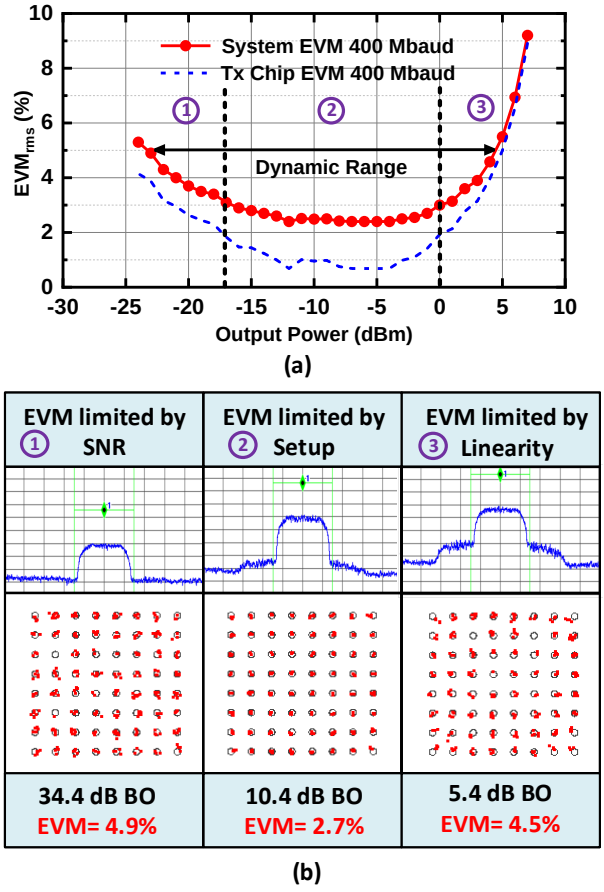

Figure 3.12: Measured (a) EVM versus output power at 60.5 GHz with a 400 MBaud 64-QAM waveform; and (b) power spectrum and constellations at different EIRP levels.

at 5 GHz. The modulated IF signal is upconverted to 60.5 GHz using a 60 GHz passive mixer (LO is set at 55.5 GHz). A 60 GHz amplifier and a variable attenuator are employed for power control used after the passive mixer. The 60 GHz amplifier also filters out the lower-sideband at 50.5 GHz by more than 25 dB. On the receive side, a Keysight DSOZ632A 63 GHz real-time oscilloscope is employed to demodulate the signal using the Keysight Vector Signal Analysis software (VSA-89600). The DSO has excellent sensitivity at 60 GHz even at -40 dBm and a pre-amplifier is not required.

Table 3.1: Comparison with Previous 60 GHz Phased-Array Transmitter Chips

Chip Parameter	This Work	[5] TMTT 2019	[1] TMTT 2018	[3] TMTT 2016	[4] ISSCC 2013	[6] TMTT 2012
Technology	**45 nm CMOS SOI**	65nm CMOS SOI	0.18µm SiGe	0.18µm SiGe	40 nm CMOS SOI	65nm CMOS SOI
System Architecture	**All RF/ Tx**	All RF/ Tx	All RF/ Tx+Rx	All RF/ Tx	RF+Mixer/ Tx	All RF/ Tx
Frequency (GHz)	**57.5-65.5**	57-66	58-65	58-64	56.8-63	57-66
Number of Elements	**1**	4	4	64	4	4
VDD (V)	**1 (2 V for PA only)**	1.2	2.3	2.5	-	1
Gain (dB)	**22**	15	20	18	31	0
Gain Control (dB)	**14**	7	18	9	-	22
Phase Resolution (deg)	**11°**	22.5°	11°	11°	-	22.5°
RMS Gain Error (dB)	**< 0.7**	< 0.53	1.2	1.2	-	< 2.5*
RMS Phase Error	**< 5°**	< 8.8°	< 9°	< 9°	-	< 18°*
Pdc (mW) @P1dB /Element	**67**	113	155	95	182	100
OP1dB (dBm)	**10**	7.1	-2	0	10.8	5
PAE (%)	**6.1 @ 5 dB BO 14.6 @P1dB 18 @Peak**	4.5 @P1dB*	0.4 @P1dB	1 @P1dB	6.6 @P1dB	3.16@P1dB*
Modulation	**18 Gbps/64-QAM 20 Gbps/16-QAM**	-	2 Gbps/16-QAM 2 Gbps/QPSK	0.6 Gbps/64-QAM 3.8 Gbps/16-QAM	4.62 Gbps/16-QAM 2.3 Gbps/QPSK	-
Efficiency (%) at linear power	**6.1 400 MB 64-QAM EVM < -26 dBc**	-	0.13	-	1.5*	-
Element Area (mm^2)	**0.45**	0.53*	1.8 (Tx+Rx)	-	1.5	0.9*

*Estimated from plots/papers.

3.4.1 EVM

A 64-QAM 400 MBaud waveform with a 5 GHz carrier is used with a pulse shaping factor α=0.35. Fig. 3.12(a) presents the EVM_{RMS} versus the output power of the proposed 60 GHz Tx beamformer chip. In region 1, the EVM is limited by the low SNR due to the low signal power output and noise floor contributed by Tx chip and measurement setup. In region 2, the EVM is limited by the AWG SNR together with the phase noise contribution of the LO signal generator and the real-time scope (EVM_{meas}=2.2%). And in region 3, the EVM is limited by the power amplifier non-linearities. The 60 GHz Tx beamformer chip is capable of delivering an average output power of 5 dBm for a 64-QAM signal with 7.7 dB peak-to-average-ratio (PAPR) and with $<$5% EVM_{RMS} (-26 dBc), which is 5 dB backoff from P_{1dB}. The DC power consumption at 5 dBm is 52 mW, resulting in a modulated system PAE of 6.1%, which is the highest to date and is even better than most 28 GHz designs [**?**]. Even including a Tx/Rx switch loss of 1.3 dB, the

linear PAE of the Tx channel is still $> 4.5\%$ and higher than designs at 28 GHz [21]-[23]. A dynamic range of 29 dB is also achieved with $< 5\%$ EVM for the 64-QAM 400 MBaud waveform (including the setup). Knowing that the output SNR needs to be > 26 dB at low power to achieve an EVM $< 5\%$, this shows the SNR is >55 dB (29+26 dB) at a linear power of 5 dBm, and especially when the measurement system noise is taken out. Note that in Fig. 12(a), the Tx-ch EVM is determined using $\text{EVM}_{sys}=\sqrt{EVM_{meas}^2+EVM_{Tx}^2}$, with $\text{EVM}_{meas}=2.2\%$. The measured constellation diagrams for different backoff regions are shown in Fig. 3.12(b).

3.4.2 Wideband Performance

Fig. **??**(a) presents the measured EVM versus data rate for 16 and 64-QAM waveforms with 0 to -1 dBm of output power (10-11 dB BO) at a carrier frequency of 60 GHz. A data rate of 20 Gbps and 18 Gbps with 16 and 64-QAM waveforms is achieved with low EVM, respectively. For the 20 Gbps 16-QAM measurement, the instantaneous bandwidth required is 5 GHz (57.5-62.5 GHz), and is within the 3-dB bandwidth of the transmit chip. Example constellations for different data rates are shown in Fig. **??**(b).

Table 1 presents a comparison with the state-of-the-art transmit channels using CMOS and SiGe technologies. While several chips employ a Tx/Rx switch with a loss of 1.5 dB in [1], [7], [8], this work would still result in the highest PAE, both at P_{1dB} and at linear power, if the switch loss is factored in.

3.5 Conclusion

In this paper, a low-power, high-linearity and high-PAE transmit beamformer chip is presented. This design employs a cascode power amplifier with neutralization, and active and passive phase shifters for 5-bit phase control. Optimization between the different phase and gain cells, and a co-design of the power amplifier with the output transformer network have resulted in record efficiency, both at P_{1dB} and using 64-QAM waveforms with 5 dB backoff.

Chapter 4

A 60 GHz passive bidirectional mixer with > 24 dBm IIP3

4.1 Introduction

The design of a high-speed and high-data rate communication system at millimeter-wave frequency range ($\sim$30 GHz), has recently been in high demand for commercial use as well as high interest in various research applications. [22]. With a remarkable improvement of silicon technology together with a skyrocketed demands of using less crowded frequency bands for less interference to each other, numerous mm-wave MMICs are introduced in many applications such as automotive radar [23–25], short-range backhaul [26, 27], imaging systems [28, 29], wideband phased-array [30], wideband modulator with complex modulation for high-data rate wireless link [31, 32], and the 5G mobile communication system [33–35]. Therefore, the performance of signal generation at mm-wave frequency becomes one of the most important figure of merits (FOM) in the entire system. However, due to the stringent requirement in the market, the design of wideband, high-power, high spectral purity LO generation remains ongoing challenges.

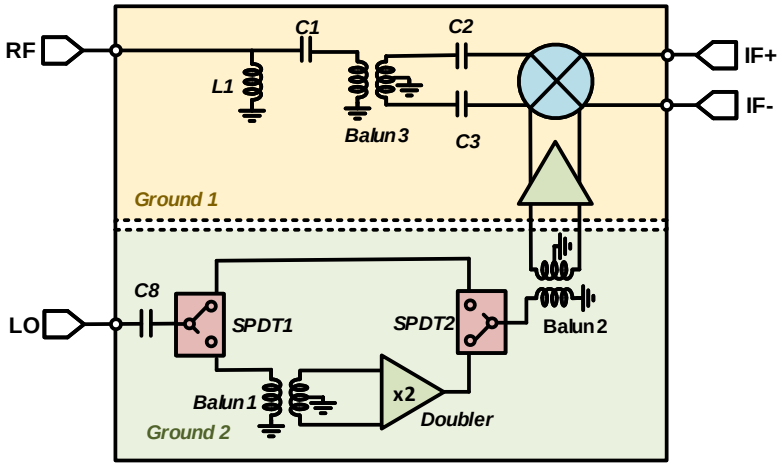

Figure 4.1: Block diagram of a 60 GHz mixer with doubler path and thru path on the LO structure.

4.2 Design Architecture

4.2.1 LO Path Design

The LO path is designed with two paths- doubler path and thru path. In the doubler path, the doubler is applied and the input frequency at the LO port is reduced to 30 GHz. Therefore, LO driving power from external source is much easier to achieve, compared with 60 GHz.In the thur path, the LO power from external source is delivered to mixer directly. In some application (eg, FMCW radar...), the LO path with doubler can not be suitable on the system design and the user can select the thru path.

Fig.4.3 and Fig.4.4 are the input and output SPDT design for LO path selection. At the 60 GHz, the good isolation is hard to achieve with the series transistors and we need to consider the trade off of isolation and switch loss. To optimize its performance, the shunt switches with $\lambda/4$ transmission line are designed as the SPDT switches. These designs are mainly optimized for insertion loss at thru path. For the input SPDT, the doubler path does not have inductor to have more wideband behavior at 25-35GHz. For the output SPDT, the doubler path and thru path

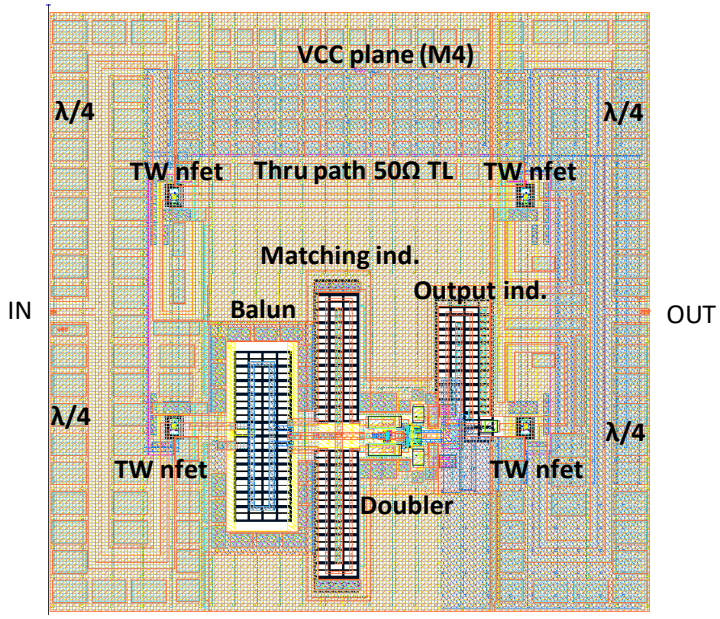

Figure 4.2: Layout of the LO structure with doubler path and thru path.

are symmetrical due to same input frequency. The loss caused by these SPDTs for both paths are around 2 dB with the $<$ -10 dB return loss and $<$-20 dB isolation. The IP_{1dB} for these SPDT designs are around 13.8 dBm.

Due the differential input required for the doubler, the balun are designed on the doubler path. MQ and M4 layers are used for higher coupling and it can achieve the 0.8 dB loss at 30 GHz and $<$ -10 return loss. Due to the symmetric layout, common mode signal is $<$ -25 dB.

Fig.**??**(a) shows the doubler design. The collectors of differential transistors are connected, which can cancel the odd mode of signal. The cascode transistor can improve the gain of this doubler. For the more wideband matching at the output, 800 Ω resistor is introduced to reduce the Q factor of the inductor. The input series inductor($\backsim$ 150 pH) can provide the good matching at 30 GHz and the bias condition is controlled by current mirror with the external current source. Due to the compact layout, the size of this 30 GHz doubler is 0.26 mm $\times$ 0.45 mm (shown in Fig. 4.5). Fig. 4.5(c) shows the power level of different harmonics versus input power. Due to the odd mode cancellation, 1^{st} and 3^{rd} harmonics are $<$ -45 dBm shown at the output with P_{in} = -5 5

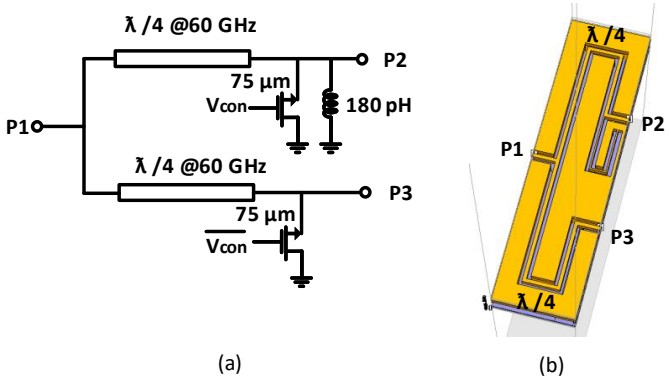

Figure 4.3: (a) Schematic and (b) layout of the input SPDT.

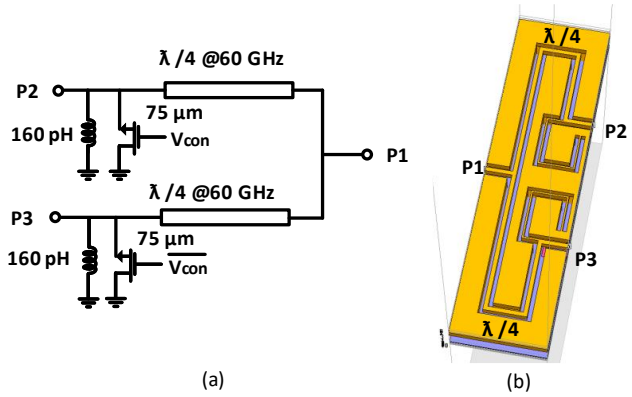

Figure 4.4: (a) Schematic and (b) layout of the output SPDT.

dBm. However, 2^{st} harmonic can be delivered over 2 dBm at 60 GHz with P_{in} = 0 dBm. It also shows that 0 dBm of input power at 30 GHz is enough to saturate the doubler and 5 dBm of that can not deliver more 2^{st} harmonic power at the output. For 4^{th} harmonic, it is $<$ -5 dBm at 120 GHz shown at the output. It is too far from our desired frequency band and can be filter out by the following components.

Fig.4.6 shows the simulation result of LO path when it is selected with doubler. Due to the frequency selection of SPDT, the 1^{st}, 3^{rd} and 4^{th} harmonic are $<$ -25 dBm and they would not have the effect on the mixer. 2^{nd} harmonic can reach 0 dBm at the LO path output with P_{in} = 0 dBm @ 30 GHz and it can be increased to over 1 dBm with P_{in} = 5 dBm @ 30 GHz.

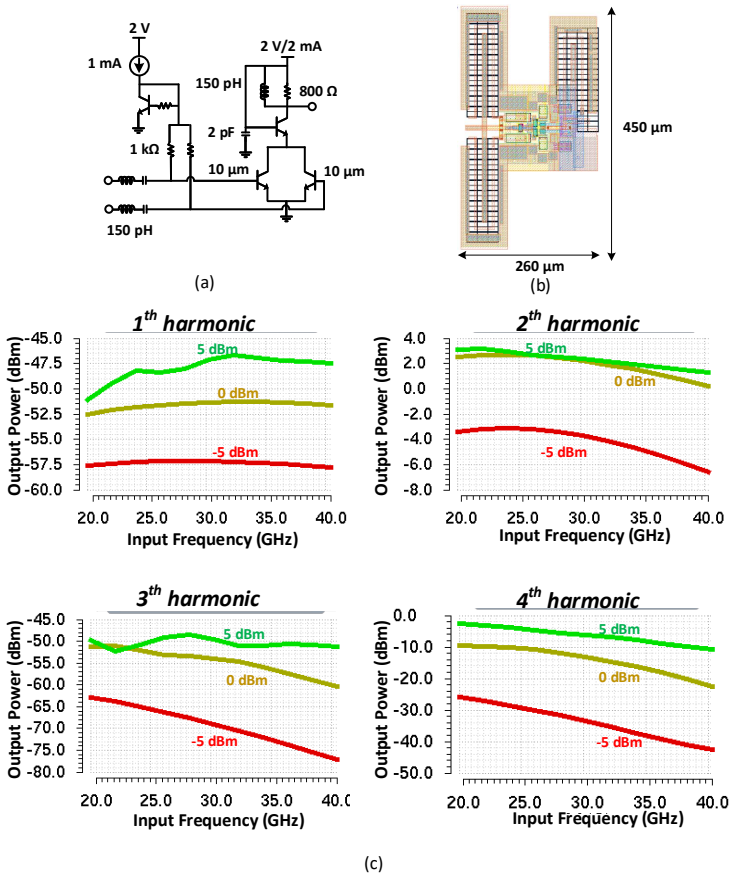

Figure 4.5: (a) Schematic and (b) layout of 30 GHz doubler and (c) power gain of various harmonics at the output.

Fig.4.7 shows the simulation result of LO structure when it is selected with thru path. It can achieve the good matching (< 10 dB) and low loss (< -4 dB) from 50-70 GHz.

Based on the simulation result, the LO structure can be used with doubler and it is required with 0 dBm @ 30 GHz input power. It also can be used with thru path and it is required with 60 GHz input power. Then the external LO power can be fed to mixer directly.

The differential LO power need to be fed to double balanced mixer. Therefore, the 60 GHz balun is designed after the output SPDT to transfer the single-ended LO to differential LO. It causes the 1.2 dB loss and > 20 dB common mode rejection.

The ground bump can introduce around 50 pH inductance. Therefore, the ground layer

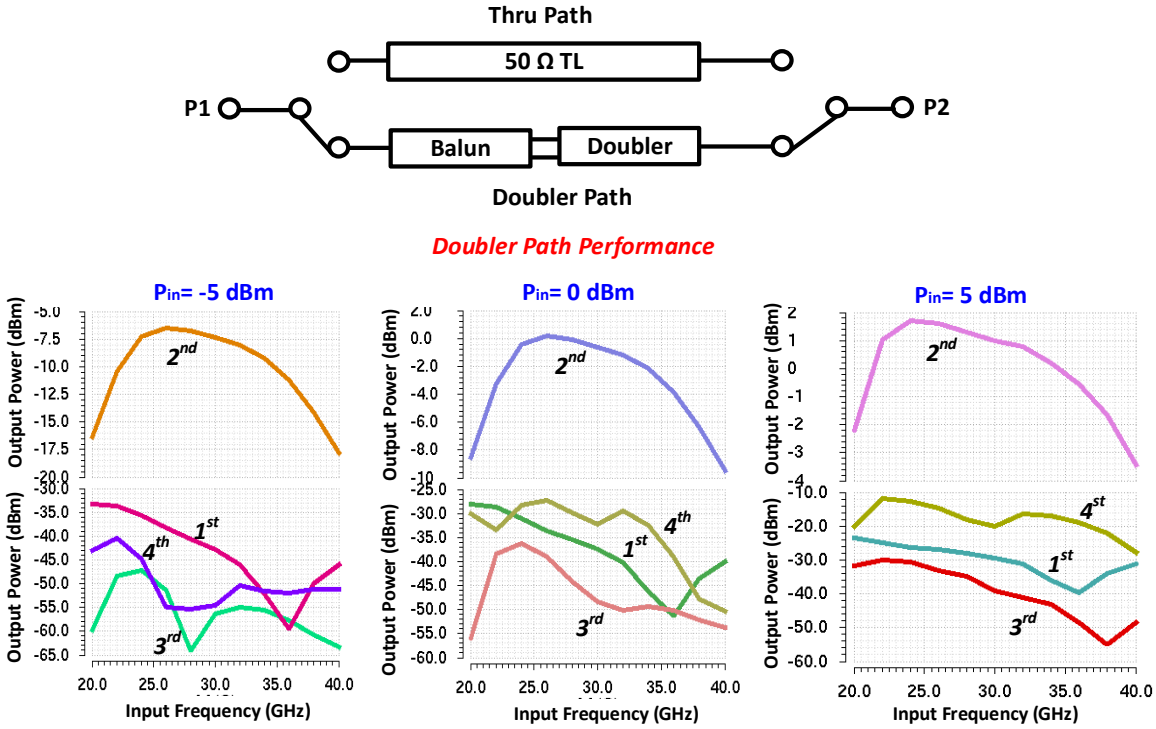

Figure 4.6: Power level with various harmonics on the doubler path.

on the chip is not the ideal ground for 60 GHz. In this case, The singled ended LO transmission line can caused the LO leakages through the ground layer, which is the dominant factor of LO leakage for 60 GHz mixer design. To reduce the LO leakage, the two separated ground planes are designed for this mixer system (Fig. 4.1). The plane 1 can provide the ground level for the mixer and differential LO path and the plane 2 can provide the ground level for the singled-ended LO path. These two ground plane are not physically connected on the chip and there is 45 μm gap between them to provide the isolation. Then the LO leakage on the ground plane 2 caused by the single-ended LO path can not be shown at the RF port of the mixer.

The larger LO voltage swing on the transistor gate can improve the conversion loss and linearity of the mixer. To provide the larger voltage swing on the LO port of mixer, the LO driver is applied before the mixer. The schematic and layout of LO driver are shown on the Fig. 4.8(a) and (b), respectively. The -3 dBm of input power is enough to saturate the LO driver and deliver

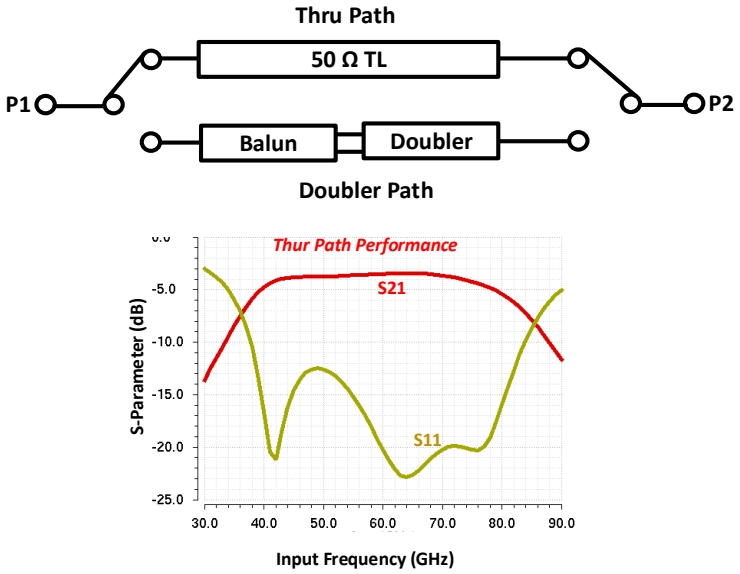

Figure 4.7: S-parameters on the thur path.

the maximum power 3.5 dBm to the mixer. The power consumption for the small signal is 32 mW and that at the saturation is 38 mW. The output matching of the LO driver is optimized for the maximum voltage swing on the transistor gate of the mixer.

4.2.2 Double Balanced Passive Mixer Design

This project goal is to achieve the high linearity bidirectional mixer. The double balanced passive mixer is the best architecture for this project.

The benefit of double balanced mixer can be presented in Fig. 4.9. Firstly, the signal can be analyzed based on Equation 4.1-4.4. Due to the differential LO, the conversion voltage gain can be improved by 6 dB and, which also causes the reduction of the NF. Additionally, RF feedthrough can be canceled at the IF port.

$$V_{IF}(t) = V_{IF+}(t) - V_{IF+}(t) \tag{4.1}$$

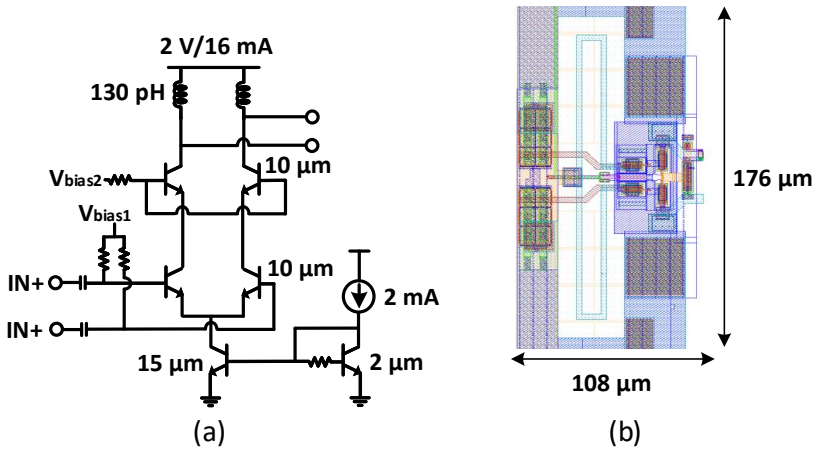

Figure 4.8: (a) Schematic and (b) layout of 60 GHz LO driver.

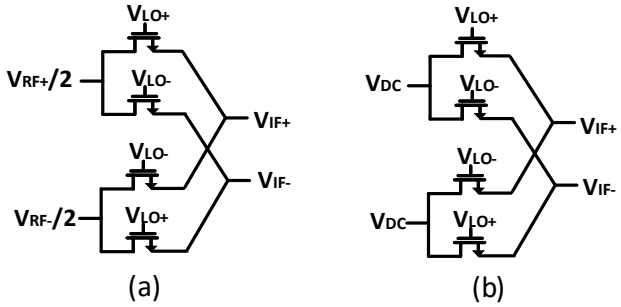

Figure 4.9: Schematic of double balanced mixer.

$$V_{IF+}(t) = c_1 e^{j\omega_{LO}t} V_{RF}(t) + c_{-1} e^{-j\omega_{LO}t} V_{RF}(t) + \ldots \tag{4.2}$$

$$V_{IF-}(t) = -c_1 e^{j\omega_{LO}t} V_{RF}(t) - c_{-1} e^{-j\omega_{LO}t} V_{RF}(t) + \ldots \tag{4.3}$$

$$V_{IF}(t) = 2c_1 e^{j\omega_{LO}t} V_{RF}(t) + 2c_{-1} e^{-j\omega_{LO}t} V_{RF}(t) + \ldots \tag{4.4}$$

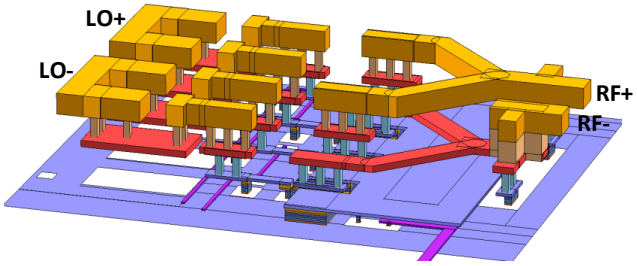

Figure 4.10: Layout of this proposed double balanced mixer.

The LO leakage can be canceled due to the differential RF port. Based on Equation 4.5-4.6, the LO leakage caused by the V_{DC} component at RF port can be removed.

$$V_{LO@RF+}(t) = Eff_{transistor}(LO_+ + LO_-) = 0 \tag{4.5}$$

$$V_{LO@RF-}(t) = Eff_{transistor}(LO_+ + LO_-) = 0 \tag{4.6}$$

Notes: LO_+ and LO_- are opposite and same magnitude.

However, the LO leakage cancellation is a precondition: the same LO leakage on the IF+ and IF- port. To reduce the mismatch of the LO leakage on IF+ and IF-, the differential RF and LO routing are perfectly symmetrical (shown Fig. 4.10). However, the mismatch of the transistors are another potential contribution on the imperfect cancellation. Therefore, the gate bias control is applied on these transistors(shown Fig. 4.11).. As shown in Equation 4.7, V_{gate1} and V_{gate2} can be adjusted to counteract the mismatch of transistor M1 and M2. Transistor size is selected with 12.5 μm width with R_{on}=37Ω and C_{off}=6,4 fF, which is optimized for the lower conversion loss of the mixer.

$$V_{LO@RF+}(t) = (Eff_{Vgate1} * Eff_{M1})LO_+ - (Eff_{Vgate2} * Eff_{M2})LO_- \tag{4.7}$$

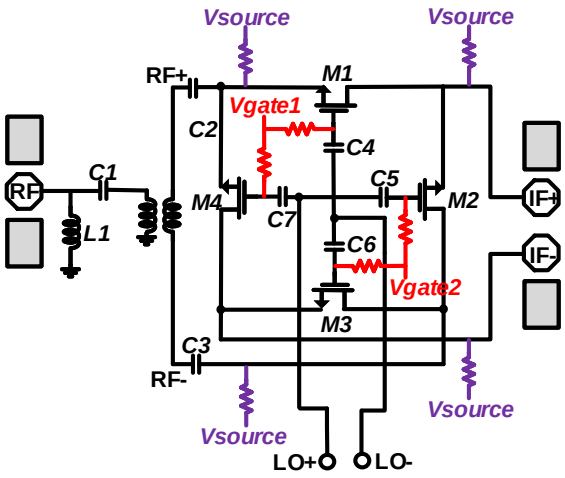

Figure 4.11: Double balanced mixer with bias voltage control to cancel the transistor mismatch.

Input matching at RF port is achieved by shunt 100 pH inductor and series 86 fF capacitor (Fig. 4.12(a)). 100 pH inductor is designed with AM layer with 27 of Q factor. Fig. 4.12(b) presents the good matching in 55-75 GHz.

Input matching at RF port is achieved by shunt 100 pH inductor and series 86 fF capacitor (Fig. 4.12(a)). 100 pH inductor is designed with AM layer with 27 of Q factor. Fig. 4.12(b) presents the good matching in 55-75 GHz.

Fig. 4.13 presents the mixer performance with the harmonics simulation at different nodes. The -10 dBm at 62 GHz RF signal is fed and the LO leakage at 60 GHz shown at RF port is -35 dBm. After the RF matching and balun, RF signal power at 62 GHz is reduced to -12.7 dBm, due to the loss from these passive structure. After the mixer, the RF signal is down-converted to 2 GHz with -21 dBm signal level. Therefore, the conversion loss of this proposed mixer is 11.5 dB based on the simulation, which is matched with our expectation.

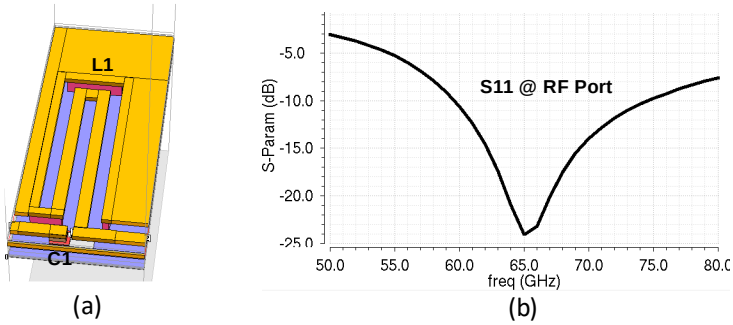

Figure 4.12: (a) RF matching layout and (b) simulated matching performance at RF port of the mixer.

4.3 Measurement Results

The 60 GHz mixer chip is measured with the Keysight PNA nextwork analyzer and Keysight E8663D PSG to provide the LO power(Fig. 5.15). In order to reduce the probe usage in the measurement, DC board for wirebonding is designed for this chip. DC bias pads and IF pads are connected to the board through the bond wire. The IF SMA connector is assembled for the IF signal measurement.

A 3ft 1.85 mm cable is used to connect the PNA to the RF port of mixer with 100 μm, which will introduce the 7 dB loss at 60 GHz. The IF port is differential and one of IF port is terminated by 50 Ω. Therefore, the additional 3 dB loss is shown in the measurement(it will be de-embeded in the following the measurements result). A 3 ft SMA cable is applied to connect with PNA. Due to the $<$ 6 GHz at IF port, the loss caused by the IF cable is around 1 dB. Keysignt PSG can provide the LO power up to 66 GHz and it can deliver enough LO power for the mixer. Based on the measurement result, the mixer shows the same performance with doubler and thru path.

Fig. 4.15(a) presents the simulated and measured conversion loss of the mixer chip with IF = 1 GHz. The conversion loss is around -13.5 dB with over 55-67 GHz 1.5 dB bandwidth and is well-matched with the simulation result. Fig. 4.15(b) presents the conversion loss at 60 GHz

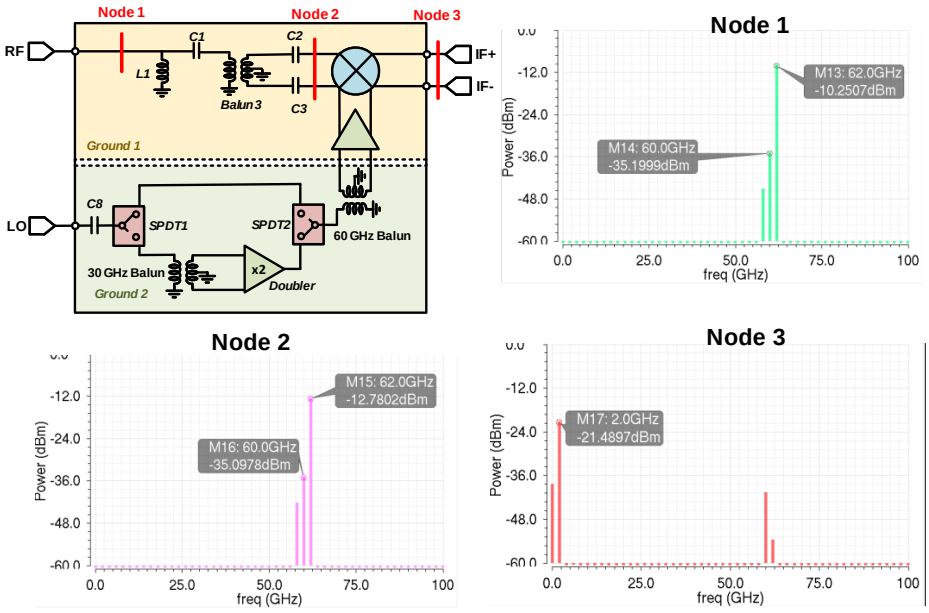

Figure 4.13: Simulated harmonic level at different node of the mixer.

versus LO driving power. It clearly shows that 0 dBm of LO power is enough to saturate the LO driver.

Fig. 4.16 shows the IF bandwidth with RF = 60 GHz. The mixer chip can achieve the 3 dB bandwidth of 4 GHz. It is limited the wirebond on the IF path. This can cause $\backsim$150 pH inductance which drop the bandwidth significantly.

Fig. 4.17(a) presents the measured noise figure of this proposed chip. Due to the passive structure of the mixer, the noise figure is around 14.5 dB, which is related to its loss. In the LO leakage measurements, it is $<$ -44 dB leakage shown at RF port in 55-65 GHz.

Due to its symmetric layout and adjustable bias voltage, 2^{nd} harmonic can be canceled perfectly on the differential IF port and it can provide over 32 dBm IIP2 from Fig. 4.18.

To make the mixer easier to integrate for the 60 GHz system, the mixer board is design in Fig. 4.19(a) for flip chip packaging. Based on the HFSS simulation, the bump can introduce the 50 pH inductance and the matching structures are design on RF port and LO port on the board to

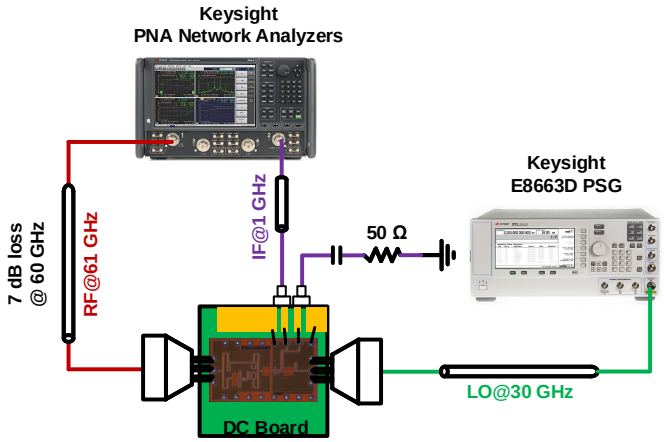

Figure 4.14: Measurement setup for conversion loss and linearity measurements.

solve the mismatch issue. In Fig. 4.20(a), the conversion loss of this mixer is around -18 dB with over 10 GHz bandwidth. The loss from the connector and PCB path at 60 GHz are around 2 dB and 3 dB, respectively. After de-embedding these loss, the conversion loss is the same with the measured result on the mixer chip. The IF bandwidth of this mixer board can reach to over 6 GHz with 1.5 dB bandwidth from Fig. 4.20(b). In the IIP3 measurement, the IIP3 of the mixer board is pretty high and all the IIP3 measurement is limited by the measurement equipment(PNA). In the Fig. 4.21, the measured IIP3 of this mixer is same with the that of the cable, especially for over 59 GHz. Therefore, the conclusion for IIP3 measurement is that this mixer can provide $>$ 24 dB and the accuracy value can not be measured because it is over the measurement range of the measurement equipment. Considering the connector and PCB path loss, the IIP3 referred to the chip can achieve $>$ 20 dB, which is the highest known to-date.

4.4 Conclusion

In this paper, a high linearity 60 GHz mixer is designed in GF8HP 0.12 μm SiGe BiCMOS technology and its flip-chip packaging is achieved on the low cost PCB. The LO structure can be selected for doubler path and thru path by SPDTs for various applications. And the mixer design

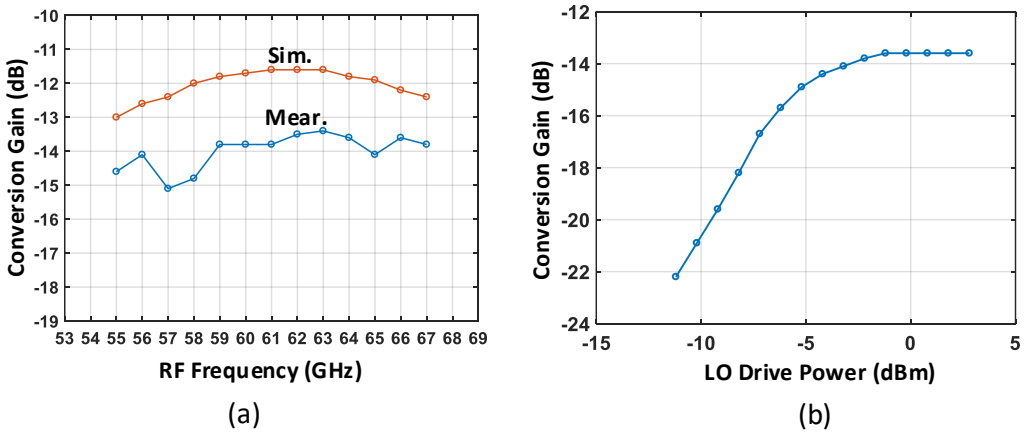

Figure 4.15: Measured conversion loss of the 60 GHz mixer chip.

is based on the double balanced passive mixer with adjustable bias voltage control to compensate the transistors mismatch. Optimization on the transistor and its layout has resulted in the around -13.5 dB conversion loss in 55-67 GHz with 0 dBm LO driving power. With assembled on the low cost RF board, the mixer board can reach around -18 dB conversion loss with $<$ 45 dBm LO leakage shown at the RF port. The IIP3 measurement is limited by the measurement setup and IIP3 of this proposed mixer board should be $>$ 24 dBm, which is the highest known to-date.

Acknowledgment

The authors thank GlobalFoundries for access to GF8HP 0.12 μm SiGe BiCMOS technology, Integrand Software for EMX, and Ansys for HFSS. This project is supported by NIST(National Institute of Standards and Technology).

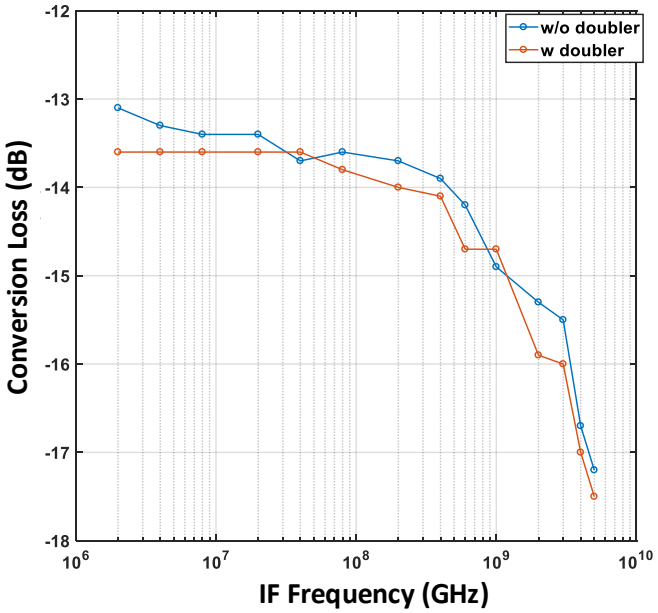

Figure 4.16: Measured IF bandwidth of the 60 GHz mixer chip when RF = 60 GHz.

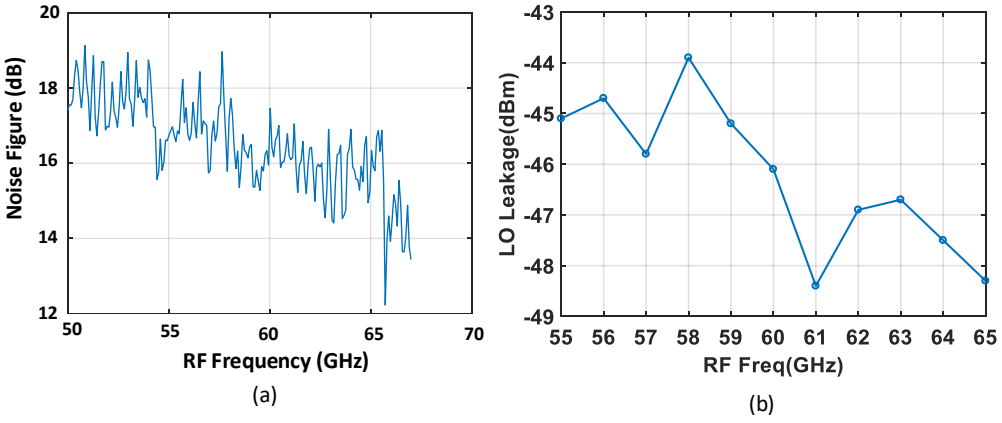

Figure 4.17: Measured (a) noise figure (b) LO leakage at the RF port of the mixer chip.

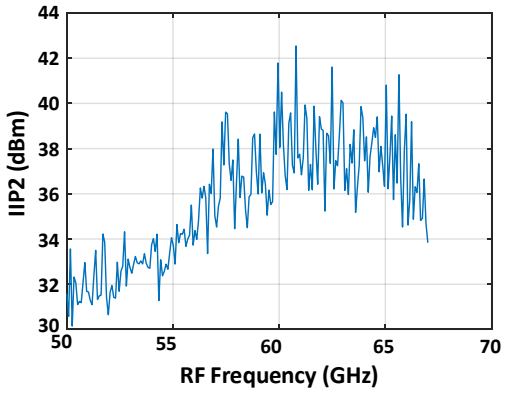

Figure 4.18: Measured IIP2 of the mixer chip.

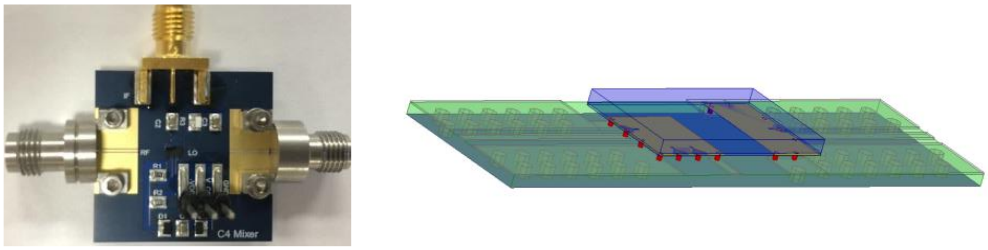

Figure 4.19: (a)Photograph of the 60 GHz flip chip packaged mixer board. (b) bump simulation structure by HFSS

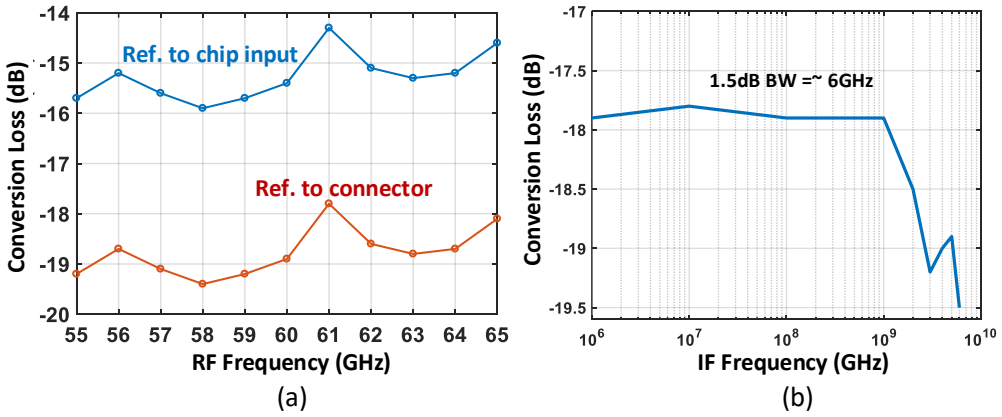

Figure 4.20: Measured (a) conversion loss (b) IF bandwidth of the packaged mixer board.

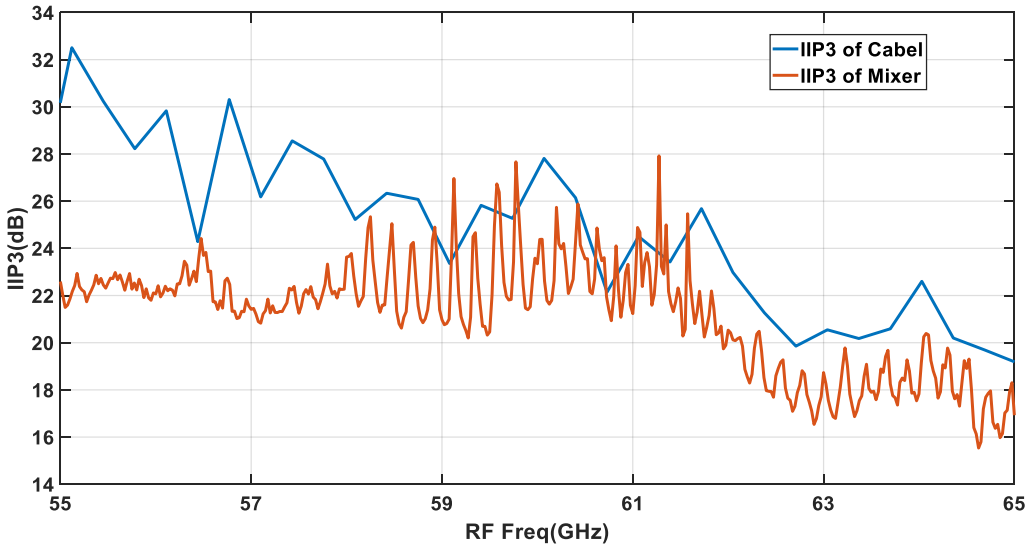

Figure 4.21: Measured IIP3 of the package mixer board and cable with PNA.

Chapter 5

A Low-Power 30-Gbps 16×16 Active Cross-Point Switch Matrix in 45-nm CMOS SOI

5.1 Introduction

5.2 Introduction

Due to the growing amount of data traffic in both long-haul and short-haul communication networks, high-speed non-blocking cross-point switches have attracted a lot of interest in the past few years. This versatile circuit, which can connect any input port (N) to any output port (M), is essential for reconfiguring optical networks both at the server level and between a cluster of servers, so as to meet changing traffic requirements or to switch multiple SONET packets. If they can be reconfigured rapidly, the switch matrix can also form the basis for packet-routing within a packet network, especially in cloud-computing architectures.

Switch matrices are typically built using advanced SiGe or CMOS circuits, and are based

on terminated amplifiers on each cross-over point between the input lines (rows) and output lines (columns) [36] [37] [38] [39]. The wideband amplifiers act as switches when turned off, have resistive loads at their input and ouput ports for wideband matching, and sometimes include inductive peaking at their loads. In large switch matrices and in order to avoid having 16 or 64 resistive loads all in parallel, line amplifiers are also used between the different row/column cells to act as isolators between the switching cells. This requires a lot of DC power, and switch matrices are known to be highly inefficient.

This paper presents a high-speed 16×16 active switch matrix in 45 nm RFSOI CMOS technology for digital networks. The design approach is a radical departure from the traditional matched-amplifier techniques, and is based on a loaded transmission-line designs with CMOS inverter-switches on each cross-cover. It is shown that this design methodology, when optimized, results in 32-64 Gbps 16×16 switching matrices with very low power consumption. Also, the physical dimension of the 16×16 switch matrix remains very small, with unit cells of 22×22 μm^2 and a total dimension of only 360×360 μm^2, which makes it suitable for multi-core microprocessors, multi-core graphics processors, and other data-intensive digital chips. Furthermore, the design can be easily scaled to 64×64 and higher-count switching matrices with virtually no changes.

This paper presents design methodology for the transmission-line approach and its optimization procedure, together with measurements on a 16×16 switch matrix at 30 Gbps with $<$ 0.55 pJ/bit (16-17 mW) per path. The design techniques can also be used in 22 nm, 14 nm and even 7 nm nodes.

5.3 ARCHITECTURE AND DESIGN

Fig. 5.1 presents the block diagram of the 16×16 switch matrix. Three-stage drivers are used at the input of each row to compensate for the printed-circuit board (PCB) path loss and

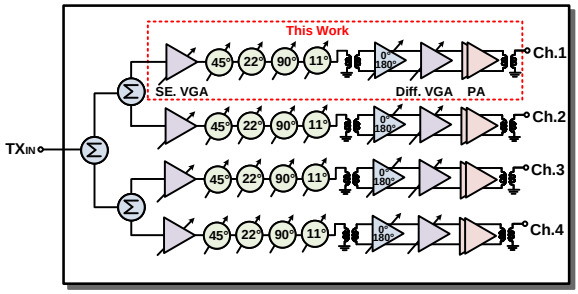

Figure 5.1: Block diagram of the 16×16 switch matrix. Retimer circuits are implemented on selected paths for test purposes.

regenerate the digital signals. Also, 50 Ω loads are employed at the input drivers to result in a matched transmission line and reduce any standing waves on the PCB. A three-stage driver is also used at the output of the switch matrix to drive other chips connected to the switch matrix on the PCB. The output buffer is sized large enough to drive a large capacitive load and does not have a resistive termination. A retimer circuit is placed at the input of some paths (paths 2, 7, 10, 15) so as to re-trigger the data with a clock signal. This allows the input data to be resampled at the clock edges and removes any group delay variations, and is placed for test on selected paths.

An active switch composed of a 3-stage buffer and a pass-switch is placed at every cross-point between the row (input) and column (output) transmission-lines. These switches allow for any input (IN_N) to be connected to any output (OUT_M) with conflicts prohibited by the control logic (e.g., multiple inputs cannot be connected to the same output). The row and column transmission-lines are terminated with 100 Ω and 75 Ω resistors, respectively, to provide an impedance match at the input and output ports of the active switches as detailed in Section E. These resistors could be replaced by matched drivers in the row and column directions and will allow the switch matrix to grow to 64×64 ports.

5.3.1 Technology

The switch matrix is designed in the GlobalFoundries 45-nm RFSOI process (IBM12SOI, precursor of the 45RFSOI technology used today) with thick metals layers as shown in Fig. 5.2(a).

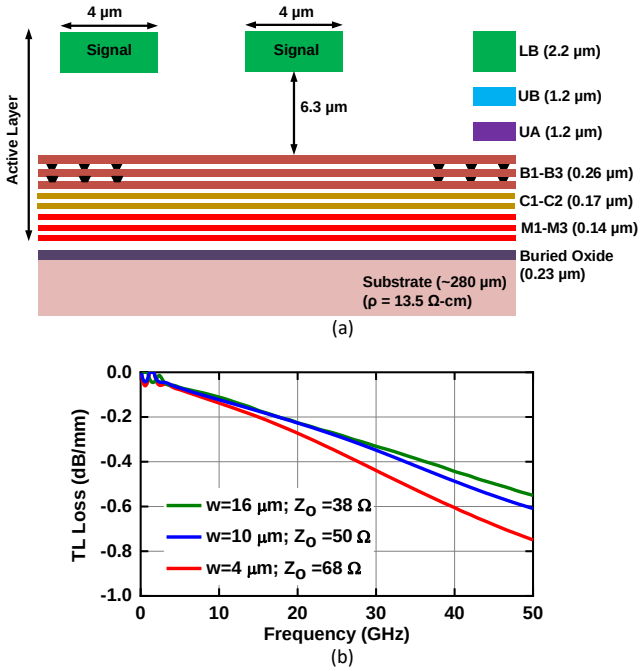

Figure 5.2: (a) GlobalFoundries 45 nm CMOS RFSOI back-end, (b) loss versus frequency for different Z_o.

A microstrip line with a width of 4-10 μm on LB with B3 as a ground plane and with Z_o=68-50 Ω has a simulated loss of 0.2-0.35 dB/mm at 30 GHz (Fig. 5.2(b)). The lower metals are used for supply, biasing and logic routing. The 45nm RFSOI CMOS transistor results in an f_t and f_{max} of 245 and 265 GHz, respectively, when used as an RF amplifier [40]. This process also provides advanced switch performance for mm-wave operation. The SOI switch has a figure of Merit (FoM):

$$FoM = R_{on}C_{off} = 5\ \Omega \times 18.8\ fF = 94\ fs \tag{5.1}$$

for a 48 μm NMOS transistor. This increases to 110-120 fs when referenced to the top metal and remains in this region for transistor sizes of 20-160 μm. A 0.23 μm thick buried-oxide (BOX) layer underneath the active layer results in high isolation between the transistors and the medium resistivity substrate. Therefore, the substrate resistance network, which degrades the insertion loss and isolation of CMOS switches at mm-wave frequencies, has minimal effect in this RFSOI process [41], [42].

5.3.2 Buffer and Active Switch Design

The input, output and clock buffers employ the same design, consisting of three inverters with a fan out ratio of 1:3:9 (Fig. 5.3(a)). The ratio of the PMOS and NMOS sizes are chosen to get a transition point at half the supply voltage.

A key parameter in the active cross-point switch design is the trade off between drive capacity and C_{off}. A large-size transistor can drive a large capacitive load, but leads to a higher C_{off} which can load the input or output lines. The $C_{off,in}$ and $C_{off,out}$ of the 3-stage buffer are 9 fF and 40 fF, respectively.

The active switch is a three-stage buffer with the ratio of 1:3:6 rather than the theoretically best fan out of 1:3:9 (Fig. 5.3(b)), for a lower C_{off} at the buffer output. Large control switches on the VDD and ground paths are used to save power consumption when a switch is turned off, which is the case of 15 out of 16 switches in a row. To further decrease the C_{off} at the switch output, a transmission gate with R_{on}=5 Ω and C_{off}=40 fF is used after the buffer. The transmission gate results in much faster turn-on and turn-off time than a single series switch. The large gate resistor (10 kΩ) reduces the C_{gs} and C_{gd} contribution on the signal path and improves the high frequency performance. The output capacitance of the active switch with the transmission gate is 25 fF (instead of 40 fF).

5.3.3 Retimer System Design

The retimer system comprises two D-latches and a clock distribution network (Fig. 5.4(a)). The clock distribution network features a broadband single-ended to differential conversion circuit, shown in Fig. 5.4(b). To reduce the imbalance of the differential clock, an “always on” series switch is placed in the thru path and provides the same delay compared with the inverted path.

In the signal path, a three-stage buffer is implemented before the re-trigger circuit to improve the rise/fall time and is the same as in Fig. 5.3(a). Fig. 5.4(c) presents the circuit diagram

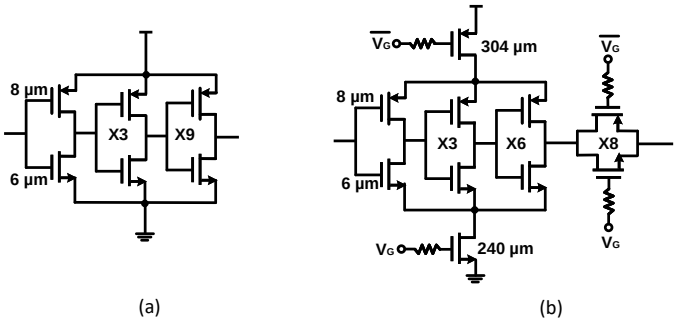

Figure 5.3: Schematic of (a) three-stage buffer, and (b) active switch.

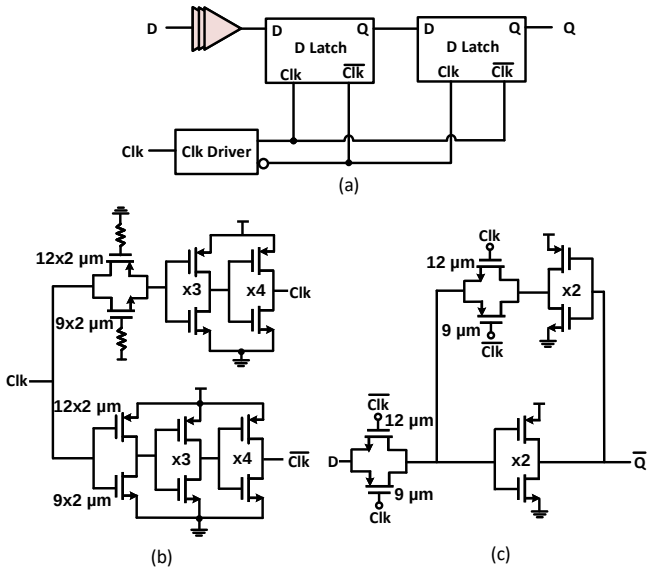

Figure 5.4: Schematic of (a) retimer system, (b) clock driver, and (c) D-latch.

of the re-trigger circuit, and the data is re-sampled at the input port with the clock period. The retimer circuit can recover a data rate of $>$ 32 Gbps and eliminate any group-delay variation and voltage-level reduction of data bits due to the long transmission lines before the switch matrix.

5.3.4 Loaded Transmission-Line Design

To connect the 16 inputs (rows) to the 16 outputs (columns), only one switch is activated in each row (Fig. 5.5). This creates capacitively-loaded transmission-lines for the row and columns

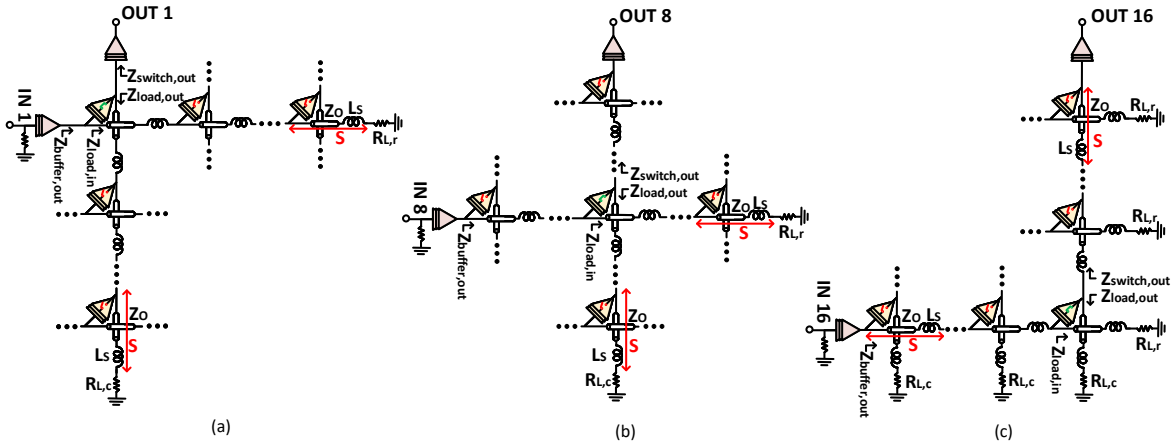

Figure 5.5: Signal paths for (a) (1,1), (b) (8,8), and (c) (16,16).

due to the off-state active switches ($C_{off,in/out}$) and cross-over capacitance (C_c) between the rows and columns. The loading is periodic with a unit cell given by a distance, s, which comprises an active switch, a row/column cross-over and an optional series inductor.

The equivalent circuits for paths (1,1), (8,8) and (16,16) are shown in Fig. 5.5, which present the three extremes in the switch-matrix design: For the (1,1) path, a long transmission line is attached to the active switch input node and acts as a parasitic load ($Z_{load,in}$), and another long transmission line is also attached to the active switch output node and also acts as a parasitic load ($Z_{load,out}$). For the (8,8) path, the parasitic transmission-line lengths are half, but there are long input and output lines (from the input buffer to the active switch and from the active switch to the output buffer). For the (16,16) path, the parasitic loads, $Z_{load,in}$ and $Z_{load,out}$, are effectively $R_{load,row}$ ($R_{L,r}$) and $R_{load,column}$ ($R_{L,c}$), but the input and output lines are long.

The loaded transmission-line impedance for the rows and columns is given by [43]

$$Z_{l,r} = \sqrt{\frac{sL_t + L_s}{sC_t + C_c + C_{off,in}}} \sqrt{1 - (\frac{\omega}{\omega_B})^2} \tag{5.2}$$

$$Z_{l,c} = \sqrt{\frac{sL_t + L_s}{sC_t + C_c + C_{off,out}}} \sqrt{1 - (\frac{\omega}{\omega_B})^2} \tag{5.3}$$

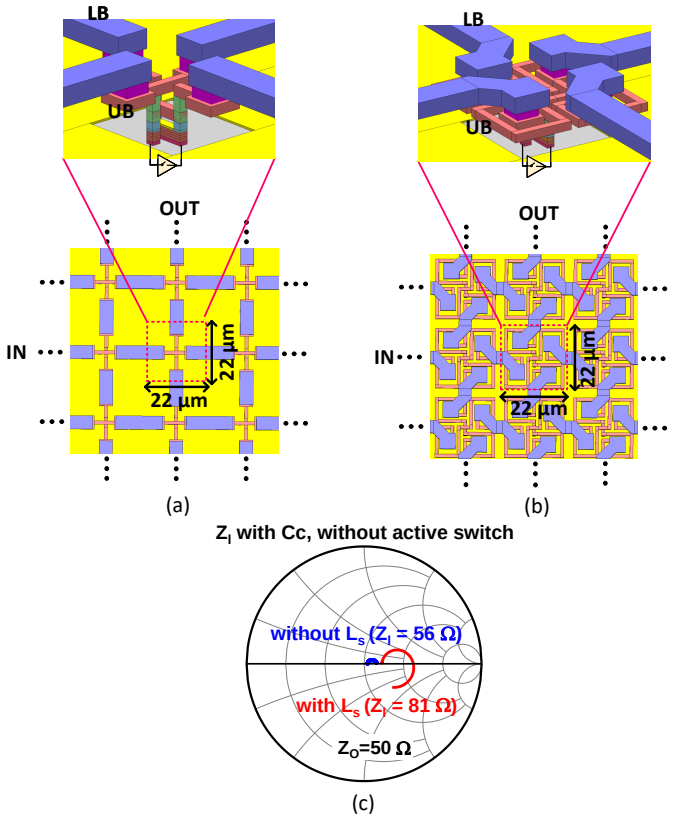

Figure 5.6: Layout of switching cell with (a) w=4 μm on LB and w=1 μm on UB, (b) spiral L_s included on UB (w=1 μm), (c) simulated S_{11} with a 50 Ω load with or without L_s (S_{11} plotted for 16 switch cells from DC to 50 GHz. The center of the S_{11} circle is the characteristic impedance of the loaded line).

where L_s is a lumped-element inductor added in each unit cell, and L_t and C_t and the inductance and capacitance per unit length for a transmission-line with Z_o and ε_{eff} given by:

$$L_t = \frac{\sqrt{\varepsilon_{eff}}}{c} Z_o \tag{5.4}$$

$$C_t = \frac{\sqrt{\varepsilon_{eff}}}{c Z_o} \tag{5.5}$$

and c is the speed of light. ω_B is the Bragg frequency given by [44]:

$$\omega_{B,r} = \frac{2}{\sqrt{(sL_t + L_s)(sC_t + C_c + C_{off,in})}} \tag{5.6}$$

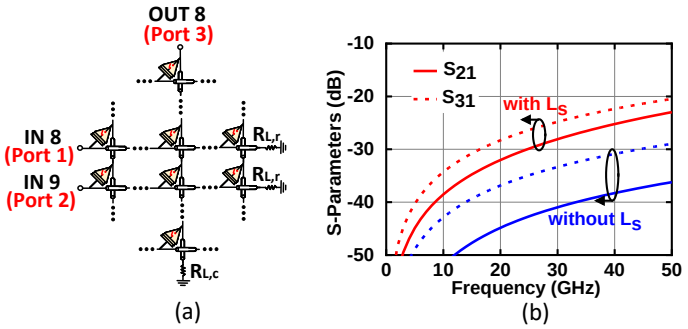

Figure 5.7: (a) Block diagram for coupling simulation, and (b) simulated S-parameters.

$$\omega_{B,c} = \frac{2}{\sqrt{(sL_t + L_s)(sC_t + C_c + C_{off,out})}} \tag{5.7}$$

The Bragg frequency is defined when the loaded transmission-line starts behaving as a low-pass filter with a sharp rejection skirt [44]. In general, one should operate at $f < f_B/2.2$ for best operation. In this frequency range, the line impedance is given by:

$$Z_l = \sqrt{\frac{sL_t + L_s}{sC_t + C_{load}}} \tag{5.8}$$

where C_{load} is the total loading capacitance in the period, s.

Fig. 5.6(a) and Table 5.1 present the switch matrix unit cells and detailed impedance calculations for the loaded row and columns. Starting with a line width of 4 μm, Z_o=68 Ω and s=22 μm, one finds that C_c (1 fF) drops the loaded-line impedance to Z_l= 56 Ω as shown in Fig. 5.6(c). The row and column loaded-line impedance further drop to $Z_{l,r}$=29 Ω and $Z_{l,c}$=19 Ω when the active switch input and output capacitances are taken into account. This is unacceptable and will result in large power consumption and low voltage swings.

One way to solve it is to add a series inductance in every unit cell as shown in Fig. 5.6(b). The inductors are built using the UB layer and are placed before and after the active switch, both in the row and in the column circuits, with a total inductance of 21 pH simulated using full-wave analysis in Ansys HFSS. The period increases to s=45 μm and the unloaded line impedance

Table 5.1: Comparison of Row and Column Routing Method

	Unloaded TL (4 µm width LB layer)	Loaded TL (Load C_c)		Loaded Row TL (Load $C_c + C_{off,in}$)		Loaded Column TL (Load $C_c + C_{off,out}$)	
		Without L_s	With L_s	Without L_s	With L_s	Without L_s	With L_s
s (µm)	22	22	45	22	45	22	45
C_c (fF)	-	1	2	1	2	1	2
$C_{off,in/out}$ (fF)	-	-	-	9	9	25	25
L_s (pH)	-	-	21	-	21	-	21
L_t (nH/mm)	0.46	0.46	0.46	0.46	0.46	0.46	0.46
C_t (pF/mm)	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Z_o (Ω)	68	-	-	-	-	-	-
Z_l (Ω)	-	56	81	29	52	19	37
f_B (GHz)	-	1540	436	672	247	430	166
ε_{eff}	4.2	6.0	12.0	23.0	28.7	53.1	58.4
α @16 GHz (dB/mm)	0.21	0.70	1.30	1.75	2.30	4.20	4.40

increases to Z_l=81 Ω using (5.8) with C_{load}=C_c only (Fig. 5.6(c)). Note that the physical period is still 22 μm, but the electrical length with the meander high-impedance transmission line (series inductor) becomes s=45 μm. The row-column coupling capacitance increases to C_c=2 fF (done using HFSS). The row and column loaded impedance drop to $Z_{l,r}$=52 Ω and $Z_{l,c}$=37 Ω, when taking into account the active switch capacitance loads, but are still $\sim 2\times$ higher than when no L_s is used. The Bragg frequency with L_s drops to 166 GHz for the column lines, and the switch matrix can be operated up to 75 GHz ($>$ 100 Gbps) before the Bragg response starts to dominate.

A loaded-line has a very high effective dielectric constant, ε_{eff}, given by:

$$V_{phase} = \frac{1}{\sqrt{(sL_t + L_s)(sC_t + C_c + C_{off,in/out})}} = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{5.9}$$

where c is the speed of light. ε_{eff} increases to 28.7 and 58.4 for the row and column lines, resulting in λ_{eff}=3.498 mm and 2.452 mm, respectively, at 16 GHz. With s=45 μm and 16-cells, the 16×16 switch matrix has an electrical length of $0.20\lambda_{eff}$ and $0.29\lambda_{eff}$ at 16 GHz for row and columns, respectively, and therefore transmission-line analysis is essential for this design.

The loss per unit length for loaded-lines is given by [43]

$$\alpha \sim \frac{R_s}{2Z_{loaded}} \tag{5.10}$$

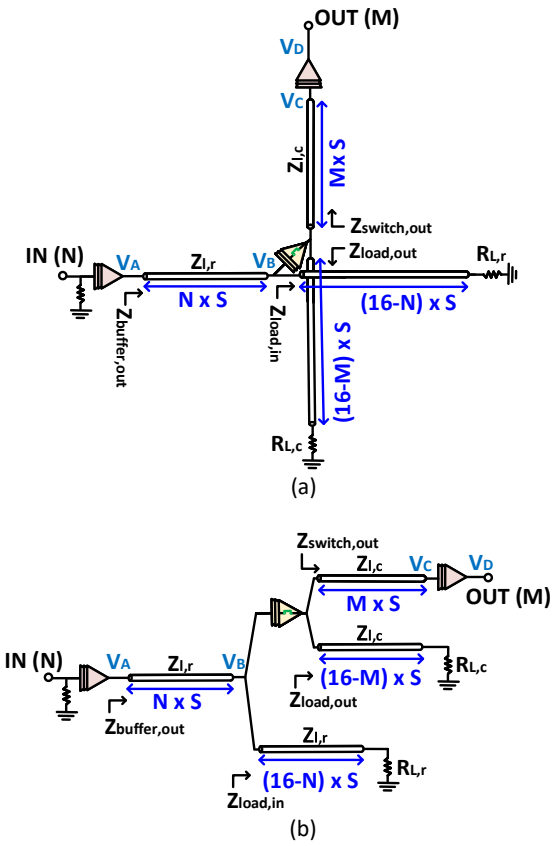

Figure 5.8: (b) Equivalent circuit for path (N,M) with loaded line impedances of the row and column lines, (b) equivalent circuit used in Cadence simulations.

where R_s is the series resistance (t-line + lumped-element inductor) per unit length. The loss was simulated using HFSS and is 2.3 dB/mm and 4.4 dB/mm at 16 GHz for the row and columns, which is much higher than the loss of a standard 50 Ω line (0.21 dB/mm). Again, and due to the short distance in the 16×16 switch matrix, the line loss remains relatively low and does not impact the operation at 32 Gbps.

For completeness, the passive coupling between rows and columns is simulated with all active switches turned off (Fig. 5.7). The coupling is $<$ -31 dB at 16 GHz (S_{31}) with L_s, which is low for a digital waveform. The coupling between rows remains at $<$ -35 dB at 16 GHz.

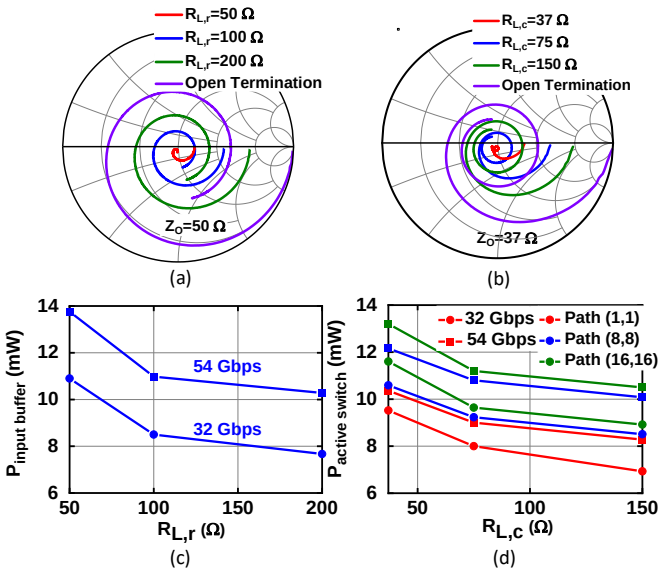

Figure 5.9: Simulated (a) $Z_{load,in}$ of path (1,1) and (b) $Z_{load,out}$ of path (1,1) with various terminal resistors for 0-50 GHz; (c) power consumed on input buffer and (d) power consumed on active switch by 32 Gbps and 54 Gbps data rate versus termination resistor values.

5.3.5 Row and Column Load Design

Fig. 5.5 presented the equivalent circuits of a row/column path. A simpler circuit using the loaded row and column transmission-line impedances can be drawn as in Figs. 5.8(a) and 5.8(b) with the parasitic load impedances $Z_{load,in}$ and $Z_{load,out}$ defined for the active-switch. Note that there are 64 different circuits for Fig. 5.8(b) for N=1-16 and M=1-16, but we will concentrate on paths (1,1), (8,8) and (16,16) for analysis purposes, as they represent the extremes of the 16×16 switch operation.

Path (1,1) has long transmission-lines as parasitic loads, and therefore, needs to be optimized first. Fig. 5.9 presents the simulated $Z_{load,in}$ and $Z_{load,out}$ for (1,1) versus the row and column termination resistors at DC-50 GHz. It is seen that if an open circuit (or an active buffer with no matched termination) is placed at the end of the row or column, $Z_{load,in}$ and $Z_{load,out}$ start as open circuits at low frequencies. But due to the large ε_{eff} of the loaded line, these impedances quickly turn into low values at 15-20 GHz, thereby resulting in a low voltage at the active switch input node. On the other hand, $R_{L,r}$=50 Ω and $R_{L,c}$=37 Ω result in an excellent

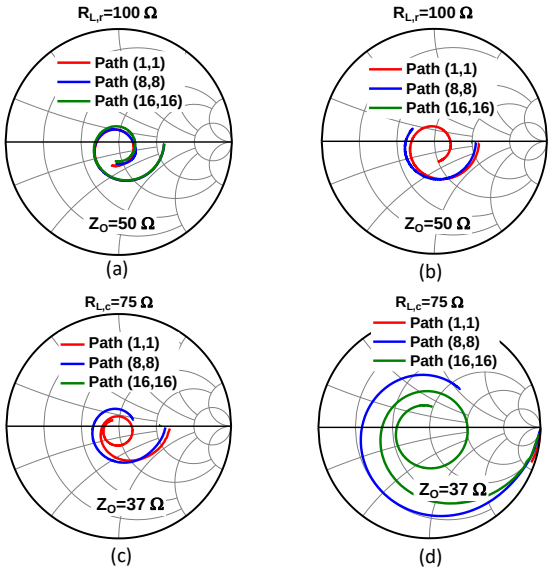

Figure 5.10: Simulated (a) $Z_{buffer,out}$, (b) $Z_{load,in}$, (c) $Z_{load,out}$, (d) $Z_{switch,out}$ for 0-50 GHz for paths (1,1), (8,8) and (16,16).

match for $Z_{load,in}$ and $Z_{load,out}$, respectively, but with a relatively low impedance which increases the input driver and active switch power consumption (Fig. 5.9(c), (d)). A compromise is found between impedance match and power consumption by selecting $R_{L,r}$=100 Ω and $R_{L,c}$ =75 Ω, which results in a VSWR <2 (S_{11} <-10 dB) over all frequencies and reduces the power consumption as compared to matched row and column lines.

The next step is to simulate the equivalent impedances defined in Fig. 5.8(b) for paths (1,1), (8,8) and (16,16) for $R_{L,r}$=100 Ω and $R_{L,c}$=75 Ω. These impedances are shown in Fig. **??**. $Z_{buffer,out}$, $Z_{load,in}$, and $Z_{load,out}$ are virtually the same for all paths, but $Z_{switch,out}$ varies with frequency because the output buffer is not terminated at its input port. Simulations on all 16×16 different paths indicate that the voltage at the V_C node is still high and that the output buffer will trigger correctly. Therefore, a load resistor is not placed at V_C to save power in the active switch.

Fig. 5.11 presents the simulated transmission-line loss from the input buffer to the active switch and from the active switch to the output buffer. As expected, path (1,1) has the shortest paths and with virtually no loss. Path (16,16) has the highest loss due to the loaded row and

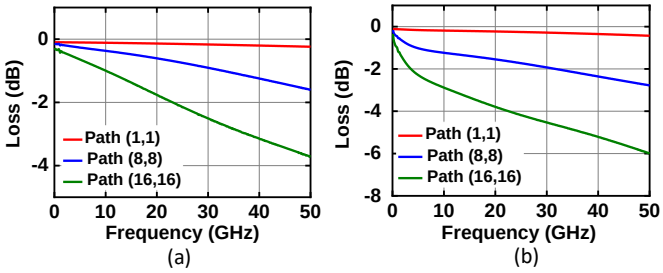

Figure 5.11: Simulated (a) loss from input buffer to the switch, (b) loss from the switch to the output buffer, for paths (1,1), (8,8) and (16,16).

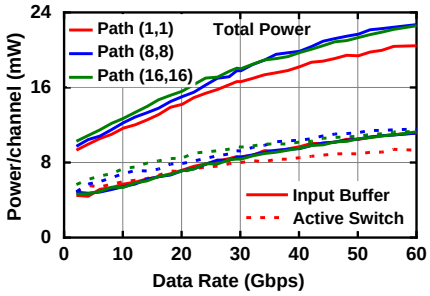

Figure 5.12: Simulated power consumption versus data rate for the input buffer and active switch, and total power consumption per channel.

column transmission-lines, but is still acceptable up to 16 GHz (3.3 dB). These simulations can be used for the design of a passive RC high-pass network to equalize the loss versus frequency, but this was not implemented in this work. The simulated loss agrees with the loaded-line loss from Table 5.1, as 4.4 dB/mm$\times$16$\times$45 μm = 3.2 dB.

5.3.6 Power Consumption

The simulated power consumption for a single path is shown in Fig. 5.12. The input buffer and active switch consume $\sim$ 8 mW each at 30 Gbps and is nearly each independent of the path, resulting in a total power consumption of 16-17 mW at 30 Gbps. Note that at very low data rates, the input buffer is effectively loaded by 100 Ω, and consumes 0.5$\times$(0.8 V/100 Ω) = 4 mW for a PRBS data rate. The active switch is loaded by 75 Ω, and consumes 5.33 mW at low

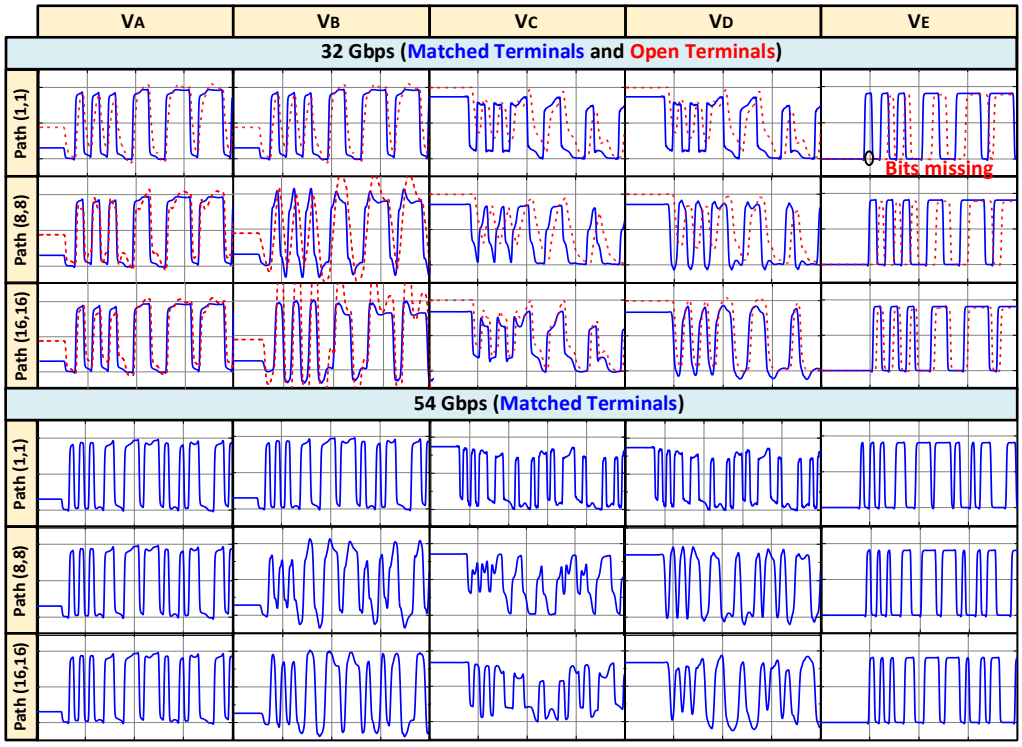

Figure 5.13: Simulated waveforms at different nodes for resistive and open-terminations (rows and columns), with data rates of 32 Gbps and 54 Gbps for paths (1,1), (8,8) and (16,16).

data rates. Therefore, the minimum power consumption per path is 9.33 mW at low data rates and increases to 16-17 mW at 30 Gbps. At 30-60 Gbps, the 16×16 switch matrix operates at 0.55-0.36 pJ/bit per path.

The output buffer is not taken into account as it can be driving a capacitive load (on the same chip) or driving a 50 Ω load (external to the chip for measurement instrumentation). If the output buffer is driving yet another 16×16 switch matrix, then it will consume 8 mW at 30 Gbps as it will be nearly the same as the input buffer.

5.3.7 16×16 Switch Simulations

Fig. 5.13 presents the 16×16 switch matrix simulations with paths (1,1), (8,8) and (16,16) shown in detail. A 10,000-bit PRBS-23 pattern was injected into the proposed switch matrix for

the Cadence simulations. Due to the size of the switch matrix, not all paths were energized as this will take a very long time to simulate in Cadence. Still, no matter what row/column path is energized (and its neighbors), there were no bit error rates found up to 54 Gbps, and Fig. 13 presents the extreme case paths of (1,1), (8,8) and (16,16). The effect of open-circuit loading for row and columns is clearly seen in the 32 Gbps results with the switch matrix failing in path (1,1).

Simulations (not shown) indicate that for $R_{L,r}$=50 Ω, $R_{L,c}$= 37 Ω, and a terminated output buffer with 100 Ω, the data rate exceeds 64 Gbps, at the expense of higher power consumption in the input buffer and active switch. In this case, the input buffer consumes 12-16 mW and the active switch consumes 16-20 mW, resulting in a power/channel of 28-36 mW at 32-64 Gbps, which is 1.6-1.7× higher than with $R_{L,r}$=100 Ω and $R_{L,c}$=75 Ω. Therefore, if higher power consumption is acceptable, then the optimal $R_{L,r}$ and $R_{L,c}$ values should be used for higher data rate.

5.3.8 16×16 Switch Fan Out and Chip Details

A microphotograph of the switch matrix is shown in Fig. 14(a), together with a blow up of the center part (Fig. 14(b)). The core is only 0.36×0.36 mm, with a physical cell size of 22×22 μm. The input and output lines are fanned-out for GSG probing using microstrip lines of w=10 μm (Z_o=50 Ω) and a ground plane height of h=6.3 μm, and with an edge-to-edge separation of 12 μm (∼2h) to fit within the physical period. This ensures very low coupling between the lines as shown in Fig. 5.14(c) and (d). The insertion loss between the GSG pads and the row or column feeds is $<$ 0.5 dB at 16 GHz for all paths.

The chip is operated from a 1 V supply and consumes 260 mW at 32 Gbps when all rows and columns are active (output buffer not included). Control logic is available and the pads are placed on the non-RF side.

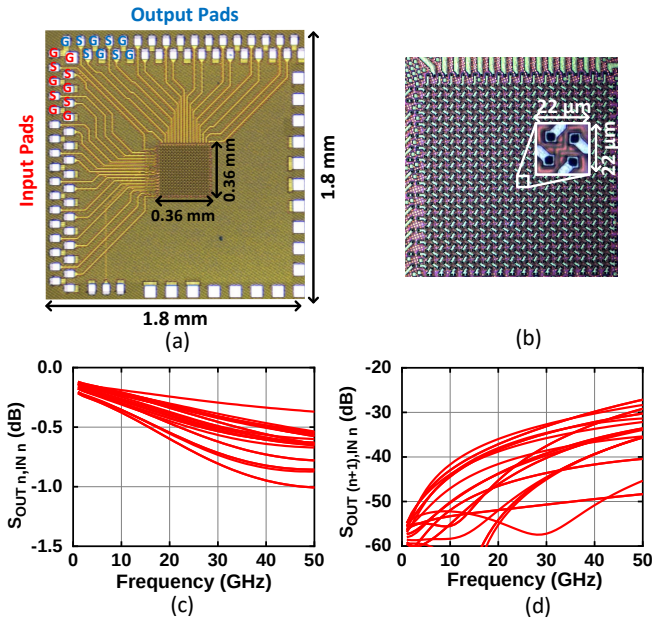

Figure 5.14: (a) Microphotograph of the 16×16 active switch matrix chip in 45nm CMOS SOI, (b) details of the 16×16 active switch matrix core and single switch cell, (c) simulated loss and (d) coupling of the routing lines between the core and the pads.

5.4 Measurements

Fig. 5.15 presents the measurement setup. All measurements are performed using two DC-50 GHz GSG probes and one path is activated at a time. The input pattern is generated using a Picosecond programmable pattern generator (PPG) with non-return to zero (NRZ) PRBS31 pattern and a maximum data rate of 30 Gbit/s. A 1 m long 2.4 mm cable is connected with the input probe and the pattern generator due to physical limitation. The output is sampled using a Keysight DSO-Z632A 63 GHz real-time oscilloscope, after another 1 m long 2.4mm cable. The equalizer is applied on the DSO to compensate the loss and group delay of the output cable. The pattern generator and DSO scope are synchronized using a 10 MHz clock.

Fig. 5.16 presents the measured eye diagram of path (1,1), (8,8) and (16,16) for different data rates and excellent results are achieved at all data rates.

Fig. 5.17 presents the measured output eye diagrams for different paths (labeled in Fig.

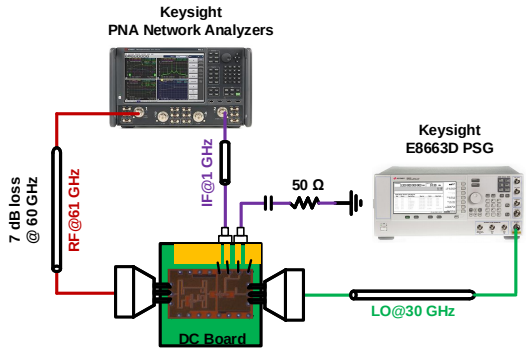

Figure 5.15: (a) Setup and (b) photo of the measurement environment.

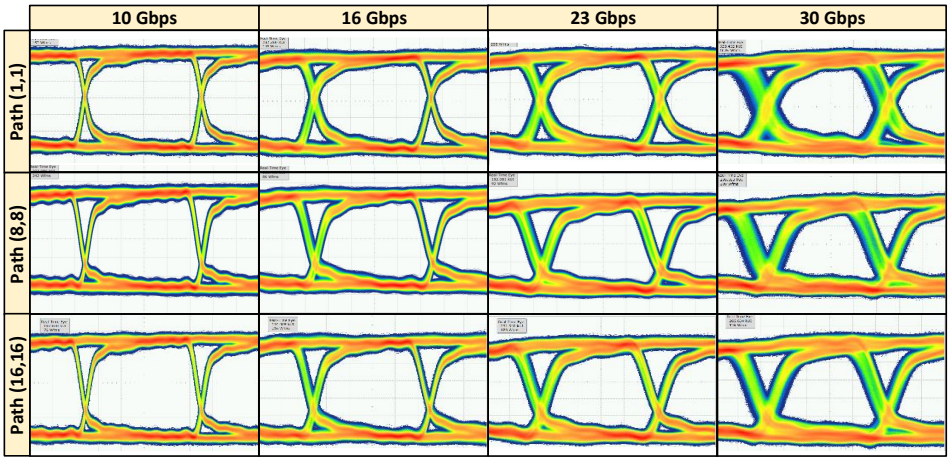

Figure 5.16: Measured eye diagrams for paths (1,1), (8,8) and (16,16) at different data rates.

5.1) at 30 Gbps. All provide an excellent eye diagrams with <8.3 ps peak-to-peak jitter and >5.2 V eye height. Path (1,1) is the worst case due to its long loading lines, for row and column, as predicted by simulations. The worst-case $jitter_{\sigma}$ is < 2.67 ps for all the measured eye diagrams, and the bit-error-rate (BER) can be estimated using [45]:

$$BER = Q(\frac{UI}{2Jitter_{\sigma}}) = 2 \times 10^{-10} \tag{5.11}$$

where UI is 33.3 ps for 30 Gbps. These values include the 1 m cable length as a real-time scope is used, and not a sampling scope with a sampling head at the GSG pads. The average peak-to-peak

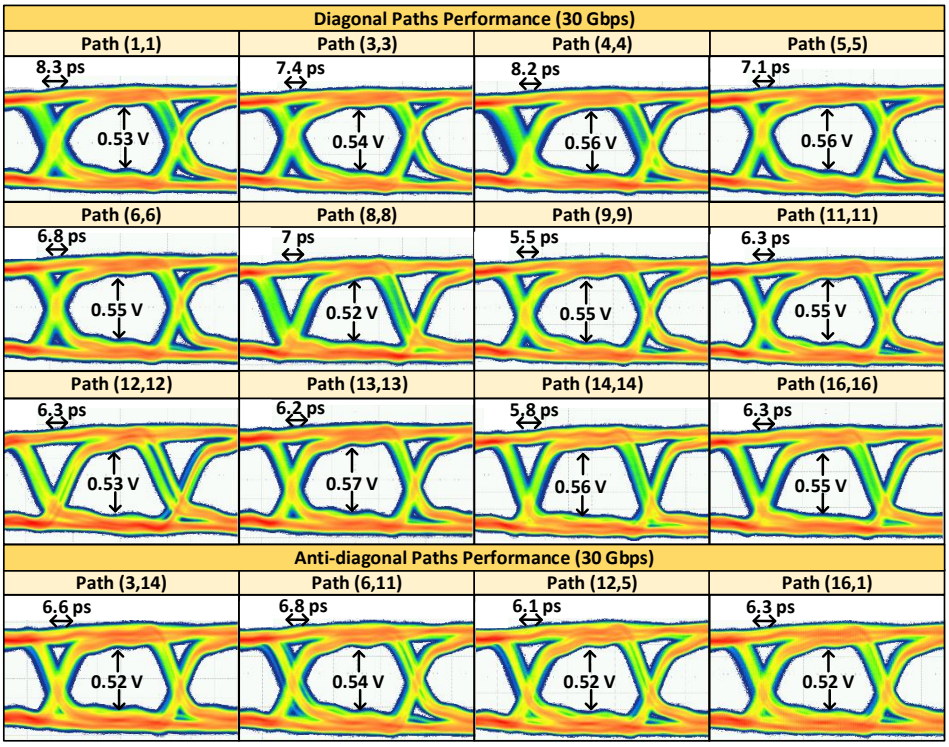

Figure 5.17: Measured eye diagrams for various paths at 30 Gbps.

jitter along all measured paths is 6.6 ps resulting in a simulated BER of $< 1.8 \times 10^{-14}$ for 30 Gbps. Measurements on paths having the clock re-timer circuit showed similar results and are not shown. Note that (5.11) and the BER values quoted above are estimates only, as (5.11) determines the BER at the center of the eye and assumes that the horizontal eye margin dominates the BER (which is the case here due to the large eye opening), assumes the system only has the Gaussian distributed random noise (random jitter), and finally assumes that the deterministic jitter is zero (which is not the case here based on the shape of the measured eye diagrams).

The coupling between adjacent outputs was also measured. Path (3,3) and path (8,8) are activated with 30 Gbps and the adjacent outputs are monitored. No data bit is recorded at any adjacent (or non-adjacent) output. Similar measurements were done on different paths, and again, with no measurable coupling.

The DC power versus data rate was measured for several channels and were within +/- 1

mW of each other (Fig. 5.18). Note that due to the GSG open circuits at the input of the unused rows, and the 3-stage input buffer on each row, the input buffer output voltage is constant at 0.8 V due to 100 Ω load impedance. The power consumed by each buffer is 0.8 V/100 Ω=8 mW (120 mW for all 15 un-used rows). This static power is removed from Fig. 5.18 as in reality, all input lines will be energized with PRBS data. It is seen that the switching matrix operates at 16-17 mW and $<$ 0.55 pJ/bit at 30 Gbps, per path, with the output buffer having an open circuit load as predicted by simulations. Table II summarizes the switch performance and compares it with published work.

The 16$\times$16 switch matrix can be extended to a 64$\times$64 design with virtually no change in any of the circuits (Fig. 5.19). Every 16$\times$16 switch matrix is self-contained with its own termination resistors and input and output drivers, and the 16$\times$16 blocks are concatinated together in the row and column directions. The average power consumption per path increases by 4$\times$ to 2.2-1.44 pJ/bit at 32-64 Gbps. The design can also be extended to 256$\times$256 switch matrices using the same technique.

5.5 Conclusion

In this paper, a low-power, high-speed and large-scale active switch matrix chip is presented. This design employs a buffer based switch as the switch core and optimized transmission line and terminal resistor to solve the low load impedance issue in the large scale switch matrix. Due to the low power consumption and compact layout, this proposed 16$\times$16 switch matrix can be widely used for receiver systems and backplane switching networks. Furthermore, the designs can be extended to differential circuits, which are less sensitive to ground inductance and are compatible with backplane data networks.

Table 5.2: Comparison With Previous Switch Matrix Chips

	This Work	[2]	[3]	[4]	[7]
Topology	16x16	16x16	16x16	20x20	4x4
Technology	45 nm RFSOI	AlGaAs/ GaAs HBT	GaAs HBT	0.25 µm SiGe BiCMOS	45 nm RFSOI
Data Rate (Gbps)	30	10	10	12.5	32
Isolation (dB)	>40	>40	>23	-	>40
Power (pJ/bit)	0.55	70.6	65.6	16	~0[1]
Dimensions (mm)	0.36x0.36	6.0x6.6	7.1x6.4	6.0x6.0	1.4x1.5

[1] : passive design

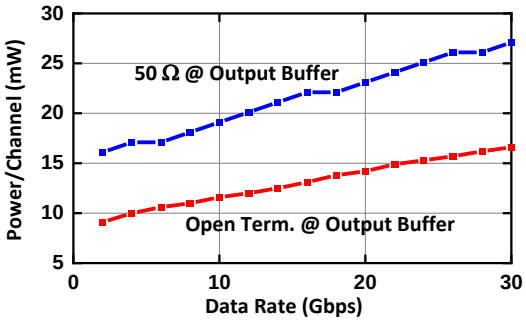

Figure 5.18: Measured average power consumption versus data rate.

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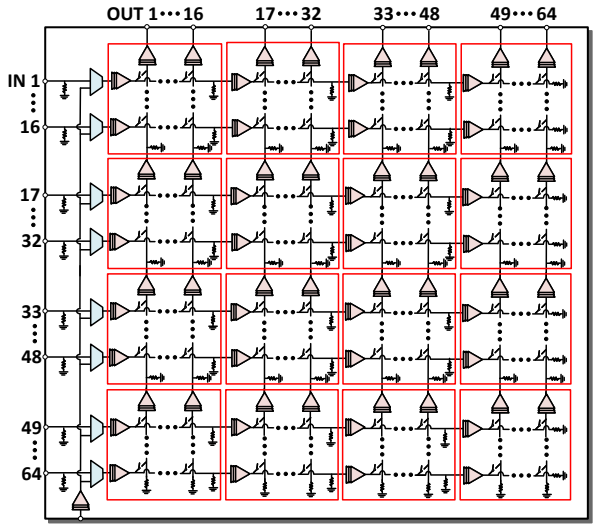

Figure 5.19: Extension to a 64×64 switch matrix using 16×16 building blocks.

Bibliography

[1] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "An ultra low-cost 32-element 28 ghz phased-array transceiver with 41 dbm eirp and 1.0–1.6 gbps 16-qam link at 300 meters," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2017, pp. 73–76.

[2] F. Daum, "Radar handbook, 3rd edition (m.i. skolnik, ed; 2008) [book review]," *IEEE Aerospace and Electronic Systems Magazine*, vol. 23, no. 5, pp. 41–41, 2008.

[3] B. Rupakula, A. Nafe, S. Zihir, Y. Wang, T. Lin, and G. Rebeiz, "63.5–65.5-ghz transmit/receive phased-array communication link with 0.5–2 gb/s at 100–800 m and ± 50° scan angles," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 9, pp. 4108–4120, 2018.

[4] Y. Wang, T. Phelps, K. Kibaroglu, M. Sayginer, Q. Ma, and G. M. Rebeiz, "28 ghz 5g-based phased-arrays for uav detection and automotive traffic-monitoring radars," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, 2018, pp. 895–898.

[5] F. Daum, "Radar handbook, 3rd edition (m.i. skolnik, ed; 2008) [book review]," *IEEE Aerospace and Electronic Systems Magazine*, vol. 23, no. 5, pp. 41–41, 2008.

[6] M. Jankiraman, B. J. Wessels, and P. Van Genderen, "Pandora multifrequency fmcw/sfcw radar," in *Record of the IEEE 2000 International Radar Conference [Cat. No. 00CH37037]*, 2000, pp. 750–757.

[7] B. Rupakula, A. Nafe, S. Zihir, Y. Wang, T. Lin, and G. Rebeiz, "63.5–65.5-ghz transmit/receive phased-array communication link with 0.5–2 gb/s at 100–800 m and ± 50° scan angles," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 9, pp. 4108–4120, 2018.

[8] B. Rupakula, S. Zihir, and G. M. Rebeiz, "Low complexity 54–63-ghz transmit/receive 64- and 128-element 2-d-scanning phased-arrays on multilayer organic substrates with 64-qam 30-gbps data rates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 12, pp. 5268–5281, 2019.

[9] S. Zihir, O. D. Gurbuz, A. Karroy, S. Raman, and G. M. Rebeiz, "A 60 ghz single-chip 256-element wafer-scale phased array with eirp of 45 dbm using sub-reticle stitching," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2015, pp. 23–26.

[10] V. Vidojkovic, V. Szortyka, K. Khalaf, G. Mangraviti, S. Brebels, W. v. Thillo, K. Vaesen, B. Parvais, V. Issakov, M. Libois, M. Matsuo, J. Long, C. Soens, and P. Wambacq, "A low-power radio chipset in 40nm lp cmos with beamforming for 60ghz high-data-rate wireless communication," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 2013, pp. 236–237.

[11] J. G. Lee, T. H. Jang, G. H. Park, H. S. Lee, C. W. Byeon, and C. S. Park, "A 60-ghz four-element beam-tapering phased-array transmitter with a phase-compensated vga in 65-nm cmos," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 2998–3009, 2019.

[12] J. Kuo, Y. Lu, T. Huang, Y. Chang, Y. Hsieh, P. Peng, I. . Chang, T. Tsai, K. Kao, W. Hsiung, J. Wang, Y. A. Hsu, K. Lin, H. Lu, Y. Lin, L. Lu, T. Huang, R. Wu, and H. Wang, "60-ghz four-element phased-array transmit/receive system-in-package using phase compensation techniques in 65-nm flip-chip cmos process," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 3, pp. 743–756, 2012.

[13] E. Cohen, M. Ruberto, M. Cohen, O. Degani, S. Ravid, and D. Ritter, "A cmos bidirectional 32-element phased-array transceiver at 60ghz with ltcc antenna," in *2012 IEEE Radio Frequency Integrated Circuits Symposium*, 2012, pp. 439–442.

[14] M. Boers, B. Afshar, I. Vassiliou, S. Sarkar, S. T. Nicolson, E. Adabi, B. G. Perumana, T. Chalvatzis, S. Kavvadias, P. Sen, W. L. Chan, A. H. Yu, A. Parsa, M. Nariman, S. Yoon, A. G. Besoli, C. A. Kyriazidou, G. Zochios, J. A. Castaneda, T. Sowlati, M. Rofougaran, and A. Rofougaran, "A 16tx/16rx 60 ghz 802.11ad chipset with single coaxial interface and polarization diversity," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3031–3045, 2014.

[15] Y. Yu, P. G. M. Baltus, A. de Graauw, E. van der Heijden, C. S. Vaucher, and A. H. M. van Roermund, "A 60 ghz phase shifter integrated with lna and pa in 65 nm cmos for phased array systems," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1697–1709, 2010.

[16] W. Chen, Ming-Huei Huang, Pei-Yu Lyu, S. Chang, and C. Chang, "A 60-ghz cmos 16-beam beamformer for two-dimensional array antennas," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1–3.

[17] S. Wu, L. Chiu, K. Lin, and T. Chang, "Robust hybrid beamforming with phased antenna arrays for downlink sdma in indoor 60 ghz channels," *IEEE Transactions on Wireless Communications*, vol. 12, no. 9, pp. 4542–4557, 2013.

[18] H. Chung, Q. Ma, and G. M. Rebeiz, "A 1 v 54-64 ghz 4-channel phased-array receiver in 45 nm rfsoi with 3.6/5.1 db nf and -23 dbm ip1db at 28/37 mw per-channel," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2019, pp. 119–122.

[19] S. Zihir and G. M. Rebeiz, "A 60 ghz 64-element phased-array beam-pointing communication system for 5g 100 meter links up to 2 gbps," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016, pp. 1–3.

[20] O. Inac, M. Uzunkol, and G. M. Rebeiz, "45-nm cmos soi technology characterization for millimeter-wave applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 6, pp. 1301–1311, 2014.

[21] M. Sayginer and G. M. Rebeiz, "A w-band lna/phase shifter with 5-db nf and 24-mw power consumption in 32-nm cmos soi," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 4, pp. 1973–1982, 2018.

[22] T. S. Rappaport, J. N. Murdock, and F. Gutierrez, "State of the art in 60-ghz integrated circuits and systems for wireless communications," *Proceedings of the IEEE*, vol. 99, no. 8, pp. 1390–1436, 2011.

[23] H. Rohling and E. Lissel, "77 ghz radar sensor for car application," in *Proceedings International Radar Conference*, 1995, pp. 373–379.

[24] B. . Tullsson, "Alternative applications for a 77 ghz automotive radar," in *Record of the IEEE 2000 International Radar Conference [Cat. No. 00CH37037]*, 2000, pp. 273–277.

[25] V. Jain, F. Tzeng, L. Zhou, and P. Heydari, "A single-chip dual-band 22–29-ghz/77–81-ghz bicmos transceiver for automotive radars," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3469–3485, 2009.

[26] Y. Wang, D. Luo, Q. Pan, L. Jing, Z. Li, and C. P. Yue, "A 60ghz 4gb/s fully integrated nrz-to-qpsk modulator soc for backhaul links in fiber-wireless networks," in *ESSCIRC Conference 2015 - 41st European Solid-State Circuits Conference (ESSCIRC)*, 2015, pp. 152–155.

[27] M. Z. Aslam, Y. Corre, J. Belschner, G. S. Arockiaraj, and M. Jäger, "Analysis of 60-ghz in-street backhaul channel measurements and lidar ray-based simulations," in *2020 14th European Conference on Antennas and Propagation (EuCAP)*, 2020, pp. 1–5.

[28] Z. Briqech and A. Sebak, "Millimeter-wave imaging system using a 60 ghz dual-polarized aftsa-sc probe," in *2016 33rd National Radio Science Conference (NRSC)*, 2016, pp. 325–332.

[29] M. Seo, B. Ananthasubramaniam, U. Madhow, and M. J. W. Rodwell, "Millimeterwave (60 ghz) imaging wireless sensor network: Recent progress," in *2007 Conference Record of the Forty-First Asilomar Conference on Signals, Systems and Computers*, 2007, pp. 396–400.

[30] S. Xiao, S. Yang, Y. Chen, and S. Qu, "A planar ultra- wideband phased array antenna with low electromagnetic scattering," in *2018 IEEE International Symposium on Antennas and Propagation USNC/URSI National Radio Science Meeting*, 2018, pp. 2339–2340.

[31] H. Al-Rubaye and G. M. Rebeiz, "A dc-60 ghz i/q modulator in 45 nm soi cmos for ultra-wideband 5g radios," in *2018 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 2018, pp. 275–278.

[32] Q. Ma, H. Chung, and G. M. Rebeiz, "A low evm sige bicmos 40–100 ghz direct conversion iq modulator for multi-gbps communications systems," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2018, pp. 188–191.

[33] Y. Yin, S. Zihir, T. Kanar, and G. M. Rebeiz, "A 37-42 ghz 8x8 phased-array for 5g communication systems with 48-50 dbm eirp," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019, pp. 480–483.

[34] Y. Wang, T. Phelps, K. Kibaroglu, M. Sayginer, Q. Ma, and G. M. Rebeiz, "28 ghz 5g-based phased-arrays for uav detection and automotive traffic-monitoring radars," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, 2018, pp. 895–898.

[35] Y. Yin, T. Phelps, B. Ustundag, K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A 1 gbps 3.5-4.75 km communication link based on a 5g 28 ghz 8×8 phased-array," in *2019 IEEE International Symposium on Phased Array System Technology (PAST)*, 2019, pp. 1–4.

[36] W. J. Turner, J. W. Poulton, J. M. Wilson, X. Chen, S. G. Tell, M. Fojtik, T. H. Greer, B. Zimmer, S. Song, N. Nedovic, S. S. Kudva, S. R. Sudhakaran, R. Bashirullah, W. Zhao, W. J. Dally, and C. T. Gray, "Ground-referenced signaling for intra-chip and short-reach chip-to-chip interconnects," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, 2018, pp. 1–8.

[37] A. G. Metzger, C. E. Chang, K. D. Pedrotti, S. M. Beccue, Keh-Chung Wang, and P. M. Asbeck, "A 10-gb/s high-isolation, 16/spl times/16 crosspoint switch implemented with algaas/gaas hbt's," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 593–600, 2000.

[38] K. S. Lowe, "A gaas hbt 16/spl times/16 10-gb/s/channel crosspoint switch," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 8, pp. 1263–1268, 1997.

[39] H. Veenstra, P. Barre, E. van der Heijden, D. van Goor, N. Lecacheur, B. Fahs, G. Gloaguen, S. Clamagirand, and O. Burg, "A 20-input 20-output 12.5gb/s sige cross-point switch with less than 2ps rms jitter," in *2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC.*, 2003, pp. 174–486 vol.1.

[40] O. Inac, M. Uzunkol, and G. M. Rebeiz, "45-nm cmos soi technology characterization for millimeter-wave applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 6, pp. 1301–1311, 2014.

[41] M. Uzunkol and G. M. Rebeiz, "140–220 ghz spst and spdt switches in 45 nm cmos soi," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 8, pp. 412–414, 2012.

[42] D. Shin and G. M. Rebeiz, "A 32-gbps 4×4 passive cross-point switch in 45-nm soi cmos," in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2013, pp. 253–256.

[43] S. Barker and G. M. Rebeiz, "Distributed mems true-time delay phase shifters and wide-band switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1881–1890, 1998.

[44] N. S. Barker and G. M. Rebeiz, "Optimization of distributed mems transmission-line phase shifters-u-band and w-band designs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 11, pp. 1957–1966, 2000.

[45] L. W. C. II, "Digital and analog communication systems, 5th edition (prentice hall; 1997) [book review]," *IEEE Aerospace and Electronic Systems Magazine*, vol. 23, no. 5, pp. 41–41, 1997.