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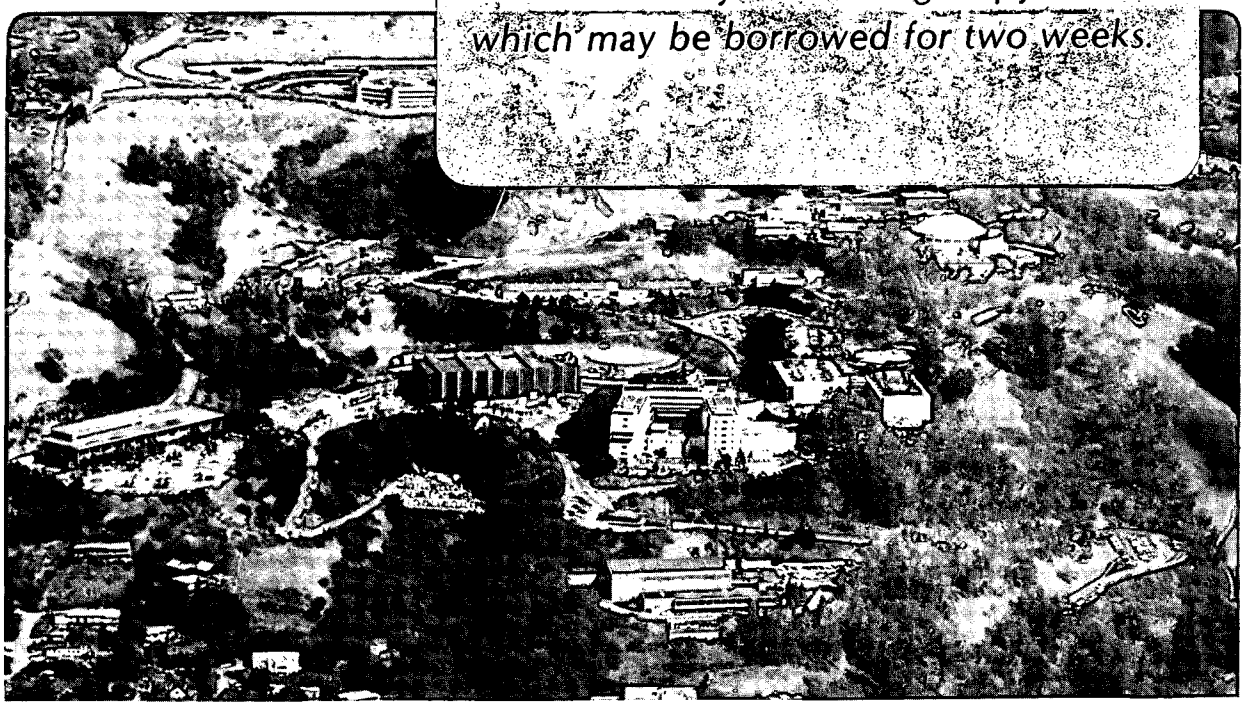

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DISCLAIMER

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SUMMARY

An end cap calorimeter system has been added to the MARK II detector in preparation for its use at the SLAC Linear Collider. The calorimeter uses 8744 rectangular proportional counter tubes. This paper describes the design features of the data acquisition electronics that has been installed on the calorimeter. The design and use of computer-based test stands for the amplification and signal-shaping components is also covered.

A portion of the complete system has been tested in a beam at SLAC. In these initial tests, using only the calibration provided by the test stands, a resolution of $18\%/\sqrt{E}$ was achieved.

INTRODUCTION

The MARK II detector system will soon be installed in its third collider. It was originally installed on the SPEAR storage ring at SLAC in 1977, where it ran for two years. In 1979, it was moved to PEP, where it was used from December 1979 to April 1984. Recently, it was chosen to be the first detector system to be installed on the SLAC Linear Collider (SLC), which will become operational in 1986.

In preparation for the SLC installation, the detector has been undergoing modifications and upgrades. This paper is concerned with one of those upgrades: the End Cap Calorimeter.

The End Cap Calorimeter uses an array of aluminum proportional tubes of rectangular cross-section—0.9 x 1.5 cm. Layers of proportional tubes are sandwiched between layers of 3 mm thick lead. Each layer contains 244 tubes. The layers are toroidal in nature, with an outer diam of 2.95 m and an inner diam of 0.67 m. A portion of a layer is shown in the sketch of Fig. 1. To conform to the geometry of the cross-section, the tubes vary in length from 44 to 280 cm. Thirty-six of these layers of tubes and lead are laminated to form each end cap. The assembled end cap is 0.51 m thick which corresponds to 18 radiation thicknesses.

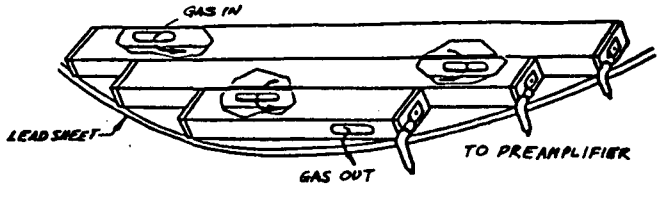


Fig. 1. Sketch of a portion of a layer of the calorimeter. Three proportional tubes of rectangular cross-section are shown.

The wires in the proportional tubes are 2 mil diam Stablohm. The tubes are operated with a mixture of 89% Argon, 10% Carbon Dioxide and 1% Methane (HRS gas). At approx. 1650 v, the gas gain is 2.3×10^4.

Each end cap has 8734 proportional tubes. In order to reduce the number of electronic signal channels to 1276 per endcap, the anodes of small groups of tubes (~ 7 on the average) are connected together to form a single signal channel. This ganging uses projective geometry to maximize the signal (improve resolution) from a typical track into a few electronic channels.

Each set of tubes is connected via a small 0.1 in. diam coaxial cable to the electronics. The cable carries the dc high voltage to the tubes, and the signal from the tubes to the electronics. The average cable length is 3 m.

SIGNAL CHANNELS

Overview

A block diagram of the electronics of a signal channel is shown in Fig. 2. A signal chain consists of a charge-sensitive preamplifier, a shaping amplifier and a sample-and-hold analog module (SHAM). The signals from the latter are multiplexed onto a 12-bit ADC. For triggering, the shaping amplifier provides a "copy" of the signal to a summing amplifier, which produces the analog sum for eight signal channels.

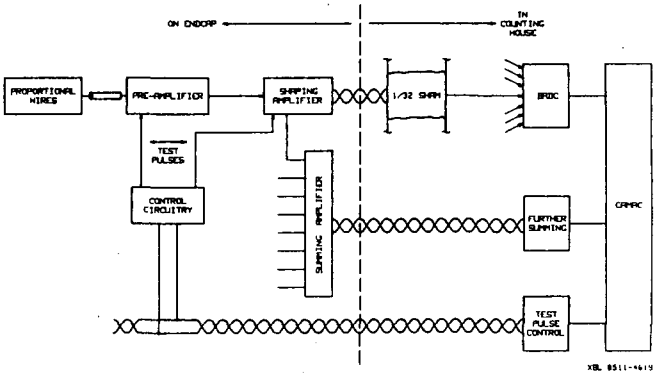


Fig. 2. Block diagram of the system components associated with each signal channel.

Calibration test pulses can be introduced into any combination of selected channels at the preamplifier inputs; test pulses can also be applied at shaping amplifier inputs for diagnostics. The test pulser system was designed to be able to induce the same charge into all signal channels. During the initial testing of each preamplifier, its test pulse circuitry was calibrated to do this to within 1%. With only this initial adjustment, a resolution of better than $18\%/\sqrt{E}$ was obtained in the first beam test of the calorimeter.

A signal channel has a useful dynamic range of ~ 4000:1. The gain in the channel is set such that a signal of maximum amplitude is near full scale within the dynamic range. In implementing the projective geometry, the proportional tubes were divided into three sets. In each set, the groups contain the same number

of tubes. For two sets--at the front and back of the detector--the collected charge per track is nearly the same for all groups of the set. For these, the sensitivity is set to 175 pC/v. For the third set--in the middle--the sensitivity is set to 87 pC/v.

Preamplifier

A diagram of the preamplifier is shown in Fig. 3. It is a conventional charge-sensitive preamplifier with an FET input stage. The differentiation time constant is 120 μs with no detector capacitor. Design parameters include a 40:1 signal/noise ratio for minimum ionizing particles and a gain stability of 0.01% per °C.

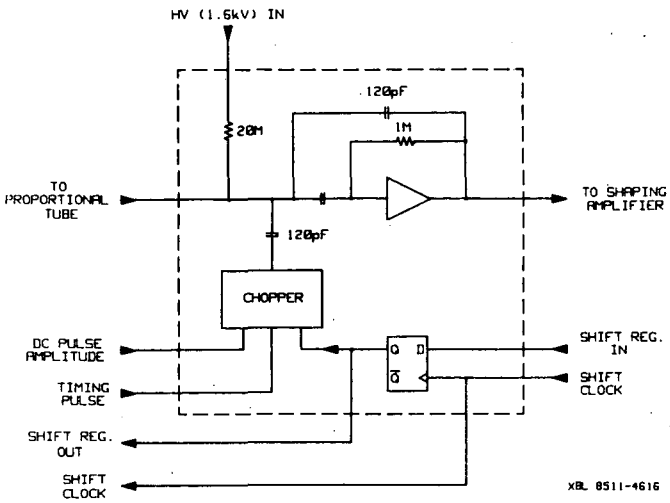


Fig. 3. Simplified diagram of a preamplifier. The chopper generates calibration pulses.

Shaping Amplifier

The shaping amplifier circuitry is shown in Fig. 4. It consists of an operational amplifier followed by a buffer of unity gain. Together with the preamplifier, it generates standardized pulse shapes from the proportional tube signals.

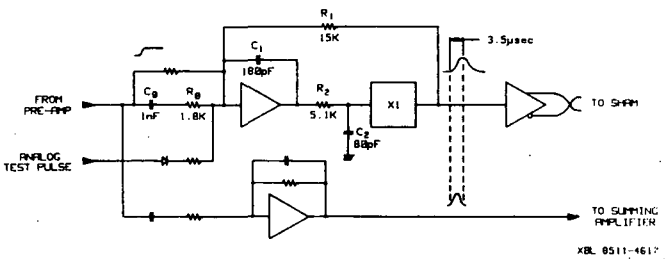


Fig. 4. Simplified diagram of a shaping amplifier.

With respect to a beam crossover, the arrival of primary electrons at a proportional tube wire can vary by up to ~ 200 ns, according to whether the particle track intersects a wire or a side of the proportional tube. However, the digitizer samples (with a 50 ns time jitter) the signal from the shaping amplifier at a fixed time with respect to crossover. To accomodate this uncertainty and to allow for the sampling time of the digitizer, the shaping amplifier must deliver a pulse shape whose peak amplitude is constant to within 1% for 250 ns.

This requirement is satisfied by providing a semi-Gaussian pulse shaping in each signal channel, with a peaking time of 3.5 μs. To effect this, the impulse response of the combined preamplifier and shaping amplifier is designed to be:

$$H(t) = K \left[Le^{-At} - Me^{-Bt} \cos(Ct + \phi) \right]$$

where

$$A = \frac{1}{R_o C_o}$$

$$B = \frac{1}{2 R_2 C_2}$$

$$C = -B \sqrt{\frac{4R_2 C_2}{R_1 C_1} - 1}$$

$$\phi = \tan^{-1} \frac{A-B}{C}$$

$$L = \frac{1}{A^2 + B^2 + C^2 - 2AB}$$

$$M = \frac{1}{\sqrt{4C^2 + 4C^2 (A-B)^2}}$$

and t = time relative to beam crossover.

When the values for Rs and Cs shown in Fig. 3 and 4 are substituted in this equation, it is found that the waveform peaks at t = 3.5 μs. Also, the peak is broad enough that the amplitude is constant to within 1% for 600 ns near t = 3.5 μs. The result is that the charge deposited by a track is digitized to within 1% regardless of the position of the track within a proportional tube. The broad peak also allows for the 50 ns sampling window of the SHAM digitizer.

Summing Amplifier

The summing amplifier generates an output proportional to the sum of summing signals from eight shaping amplifiers. These outputs are further summed as necessary to develop an energy-sensitive trigger.

Digitization

Output signal pulses from the shaping amplifiers are digitized by a CAMAC-based system described elsewhere.[1] The heights of the pulses are captured by a 32-channel SHAM. The stored pulse-heights in all SHAMs in a crate are multiplexed into an analog-to-digital converter module (BADC).

Calibration System

An important design requirement was that the calibration system be capable of determining the relative gain of signal channels to a 1% accuracy. Since this calorimeter is built of proportional tubes, there was

no practical way of including a calibration system in the physical detector. Instead, an individual calibration test pulser based on an FET chopper was incorporated in each preamplifier. In a test stand, each such calibration test pulser is itself calibrated to inject standard values of charge into each channel to within 1%.

Calibration pulses are generated by an FET chopper. The amplitude of the pulses is controlled by a dc voltage, labelled "DC Pulse Amplitude" in Fig. 3. The chopper is enabled or disabled by a control signal from one bit of the 8-bit shift register shared by seven other preamplifier cards. If enabled, the chopper forces a charge signal on the preamplifier input on command of the Timing Pulse. Design parameters for the calibration include a 0.5% stability over time and a resolution of 1%.

CONSTRUCTION

The physical partitioning of system components was dictated by a typical tradeoff. On the one hand, for noise considerations, amplifier inputs should be close to the chambers; this puts them in an area that is inaccessible while the beams are colliding. On the other hand, one is concerned about the effects of failures in equipment that can be serviced only when the beam is down. To alleviate this concern, the system designer: 1) puts as many components as possible in inhabitable areas, and 2) takes care to reduce the scope of the effect of a component failure in the inaccessible equipment. In addition, he provides diagnostic tools to help identify the location of faults so that maintenance time is minimized—particularly maintenance time that reduces beam time.

In view of these factors, the preamplifiers, shaping amplifiers and summing amplifiers are physically located on the endcap doors, with a max of about 4 m of cable between the preamplifier input and the chamber tubes to which it is connected. These three types of amplifiers were each constructed on individual, plug-in, printed circuit cards about 1 x 4 in. (see Fig. 8). They are supported on "mother-boards". A mother board has a capacity of 32 channels--32 each of preamplifiers and shaping amplifiers, and four summing amplifiers. It also contains the calibration pulse circuitry that is common to a group of 32 channels. The mother boards also distribute the high voltage to groups of 16 preamplifier inputs (and thus to the chambers). Each group of 16 is isolated by a 20 MΩ resistor.

Mother boards are, in turn, supported by crates--each crate having a capacity of 16 mother boards. A crate also contains calibration pulse circuitry that is common to 16 mother boards.

CALIBRATION SYSTEM

Large-scale detector facilities require a self-test capability. Faults will inevitably develop in systems that have thousands of individual signal channels and the ability to detect a faulty channel is essential. Also, the stability requirements and the costs of signal channels are lowered if the ability to frequently calibrate individual channels is provided.

In the MARK II End Cap Calorimeter, these requirements are satisfied by a calibration system that can inject test pulses into the preamplifiers or into the shaping amplifiers. The amplitudes of these pulses and the channels which receive the pulses are both computer controlled.

Physical Partition

The parts of the calibration system are distributed. The actual test pulse is generated on the preamplifier card with a level set by a DAC on the mother-board. The DAC level is set by a CAMAC calibration controller in the electronics house, which is 200 ft from the end cap.

The test pulse is generated on the preamplifier card with an FET chopper and a flip-flop that enables or disables the chopper as shown in Fig. 3. In order to take into account tolerance on the value of the calibration capacitor, an adjustment is provided which is set during the initial preamplifier testing so that each channel receives the same charge for a given test pulse amplitude.

Individual flip-flops on the preamplifier cards are connected into eight-bit shift registers, as shown in Fig. 5a. Each mother board has four such shift registers. Each mother board also has a digital-to-analog converter (DAC) that drives the DC Pulse Amplitude bus which delivers a dc level to all FET choppers on a mother board. The mother board also distributes the Timing Pulse to the chopper on each preamplifier card.

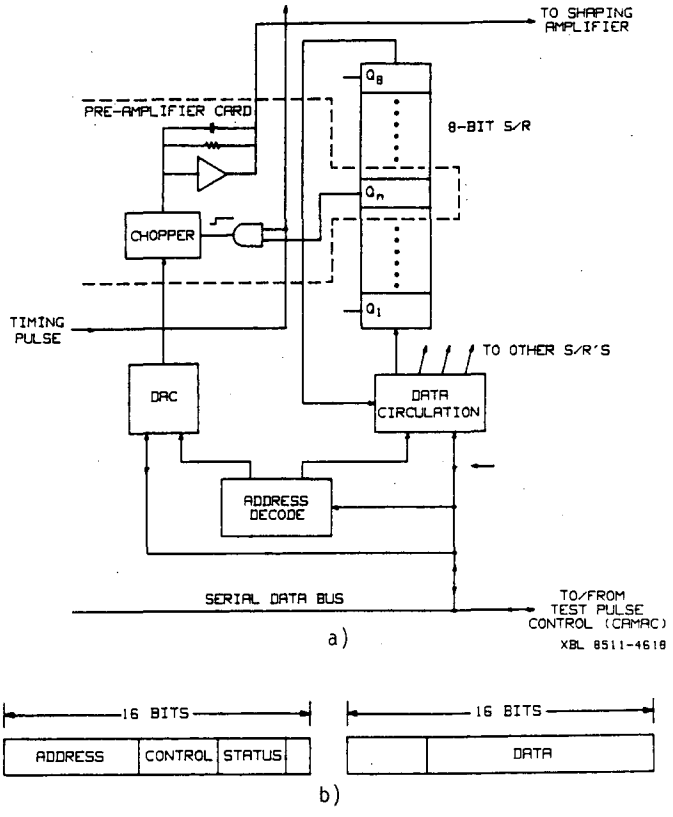


Fig. 5. a) Block diagram of the test pulser system.
b) Format of data on the bit-serial bus.

Operation

All mother boards can receive data or transmit data on a bit-serial bus. This bus carries data and command information between the mother boards and the CAMAC control module. The data are transmitted differentially from the CAMAC control module to a receiver board in each crate which busses the data on the crate backplane. The format of the data transmitted on the

serial bus is shown in Fig. 5b. Each transmission consists of two 16-bit words. The first word, the Address-Control-Status word, has an eight-bit address field which uniquely identifies every eight-bit shift register in the system, a three-bit control field which sets the direction of data flow and the kind of operation being performed, and a three-bit status field which reports errors. The second word is the DAC or Shift-Register Data word, with 12 bits used for data to/from a DAC register and eight bits to/from a shift register.

Each DAC and each eight-bit shift register in the system has a unique address on the serial bus. Under computer control, 12-bit data words can be loaded into the DAC on any mother board, controlling the amplitude of the calibration pulses generated on that mother board. For checking, the data word can be read back from the DAC register to the CAMAC module.

Also, under computer control, eight-bit data words (test-pulse masking patterns) can be loaded into any addressed shift register. These data words can also be read back for checking. With appropriate Address-Control-Status and data words, any control flip-flop on any preamplifier card can be set or reset. The associated FET chopper is thus enabled or disabled, controlling whether charge is injected into its preamplifier in response to the timing pulse. The amplitude of the test pulse on each mother board can also be set, resulting in a very flexible system in which any pattern of channels can be pulsed with controllable amplitude.

In the normal operation of the detector, a standardized calibration is done about every eight hours. This calibration pulses all the channels in the system in various combinations and reads back the digitized data in exactly the same way as data are normally acquired. The response of each channel as a function of DAC amplitude is measured and the result is fit to a quadratic function. Constants are calculated which are used to correct each data word acquired during operation. Also, various criteria are applied to the calibration data and then fit to determine that the channel is behaving normally. For example, the gain must fall within specified tolerances and the variation of the measured amplitude must not vary too much from pulse to pulse. A typical calibration consists of 200 test "events" with 10 amplitudes and takes about one min for data acquisition and fitting for 2552 channels. The results of the calibration are available to the operator in several forms, from a simple good-or-bad answer to plots of the data and the fit and residuals. Figure 6 is an example of a plot of the data and residuals which is available in real time for each channel. Often the information provided by the calibration is sufficient to identify a faulty component in the system.

TEST STANDS

This project required the construction of a large number of individual components--2800 preamplifiers, 2800 amplifiers and 350 summing amplifiers. In such a situation, the use of automated test stands is strongly indicated. Accordingly, two computer-operated test stands were designed and built, one for the preamplifiers and one for the amplifiers. A third manually operated test stand was built for the summing amplifiers. In the following, the preamplifier test stand is described as an example.

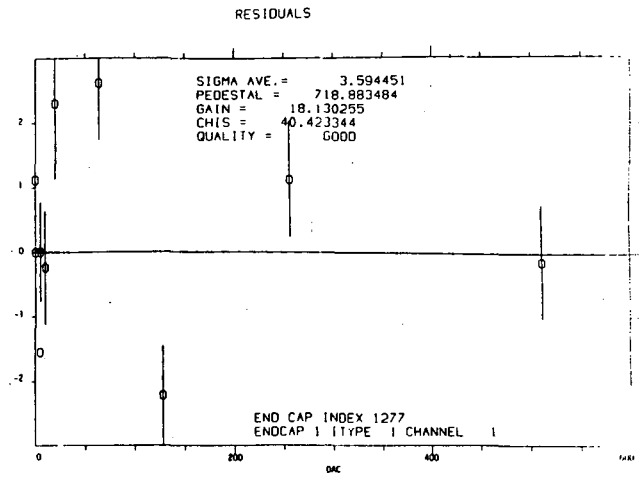


Fig. 6. Example of online plot of residuals from linear fit available for each channel.

Automated test stands

The two automated test stands are based on an IBM Personal Computer (PC). Two components were added to the basic PC to implement a test station—an interface board that plugs into the PC chassis and a tester module. A photograph of a test module is shown in Fig. 7. It features a zero-insertion-force socket for accepting the card under test. The tester module shown in the figure tests preamplifier cards; the interlocked cover is closed for safety while high-voltage tests are going on.

Tests performed

For each preamplifier, the test stand checks the following parameters. Test limits are given in parentheses.

* Current drawn from the ± 12 V power supplies (within 20% of the nominal value)
* Leakage current from the 3 kV power supply (< 1 μA)
* Output pulse shape (chi-squared of fit to reference pulse shape < 5)
* Gain (within 7% of nominal value)
* Gain linearity (maximum deviation from straight-line fit < .4%)
* Output pulse rise time (< 150 ns)
* Output pulse fall time (> 20 μs)
* Noise at output--high voltage off (< 0.5 mV rms)
* Noise due to high voltage (< 50 mV peak)
* FET transconductance (within 60% of nominal)
* Flip-flop read back (within normal TTL specs)

In addition, the calibration pulser on each preamplifier card is normalized with a potentiometer so that a standard charge is injected into the preamplifier input for a defined dc voltage input to the chopper circuitry.

Block diagram

The principal components of the test stand are shown in Fig. 8. The signal paths and other conditions for each test are selected by computer controlled devices--relays, DACs, etc. The computer also selects an

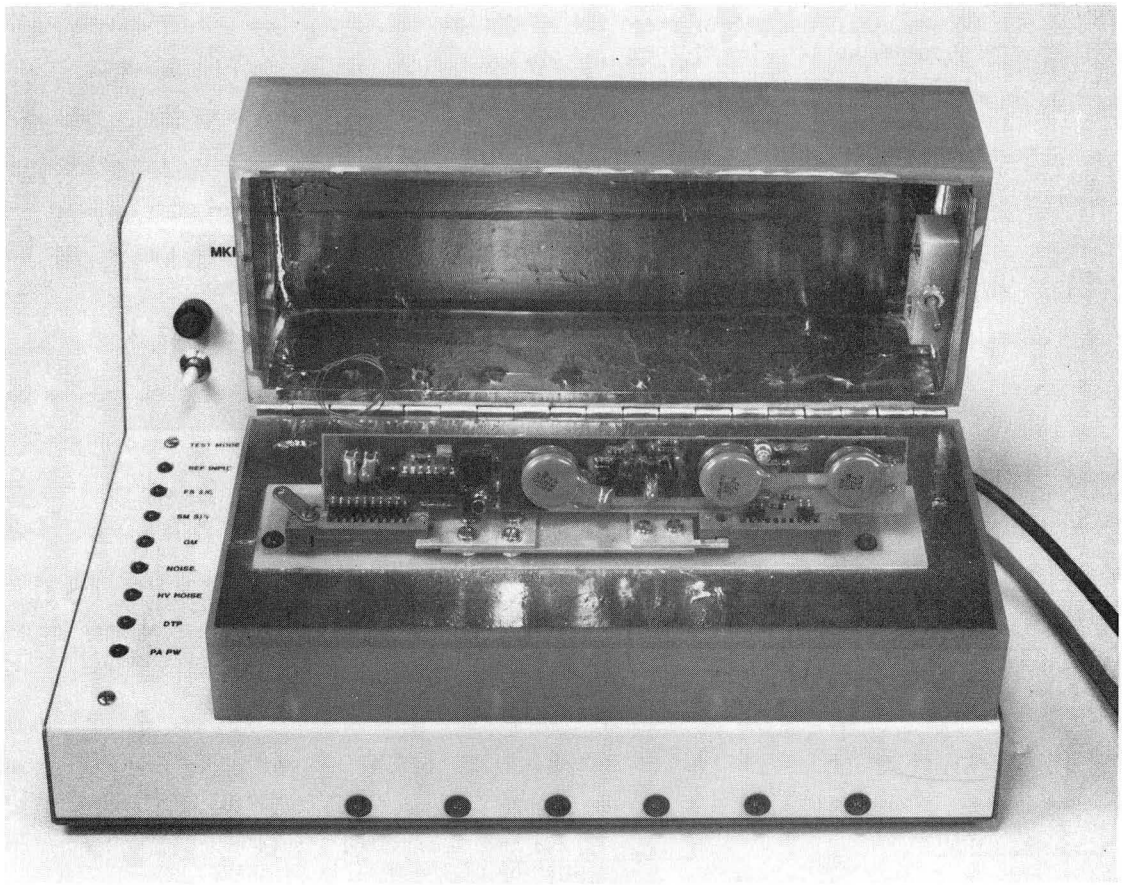


Fig. 7. Photograph of the test module of a test stand. A preamplifier card is in place for testing. The shielded cover is closed for high voltage tests.

appropriate signal to monitor. All such signals are analog in nature. Some of the tests--monitoring power supply voltages, for example--can be made by measuring simple dc values.

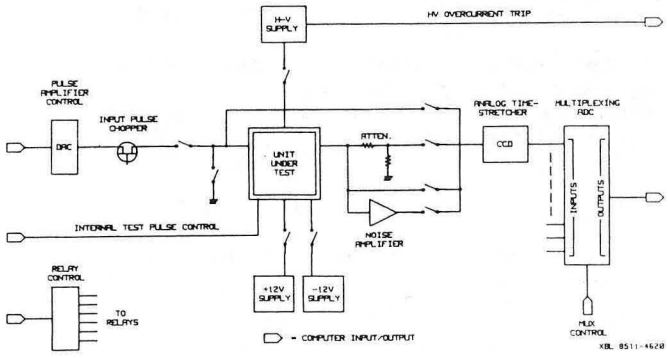
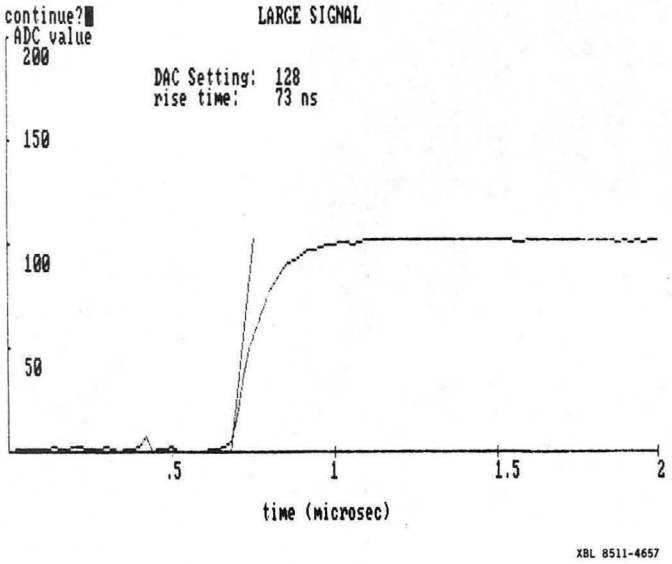


Fig. 8. Block diagram of a computer-operated test stand.

Other tests--pulse shape tests, for example--require analysis of the time structure of signals. In such cases, a charge-coupled-device (CCD) is used to acquire and store 455 analog samples of a pulse at a 10 MHz rate. The samples are subsequently read out of the CCD at a slower rate, and individually digitized. The results of the digitizations are then available to the software used in time response, gain, linearity, transconductance and noise tests. In addition, four 20 ns delay units, residing on the interface board, can be used to provide an effective sampling rate of 50 MHz. This finer time resolution is applied in the measurement of rise times. The use of a CCD introduces some non-linearity in the signal measurement which is calibrated and corrected for in software.

All programming for the IBM PC was done in compiled BASIC. The system is designed to be usable by relatively unskilled personnel. The user plugs a preamplifier card into the module, then pushes the indicated key to start the test. After he enters the serial number of the card, the process proceeds independently, executing the series of tests in automatic sequence. Only the last test--normalization of the calibration pulser on the card--requires manual intervention. In this process the operator is required to adjust a potentiometer on the card. He is given a graphical display on the PC screen indicating which direction the potentiometer should be turned. The PC responds with a tone when the adjustment is complete. At the conclusion of the test sequence, a printed report is generated. The complete series of tests requires ~ 1 min per preamplifier card.

Additional diagnostic options are available to the more expert user, including graphical displays of the measured signals. Figure 9 shows two examples of the graphical output generated by the tester program. Figure 9a is an example of the digitized output signal from the amplifier; Fig. 9b shows a linearity plot for a preamplifier.



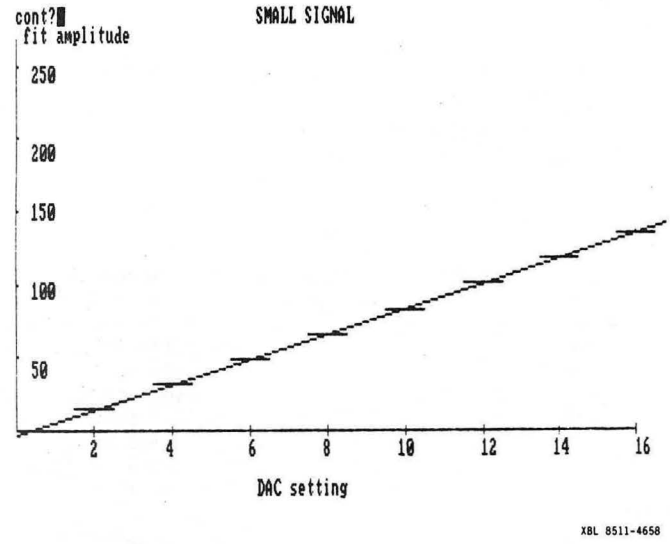


Fig. 9. Computer-generated plots from the preamplifier test stand. a) Output waveform. b) Output linearity.

RESULTS

The End Cap Calorimeter was tested in a 3-15 GeV positron beam at SLAC. The beam scanned a limited region of the end cap and about 40% of the channels were instrumented. Several different gas mixtures were tried, and the high voltage was varied so that the proportional gain was varied by a factor of 100. The resolution and linearity were studied as a function of gain, as shown in Fig. 10, for example.

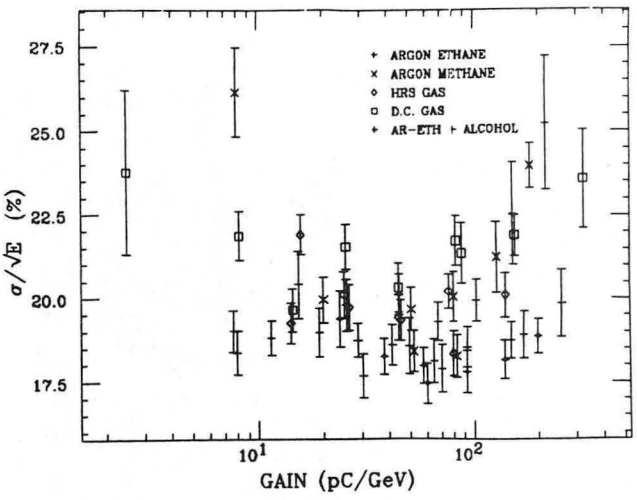


Fig. 10. Measured resolution as a function of proportional gain in the calorimeter. Note that the measured charge has not been corrected for the charge collection time of the shaping amplifier.

We found a minimum resolution of about $18\%/\sqrt{E}$. This agrees well with the design goals of the system and complements the liquid argon calorimeter in the barrel of the MARK II detector.

ACKNOWLEDGMENTS

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1. E.L. Cisneros, et al, Drift Chamber and Pulse Height Readout Systems Using Analog Multiplexing, IEEE Trans. Nucl. Sci., NS-24, No. 1, 413-418 (1977).

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