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***Abstract*—The conventional dc-link aluminum electrolytic capacitor bank simply, efficiently, and cost-effectively decouples the instantaneous power mismatch inherent to all single-phase ac-dc power converters. However, the practical realization of the capacitor bank remains largely qualitative and dependent on the opaque performance capabilities of the capacitor technology. This work presents an exhaustive survey of commercial aluminum electrolytic capacitors and defines both quantitative and justly comparative device-level figures-of-merit (FOM). By configuring the relative voltage ripple ratio specification α of the dc bus, these device FOM enable the determination of minimal dc-link capacitor volume, cost, and/or mass. Graphical illustration demonstrates that the set of commercially available yet viable components diminishes as specification α increases; the realized dc-link capacitor bank volume and cost will grow appreciably for $\alpha > 10\,\%$ and $\alpha > 5\,\%$, respectively.**

***Index Terms*—Single-phase dc-link, twice-line frequency power decoupling, dc-link capacitor, capacitor survey, aluminum electrolytic capacitor, device figure-of-merit.**

I. Introduction

SINGLE-PHASE (ac-dc or dc-ac) electric power converters have a fundamental discrepancy between the instantaneous dc power and the instantaneous ac power pulsating at twice the ac line frequency. The most common solution is an aptly named 'dc-link' capacitor tied in parallel across the dc bus of the converter. For sufficiently large capacitance C, this capacitor can decouple much of the ac power fluctuations from the dc port of the system.

Aluminum electrolytic capacitors in particular serve as an excellent choice for buffering in single-phase applications at low distribution voltages (50–1000 V) as they are manufactured in the largest capacitance denominations near the required voltage ratings as shown in Fig. 1; exhibit minimal losses (ESR) at grid frequencies [**?**]; maintain high energy density by both volume and mass [**?**]; and remain commercially competitive with low cost per unit energy [**?**]. However, the technology also has lower rms current rating resulting in relatively poor reliability and lifetime [**?**].

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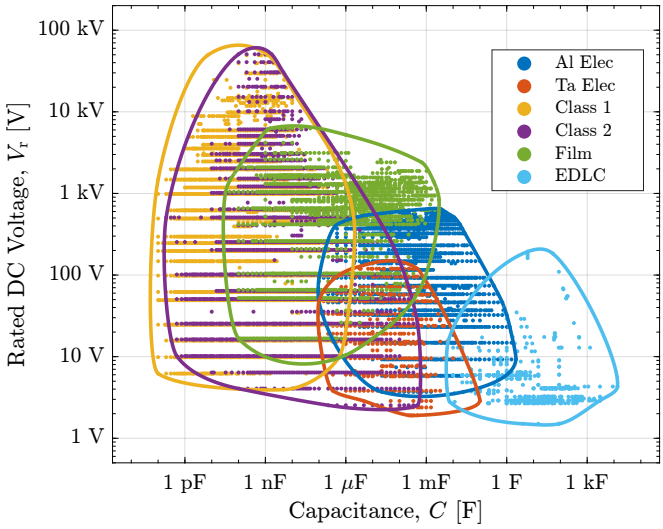

Fig. 1. Survey of component rated capacitance C versus rated dc voltage V_r across all major capacitor technologies including aluminum electrolytic, tantalum electrolytic, Class 1 ceramic, Class 2 ceramic, film, and electrolytic double-layer capacitors (EDLC).

This work aggregates a comprehensive breadth of presently commercially available aluminum electrolytic capacitors [**?**], introduces and motivates several useful device figures-of-merit (FOM), and applies these metrics to single-phase dc-link design. The results reveal the performance limitations of aluminum electrolytic capacitors for this application and yield quantifiable engineering insight.

II. Defining Performance Metrics

Exhaustive data aggregation and robust FOM are both required to characterize the actual performance limitations of dc-link capacitors and relate them to the single-phase application.

A. Internally Derived Characteristics

One approach to comprehensive device characterization is to assess internal properties and relate them to the macroscopic device performance or FOM [**?**]. Consider the aluminum electrolytic capacitor conventionally modeled with the circuit shown in Fig. 2; loss and leakage characteristics are captured with a lumped series R_s and parallel R_p parasitic resistance. At any particular frequency, these resistances jointly contribute to an equivalent series resistance ESR.

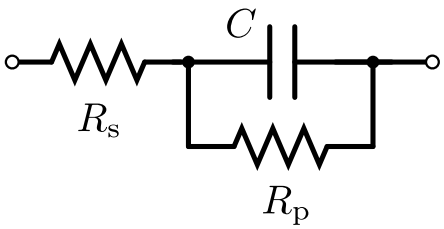

Fig. 2. Conventional capacitor lumped circuit model including primary loss and leakage parasitics.

Within the capacitor, reducing plate separation increases the capacitance C and decreases the ESR and volume, but the worsened breakdown threshold of the thinner dielectric reduces the rated voltage V_r. Increasing the effective plate area also increases capacitance C and decreases ESR, but subsequently increases the volume. Larger volume and lower ESR both generally correlate to an increased rated current I_r. Internal design trade-offs influence realizable FOM and several of these trends have been explored for aluminum electrolytic capacitors in prior literature [**?**], [**?**].

B. Externally Derived Characteristics

The internal device characterization approach is limited since each capacitor is unique, and internal specifications are difficult to ascertain. Device performance is better determined by utilizing a component survey that externally considers all possible commercially viable capacitor variants. Additionally, an accurate assessment of trends is only possible by investigating the entire breadth of the capacitor technology. Consequently, this work aggregates all aluminum electrolytic capacitors which are available for purchase from the prominent distributor Digi-Key Electronics. In total, the data extensively surveys nearly 29,000 unique capacitors produced by twenty distinct manufacturers and thus represents the entire component technology in aggregate.

C. Robust FOM

Before considering the essential attributes of a valuable capacitor FOM, consider first how whole power converters are benchmarked. A comparative study of power conversion systems necessitates FOM with invariance to series and parallel configurations; conventional examples include input-to-output efficiency, volumetric and gravimetric power density, loss density, and relative power per cost. All realizable values for these metrics form a feasible range of performance—or performance space—for power converters and are used to ultimately identify trade-offs and inform design [**?**]. One viable technique—Monte-Carlo optimization—has been utilized to identify the feasible performance space for the dc-link capacitor and several active buffering alternatives within the full single-phase conversion system [**?**].

Series and parallel modular invariance should also apply to device-scale FOM. Capacitors connected in series effectively increase the voltage rating of the capacitor bank, and likewise paralleled configurations increase the current rating. To adequately relate physical capacitors of various capacitance, voltage, current, volume, mass, and cost, all comparative metrics must be agnostic with respect to bank configurations of parallel and/or series connected components. For example, a bank configured as ten parallel branches of two series-connected capacitors each (i.e., twenty total capacitors) should have the same overall FOM as a single constituent capacitor.

In this work, three series-parallel invariant and easily calculable figures-of-merit are derived from base component metrics of rated (peak) voltage V_r, rated (rms) current I_r, capacitance C, box volume, and cost [**?**]:

1) Volumetric dc energy density $\rightarrow \gamma_v = \frac{E_r}{\text{Vol}}$
   - The rated 'released energy' E_r from rated dc voltage to zero is defined as $E_r = \frac{1}{2}CV_r^2$ for a linear voltage-independent capacitance [**?**], [**?**], [**?**].
2) Volumetric power density $\rightarrow \rho_v = \frac{P_r}{\text{Vol}}$
   - The rated power P_r is defined as $P_r = V_r I_r$ at the rated peak voltage and rated rms current [**?**].
3) Energy per unit cost $\rightarrow \gamma_c = \frac{E_r}{\text{Cost}}$
   - The per unit cost is defined as a single-unit cost rather than widely varying bulk component pricing.

This work defines the rated power $P_r = V_r I_r$ at the conditions maximizing leakage current and at the same operating conditions where the rated current I_r is specified—at rated voltage with a sinusoidal excitation at a specified frequency. Additionally, the rated rms current I_r depends heavily on the equivalent series resistance ESR of the capacitor and it is not a hard upper limit but rather a rating which guarantees a particular lifetime at rated voltage V_r and temperature [**?**]. This particular definition for power rating derives from both its computational simplicity and the deficiencies in the surveyed data.

The presented energy and power density device-level FOM—γ_v, ρ_v, and γ_c—are not immediately useful until they can be connected to the capacitor's application. The following analysis relates these FOM to the energy and power requirements of the single-phase dc-link application.

III. Constraining the DC-Link Capacitor

Consider the general single-phase system with dc-link capacitor in Fig. 3. The dc-link capacitor is quantifiably constrained with respect to its energy and power requirements.

A. Single-Phase Buffering Requirement

To fully decouple the instantaneous power difference between the ac and dc ports, a fundamental peak energy E_{buf} must be buffered within a quarter of each line cycle

$$E_{buf} = \frac{P_o}{\omega_g} \tag{1}$$

where P_o is the system apparent power rating and ω_g is the angular frequency of the ac line [**?**], [**?**].

Assuming the dc-link capacitor buffers the entire energy requirement in (1), a design relationship between capacitance C and peak-to-peak dc bus (i.e., capacitor) voltage ripple ΔV_{dc} can be derived for particular system specifications:

$$E_{buf} = \frac{1}{2}C\,V_{C,max}^2 - \frac{1}{2}C\,V_{C,min}^2 = C\,V_{dc}\,\Delta V_{dc} \tag{2}$$

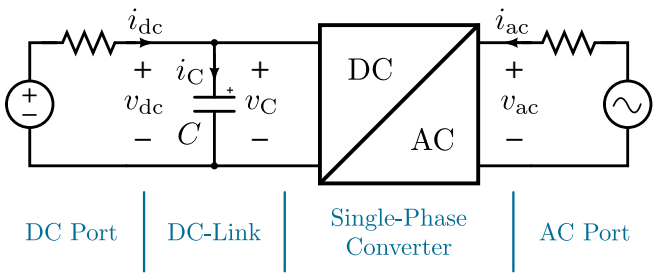

Fig. 3. Circuit diagram of of dc-link capacitor in a single-phase power conversion system.

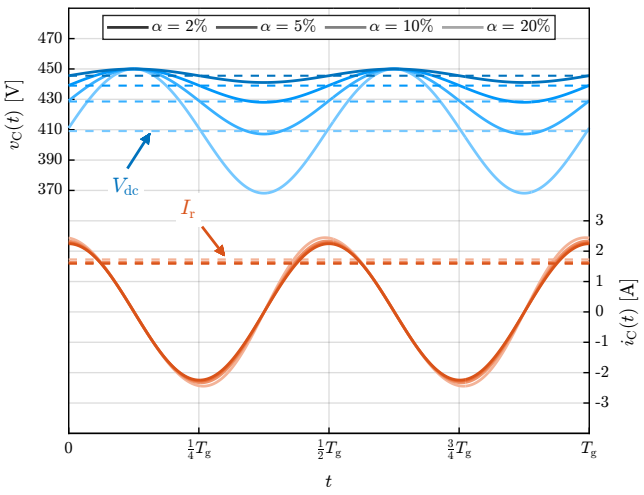

Fig. 4. Dc-link capacitor voltage and current waveforms across one full line cycle with period T_g and with increasing specification of dc bus voltage ripple ratio α. As the ripple ratio increases, the capacitor is constrained with the same rated voltage V_r and a decreasing average bus voltage V_{dc}.

where V_{dc} is the dc bus voltage and the midrange average of the fluctuating capacitor voltage [**?**], [**?**].

A pertinent design specification is the bus voltage ripple ratio

$$\alpha := \frac{\Delta V_{dc}}{V_{dc}} \tag{3}$$

where limits are typically constrained by the source/load of the single-phase converter system. A photovoltaic (PV) panel can tolerate values up to roughly $\alpha = 10\,\%$ on the dc port before a significant degradation in the delivery of the maximum available power [**?**], [**?**].

Fig. 4 illustrates the instantaneous voltage $v_C(t)$ and current $i_C(t)$ of the dc-link capacitor across a full ac line cycle. The peak instantaneous capacitor voltage $V_{C,max}$ and system power P_o are constrained while the ripple ratio α (and thus capacitance C) is varied for an approximate $400\,V$, $1\,kW$ application. Additionally, in the small ripple approximation (i.e., $\alpha < 10\,\%$), the instantaneous capacitor or dc port voltage is analytically expressed as

$$v_{dc}(t) = v_C(t) \approx V_{dc} + \frac{1}{2}\Delta V_{dc}\cos(2\omega_g t) \tag{4}$$

with a dc component and a sinusoidal ripple at twice the line frequency.

B. Energy Rating

A link between the capacitor's rated dc energy E_r and the required buffering energy E_{buf} must be determined to relate the rated energy density γ_v or γ_c of the component to its application.

If the peak instantaneous capacitor voltage is constrained to its rated voltage $V_{C,max} = V_r$ as shown in Fig. 4, then the dc bus voltage V_{dc} is alternatively expressed as

$$V_{dc} = V_r - \frac{1}{2}\Delta V_{dc} = (1 - \frac{1}{2}\beta)\, V_r. \tag{5}$$

where an intermediate ripple variable β is defined

$$\beta := \frac{\Delta V_{dc}}{V_r} = \frac{2\alpha}{(2+\alpha)} \tag{6}$$

and incidentally forms a bijective function with the ripple ratio α. By substituting (5) and (6), the buffered energy E_{buf} in (2) is identified as linearly proportional to the capacitor rated energy metric E_r:

$$E_{buf} = (2-\beta)\,\beta \cdot \left(\frac{1}{2} C\, V_r^2\right) = \frac{8\alpha}{(2+\alpha)^2} E_r. \tag{7}$$

For a specified α, this expression describes the maximum energy buffering capability of a dc-link capacitor bank with rated energy E_r.

C. Power Rating

Similar to the energy requirements, a capacitor's rated power P_r and the system power rating P_o must be related to utilize the capacitor's power density metric ρ_v.

An expression for the peak-to-peak dc bus voltage ripple ΔV_{dc} of the system is determined by substituting (1) into (2):

$$\Delta V_{dc} = \frac{P_o}{\omega_g C\, V_{dc}}. \tag{8}$$

The instantaneous current $i_C(t)$ through the dc-link capacitor is derived from the small-ripple approximation for voltage $v_C(t)$ in (4)

$$i_C(t) = C\frac{\mathrm{d}}{\mathrm{d}t} v_C(t) \approx \omega_g C\, \Delta V_{dc} \cos(2\omega_g t) \tag{9}$$

which, with (8) substituted, has rated rms current value

$$I_r \approx \frac{1}{\sqrt{2}}\omega_g C\, \Delta V_{dc} = \frac{P_o}{\sqrt{2}\, V_{dc}}. \tag{10}$$

The system power P_o is identified as linearly proportional to the capacitor rated power metric P_r by using (3) and (6) to perform a change of variable from V_{dc} to V_r in (10)

$$P_o = \frac{2\sqrt{2}}{2+\alpha} \cdot (V_r I_r) = \frac{2\sqrt{2}}{2+\alpha} P_r. \tag{11}$$

For a specified α, this expression describes the maximum system power capability for a dc-link capacitor bank with rated power P_r.

D. Energy Versus Power

The single-phase energy buffering requirement E_{buf} and the system power rating P_o are fundamentally related as in (1).

Consequently, (7) and (11) can be substituted and simplified to produce a preferred relationship between the rated energy E_r and rated power P_r of a capacitor

$$P_\mathrm{r} = \frac{4\alpha}{\sqrt{2}\,(\alpha+2)}\omega_\mathrm{g} E_\mathrm{r} = kE_\mathrm{r}. \tag{12}$$

A capacitor or bank of capacitors lying on this contour will have an rms current rating I_r perfectly suited to its voltage rating V_r and capacitance C for a specified dc voltage ripple ratio α. However, capacitor solutions with rated power $P_\mathrm{r} > kE_\mathrm{r}$ will also satisfy the requisite buffering requirements.

Normalizing (12) with respect to volume, cost, or mass yields a minimum constraint between the energy density and power density of a capacitor for the dc-link application. These metrics are series-parallel invariant figures-of-merit and thus can be used to compare all configurations of capacitor banks regardless of individual device voltage or current ratings.

IV. Analysis

The dc-link capacitor constraint derived in (12) between the desired rated energy and power at $2\omega_\mathrm{g}$ frequency can be applied to the entire breadth of surveyed commercially available aluminum electrolytic capacitors.

A. Application to Volume

Fig. 5 presents a large spread of component volumetric energy and power densities, γ_v and ρ_v, computed directly from datasheet specifications. The data set illustrates that the highest performance capacitors—with superior energy and power density in the upper-right quadrant—tend to be those rated for the highest voltages (e.g., $400\,\mathrm{V} \le V_\mathrm{r} \le 630\,\mathrm{V}$) dissuading series configurations of lower voltage rated capacitors and motivating power conversion architectures with high voltage dc-links. The

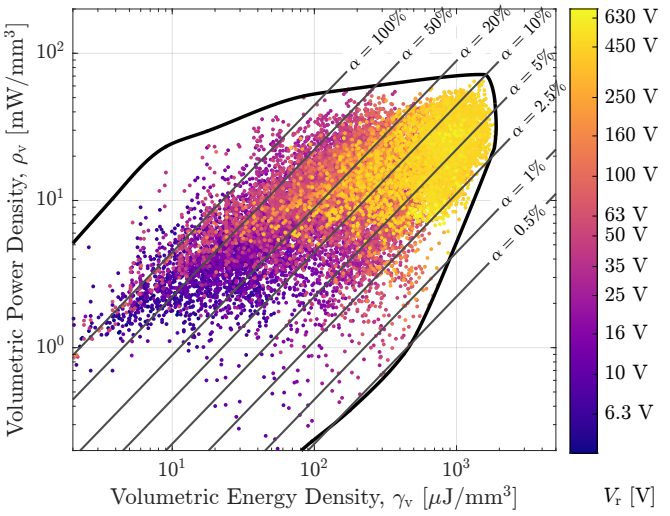

Fig. 5. Volumetric energy density γ_v versus power density ρ_V versus rated dc voltage V_r for all commercially available aluminum electrolytic capacitors. The dc-link capacitor rated energy versus rated power isocline is shown for various ripple ratio α at line frequency $\omega_\mathrm{g} = 2\pi \cdot 60\,\mathrm{rad/s}$. For a specific α, capacitor banks formed with components lying above the isocline satisfy energy buffering requirements.

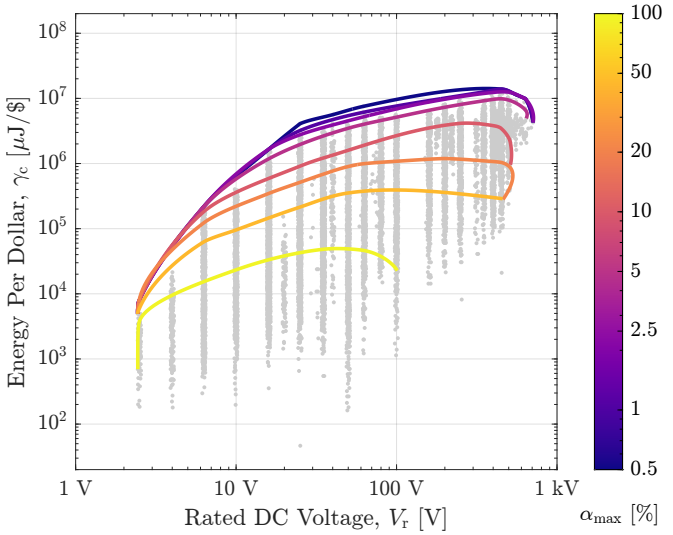

Fig. 6. Rated dc voltage V_r versus energy per unit cost γ_c for all commercially available aluminum electrolytic capacitors. For increasing bus ripple ratio rating α_max, the full data set reduces to only those components satisfying rated energy and power requirements and the best performers in each subset are indicated with Pareto fronts.

energy-power constraint in (12) is superimposed as an isocline for various bus voltage ripple ratio α. For each isocline, all components with simultaneous energy and power density FOM above the contour will satisfy both the energy and power requirements dictated by dc-link twice-line frequency energy buffering. The entire set of isoclines reveal that the pool of applicable highest performance capacitors begins to shrink for $\alpha > 2.5\,\%$. Above $\alpha = 10\,\%$, the realized capacitor bank solution which still meets fundamental requirements will grow significantly in volume since the highest achievable volumetric energy density drops below $\gamma_\mathrm{v} = 150\,\mu\mathrm{J/mm}^3$.

B. Application to Cost

Fig. 6 illustrates the rated dc voltage V_r versus energy per cost FOM γ_c across all commercially available aluminum electrolytic capacitors. Capacitors with relatively high voltage rating (e.g., $V_\mathrm{r} = 450\,\mathrm{V}$) have the lowest costs relative to their rated energy storage capability, and there is a sharp increase in cost for capacitors with rated voltage below $V_\mathrm{r} < 50\,\mathrm{V}$.

In addition to volume, the rated energy-power constraint in (12) also informs the lowest realizable costs for the practical dc-link capacitor bank. The full component data set reduces to a subset with quantitatively lower performance once a desired maximum relative ripple $\alpha = \alpha_\mathrm{max}$ at P_o is specified. As the ripple ratio α on the dc bus increases, the Pareto set of compliant capacitors diminishes, and is dramatically reduced for $\alpha > 5\,\%$. For cost-constrained designs, this insight can narrow the set of viable capacitor choices and aid determination of cost-optimal dc-link capacitor solutions.

V. Conclusion

Design of a dc-link capacitor bank for single-phase applications presently requires a component search based largely on ad hoc procedures, and existing generalizations about

capability (i.e., density, cost, loss) are primarily qualitative. This work presents a set of easily calculable device figures-of-merit—volumetric energy density, volumetric power density, and energy per cost—all with the special property requisite for invariance to arbitrary series or parallel component configurations. An exhaustive survey of commercial aluminum electrolytic capacitors is performed to enable empirical quantitative measures. Additionally, the dc-link capacitor's rated energy and power are analytically related for the single-phase buffering application with respect to the relative voltage ripple ratio α on the dc bus. This analysis supplements visualization of the surveyed data and demonstrates the range of practicable dc-link capacitor solutions. The data reveals meaningful design insights such as unavoidably high volume solutions for bus voltage ripple ratio $\alpha > 10\,\%$ and inevitable high cost solutions for $\alpha > 5\,\%$.

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