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Novel High Efficiency CMOS On-Chip Antenna Structures at Millimeter Waves

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Abstract—In this work, four designs of (Bi)CMOS on-chip antenna (OCA) at 90GHz and 140GHz are shown and compared, aiming at the difficult task of broadside radiation (off the top chip metal surface). A bowtie-shaped slot antenna is fabricated and expected to offer a gain of -1.5dB at 90GHz and 30GHz impedance bandwidth. Another design of slot antenna backed by a cavity, which is fully isolated from the circuits, gives a gain of -2 dB at 140GHz and 5 GHz bandwidth. Additionally, a design of a slot antenna based on an integrated waveguide in (Bi)CMOS showing -1 dB gain is proposed. At last, a proposed E-shaped patch antenna, which only occupies $0.7\text{ mm} \times 0.7\text{ mm}$ area, shows -2 dB gain with 10 GHz bandwidth.

Keywords—on-chip antenna; CMOS; patch antenna; cavity; millimeter wave; slot antenna

I. INTRODUCTION

Thanks to the fast advancement in semiconductor technology, research efforts in radio frequency ICs have started to focus on the millimeter wave (mmWave) spectrum. Meanwhile antennas, usually one of the largest components in a wireless system, have shown the potential to be integrated alongside the mmWave front-end on a single die. On-chip antennas (OCA) could shrink the size of mmWave wireless systems. To integrate with next generation mmWave single-chip radio [1-2], OCAs have the clear advantage over antennas on printed circuit boards (PCBs) in terms of reduction of feed loss due to the absence of long interconnection. For a typical antenna on a PCB, the feed line is so long that the signal of the chip output has to pass through the wirebond/bump, the interconnection layers in chip package and the feed line on board.

However, it is difficult to achieve high efficiency for (Bi)CMOS OCA because of the low resistivity substrate, and for the extremely thin thickness provided for antenna (between M1 and M6, shown in Fig. 1) and area size restriction. Several CMOS OCAs have been studied whose radiation efficiency is always very poor [1, 3]. Others like in [4] propose to increase the gain by covering the whole chip with a lens which needs extra bulky space out of the chip. Meanwhile, the micromachining technique and proton implantation process have been proposed to improve the radiation efficiency by reducing the substrate losses [5-6], but the shielding problem from other circuitry would still remain.

Fig. 1. (a) Cross section (lateral) view of CMOS chip environment with six metal layers over the silicon substrate. (b) Photo of part of chip fabricated including bowtie antenna (from [7]).

One of the major concerns in the integration of OCA is the electromagnetic interference (EMI) resulting from mutual coupling between the antenna and the high frequency front end or other CMOS circuits, that could be significant due to substrate coupling, which could also degrade the proper operating of the integrated antenna. In practice, it is prerequisite to utilize some techniques to reduce the EMI. It should be mentioned that the OCA is not simply a matter of straightforward copy of integrated antennas developed by the process of III-V semiconductor, like GaAs. For instance, through wafer via can be easily realized through the substrate and used as a shield between antenna and circuit in standard GaAs, but not in a standard mainstream silicon process.

In this paper, four different designs of high efficiency antennas, which are all fully on-chip, are demonstrated considering realistic material parameters. The frequency domain HFSS and the time domain solver CST are used for the simulations. Fig. 1(a) illustrates the side (lateral) view of chip environment used in this paper. The silicon substrate has the thickness of $275\text{ }\mu\text{m}$ with the dielectric constant of 11.9 and resistivity of $12.5\text{ }\Omega\cdot\text{cm}$.

II. BOWTIE-SHAPED SLOT ANTENNA

Fig. 1 (b) shows part of the chip photo of a 90GHz fully integrated passive imaging chip including a bowtie-shaped slot antenna connected to an LNA via a CPW line (in collaborator with L. Gilreath and P. Heydari, UC Irvine.) The antenna is placed at M6 and has an area of $1.4\text{ mm} \times 0.9\text{ mm}$ while the whole chip (not shown here) has an area of $1.6\text{ mm} \times 5\text{ mm}$. It is assumed that there is a ground plane below the chip, which

could be realized by a package interconnection layer or by a PCB. According to the antenna pattern in the E and H planes in Fig. 2(b), the peak gain at 90 GHz occurs at the broadside direction ($\theta = 0^\circ$) and it is around -1.5 dB. The 3dB realized gain bandwidth is from 72 GHz to 120 GHz as shown in Fig. 3. However, due to the proximity between the antenna and the circuit, the antenna performance could be greatly affected by interference with the circuit. Since the wave could travel through the substrate, it was observed that the radiation pattern and peak radiation direction are affected by the presence of circuit parts (modeled as a metal plate), when included in the antenna simulation.

Fig. 2. Bowtie antenna. Simulated accepted gain pattern in the E and H-planes.

Fig. 3. Bowtie antenna. Simulated realized and accepted gain at broadside ($\theta = 0^\circ$) versus frequency.

III. CAVITY-BACKED SLOT ANTENNA

The top and side view of a cavity-backed slot antenna are shown in Fig. 4. The cavity is placed under the slot antenna between the bottom metal layer M1 and the top one M6 to enhance the antenna radiation and provide a good isolation between antenna and rest of the chip. The side wall of the cavity, shown in Fig. 4(b), is implemented by connecting the metal layers from M1 to M6 using multiple vias in between. The cavity is designed to resonate at its TE_{110} mode close to 140 GHz. The slot location and size are optimized to achieve high gain around 140GHz. The antenna is fed by a 50 Ω microstrip line. The total antenna area is $1.2\text{mm} \times 0.6\text{mm}$. The width and length of the cavity, the slot width and length, and the slot offset to the center of the cavity are respectively $a = 0.6$ mm, $b = 1.2$ mm, $L_{\text{width}} = 20$ μm , $L_{\text{slot}} = 1$ mm, and $L_{\text{offset}} = 10$ μm .

The gain patterns in the E and H planes are shown in Fig. 5(a). The peak gain is around -1.4 dB. The cavity under the antenna is used to provide good shielding from the circuitry but also limits the operational bandwidth. It can be observed in Fig. 5(b) that the impedance bandwidth is around 5GHz, from

136GHz to 141 GHz. Fig. 5(c) shows the simulated gain versus frequency of the optimized antenna. The peak appears around

Fig. 4. (a) Top view of cavity-backed slot antenna (b) Side (lateral) view.

Fig. 5. Comparison of simulation results of the cavity-backed slot antenna by CST and HFSS (a) E and H-plane gain patterns at 140 GHz; (b) Input reflection coefficient; (c) Accepted gain at broadside ($\theta = 0^\circ$) versus frequency.

141 GHz and the 3dB gain bandwidth is from 136 GHz to 156 GHz.

IV. EXTREMELY FLAT WAVEGUIDE SLOT ANTENNA

Another potential prototype of slot antenna design using an extremely flat waveguide is proposed, with characteristics like ease of fabrication, low cost, weak interference to the nearby circuit components and also completely isolated with the lossy

silicon substrate. The flat waveguide structure is created within a dielectric layer by adding a top metal over the ground plane

Fig. 6. (a) Top view of an extremely flat waveguide slot antenna. (b) Accepted gain and realized gain at broadside ($\theta = 0^\circ$) versus frequency.

and caging the structure with rows of plated vias on either side as was done in [8] at mmWave.

Similar to the cavity-backed slot as Fig. 4(b), the waveguide is realized by M1, M6 and multiple vias in between. As illustrated in Fig. 6(a), it looks like a very flat, short ended and dielectric-filled rectangular waveguide, with highly reduced height compared to the "normal" 2:1 width-height ratio. The waveguide is working with its dominant TE_{10} mode. Since the cutoff frequency of the dominant mode in a rectangular waveguide is independent of the height, the reduced height does not affect the working frequencies of the waveguide but only reduces the impedance of the wave, which strongly affects losses. The open-end of waveguide is matched to a 50 Ω microstrip line with a tapered transition structure.

As shown in Fig. 6, -1 dB broadside gain at 140 GHz is achieved by using a single integrated waveguide slot antenna in the longitudinal direction. However, because of the extremely flatness (height) of waveguide, the bandwidth of this type of antenna is comparably small (around 3 GHz). The total area of antenna is 0.6mm $\times$ 2mm.

V. E-SHAPE PATCH ANTENNA

The E-shaped patch antenna shows wider bandwidth compared with traditional rectangular patch antenna [9]. Two additional slots are introduced at one side of the patch to pull in another resonant frequency in addition to the resonant frequency of rectangular patch. When the two resonant frequencies get close, wider bandwidth could be achieved.

In the design shown in Fig. 7(a), the slot length L_T , slot width L_W and the slot location L_{offset} are optimized in the way such that the two resonant frequencies get close to each other

around 140 GHz. Fig. 7(a) shows the top metal layer of the proposed E-shaped patch antenna, which is on M6 of CMOS structure while M1 is set as ground plane as indicated in Fig. 7(b). Note that the presence of ground plane of the patch at M1 could effectively reduce the electromagnetic interference between antenna and RF front-end by shielding the wave travelling through the silicon substrate. Vias between M1 and M6 could also be introduced close to the patch edges without altering significantly the operation. The antenna is fed by a 50 Ω microstrip line. The width and length of the patch, the slot width and length, and the slot's offset to side of patch are respectively $a = 0.51$ mm, $b = 0.655$ mm, $L_{width} = 37$ μ m, $L_{slot} = 165$ μ m, and $L_{offset} = 110$ μ m. The total antenna area, when including the ground plane, is 0.7 mm $\times$ 0.7 mm.

The accepted gain pattern in the E and H planes of the E-shape patch antenna are shown in Fig. 7(c) and the simulation results are verified by two simulators, CST and HFSS. The results from two solvers are in good agreement. Also, from the plot of input impedance shown in Fig. 7(d), one can observe the two resonances, at 141 GHz and at 146 GHz. The -10 dB reflection impedance bandwidth is around 10 GHz, from 138 GHz to 148 GHz.

Fig. 7. (a) Top view of the E-shape patch antenna fed by a microstrip. (b) Side (lateral) view. (c) Comparison of accepted gain pattern in the E and H planes at 140 GHz, by HFSS and CST. (d) Reflection coefficient by HFSS and CST.

VI. CONCLUSION

Four types of novel on-chip antenna structures based on (Bi)CMOS process are proposed in this study. Numerical simulation by HFSS and CST are utilized to examine the antennas' performance. It should be noted that the cavity-backed slot antenna, flat waveguide slot antenna, and the E-shaped patch antenna all use M1 as ground plane. Therefore, all these designs could reduce the EMI effectively. The E-shape patch antenna shows a greater degree of miniaturization and larger bandwidth.

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REFERENCES

- [1] S. T. Nicolson, A. Tomkins, K. W. Tang *et al.*, "A 1.2 V, 140 GHz receiver with on-die antenna in 65 nm CMOS," in *2008 IEEE Radio Frequency Integrated Circuits Symposium*, Atlanta, GA., 2008, pp. 229-232.
- [2] A. Natarajan, A. Komijani, X. Guan *et al.*, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Transmitter and local LO-path phase shifting," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2807-2819, Dec, 2006.
- [3] Y. P. Zhang, M. Sun, and L. H. Guo, "On-chip antennas for 60-GHz radios in silicon technology," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, pp. 1664-1668, Jul, 2005.
- [4] A. Babakhani, X. Guan, A. Komijani *et al.*, "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2795-2806, Dec, 2006.
- [5] K. T. Chan, A. Chin, Y. D. Lin *et al.*, "Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 11, pp. 487-489, Nov, 2003.
- [6] K. Jeong-Geun, L. Hyung Suk, L. Ho-Seon *et al.*, "60-GHz CPW-fed post-supported patch antenna using micromachining technology," *Microwave and Wireless Components Letters, IEEE*, vol. 15, no. 10, pp. 635-637, 2005.
- [7] S. Pan, L. Gilreath, P. Heydari, and F. Caplino, "Investigation of CMOS on-chip-integrated antenna at millimeter wave," *SRC TECHCON Conference, Paper 4.8, Sept. 2010*.
- [8] D. Deslandes, and K. Wu, "Integrated microstrip and rectangular waveguide in planar form," *Microwave and Wireless Components Letters, IEEE*, vol. 11, no. 2, pp. 68-70, 2002.
- [9] F. Yang, X. Zhang, X. Ye *et al.*, "Wide-band E-shaped patch antennas for wireless communications," *Antennas and Propagation, IEEE Transactions on*, vol. 49, no. 7, pp. 1094-1100, 2002.