UNIVERSITY OF CALIFORNIA SAN DIEGO

Miniaturized Energy Harvesting and Li-Ion Compatible Power Management Solutions for Wearable and IoT Devices in 28nm FDSOI

A dissertation submitted in partial satisfaction of the requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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2018

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Chair

University of California San Diego

2018

DEDICATION

To Mum: Esmat Wahib

To the Memory of Dad: Safwat Moawad Amin

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- S. S. Amin and P. P. Mercier, "A Fully-Integrated Li-ion-Compatible Hybrid 4-Level DC-DC Converter in 28nm FDSOI," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, March 2019.

The dissertation author is the primary investigator and author of the work in these papers.

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ABSTRACT OF THE DISSERTATION

Miniaturized Energy Harvesting and Li-Ion Compatible Power Management Solutions for Wearable and IoT Devices in 28nm FDSOI

by

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Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)
University of California San Diego, 2018
Patrick P. Mercier, Chair

Today, internet of things (IoT) connect the world in way more than we ever thought possible, changing the way we live, work, and interact with each other. Power management has an important role in a successful IoT deployment. Building an efficient, low-cost, and compact power management unit (PMU) becomes a key for enabling remote, long-lived, and small wearable and IoT devices. Thus, this thesis presents miniaturized, efficient, and low cost power management solutions using innovation on both the architecture and circuit level.

The wireless sensor network (WSN) modules of next generation IoT and wearable devices will be implemented on a single system on a chip (SoC) platform that can ultimately combine digital, analog/mixed signal, and RF to provide the highest level of integration and conservation of area. Most of IoT SoC designs will be implemented in FDSOI technology which is available in small geometry processes to merge the benefits of ultra-low power as well as high performance. Accordingly, the proposed power

management solutions for IoT and wearable devices in this thesis, fabricated in 28nm FDSOI to be integrated on the same die as the WSN modules.

Energy harvesting is an essential concept for the future of power management in IoT to enable autonomous operation that doesn't require battery charging or replacement. Thus, the first part of the thesis presents a power management unit that meets the need of small-form-factor net-zero energy systems by aggregating the maximum available power from three different energy sources while simultaneously regulating three output power rails over a wide dynamic load range, while also managing the charging and discharging of a battery, all in a single-stage single-inductor converter. IoT and wearable devices are powered by efficient and durable Li-ion batteries with voltage range 2.8-4.2V. Thus, the second part presents a fully integrated Li-ion compatible hybrid DC-DC converter that meets the needs of small-form-factor IoT while offering superior performance compared to prior-art fully-integrated converters. The challenges of implementing a high-voltage tolerant DC-DC converter with high conversion ratio, using low voltage transistors and poor quality on-chip passives on 28nm FDSOI addressed. The third part presents a miniaturized Li-ion compatible hybrid single-inductor multi-output (H-SIMO) that independently regulates three different output power rails while combining the hybrid topology benefits for compact and efficient implementation. The last part focuses on finding the maximum number of levels and possible multilevel configurations for a given number of capacitors.

Chapter 1

Introduction

Wearable sensors technology and Internet of things (IoT) enable a wide range of health, fitness, personal entertainment, home security, and industrial control applications that bring exceptional benefits and make our life easier. Today billions of wearable sensors and IoT devices are connected on wireless sensor network (WSN) and communicate over the internet, as shown in Figure 1.1, hence, the name "Internet of Things".

Wearable sensors can be embedded into media such as clothing, glasses, or can be worn on the skin as a temporary printed tattoo [1] to enable remote patient monitoring. For example, patient's data such as heart rate, hydration levels, temperature, and blood sugar is collected, processed using advanced signal conditioning and/or machine learning algorithms, and delivered either directly to the user or sent to a physician. Wearable sensors can also enable many other exciting applications, such as location and activity tracking of children to protect them from kidnapping and threats [2]. Mouth guard based salivary sensors [3] can be used for monitoring athlete's lactic acid concentration to give them an alarm when they are reaching exercise limits. In IoT-based smart farming, the farmers can monitor the field conditions from anywhere [4]. A system is built for monitoring the crop field with the help of sensors (light, humidity, temperature, soil moisture, etc.) and automating the irrigation system.

IoT is pushing towards connecting billions of sensors and actuators on wireless sensor network (WSN) [5, 6], improving the way we live, work, and interact with each other. Figure 1.2 shows the number of connected devices from 2012 through 2025. The expected number of connected devices in 2025 is more than 74 Billion. While Figure 1.3 shows the semiconductor market for IoT from 2012 through 2025. The integrated circuit

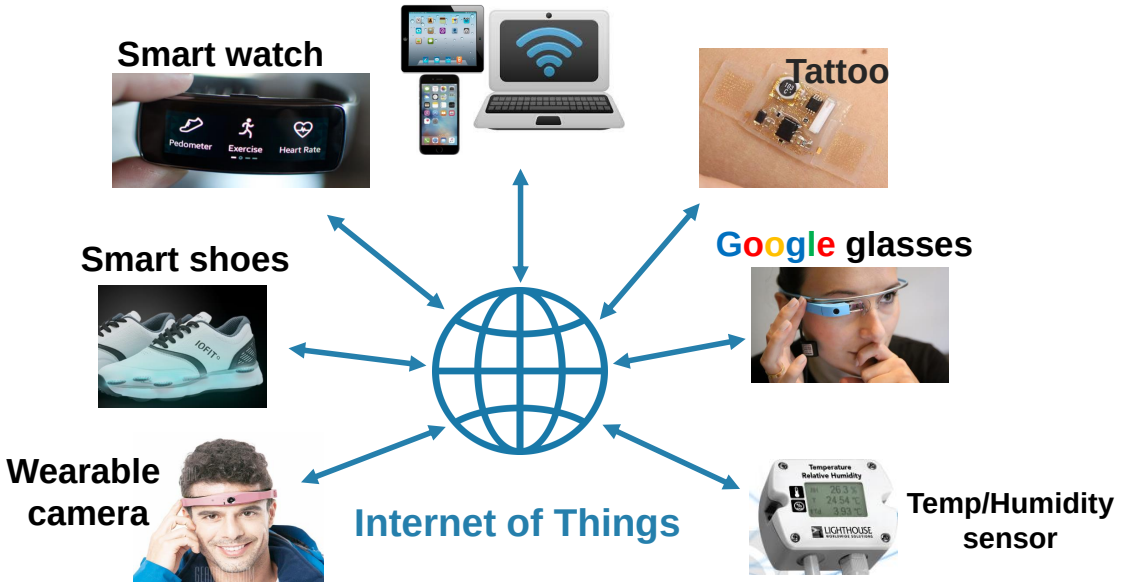

Figure 1.1: Wireless sensor network: wireless sensor devices connected together through the internet.

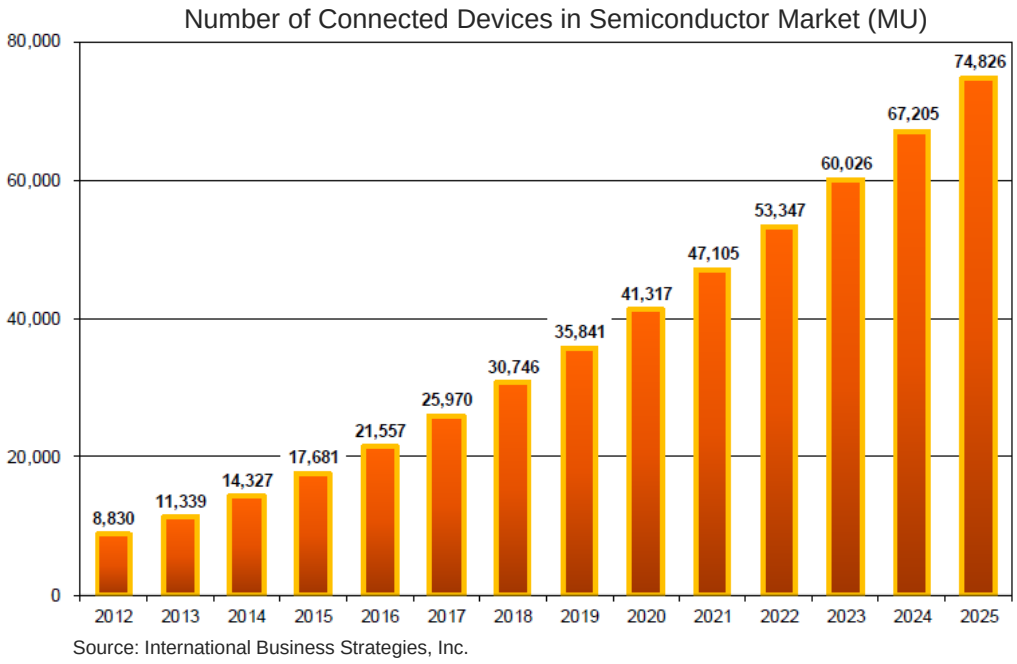

Figure 1.2: Number of connected devices in semiconductor market from 2012 to 2025 showing the growth potential for IoT.

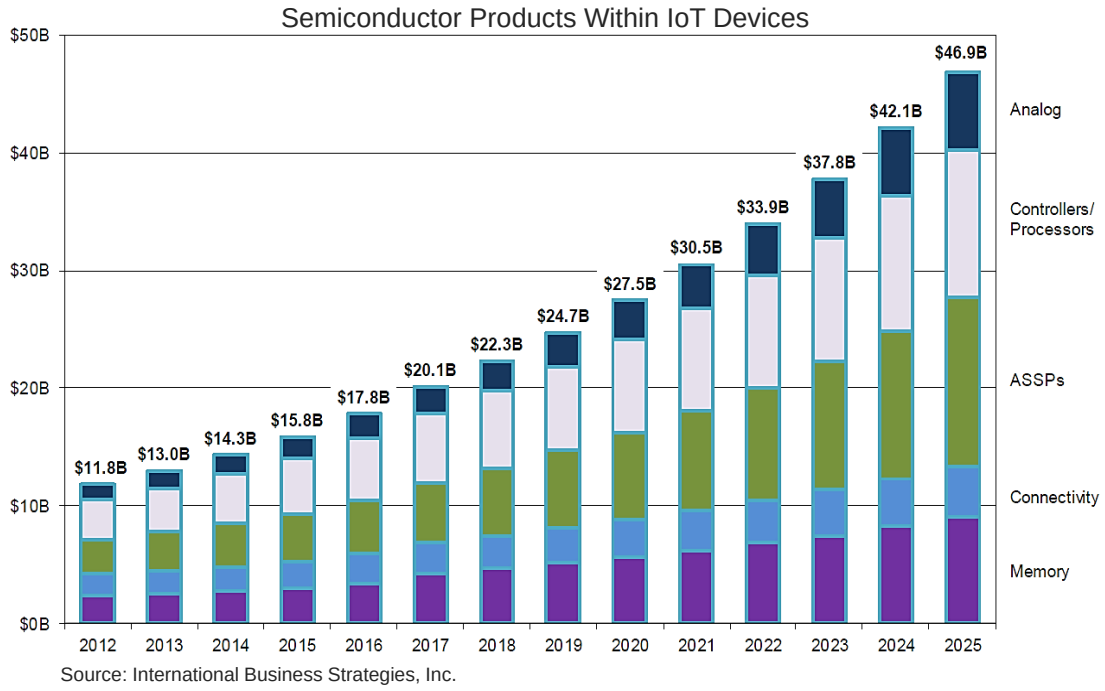

Figure 1.3: Semiconductor market for IoT from 2012 to 2025.

(IC) market for IoT is predicted to be $46.9B in 2025 compared to $11.8B in 2012. While the overall growth of the semiconductor market is expected to be lower than in the past, the semiconductor and sensor markets for IoT will have significantly higher growth than the overall semiconductor market [7].

1.1 IoT Power and Miniaturization Challenge

Despite the exceptional benefits that wearable and IoT devices offer to improve human life, their large size and poor battery life make them undesirable for practical use. Users already complain about having to re-charge batteries of their smart phones and smart watches on a daily basis. As a result, they will not likely tolerate doing this for even a small number of additional devices. The simplest way to improve the battery lifetime is to use larger battery with larger capacity. However, this simple solution is not practical due to the physical size constrain. IoT and Wearable sensor devices need to be small in size, operating from small batteries. On the other hand, in some applications

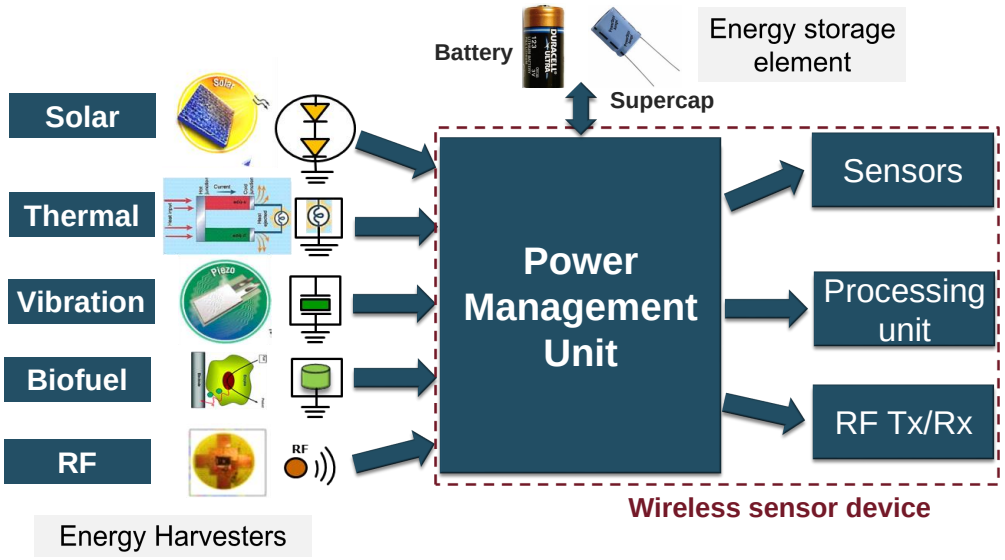

Figure 1.4: Wireless sensor network device block diagram including different powering sources.

such as smart farming, battery replacement is quite expensive especially for remote areas. Therefore, battery lifetime, device size, and cost remain major challenges for wearable and IoT devices.

The high-level goal of the research presented in this thesis is to explore the wireless sensor devices design space, with an emphasis on reducing the power and size to create miniaturized devices with long battery lifetime to fit within the IoT applications. Improving the battery life can be either through reducing the power in the underlying load circuits by leveraging low power techniques, or through building efficient power management systems and energy harvesting platforms that harvest energy from the surrounding environment to extend battery life, or through both. This thesis focuses on the design of compact and efficient energy harvesting platforms and power management architectures for powering the next generation IoT and wearable devices.

IoT devices are not like smart phones – they are relatively simple from functional point of view, but they are required to do their job for an extended period (in some cases, years) while powered by battery. IoT devices functionality is limited to sensing data, processing it then communicating the processed data to other wireless sensor nodes, they are not required to send and receive data all the time. Wireless sen-

sor network device typically consists of 4 main modules, as shown in Figure 1.4: 1) sensor: interfaces to the real world and sense conditions based on the application such as temperature, humidity, heart rate, etc; 2) processing unit/ microcontroller: the brain that accepts the data and performs data compression, analysis, and adds security bits on the sensed data before sending; 3) RF transceiver: communicates the processed date to the other wireless sensor nodes; 4) power management unit (PMU): the block that generates different regulated power rails for the different modules in the wireless sensor device and delivers power to these modules efficiently.

Extensive research has been done to build a comprehensive model for the power consumption of the wireless sensor nodes [8, 9]. It turns out that the wireless sensor devices spend most of the time in the idle low power state. As a result, although they require high instantaneous power during RF communication that can only be delivered by the battery, the average power requirement can be very low. This makes energy harvesting an attractive powering solution to extend the battery life. Energy harvesting is not a new concept but it is an important concept for the future of the power management in IoT.

IoT application space is diverse and how frequently the device sends and receives data highly depends on the application. As an example, in wireless patients monitoring application for heart rate or glucose, the device needs to send the sensed data only every 5-10 minutes and can spend the rest of the time in low power sleep mode. While in seizure patients monitoring, there is a need for a continuous monitoring of brain activity and instantaneous communication upon a detected event [10]. If the average power available from the harvester is higher than or equals to the average power requirement of the system, energy harvesting can enable net-zero-energy system with autonomous operation that doesn't require battery charging or battery replacement [11, 12]. However, the energy available from the harvester is usually low and stochastic, highly depending on the environmental conditions and the harvesting source type. To overcome the stochastic nature of the harvester source and increase the average power available from the harvester, it is required to build a PMU that aggregates power from different energy

sources efficiently. Then, delivers this power efficiently to the different wireless sensor device modules, while regulating the different generated power rails efficiently. This power management unit has to be built in a small form-factor to meet the small size constraint of the emerging IoT devices. Chapter 2 addressed this challenge and push the state-of-the-art by implementing a PMU that aggregates the maximum power from three different energy sources while simultaneously regulating three output loads in a single stage using a single inductor.

On the other hand, there are thousands of battery products available with variety of sizes, voltage, and characteristics. Selecting an appropriate battery option can increase the battery lifetime. Li-ion batteries are rechargeable batteries, commercially available with the highest energy density. To power IoT devices, efficient and durable Li-ion batteries with a voltage range of 2.8-4.2V are required. Operation at Li-ion-compatible voltages in scaled CMOS can be enabled only by stacking low-voltage transistors; such that each transistor experiences only a fraction of the battery voltage across any of its terminals. This results in efficiency degradation that can only be alleviated by using bulky off-chip inductors. Chapter 3 and Chapter 4 addressed these challenges and introduced new miniaturized hybrid Li-ion compatible power management solutions in 28nm FDSOI.

1.2 Towards FDSOI Technology for IoT

One of the major challenges when it comes to IoT is the ultra-low power requirements necessary for a long battery life. The system is required to switch dynamically between a high performance mode during sensing, TX/Rx and ultra-low power mode during sleep state [13]. For wireless sensor devices spending most of the time in the idle low power state, low leakage technology option is usually the choice to increase battery life. Traditionally, large nodes 180nm down to 65nm offer low leakage but limit the overall performance [14]. Fully-Depleted Silicon-On-Insulator (FDSOI) technology offers low leakage along with high performance on small nodes 28nm, 22nm, 14nm,

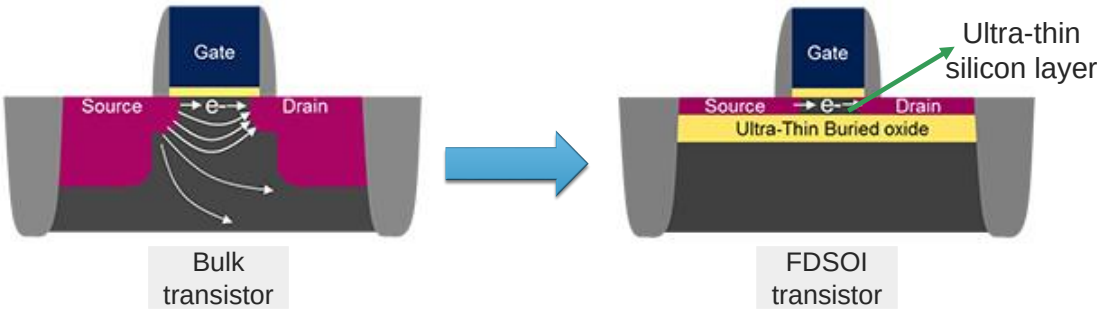

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Figure 1.5: Transistor cross-section: evolution from bulk to UTBB FDSOI.

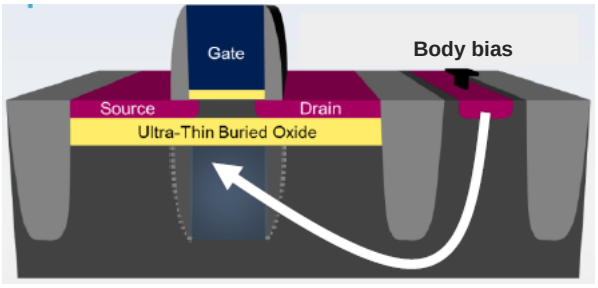

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Figure 1.6: Body biasing: extremely powerful and flexible concept in FDSOI to boost performance, optimize power consumption, and cancel out process variation.

etc. Thereby, FDSOI is a technology setting new standards for IoT.

FDSOI technology is a planar technology that extends Moores Law [15] without the need for a high cost and complicated manufacturing processes like the 3D FinFET technology [16]. FDSOI is targeted as a low Power and a high performance technology, relying on two primary innovations compared to bulk, as shown in Figure 1.5: 1) ultra-thin Buried Oxide (BOX) layer on the top of the base silicon acting as an insulator; 2) ultra-thin layer of silicon over the thin BOX implementing the transistor channel with no need for channel doping, hence, the transistor is fully depleted. These two primary innovations are what gave the technology its other name: "Ultra-Thin Body and Buried oxide FDSOI" or "UTBB FDSOI".

The doping is not needed in FDSOI because of the ultra-thin body (i.e., no ran-

dom dopant fluctuation problems). This result in a reduced process cost, immunity to threshold voltage variation and mismatch, higher mobility and performance, and immunity to short channel effect [17].

On the other hand, the ultra-thin BOX layer lowers the parasitic capacitance between the source and the drain and efficiently confines the electrons flowing from the source to the drain, reducing the leakage current. In addition, the ultra-thin BOX enables one key advantage of the FDSOI technology which is the body biasing that brings flexibility for the designers to control the threshold voltage of the transistor.

Body biasing is an efficient knob for leakage and speed optimization. The ground plane of the device can act as a second gate to control the threshold voltage of the transistors [13], as shown in Figure 1.6. Forward body bias (FBB) lowers the threshold voltage and increases the speed by applying a positive (negative) body-to-source voltage to an nMOS (pMOS) transistor. While reverse body bias (RBB) increases the threshold voltage and lower the leakage by applying a negative (positive) body-to-source voltage to an nMOS (pMOS) transistor. Body biasing enables efficient and simple dynamic switching between high performance mode (forward body biasing) and low leakage mode (reverse body biasing).

As of today, 28nm FDSOI is already in production and from IoT and wearable market perspective, UTBB FD-SOI technology is the prominent technology [14]. To build a small form-factor power management solution compatible with the needs of the next-generation wearable and IoT devices, it is desired to integrate all the DC-DC conversion and power supply regulation on the same technology as system on chip (SoC). Therefore, in this thesis, the implemented energy harvesting platform and Li-ion-compatible power management architectures are built on 28nm FDSOI.

1.3 Thesis Contribution and Organization

The battery lifetime and device size constrains of IoT put unprecedented challenges on power management system that requires innovation and out of the box think-

ing, not only at the circuit level, but perhaps more importantly at the architectural level. The research in this thesis presents compact, low cost, and efficient energy harvesting and Li-ion-compatible power management solutions for the next-generation wearable and IoT devices on 28nm FDSOI, to be integrated on the same technology as the IoT SoC. The contributions in this thesis are organized as follows:

- *Multi-Input Single-Inductor Multi-Output (MISIMO) Energy Harvesting Platform* – chapter 2 presents a small form-factor energy harvesting platform for powering net-zero-energy systems. The proposed MISIMO aggregates the maximum available power from three different energy sources while simultaneously regulating three output power rails over a wide dynamic load range, while also managing the charging and discharging of a battery, all in a single-stage using a single-inductor. The converter, fabricated in 28nm FDSOI, achieves a peak efficiency of 89%, and supports an output power range from 1μW to $60mW$, with efficiency >75% at $V_{out} = 1V$, and >69% at $V_{out} = 0.6 - 0.9V$, all with a quiescent power of only $262nW$.

- *Fully Integrated Li-ion Compatible Hybrid DC-DC Converter* – chapter 3 presents a battery-connected DC-DC converter fully integrated in 28nm FDSOI. To achieve high efficiency while blocking the $2.8 - 4.2V$ Li-ion battery voltage range using only 1.5V-transistors and on-chip passives, a modified 4-level buck converter is proposed. The fabricated converter switches at up to $200MHz$, regulating down to 0.6-1.0V over a 10μW-40mW output power range via use of DCM-PFM control. The converter occupies $1.5mm^2$ of silicon area (including a pair of $5nF$ flying capacitors and a $3nH$ inductor), and achieves a peak efficiency of 78%.

- *A miniaturized Li-ion Compatible Self-Clocked Hybrid Single-Inductor Multi-Output (H-SIMO)* – chapter 4 presents a miniaturized DCM-operated hybrid PMU in 28nm FDSOI that independently regulates three different power rails at $V_{out} = 0.4 - 1V$ and an output power range from 1μW to 100mW. The thin-oxide $1V$-transistors in 28nm are utilized to build up the stacked power train and

convert the 2-level buck into 5-level converter, reducing the switching frequency by up to 76× for an up to 21.5% efficiency improvement. As a result, the proposed H-SIMO eliminates the need for a bulky off-chip inductor, reducing the area of the required off-chip passives by 12.55× and thickness by 3×.

- *Evaluation of the Possible Number of Levels and Multilevel Configurations for N Capacitors* – Appendix A presents a methodology to realize the maximum possible number of levels for N capacitors and the different configurations of multilevel converters. Expressions representing the possible N capacitors switching states along with their equivalent steady state equations are derived. General topology for multilevel converters with $N + 2$ levels and $2^N + 1$ levels for N capacitors are shown.

- *Multi-State Switched Capacitor Voltage Regulator* – Appendix B introduces a reconfigurable multi-state switched capacitor (SC) that enables more conversion ratios without adding flying capacitors or power switches. The proposed multi-state reconfigurable SC with three flying capacitors realize 23 conversion ratios and proved to achieve higher efficiency compared to the binary SC which can only realize 7 conversion ratios. Simulations on 28nm CMOS show increase of up to 40% in the efficiency and reduction of up to 87% in the output voltage ripple.

Chapter 2

MISIMO: A Multi-Input Single-Inductor Multi-Output Energy Harvesting Platform for Powering Net-Zero-Energy Systems

Wireless sensor devices used in Internet-of-Things (IoT) applications ranging from wearables to environmental monitors typically consist of three main functional modules as illustrated in Figure 2.1(a): sensors, a processing unit, and an RF transceiver. A power management unit (PMU) is responsible for generating the various supply rails needed by these functional modules. A typical power demand pattern for a wireless sensor device is shown in Figure 2.1(b). For applications that require infrequent monitoring, such as remote patient heart-rate monitoring or industrial temperature sensing, the wireless sensor devices can spend a large fraction of time in a low-power idle state, with correspondingly little time in active mode (e.g., 97% idle / 3% active in [8]). As a result, while the peak power of such systems can be high (e.g., 10s of mW during TX/RX modes), the average power of such systems can be fairly low. Energy harvesting sources, which for small form-factor devices can typically supply power in the μW regime, can thus be employed in conjunction with a battery to enable energy-autonomous, net-zero-power operation [11, 12] if the average power of harvesting equals to or exceeds the average power demands of the load over long time intervals.

However, the energy available from most harvesting sources is stochastic, and can vary significantly with changing environmental conditions. Thus, true net-zero-

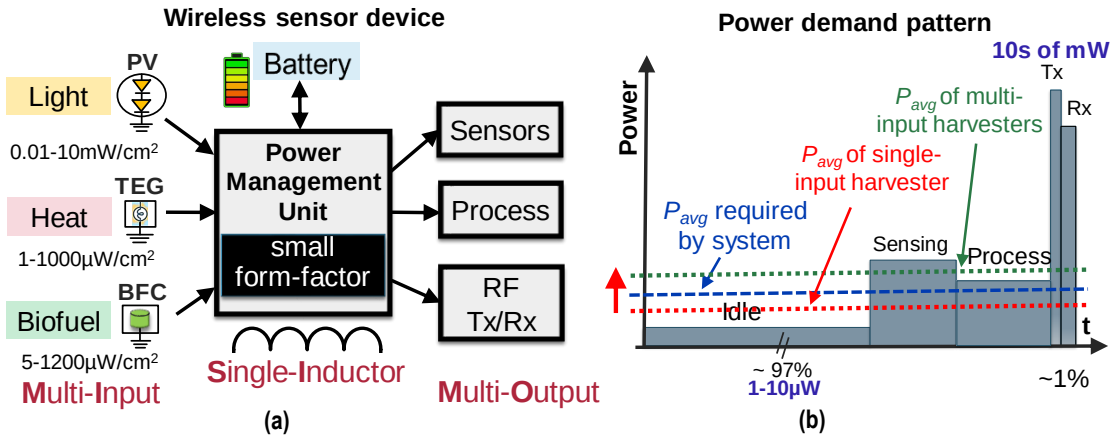

Figure 2.1: (a) Proposed MISIMO architecture. (b) Typical power demand pattern for wireless sensor devices.

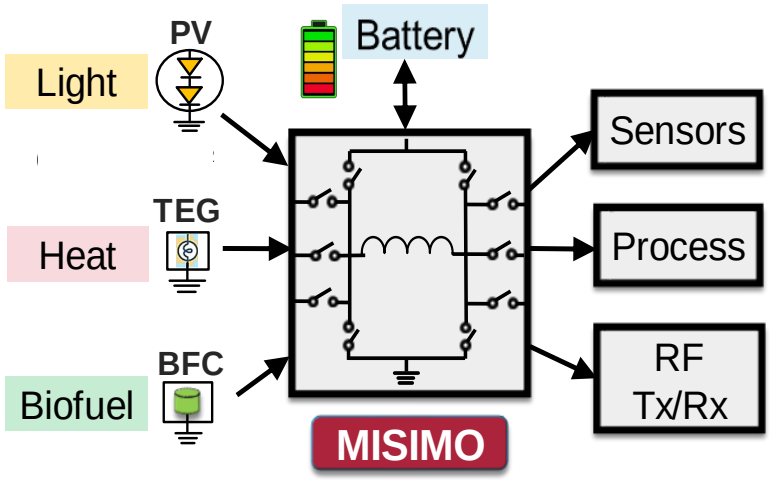

Figure 2.2: Block diagram of the MISIMO buck-boost architecture.

energy operation is a probabilistic condition. To increase the probability of successful energy harvesting, or conversely to increase the average amount of harvested energy across varying environmental conditions, it is possible to construct a PMU that aggregates power from different energy sources [18–23]. To support the small form-factor needs of emerging IoT devices, an architecture that accomplishes this with a single-inductor is desired. At the same time, the PMU should support efficient regulation of multiple output loads. Thus, this chapter introduces a MISIMO PMU: a Multi-Input Single-Inductor Multi-Output PMU (Figure 2.1 (a)).

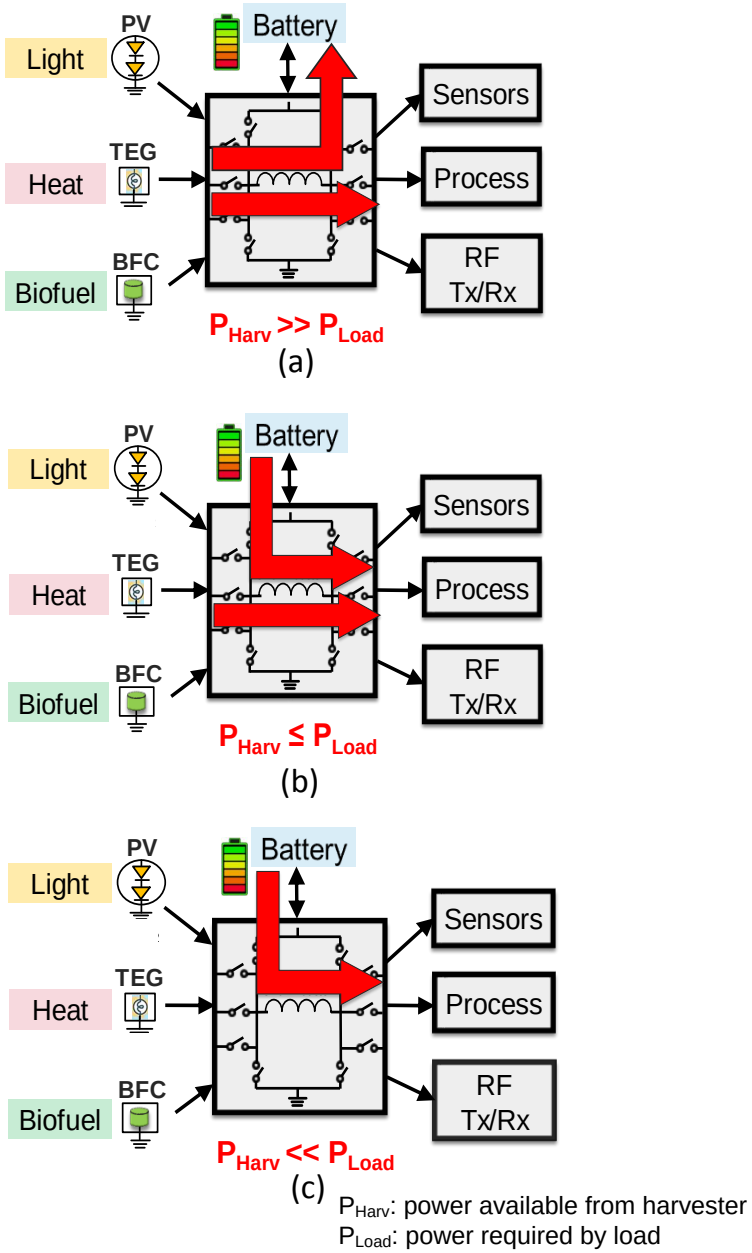

Figure 2.3: (a) If $P_{harv} > P_{Load}$, then harvesting sources deliver energy to the loads directly and also charge the battery. (b) If $P_{harv} < P_{Load}$, then both the harvesting sources and the battery deliver energy to the loads. (c) If $P_{harv} << P_{Load}$, then only the battery is selected as a source to deliver energy to the loads.

The proposed MISIMO converter employs a single-stage buck-boost architecture operating in the discontinuous conduction mode (DCM), as shown in Figure 2.2. The inductor is time-shared among different input sources and different output loads, switching dynamically between different configurations to support different harvester and load conditions as shown in Figure 2.3. For instance, if the the device is operating in a low-power idle state and the available energy from the harvester(s), P_{harv}, is higher than the power required by the load, P_{Load}, MISIMO will select the harvesting sources as a source to deliver power directly to the load and charge the battery as shown in Figure 2.3(a). On the other hand, if the energy available from the harvester is lower than or around the same as the load requirement, both the harvesting sources and the battery will be selected to deliver power to the load as shown in Figure 2.3 (b). Likewise, during periods of high instantaneous load power requirements, only the battery will be selected as a source to deliver energy to the load as shown in Figure 2.3 (c).

Multi-input energy harvesting can be useful for a variety of wearable and/or IoT-type of applications, for example by stacking or co-integrating multiple energy harvesters on-device. While the developed test chip was specifically tested for harvesting from photovoltaic (PV), thermo-electric generator (TEG), and biofuel cell (BFC) sources, the MISIMO architecture and control schemes can be applied to any number and type of DC harvesting sources, depending on the application.

This chapter is organized as follows: Section 2.1 summarizes prior-art energy-harvesting architectures and contrasts them to the proposed MISIMO architecture, while Section 2.2 and 2.3 describe the challenges of extracting the maximum possible power from multiple energy harvesting sources and regulating multiple loads with a single inductor. Section 2.4-2.6 describe the challenge of separating the input and output regulation, and introduce techniques to enable multi-input single-inductor multi-output regulation in an efficient manner. Section 2.7 then describes the specific regulation algorithms employed, while Section 2.8 describes circuit implementation details. Finally, measurement results are presented in Section 2.9.

2.1 Energy harvesting architectures

2.1.1 Prior Art

Back in 90's, single-inductor multiple-output (SIMO) shown in Figure 2.4 was proposed to regulate multiple outputs using single inductor [24–29]. And until now SIMO is a fertile research area because of the advantages it offers in terms of small form-factor. In this work, we borrowed some of the SIMO techniques for the multiple output regulation in MISIMO, as will be illustrated in Section 2.3.

Harvesting energy at the energy harvester's maximum power point (MPP) typically involves some sort of regulation at the input to the energy harvesting circuit. Likewise, any load to be powered requires regulation at the energy harvesting circuit output. Conventionally, this is achieved by separating input and output regulation via a two-stage architecture, as illustrated in Figure 2.5 for a single-input and single-output [30, 31]. Here, the first stage is dedicated for energy harvesting and maximum power point tracking (MPPT) from single input, and storing this energy in an unregulated super capacitor or battery [32, 33], while the second stage is dedicated for regulating a single load. Such approach has two major downsides: two inductors are required, which increases the implementation footprint, and the cascading of two power conversion stages results in multiplicative losses, which serve to limit the overall achievable efficiency.

Other prior work has suggested utilizing multiple energy harvesting sources to increase the overall harvesting power [18, 20–23]; however, such prior-art still utilized two-stage architectures as shown in Figure 2.6. To reduce the effects of cascaded losses and therefore improve the average harvesting efficiency, a dual path multi-input single-output harvesting architecture with a shared inductor was presented in [19], where single-stage conversion occurs under low load conditions. However, the proposed architecture supports only a single output, and, under heavy load conditions, a two-stage approach is utilized.

Other prior-art has combined energy harvesting and load regulation in purely sin-

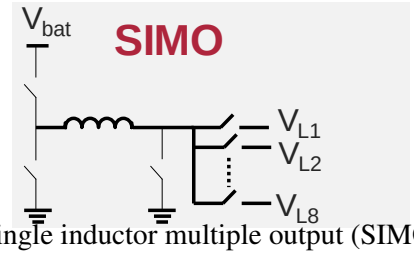

Figure 2.4: A single inductor multiple output (SIMO) architecture.

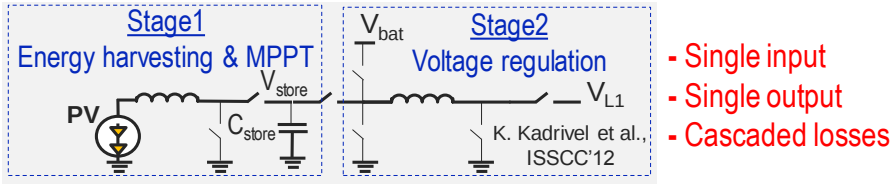

Figure 2.5: A conventional two-stage single-input single-output energy harvester.

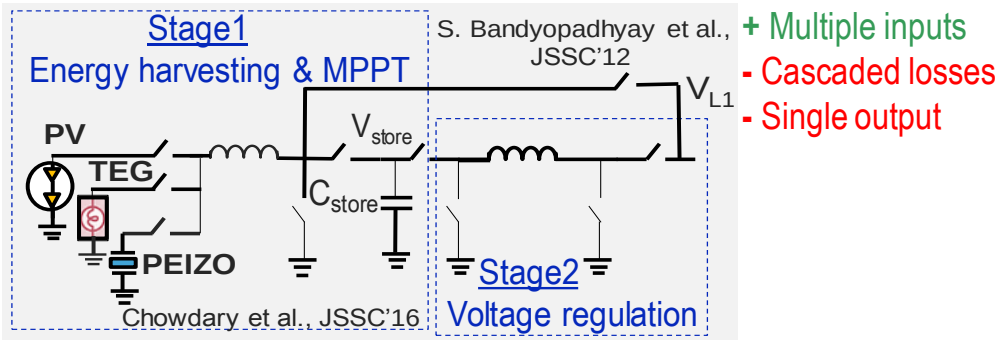

Figure 2.6: A multi-input single-output two-stage architecture.

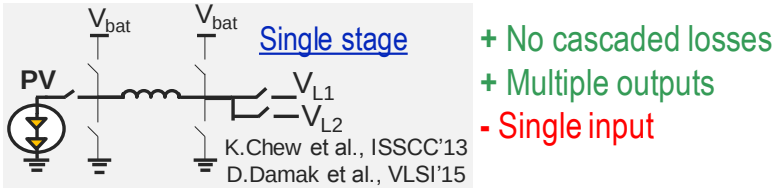

Figure 2.7: A single-input multi-output single-stage architecture.

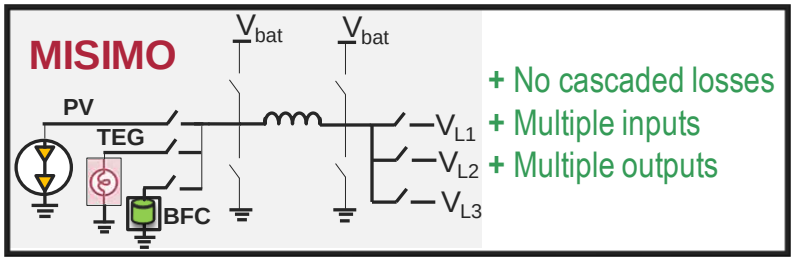

Figure 2.8: The proposed multi-input single-inductor multi-output single-stage architecture.

gle stage designs [34,35] as shown in Figure 2.7, and while efficient, the proposed architectures only supports a single input harvester and a single output load (plus a battery). To further improve efficiency, energy recycling from the load to battery was proposed in [35], which enables a reduced number of switches. The work in [36, 37] incorporated many of the aforementioned techniques, yet supported single-inductor multiple-load regulation, though with only single-input energy harvesting.

To the best of the author's knowledge, no fabricated prior-art converters have supported multiple-input energy harvesting with per-source MPPT, alongside simultaneous multiple-load regulation, all with a single-stage single-inductor topology.

2.1.2 Proposed MISIMO Architecture

The proposed MISIMO architecture combines both multi-input energy harvesting and multi-output load regulation, all in a single-stage topology using single inductor. However, there are many challenges. First, at the source side, simultaneous MPPT must be applied across all sources, where each source has a different MPP voltage and different amounts of instantaneous power available. Second, at the load side, each load needs to be simultaneously regulated at different voltages and for different load conditions, all while meeting ripple specifications. Third, all of this needs to be accomplished using a single shared inductor, so it is required to find a technique that decouples the source side MPPT from load regulation. Fourth, as for any DC-DC converter, high end-to-end efficiency across a wide input and output dynamic range is desired, which places stringent constraints on the power consumption of the controller, and the optimization strategies of leakage, conduction, and switching losses.

The work in this thesis overcomes the mentioned challenges and enables the MISIMO by: 1) allowing excess inductor energy to recycle back to the battery as needed to decouple input source and load regulation from each other, thereby enabling simultaneous MPPT across all sources and independent regulation of all loads, all with a single inductor; 2) performing 2-D MPPT for each source by dynamically adapting both the

inductor ON-time and switching frequency via a hysteretic event-driven control circuit; 3) performing multi-load regulation within a single-inductor switching cycle to reduce switching losses by 3×; 4) calibrating the battery discharge time to increase the inductor time allocated to energy harvesting by 10× and improve light load efficiency by up to 34%; and 5) modulating power-switch sizes with load conditions to improve the light-load efficiency by up to 24%, while utilizing cascoded switch structures to reduce the leakage power losses by 9×.

2.2 Simultaneous MPPT Across all Sources

While the general MISIMO architecture is scalable to an arbitrary number of harvesting sources, the developed test chip was specifically designed for harvesting from three different energy sources: light, heat and biofuels (biochemical energy found in glucose, lactate, and other metabolites in human body [38,39]). Specifically, a photovoltaic (PV) cell, a thermo-electric generator (TEG), and biofuel cell (BFC) are employed as transducers for these energy sources. Figure 2.9 shows the electrical characteristics of these energy sources. As illustrated, the voltage for the maximum power point, V_{mpp}, and the open circuit voltage, V_{oc}, changes with the available energy. However, V_{mpp} is, within a reasonable degree of accuracy, a constant fraction of V_{oc} for all three sources. For MPPT, the input voltage of MISIMO, V_{in}, for each source is regulated around a reference voltage which is equal to V_{mpp}, that is generated from a circuit that samples and holds the fraction of the open circuit voltage. The fractional open circuit sample and hold can be a resistive or capacitive divider with flip flop, as presented in details in [23, 35]. For simplicity, the reference voltage V_{mpp} was provided off-chip in this prototype.

Fractional Open circuit voltage algorithm offers a simple and high efficient MPPT across low power input range for PV cell [33] which is suitable for many low power IoT and wearable applications. The challenge here is finding an efficient manner to achieve this input voltage regulation across all three sources.

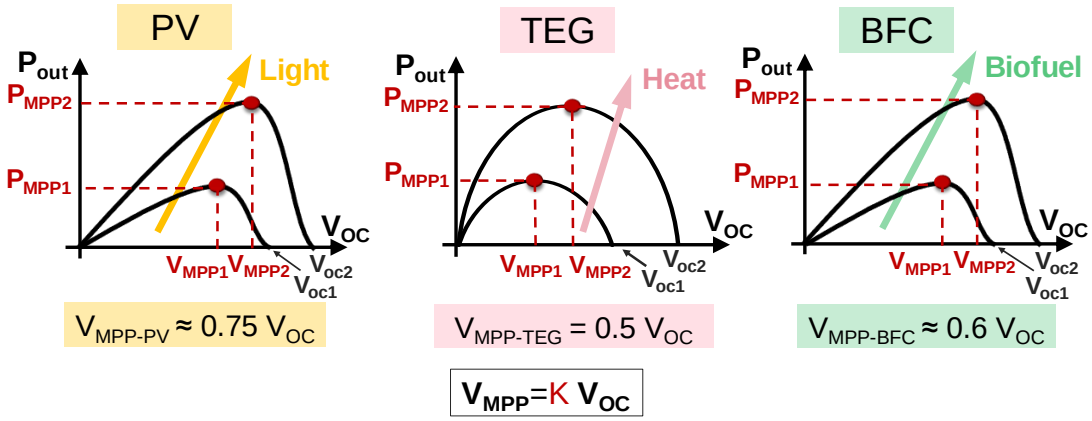

Figure 2.9: Electrical characteristics of different energy sources: PV, TEG and BFC.

2.2.1 Hysteresis-Control for Self-Clocked MPPT

As in most DCM converters, there are three different switching phases during a single inductor switching cycle in the MISIMO architecture: the inductor charging phase, ϕ_1, the inductor discharging phase, ϕ_2, and the inductor freewheel (FW) phase, ϕ_3.

To realize MPPT for DC sources, the converter input resistance, R_{conv}, has to be adaptive and equals to the equivalent resistance seen at the harvester side, R_{harv} [19] at a particular operating point, as shown in Figure 2.10. This would result in $V_{in} = V_{mpp}$. By simple derivation, R_{conv} can be found as function of the inductor charging time, $T_{\phi 1}$, and switching frequency, F_{sw}, as the following:

$$R_{conv} = \frac{2L}{T_{\phi 1}^2 F_{sw}} \tag{2.1}$$

$$MPPTcondition \begin{cases} R_{conv} = R_{harv} \\ V_{in} = V_{mpp}. \end{cases} \tag{2.2}$$

For efficient input voltage regulation, both F_{sw} and $T_{\phi 1}$ are designed to be adaptive to the available energy, and hence, the MISIMO converter performs 2D MPPT via pulse frequency modulation (PFM) with adaptive ON-time. This is in contrast to prior-art that performs 1D MPPT by either fixing the switching frequency and adapting

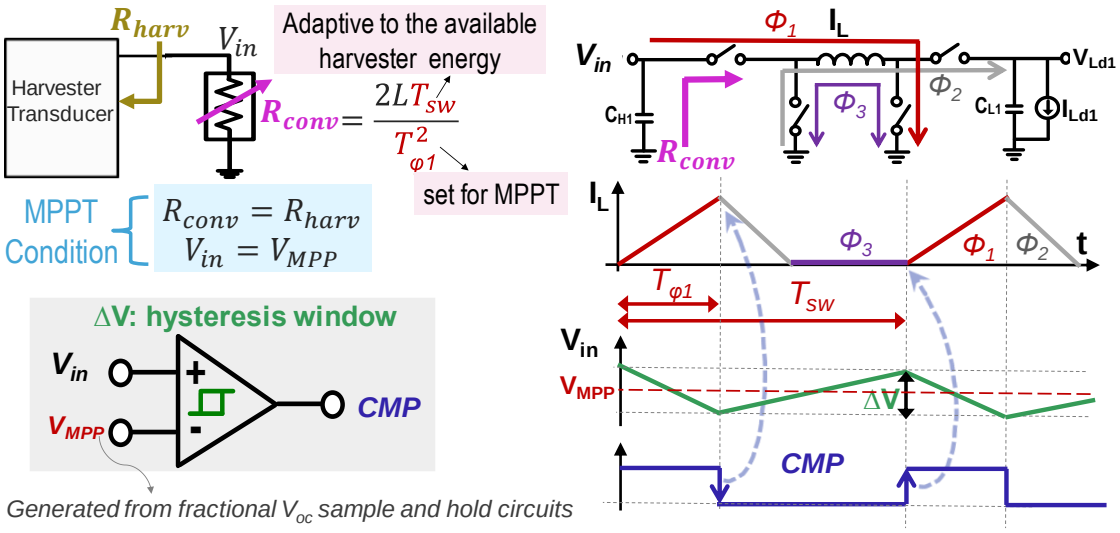

Figure 2.10: Hysteresis-Control for 2-D per-Source MPPT, where the comparator output, CMP, is used as an asynchronous clock for automatic PWM and PFM control.

$T_{\phi 1}$ [19], or by fixing $T_{\phi 1}$ and adapting F_{sw} [37]. Unfortunately, fixing F_{sw} results in a fixed quiescent power that can limit efficient dynamic range, while fixing $T_{\phi 1}$ can result in large input voltage ripple when the energy available from the harvester is low, which reduces the effectiveness of MPPT due to large V_{in} deviation from the MPP. Thus, a 2D MPPT strategy can potentially achieve higher efficiency over a wider dynamic range if implemented carefully.

To enable efficient 2D MPPT in the MISIMO converter, each harvester voltage is regulated around V_{mpp}, using adaptive $T_{\phi 1}$ and PFM control techniques based on a hysteretic control scheme. Specifically, a source hysteresis comparator regulates V_{in} around V_{mpp} within a hysteresis window ΔV, as illustrated in Figure 2.10. Once V_{in} reaches the lower hysteric limit, the negative edge of the comparator output triggers the end of ϕ_1, thereby defining $T_{\phi 1}$. When V_{in} reaches the upper hysteric limit, the positive edge of the comparator output triggers the start of new inductor switching phase, thereby defining F_{sw}. Therefore, there is no need for a clock: unlike conventional approaches, the hysteresis comparator output, CMP, becomes a defacto asynchronous clock. It performs pulse width modulation (PWM) and PFM as shown in Figure 2.10.

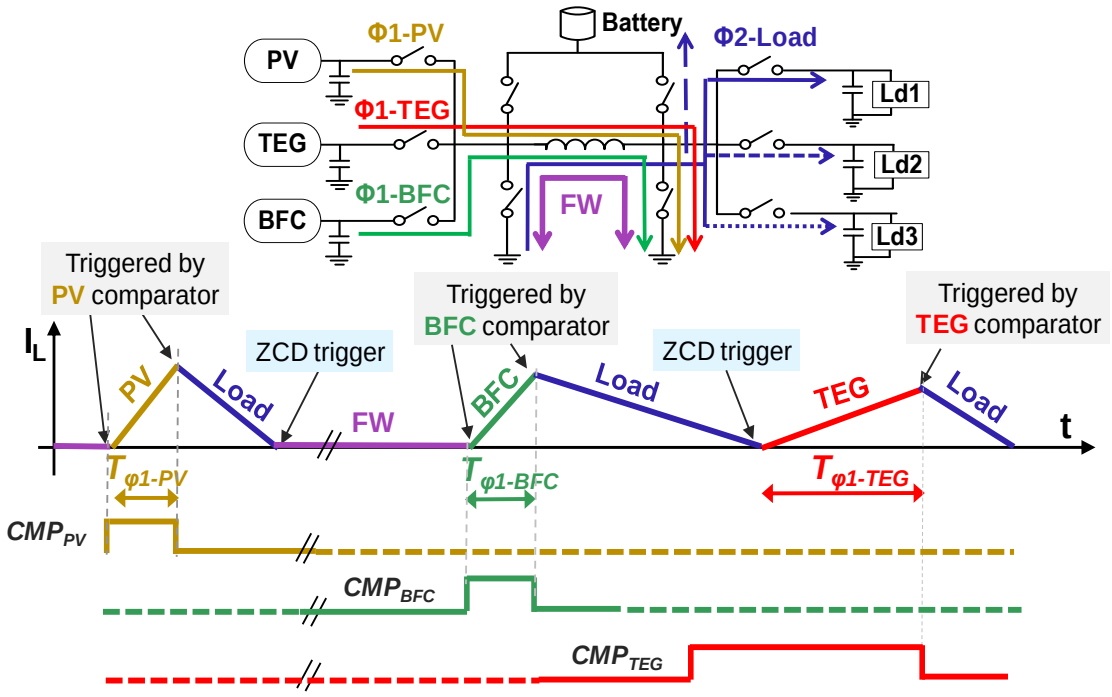

Figure 2.11: Multi-input MPPT using the outputs of the hysteresis comparators and the output of the ZCD circuit as defacto asynchronous clocks.

2.2.2 Multi-Input Energy Harvesting using a Single Inductor

The proposed 2-D MPPT hysteresis control scheme is individually applied to each of the three input sources, where each source is regulated around its own V_{mpp} using separate hysteresis comparator outputs. Thus, when multiple sources are sharing the same inductor, each source has an inductor charging time $T_{\phi 1}$ and switching frequency F_{sw} defined by its comparator output, depending on the available energy and the MPP. Figure 2.11 shows an example for multi-input harvesting. In the first inductor switching cycle, the PV hysteresis comparator output triggers the start of the inductor switching cycle, as well as the end of ϕ_1. In ϕ_2, once zero inductor current is detected via a zero current detector (ZCD) circuit, described later, the controller then looks to see if any other harvesting source's comparator output is high. If more than one comparator output is high at the same time, the controller will select the first harvester in the sequence. If

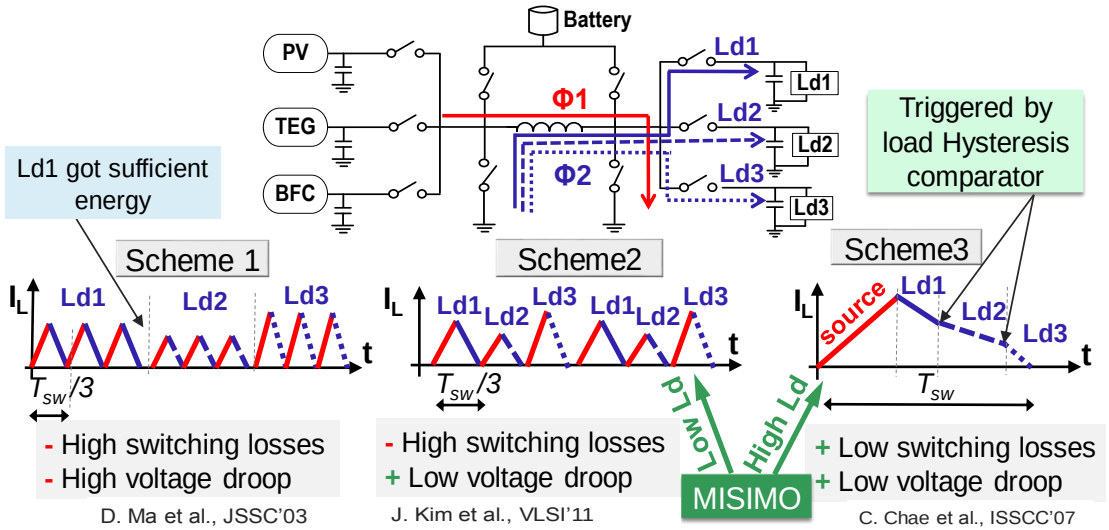

Figure 2.12: Possible switching schemes for multi-load regulation using a single inductor

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all comparator outputs are low, i.e., there is no energy available, the converter goes to the FW phase, waiting to the next trigger from hysteresis comparators (BFC in this case) to start new cycle, and so on.

2.3 Multiple Load Regulation

Each of the loads must be independently regulated regardless of load voltage and instantaneous current demands. Fortunately, there have been extensive development on single-inductor multiple-output (SIMO) DC-DC converters that support such requirements with a single inductor [26–29]. There are multiple possible switching schemes available in SIMO converters, each with their own advantages and disadvantages [40]. Figure 2.12 illustrates the schemes appropriate for inclusion in MISIMO.

In scheme 1, one inductor energizing switching cycle is dedicated for each load, and thus there are no cross regulation issues [26]. However, this scheme results in high switching frequency, increasing proportional to the number of the loads. In addition, the controller never switches to the next load before the current load receives sufficient energy so in case of applying load-step on one of the loads, the heavy load can monopo-

lize the inductor time and causes a droop on the other rails. This problem was addressed in scheme 2 by limiting the number of cycles for each load [29]. Meanwhile, scheme 3 suggested using a single inductor energizing switching cycle to charge all the loads sequentially, hence, reducing the switching frequency by the number of the loads, N (i.e., F_{sw}/N) [27].

The proposed MISIMO design adopts scheme 3, to reduce the switching frequency and switching losses by $3\times$ under high load condition. While under low load condition, the loads are regulated automatically under inductor switching scheme 2. The loads do not receive power in the same order in each cycle, instead they are interchanged in each cycle to avoid voltage droop on the last loads in the cycle as illustrated in scheme 2.

Like the input regulation scheme, the load voltages are also regulated using hysteresis PFM control. The proposed controller allows multiple loads to be regulated in a single inductor energizing switching cycle. In the inductor discharging phase ϕ_2, the upper hysteretic limit of each hysteresis load comparator prompts the inductor to discharge into the next load until zero current is detected by the ZCD circuit. Under light load condition, the loads are adaptively regulated by switching scheme 2 because the load demand for energy becomes very low.

2.4 Decoupling Source MPPT and Load Regulation

Simultaneous regulation of multiple input sources (for MPPT purposes) and loads using single inductor is not possible with conventional control techniques. If the harvester energy is available and selected as a source in ϕ_1, the inductor charging time from harvester $T_{\phi 1-Hi}$ is set for MPPT as described before (i.e., the inductor peak current set for MPPT), and this charge is dumped to the load in ϕ_2 regardless of the load requirements. Thus, if this charge is more than what is required by all of the loads,

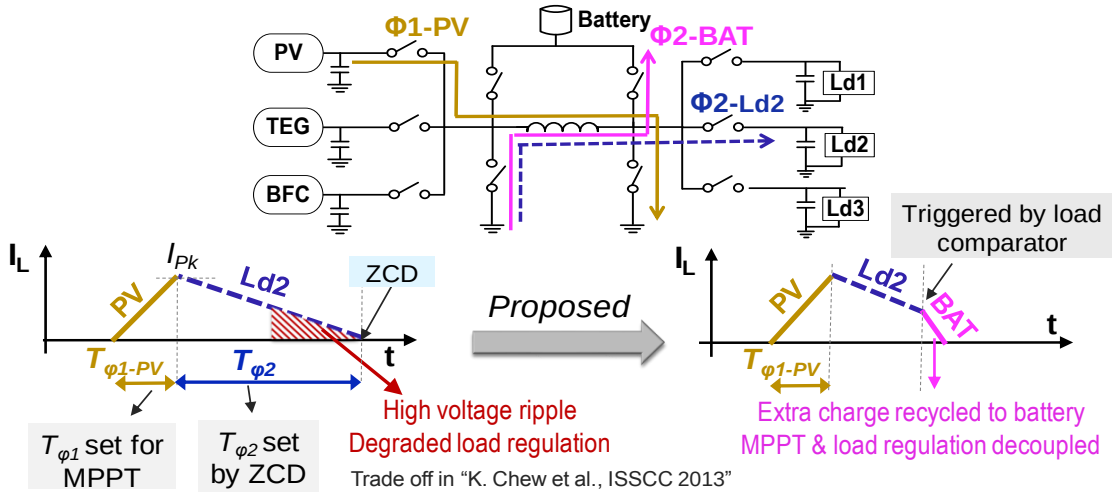

Figure 2.13: Decoupling source MPPT and load regulation in a single-inductor architecture through an optional battery charge recycling phase.

this conventional technique would result in high load voltage ripple and degraded load regulation as illustrated in Figure 2.13. This is the main issue identified in [37], and while [41] proposed to employ the battery as an auxiliary load to help address this issue, the simulated design only employed a single input and single output, and no measurement results were demonstrated.

The proposed decoupling technique overcomes this problem by recycling any extra charge back to the battery in ϕ_2 once the load receives sufficient energy, as indicated by load hysteresis comparators outputs. By this technique, load regulation becomes independent of the the inductor peak current and source side regulation, solving the trade-off described in [37]. In addition, adopting this decoupling technique allows the harvester to deliver power to the load and charge the battery in the same inductor switching cycle, which, importantly, also reduces switching losses.

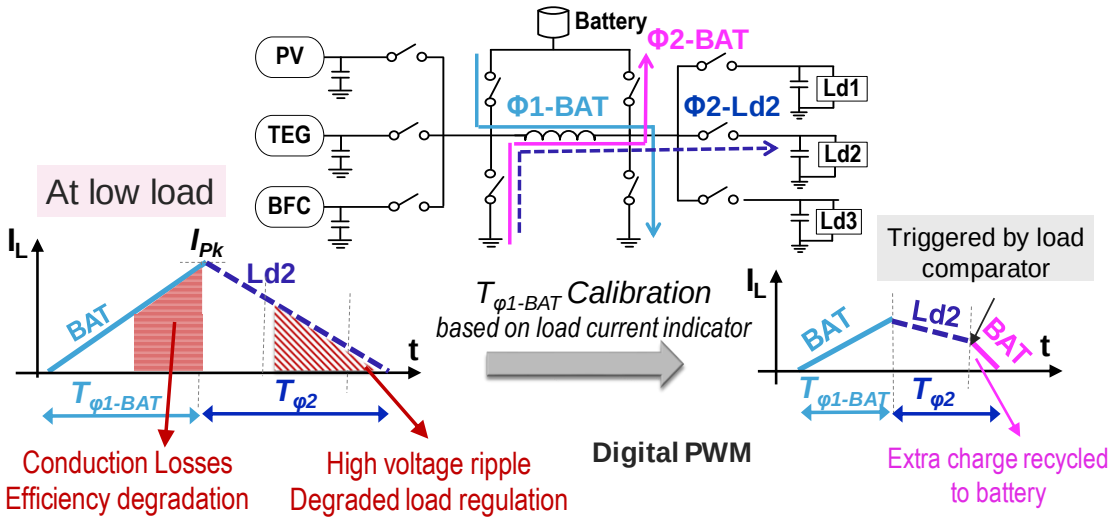

Figure 2.14: Inductor charging time under battery power ($T_{\phi 1-BAT}$) calibration for ripple control and efficiency improvement.

2.5 Inductor Charging Time under Battery Power ($T_{\phi 1-BAT}$) Calibration

If the battery is selected as a source, the inductor peak current, I_{pk}, has to be large enough to support the maximum load and to minimize the switching frequency to reduce switching losses. The inductor charging time, $T_{\phi 1-BAT}$, controls I_{pk} (i.e., $I_{pk} = (V_{in}/L)T_{\phi 1-BAT}$). If $T_{\phi 1-BAT}$ was fixed to be the largest possible value given the expected load conditions at design time, this would result in large output ripple and high conduction losses under light load conditions, as illustrated in Figure 2.14. On the other hand, if $T_{\phi 1-BAT}$ was fixed to be smaller than this, this would limit the maximum power of the converter, and result in high switching frequency and switching losses under high load condition. This trade-off described in [37].

In the MISIMO converter, $T_{\phi 1-BAT}$ is digitally calibrated based on load current indicator bits, described in Section 2.8, hence I_{pk} varies adaptively with the load requirement using ON-time digital control. This is similar to digital pulse width modulation described in [29]. For a buck-boost converter operating in DCM, $T_{\phi 1-BAT}$ can be expressed as function of load current, I_{Ld} as follows:

$$T_{\phi 1-BAT} = \frac{1}{V_{in}}\sqrt{\frac{2LI_{Ld}V_{out}}{F_{sw}}}. \tag{2.3}$$

In the MISIMO converter, $T_{\phi 1-BAT}$ is calibrated such that each load receives sufficient energy from the battery in a single cycle, reducing the output ripple and conduction losses under low load condition, and reducing switching losses at high load condition. Calibrating $T_{\phi 1-BAT}$ also increases the inductor time allocated to energy harvesting by up to $10\times$, and ensures that load regulation is not dominated by the battery when harvestable energy is available. Equation (2.3) shows that $T_{\phi 1-BAT} \propto \sqrt{I_{Ld}}$. Therefore, the digital calibrated bits controlling $T_{\phi 1-BAT}$ can be used as load current indicator, described later in Section 2.8.

While calibrating $T_{\phi 1-BAT}$ using analog feedback circuitry is faster than the employed linear-search digital calibration, the power-hungry analog feedback circuitry (specifically for multiple load regulation) is not suitable for this DC-DC converter, where light-loads must also be supported. To support an output power as low as $1\mu W$, an ultra-low power controller with a quiescent power in a nW range is a must, thereby justifying the use of the digital $T_{\phi 1-BAT}$ calibration.

2.6 Multi-Input Multi-output Regulation

Putting all of the techniques described in Sections 2.2-2.5 together, hysteresis comparators for PFM control are employed to regulate each source at its maximum-power point voltage, $V_{mpp,i}$, and each load at its own reference voltage, $V_{ref,i}$. Figure 2.15 shows the inductor current switching cycles under different scenarios for source and load conditions.

The representative inductor switching schemes in Figure 2.15 illustrates the adaptive inductor on-time, automatic PFM control, automatic battery/energy source selection, and the ability to recycle charge back to the battery, which decouples MPPT regulation from load regulation in a single-inductor converter. During periods where

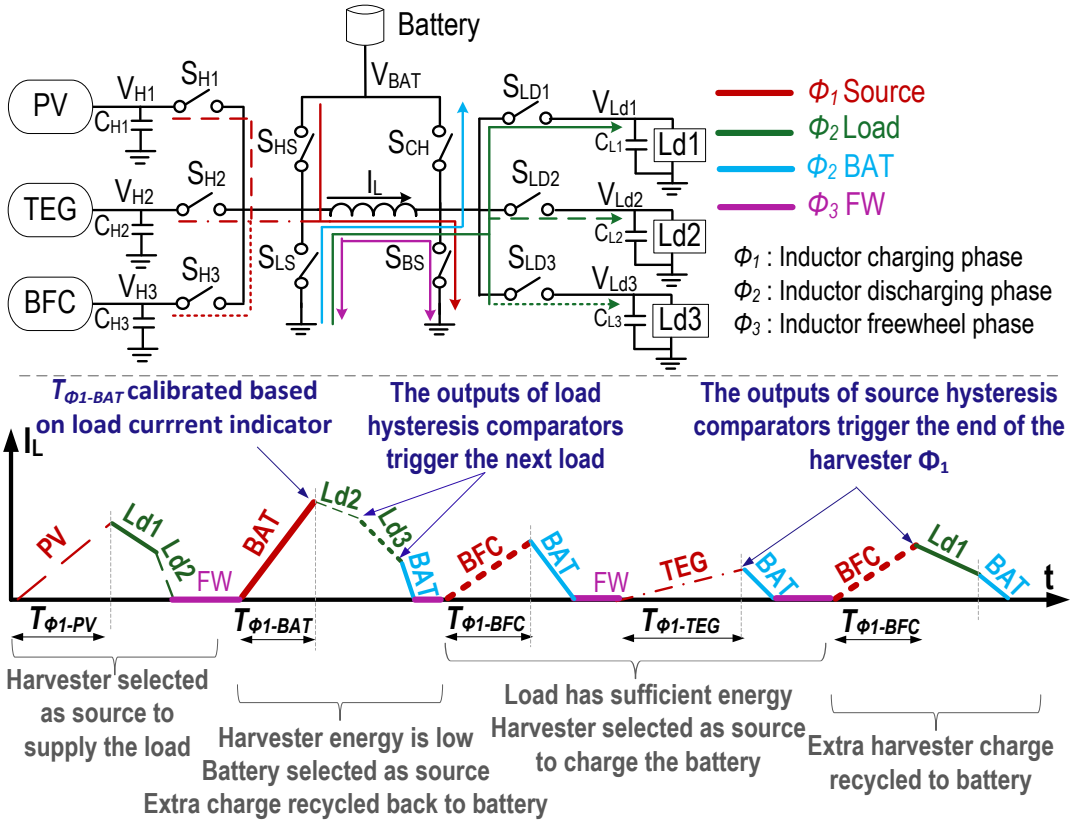

Figure 2.15: The MISIMO switch-level power stage, along with representative inductor switching schemes under different source and load conditions.

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instantaneous load demands outstrip harvesting capacity, the MISIMO controller selects the battery as the source for a calibrated time in ϕ_1, to deliver energy to one or more loads in ϕ_2. If harvester energy is available, it is extracted in ϕ_1 for T_{ϕ_1} determined by the harvester hysteresis comparator output, then this energy is delivered to up to three loads and/or the battery in ϕ_2.

2.7 Event-Driven Control Algorithm

The proposed MISIMO platform is controlled by an asynchronous event-driven digital controller designed to support low quiescent power. The overall MISIMO block diagram is shown in Figure 2.16. There are three trigger sources for the digital con-

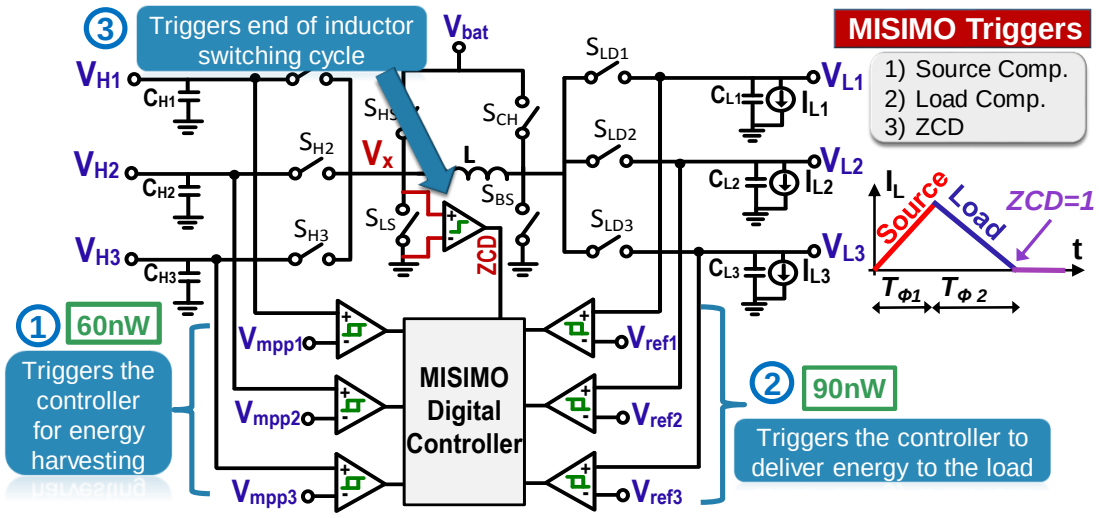


Figure 2.16: MISIMO event driven controller is triggered by three sources: source hysteresis comparators, load hysteresis comparators and ZCD.

troller: 1) source hysteresis comparator outputs trigger the controller whenever there is available energy at the source side to harvest; 2) load hysteresis comparator outputs trigger the controller if any of the loads do not have sufficient energy; 3) the zero current detector output triggers the end of the inductor switching cycle and the start of new cycle.

Figure 2.17 shows the overall MISIMO controller flow chart. At the beginning of each inductor switching cycle, if load doesn't need energy and harvester energy not available, the converter goes to the freewheel phase. But if load doesn't need energy and harvester energy is available, harvester is selected as a source to charge the battery (if the battery is not overcharged). On the other hand, if load needs energy and there is no load alarm, harvesters are selected to deliver power to the load. Load alarm is generated when the harvester power is less than the power required by the load. If the load needs energy and there is load alarm, battery is selected a s a source to deliver power to the load.

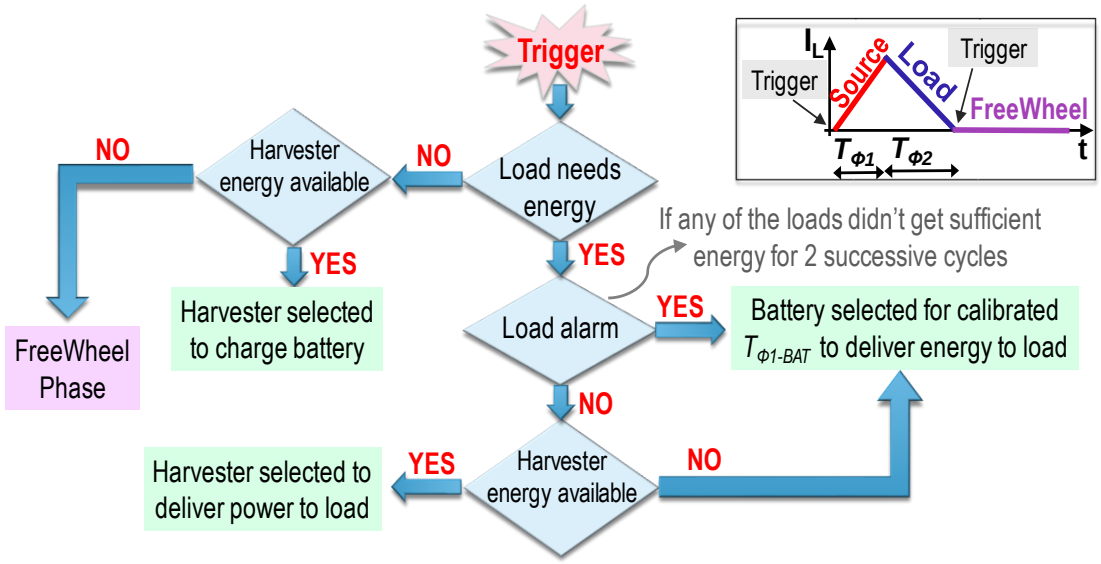


Figure 2.17: MISIMO controller flowchart.

2.7.1 Source side control algorithm

Figure 2.18 and Figure 2.19 show the detailed source side and load side algorithm, respectively. The source side controller is triggered only if any of the three loads have an energy deficit ($Ld_{j\_cmp} =' 0'$), or if harvester energy is available ($H_{i\_cmp} =' 1'$) and battery is not fully charged ($BAT_{OV} =' 0'$). Otherwise, the converter is in the freewheel phase and the source side controller is disabled to save power.

The proposed source side algorithm shown in Figure 2.18 selects one of the three harvesters or the battery as a source in ϕ_1, based on harvester and load condition. The harvester condition is defined by the source hysteresis comparators outputs H_{i_cmp}, while the load condition is defined by two signals: ld_alarm and ld_needs_energy. The ld_needs_energy signal is asserted if the output of any of the load hysteresis comparators Ld_{j_cmp} is low; which indicates that one of the loads require energy. The ld_alarm signal is asserted if any of the output loads did not receive sufficient energy for two successive switching cycles (i.e., Ld_{j_cmp} is low for two successive periods).

If the ld_alarm signal is high, the battery is selected as a source regardless the harvester condition (i.e., $ld\_alarm =' 1'$ indicates that the energy available from the

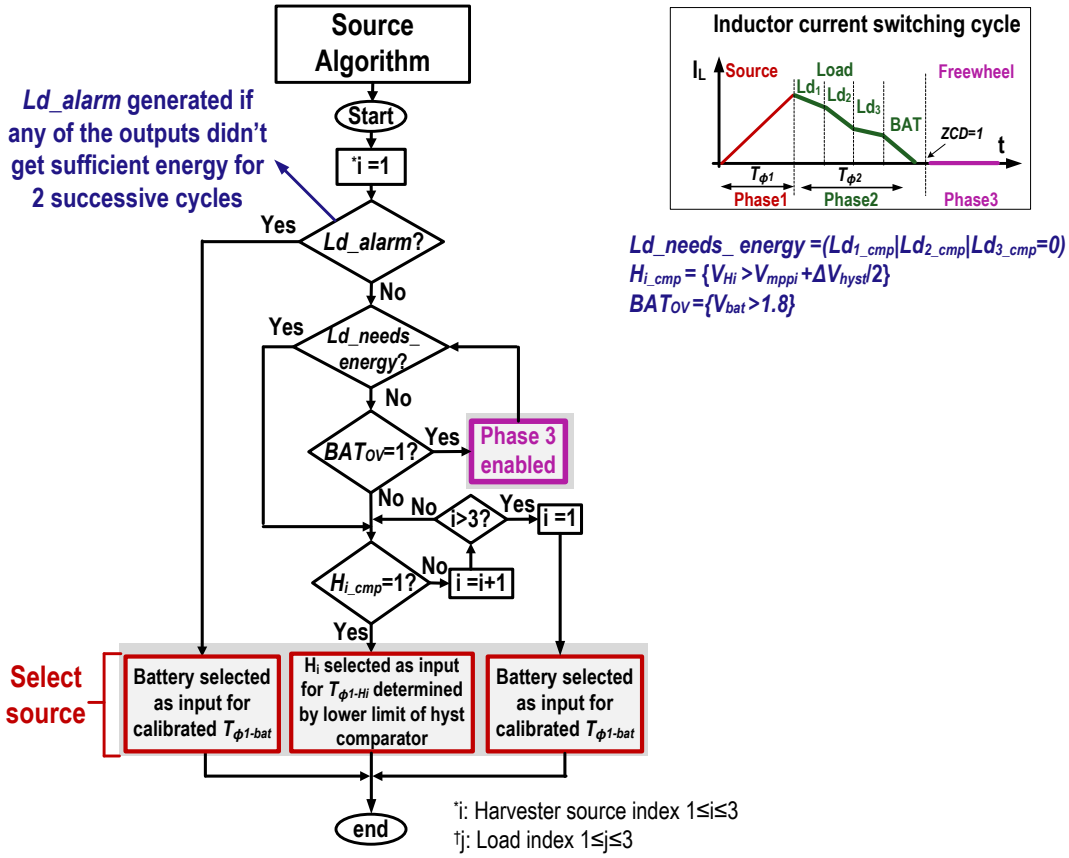


Figure 2.18: MISIMO controller source side algorithm.

harvesting sources is less than the load requirement). If the ld_alarm signal is low and the ld_needs_energy signal is high, the algorithm checks the source hysteretic comparator output of the first harvester, H_{1_cmp}. If H_{1_cmp} is high, H_1 is selected as a source to deliver power to the load; else, the algorithm checks the successive harvester comparator output H_{2_cmp}, and so on. If the output of all source comparators are low, the battery is selected as a source to deliver power to the load. On the other hand, if the ld_needs_energy signal is low, this indicates that all loads have sufficient energy and in this case if any of the harvester energy is available, the harvester will be selected as a source to charge the battery if the battery is not fully charged ($BAT_{ov} =' 0'$); else, the converter enters the freewheel phase.

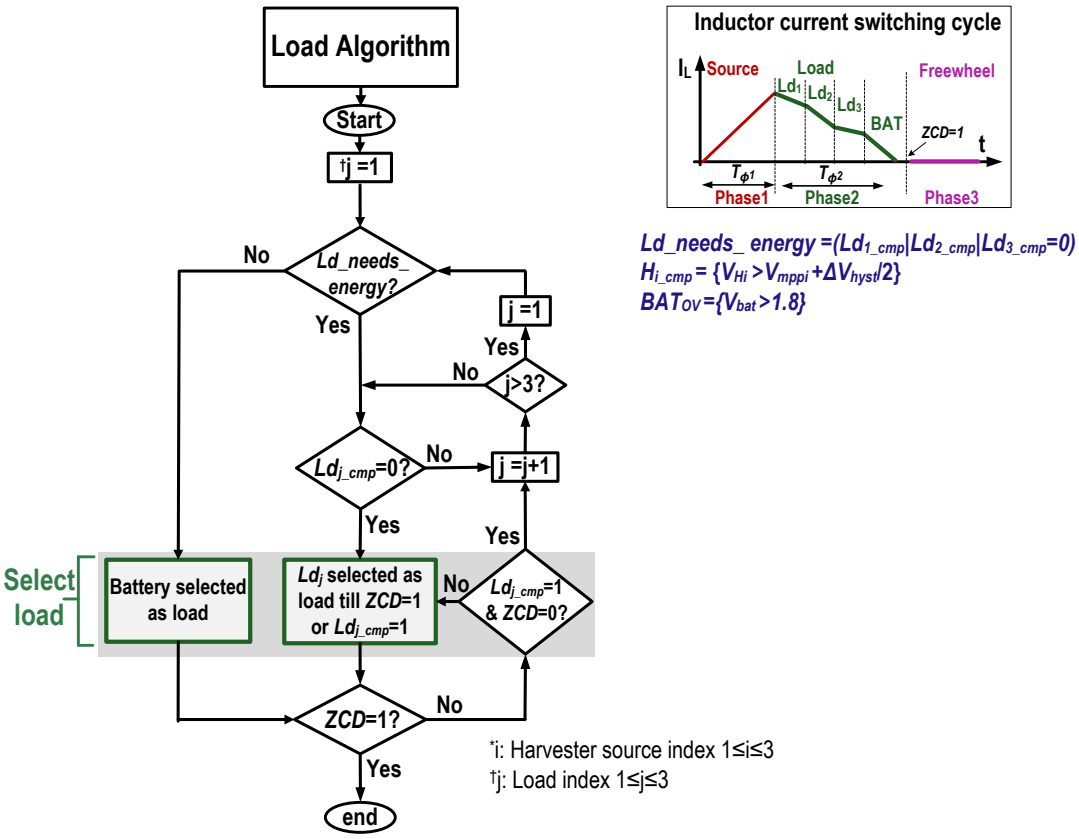


Figure 2.19: MISIMO controller load side algorithm.

2.7.2 Load side Algorithm

Figure 2.19 shows the proposed load side algorithm, which is enabled only during phase ϕ_2, where the three loads and the battery are time multiplexed. The algorithm checks the load hysteresis comparator outputs sequentially and charges each load j until its comparator output equals to '1' ($Ld_{j\_cmp} =' 1'$), then switches to next load with a low comparator output and so on until the zero current state is detected ($ZCD =' 1'$). If all loads are charged ($ld\_needs\_energy =' 0'$) and there is still current in the inductor, extra charge recycled back to battery at the end of ϕ_2.

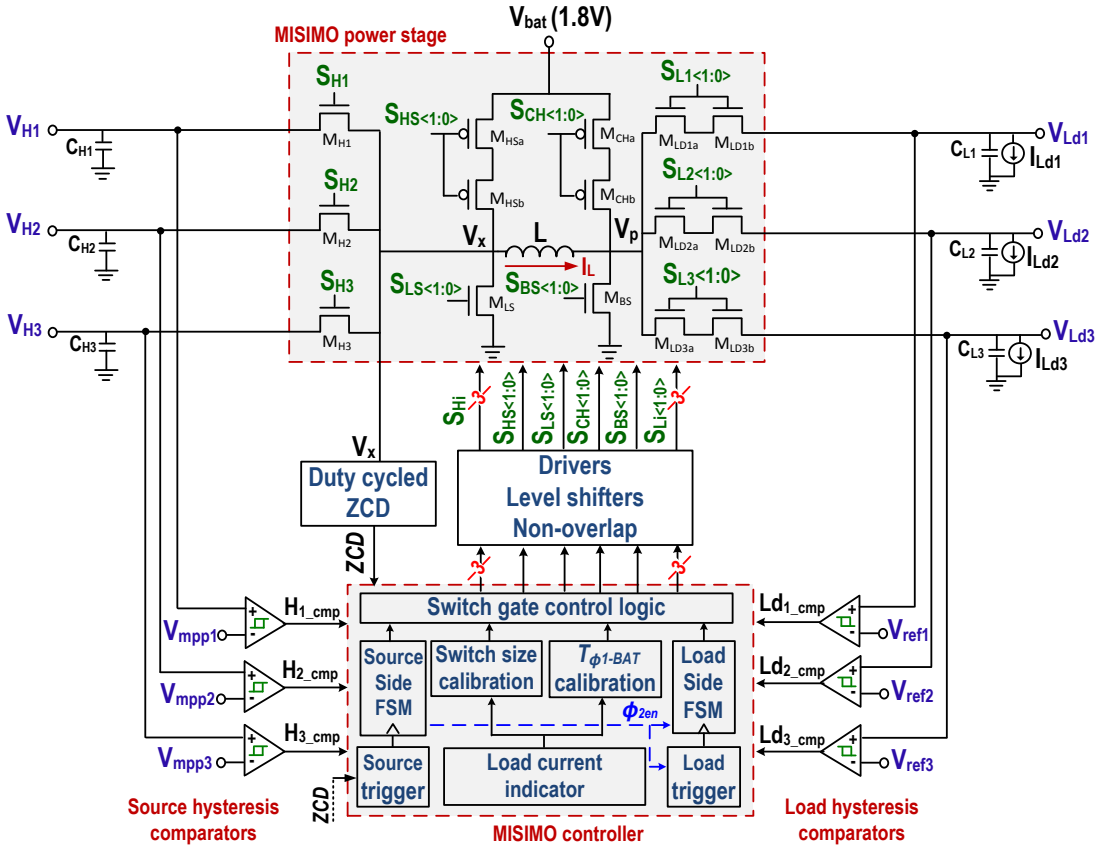


Figure 2.20: Block diagram of the MISIMO chip, including detailed schematics of the power stage with power-switch width control.

2.8 MISIMO Architecture and Circuit Details

The proposed MISIMO architecture is shown in Fig 2.20. It consists of a power stage, a digital controller, hysteresis source comparators for MPPT, hysteresis load comparators for load regulation, and a zero-current detector (ZCD) circuit. MISIMO can be extended to any number of inputs or outputs by adding switches to the source side or the load side of the power stage, respectively.

2.8.1 Power Stage Efficiency Improvement Techniques

To achieve high efficiency across wide input and output power dynamic range, different control techniques are employed. The power stage losses at low loads can dom-

inate the converter quiescent power. Specifically, at low loads, the converter spends most of the time in the freewheel phase where the power switches connected to the battery and to the loads suffer from high leakage because of their large sizes, and relatively large blocking voltage. To address this, load and battery power switches are implemented by cascoding transistors, which push them into the super cut-off region, reducing leakage by 9×. To achieve high efficiency over a wide dynamic load current range, the power switches are each split up into 2-bit binary-weighted arrays and MISMO performs dynamic switch size modulation (SSM). The switch size is calibrated dynamically based on the load current indicator output, described later in Section 2.8.4.

2.8.2 Hysteresis Comparator

Figure 2.21 shows the detailed schematics of the hysteresis comparator used for source side and load side voltage regulation. The hysteresis window is determined by the ratio between the width of the cross-coupled transistors (M_6 and M_7) and the diode connected transistors (M_3 and M_4). The hysteresis window ΔV can be described by the following equation:

$$\Delta V = \pm \frac{1 - \sqrt{(W/L)_{6,7}/(W/L)_{3,4}}}{\sqrt{1 + (W/L)_{6,7}/(W/L)_{3,4}}} V_{ov_{1,2}}. \tag{2.4}$$

2.8.3 Duty-Cycled Zero Current Detector

The ZCD block shown in Figure 2.22 detects the inductor zero current crossing by comparing the voltage at Vx node to GND. In general, zero current detection requires significant power, as the detector has to operate at sufficiently high speed in order to avoid negative inductor current that results in efficiency degradation. To reduce ZCD power, prior work has suggested digital calibration techniques for $T_{\phi 2}$ to avoid the need for a power-hungry analog comparator [35]. However, this is not applicable for MISIMO because the ZCD point changes every inductor switching cycle due to the

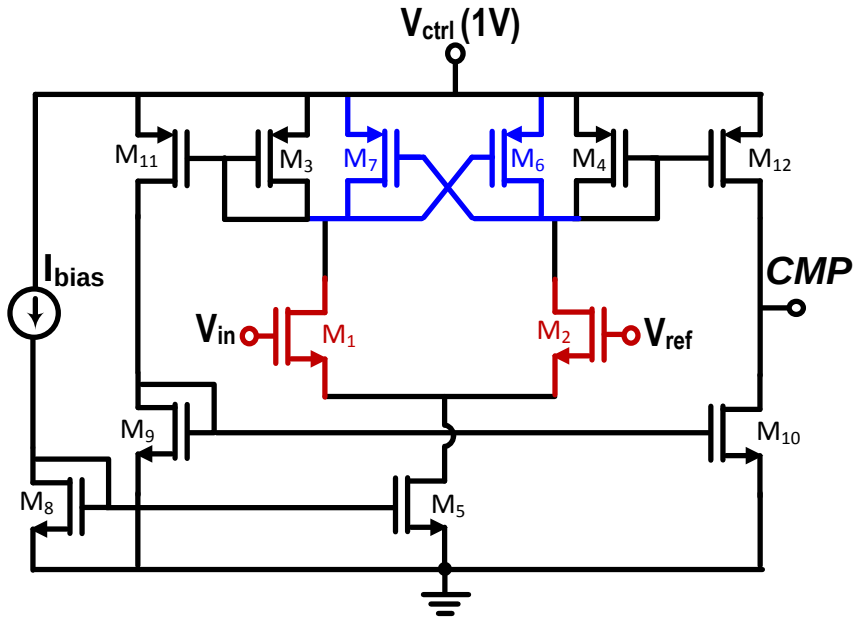


Figure 2.21: Hysteresis comparator.

dynamic multiple source harvesting and multiple load regulation. Thus, an analog ZCD is necessary in MISIMO. Fortunately, it can be noted that zero current detection only needs to occur at the end of ϕ_2. Thus, to save power, the ZCD comparator is duty-cycled to be enabled only during ϕ_2, which, importantly, is much smaller than ϕ_1 and ϕ_3 at low load currents. Once the ZCD output triggers the end of ϕ_2, it is turned off the rest of the switching cycle. By implementing a duty cycled ZCD, the power consumption of ZCD reduced from 2.23μW to 1nW @ Pout=10μW, saving power by more than 2000$\times$.

One of the advantages of the employed SSM technique is that it avoids having small voltage at the V_x node under low load condition, which nominally can't be detected by conventional low-power ZCD circuits. Specifically, since switch size modulation scales down the transistor size at low load current, making its ON resistance large, the voltage on V_x can still be large enough to be detected by the present ZCD circuit.

In order to to reduce the inductor negative current and efficiency degradation result from late switching, offset added intentionally by mismatching the width of the input differential pair to compensate for loop delay (delay from ZCD output to power stage switches input).

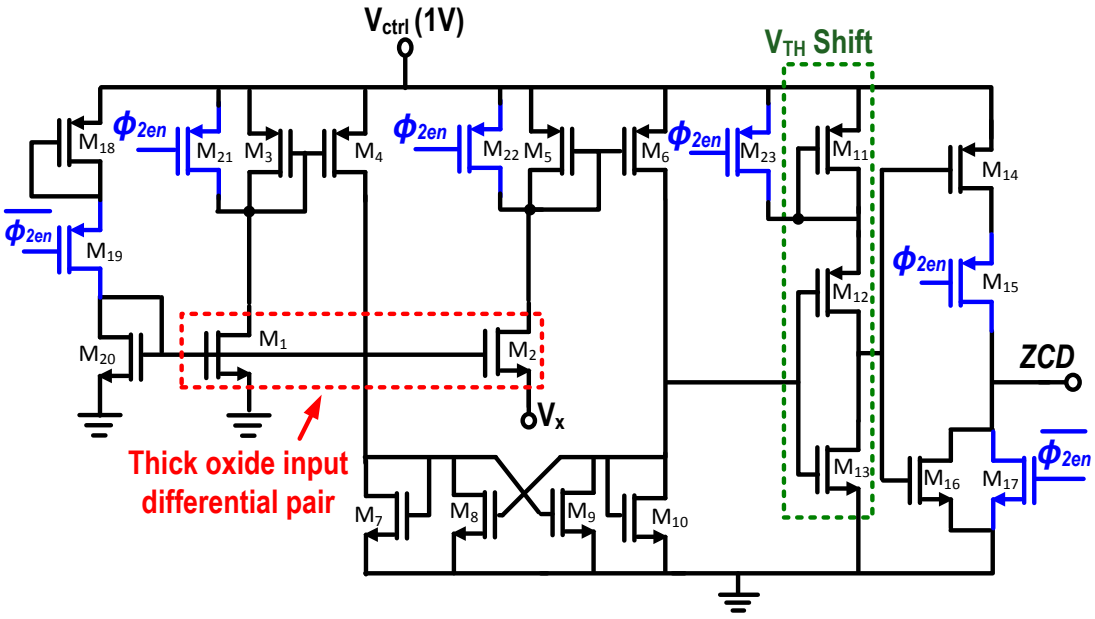


Figure 2.22: Duty-cycled zero current detector.

The designed ZCD circuit utilized fairly small devices, and thus result in a simultaed 3σ offset of 20mV. This worst-case offset was simulated to adversely affect power stage efficiency by up to 9%. Offset compensation schemes using capacitive trimming or other techniques can reduce the offset down to $< 1mV$ at zero static power consumption (with only a one-time calibration cost to implement), which would, at that offset level, negligibly affects converter efficiency. Despite the fact that an offset cancellation scheme was not implemented in the developed chip, a high peak efficiency was still achieved, as will be described in Section 2.9.

2.8.4 MISIMO Asynchronous Controller

Asynchronous Source Side Clock Generation and $T_{\phi 1-Hi}$ Control

Figure 2.23 shows the block diagram of the asynchronous source side FSM clock generation. The negative edge of the chip RST signal acts as the first trigger for the source side algorithm to kick-start MISIMO. During the operation of MISIMO, there are three trigger sources for the source side algorithm: 1) zero current detector output,

ZCD; 2) negative edge of the load hysteresis comparators outputs (i.e negative edge of ld_needs_energy signal); 3) positive edge of the source hysteresis comparators outputs (i.e positive edge of $EH\_available$ signal). At the end of ϕ_2, a ZCD pulse is generated to trigger the source side FSM. While during the freewheel phase, ld_needs_energy or $EH\_available$ signal trigger the source side algorithm. When a harvester selected as a source in ϕ_1 by the source side FSM, the negative edge of the harvester comparator output triggers the end ϕ_1, defining $T_{\phi 1-Hi}$ as shown in Figure 2.23.

Load Current Indicator and $T_{\phi 1-BAT}$ Control

As described in Section 2.7.1, ld_alarm signal is asserted if any of the output loads didnt receive sufficient energy for 2 successive cycles (indicated by the hysteresis comparators outputs). The circuit details of the ld_alarm signal generation block is shown in Figure 2.24. If ld_alarm is high, the battery is selected as a source for a calibrated $T_{\phi 1-BAT}$. The load current indicator bits, $Ld_{ind}\_bit < 4:0 >$, are the bits controlling the pulse width $T_{\phi 1-BAT}$. A binary-wighted MIM-capacitor delay-controlled line is used to generate the digital calibrated pulse using the $Ld_{ind}\_bit < 4:0 >$ control bits, as illustrated in Figure 2.24.

The load current indicator checks the ld_alarm signal when battery is selected as a source: if ld_alarm is high for two successive cycles, the load current indicator bits $Ld_{ind}\_bit < 4:0 >$ increments by one, increasing $T_{\phi 1-BAT}$ accordingly. On the other hand, if ld_alarm is low (all loads receive sufficient energy in one inductor switching cycle), and the battery is selected as a source and load in the same switching cycle, $Ld_{ind}\_bit < 4:0 >$ decrements by one, reducing $T_{\phi 1-BAT}$ accordingly. In steady state, each load receives sufficient energy in one inductor switching cycle.

Asynchronous Load Side Clock Generation

Figure 2.25(a) shows the circuit details of the asynchronous clock generation for the load side FSM. In ϕ_2, once a load receives sufficient energy and its comparator

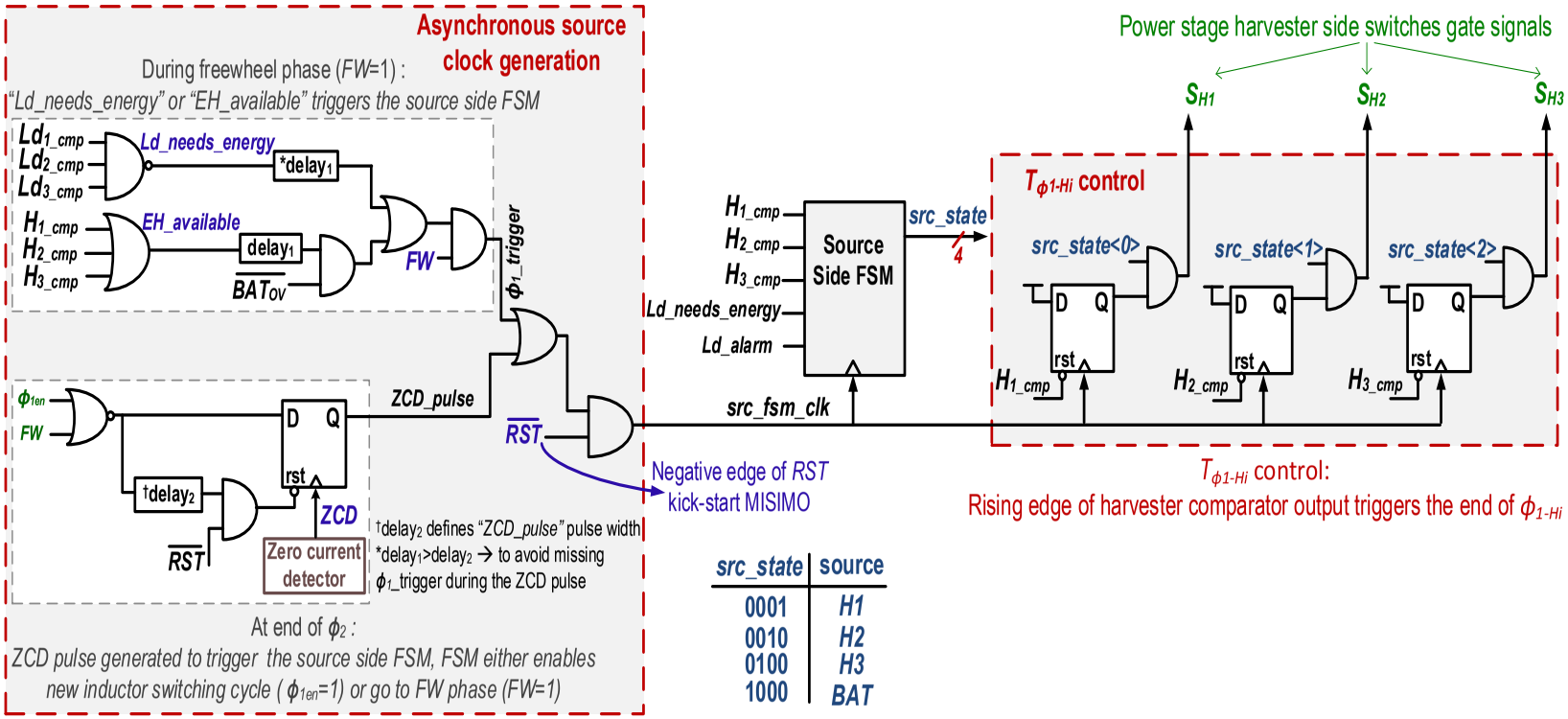


Figure 2.23: Circuit details of the asynchronous source clock generation block and adaptive $T_{\phi 1-Hi}$ control.

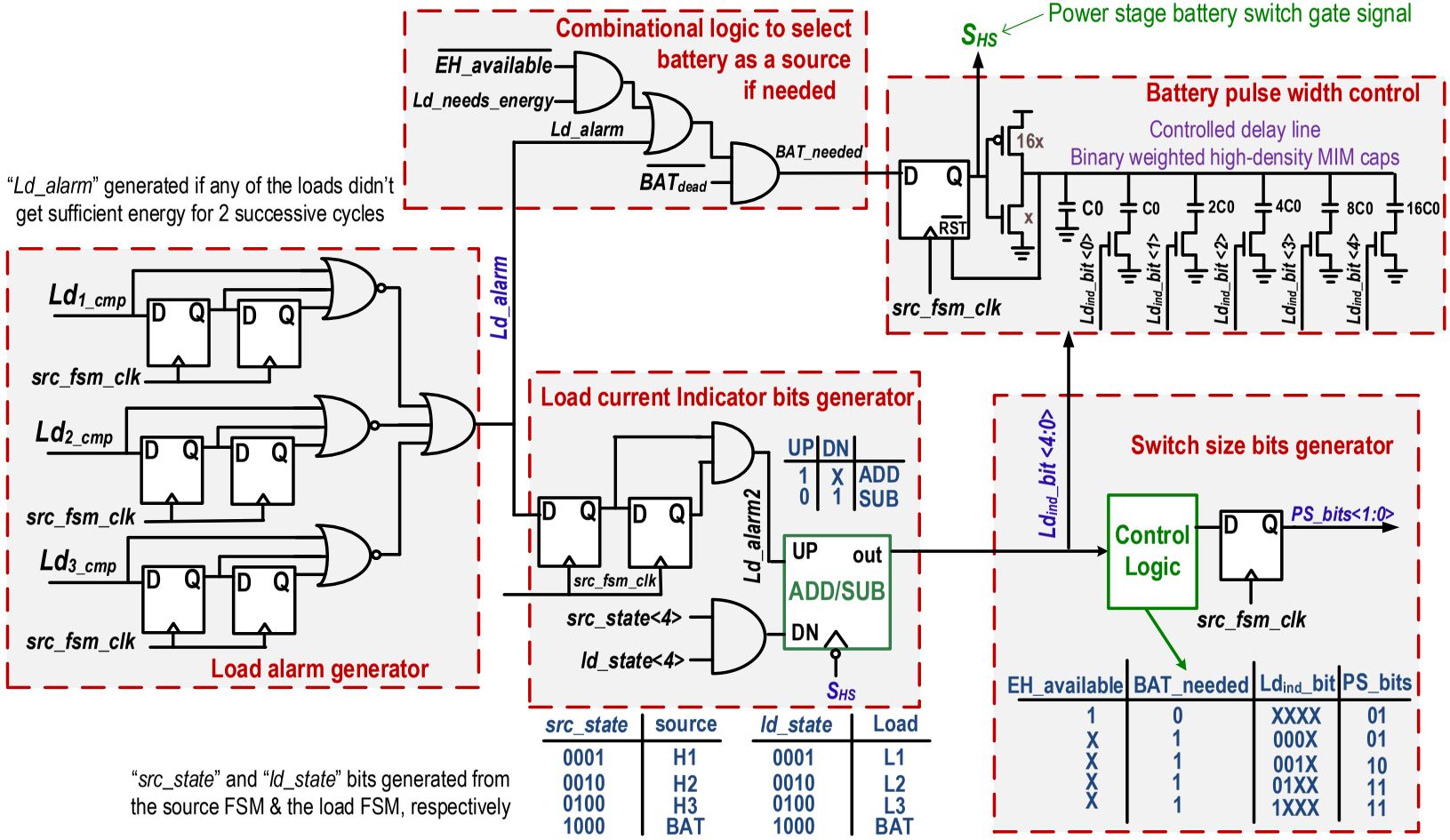


Figure 2.24: Circuit details of ld_alarm signal generation block, and load current indicator block that generates $Ld_{ind}\_bit < 4:0 >$ used for $T_{\phi 1-BAT}$ and switch size control

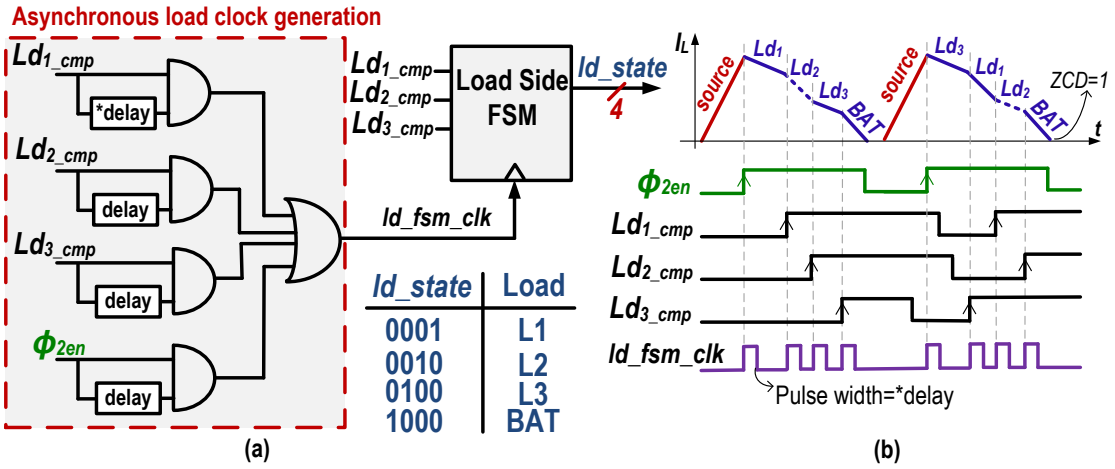


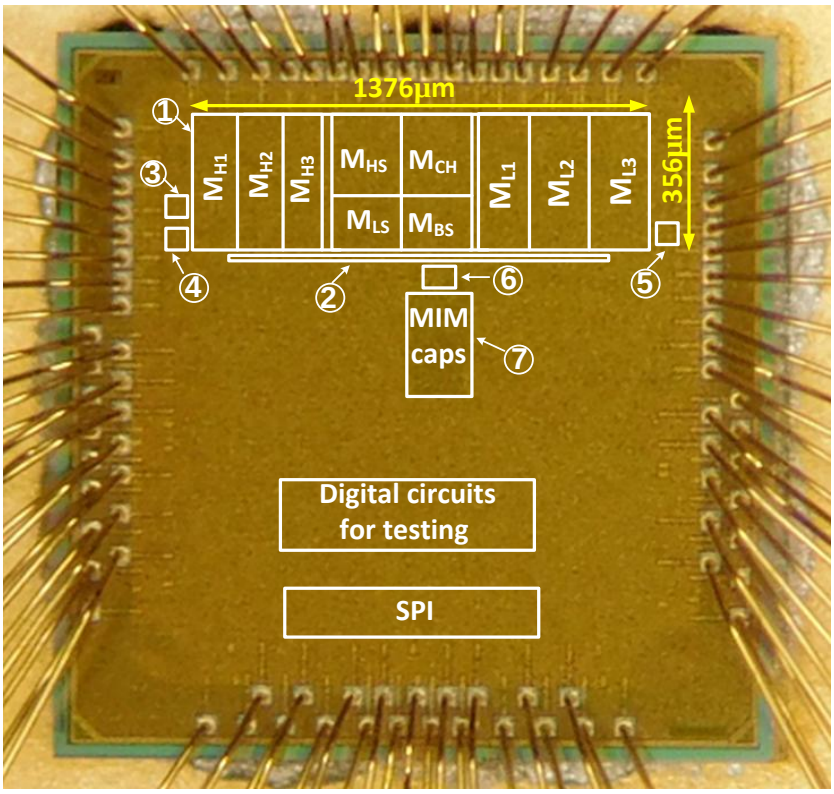
Figure 2.25: (a) Circuit details of asynchronous load clock generation block. (b) Equivalent waveforms.

output goes high, a pulse generated to trigger the load FSM to switch to the next load and so on until inductor zero current detected. Waveforms describing the asynchronous clock generation is shown in Figure 2.25 (b).

2.9 Experimental Result

The proposed MISIMO converter is implemented in $0.5mm^2$ in 28nm FDSOI. The power stage occupies $0.48mm^2$, dominating the total area of MISIMO. A die micrograph is shown in Figure 2.26. The chip is directly wire-bonded to a printed circuit board (PCB) using chip-on-board packaging technology. The wirebonded chip-on-board used for testing is shown in Figure 2.27. MISIMO controller is complicated, therefore, many IO pads were added for testing the controller, and monitoring the ZCD and comparators signals. Also, dedicated supply pads were added to measure the power consumption of each block. In real implementation, the area would be much smaller because few numbers of IO pads are required for MISIMO IP.

Figure 2.28 shows the MISIMO testing board. MISIMO PCB board interfaces with field programmable gate array (FPGA) for testing purposes.The digital controller signals of MISIMO are monitored on Chipscope Pro by connecting the FPGA JTAG



① MISIMO Power Stage [0.48mm^2]
② Level Shifters and Drivers [0.013mm^2]
③ Zero Current Detector [0.0000845mm^2]
④ Source Hysteresis Comparators [0.00004mm^2]
⑤ Load Hysteresis Comparators [0.00004mm^2]
⑥ MISIMO Controller [0.002156mm^2]
⑦ Battery controlled pulse width generator Controller [0.0375mm^2]

Figure 2.26: Micrograph of the fabricated MISIMO die in 28nm FDSOI.

port to the computer by Xilinx platform cable USB II.

The implemented MISIMO chip harvests energy from up to three sources simultaneously: a PV cell at 0.2 to 1V, a TEG at 0.1 to 0.4V, and a BFC at 0.2 to 0.5V; all while independently regulating 3 different power rails (each between 0.4 and 1.4V). During testing, a real PV cell was connected to one of the inputs, while voltage sources with series resistors were used to model TEG and BFC sources to simplify testing. The TEG model values are computed from Micropelt Thermogenerator ($R_{TEG} = 526\Omega$), while the BFC model values are computed from the BFC measurement results in [38].

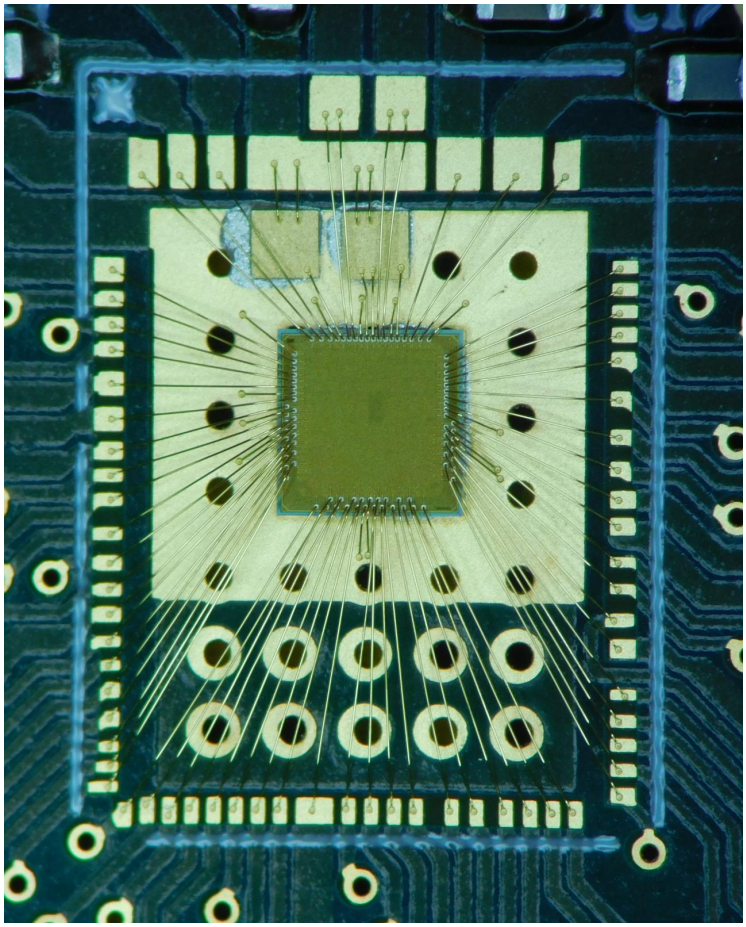


Figure 2.27: Micrograph of the wirebonded MISIMO chip on board.

A Keithley sourcemeter is connected to the battery terminal of the test chip alongside a large capacitor ($10\mu F$), so that power in and out can be measured. The source meter model used in testing is operating as a source and a sink.

Measurement in Figure 2.29 demonstrates the MISIMO PFM control under battery power. It shows the output voltage of the three loads under a turn-ON transient test, alongside the ZCD output, which used as a defacto asynchronous clock in the MISIMO converter. The ZCD output effectively indicates the inductor switching frequency. Immediately after turn-ON, the converter operates at the maximum switching frequency (500kHz), and once the outputs reach steady state, the frequency goes down in proportion to the load currents. This measurement result demonstrates that the MISIMO energy-harvesting chip can effectively regulate three independent loads at different volt-

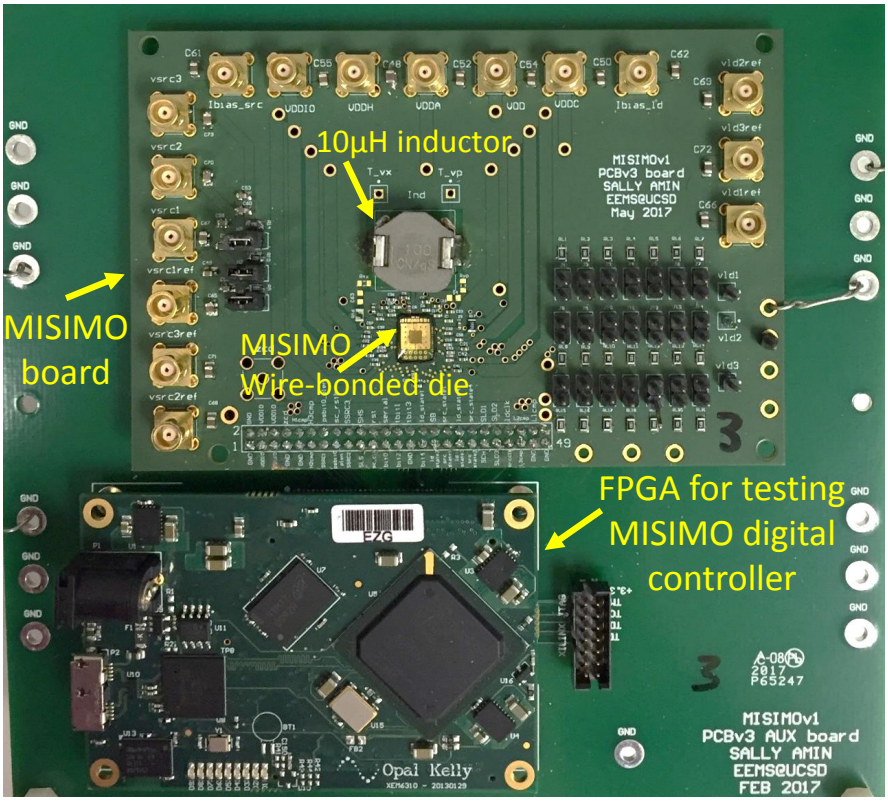


Figure 2.28: Photograph of MISIMO testing board.

ages and load condition with dynamic ON time and PFM control. Figure 2.30 shows a load-step response measurement and cross regulation test. Here, a load step is applied on one of the rails, and the measurement results demonstrate independent voltage regulation across the three loads with only 30mV ripple and negligible droop.

Measurements in Figure 2.31 shows the input voltage of two harvesting sources: a BFC and a TEG, alongside the output voltage of one of the loads: V_{Ld3}. It demonstrates that the MISIMO chip can simultaneously regulate input sources (to <15mV ripple for MPPT purposes) and output loads with the single-inductor. It also shows that load step has no effect on the source regulation or on the output voltage ripple, thanks to the proposed source/load decoupling technique.

Figure 2.32 shows an energy harvesting light step response measurement. This measurement demonstrates the capability of MISIMO to switch dynamically between different configurations. It shown the input voltage at the PV cell and the regulated

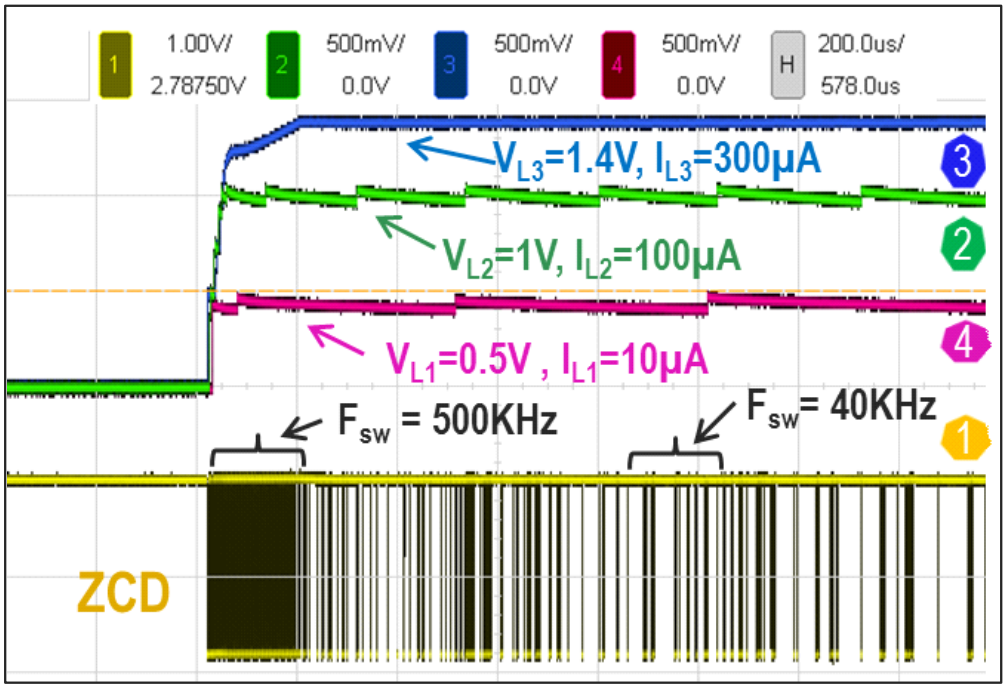


Figure 2.29: Measured turn-on transient demonstrating automatic PFM control.

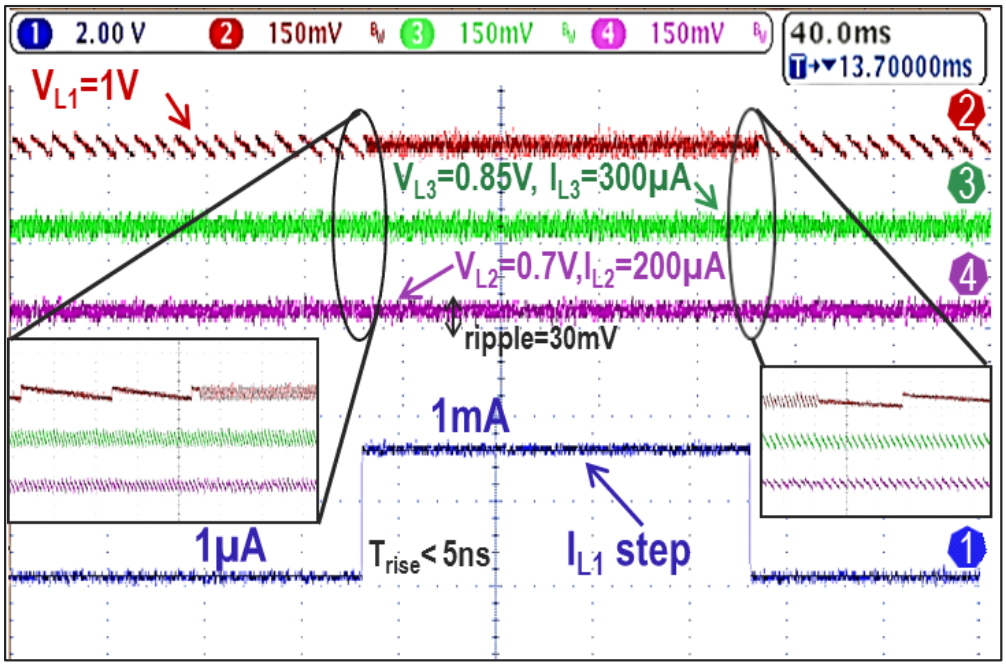


Figure 2.30: Measured load step under battery power demonstrating independent voltage regulation across all three loads.

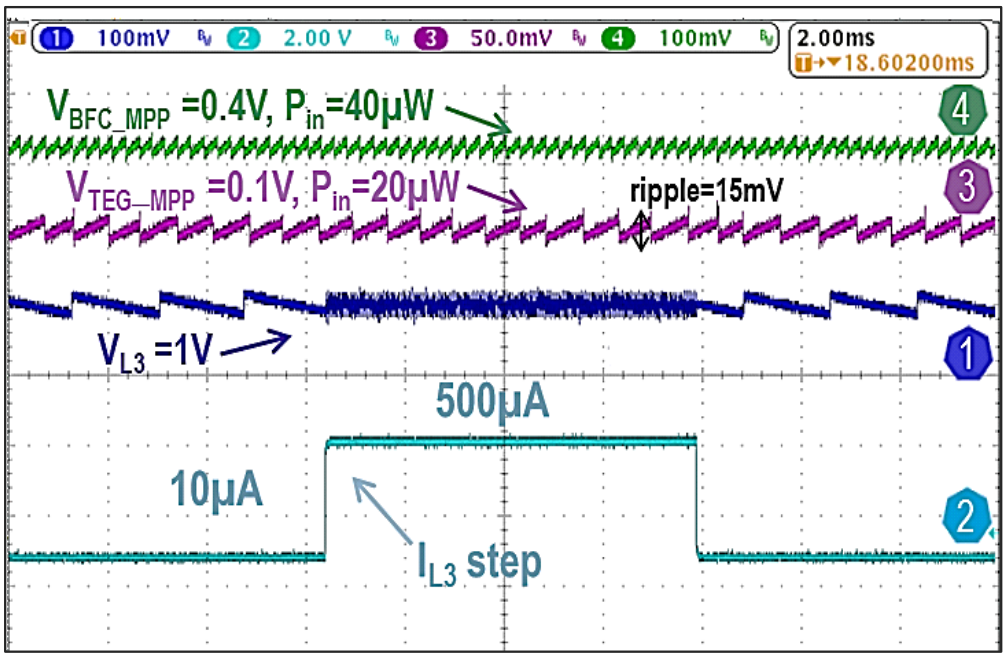


Figure 2.31: Measured load step response during energy harvesting demonstrating simultaneous source regulation (for MPPT) and load regulation.

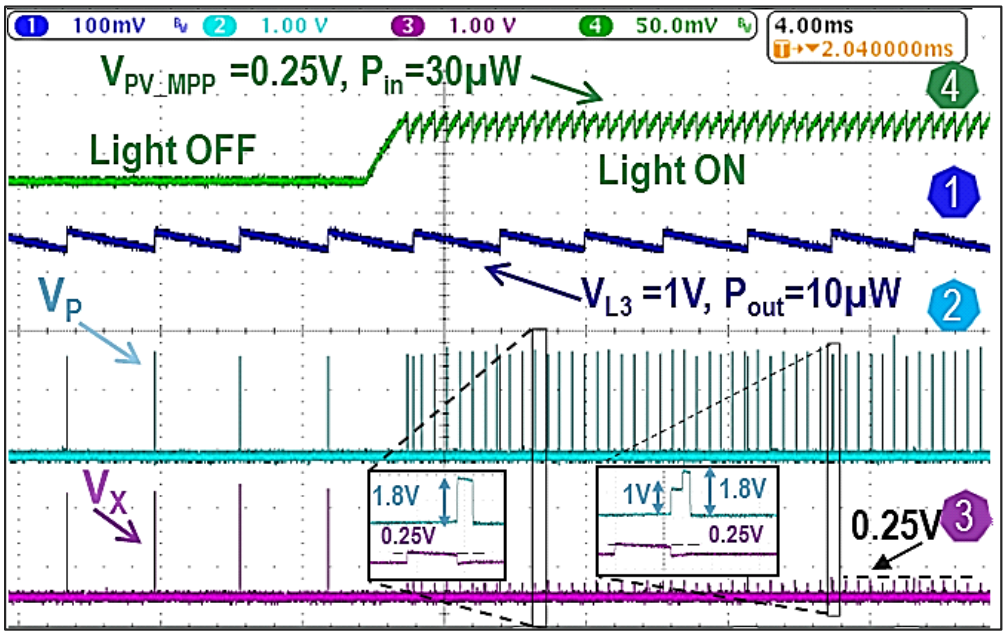


Figure 2.32: Measured source step response demonstrating the capability of MISIMO to dynamically switch between different configurations.

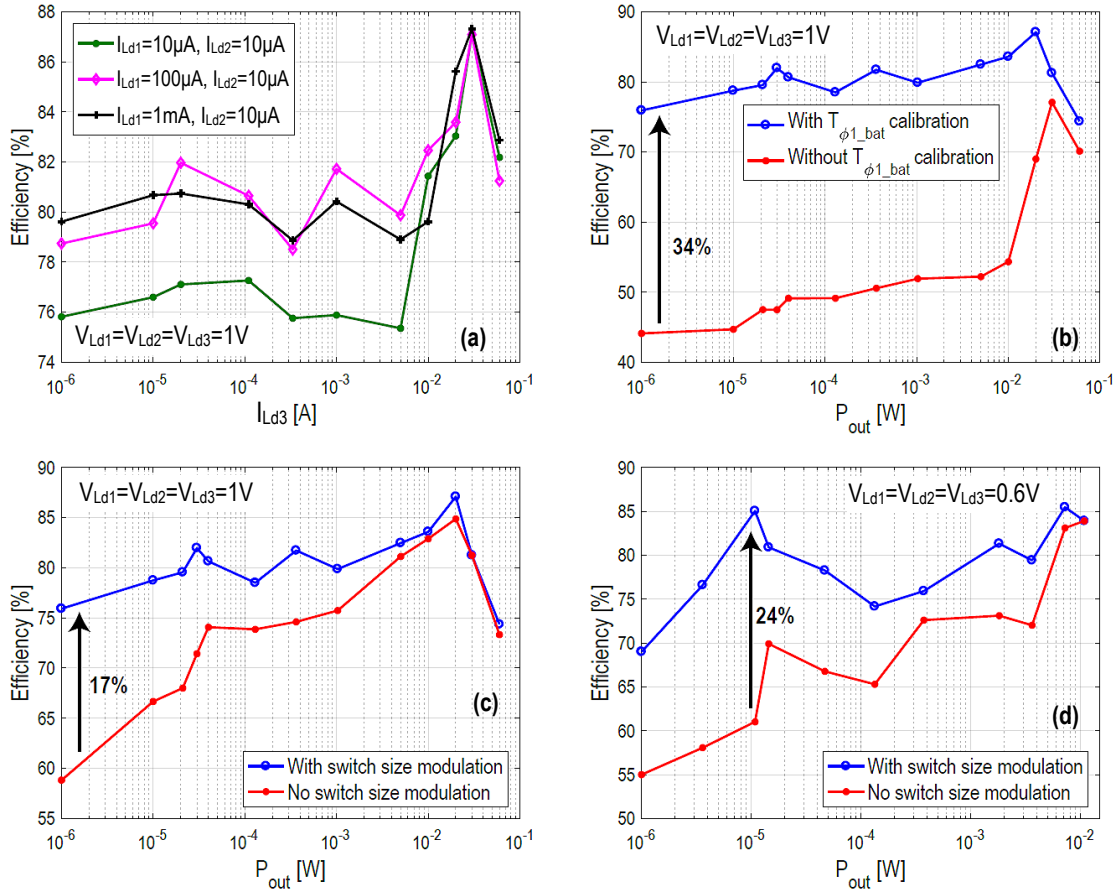


Figure 2.33: (a) Measured efficiency for all three loads vs. current in load three. (b) Measured efficiency improvement with dynamic $T_{\phi 1BAT}$ calibration. (c) Measured efficiency improvement with dynamic switch-size modulation at 1V. (d) Measured efficiency improvement with dynamic switch-size modulation at 0.6V.

output voltage. Also it shows the inductor terminals Vx and Vp to indicate the selected source and load in the inductor switching cycle. When light is OFF, the battery selected as source to deliver power to load. Once the light turned ON, the input voltage regulated around the VMPP and the PV selected to charge the battery and deliver power to the load directly.

Efficiency measurements in Figure 2.33 reveal a peak efficiency of 89% and an efficiency $> 75\%$ across all loads over a 60,000$\times$ dynamic range ($1\mu W - 60mW$) at $V_{out} = 1V$. Figure 2.33 (b) shows the measured efficiency for $1\mu W < P_{out} < 60mW$ with and without $T_{\phi 1-BAT}$ calibration. Measurements shows that $T_{\phi 1-BAT}$ calibration

improves the MISIMO efficiency by up to 34%. Figure 2.33 (c) and (d) show the efficiency measurements of MISIMO versus the output power with and without SSM at output voltage equals to 1V and 0.6V, respectively. It shows that the SSM technique improves the MISIMO efficiency by up to 24%.

Comparisons to prior work in Table 2.1 shows that the MISIMO chip is the first to perform MPPT harvesting from multiple sources while regulating multiple loads with a single inductor. The MISIMO chip achieves the widest dynamic range amongst prior-art multi-input harvesters, all in a small die area and with competitive efficiency. The fabricated converter achieves a peak efficiency of 89%, and supports output power range of $1\mu W$ to $60mW$ – i.e., a $60,000x$ dynamic range, with efficiency $> 75\%$ at $V_{out} = 1V$, and efficiency $> 69\%$ across $V_{out} = 0.6 - 1V$, thanks in part to the 3 different load regulation techniques: PFM, PWM, and SSM.

2.10 Conclusion

This chapter presented the design and implementation of MISIMO energy harvester platform on 28nm FDSOI. The demonstrated MISIMO energy harvester platform meets the needs of small form-factor net-zero-energy systems by aggregating the maximum power from three different energy source and independently regulating three different power rails in a single-stage single-inductor architecture. The proposed architecture decoupled the input source regulation from the output load regulation by allowing excess inductor energy to recycle back to the battery. The MISIMO converter performed 2D MPPT at the source side by dynamically adapting the inductor charging time and frequency, hence, improving the MPPT efficiency. Multiple load regulation actions were performed within a single inductor switching cycle to reduce the switching losses by 3×. The MISIMO chip utilized different load regulation techniques: PFM, PWM, and SSM to achieve high efficiency across wide dynamic range. Measurements showed that calibrating $T_{\phi 1-BAT}$ and SSM improve efficiency by up to 34% and up to 24%, respectively.

Table 2.1: Comparison of the proposed MISIMO converter to State-of-The-Art.

	Bandyopadhyay, JSSC'12 [5]	Shrivastava, VLSI'14 [16]	Yu, JSSC'15 [17]	Chen, ISSCC'15 [15]	Damak, VLSI'15 [14]	*Lu, ISSCC'16 [31]	Chowdary, JSSC'16 [9]	This Work
Technology	0.35µm	0.13µm	0.18µm	0.5µm	0.18µm	0.35µm	0.18µm	**28nm**
No of inputs	3+battery	1+battery	1+battery	1+battery	1+battery	1+battery	3+supercap	**3+battery**
No of outputs	1+battery	3+battery	2+battery	1+battery	1+battery	1+battery	1+supercap	**3+battery**
Converter architecture	2-stage, 1-ind Buck/Boost	2-stage, 1-ind Buck/Boost	1 stage, 1-ind Buck-Boost	1-stage, 1-ind Buck/Boost	2 stage-1ind Buck-Boost	1-stage, 1-ind Buck-Boost	2-stage, 1-ind Buck-Boost	**1-stage, 1-ind** Buck-Boost
Energy sources (input voltage)	PV(0.15-0.75V) Piezo(1.5-5V) TEG(0.02-0.16V) Battery (3.3V)	PV (0.38-3.3V) Battery (<5V)	PV (2.6V) Battery (3V)	PV (3.6V) battery (4V)	PV(0.14-0.62V) Battery (3V)	PV (0.03-3.6V) Battery (<3.6V)	PV Piezo RF	PV (0.2-1V) TEG (0.1-0.4V) BFC (0.2-0.5V) Battery (1.8V)
Load regulation mechanism	PFM	PFM I_{pk} Control	PFM	PFM	PFM	PFM	PFM	**PFM+PWM+SSM**
MPPT mechanism	Adaptive T_{on} Fixed F_{sw}	Constant T_{on} Vary F_{sw}	Constant T_{on} Vary F_{sw}	Constant T_{on} Vary F_{sw}	Vary T_{on} Vary F_{sw}	N.R	Constant I_{pk} Vary F_{sw}	**Adaptive T_{on} Adaptive F_{sw}**
L	22µH	20µH	10µ	4.7µH	47µ	22µH	47µH	10µH
C_L	15µF	8µF	10µ	4.7µF	NA	4.7µF	10µF	1µF
Die area (mm2)	~15	2.25	4.62	0.5	2.12	4	1.1	0.5
V_{out} (V)	1.8V	1.2, 1.5, 3.3V	1V, 1.8V	1-3.3V	1V	3.6V	1.2V-1.8V	0.4-1.4V
Quiescent P/I	2.7µA @V_{DD}=1.8V	1.2 µW	0.4µA @V_{DD}=1V	1µA @V_{DD}=4V	3.2nA @V_{DD}=1V	200nA	18nA	**262nA @V_{DD}=1V**
Output power (P_{out})	9µW~540µW	<100mW	1µW ~ 10mW	1µW~15mW	50n~1µW	N.R.	60nW~40µW‡	1µW-60mW
Dynamic range (DR)	60X	10,000X‡	10,000X	15,000X	20	N.R.	667X‡	**60,000X**
Peak efficiency (η_{pk})	90%	92%	83%	93%	~80-87%	85%	87%	**89%**

***** Load is regulated from an LDO if the harvester energy is not available

N.R.: Not Reported

‡ Estimated from plotted data

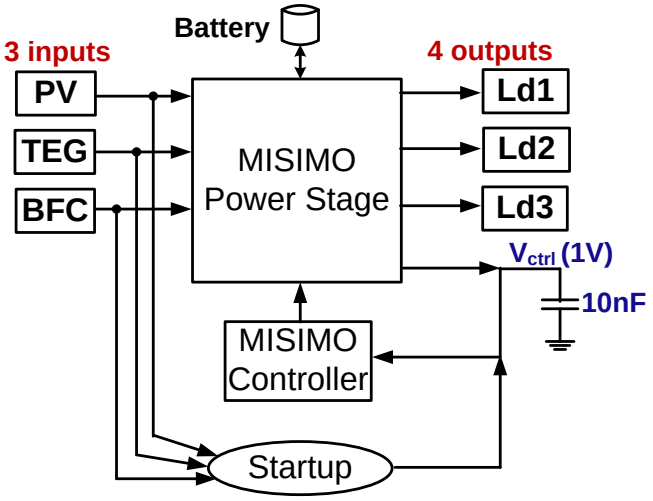


Figure 2.34: Self-powerd and self-starting MISIMO.

2.11 Future Direction

Self-Powered and Self-Starting MISIMO

Figure 2.34 shows the top-level architecture of a self-powered and self-starting MISIMO. MISIMO can generate and regulate additional output rail, V_{ctrl}, to supply its controller. However, a startup circuit is required to initially generates V_{ctrl} rail till MISIMO becomes self-sustained and power itself. The available energy from the harvesting sources can be utilized to initially generate V_{ctrl} using startup circuits. Once $V_{ctrl} = 1V$ generated, the startup circuits disabled and MISIMO starts normal operation while regulating the V_{ctrl} power rail.

Startup Architecture

Extensive research effort has been done to develop startup circuits for energy harvesting [42–44]. Figure 2.35 shows a PV starup architecture as an example for a single input startup. It consists of 9-stages ring oscillator, non-overlap, buffer, 4-stages cross-coupled charge pump, and control voltage capacitance. The ring oscillator generates the clock for a cross coupled bootstrap to up convert the harvester voltage to the desired control voltage, $V_{ctrl} = 1V$. Once $V_{ctrl} = 1V$ detected, the startup circuits

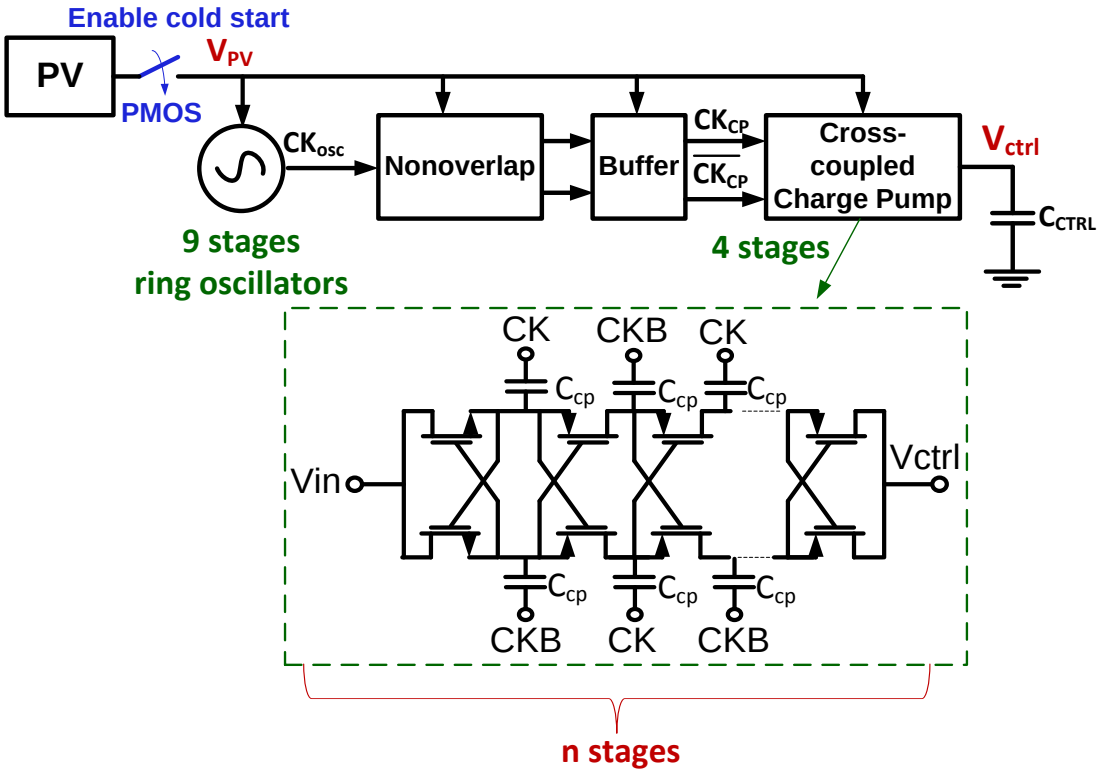


Figure 2.35: PV startup architecture.

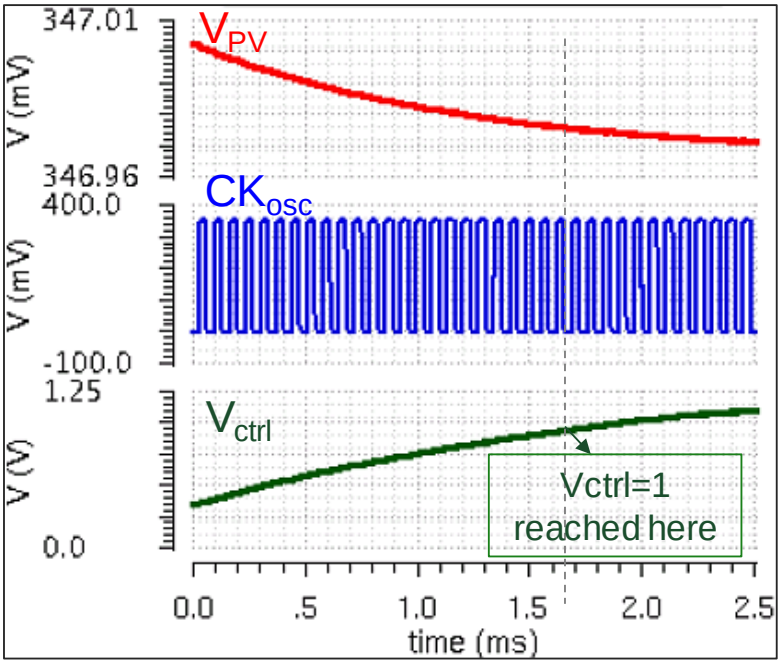


Figure 2.36: Simulation results on 28nm FDSOI for startup from PV cell.

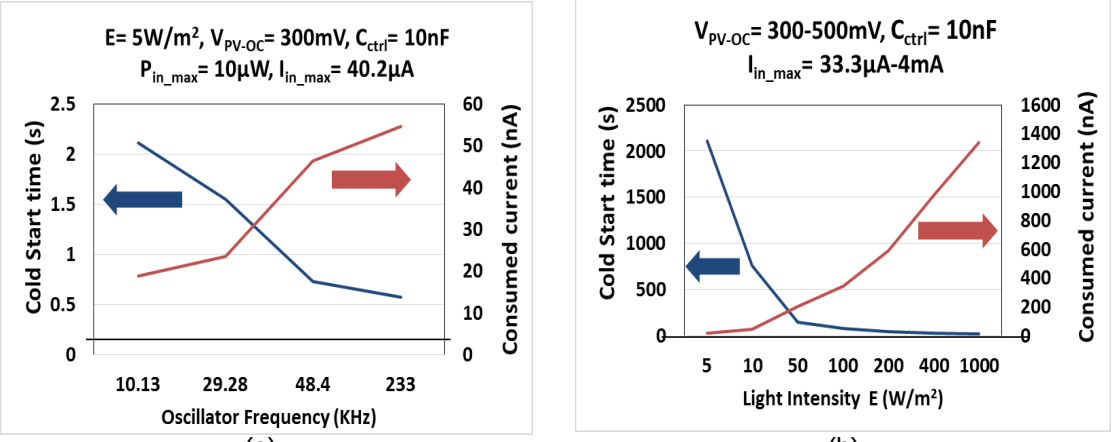


Figure 2.37: PV startup time and consumed current versus (a) oscillator frequency and (b) light intensity.

disabled and MISIMO starts normal operation. Figure 2.36 shows simulation results on 28nm FDSOI for a startup from PV cell. The same architecture can be used for TEG and BFC harvesting sources but with appropriate choice for the number of stages for the ring oscillator and charge pump, based on the harvesting source voltage and current range. For example, a TEG cell would require 11-stages cross-coupled charge pump instead of 4-stages to up convert the MISIMO input voltage that can go as low as 100mV to 1V.

Figure 2.37 shows the trade-off between the startup time and the consumed current. Figure 2.37(a) shows that as the oscillator frequency increases, the startup time decreases and the current consumption increases. While Figure 2.37(b) shows that as the light intensity increases, the startup time decreases and the current consumption increases.

Proposed Multi-input Startup

Figure 2.38 shows the proposed multi-input startup circuits for the 3-input harvesting sources: PV, TEG, and BFC. The single input startup architecture in Figure 2.35 used for the three different harvesting sources, then a cross coupled pMOS-based structure added to pass only the highest output voltage and avoid reverse current. This multi-input startup architecture doesn't allow power aggregation but rather selects the har-

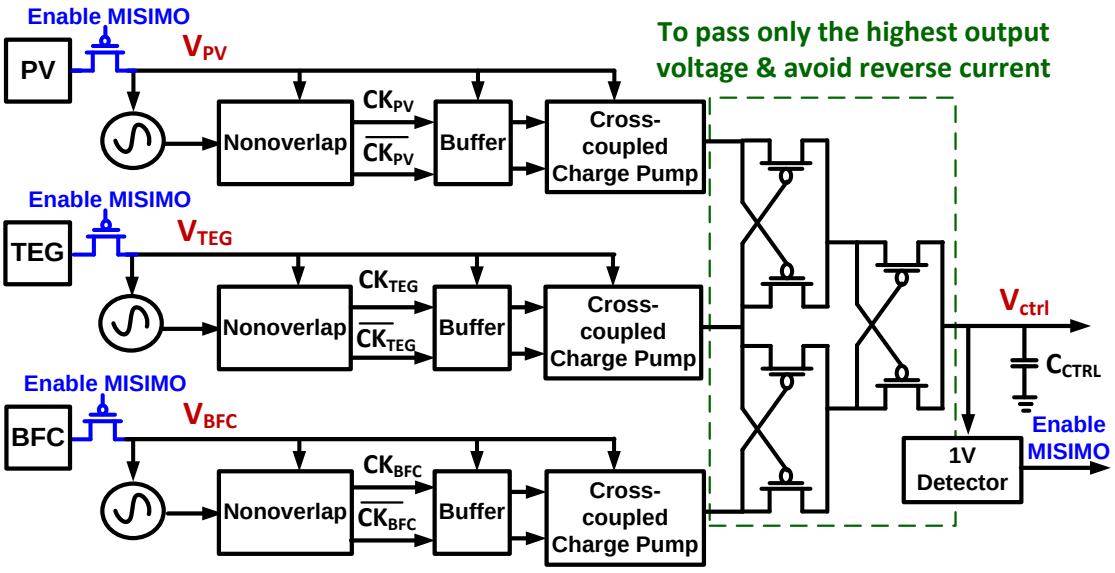


Figure 2.38: Proposed MISIMO startup architecture.

vester with the highest power. Future work should explore architecture that aggregates power from multiple inputs to speed up the startup.

2.12 Acknowledgement

Chapter 2 is based on and mostly a reprint of the following publications:

- S. S. Amin and P. P. Mercier, "MISIMO: A multi-input single-inductor multi-output energy harvester employing event-driven MPPT control to achieve 89% peak efficiency and a 60,000x dynamic range in 28nm FDSOI," *IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, 2018, pp. 144-146.

- S.S. Amin and P.P. Mercier, "MISIMO: A Multi-Input Single-Inductor Multi-Output Energy Harvesting Platform in 28nm FDSOI for Powering Net-Zero-Energy Systems," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 12, Dec. 2018.

The dissertation author is the primary investigator and author of the work in these papers.

Chapter 3

A Fully-Integrated Li-ion-Compatible Hybrid 4-Level DC-DC Converter in 28nm FDSOI

Next generation wearable and Internet of Things (IoT) devices require small form-factor implementations. Typically, most circuits, including computation, sensing, and wireless communications, are integrated on a single system-on-chip (SoC), implemented in scaled CMOS (e.g., $\leq$ 28nm), which operates at 0.6-1V. However, such devices are typically powered by Li-ion batteries, which provide voltages on the order of 2.8-4.2V. Since the high Li-ion voltage range is not compatible with the low voltage requirements of the system implemented in scaled technologies, a DC-DC converter must be placed between the battery and load.

Typically, the required DC-DC converter is implemented as a discrete power management IC (PMIC), fabricated in large geometry technologies (e.g., $\geq 180nm$) that can natively handle the high battery voltage. To achieve high efficiency, PMICs typically utilize inductive switching topologies using off-chip inductors as shown in Figure 3.1(a). However, once the supply is brought on-chip, a low drop-out regulator (LDO) is used to support dynamic voltage scaling [45], which degrades end-to-end system efficiency. Additionally, the employed off-chip inductors are large, which results in increased PCB design complexity/cost and increased overall system size.

To build a small form-factor power management solution compatible with the needs of next-generation wearable and IoT devices, it is desired to integrate all DC-DC conversion and supply regulation functionality into the SoC itself as shown in Fig-

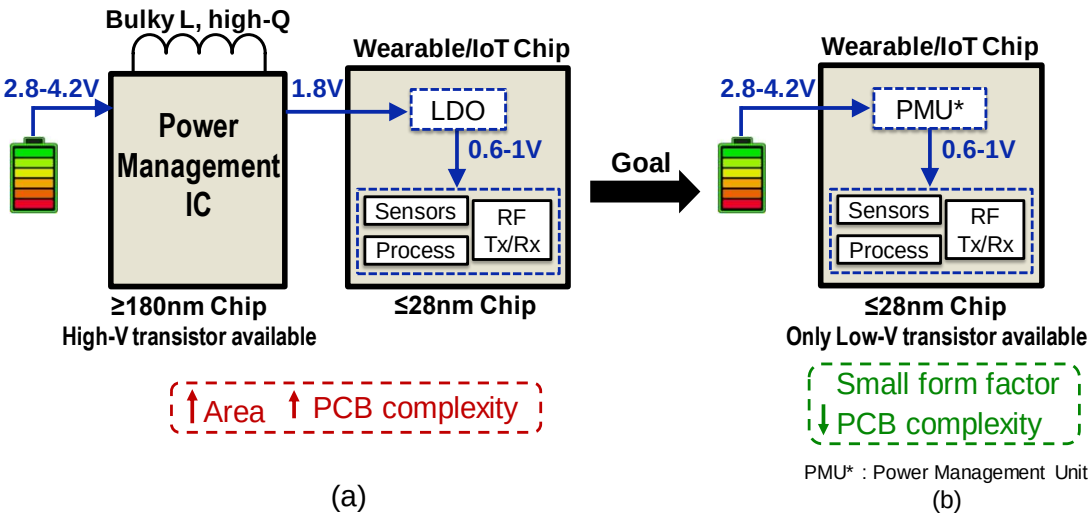


Figure 3.1: (a) Conventional PMIC for powering scaled CMOS SoCs. (b) Proposed concept for a fully-integrated Li-ion-compatible voltage regulator.

ure 3.1(b). There are two primary challenges here: most scaled processes do not have transistors that natively support Li-ion voltages, and the quality of on-chip passives are typically not nearly as good as what is available off-chip. Fortunately, it is possible to stack low-voltage transistors to support high voltage blocking capabilities, and furthermore, the small parasitic capacitance of scaled transistors can allow high switching frequencies, which can shrink the size of the switching passives to the point where they can be reasonably integrated on-chip. Additionally, the high switching frequency enables fast transient voltage tracking and reduced voltage droop. However, stacking transistors does invoke additional loss mechanisms and can complicate the control signals generation, while the use of conventional converter topologies may not exploit the available energy or power density of on-chip passives to the fullest extend possible.

This chapter presents a fully-integrated modified 4-level hybrid converter that achieves up to 78% efficiency when converting from 2.8-4.2V to 0.6-1.2V using low-voltage transistors and on-chip passives in 28nm FDSOI. The following sections are organized as follows: Section 3.1 summarizes the prior-art fully-integrated DC-DC converter architectures in Section 3.1. Section 3.2 describes a conventional 2-level buck solution, a conventional 4-level hybrid, and then introduces the modified 4-level hybrid

topology. Section 3.3 then describes the power stage parasitic model and associated losses, while comparing the results of different topologies. Section 3.4 discusses circuit implementation details, with specific emphasis on the driver architecture and the proposed level shifter. Finally, measurement results are presented in Section 3.5.

3.1 Li-Ion-Compatible Fully-Integrated Architectures

3.1.1 Prior Work

Integrated DC-DC conversion can occur either via linear regulation or via switching converters, the latter of which is preferred for efficiency reasons. In either case, conversion can occur from a low, PMIC-derived supply voltage , or directly from the Li-ion battery , the latter of which is preferred for miniaturized systems.

Existing switching converter architectures include on-chip buck converters [46], buck converters with magnetic coupling [47, 48], switched capacitor (SC) converters [49–53], and 3-level converters [54, 55]. While the cited work are all fully-integrated, the input voltage is limited by the maximum voltage supported by the technology, which is unfortunately not compatible with Li-ion battery voltages, and thus an external PMIC is still necessary with such approaches.

Some other prior work has implemented fully-integrated SC converters compatible with Li-ion voltages, though they were implemented in technologies that include high voltage transistors [56–59], not in deeply scaled CMOS where such transistors are not available. In addition, while SC converters can, with careful design, achieve high efficiency and/or power density [60], this only occurs at discrete ratios of input to output due to fundamental charge sharing losses, limiting their utility in applications where DVS or arbitrary output voltages are required. Increasing the number of SC ratios can help (to, for example, >10), though complex switch structures may make large volt-

age compatibility and/or achievement of high power density difficult [58, 61]. For these reasons, to date there have not been any scaled-CMOS-integrated switched-capacitors converters that are compatible with Li-ion voltages and that achieve high efficiency and power density over a large input and output voltage range.

Since SC converters have not been pragmatic for Li-ion-compatible DVS-enabled applications, others have examined the possibility of integrating the inductor of a buck converter into the SoC. Unfortunately, such work achieved efficiency improvements over an ideal LDO of only 2% in [46] and up to 20.4% in [47,48] by using magnetic coupling, all at substantially larger area than an LDO and, importantly, at low (i.e., non Li-ion-compatible) voltage conversion ratios. The poor quality of available on-chip inductors (due to high ESR) result in high conduction losses and severe efficiency degradation over converters that utilize off-chip inductors. In addition, the very low on-chip inductor value (nH range) results in a high switching frequency (100s of MHz), that result in high switching losses and further efficiency degradation. Thus, conventional 2-level buck topologies are not well suited for fully-integrated battery-connected converter in scaled CMOS unless the quality of on-chip inductors can be substantially improved. While it has been shown that it is possible to integrate a Li-ion-compatible buck converter in a scaled technology by stacking the available low voltage transistors in buck converter [62, 63], such prior work utilized a bulky off-chip inductor to achieve high efficiency.

Multilevel converters [54,55] enable wide input/output voltage range and achieve higher overall efficiency by merging the benefits of inductive and capacitive converters. Specifically, the flying capacitors in a multilevel converter reduce the voltage swing seen at the switching terminal of the inductor, and hence reduce the switching frequency and improve the overall efficiency. Additionally, the inductor helps to soft charge/discharge the capacitors [64], eliminating charge sharing losses towards increased efficiency and/or power density. Thus, multilevel converters make better use of passives than conventional SC or buck topologies, which, due to the poor quality of on-chip passives, make multilevel topologies an attractive choice for fully-integrated

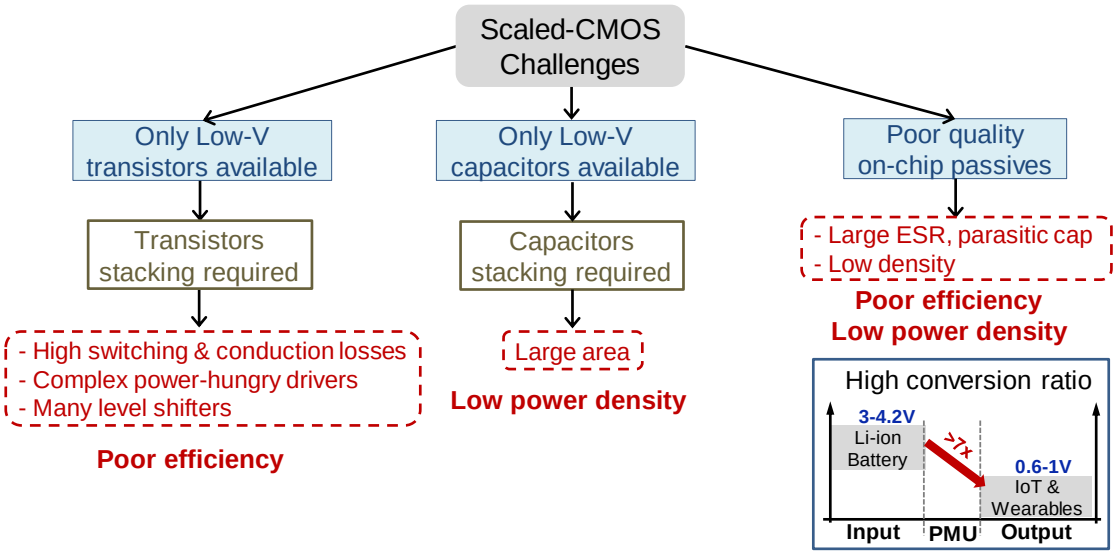


Figure 3.2: Li-ion Fully-Integrated PMU challenges in 28nm FDSOI.

converters. However, to-date, there have not been any demonstrations of fully-integrated Li-ion-compatible multilevel converters implemented in scaled CMOS processes.

3.1.2 Challenges of Integrating Li-ion Converters in Scaled CMOS

The main challenges of integrating Li-ion-compatible converters in scaled CMOS (e.g., $\leq 28nm$) are illustrated in Figure 3.2. First, the voltage blocking capabilities of scaled CMOS processes tend to be low (e.g., 1.5V in 28nm). As a result, it is necessary to stack transistors on top of one another to distribute the voltage stress and support the Li-ion voltage range. Unfortunately, stacking transistors tends to increase conduction and switching losses, and may require complex and power hungry drivers with many level shifters to generate the appropriate gate drive signals. Second, high-density capacitors in scaled CMOS processes also tend to have low voltage blocking capabilities (e.g., 1.5V in 28nm), and thus it is necessary to stack capacitors to block high voltages, which increases area and thus decreases power density. Third, the quality and size of on-chip passives, particularly inductors, tends to be poor in scaled CMOS. Poor quality

passives increases losses, and increasing the size of the passives to mitigate losses tends to reduce power density. Finally, DC-DC conversion must occur not at 2:1 ratios, but rather over much larger, 7:1 ratios to support Li-ion voltages (e.g., up to 4.2V) and low load voltages (e.g., down to 0.6V). It is generally much more difficult to achieve high efficiency at large conversion ratios compared to low conversion ratios.

This work overcomes the aforementioned challenges and enables Li-ion compatible fully-integrated DC-DC conversion in scaled CMOS by: 1) stacking three 1.5V-transistors to block the input voltages up to 4.5V when driving an inductor in a buck configuration; 2) connecting flying capacitors to the exiting internal nodes of the stacked 2-level buck converter, converting the nominal 2-level buck converter into a 4-level hybrid converter, which reduces the switching frequency by up to 23x for an up to 33% efficiency improvement; 3) soft-charging/discharging the capacitors through the inductor, thereby eliminating capacitor charge sharing losses (which tend to dominate the losses in SC converters); 4) modifying the 4-level converter by changing the switching states of the flying-capacitor circuit to reduce the steady-state voltage on the first flying capacitor and reducing its implementation area by $4\times$; 5) operating the converter in discontinuous conduction mode (DCM) to achieve high efficiency at low loads; 6) adding freewheel switches across the inductor to improve the efficiency and reliability in the zero current switching phase with negligible effect on losses; 7) exploiting the naturally switching voltages across the flying capacitors as power/gnd rails for the power stage drivers, eliminating the need for dedicated power rails, level shifters, or power-hungry stacked drivers.

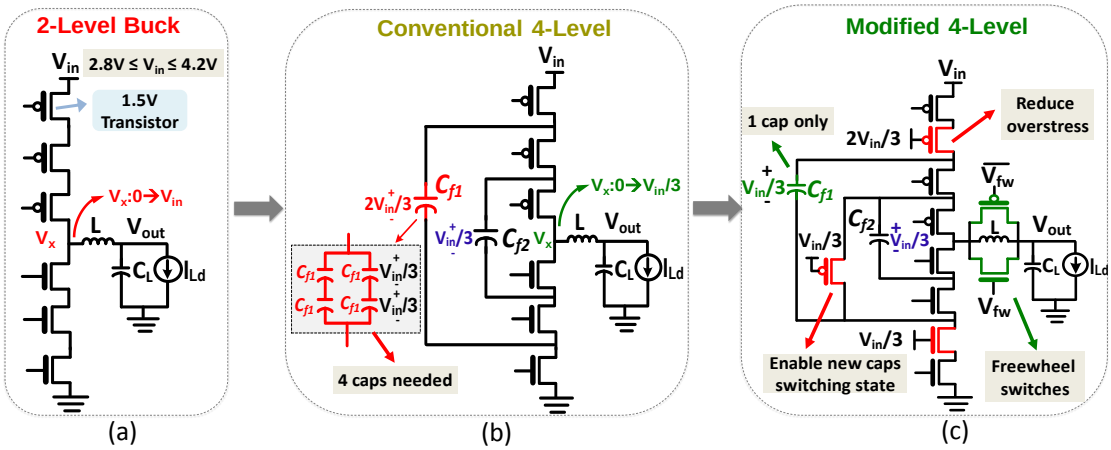


Figure 3.3: (a) Conventional stacked 2-level buck. (b) Conventional way to convert a stacked 2-level buck to a hybrid 4-level converter. (c) Proposed modified 4-level topology.

3.2 Building a Li-ion-Compatible DC-DC Converter in 28nm

3.2.1 Starting Point: Stacked 2-Level Buck

If a conventional 2-level buck converter was to be implemented in 28nm using the available 1.5V-transistor, at least 3 stacked transistors would be required to block 4.2V as shown in Figure3.3 (a). When operating in the discontinuous conduction mode (DCM), the switching frequency of the 2-Level buck is given by:

$$F_{sw-2L} = \frac{2I_{Ld}V_{in}CR(1-CR)}{LI_{pk}^2}, \tag{3.1}$$

where I_{Ld} is the load current, CR is the conversion ratio (i.e., $CR = V_{out}/V_{in}$), and I_{pk} is the peak inductor current. As mentioned in Section 3.1, the poor quality of on-chip inductor makes the 2-Level buck not suitable for the implementation of a fully integrated battery-connected PMU in scaled CMOS. The large ESR results in high conduction losses and the small on-chip inductor increases the switching frequency to 100s of MHz, increasing the switching losses and result in a poor efficiency.

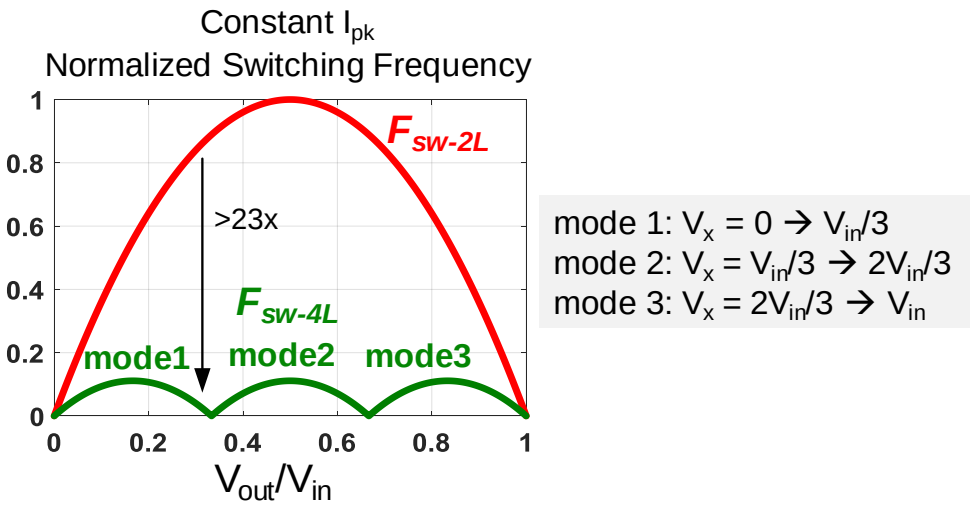


Figure 3.4: Normalized switching frequency versus the conversion ratio, for the 2-level buck and the 4-level converter, operating in DCM with constant peak current I_{pk}.

3.2.2 Improving Efficiency: 4-Level Converter

A) 4-Level: Favorable for Converters with Off-Chip Passives

Given that the stacked transistors are necessary, it is advantageous to exploit the existing internal nodes of the nominally 2-level buck, and add flying capacitors to convert the 2-Level buck into a 4-level converter, as inspired by the 3-level work in [54], and shown in Figure3.3 (b). The hybrid converter in Figure 3.3(b) utilizes the high density flying capacitors to reduce the swing at the inductor terminal, V_x, from V_{in} to $V_{in}/3$. As a result, the switching frequency of the 4-level converter operating in DCM is:

$$F_{sw-4L} = \begin{cases} \frac{2I_{Ld}V_{in}CR(1/3-CR)}{LI_{pk}^2} & 0 < CR < 1/3; \\ \frac{2I_{Ld}V_{in}(CR-1/3)(2/3-CR)}{LI_{pk}^2} & 1/3 < CR < 2/3; \\ \frac{2I_{Ld}V_{in}(CR-2/3)(1-CR)}{LI_{pk}^2} & 2/3 < CR < 1. \end{cases} \tag{3.2}$$

Figure 3.4 shows the normalized switching frequency versus the conversion ratio, for the 2-level buck and the 4-level converter, operating in DCM with constant peak current. The figure shows that for the same value of inductor, the 4-level converter can

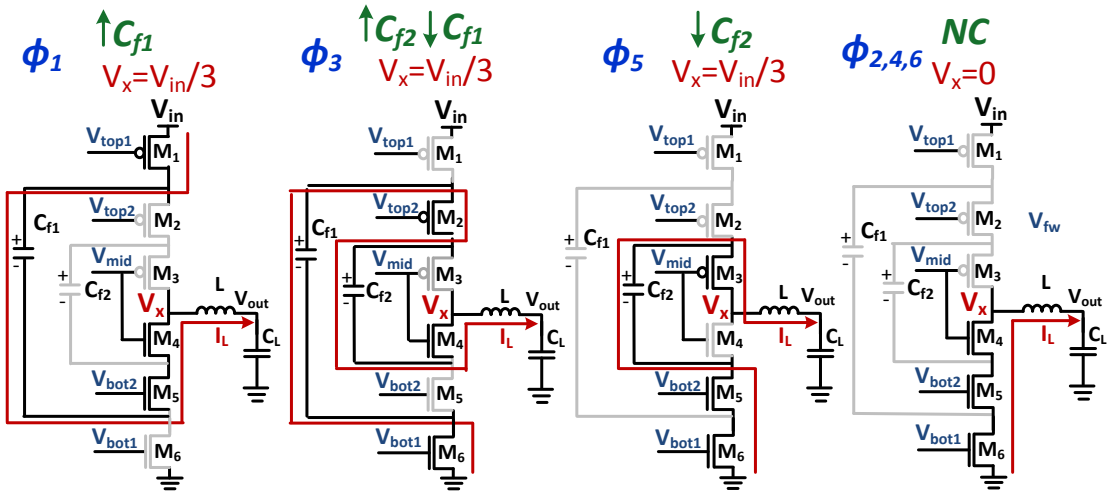
reduce the switching frequency by $> 23\times$, which is translated into up to 33% improvement in the efficiency, making this topology promising for a fully-integrated battery-connected PMU in scaled technology.

The 4-level converter has three different modes of operation to support an output voltage from 0 to V_{in}, and the name 4-level comes from the fact that V_x node takes four different values: 0, $V_{in}/3$, $2V_{in}/3$ and V_{in}. More specifically, V_x switches between 0 and $V_{in}/3$ (mode 1) or $V_{in}/3$ and $2V_{in}/3$ (mode 2) or $2V_{in}/3$ and V_{in} (mode 3), to enable output voltage range: $0 < V_{out} < V_{in}/3$, $V_{in}/3 < V_{out} < 2V_{in}/3$, and $2V_{in}/3 < V_{out} < V_{in}$, respectively. At the boundary of the operating modes (i.e at $CR = 1/3,\ 2/3,\ 1$), the inductor current ripple is approaching 0 and the converter operates as SC converter. Since the target output voltage of a fully-integrated converter in scaled CMOS will typically range from 0.6 to 1.0V when converting from a Li-ion battery that varies between 2.8-4.2V, mode 1 would be the primary mode of operation. Other modes of operation are discussed in Section 3.6.3.

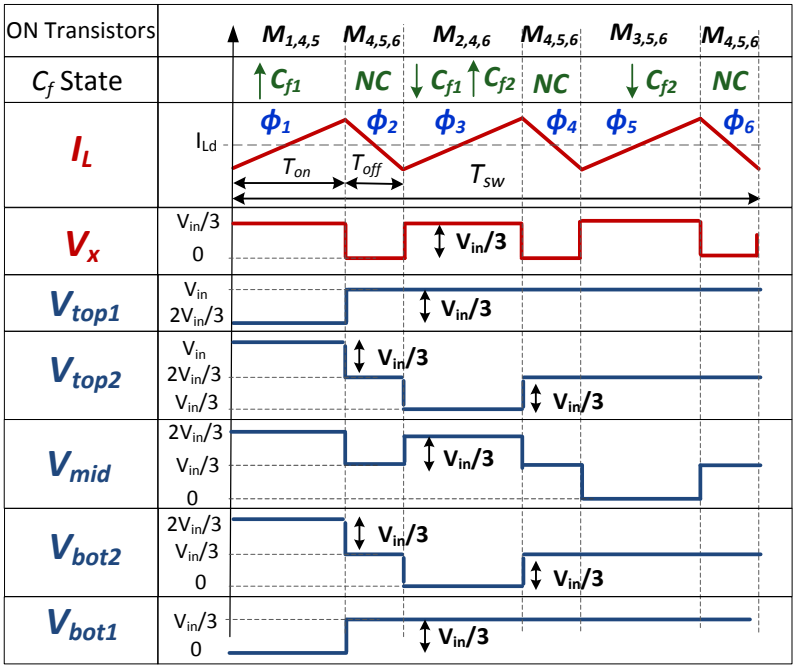
Figure 3.5(a) shows the inductor current path in different switching phases for the 4-level converter operating in mode 1, along with the equivalent voltage at V_x and the flying capacitors state. The timing diagram of the power stage gate signals are shown in Figure 3.5(b). As shown, the gate-to-source, V_{gs}, gate-to-drain, V_{gd}, and drain-to-source, V_{ds}, voltages of each power stage transistor in each phase never exceeds $V_{in}/3$. Thus, no transistor exceeds its maximum voltage rating, even at the highest compatible V_{in}. In each switching phase, the flying capacitors C_{f1} and C_{f2} are either charging, discharging, or not connected (NC), such that, the capacitors charge is balanced at the end of ϕ_6. The inductor switching phases of the 4-level converter operating in mode 1, can be described as following:

- Phase ϕ_1: M_1, M_4 and M_5 are turned ON, while C_{f1} is charged and C_{f2} is NC. The voltage on V_x node can be described as: $V_x = V_{in} - V_{f1}$.

- Phases $\phi_{2,4,6}$: M_4, M_5, and M_6 are turned ON, C_{f1} and C_{f2} are NC, and $V_x = 0$.



(a)



(b)

Figure 3.5: (a) Four-level converter current path in different inductor switching phases, operating on mode 1: $0 < V_{out} < V_{in}/3$. (b) Equivalent Power stage gate signal timing diagram.

- Phase ϕ_3: M_2, M_4, and M_6 are turned ON, while C_{f1} is discharged and C_{f2} is charged. The voltage on V_x node can be described as: $V_x = V_{f1} - V_{f2}$.

- Phase ϕ_5: M_3, M_5, and M_6 are turned ON, while C_{f1} is NC and C_{f2} is discharged. The voltage on V_x node can be described as: $V_x = V_{f2}$.

In steady state: $V_{f1} = 2V_{in}/3$, $V_{f2} = V_{in}/3$, and V_x equals 0 in $\phi_{2,4,6}$, and $V_{in}/3$ in $\phi_{1,3,5}$.

B) Modified 4-Level: Favorable for Fully-Integrated Converter with ON-Chip Passives

While the 4-level topology in Figure 3.3(b) improves the efficiency over the 2-level buck and supports operation from a Li-ion battery without additional power switches, the steady state voltage across the flying capacitor C_{f1} equals $2V_{in}/3$. If implemented using the available high-density 1.4V capacitors, capacitor stacking of C_{f1} would be required, resulting in a flying-capacitor that is 4$\times$ the implementation area of C_{f2} for the same amount of capacitance.

To reduce the voltage stress on C_{f1} and eliminate its area penalty, a modified 4-level topology, shown in Figure 3.3(c), is proposed and fabricated in this work. The switching states of the flying capacitors are changed to reduce the voltage stress on C_{f1} from $2V_{in}/3$ to V_{in}/3, thereby reducing the C_{f1} implementation area by 4$\times$. Here, three extra power switches are added: two in series with the stack to reduce the voltage stress on the top and the bottom switches, and one in parallel to enable the new capacitor switching state. For the same total area as the 4-level topology in Figure 3.3(b), the proposed modified 4-level topology in Figure 3.3(c) can utilize larger passives, and thus achieves up to 12% higher overall efficiency, even when including the losses of the additional power switches.

The proposed converter operates in DCM to achieve high efficiency over low output current ranges appropriate for IoT applications. If the inductor were left floating during the zero switching phase, large ringing may present itself at the V_x node,

potentially over-stressing the power switches. To prevent this from occurring, a pair of freewheel switches that help to eliminate ringing are added. The freewheel switches turn ON only when the inductor current is nearly zero so they do not contribute to conduction losses. Therefore, the freewheel switches are sized small relative to the main power stage switches, making them not contribute to tangible switching losses either. Thus, the freewheel switches have a negligible effect on the overall achievable efficiency.

Figure 3.6 shows the power stage inductor current path, the flying capacitors state, and the V_x node voltage of the proposed modified 4-level during each inductor switching phase. Figure 3.7 shows the corresponding timing diagram of the power stage gate signals. The gate voltage of the power stage transistors in each phase is set such that V_{gs}, V_{gd}, and V_{ds} for each transistor do not exceed the maximum voltage of $V_{in}/3$. In each switching phase, flying capacitors C_{f1} and C_{f2} are either charging, discharging, or not connected (NC), such that the capacitor's charges are balanced at the end of ϕ_6. The inductor switching phases of the modified 4-level converter can be described as following:

- Phase ϕ_1: M_1, M_{1s}, M_4 and M_7 are turned ON, while C_{f1} and C_{f2} are charging. The voltage on V_x node can be described as: $V_x = V_{in} - V_{f1} - V_{f2}$.

- Phases $\phi_{2,4,6}$: M_4, M_5, M_{6s} and M_6 are turned ON, C_{f1} and C_{f2} are NC, and $V_x = 0$.

- Phase ϕ_3: M_2, M_3, M_{6s} and M_6 are turned ON, while C_{f1} is discharged and C_{f2} is NC. The voltage on V_x node can be described as: $V_x = V_{f1}$.

- Phase ϕ_5: M_3, M_5, M_{6s} and M_6 are turned ON, while C_{f1} is NC and C_{f2} is discharged. The voltage on V_x node can be described as: $V_x = V_{f2}$.

- Phase ϕ_{FW}: M_{fwn}, M_{fwp} are turned ON, and the inductor terminals are shorted to V_{out} to avoid ringing in this phase.

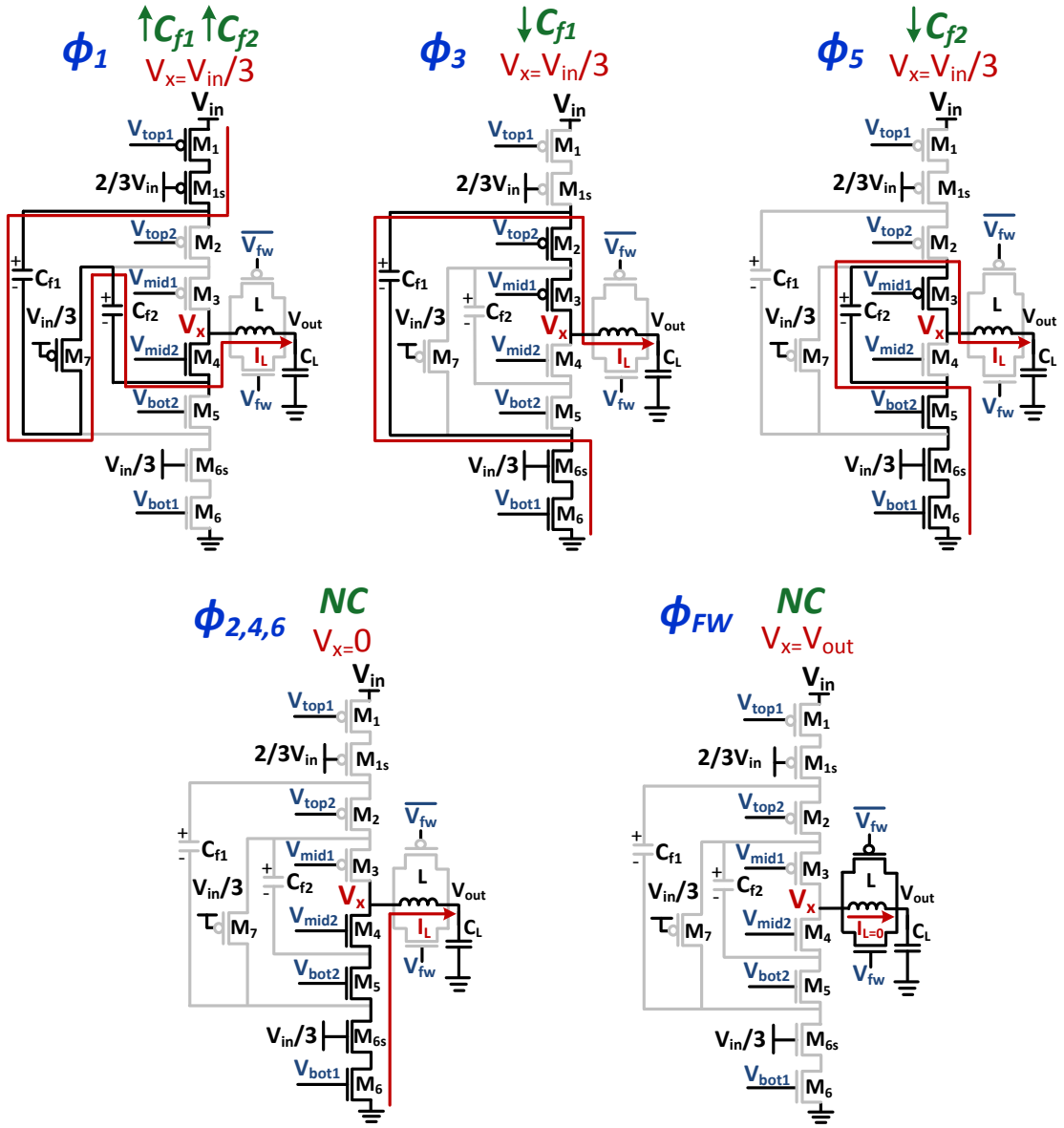


Figure 3.6: Proposed modified 4-level converter current path in different inductor current switching phases in operating mode 1: $0 < V_{out} < V_{in}/3$, and the equivalent flying capacitors state in each phase

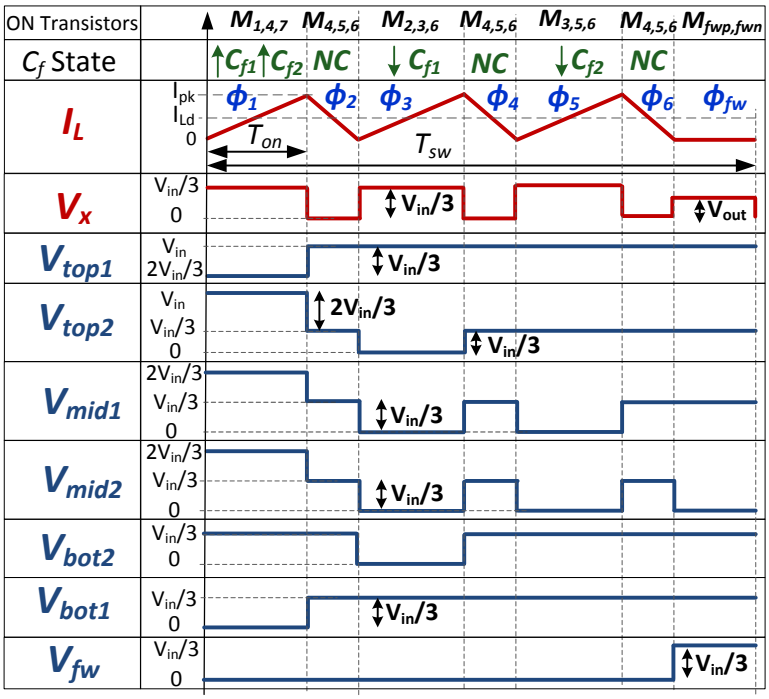


Figure 3.7: Power stage gate signal timing diagram of the proposed modified 4-level converter.

In steady state: $V_{f1} = V_{in}/3$, $V_{f2} = V_{in}/3$, and V_x equals 0 in $\phi_{2,4,6}$, $V_{in}/3$ in $\phi_{1,3,5}$, and V_{out} in ϕ_{FW}.

It should be noted that the proposed modified 4-level topology in Figure 3.3(c) is better suited relative to the 4-level in Figure 3.3(b) in fully-integrated applications where low-voltage on-chip passives are utilized. If off-chip passives are utilized, which tend to have higher voltage ratings, then the 4-level topology in 3.3(b) is superior due to fewer switches in the power stage and the lack of needing to limit the voltage swing on the off-chip capacitors.

3.3 Power Stage Losses Analysis

The efficiency of a DC-DC converter depends on the power losses, and can be computed via the following equation:

$$\eta = \frac{1}{1 + P_{loss}/P_{out}}. \tag{3.3}$$

The dominant power stage losses, P_{loss}, in an inductive converter are comprised of conduction losses, P_{cond}, and switching losses, P_{sw}, (i.e., $P_{loss} = P_{cond} + P_{sw}$). Conduction and switching losses can be represented by an effective resistance, R_{eff}, and an effective capacitance, C_{eff}, respectively [65].

For an inductive converter operating in DCM, the power stage conduction loss is given by:

$$P_{cond} = \left(\frac{2}{3} I_{pk} I_{Ld}\right) R_{eff}, \tag{3.4}$$

while the power stage switching loss is given by:

$$P_{sw} = C_{eff} F_{sw} V_{in}^2, \tag{3.5}$$

where C_{eff} is the total capacitance of the power stage topology referred to ground, and switching between 0 and V_{in} at switching frequency F_{sw}.

3.3.1 Effective Resistance Computation

The effective resistance of an inductive converter can be computed based on the power switch ON resistance, r_{sw}, the flying capacitors ESR, r_c, and the inductor ESR, r_L.

The flying capacitors charge balance can be maintained by keeping the the same capacitor charging and discharging time (i.e., constant inductor charging time, T_{on}), and the same RC time constant in each charging/discharging phase. Therefore, the pMOS and nMOS are sized such that, the pMOS ON resistance, r_{sw_p}, equals to the nMOS ON resistance, r_{sw_n}, (i.e., $r_{sw_p} = r_{sw_n} = r_{sw}$):

$$W_p = W_n \frac{r_{sw_{po}}}{r_{sw_{no}}}, \tag{3.6}$$

where W_p is the pMOS transistor width, W_n is the nMOS transistor width, $r_{sw_{po}}$ is the the pMOS transistor ON resistance per unit width, and $r_{sw_{no}}$ is the the pMOS transistor ON resistance per unit width. For the 1.5V-transistors in the employed technology, $r_{sw_{po}}/r_{sw_{no}} \approx 2$ (i.e., $W_p = 2W_n = 2W$).

The computed R_{eff} for the 3 different topologies operating in mode 1 ($0 < V_{out} < Vin/3$) is:

- 2-Level Buck: $R_{eff} = 3r_{swo}/W + r_L$
- 4-Level: $R_{eff} = 3r_{swo}/W + r_L + 4CR\, r_c$
- Modified 4-Level: $R_{eff} = 4r_{swo}/W + r_L + 4CR\, r_c$

where r_{swo} is the transistor ON resistance per unit width. Figure 3.8 shows the computed series resistance for the three different topologies.

3.3.2 Effective Capacitance Computation

There are many internal switching nodes in the stacked configuration of the power stage. The effective capacitance is computed based on Miller Coupling Factor (MCF) [66]. MCF is a multiplying factor that describes the coupling capacitance, C_c, between two switching nodes; V_1 and V_2 to find the equivalent capacitance to ground:

$$MCF = \frac{dV_1/dt - dV_2/dt}{dV_1/dt}. \tag{3.7}$$

The equivalent capacitance to ground normalized to V_{in}^2 can be expressed as following:

$$C_{gnd} = C_c \left(\frac{\Delta V_1}{V_{in}}\right)^2 MCF, \tag{3.8}$$

where C_c is specifically the gate-to-source capacitance, C_{gs}, and the gate-to-drain capacitance, C_{gd} of the MOSFET. Figure 3.8 (a), (b), and (c) show the computed capacitance referred to ground and the effective junction capacitance, C_j, at all nodes

for the three different topologies: 2-Level Buck, 4-Level, and the proposed modified 4-Level, respectively.

The total MOSFET effective parasitic capacitance for each topology can be computed by summing up the total capacitance n referred to ground and normalized to V_{in}^2 as follows:

$$C_{eff} = K_{4L} \sum_{i=1}^{n} C_c \left(\frac{\Delta V_{i,1}}{V_{in}} \right)^2 MCF_i, \tag{3.9}$$

where K_{4L} is the multilevel converter improvement factor. To find the total effective capacitance at the same switching frequency for the three topologies, the total power stage capacitance is multiplied by K_{4L}, where $K_{4L} = F_{sw-4L}/F_{sw-2L}$ (i.e., $K_{4L} = 1$ for the 2-level buck converter, and $K_{4L} = (1 - CR)/(1/3 - CR)$ for the 4-level converter, operating in mode 1).

Since $W_p = 2W_n = 2W$, then $C_{gp} = 2C_{gn}$ and $C_{jp} = 2C_{jn}$, where C_{jp} and C_{jn} are the junction capacitance of the pMOS and nMOS, respectively, and C_{gp} and C_{gn} are the total gate capacitance of the pMOS and nMOS, respectively. Note that $C_g = C_{gs} + C_{gd}$, and $C_{gs} \approx C_{gd}$.

The computed C_{eff} for the three different topologies can be expressed as following:

- 2-Level Buck:

  $C_{eff} \approx 2.7WC_{gno} + 6.3WC_{jno} + C_x$

- 4-Level:

  $C_{eff} \approx K_{4L}(1.5WC_{gno} + 3WC_{jno} + C_x/3 + 1.3C_{par})$

- Modified 4-Level:

  $C_{eff} \approx K_{4L}(3.7WC_{gno} + 6WC_{jno} + C_x/3 + 1.1C_{par})$,

where C_{gno} and C_{jno} are capacitance per unit width, C_{par} is the parasitic capacitance of the flying capacitors, and C_x is the parasitic capacitance at V_x node.

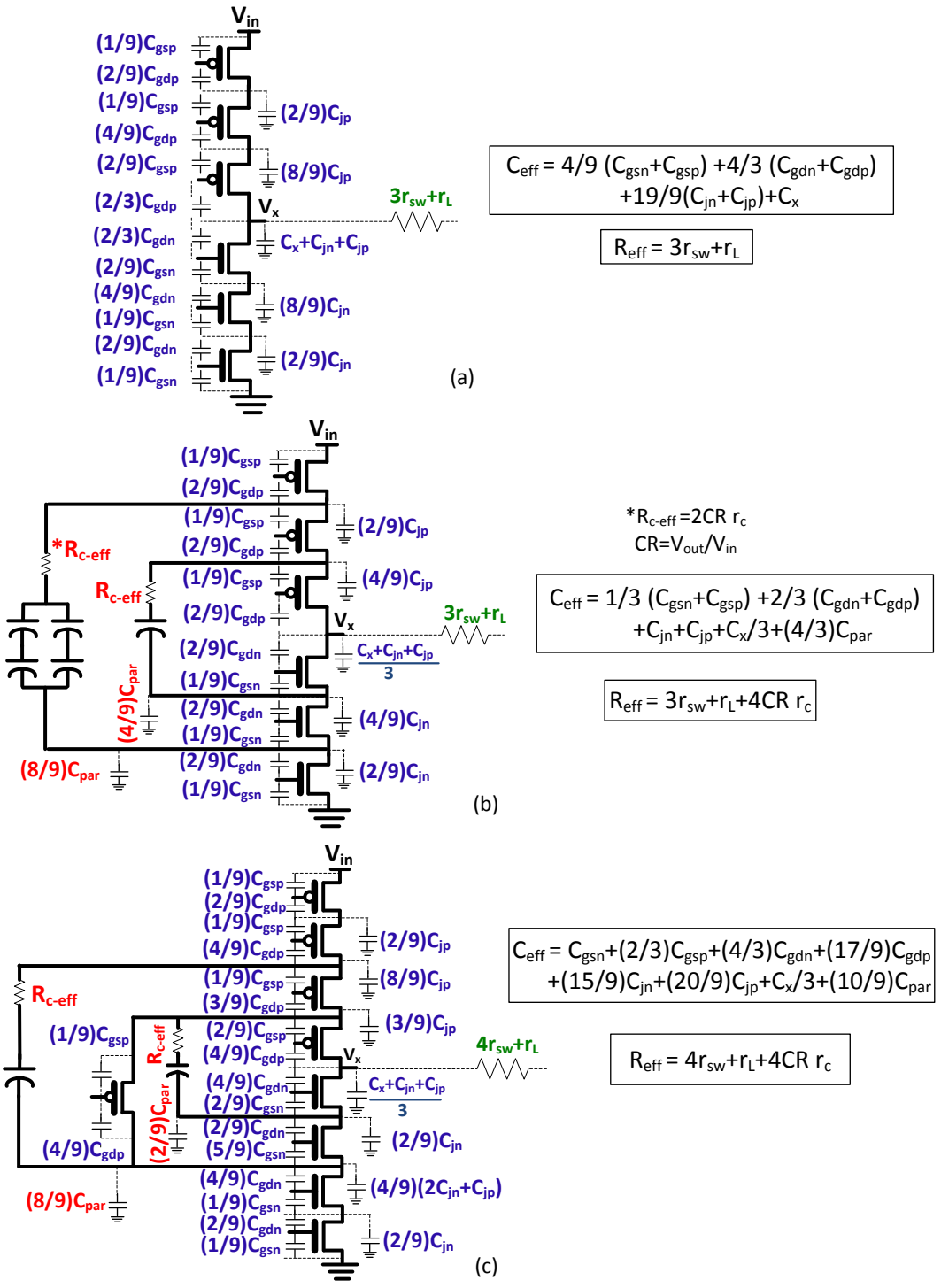


Figure 3.8: Power stage parasitic model including the equivalent effective resistance and effective capacitance computed based on voltage switching on each node and normalized to V_{in}^2: (a) Two-Level Buck, (b) Four-Level converter,(c) Modified four-Level converter.

Table 3.1: Effective resistance and capacitance for different topologies.

	2-Level Buck	4-Level	Modified 4-Level
R_{eff}	$3r_{sw} + r_L$	$3r_{sw} + r_L + 4CR\ r_c$	$4r_{sw} + r_L + 4CR\ r_c$
C_{eff}	$2.7C_{gn} + 6.3C_{jn} + C_x$	$K_{4L}(1.5C_{gn} + 3C_{jn} + C_x/3 + 1.3C_{par})$	$K_{4L}(3.7C_{gn} + 6C_{jn} + C_x/3 + 1.1C_{par})$

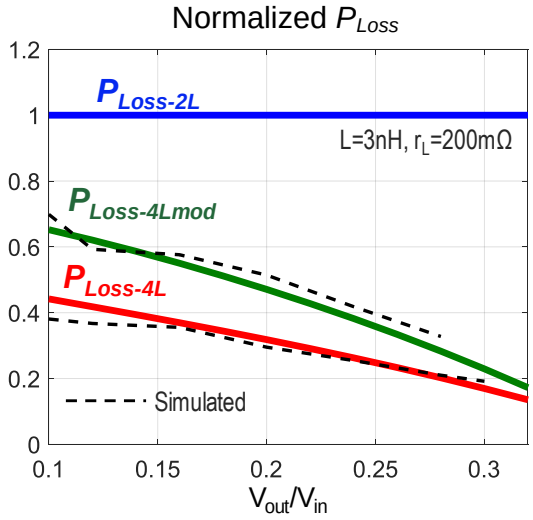


Figure 3.9: Normalized losses for the 2-level buck, $P_{Loss-2L}$, the 4-level, $P_{Loss-4L}$, and the modified 4-level, $P_{Loss-4Lmod}$, using the same passive values ($L = 3nH, r_L = 200m\Omega$).

3.3.3 Losses Comparison

The losses of the three different topologies: 2-Level Buck, 4-Level, and the proposed modified 4-Level are compared using the following equation:

$$\begin{aligned} P_{loss} &= \frac{2}{3} I_{pk} I_{Ld} R_{eff} + C_{eff} F_{sw-2L} V_{in}^2 \\ &= \frac{2}{3} I_{pk} I_{Ld} R_{eff} + 2V_{in}^3 C_{eff} I_{Ld} \frac{CR(1-CR)}{L I_{pk}^2} \end{aligned} \tag{3.10}$$

Table 3.1 summarizes R_{eff} and C_{eff} of the three different topologies for $0 < CR < 1/3$. The power stage transistors width, W_p and W_n, are optimized for each topology for minimum losses (i.e., $\partial P_{loss}/\partial W = 0$).

Figure 3.9 shows the power stage losses for the 2-level buck, $P_{Loss-2L}$, the 4-

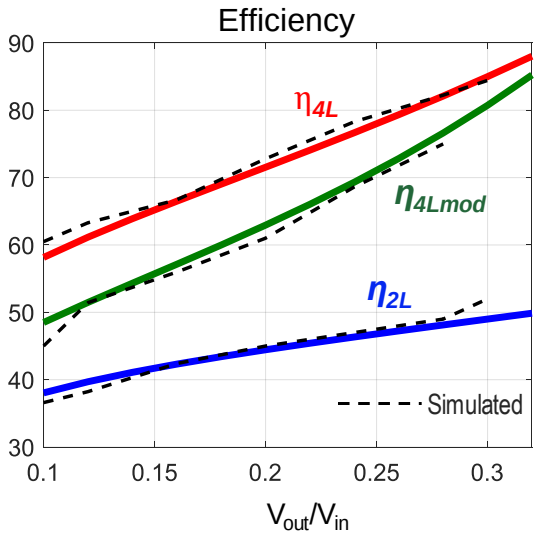


Figure 3.10: Efficiency of the 2-level buck, η_{2L}, the 4-level, η_{4L}, and the modified 4-level, η_{4Lmod}, using the same passive values ($L = 3nH, r_L = 200m\Omega$).

level, $P_{Loss-4L}$, and the modified 4-level, $P_{Loss-4Lmod}$, normalized to $P_{Loss-2L}$. The normalized power stage losses in Figure 3.9 are compared using the same passive values. The benefit of the 4-Level converter compared to the 2-level buck in reducing the power stage losses is clear. It can be noticed that for the same passive values, $P_{Loss-4L}$ is lower than $P_{Loss-4Lmod}$, as was expected in Section 3.2. However, as mentioned in Section 3.2, the implementation area of C_{f1} in the 4-level is $4\times$ the implementation area of C_{f1} in the modified 4-level. More specifically, for an inductor value of $3nH$, the implementation area for the 4-level converter would be around $3.2mm^2$, while it would be only $1.5mm^2$ for the modified 4-level converter. Figure 3.10 shows the equivalent efficiency for the 2-level buck, η_{2L}, the 4-level, η_{4L}, and the modified 4-level, η_{4Lmod}, using the same passive values. The modeled results match transistor-level simulations to within 2%.

For the same on-die implementation area, it is expected that the modified 4-level topology should outperform the 4-level topology due to better capacitor area utilization. As shown in Figure 3.11, $P_{Loss-4Lmod}$ is indeed lower than $P_{Loss-4L}$ because the modified 4-level converter allows larger passives than the conventional 4-level converter. It can be noticed that for the same implementation area, $P_{Loss-2L}$ is lower than $P_{Loss-4L}$

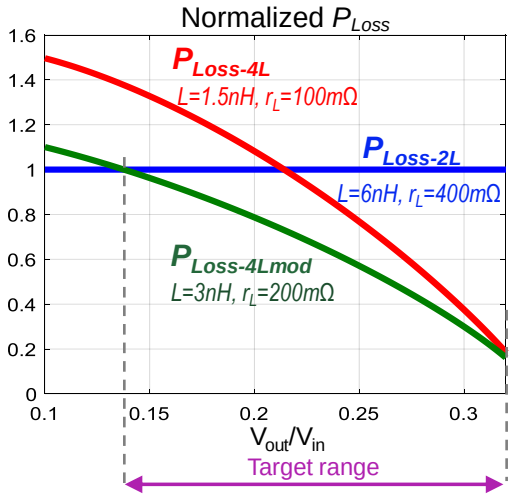


Figure 3.11: Normalized losses for the 2-level buck, $P_{Loss-2L}$, the 4-level, $P_{Loss-4L}$, and the modified 4-level, $P_{Loss-4Lmod}$, using the same on-chip implementation area.

and $P_{Loss-4Lmod}$ at low V_{out}/V_{in}. Thus, it may be advantageous to design a reconfigurable converter that can switch between 2-level buck mode and 4-Level mode to achieve high efficiency across a wide voltage range. However, For the target conversion ratio in this work, the modified 4-Level converter has the lowest power stage losses among the three topologies, and is therefore selected for implementation.

3.4 Modified 4-Level Converter Circuit Details

Previously reported buck and hybrid converters [46, 48, 55], operating in continuous conduction mode (CCM) support high output power but with a limited minimum load current and poor low load efficiency. In order to achieve high efficiency over low output current ranges appropriate for IoT applications, the proposed converter is designed to operate in DCM, and regulates the output voltage with constant ON-time pulse-frequency modulation (PFM). DCM converters exhibit a single-pole system behavior, making the control inherently stable, eliminating the need for complex analog compensation loop design. Figure 3.12 shows the top-level architecture of the proposed DCM-operated converter. Since a zero current detector was not implemented in the cur-

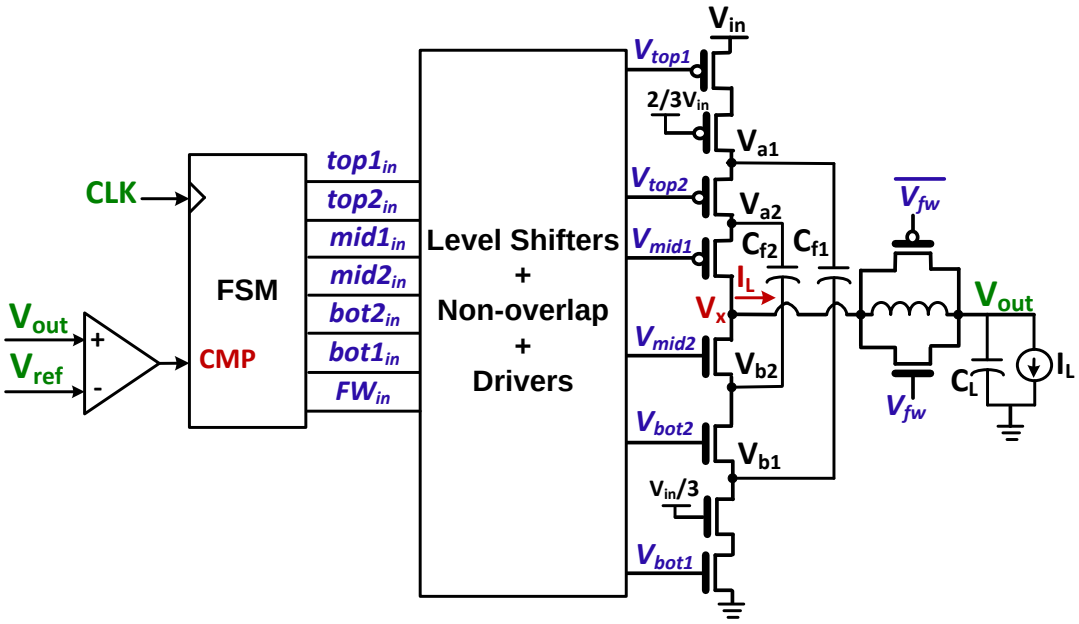


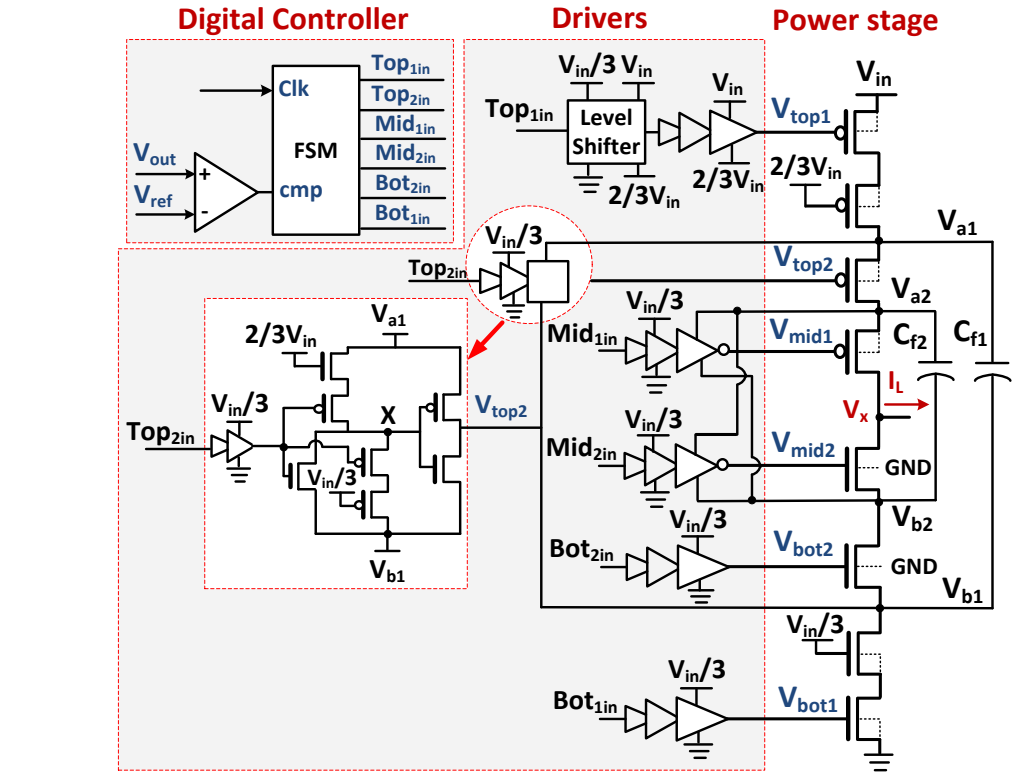
Figure 3.12: DCM-operated top-level architecture.

rent prototype, an external clock with appropriate duration of off-time pulses has been used for testing purposes.

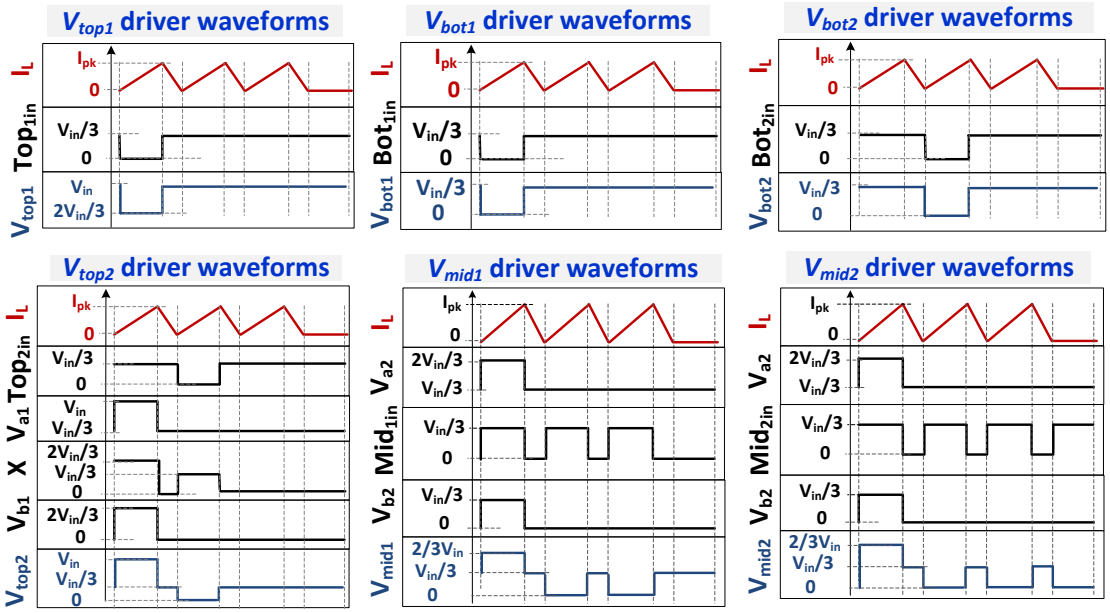
3.4.1 Proposed Driver Circuits

To implement the modified 4-level converter, it is required to drive the power stage with 3-level gate signals (shown in Figure 3.7) to ensure that no transistor exceeds the maximum rating of 1.5V (i.e., $V_{in}/3$). Figure 3.13(a) and (b) show the detailed schematic of the proposed drivers and their corresponding waveforms, respectively. Signals V_{bot1}, and V_{bot2} switches between GND and $V_{in}/3$, and can thus use a conventional 2-transistor inverter-based CMOS driver. On the other hand, signals V_{Mid1}, and V_{Mid2} are 3-level gate signals which must switch between GND, $V_{in}/3$, and $2V_{in}/3$. Similarly, signal V_{Top2} must switch between GND, $V_{in}/3$, and V_{in}.

Rather than creating new, dedicated power rails for the sole purpose of driving the power transistors, the proposed drivers exploit the existing switching terminals of the flying capacitors as dynamic power/ground rails. This eliminates the need for com-



(a)



(b)

Figure 3.13: (a) Detailed schematic of the power Stage drivers architecture. (b) Equivalent signal timing diagram.

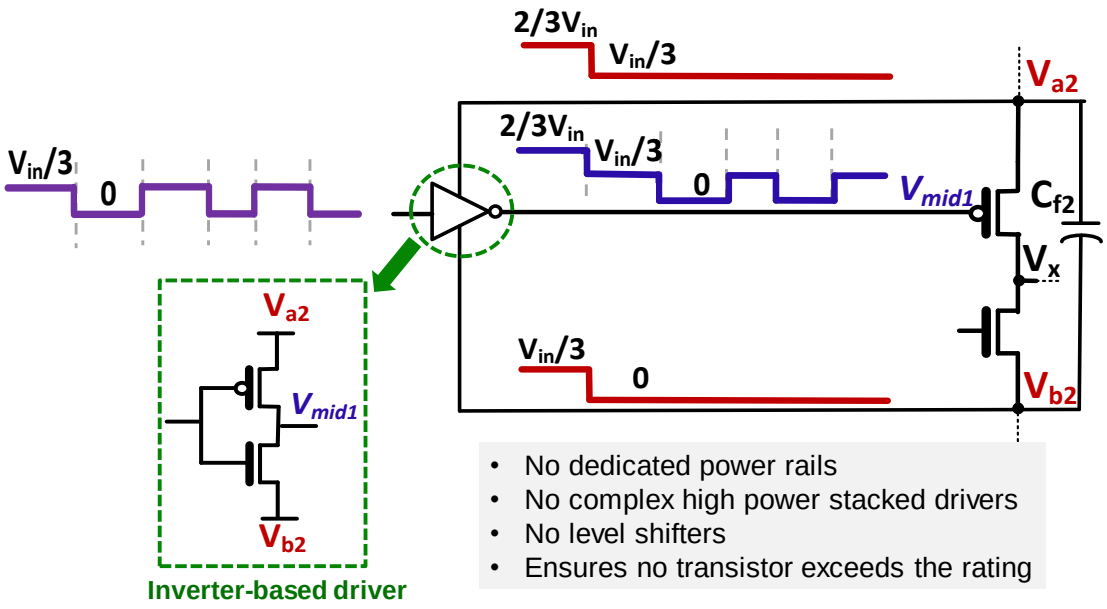


Figure 3.14: The proposed 3-Level gate signal driver with its power and ground rail connected to the positive and negative terminals of the flying capacitor, respectively.

plex power-hungry stacked drivers with dedicated power rails, while simultaneously eliminating the need for many level-shifters. Specifically, the positive terminal of C_{f2} (V_{a2}) and the negative terminal of C_{f2} (V_{b2}) are used as power and ground of the two middle switches drivers, respectively. While the positive terminal of C_{f1} (V_{a1}) and the negative terminal of C_{f1} (V_{b1}) are used as power and ground of the V_{Top2} driver, respectively. Since the voltage across the flying capacitors equals $V_{in}/3$, stacked drivers are not required, but rather conventional 2-transistor inverter-based CMOS drivers can be utilized. Figure 3.14 shows the 3-level gate signal generation using conventional 2-transistor inverter-based CMOS driver. The driver generating V_{Top2} uses mixed stacked transistors in the first stage to do level shifting in ϕ_1 only using the flying capacitor terminals voltage. On the other hand, the top switch gate signal, V_{Top1}, switches between $2V_{in}/3$ and V_{in} and thus requires a level shifter to shift up the input signal switching between GND and $V_{in}/3$ to a signal switching between $2V_{in}/3$ and V_{in}.

Timing between power stage gate signals is critical for reliability. Non-overlap circuits are added to ensure none of the transistors are overstressed during transitions.

For example, a non-overlap circuit is added between Top_{1in} and Bot_{1in} to avoid shorting C_{f1} between V_{in} and GND during transitions. Also, a non-overlap circuit is added between Top_{2in} and Bot_{2in} to avoid shorting C_{f1} to C_{f2} during transitions.

When switching from ϕ_1 to ϕ_2, if Mid_{1in}/Mid_{2in} signal switches from $V_{in}/3$ to GND before V_{a2} and V_{b2} switch from $2V_{in}/3$ and $V_{in}/3$ to $V_{in}/3$ to GND, V_{Mid1}/V_{Mid2} transistors will be overstressed. To ensure that this does not occur, a non-overlap circuit is added to delay the negative edge of Mid_{1in} and Mid_{2in} signals with respect to the rising edge of Top_{1in}/Bot_{1in}. This ensures that Mid_{1in}/Mid_{2in} will not switch to GND while V_{a2} still equals $2V_{in}/3$.

3.4.2 Proposed Level Shifter in FDSOI

The top switch gate signal V_{Top1} does require a level shifter to convert the FSM output signal switching between GND and $V_{in}/3$ up to signal switching between $2V_{in}/3$ and V_{in}. Figure 3.15 shows the proposed level shifter. The proposed topology is all digital and ensures that no transistor exceeds the maximum voltage of $V_{in}/3$. FDSOI body biasing is used to improve performance by reducing the threshold voltage when turned ON and reducing leakage when turned OFF. The low input voltage is shifted-up by the positive feedback action of the cross-coupled transistors. Connecting the body of the cross-coupled transistors to their drains instead of their sources reduces the strength of the pMOS latch [67], and hence enables fast transitions and reduces the level shifter delay. Connecting the body of the top MOSFETS transistors to a high voltage reduces the leakage power consumption. Simulations show that the delay of the proposed topology is only 230ps with total power of 1.27nW at a switching frequency of 1kHz.

3.4.3 FSM Operation

The output is regulated using constant ON-time pulse-frequency modulation (PFM). The controller operation is illustrated in the inductor timing diagram in Fig-

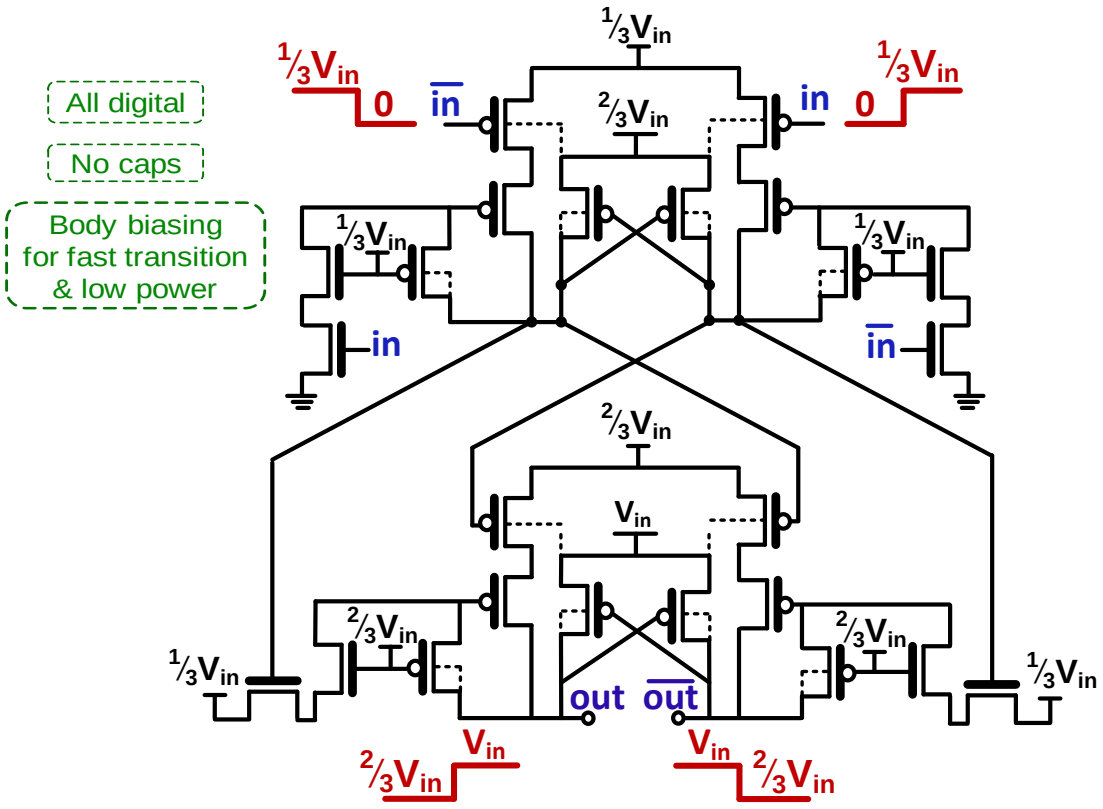


Figure 3.15: Proposed top switch level-shifter topology using body biasing in FDSOI ($in = 0 : V_{in}/3 \rightarrow out = 2V_{in}/3 : V_{in}$).

ure 3.16. The finite state machine (FSM) checks the comparator output every six inductor switching phases. At the end of ϕ_6, if the load did not receive sufficient energy (i.e., V_{out} is below the reference voltage, V_{ref}), the comparator output is low, and the FSM triggers new six inductor switching phases. But if the load has sufficient energy ($V_{out} > V_{ref}$), the comparator output is high, and the converter goes to the freewheel phase ϕ_{FW}. During the freewheel phase, if V_{out} goes below V_{ref}, the comparator output goes low and the FSM triggers new six inductor switching phases.

The FSM checks the comparator output and acts only at the end of ϕ_6 for two reasons. First, to not interrupt the charge balance of the flying capacitors. Second, if the the FSM checks the comparator's output at end of ϕ_2, ϕ_4, and ϕ_6, and accordingly switches to ϕ_{FW} in between, this will result in an effective switching frequency increase of $3\times$, resulting in more losses.

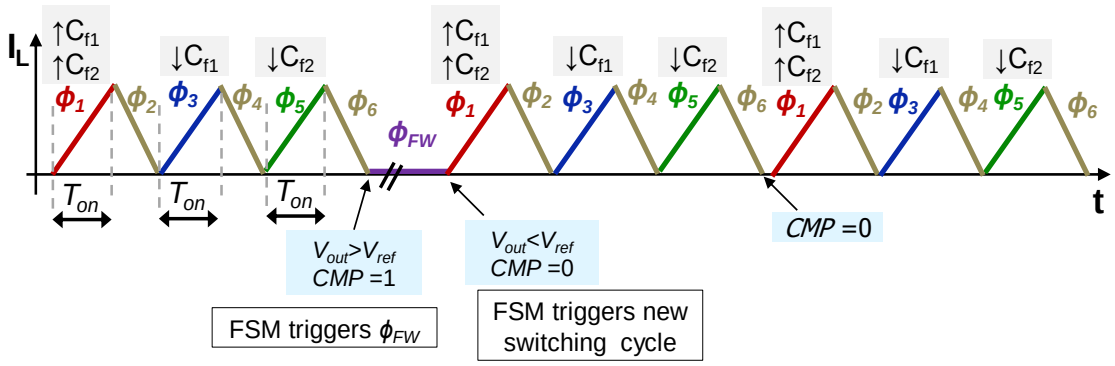


Figure 3.16: Inductor current timing diagram, representing FSM operation under different load conditions.

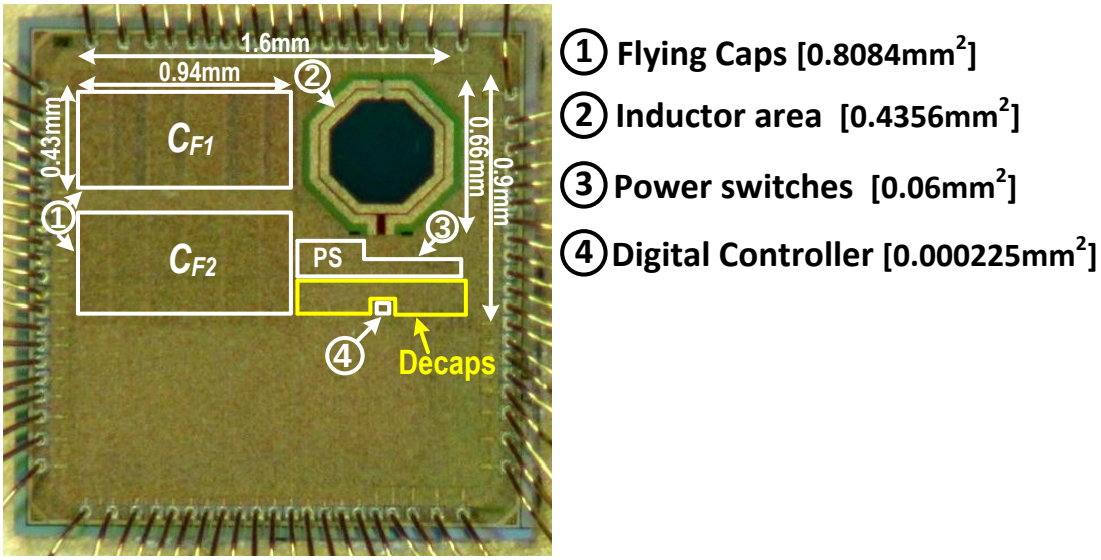


Figure 3.17: Micrograph of the fabricated MISIMO die in 28nm FDSOI.

3.5 Experimental Results

The proposed hybrid 4-level converter is implemented in 28nm FDSOI and occupies a total area of $1.5mm^2$. A die micrograph is shown in Figure 3.17. The inductor is implemented in $0.4356mm^2$ using the top metal layer, and the flying capacitors are implemented using high density MIM capacitors. Decoupling capacitors are implemented by stacking MOS, MOM and MIM capacitors vertically. The chip is directly wire-bonded to a PCB using chip-on-board packaging technology. The wirebonded

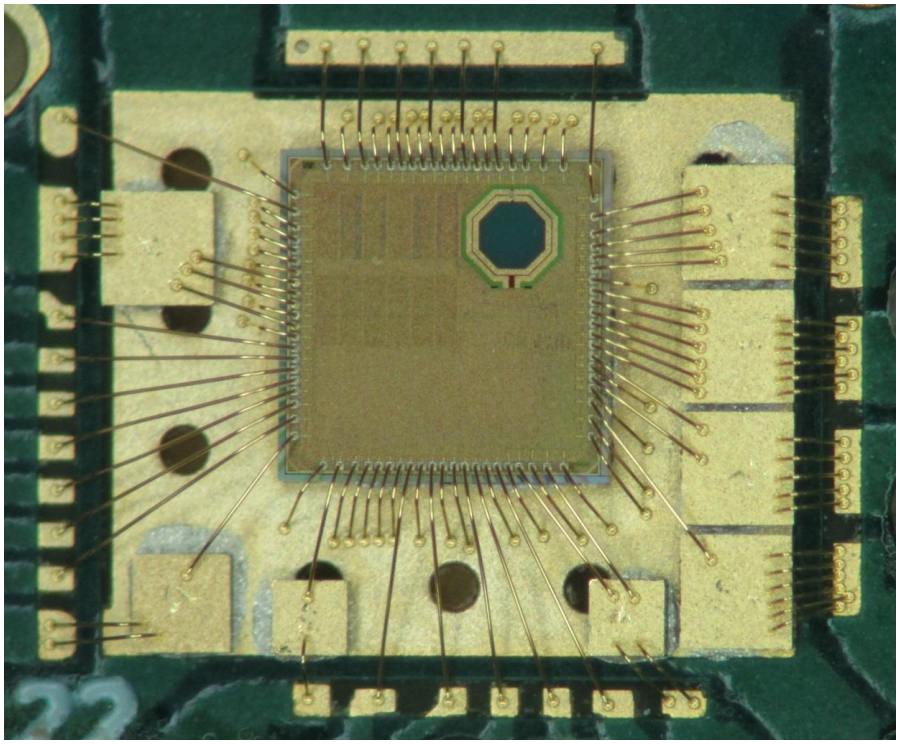


Figure 3.18: Micrograph of the wirebonded chip on board.

chip-on-board used for testing is shown in Figure 3.18. There are many IO pads used for testing, in real implementation, the area would be much smaller.

The fabricated converter supports an input voltage range of 2.8−4.2V while regulating an output power rail with a voltage range of 0.6−1.2V, and an output power of 10μW−40mW. The proposed converter is PFM controlled with a maximum output switching frequency of 200MHz, though due to the 4-level operation, the power switches maximum switching frequency is only 67MHz.

Measured efficiency versus output power curves for various output voltages are shown in Figure 3.19. Measurements reveal a peak efficiency of 78% at V_{in}=3.6V and V_{out}=1V. All measurements include the power of the $V_{in}/3$ and $2V_{in}/3$ rails, which in this prototype are provided externally. It should be noted that similar rails would be needed anyways in a conventional 2-level buck to drive the stacked transistors. Compared to an ideal LDO (shown in dotted lines in Figure 3.19), the proposed modified 4-level converter shows improved efficiency of 39%−50.5% over $(1/CR) = 3 - 7$,

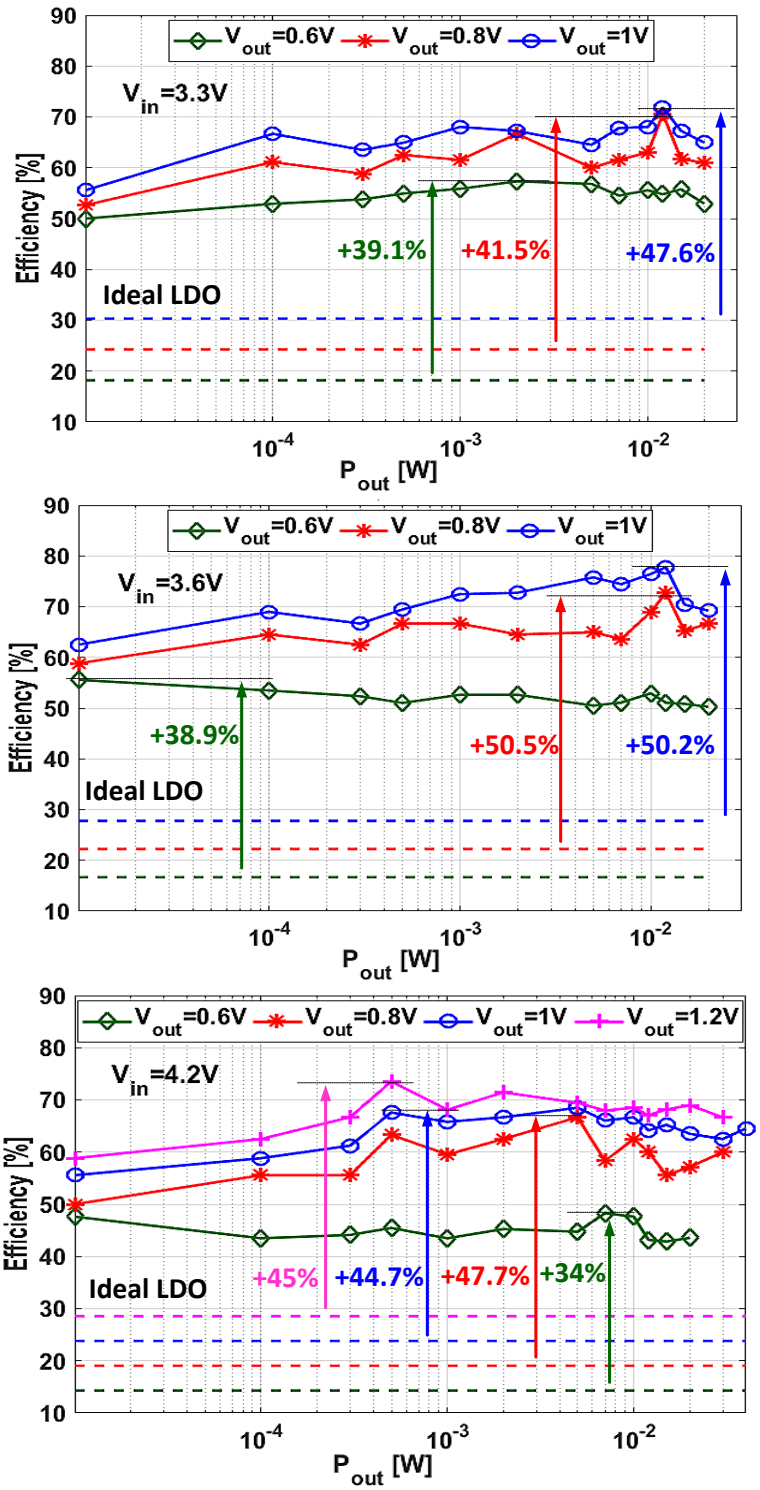


Figure 3.19: Measured Efficiency versus output power for different V_{out} and V_{in}, alongside a comparison with an ideal LDO.

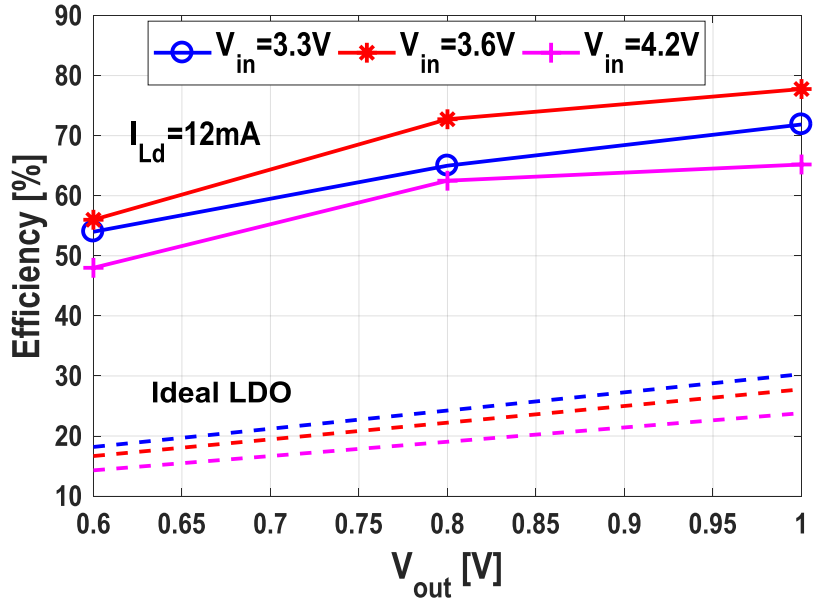


Figure 3.20: Measured efficiency versus output voltage for different V_{in} at $I_{Load} = 12mA$.

which exceeds prior-art Li-ion-compatible converters integrated in scaled CMOS, as shown in Table 3.2.

Figure 3.20 shows the measured efficiency versus output voltage for different V_{in} at I_{Load} =12mA. It is expected from (3.10) that the power losses reduce as V_{in} decreases, and hence, efficiency increases (i.e., efficiency at V_{in}=3.6V is higher than efficiency at V_{in}=4.2V in Figure 3.20). However, in the proposed design, the power switches over-drive voltage, V_{ov}, equals to $V_{in}/3$, thus, as V_{in} decreases, V_{ov} decreases and the switches ON resistance increases, thereby increasing the conduction losses. This explains why the efficiency at V_{in}=3.3V degrades compared to efficiency at V_{in}=3.6V.

To test the transient behavior of the circuit, a load step is applied by turning ON an external MOSFET switch in series with a test load resistor. Figure 3.21 shows that a 10μA to 1mA load step has negligible droop, and the output regulated voltage has only 12mV ripple with a decoupling capacitor 50nF.

Table 3.2 shows a comparison to other Li-ion-compatible fully-integrated. To the best of the author's knowledge, no fabricated prior-art fully-integrated converter

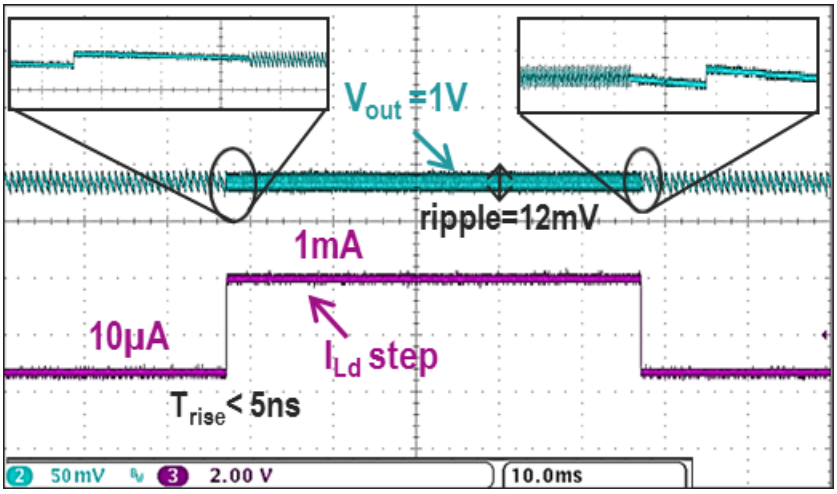


Figure 3.21: Measured load step response at Vin=3.6V with negligible droop and 12mV ripple.

supported Li-ion in scaled CMOS ($\leq 28nm$) with fine-grain output voltage control for DVS applications. Thanks in part to DCM-enabled PFM control, the converter achieves a dynamic load range of 4,000× (10μW-40mW), which exceeds prior-art by ≥8.9×. While the SC converters presented in [56,57,59] achieve higher power density than this work, they are implemented in non-scaled technology (i.e 90nm, 65nm, 130nm), with limited conversion ratios ($1/CR = 2.8$ in [56], $1/CR = 3-4$ in [57], $1/CR = 3-3.7$ in [59]).

3.6 Discussion

3.6.1 Power Density Limits in DCM

Despite the fact that DCM is favorable mode for low power applications as discussed in Section 3.4, DCM-operation limits the maximum output power of the converter (and thus the power density), which is determined by the inductor peak current. In DCM operation, the inductor peak current must be at least double the load current (i.e., $I_{pk} \geq 2I_{Ld}$). Therefore, the current capability of the converter, operating in DCM is determined by its maximum I_{pk}. Designing a converter to operate in DCM with a large I_{pk} can increase the converter current capability and reduce the converter switch-

Table 3.2: Comparison with Prior Li-ion Compatible Fully-Integrated DC-DC Converters.

	Breussegem, JSSC'11	**Le, ISSCC'13**	**Bang, JSSC'16**	**Nguyen, TPEL'18**	**Kim, JSSC'12**	**This Work**
Technology	90nm	65nm	180nm	130nm	130nm	**28nm FDSOI**
Topology	SC	SC	SC	SC	Buck 3-Level	Buck 4-Level
Li-ion Capability	YES	YES	YES	YES	NO	**YES**
L (H) No of phases	NA	NA	NA	NA	4n 4 phases	3n 1 phase
Capacitor	MIM	MOS	MIM	MIM+MOS	MOS	MIM
CR	1/2	1/3, 2/5	117 CRs	1/3	NA	NA
V_{in} (V)	3-3.9	3-4	3.4-4.3	3.2-4	2.4	**2.8 - 4.2**
V_{out} (V)	1.3@Vin=3 1.42@Vin=3.3 1.5@Vin=3.6	1	0.45-1.5	1.07	0.4-1.4	0.6-1.2
F_{max} (MHz)	70	300	2.7	100	200	200
P_{out} (mW)	1*-150	6*-162	0.001*-0.45	4*-45	120*-1000	0.01-40
Dynamic Range (P_{max}/P_{min})	150	19	450	11.25	8.3	**4,000**
Area (mm^2)	3.6*	0.64	1.69	0.39	5	1.5
Power density (mW/mm^2)	41.7	190	0.27	115	200	26.7
Overall peak efficiency @1/CR	77.3%@2.3	74.3%@3.6	72%@2.6	80%@3.45	77%@2.2*	**78%@3.6**
Maximum improvement over LDO@ (1/CR) $_{range}$	33.9%* @2.3	35-45%* @3-4	21%-49.5%* @3-7	28%-49* @3-3.7	18-31%* @2-4	**34-50.5% @3-7**

*Estimated from plotted data

ing frequency as well, and hence, improve efficiency. However, in hybrid topologies, I_{pk} is limited by the inductor value, the inductor series resistance, the maximum inductor charging time (T_{on}), and the resistance of the employed switches. The inductor on-time T_{on} must be less than the inductor resonance time, T_r, where T_r is defined as:

$$T_r = 2\pi\sqrt{LC_{tot}}, \tag{3.11}$$

where C_{tot}= C_{f1}//C_{f2}//C_L. Hence, as the converter passives increase, T_{on} and I_{pk} can be increased, and thus, the converter current capability and efficiency will increase accordingly. However, there are area limitations for fully integrated converters, so for a converter to achieve maximum power (i.e power density) using the same passives value, the converter can be switched to operate in continuous conduction mode (CCM) at high load current. It can be shown that the 4-level and modified 4-level converters can be operated in CCM mode to support higher power densities, though further details will be subject to future research dissemination.

3.6.2 Flying Capacitors Choice

The flying capacitors voltage ripple, ΔV_c, is proportional to the charge/discharge time (i.e., T_{on}), and inversely proportional to the amount of flying capacitor, C_f. In SC converters, hard switching losses, which occur in the slow switching limit (SSL) region [68], are proportional to ΔV_c (i.e., $P_{ssl} \propto \frac{1}{F_{sw}C_f}$). Therefore, large flying capacitors are required to reduce the hard switching losses and improve efficiency. While in hybrid converters, C_f is soft charged/discharged through the inductor, thus small flying capacitance can, with a caveat discussed below, be used without sacrificing efficiency. However, the voltage ripple on C_f can over-stress the power switches so C_{f1} and C_{f2} values are selected such that the voltage across the power switches doesn't exceed their voltage rating. The maximum voltage across the power stage transistors, V_{max}, equals to $V_{in}/3 + \Delta V_c$. For $V_{in} \leq 4.2$, $V_{max} \leq 1.4 + \Delta V_c$. Therefore, for 1.5V-transistors,

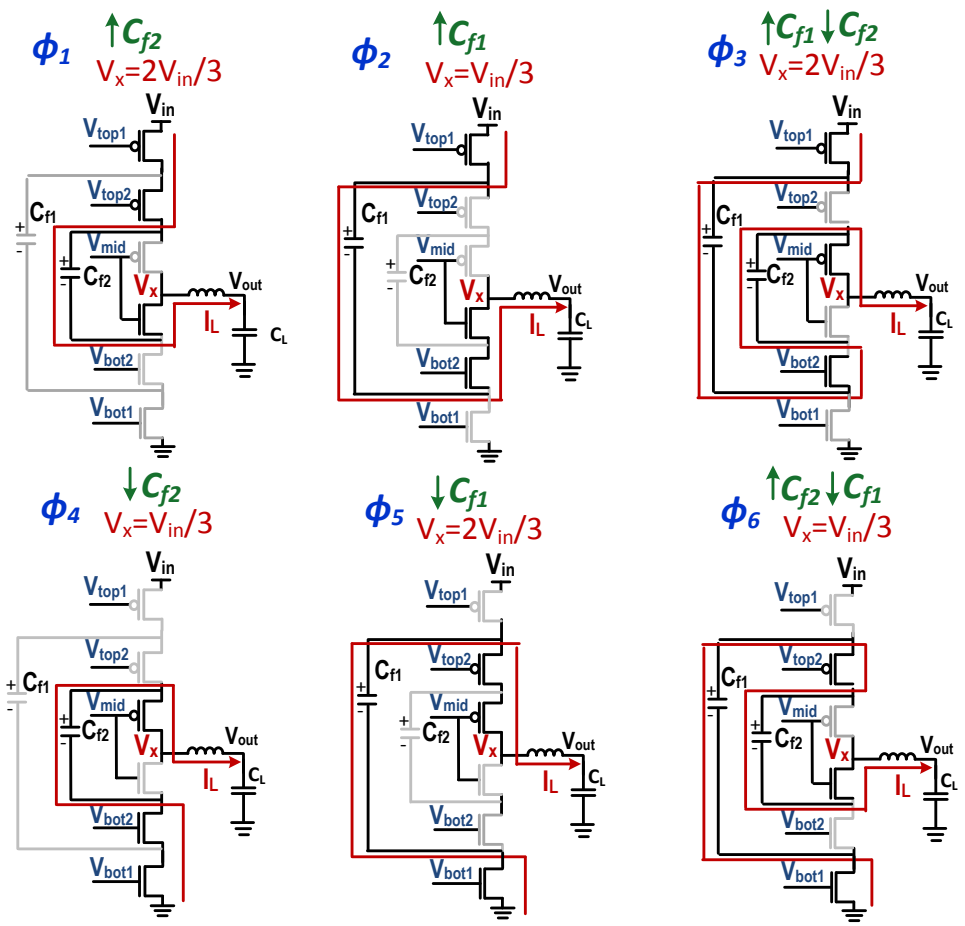
the maximum allowed flying capacitor ripple, ΔV_{max}, is $100mV$ (i.e., $\Delta V_c \leq 100mV$). The value of the designed flying capacitor can then be computed using the following formula:

$$C_f \geq \frac{LI_{pk}^2}{2V_{in}(1/3 - CR)\Delta V_{max}} \tag{3.12}$$

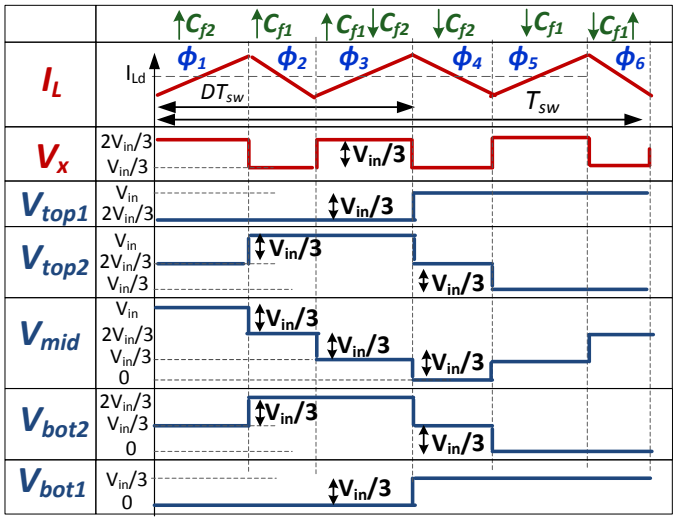
3.6.3 Multi-Mode Operation

If the 4-level converter was to be implemented to operate over an output voltage range: $0 < V_{out} < V_{in}$, operating mode 2 ($V_{in}/3 < V_{out} < 2V_{in}/3$) and mode 3 ($2V_{in}/3 < V_{out} < V_{in}$) would have to be enabled. In the 4-level converter (Figure 3.3 (b)), mode 2 and mode 3 can be enabled by changing the power stage gate signals in each mode, hence, enabling the appropriate inductor switching phases in each mode without any change in the power stage topology. Figure 3.22 (a) shows the 4-level converter switching phases and inductor current paths in mode 2 and Figure 3.22 (b) shows the equivalent gate signaling timing diagram. While Figure 3.23 (a) and Figure 3.23 (b) show the current path in different switching phases and the equivalent gate signaling timing diagram, respectively for the converter operating in mode 3.

In the modified 4-level converter (Figure 3.3 (c)), mode 2 and mode 3 can only be enabled by adding stacked switches to the power stage as shown in Figure 3.24. The additional power switches are required to enable a new capacitors switching state and reduce the voltage stress on the power stage transistors. Figure 3.25 shows the modified 4-level converter switching phases and inductor current paths in mode 2 and Figure 3.26 shows the equivalent gate signaling timing diagram. While Figure 3.27 (a) and Figure 3.27 (b) show the current path in different switching phases and the equivalent gate signaling timing diagram, respectively for the converter operating in mode 3.



(a)



(b)

Figure 3.22: (a) Four-level converter current path in different inductor switching phases, operating on mode 2: $V_{in}/3 < V_{out} < V_{in}/3$. (b) Equivalent Power stage gate signal timing diagram.

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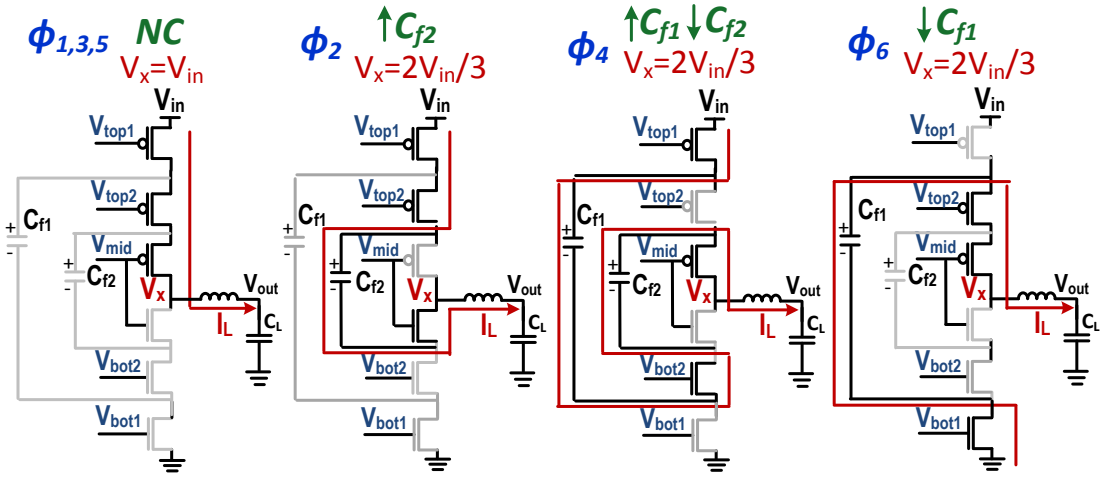
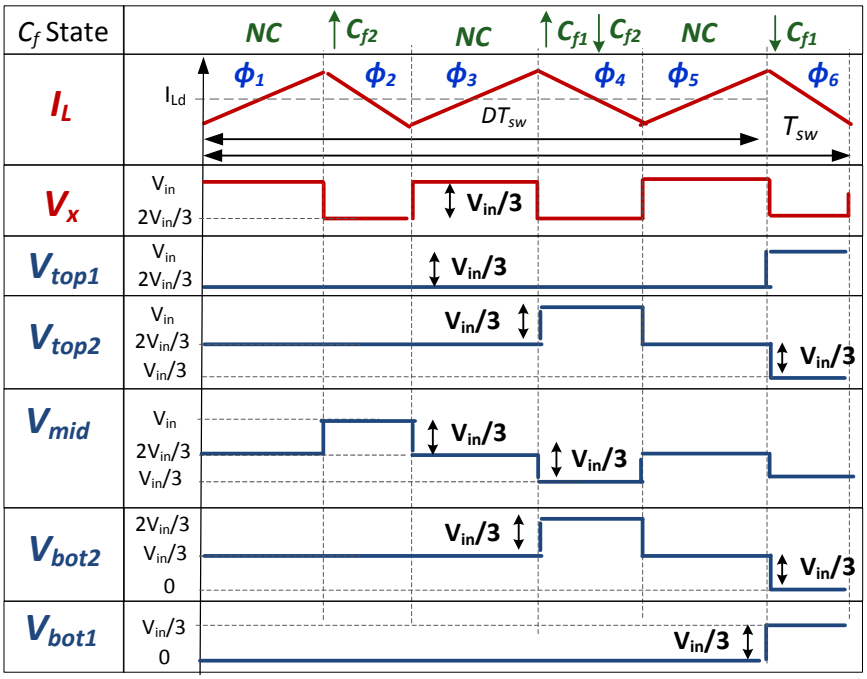


(a)



(b)

Figure 3.23: (a) Four-level converter current path in different inductor switching phases, operating in mode 3: $2V_{in}/3 < V_{out} < V_{in}$. (b) Equivalent Power stage gate signal timing diagram.

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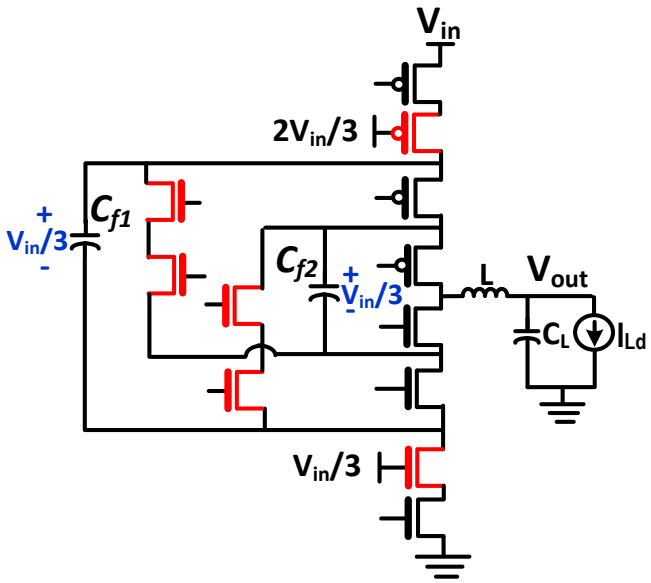

Figure 3.24: Modified four-level converter power stage, operating in the three modes of operation (mode 1: $0 < V_{out} < V_{in}/3$; mode 2: $V_{in}/3 < V_{out} < 2V_{in}/3$; mode 3: $2V_{in}/3 < V_{out} < V_{in}$)

.

3.7 Conclusion

This chapter demonstrated the feasibility of implementing a fully-integrated DC-DC converter compatible with Li-ion battery voltage (2.8-4.2V), in scaled CMOS (28nm), using only the available low-voltage transistors (1.5V) and on-chip passives. A modified 4-level converter, operating in DCM was implemented to achieve high efficiency over load range of 4,000$\times$ (10μW-40mW) appropriate for IoT applications. The proposed architecture utilizes the switching terminals of the flying capacitors as dynamic power/GND rails for the power stage drivers to eliminate the need for complex power-hungry stacked drivers with dedicated power rails and level shifters.

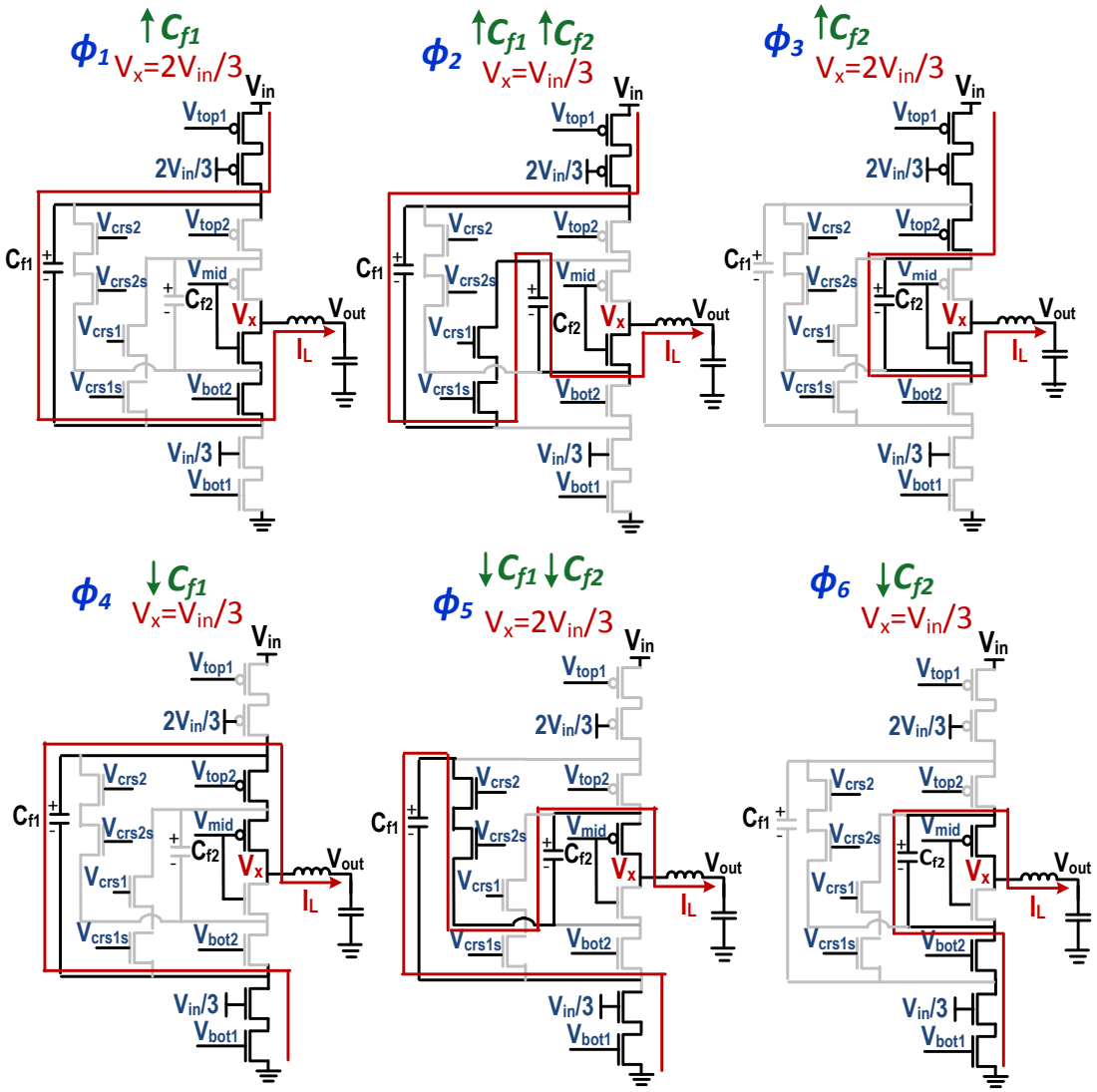

Figure 3.25: Modified four-level converter current path in different inductor switching phases, operating on mode 2: $V_{in}/3 < V_{out} < V_{in}/3$.

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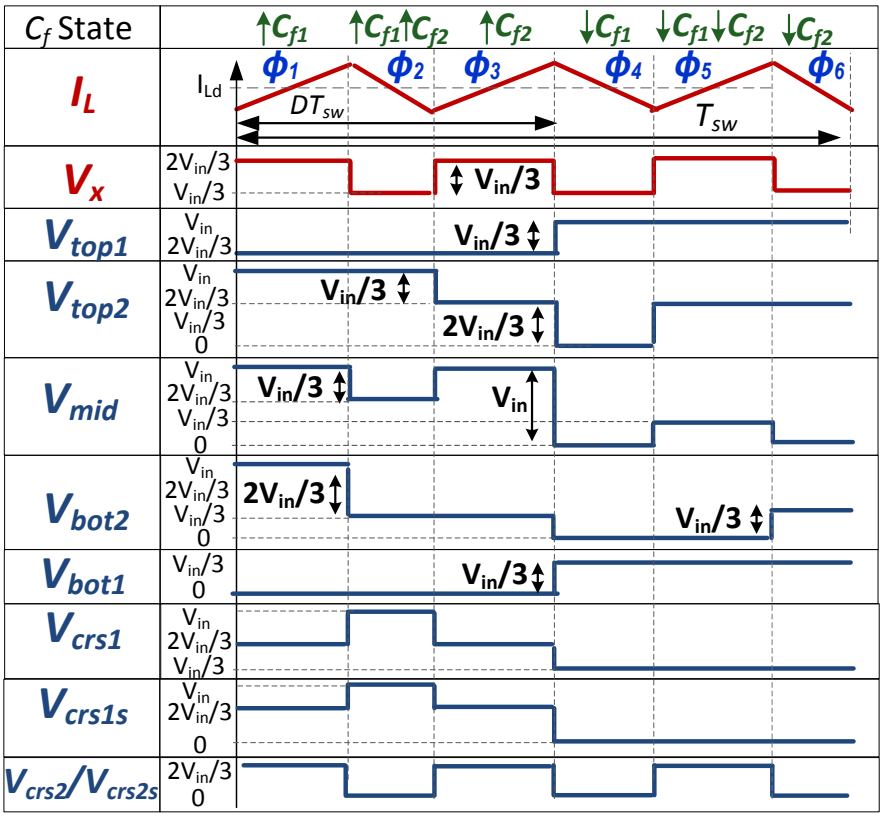

Figure 3.26: The equivalent Power stage gate signal timing diagram.

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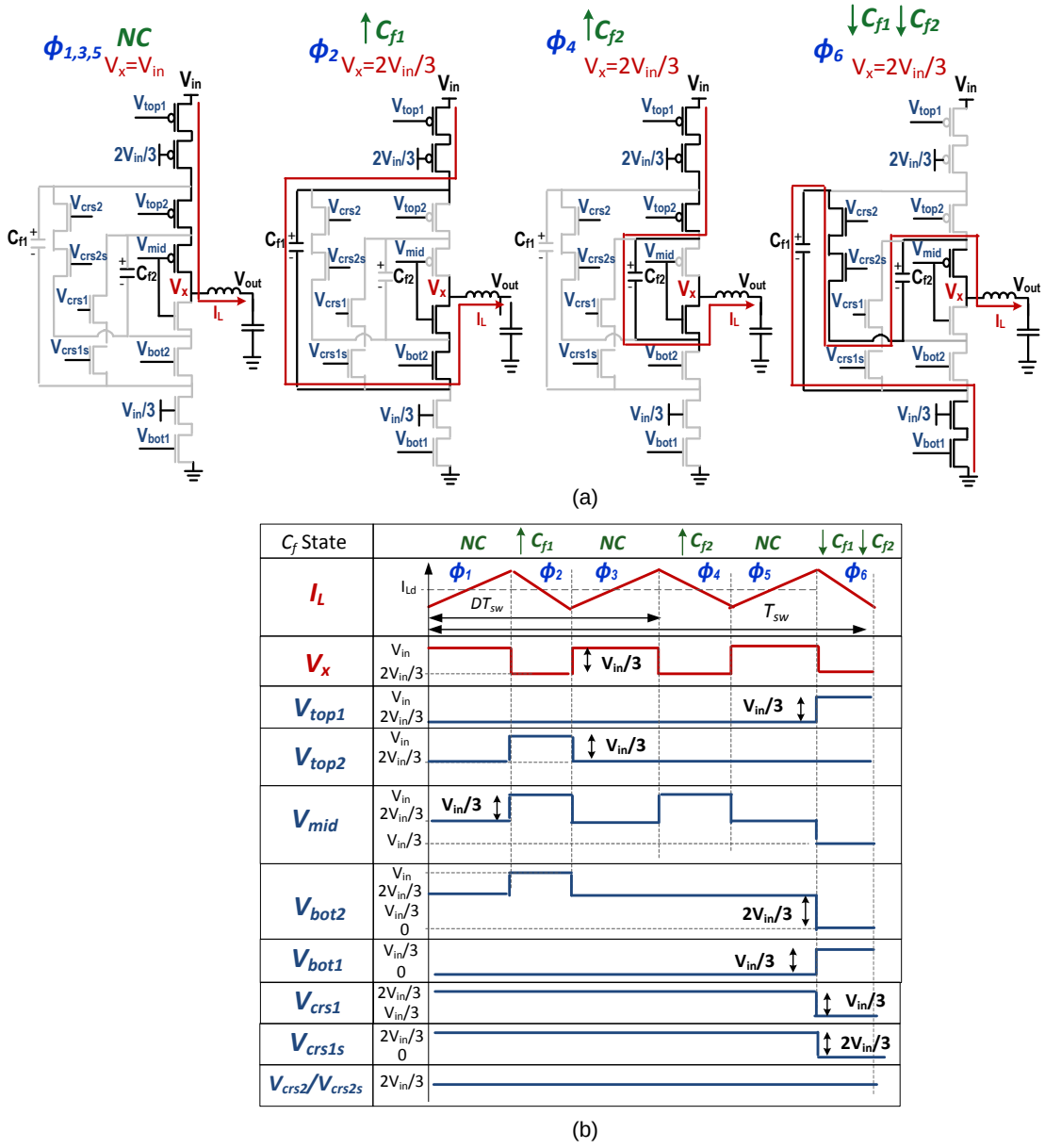

Figure 3.27: (a) Modified four-level converter current path in different inductor switching phases, operating on mode 3: $2V_{in}/3 < V_{out} < V_{in}$. (b) The equivalent Power stage gate signal timing diagram.

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3.8 Acknowledgement

Chapter 3 is based on and mostly a reprint of the following publications:

- S. S. Amin and P. P. Mercier, "A 78%-efficiency Li-ion-compatible fully-integrated modified 4-level converter with 0.01-40mW DCM-operation in 28nm FDSOI," *IEEE Custom Integrated Circuits Conference (CICC)*, San Diego, CA, 2018, pp. 1-4.

- S. S. Amin and P. P. Mercier, "A Fully-Integrated Li-ion-Compatible Hybrid 4-Level DC-DC Converter in 28nm FDSOI," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, March 2019.

The dissertation author is the primary investigator and author of the work in these papers.

Chapter 4

A Miniaturized Hybrid Single-Inductor Multiple-Output DC-DC Converter in 28nm FDSOI

As introduced in Chapter 1, the wireless sensor network device typically consists of three main functional modules: sensors, a processing unit, and an RF transceiver. The power management unit (PMU) is responsible for generating dedicated power supply rails for each module and delivering power efficiently. MISIMO energy harvester architecture presented in Chapter 2 performed independent multiple load regulation using a single inductor to meet the small form-factor needs of IoT devices. Although the proposed architecture is using bulky inductor (10μH) to achieve high efficiency but it enables net-zero energy system with autonomous operation by simultaneously aggregating the maximum power from multiple energy source while also managing the charging and discharging of a battery, all with a single inductor. In Chapter 3, a fully-integrated Li-ion compatible hybrid DC-DC converter for single-output in 28nm FDSOI presented to meet the small form-factor challenge of IoT and wearable applications while offering superior performance compared to prior-art fully-integrated converters. A hybrid 4-level topology proposed to achieve high efficiency while using the available low voltage transistors and low-quality on-chip passives. Although the fabricated converter achieves only 78% peak efficiency and integrating passives (i.e, inductor and capacitors) on 28nm silicon might be expensive, it is very useful implementation if area is the biggest concern because it eliminates the need for off-chip components.

In IoT applications; small size, long battery life (i.e, high efficiency), and low

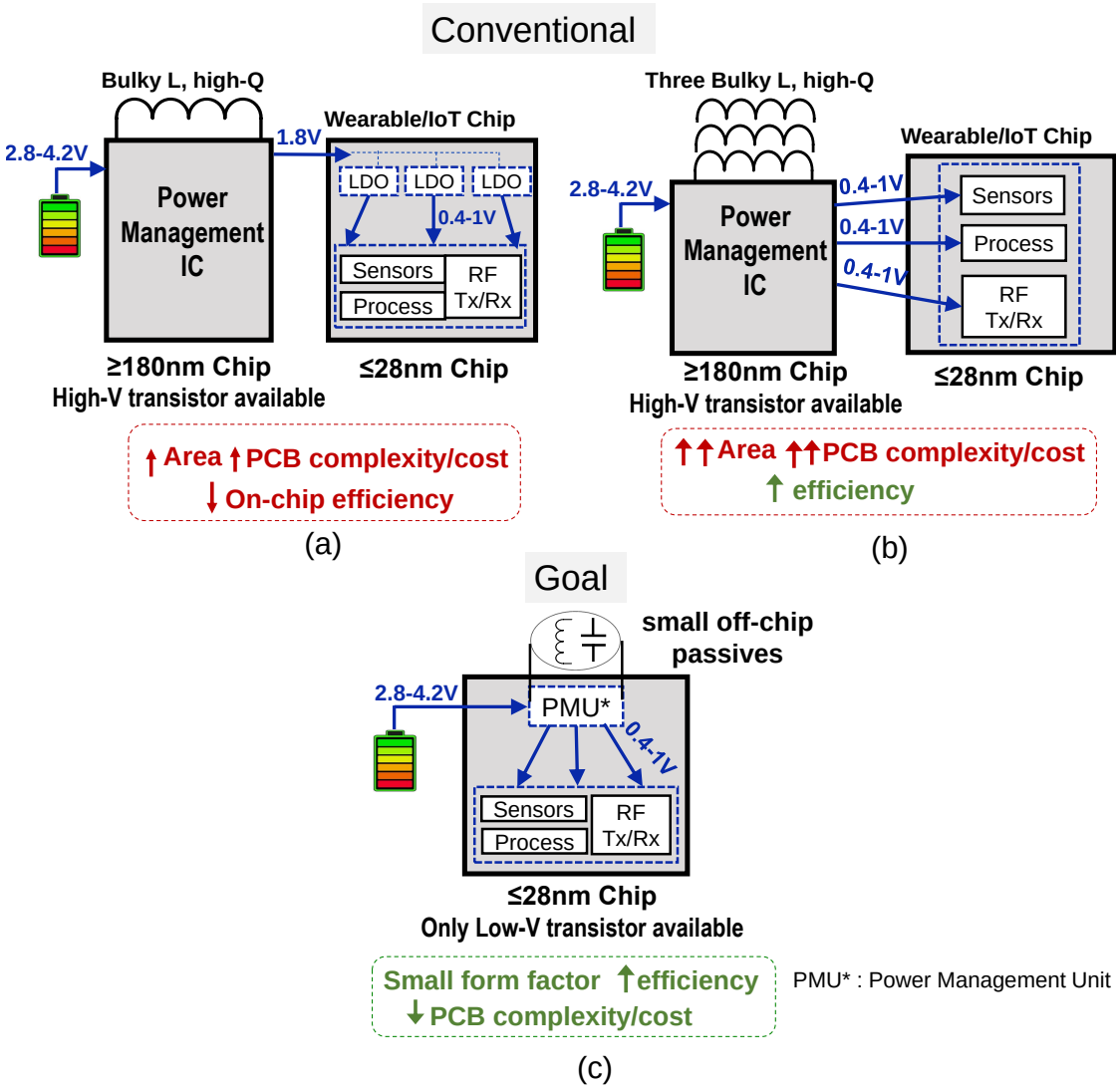

Figure 4.1: (a) Conventional PMIC for powering loads in scaled-CMOS followed by multiple inefficient LDOs for DVS. (b) Conventional PMIC with multiple switching regulators and multiple bulky off-chip inductors for efficient DVS. (c) Proposed concept of miniaturized hybrid SIMO in 28nm FDSOI.

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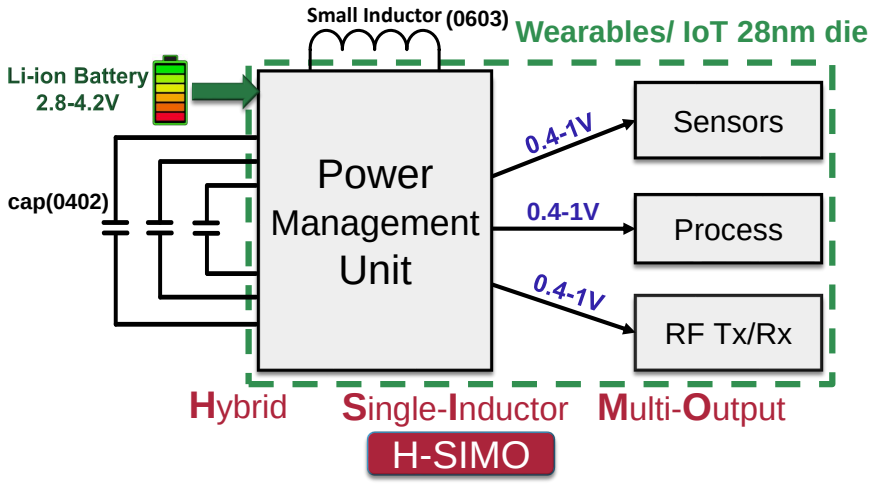

Figure 4.2: Hybrid SIMO for Powering IoT and Wearable Devices in Scaled CMOS.

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cost are three essential requirements. The work in this chapter presents a power management solution that can balance the three requirements. As mentioned in Chapter 3, small IoT and wearable devices implemented in scaled CMOS use Li-ion batteries with voltage range of 2.8-4.2V to supply their low power circuits operating at 0.6-1V. Typically, a discrete power management integrated circuit (PMIC) implemented in larger-geometry CMOS nodes ($\geq$ $180nm$), that can handle the high battery voltage and utilize bulky off-chip inductor to achieve high efficiency. Then, multiple LDOs are implemented on-chip in scaled-CMOS to supply different modules and perform dynamic voltage scaling (DVS), as shown in Figure 4.1(a). The employed large off-chip inductors and discrete components result in increased PCB design complexity/cost and increased overall system size. In addition, the use of multiple LDOs for multiple outputs DVS results in a dramatic efficiency degradation. Another conventional implementation is shown in Figure 4.1(b), where multiple independent switching regulators and multiple inductors are used to generate the multiple required supply rails. Although this is an efficient power management implementation but this method is bulky, noisy, expensive and not applicable for the small form-factor IoT applications. The objective of this work (Figure 4.1(c)) is to integrate the DC-DC conversion into the SOC itself on 28nm FDSOI

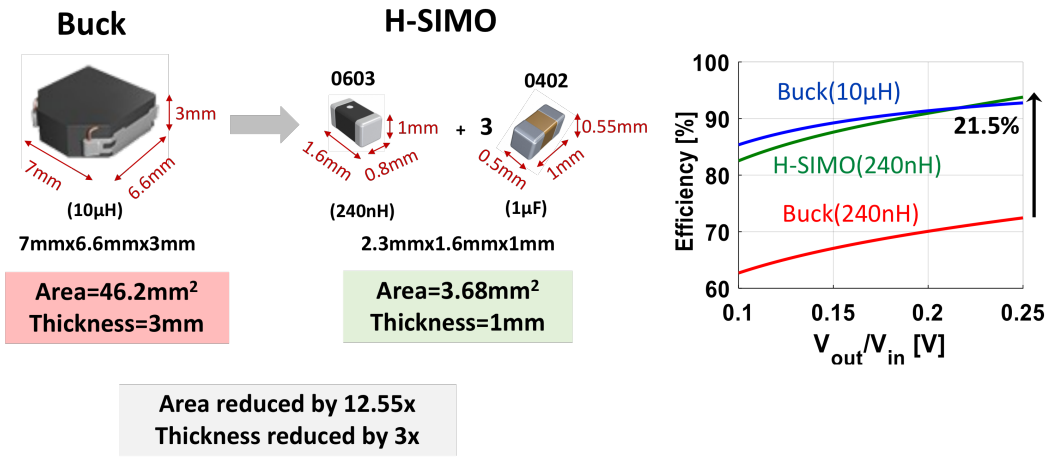

Figure 4.3: Towards small form-factor H-SIMO for powering IoT applications.

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and use switching topology with small off-chip passives to perform efficient independent multiple load regulation at different voltage and load conditions.

This chapter presents a 5-level hybrid single-inductor multiple-output (H-SIMO) DC-DC converter, shown in Figure 4.2 that enables a miniaturized, low cost, and efficient Li-ion compatible power management solution for next-generation IoT and wearable devices by: 1) utilizing the 1V-thin-oxide transistor of the 28nm FDSOI to build up the stacked power train necessary for 5-level converter without losing efficiency; 2) connecting flying capacitors to the existing internal nodes in the power train to convert the 2-level buck into 5-level, reducing the switching frequency by up to 76× for an up to 21.5% efficiency improvement; 3) eliminating the need for bulky inductor, reducing the area of the required off-chip passives by 12.55× and thickness by 3× (Figure 4.3); 4) performing efficient independent multiple load regulation using a single inductor embedded in a hybrid architecture; 5) eliminating the need for a clock generation by using the load comparators and zero-current-detector outputs as asynchronous clock for the DC-DC converter; 6) allowing the thin-oxide power train to operate in the sub-threshold at the startup during the power supply ramp up to charge the flying capacitors and avoid over-stressing the thin-oxide top-switch that would nominally implemented using thick-

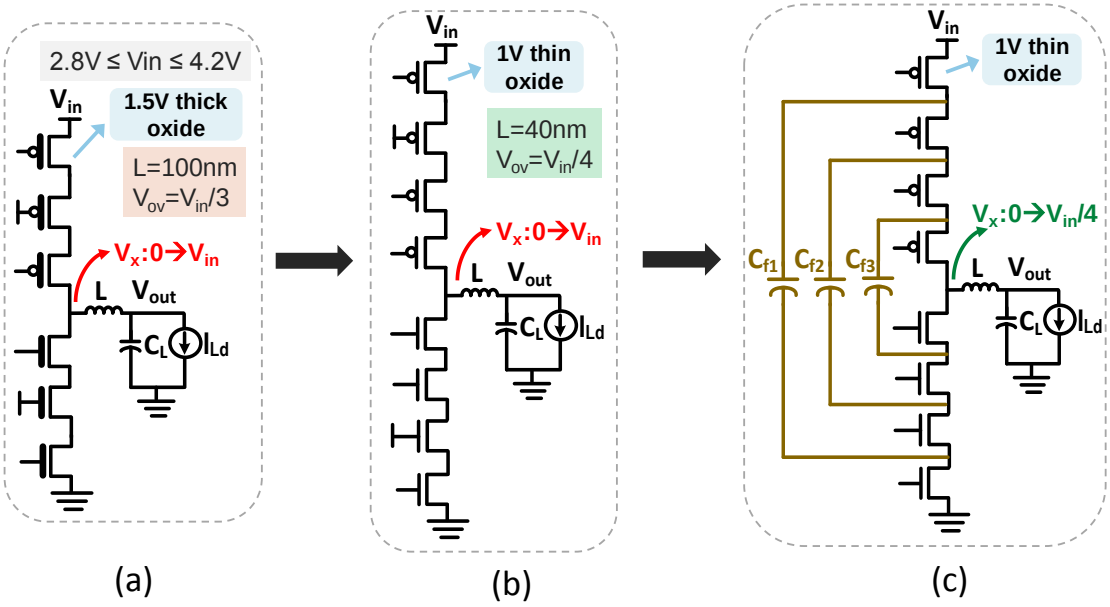

Figure 4.4: Building buck converter power stage by stacking: (a) 1.5V-transistors (b) 1V-transistors. (c) Converting the stacked thin-oxide 2-level buck into 5-level converter.

oxide transistor degrading efficiency.

This chapter is organized as follows: Section 4.1 provides an overview for the conventional 2-level buck solution using thick-oxide and thin-oxide transistors, then introduces the 5-level hybrid topology. Section 4.2 describes the power stage parasitic model and the associated losses. Section 4.3 then describes the hybrid topology switching phases. While Section 4.4 describes the multiple-outputs regulation algorithm employed. Section 4.5 details the circuit implementation of H-SIMO architecture. Finally, Section 4.6 describes H-SIMO startup.

4.1 Li-ion-Compatible DC-DC Converter

4.1.1 Stacked Buck in 28nm FDSOI

If a conventional 2-level buck converter were to be implemented with the thick-oxide 1.5V-transistors available in the employed 28nm process, operating from a Li-ion-compatible $V_{in} \leq 4.2V$, at least three transistors would be required to make up a power

switch, as depicted in Figure 4.4(a). Previously reported buck in scaled-CMOS [62, 63] showed that stacking the available low-voltage transistors in a Li-ion-compatible buck converter while achieving high efficiency is possible but with the use of a bulky off-chip inductor. Prior work [62] achieved a peak efficiency of only 87.4% using L=10μH ($10mm \times 10mm$) while utilizing the high-voltage drain extended transistors through a special process option, to help reducing the number of stacked transistors.

To achieve higher efficiency, thin-oxide 1V-transistors can be utilized and stacked to build the buck converter as shown in Figure 4.4(b). At least four transistors are required to block the $4.2V$ input voltage. Stacking lower voltage transistors would enable switching the transistors at lower voltage (i.e., $V_{in}/4$ instead of $V_{in}/3$). Although stacking 1V-transistors would add two extra switches to the power train, the ON resistance, r_{on}, and gate capacitance, C_g, of the 1V-thin-oxide transistor are lower than the 1.5V-thick-oxide transistor ($C_{g,1V} \approx 0.6C_{g,1.5V}$, $r_{on,1V} \approx 0.68r_{on,1.5V}$, i.e., $(RC)_{1V} = 0.4(RC)_{1.5V}$), reducing the power stage losses and making the overall efficiency higher. Although the overall improvement of efficiency is only $\approx$ 3.4% at L=240nH, the thin-oxide implementation always offer lower power stage losses than the thick-oxide implementation. It should be noted that $l = 40nm$ is used for the thin-oxide power switch sizing rather than the minimum length $l = 30nm$ to reduce the leakage losses.

Figure 4.5(a) and (b) show the current path in the inductor charging and discharging phases for a buck converter using 1.5V-thick-oxide transistor and the equivalent power stage gate signal timing diagram, respectively. While Figure 4.6(a) and (b) show the current path in the inductor charging and discharging phase for a buck converter using 1V-thin-oxide transistor and the equivalent power stage gate signal timing diagram, respectively.

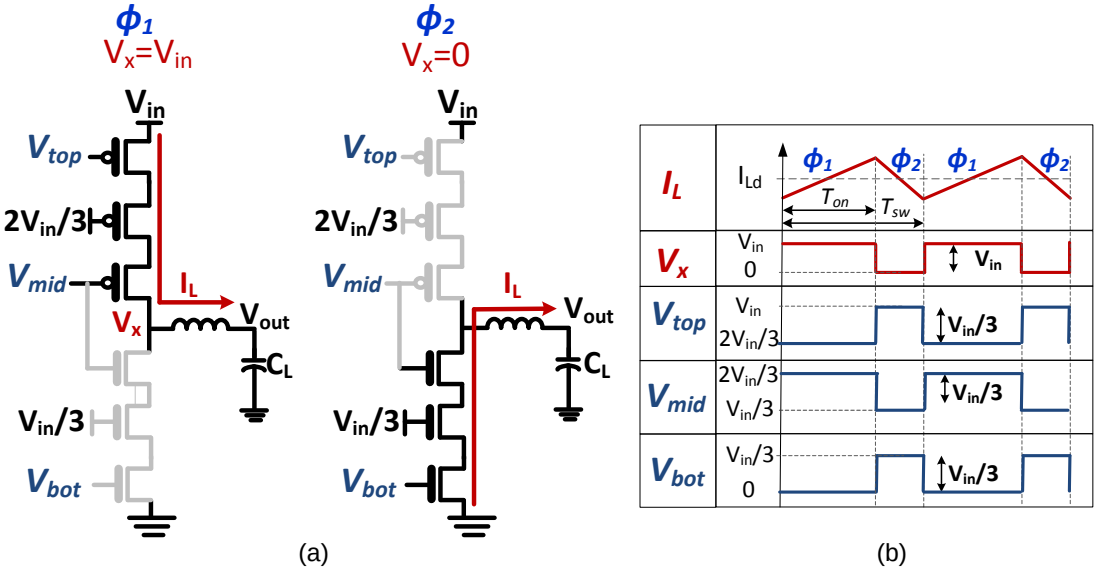

Figure 4.5: (a) Current path in inductor switching phases for a buck converter using 1.5V-thick-oxide transistor (b) Equivalent power stage gate signal timing diagram.

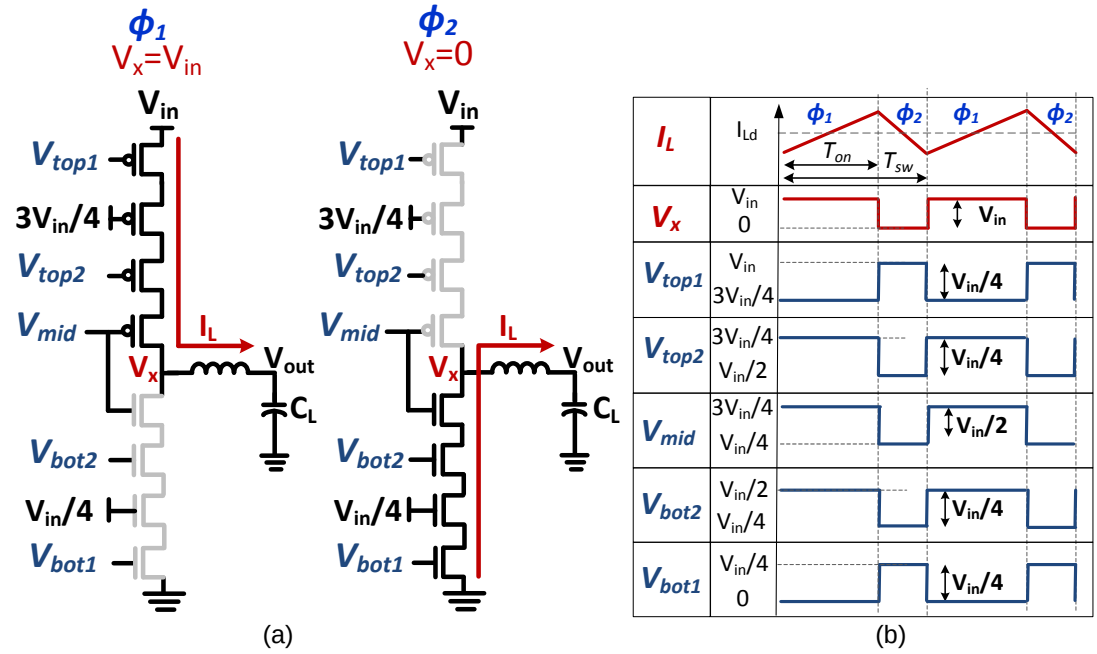

Figure 4.6: (a) Current path in inductor switching phases for a buck converter using 1V-transistor (b) Equivalent power stage gate signal timing diagram.

4.1.2 Miniaturization: Hybrid DC-DC Converter

The small inductor size (nH range) results in high switching frequency that causes high switching losses and efficiency degradation. This makes it difficult for prior work [62, 63] to implement a Li-ion compatible buck in scaled-CMOS with a small inductor. The switching frequency for a 2-level buck operation in DCM is given by:

$$F_{sw-2L} = \frac{2I_{Ld}V_{in}CR(1-CR)}{LI_{pk}^2}, \tag{4.1}$$

where I_{Ld} is the load current, CR is the conversion ratio (i.e., $CR = V_{out}/V_{in}$), and I_{pk} is the peak inductor current.To achieve higher efficiency with smaller inductor, it is advantageous to exploit the existing internal nodes of the stacked 2-level buck in Figure 4.4(b), and convert it into a 5-level converter by adding flying capacitors, as shown in Figure 4.4(c). The 5-level hybrid converter in Figure 4.4(c) effectively reduces the swing at the inductor terminal V_x from 0-to-V_{in} to 0-to-V_{in}/4. As a result, the switching frequency of the 5-level converter operating in DCM is:

$$F_{sw-4L} = \begin{cases} \frac{2I_{Ld}V_{in}CR(1/4-CR)}{LI_{pk}^2} & 0 < CR < 1/4; \\ \frac{2I_{Ld}V_{in}(CR-1/4)(1/2-CR)}{LI_{pk}^2} & 1/4 < CR < 1/2; \\ \frac{2I_{Ld}V_{in}(CR-1/2)(3/4-CR)}{LI_{pk}^2} & 1/2 < CR < 3/4; \\ \frac{2I_{Ld}V_{in}(CR-3/4)(1-CR)}{LI_{pk}^2} & 3/4 < CR < 1. \end{cases} \tag{4.2}$$

Figure 4.7 shows the normalized switching frequency versus the conversion ratio for the 2-level buck and the 5-level converter, operating in DCM with constant peak current. The figure shows that for the same value of inductor, the 5-level converter can reduce the switching frequency by $> 76\times$, which is translated into up to 21.5% improvement in the efficiency at $L = 240nH$, making this topology promising for a miniaturized battery-connected DC-DC converter in scaled technology.

The 5-level converter has four different modes of operation to support an output voltage from 0 to V_{in}, and the name 5-level comes from the fact that V_x node takes five

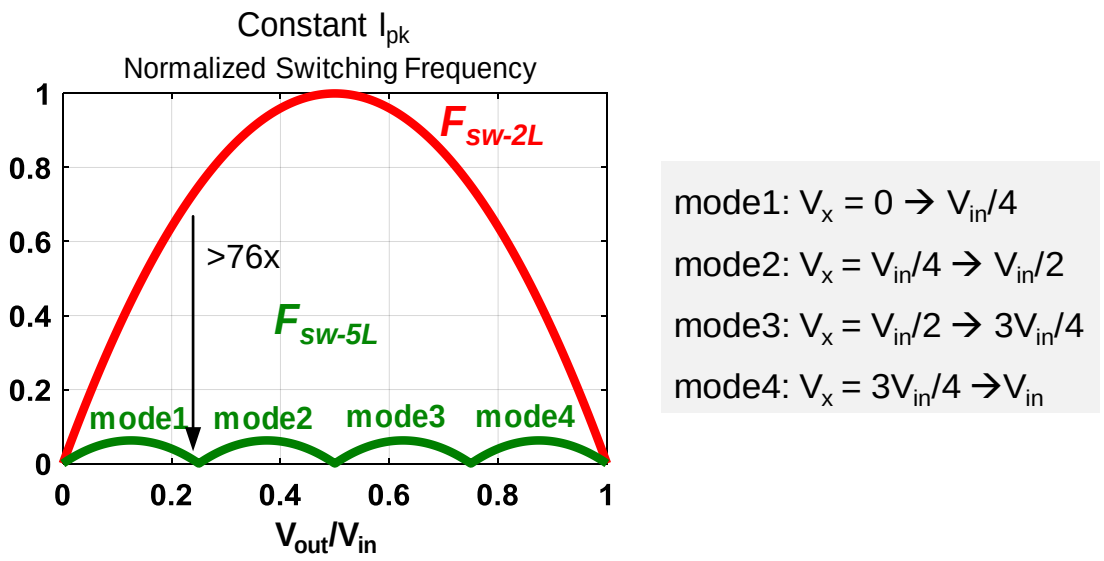

Figure 4.7: Normalized switching frequency versus the conversion ratio, for the 2-level buck and the 5-level converter, operating in DCM with constant peak current I_{pk}.

different values: 0, $V_{in}/4$, $V_{in}/2$, $3V_{in}/4$, and V_{in}. More specifically, V_x switches between 0 and $V_{in}/4$ (mode 1) or $V_{in}/4$ and $V_{in}/2$ (mode 2) or $V_{in}/2$ and $3V_{in}/4$ (mode 3) or $3V_{in}/4$ and V_{in} (mode 4), to enable output voltage range: $0 < V_{out} < V_{in}/4$, $V_{in}/4 < V_{out} < V_{in}/2$, $V_{in}/2 < V_{out} < 3V_{in}/4$, and $3V_{in}/4 < V_{out} < V_{in}$, respectively. At the boundary of the operating modes (i.e at $CR = 1/4,\ 1/2,\ 3/4,\ 1$), the inductor current ripple is approaching 0 and the converter operates as SC converter. In this prototype, mode 1 will be the primary mode of operation to target an output voltage of 0.6 to 1.0V from a Li-ion battery that varies between 2.8-4.2V.

4.2 Power Stage Losses Analysis

As detailed in Section 3.3, the dominant power stage losses, P_{loss}, in an inductive converter are comprised of conduction losses, P_{cond}, and switching losses, P_{sw}, (i.e., $P_{loss} = P_{cond} + P_{sw}$). The conduction and switching losses are represented by an effective resistance, R_{eff}, and an effective capacitance, C_{eff}, respectively as follows:

$$P_{cond} = \left(\frac{2}{3} I_{pk} I_{Ld}\right) R_{eff}, \tag{4.3}$$

$$P_{sw} = C_{eff} F_{sw} V_{in}^2 \tag{4.4}$$

The efficiency of a DC-DC converter is given by the following equation:

$$\eta = \frac{1}{1 + P_{loss}/P_{out}} \tag{4.5}$$

Figure 4.8 shows the power stage parasitic model of the three different topologies: 1.5V-thick-oxide buck, 1V-thin-oxide buck, and 5-level converter including the computed effective resistance and capacitance. The aggressive scaling of interconnect in 28nm CMOS technology makes the metal connections thinner and closely spaced, thus, increasing the interconnect resistance and capacitance significantly. As a result, the interconnections parasitic highly impacts the power stage losses and the overall efficiency so it becomes a must to include the interconnect resistance and capacitance in the parasitic model of the power stage. The dominant interconnect capacitance losses are the coupling capacitors between the source and drain metal connections of the power switch.

The computed R_{eff} for the three different topologies operating in mode 1 ($0 < V_{out} < Vin/4$) is:

- 2-Level Buck (1.5V-thick-oxide): $R_{eff} = 3r_{swo,1.5}/W + r_L + r_{int}$
- 2-Level Buck (1V-thin-oxide): $R_{eff} = 4r_{swo,1}/W + r_L + r_{int}$
- 5-Level: $R_{eff} = 4r_{swo,1v}/W + r_L + 6CR\, r_c + r_{int}$

where r_{swo} is the transistor ON resistance per unit width, and r_{int} is the interconnect resistance. The computed C_{eff} for the three different topologies can be expressed as following:

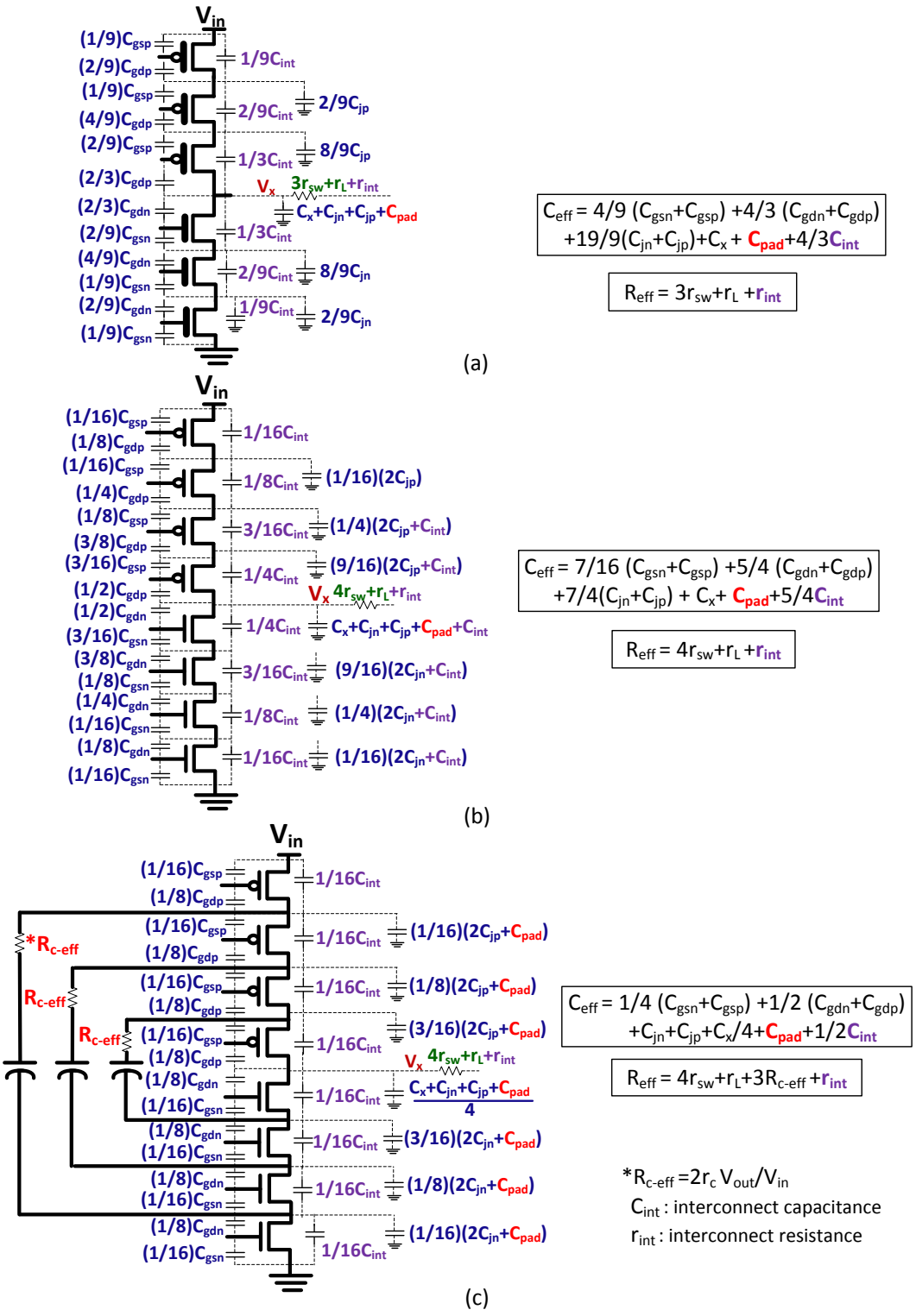

Figure 4.8: Power stage parasitic model including the equivalent effective resistance and effective capacitance computed based on voltage switching on each node and normalized to V_{in}^2: (a) two-Level Buck using 1.5V-transistors, (b) two-Level Buck using 1V-transistors, and (c) five-level converter.

Table 4.1: Effective resistance and capacitance for different topologies.

	2-Level Buck		5-Level
	1.5V	1V	
R_{eff}	$3r_{sw,1.5} + r_L + r_{int}$	$4r_{sw,1} + r_L + r_{int}$	$4r_{sw,1} + r_L + 6CR\ r_c + r_{int}$
C_{eff}	$3.6C_{gn,1.5} + 8.4C_{jn,1.5} + C_x + 2.1C_{int}$	$3.4C_{gn,1} + 7C_{jn,1} + C_x + 1.75C_{int}$	$K_{5L}(1.5C_{gn,1} + 4C_{jn,1} + C_x/4 + C_{pad} + C_{int})$

$C_{g,1} = 0.6\ C_{g,1.5}$
$r_{sw,1} = 0.68\ r_{sw,1.5}$

- 2-Level Buck (1.5V-thick-oxide):

  $C_{eff} \approx 3.556WC_{gno} + 8.4WC_{jno} + C_x + C_{pad} + 1.33C_{int}$

- 2-Level Buck (1V-thin-oxide):

  $C_{eff} \approx 3.375WC_{gno} + 7WC_{jno} + C_x + C_{pad} + 1.25C_{int}$

- 5-Level:

  $C_{eff} \approx K_{5L}(1.5WC_{gno} + 4WC_{jno} + C_x/4 + C_{pad} + 0.5C_{int})$,

where C_{gno} and C_{jno} are capacitance per unit width, C_x is the parasitic capacitance at V_x node, C_{pad} is the capacitance seen at the pad, C_{int} is the interconnect capacitance, and K_{5L} is the multilevel converter improvement factor, described in details in Section 3.3.2. For fair comparison between the three topologies, the effective capacitance is computed at the same switching frequency. Thus, the total power stage capacitance is multiplied by K_{5L}, where $K_{5L} = F_{sw}/F_{sw-2L}$ (i.e., $K_{4L} = (1 - CR)/(1/4 - CR)$ for the 5-level converter, operating in mode 1).

Table 4.1 summarizes R_{eff} and C_{eff} of the three different topologies. It should be noted that C_{eff} of the 5-level converter is significantly lower than C_{eff} of the 2-level converter.

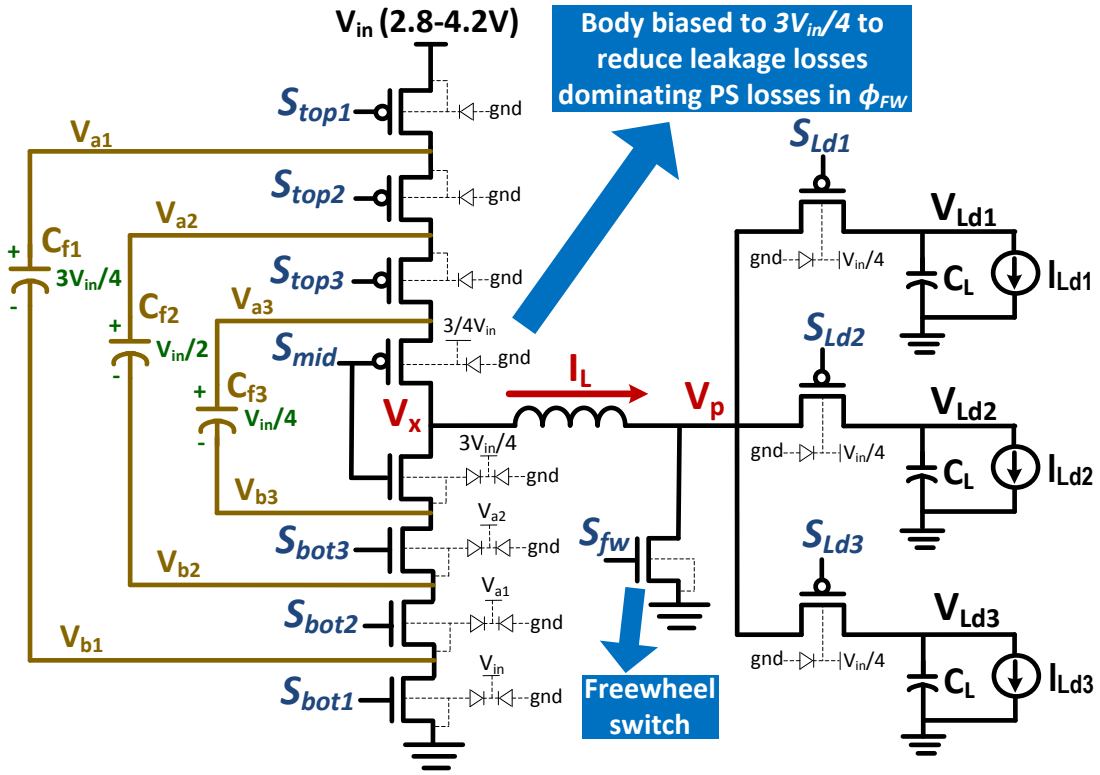

Figure 4.9: Proposed hybrid single inductor multiple output (H-SIMO) power stage.

4.3 Power Stage and Switching Phases

Figure 4.9 shows the detailed schematic of the DCM-operated H-SIMO power stage. Figure 4.10 shows the current path in the nine different inductor switching phases in one H-SIMO switching cycle when V_{Ld1} is selected as an output, along with the power stage gate voltages in each phase. The voltage at the gate of power switches in each phase is set such that the gate-to-source, V_{gs}, gate-to-drain, V_{gd}, and drain-to-source, V_{ds}, voltages of each power stage transistor never exceeds $V_{in}/4$. Thus, no transistor exceeds its maximum voltage rating, even at the highest compatible V_{in}. Figure 4.11 shows the corresponding inductor current waveform and the voltage at the inductor terminal V_x node. The nine inductor switching phases can be described as follows:

- Phase ϕ_1: C_{f1} is charged, C_{f2} and C_{f3} are not connected, $V_x = V_{in}/4$, and V_p connected to the output.

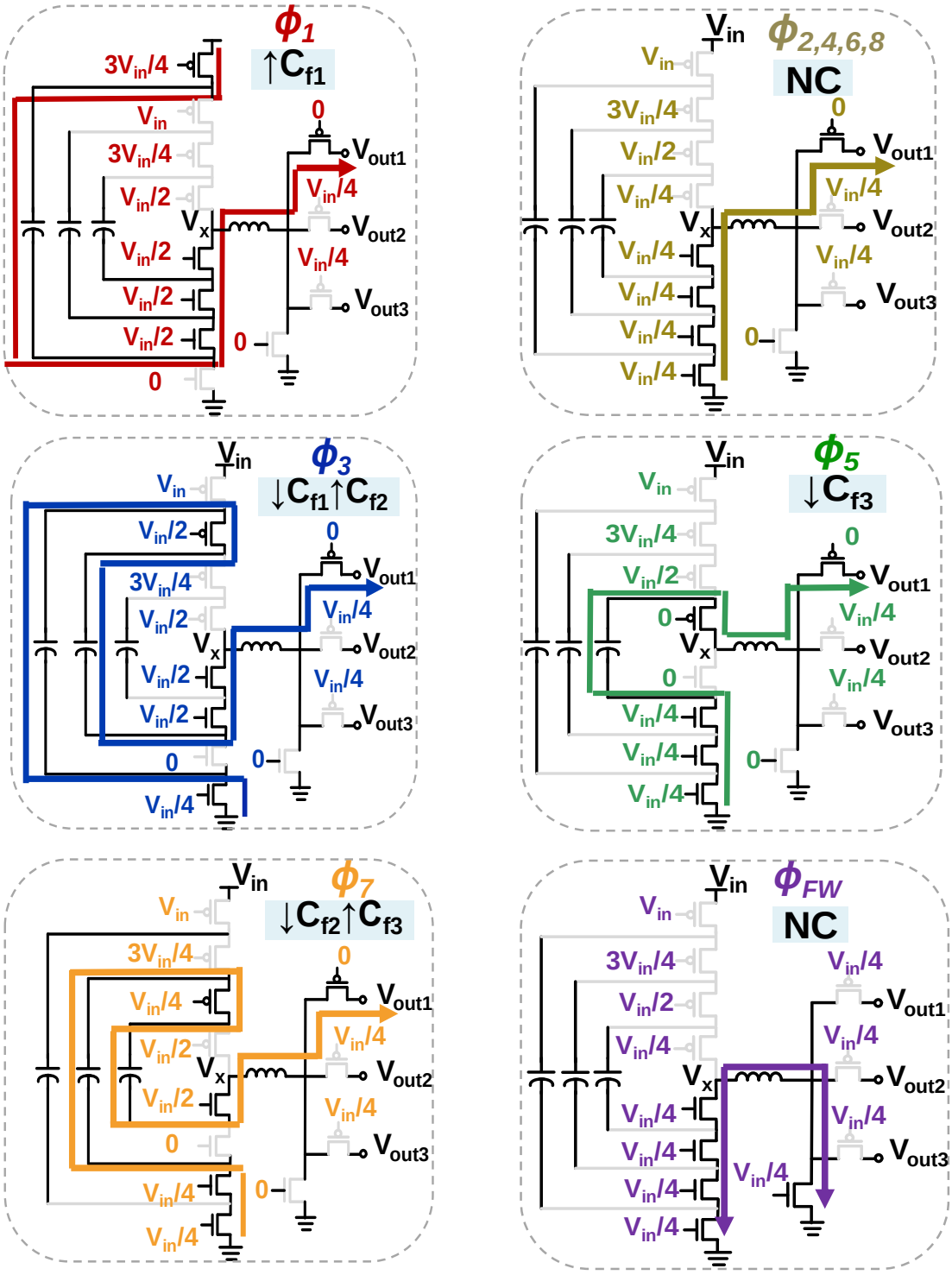

Figure 4.10: H-SIMO current path along with the gate voltage of each power stage transistor in nine inductor switching phases (one switching cycle), when V_{out1} is selected as an output.

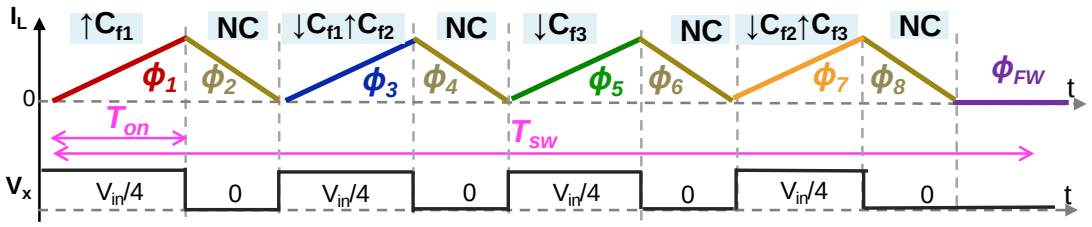

Figure 4.11: Inductor current waveform and voltage at V_x node equivalent to the nine inductor switching phases shown in Figure 4.10.

- Phases $\phi_{2,4,6,8}$: C_{f1}, C_{f2}, and C_{f3} are not connected, $V_x = 0$, and V_p is connected to the output.
- Phase ϕ_3: C_{f1} is discharged, C_{f2} is charged, C_{f3} is not connected, $V_x = V_{in}/4$, and V_p is connected to the output.
- Phase ϕ_5: C_{f1} and C_{f2} are not connected, and C_{f3} is discharged, $V_x = V_{in}/4$, and V_p is connected to the output.
- Phase ϕ_7: C_{f1} is NC, C_{f2} is discharged, C_{f3} is charged, $V_x = V_{in}/4$, and V_p is connected to the output.
- Phase ϕ_{FW}: C_{f1}, C_{f2}, and C_{f3} are not connected, $V_x = 0$, $V_p = 0$, the freewheel switch is enabled, and the output is disconnected.

The inductor is time shared among the three output loads and the same nine inductor switching phases enabled when V_{Ld2} or V_{Ld3} is selected as an output, as shown in Figure 4.12.

4.4 H-SIMO Multiple Load Regulation

Section 2.3 described the different switching schemes for single inductor multiple load regulation and discussed the advantages and disadvantages of each scheme. The switching schemes in Figure 2.12 for buck-boost converter can be applied to buck converters as well. In scheme 1 and scheme 2, inductor switching cycle is dedicated

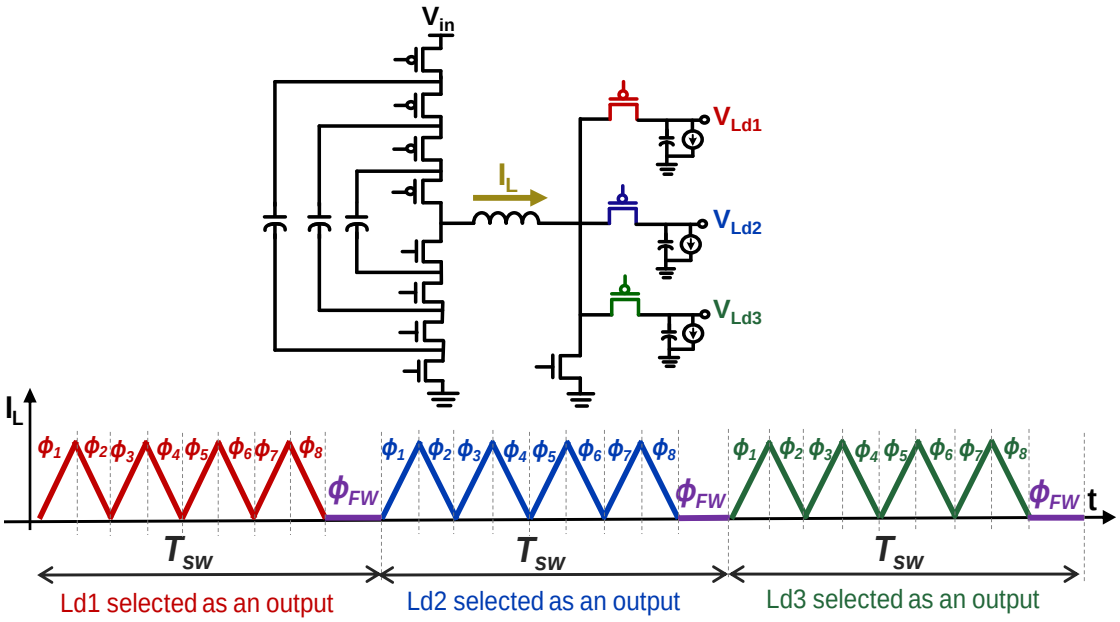

Figure 4.12: Inductor current waveform for the time shared inductor among the three outputs. Each output is selected for nine inductor switching phases.

for each load while scheme 3 suggested charging all loads in one switching cycle to reduce switching frequency. Although scheme 3 can offer lower switching losses and ripple than other schemes but can't be employed in hybrid architecture because if the output voltages of the three output loads are different, the inductor charging time, T_{on}, will be different and the capacitors charge balance will not be maintained. Therefore, scheme 1 and scheme 2 are the appropriate switching schemes for H-SIMO. As mention before in Section 2.3, the controller of scheme 1 never switches to the next load until the current load receives sufficient energy, making the high load dominates the inductor causing cross regulation and voltage droop in case of load step. While scheme 2 limits the number of cycles for each load to avoid cross regulation and voltage droop. H-SIMO adopts scheme 2 and never switches to the next load before the end of the eight inductor switching phases to maintain the capacitor charge balance. It also prevents charging the same load in two successive switching cycles if other loads requires energy to avoid cross regulation and voltage droop.

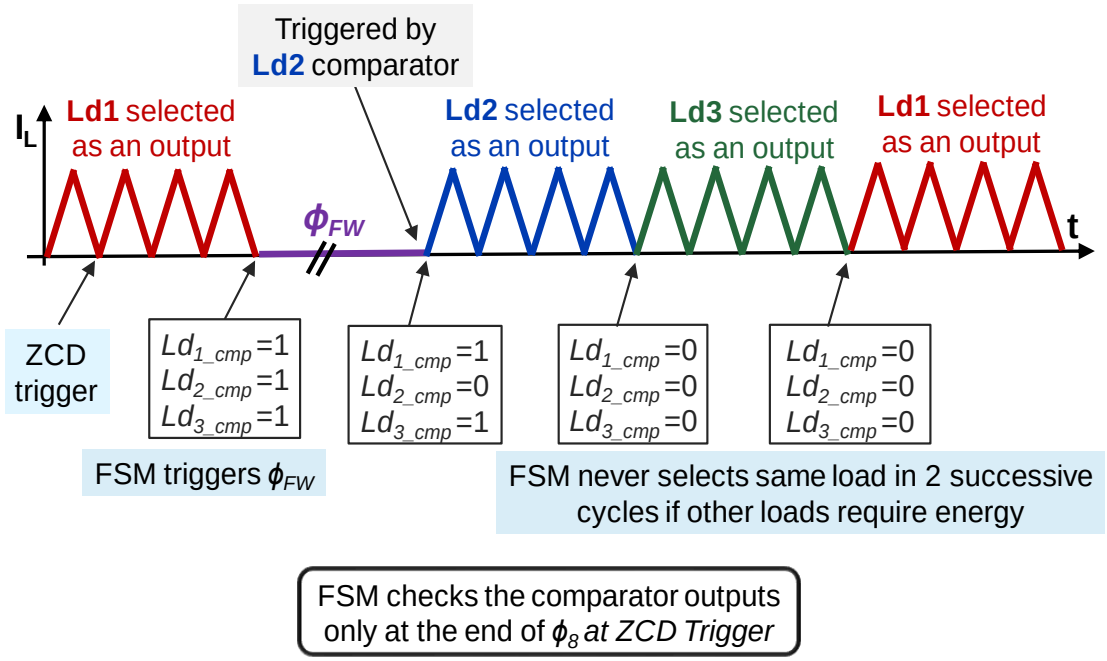

Figure 4.13: Inductor current timing diagram describing the finite state machine (FSM) operation under different load conditions.

4.4.1 H-SIMO Event-Driven Asynchronous Controller

H-SIMO controller is event driven controller and doesn't require external clock except at startup. A slow clock ($\sim 10kHz$) is required during supplies ramp up at startup to charge the flying capacitors, described later in Section 4.6. After that, the negative edge of the chip RST pulse kick start the first inductor charging phase. Then during the operation of the H-SIMO, there are three trigger sources: 1) the ON-time control block the triggers the end of the inductor charging phase; 2) the zero current detector (ZCD) output that triggers the start of inductor charging phase; 3) the load comparators outputs that trigger new switching cycle during the freewheel phase.

4.4.2 H-SIMO Control Algorithm

The outputs are regulated using constant ON-time pulse-frequency modulation (PFM). The controller operation is illustrated in the inductor timing diagram in Figure 4.13. The finite state machine (FSM) checks the comparator output every eight

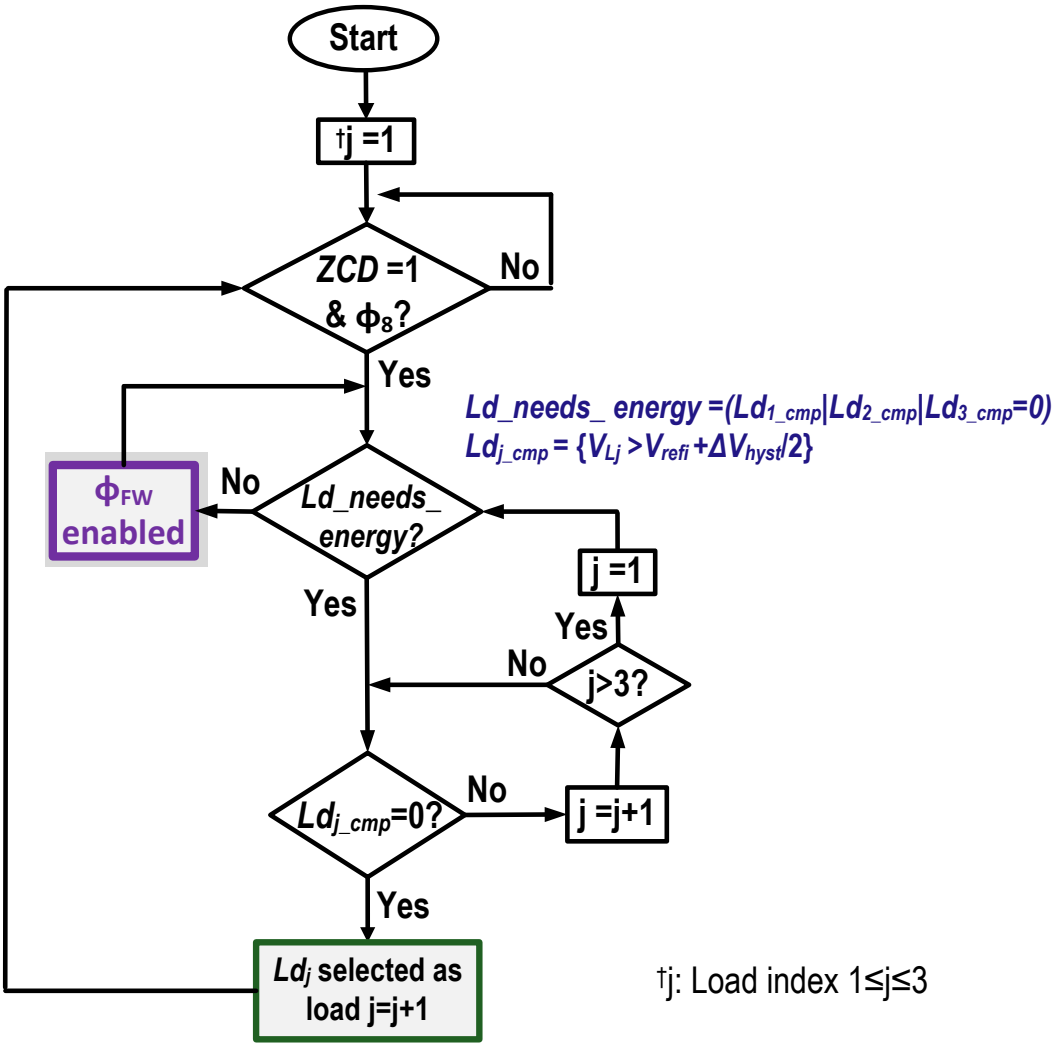

Figure 4.14: H-SIMO controller flowchart.

inductor switching phases. At the end of ϕ_8, if all loads have sufficient energy indicated by the load comparators outputs, the FSM triggers the freewheel phase ϕ_{FW}. During the freewheel phase, if any of the loads comparator outputs go low, the new eight inductor switching phases will be triggered by the comparator output of the load that requires energy. The FSM will never select the same output for two successive cycles if other outputs require energy to reduce cross regulation and avoid voltage droop.

Figure 4.14 shows the proposed H-SIMO control algorithm. The proposed algorithm selects one of the three loads as an output for one or more switching cycles

based on the load condition or enables the freewheel phase. The load condition is defined by two signals Ld_{j_cmp} and ld_needs_energy, where j is the load index. The ld_needs_energy signal is asserted if the output of any of the load comparators (i.e., $Ld_{j\_cmp} =' 0'$); which indicates that one of the loads require energy. The controller is triggered only in ϕ_8 when zero current is detected ($ZCD =' 1'$) or in ϕ_{FW} if any of the loads requires energy (i.e., $ld\_needs\_energy =' 1'$). If any of the three loads have an energy deficit ($Ld_{j\_cmp} =' 0'$), the controller triggers new switching cycle (8 phases) for the selected output. Otherwise, the controller enables the freewheel phase. During ϕ_{FW}, ld_needs_energy signal triggers the controller if any of the loads require energy to enable new eight inductor switching phases.

4.5 H-SIMO Architecture and Circuit Details

Figure 4.15 shows the proposed H-SIMO architecture. It consists of a power stage, non-overlap circuits, level shifters, drivers, load comparators, a ZCD circuit, and a digital controller. The proposed H-SIMO architecture operates in discontinuous conduction mode (DCM) and independently regulates three different output power rails. As mentioned earlier in Section 4.4.1, H-SIMO is self-clocked architecture, external slow clock is required only during startup. All the transistors used in the Li-ion compatible H-SIMO prototype are 1V-thin-oxide transistors except for the decoupling capacitors. As a result, the delay and losses are low compared to the thick-oxide implementation.

4.5.1 Driver Circuits

Figure 4.10 shows the power switches gate voltages in the nine different inductor switching phases. The voltage at the gate of power switches in each phase is set such that the V_{gs}, V_{gd}, and V_{ds}, never exceed $V_{in}/4$. Thus, no transistor exceeds its maximum voltage rating, even at the highest compatible V_{in}. Figure 4.16 shows a timing diagram including the inductor current waveform and the power switches gate voltages. It should

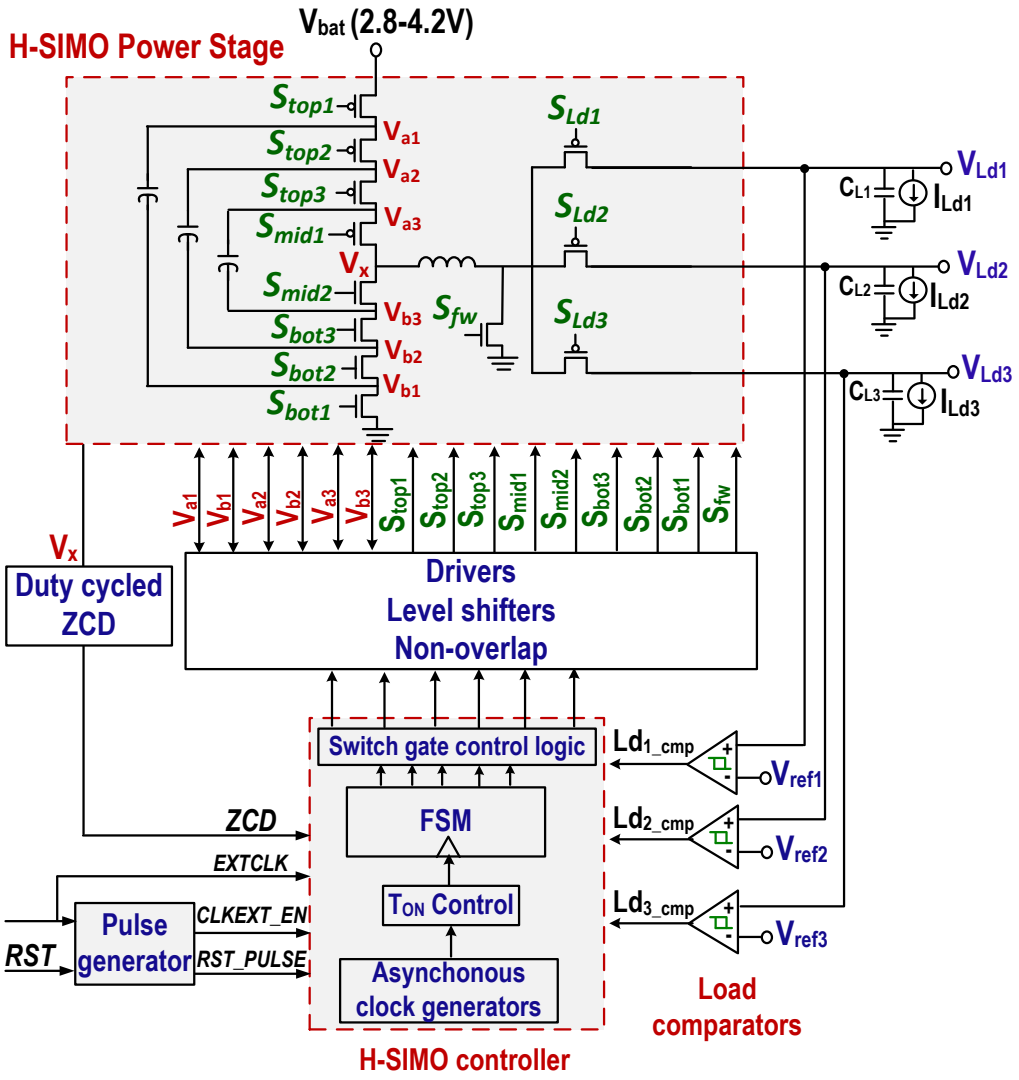

Figure 4.15: Block diagram of asynchronous H-SIMO architecture.

be noted that gate signals: S_{top2}, S_{top3}, S_{mid1}, S_{mid2}, S_{bot2}, and S_{bot3} are 3-level signals and require special design for the corresponding power switches drivers.

The proposed detailed schematic of the drivers architecture is shown in Figure 4.17. The proposed drivers driving the power switches with 3-level gate signals utilize the positive and negative switching terminals of the the flying capacitors as power and ground rails to reduce the number of the required stacked transistors and level shifters in drivers.

Figure 4.18 shows the equivalent drivers waveforms. The top switch gate volt-

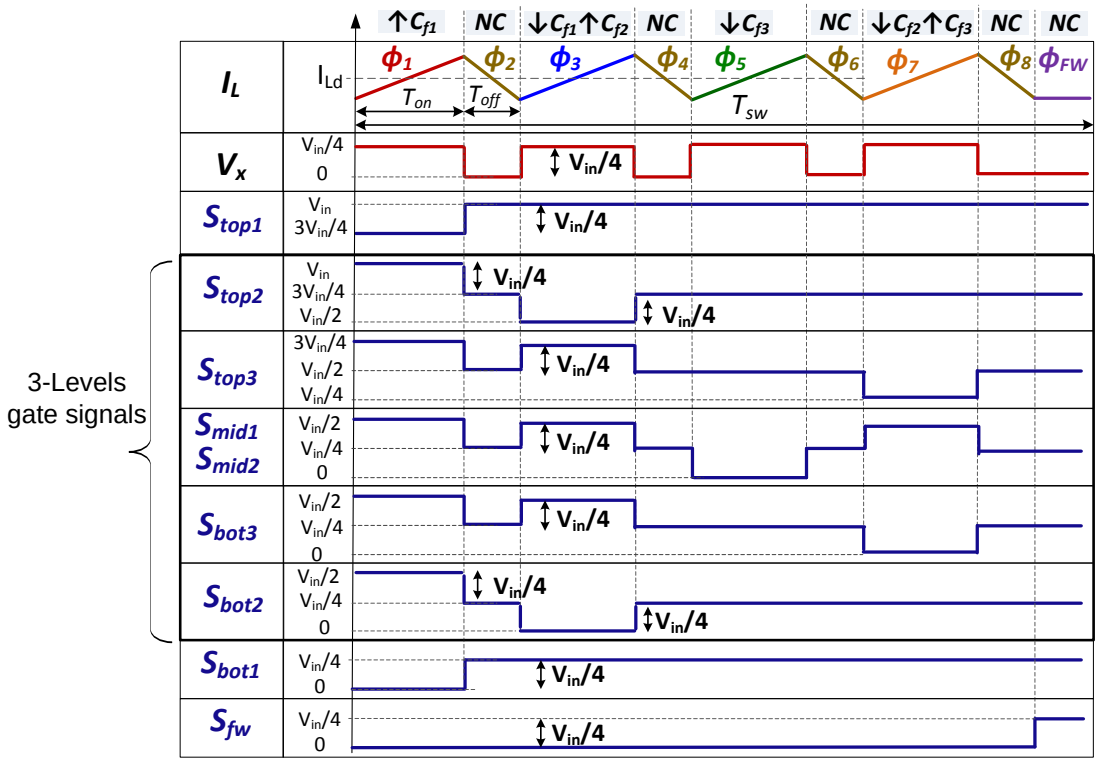

Figure 4.16: Power stage timing diagram showing the inductor current, the voltage at inductor terminal V_x, and the power switches gate voltage in different switching phases.

age, S_{top1}, switches between $3V_{in}/4$ and V_{in} and thus requires a level shifter to shift up the input FSM signal switching between GND and $V_{in}/4$ to a signal switching between $3V_{in}/4$ and V_{in}. Signals S_{bot1}, S_{Ld1}, S_{Ld2}, S_{Ld3} and S_{fw} switch between GND and $V_{in}/4$, and thus use a conventional 2-transistor inverter-based CMOS driver.

The drivers of the two middle switches with gate voltages S_{mid1} and S_{mid2} utilize the switching positive terminal of C_{f3} (V_{a3}) and the switching negative terminal of C_{f3} (V_{b3}) as power and ground rail, respectively. Since the voltage across the flying capacitors equals $V_{in}/4$, stacked drivers are not required, but rather conventional 2-transistor inverter-based CMOS drivers is utilized to drive the 3-level gate signals and no level shifters required. A non-overlap between g_{mid1} and g_mid_2 is added before the drivers.

The bottom switches with gate voltages S_{bot2} and S_{bot3} require drivers with stacked transistors shown in Figure 4.17. Drivers S_{bot2} and S_{bot3} utilize the negative switching terminals of C_{f1} (V_{b1}) and of C_{f2} (V_{b2}) as power/GND rails, respectively to

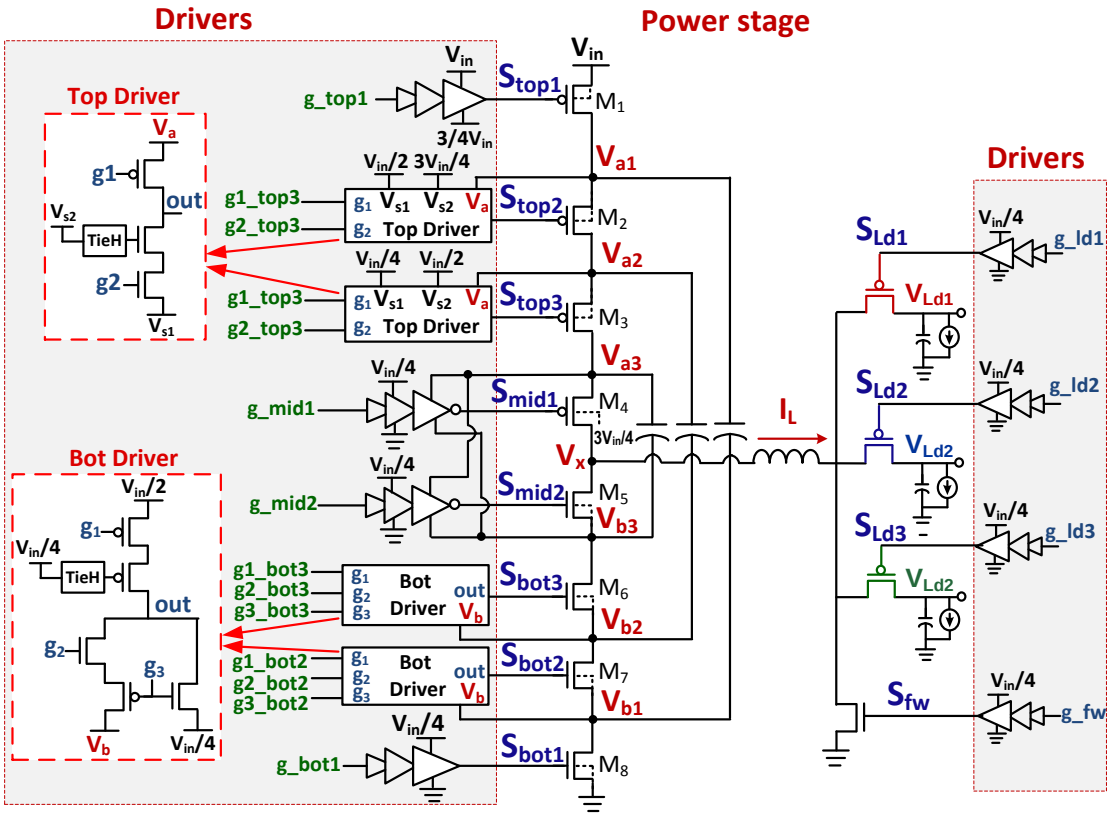

Figure 4.17: Detailed schematic of H-SIMO power stage drivers architecture.

reduce the number of stacked transistors and level shifters. The input voltages of S_{bot2} and S_{bot3} drivers: $g1\_bot2$, $g2\_bot2$, $g1\_bot3$, and $g2\_bot3$, shown in Figure 4.18 require level shifters to shift up the FSM signal switching between GND and $V_{in}/4$ to a signal switching between $V_{in}/4$ and $V_{in}/2$.

The top switches with gate voltages S_{top2} and S_{top3} require drivers with stacked nMOS transistors shown in Figure 4.17. Drivers S_{top2} and S_{top3} utilize the positive switching terminals of C_{f1} (V_{a1}) and of C_{f2} (V_{a2}) as power/GND rails, respectively to reduce the number of stacked transistors and level shifters. The S_{top2} and S_{top3} driver waveforms are shown in shown in Figure 4.18. The input voltages of S_{top2}: $g1\_top2$ and $g2\_top2$ require level shifters to shift up the FSM signal switching between GND and $V_{in}/4$ to a signal switching between $V_{in}/2$ and $3V_{in}/4$. While the input voltages of S_{top3}: $g1\_top3$ and $g2\_top3$ require level shifters to shift up the FSM signal switching

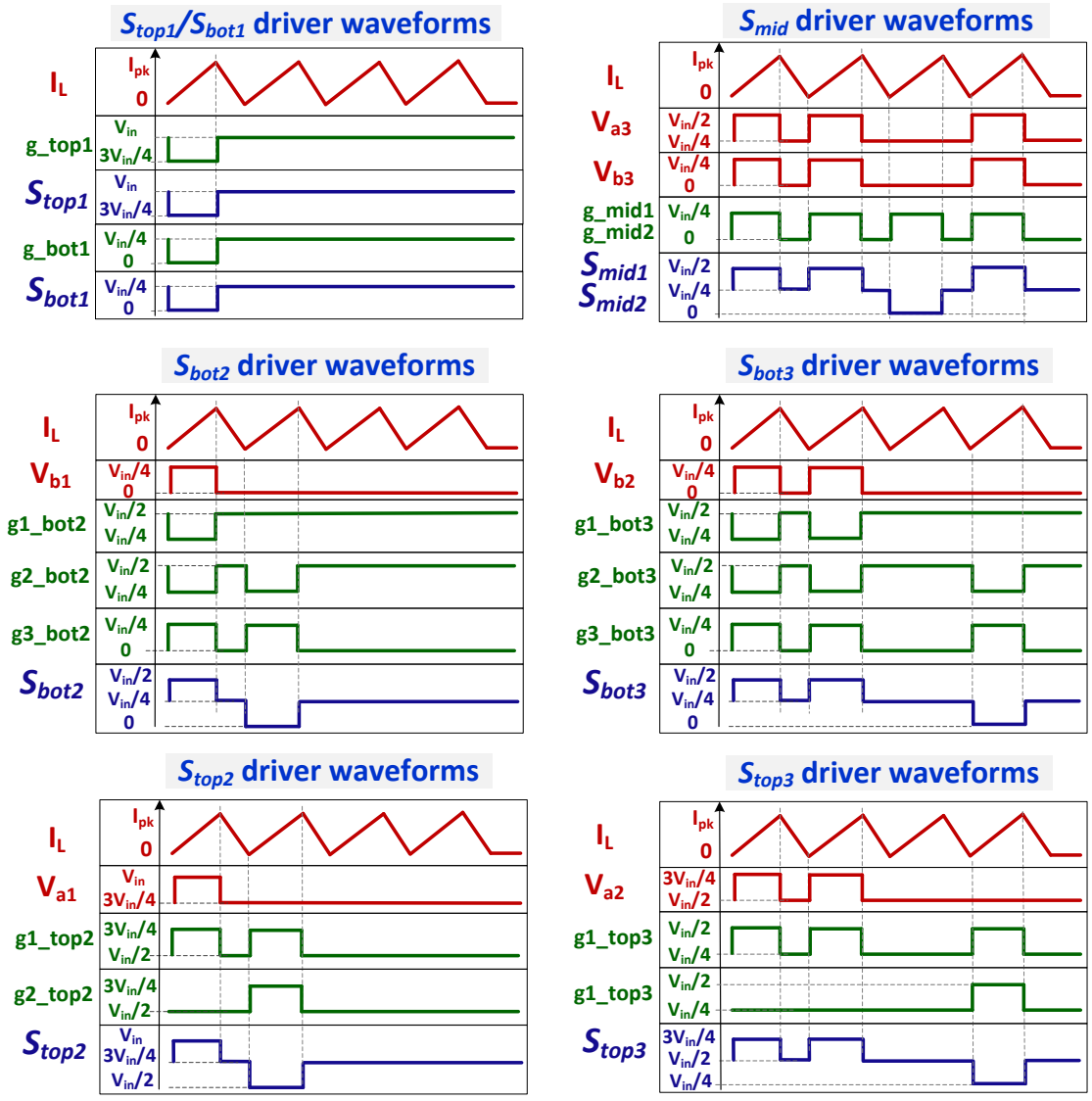

Figure 4.18: H-SIMO power stage drivers timing diagrams.

between GND and $V_{in}/4$ to a signal switching between $V_{in}/4$ and $V_{in}/2$.

4.5.2 Level Shifters

The top switch M_1 driver requires a level shifter to convert the FSM output signal switching between GND and $V_{in}/4$ to signal switching between $3V_{in}/4$ and V_{in}. The drivers of M_3, M_6, and M_7 require level shifter to shift up the FSM signal switching between GND and $V_{in}/4$ to a signal switching between $V_{in}/4$ and $V_{in}/2$. While the driver M_2 requires level shifter to shift up the FSM signal switching between GND and $V_{in}/4$ to a signal switching between $V_{in}/2$ and $3V_{in}/4$.

Figure 4.19 shows the proposed level shifter. A single cell can shift the signal by $V_{in}/4$. Then can be cascaded to achieve the desired level-shifting. The proposed topology is all digital and ensures that no transistor exceeds the maximum voltage of $V_{in}/4$. Hence, all transistors are 1V-thin-oxide. FDSOI body biasing is used to improve performance by reducing the threshold voltage when turned ON and reducing leakage when turned OFF. The low input voltage is shifted-up by the positive feedback action of the cross-coupled transistors. Connecting the body of the cross-coupled transistors to their drains instead of their sources reduces the strength of the pMOS latch [67], and hence enables fast transitions and reduces the level shifter delay. Connecting the body of the top MOSFETS transistors to a high voltage reduces the leakage power consumption.

4.5.3 Asynchronous Clock Generation

Figure 4.20 shows the circuit details of the asynchronous clock generation and T_{on} control. The negative edge of the chip RST signal acts as the first trigger to kick-start H-SIMO after startup (described later in Section 4.6). The ON time control bits, $T_{on}\_bit < 3:0 >$, are the bits controlling the pulse width, T_{on}, of H-SIMO clock. A binary-wighted MOM-capacitor delay-controlled line is used to generate the pulse using the $T_{on}\_bit < 3:0 >$ control bits, as illustrated in Figure 4.20. As shown in Figure 4.20, the zero current detector output, ZCD, is the clock trigger if the converter

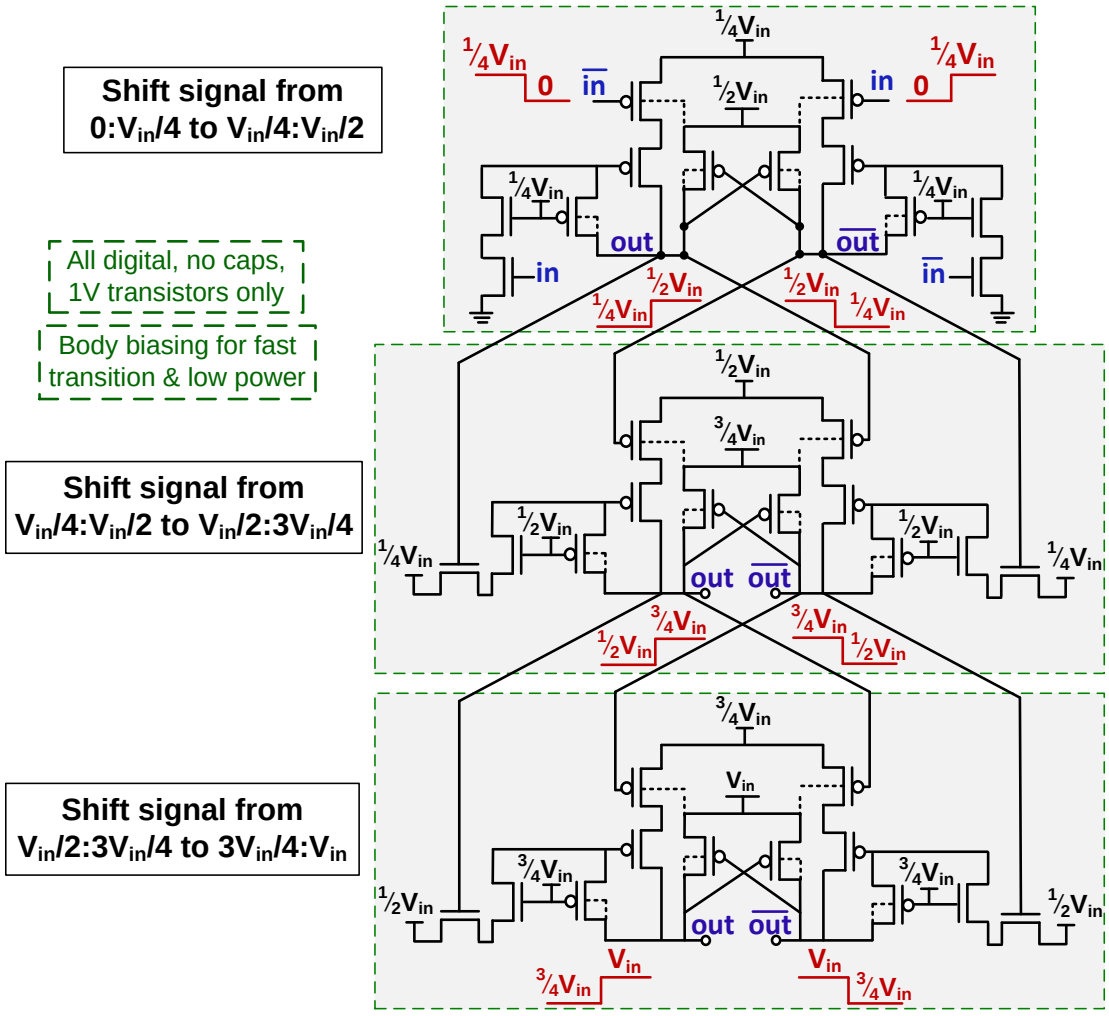

Figure 4.19: HSIMO level shifters.

is not in the freewheel phase (i.e., $FW =' 0'$) or during the inductor discharging phase (i.e., $HSIMO\_CLK = 0$). While during the freewheel phase (i.e, $FW = 1$), the negative edge of the load comparators outputs (i.e., negative edge of ld_needs_energy signal) are the H-SIMO clock triggers.

4.5.4 Duty-Cycled Zero Current Detector

The ZCD block shown in Figure 4.21 detects the inductor zero current crossing by comparing the voltage at Vx node to GND. For low inductor values (i.e., 240nH), the ZCD design is challenging as the detector has to operate at very high speed. Fortu-

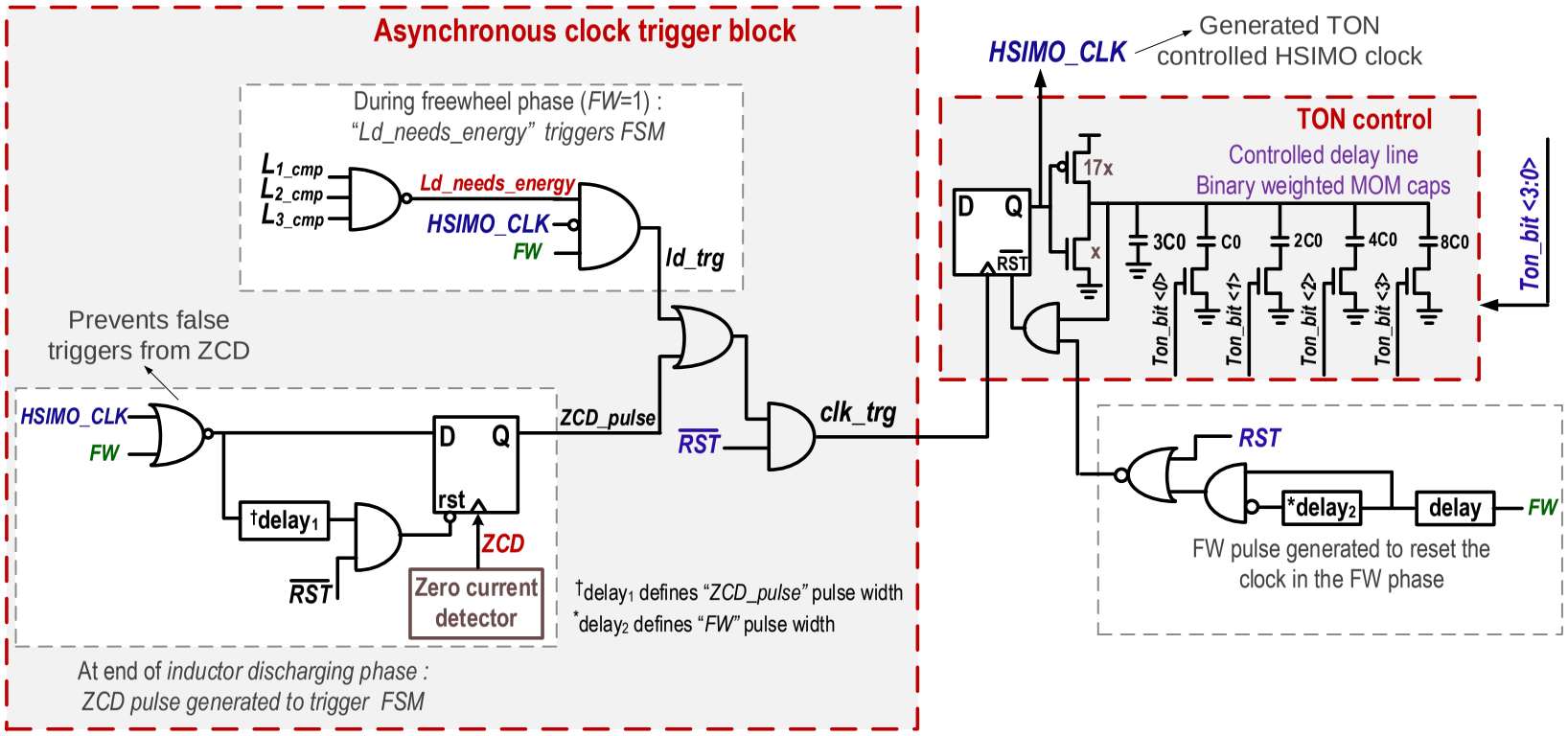

Figure 4.20: Circuit details of HSIMO asynchronous clock generation block and T_{on} control.

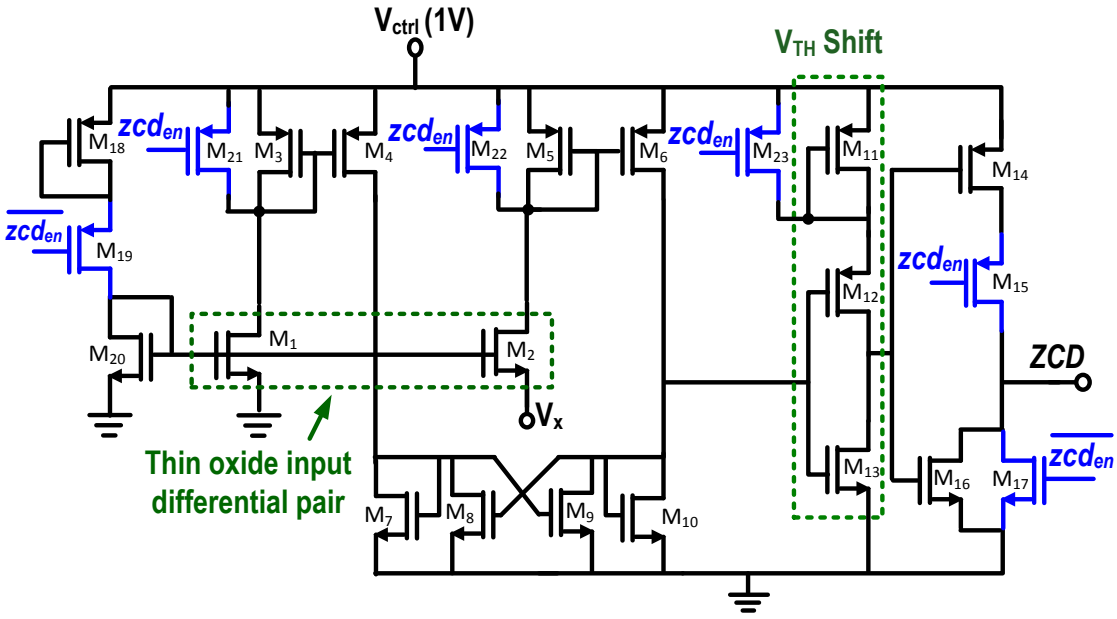

Figure 4.21: Zero current detector.

nately, the voltage at V_x node changes from 0-to-$V_{in}/4$ so the input differential pair can be implemented using common gate thin oxide rather than thick oxide, improving the performance.

The ZCD is a power hungry block, as the detector has to operate at high speed in order to avoid negative inductor current that results in efficiency degradation. To reduce ZCD power, prior work has suggested digital calibration techniques for the inductor discharging time to avoid the need for a power-hungry analog comparator [35]. However, this is not applicable for H-SIMO because the ZCD point changes every inductor switching cycle due to the multiple load regulation. Thus, an analog ZCD is necessary. Fortunately, it can be noted that zero current detection only needs to occur at the end of the inductor discharging phase. Thus, to save power, the ZCD comparator is duty-cycled to be enabled only during $\phi_{2,4,6,8}$ (i.e., $zcd_{en} =' 1'$), which, importantly, is much smaller than ϕ_{FW} at low load currents. Once the ZCD output triggers the end of $\phi_{2,4,6,8}$, it is turned off the rest of the switching cycle, making the ZCD power consumption negligible.

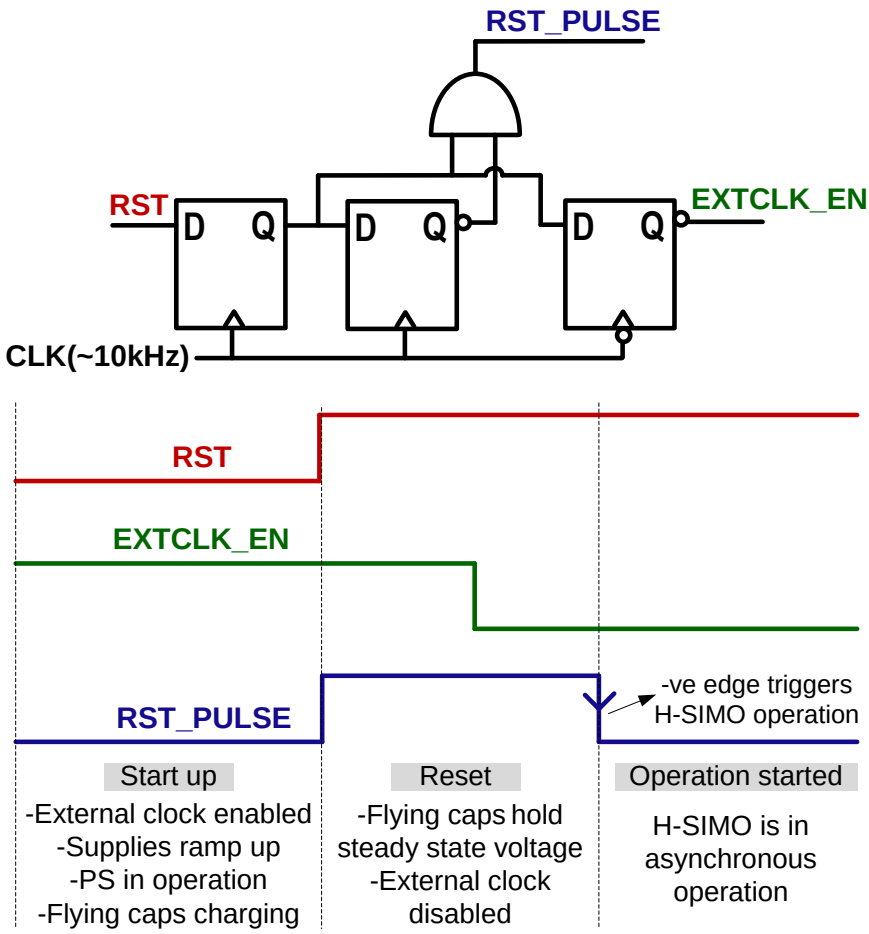

Figure 4.22: H-SIMO startup sequence, the two signals: $EXTCLK\_EN$ and RST_PULSE are generated to setup the startup sequence.

4.6 Startup

As mentioned earlier in Section 4.4.1, H-SIMO controller doesn't require external clock except at startup. A slow clock ($\sim 10kHz$) is required during supplies ramp up at startup to charge the flying capacitors. After that, the H-SIMO is self-clocked. Figure 4.22 shows the startup sequence. There are three different modes: startup, reset mode, operation. Figure 4.22 shows the digital circuits generating the two signals: $EXTCLK\_EN$ and RST_PULSE necessary to trigger the different startup sequence.

Starting up the stacked thin-oxide H-SIMO power stage is critical and if it is not planned properly, the high Li-ion input voltage can break the 1V-thin-oxide tran-

sistors. Initially, the voltage across all the flying capacitors equals to zero. Hence, the power stage input voltage, V_{in}, has to be limited to the maximum transistors voltage rating in order not to break the top switch (i.e., $V_{in} =' 1.05V'$). Therefore, initially H-SIMO power stage operates in sub-threshold, where the power switches switch at 0.25V ($V_{in}/4 =' 0.25V'$) until the flying capacitor charge up and the supplies could be ramped up to higher voltage up to 4.2V. The three flying capacitors C_{f1}, C_{f2}, and C_{f3} reach the steady state voltage $3V_{in}/4$, $V_{in}/2$, and $V_{in}/4$, respectively in the startup mode. One of the main advantages of utilizing the 1V-thin-oxide transistors in the power train is the possibility of enabling sub-threshold operation at startup. The alternative solution would be replacing the top switch with thick-oxide that would degrade the efficiency.

Once the RST signal asserted, The H-SIMO is in reset mode for one clock period and the three flying capacitors hold the steady state voltage. During the reset mode, the $EXTCLK\_EN$ signal de-asserted and the external clock is disabled. At the end of the reset mode, the negative edge of RST_PULSE triggers H-SIMO operation.

4.7 Experimental Results

H-SIMO test-chip taped out in April 2018 and the chip recieved a week before the thesis was due so measurement results in this section are just preliminary results.

The proposed H-SIMO converter is implemented in $0.42mm^2$ in 28nm FDSOI. A die micrograph is shown in Fig. 4.23. Fig. 4.24 demonstrates correct operation of H-SIMO by verifying the voltage at the internal switching nodes of the power stage during startup. Measurement in Fig. 4.25 shows a load-step response measurement and cross regulation test at V_{in}=4.2V. Here, a load step is applied on one of the rails, and the measurement results demonstrate independent voltage regulation across the three loads with only 30mV ripple and negligible droop. This measurement figure also demonstrates the H-SIMO PFM control .

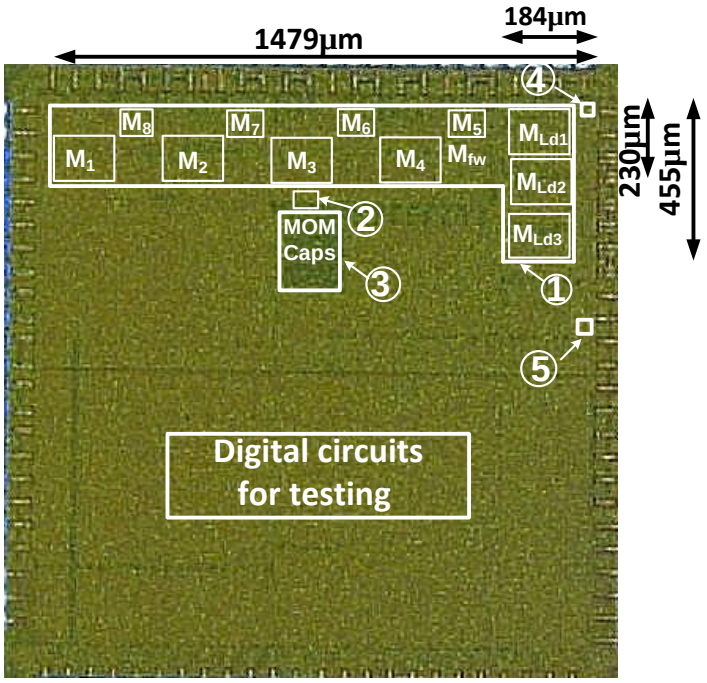

Figure 4.23: H-SIMO Test-chip.

4.8 Conclusion

This chapter presented a miniaturized hybrid single-inductor multiple-output (H-SIMO) power management unit in 28nm FDSOI. H-SIMO converter independently regulates three different power rails while combining the hybrid architecture benefits. The proposed H-SIMO utilized the 28nm 1V-thin-oxide transistor to build the 5-level converter, reducing the switching frequency by up to 76× for an up to 21.5% efficiency improvement. As a result, the proposed H-SIMO eliminates the need for a bulky off-chip inductor, reducing the area of the required off-chip passives by 12.55× and thickness by 3×.

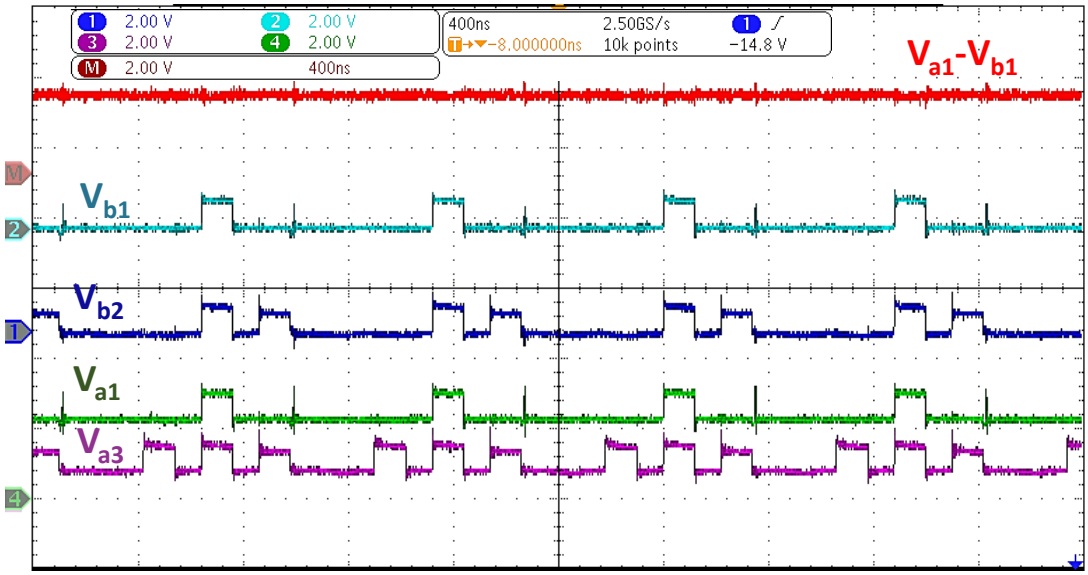

Figure 4.24: Measured voltage at the flying capacitors nodes.

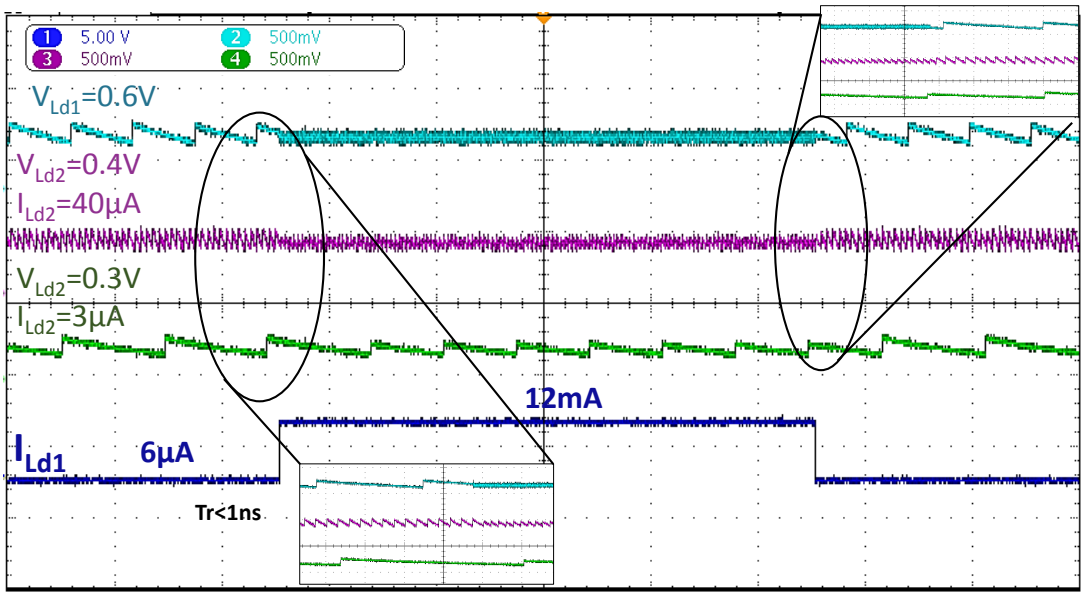

Figure 4.25: Measured load step demonstrating independent voltage regulation across all three loads and negligible droop.

Chapter 5

Conclusion

Advances in wearable sensors technology, portable devices and Internet of things (IoT) put a huge emphasis on building efficient power management unit with small form-factor. This thesis presented energy harvesting and Li-ion compatible power management solutions that meets the needs of next-generation IoT devices in 28nm FDSOI.

The first project in Chapter 2 presented a power management unit that meets the need of small-form-factor net-zero-energy systems by aggregating the maximum available power from three different energy sources while simultaneously regulating three output power rails over a wide dynamic load range, while also managing the charging and discharging of a battery, all in a single-stage single-inductor converter. The proposed architecture uses hysteresis control to regulate the voltage of each harvester at their respective maximum power points (MPP) using pulse frequency modulation (PFM) and adaptive inductor ON time, all via a low-power event-driven controller. The converter, fabricated in 28nm FDSOI, achieves a peak efficiency of 89%, and supports an output power range from 1μW to 60mW, with efficiency >75% at $V_{out} = 1V$, and >69% at $V_{out} = 0.6 - 0.9V$, all with a quiescent power of only 262nW.

The second project in Chapter 3 presented a Li-ion compatible fully-integrated hybrid DC-DC converter implemented in 28nm FDSOI. A modified 4-level converter is proposed to achieve high efficiency while operating from the 2.8-4.2V Li-ion battery range by using stacked 1.5V-transistors. The proposed driver architecture exploits the internal nodes of the power stage as power/gnd rails for drivers, eliminating the need for dedicated power rails, level shifters, or stacked drivers. The proposed converter operates in discontinuous conduction mode (DCM) and regulates the output with constant

ON-time pulse-frequency modulation (PFM), to achieve high efficiency across low load range suitable for wearable/IoT applications. The fabricated chip regulates a 0.6-1.2V output from a 2.8-4.2V input voltage over an output power range from $10\mu W$ to $40mW$ with 78% peak efficiency, and switching frequency up to 200MHz. The converter occupies 1.5mm^2 of on-die area including a pair of 5nF flying capacitors and a 3nH inductor.

The third project in Chapter 4 presented a miniaturized self-clocked Li-ion-compatible hybrid single-inductor multiple-output power management uni that simultaneously regulates three different output loads. using small footprint off-chip passives. The proposed converter utilized the 28nm 1V-transistors to build up the 5-level converter, reducing the switching frequency by up to 76$\times$ for an up to 21.5% efficiency improvement. Thereby, eliminating the need for bulky inductor, reducing the area of the required off-chip passives by 12.55$\times$ and thickness by 3$\times$. The hybrid single-inductor multiple-output converter fabricated in 28nm FDSOI.

Appendix A

Evaluation of the Possible Number of Levels and Multilevel Configurations for N Capacitors

A.1 $N + 2$ Levels for N Capacitors

The conventional way of building multilevel converter is adding flying capacitor to the internal node of the 2-level buck power train and adding power switches to the top and the bottom of the power train. For every additional level, one power switch is added to the top and one is added to the bottom and additional capacitor is connected to the internal nodes. Figure A.1 shows a general topology for N capacitors multilevel with $2N + 2$ switches. This simple way of converting 2-level buck to multilevel results in $N + 2$ level converter for N flying capacitors.

A.2 $2^N + 1$ Levels for N Capacitors

Although the conventional way of realizing multilevel topologies, described in Section A.1 can result in small number of switches and efficient topologies in some cases, specifically scaled-CMOS Li-ion compatible converters but the number of levels is proportional to the number of capacitors (i.e., $N + 2$). As a result, more capacitors and larger area are required to build a multilevel converter with larger number of levels.

The objective of this section is to realize all the possible number of levels for a given number of capacitors, N. The topologies resulted from this realization are not nec-

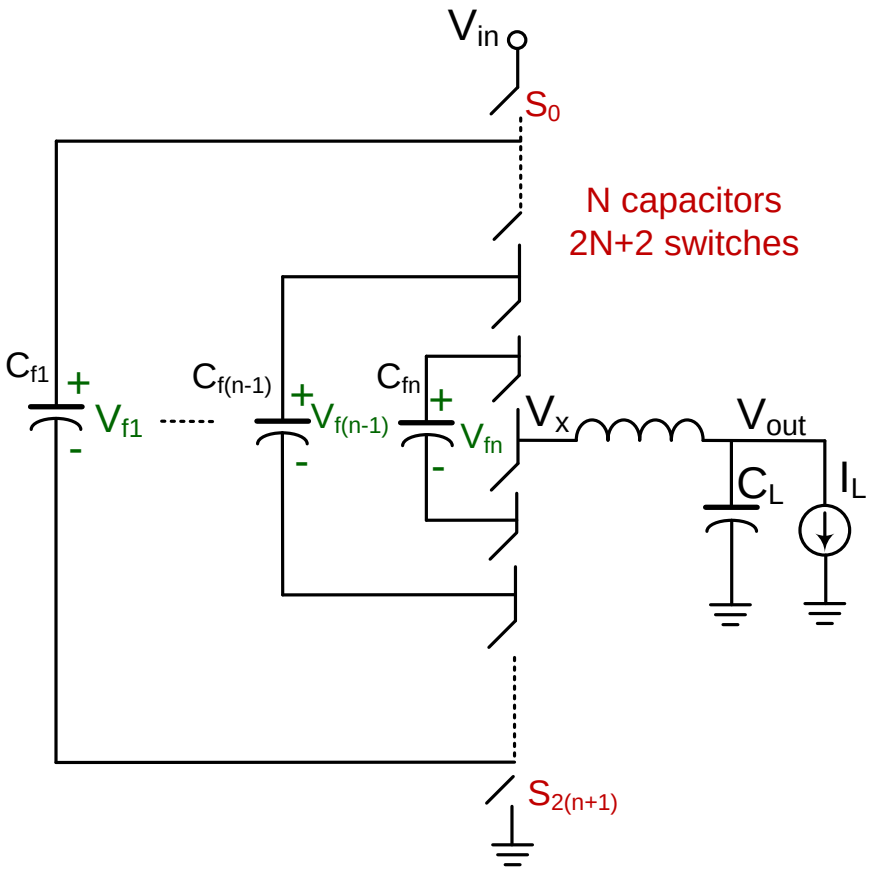

Figure A.1: Conventional way of converting buck to multilevel.

essarily efficient topologies but could be useful if area is a big concern. As an example, in Chapter 3, a modified 4-level converter was proposed to achieve higher power density than the conventional 4-level converter for same area if passives are implemented on-chip.

For N flying capacitors, there are $3^N - 1$ possible capacitor states; each flying capacitor is charging or discharging or not connected (NC). To support all the possible flying capacitors states, for every additional level, two power switches added to the top and the bottom of the power train and a flying capacitor, and two cross-switches are connected to the internal nodes. Figure A.2 shows a general topology for N capacitors multilevel that can support all the possible capacitors states with $4N$ switches. Different flying capacitor states can be represented by $M = 3^N - 1$ KVL equations in the

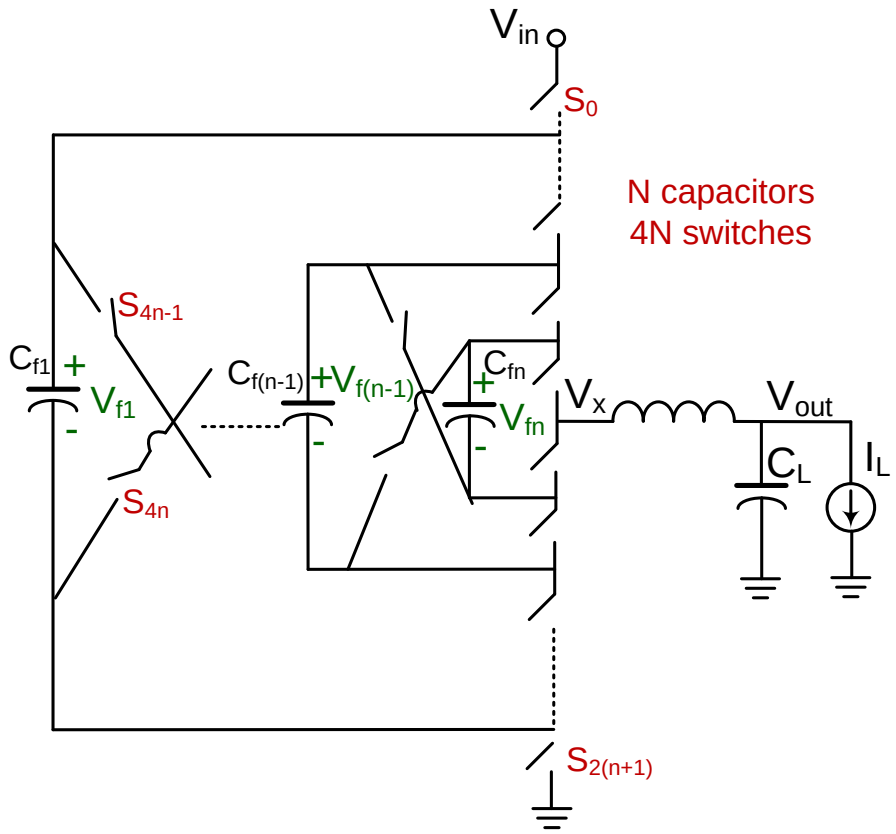

Figure A.2: General multilevel topology with N capacitors and $4N$ switches.

following form:

$$a_{in,i}V_{in} + a_{x,i}V_x + \sum_{j=1}^{N} a_{x,i}a_{fj,i}V_{fj} = 0 \tag{A.1}$$

Where the input voltage coefficient, $a_{in,i}$, the V_x coefficient, $a_{x,i}$, and the fly capacitor coefficient, $a_{fj,i}$, for the steady state equation $i = 1..M$ are defined in (A.2), (A.3), and (A.4), respectively.

$$a_{in,i} = \begin{cases} 1 & V_{in} \text{ connected;} \\ 0 & V_{in} \text{ not connected.} \end{cases} \tag{A.2}$$

$$a_{x,i} = \begin{cases} -1 & V_{in} \text{ connected;} \\ 1 & V_{in} \text{ not connected.} \end{cases} \tag{A.3}$$

$$a_{fj,i} = \begin{cases} 1 & \uparrow C_{fj,i}\ ; \\ -1 & \downarrow C_{fj,i}\ ; \\ 0 & NC\ C_{fj,i} \end{cases} \tag{A.4}$$

The M KVL steady state equations for N flying capacitors can be represented by $M \times (N+2)$ multiplied by $(N+2) \times 1$ matrix as follows:

$$\begin{bmatrix} a_{in,1} & a_{x,1} & a_{x,1}a_{f_{1,1}} & . & a_{x,1}a_{f_{N,1}} \\ a_{in,2} & a_{x,2} & a_{x,2}a_{f_{1,2}} & . & a_{x,2}a_{f_{N,2}} \\ a_{in,3} & a_{x,3} & a_{x,3}a_{f_{1,3}} & . & a_{x,3}a_{f_{N,3}} \\ . & . & . & . & \ddots \\ a_{in,_M} & a_{x,_M} & a_{x,_M}a_{f_{1,M}} & . & a_{x,_M}a_{f_{N,M}} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_x \\ V_{f_1} \\ \ddots \\ V_{f_N} \end{bmatrix} = 0 \tag{A.5}$$

By solving different combinations of M KVL steady state equations (i.e., $N+1$ out of M equations at a time), the voltage at node V_x and the voltage across the flying capacitors can be computed for different switching phases. As a result, the different configurations for all possible number of levels can be deduced along with the corresponding switching phases.

Two Capacitors Multilevel

Figure A.3 shows a general topology for a 2-capacitors multilevel converter with $4N = 8$ switches. For two capacitors, there are $3^N - 1 = 8$ possible flying capacitor states, which can be represented by eight KVL steady state equations by substituting in (A.5). The eight KVL steady state equations for two flying capacitors can be represented by 8×4 multiplied by 4×1 matrix by substituting in (A.2), (A.4), (A.3), and (A.5) as follows:

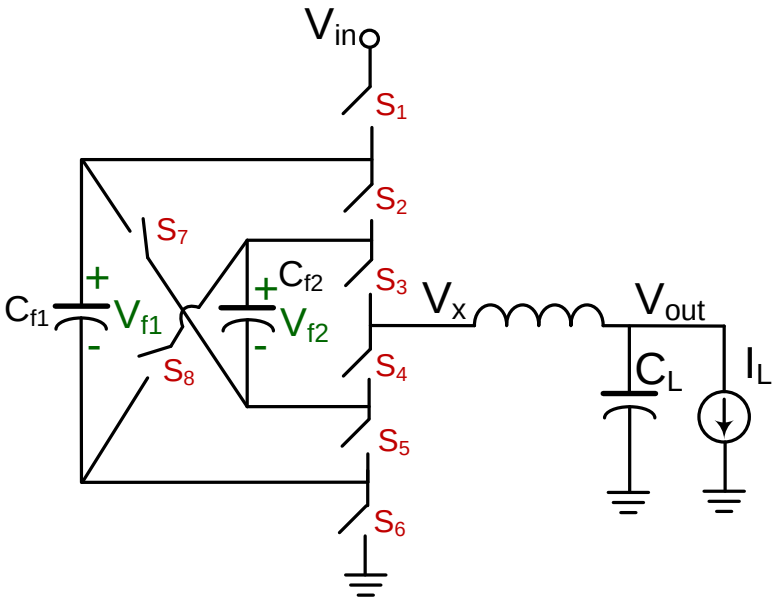

Figure A.3: Two capacitors multilevel topology.

$$\begin{bmatrix} 1 & -1 & -1 & 0 \\ 1 & -1 & 0 & -1 \\ 0 & 1 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 1 & -1 & -1 & 1 \\ 0 & 1 & -1 & 1 \\ 1 & -1 & -1 & -1 \\ 0 & 1 & -1 & -1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_x \\ V_{f_1} \\ V_{f_2} \end{bmatrix} = 0 \tag{A.6}$$

For two capacitors multilevel topology, the maximum possible number of levels and the different possible configurations can be computed by solving the following KVL equations (resulted from matrix in (A.6)):

$$\uparrow C_{f1} \Rightarrow V_{in} - V_x - V_{f1} = 0 \tag{A.7}$$

$$\uparrow C_{f2} \Rightarrow V_{in} - V_x - V_{f2} = 0 \tag{A.8}$$

$$\downarrow C_{f1} \Rightarrow V_x - V_{f1} = 0 \tag{A.9}$$

$$\downarrow C_{f2} \Rightarrow V_x - V_{f2} = 0 \tag{A.10}$$

$$\uparrow C_{f1} \downarrow C_{f2} \Rightarrow V_{in} - V_x - V_{f1} + V_{f2} = 0 \tag{A.11}$$

$$\downarrow C_{f1} \uparrow C_{f2} \Rightarrow V_x - V_{f1} + V_{f2} = 0 \tag{A.12}$$

$$\uparrow C_{f1} \uparrow C_{f2} \Rightarrow V_{in} - V_x - V_{f1} - V_{f2} = 0 \tag{A.13}$$

$$\downarrow C_{f1} \downarrow C_{f2} \Rightarrow V_x - V_{f1} - V_{f2} = 0 \tag{A.14}$$

Matlab script used to solve the different combinations of steady state equations in (A.7) to (A.14) using function $nchoosek(n, k)$, which returns $n!/k!(n-k)!$ different combinations, where n is the number of steady state equations (i.e., $3^N - 1$) and k is the number of variables (i.e., $N + 1$). The number of steady state equations describing a 2-capacitors topology are 8 and the number of variables are 3, specifically V_x, V_{f1}, and V_{f2}. Table A.1 details all possible switching phases for a 2-capacitors multilevel converter including the flying capacitors state along with the corresponding KVL equation and ON switches.

Matlab script computed the steady state voltages: V_x, V_{f1}, and V_{f2} and reported the corresponding three steady state equations for each switching phase, as shown in Figue A.4. Table A.2 summarizes the possible configurations and number of levels for a 2-capacitors multilevel converter based on a Matlab script output. The 2-capacitors multilevel converter can be configured as a 3-level, 4-level, and 5-level converter. Table A.2 shows the two possible configurations of 4-level converters described in details in Chapter 3. While the conventional way to convert buck to multilevel described in Section A.1 result in up to 4-level for 2-capacitors topology, this methodology that allows all the capacitors states shows that 2-capacitors can enable up to 5-level converter.

Table A.1: All possible switching phases for two capacitors multilevel.

State index no	Capacitors state	Equation	ON Switches
1	$C_{f1}\uparrow$	V_{in}-V_x-V_{f1}=0	$S_{1,4,5}$
2	$C_{f2}\uparrow$	V_{in}-V_x-V_{f2}=0	$S_{1,2,4}$
3	$C_{f1}\downarrow$	V_x-V_{f1}=0	$S_{2,3,6}$
4	$C_{f2}\downarrow$	V_x-V_{f2}=0	$S_{3,5,6}$
5	$C_{f1}\uparrow C_{f2}\downarrow$	V_{in}-V_{f1}+V_{f2}-V_x=0	$S_{1,3,5}$
6	$C_{f1}\downarrow C_{f2}\uparrow$	V_x+V_{f2}-V_{f1}=0	$S_{2,4,6}$
7	$C_{f1}\uparrow C_{f2}\uparrow$	V_{in}-V_x-V_{f1}-V_{f2}=0	$S_{1,4,8}$
8	$C_{f1}\downarrow C_{f2}\downarrow$	V_x-V_{f1}-V_{f2}=0	$S_{3,6,7}$
9	No change	V_{in}-V_x=0	$S_{1,2,3}$
10	No change	V_x=0	$S_{4,5,6}$

Three Capacitors Multilevel

The same methodology applied for 3-capacitors multilevel converter to find the possible number of levels and configurations. Figure A.5 shows a general topology for a 3-capacitors multilevel converter with $4N = 12$ switches. For three capacitors, there are $3^N - 1 = 26$ possible flying capacitor states, which can be represented by 26 KVL steady state equations by substituting in (A.5). The 26 KVL steady state equations for three flying capacitors can be represented by 26×5 multiplied by 5×1 matrix by substituting in (A.2), (A.4), (A.3), and (A.5).

Table A.3 lists all the possible switching phases for a 3-capacitors multilevel converter including the flying capacitors state along with the corresponding KVL equation and ON switches. A Matlab script computed the steady state voltages: V_x, V_{f1}, V_{f2}, and V_{f3} and reported the corresponding four steady state equations for each configuration. For a 3-capacitors multilevel converter, there

Table A.4 summarizes some of the possible configurations and number of levels that could be implemented for a 3-capacitors multilevel converter based on a Matlab script output. For the same number of levels, there are many possible configurations

```
 vf1 | vf2 | vx | states
-------------------------
[ 1/2, 1/2, 1/2, 1, 2, 3]
[ 1/2, 1/2, 1/2, 1, 2, 4]
[ 1/3, 1/3, 2/3, 1, 2, 8]
[ 1/2, 1/2, 1/2, 1, 3, 4]
[ 2/3, 1/3, 1/3, 1, 4, 6]
[ 1/2, 1/2, 1/2, 2, 3, 4]
[ 2/3, 1/3, 2/3, 2, 3, 5]
[ 1/2, 1/4, 3/4, 2, 5, 8]
[ 1/3, 1/3, 1/3, 3, 4, 7]
[ 1/2, 1/4, 1/4, 4, 6, 7]
```

Figure A.4: Matlab workspace results.

reported by the Matlab and the choice is based on the designer to optimize efficiency. Other than 3-level and 4-level, the 3-capacitors multilevel converter can be configured as 5-level, 6-level, 7-level, 8-level and 9-level converter. The 5-level converter described in details in Chapter 4 is shown in Table A.4 and it is also realized from the conventional way of converting buck into multilevel, described in Section A.1.

While the conventional way of converting buck to multilevel described in Section A.1 results in up to 5-level for 3-capacitors topology, this methodology that allows all the capacitors states shows that 3-capacitors can enable up to 9-level converter.

Table A.2: The number of levels and possible configurations for a reconfigurable 2-capacitors multilevel converter.

		Capacitor states	V_{f1}	V_{f2}	V_x	
3-Level		10	$V_{in}/2$	$V_{in}/2$	0	Level 1
		1,2,3,4	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	Level 2
		9	$V_{in}/2$	$V_{in}/2$	V_{in}	Level 3
4-Level	**Configuration 1**	10	$2V_{in}/3$	$V_{in}/3$	0	Level 1
		1,4,6	$2V_{in}/3$	$V_{in}/3$	$V_{in}/3$	Level 2
		2,3,5	$2V_{in}/3$	$V_{in}/3$	$2V_{in}/3$	Level 3
		9	$2V_{in}/3$	$V_{in}/3$	V_{in}	Level 4
	Configuration 2	10	$V_{in}/3$	$V_{in}/3$	0	Level 1
		3,4,7	$V_{in}/3$	$V_{in}/3$	$V_{in}/3$	Level 2
		1,2,8	$V_{in}/3$	$V_{in}/3$	$2V_{in}/3$	Level 3
		9	$V_{in}/3$	$V_{in}/3$	V_{in}	Level 4
5-Level		10	$V_{in}/2$	$V_{in}/4$	0	Level 1
		4,6,7	$V_{in}/2$	$V_{in}/4$	$V_{in}/4$	Level 2
		2,4	$V_{in}/2$	$V_{in}/4$	$V_{in}/2$	Level 3
		2,5,8	$V_{in}/2$	$V_{in}/4$	$3V_{in}/4$	Level 4
		9	$V_{in}/2$	$V_{in}/4$	V_{in}	Level 5

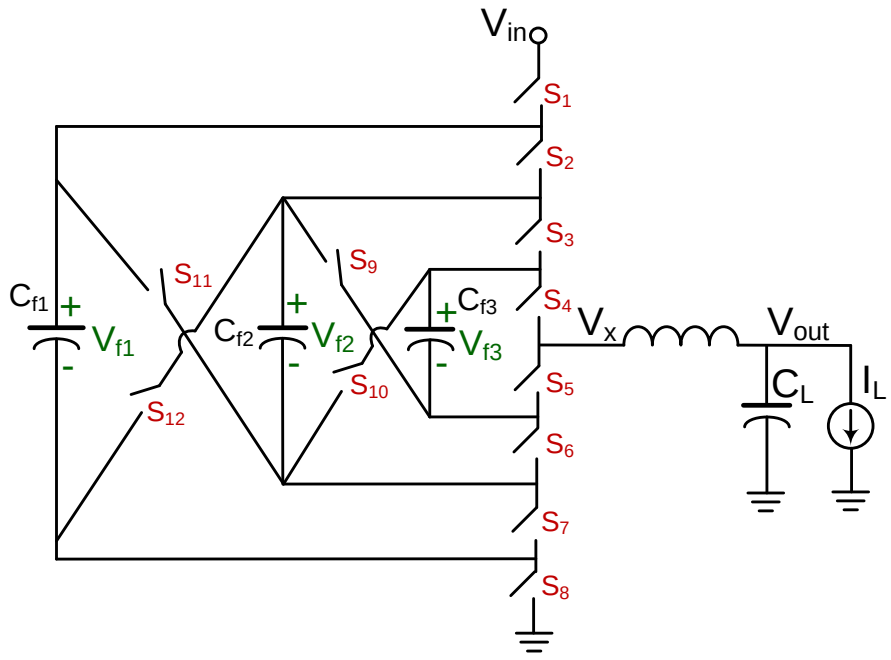

Figure A.5: Three capacitors multilevel topology.

Table A.3: All possible switching phases for three capacitors multilevel.

State index no	Capacitors state	Equation	ON Switches
1	$C_{f1}\uparrow$	$V_{in}-V_x-V_{f1}=0$	$S_{1,5,6,7}$
2	$C_{f2}\uparrow$	$V_{in}-V_x-V_{f2}=0$	$S_{1,2,5,6}$
3	$C_{f1}\downarrow$	$V_x-V_{f1}=0$	$S_{2,3,4,8}$
4	$C_{f2}\downarrow$	$V_x-V_{f2}=0$	$S_{3,4,7,8}$
5	$C_{f1}\uparrow C_{f2}\downarrow$	$V_{in}-V_{f1}+V_{f2}-V_x=0$	$S_{1,3,4,7}$
6	$C_{f1}\downarrow C_{f2}\uparrow$	$V_x+V_{f2}-V_{f1}=0$	$S_{2,5,6,8}$
7	$C_{f1}\uparrow C_{f2}\uparrow$	$V_{in}-V_x-V_{f1}-V_{f2}=0$	$S_{1,5,6,12}$
8	$C_{f1}\downarrow C_{f2}\downarrow$	$V_x-V_{f1}-V_{f2}=0$	$S_{5,8,9,11}$
9	$C_{f3}\uparrow$	$V_{in}-V_x-V_{f3}=0$	$S_{1,2,3,5}$
10	$C_{f3}\downarrow$	$V_x-V_{f3}=0$	$S_{4,6,7,8}$
11	$C_{f1}\uparrow C_{f2}\downarrow C_{f3}\uparrow$	$V_{in}-V_{f1}+V_{f2}-V_{f3}-V_x=0$	$S_{1,3,5,7}$
12	$C_{f1}\downarrow C_{f2}\uparrow C_{f3}\uparrow$	$V_x+V_{f1}-V_{f2}-V_{f3}=0$	$S_{2,5,8,10}$
13	$C_{f1}\uparrow C_{f2}\uparrow C_{f3}\uparrow$	$V_{in}-V_{f1}-V_{f2}-V_{f3}-V_x=0$	$S_{1,5,10,12}$
14	$C_{f1}\downarrow C_{f2}\downarrow C_{f3}\uparrow$	$V_x+V_{f1}+V_{f2}-V_{f3}=0$	$S_{3,5,8,11}$
15	$C_{f1}\uparrow C_{f2}\downarrow C_{f3}\downarrow$	$V_{in}-V_{f1}+V_{f2}+V_{f3}-V_x=0$	$S_{1,4,7,9}$
16	$C_{f1}\downarrow C_{f2}\uparrow C_{f3}\downarrow$	$V_x+V_{f1}-V_{f2}+V_{f3}=0$	$S_{2,4,6,8}$
17	$C_{f1}\uparrow C_{f2}\uparrow C_{f3}\downarrow$	$V_{in}-V_{f1}-V_{f2}+V_{f3}-V_x=0$	$S_{1,4,6,12}$
18	$C_{f1}\downarrow C_{f2}\downarrow C_{f3}\downarrow$	$V_x+V_{f1}+V_{f2}+V_{f3}=0$	$S_{4,8,9,11}$
19	$C_{f1}\uparrow C_{f3}\downarrow$	$V_{in}-V_{f1}+V_{f3}-V_x=0$	$S_{1,4,6,7}$
20	$C_{f1}\downarrow C_{f3}\uparrow$	$V_x+V_{f3}-V_{f1}=0$	$S_{2,3,5,8}$
21	$C_{f1}\uparrow C_{f3}\uparrow$	$V_{in}-V_x-V_{f1}-V_{f3}=0$	$S_{1,3,5,12}$
22	$C_{f1}\downarrow C_{f3}\downarrow$	$V_x-V_{f1}-V_{f3}=0$	$S_{4,6,8,11}$
23	$C_{f2}\uparrow C_{f3}\downarrow$	$V_{in}-V_{f2}+V_{f3}-V_x=0$	$S_{1,2,4,6}$
24	$C_{f2}\downarrow C_{f3}\uparrow$	$V_x+V_{f3}-V_{f2}=0$	$S_{3,5,7,8}$
25	$C_{f2}\uparrow C_{f3}\uparrow$	$V_{in}-V_x-V_{f2}-V_{f3}=0$	$S_{1,2,5,10}$
26	$C_{f2}\downarrow C_{f3}\downarrow$	$V_x-V_{f2}-V_{f3}=0$	$S_{4,7,8,9}$
27	No change	$V_{in}-V_x=0$	$S_{1,2,3,4}$
28	No change	$V_x=0$	$S_{5,6,7,8}$

Table A.4: The number of levels and possible configurations for a re-configurable 3-capacitors multilevel converter.

		Capacitor states	V_{f1}	V_{f2}	V_{f3}	V_x	
5-Level		28	$3V_{in}/4$	$V_{in}/2$	$V_{in}/4$	0	Level 1
		1,6,10,24	$3V_{in}/4$	$V_{in}/2$	$V_{in}/4$	$V_{in}/4$	Level 2
		2,19,4,20	$3V_{in}/4$	$V_{in}/2$	$V_{in}/4$	$V_{in}/2$	Level 3
		9,23,5,3	$3V_{in}/4$	$V_{in}/2$	$V_{in}/4$	$3V_{in}/4$	Level 4
		27	$3V_{in}/4$	$V_{in}/2$	$V_{in}/4$	V_{in}	Level 5
6-Level		28	$3V_{in}/5$	$2V_{in}/5$	$V_{in}/5$	0	Level 1
		6,10,17,24	$3V_{in}/5$	$2V_{in}/5$	$V_{in}/5$	$V_{in}/5$	Level 2
		1,4,16,20	$3V_{in}/5$	$2V_{in}/5$	$V_{in}/5$	$2V_{in}/5$	Level 3
		2,3,11,19	$3V_{in}/5$	$2V_{in}/5$	$V_{in}/5$	$3V_{in}/5$	Level 4
		5,9,14,22	$3V_{in}/5$	$2V_{in}/5$	$V_{in}/5$	$4V_{in}/5$	Level 5
		27	$3V_{in}/5$	$2V_{in}/5$	$V_{in}/5$	V_{in}	Level 6
7-Level		28	$3V_{in}/6$	$2V_{in}/6$	$V_{in}/6$	0	Level 1
		6,7,10,24	$3V_{in}/6$	$2V_{in}/6$	$V_{in}/6$	$V_{in}/6$	Level 2
		4,16,17,20	$3V_{in}/6$	$2V_{in}/6$	$V_{in}/6$	$2V_{in}/6$	Level 3
		1,3	$3V_{in}/6$	$2V_{in}/6$	$V_{in}/6$	$3V_{in}/6$	Level 4
		2,11,14,19	$3V_{in}/6$	$2V_{in}/6$	$V_{in}/6$	$4V_{in}/6$	Level 5
		5,8,9,23	$3V_{in}/6$	$2V_{in}/6$	$V_{in}/6$	$5V_{in}/6$	Level 6
		27	$3V_{in}/6$	$2V_{in}/6$	$V_{in}/6$	V_{in}	Level 7
8-Level	**Configuration 1**	28	$3V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	0	Level 1
		6,10,13,24	$3V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$V_{in}/7$	Level 2
		4,7,16,20	$3V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$2V_{in}/7$	Level 3
		3, 17, 21, 26	$3V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$3V_{in}/7$	Level 4
		1,14,22,25	$3V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$4V_{in}/7$	Level 5
		2,8,11,19	$3V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$5V_{in}/7$	Level 6
		5,9,18,23	$3V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$6V_{in}/7$	Level 7
		27	$3V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	V_{in}	Level 8
	Configuration 2	28	$4V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	0	Level 1
		7,10,12,24	$4V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$V_{in}/7$	Level 2
		4,6,17,21	$4V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$2V_{in}/7$	Level 3
		1,16,20,26	$4V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$3V_{in}/7$	Level 4
		3,11,19,25	$4V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$4V_{in}/7$	Level 5
		2,5,14,22	$4V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$5V_{in}/7$	Level 6
		8,9,15,23	$4V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	$6V_{in}/7$	Level 7
		27	$4V_{in}/7$	$2V_{in}/7$	$V_{in}/7$	V_{in}	Level 8
9-Level		28	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	0	Level 1
		10,12,13,24	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	$V_{in}/8$	Level 2
		4,6,7	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	$2V_{in}/8$	Level 3
		16,17,20,26	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	$3V_{in}/8$	Level 4
		1,3	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	$4V_{in}/8$	Level 5
		11,14,22,25	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	$5V_{in}/8$	Level 6
		2,8	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	$6V_{in}/8$	Level 7
		9,15,18,23	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	$7V_{in}/8$	Level 8
		27	$4V_{in}/8$	$2V_{in}/8$	$V_{in}/8$	V_{in}	Level 9

Appendix B

Multi-State Reconfigurable Switched Capacitor DC-DC Converters

Dynamic voltage scaling (DVS) is used as an efficient power reduction technique in digital circuits by scaling the voltage supply based on the operating mode to the sub- or near-threshold regions [45]. On-chip DC-DC converters are implemented using linear regulators or switching converters. Linear dropout regulators (LDO) have small cost/size overhead but their efficiency is limited to the ratio of output to input voltage. In contrast, reconfigurable switched capacitor (SC) converters can maintain high efficiency across wide output voltage by enabling multi-ratio configuration modes at the expense of increase in the area and design complexity.

Switched capacitor voltage regulators exhibit its peak efficiency at output voltage, V_{out}, equals to its maximum voltage, $V_{max} = CR.V_{in}$, where CR is the conversion ratio and V_{in} is the input voltage. Reconfigurable SC with multiple conversion ratios can maintain high efficiency across wide range of output voltages [51, 61]. In [61], a four 2:1 power stages cascaded in a recursive way is used to realize 15 conversion ratios. However, this two capacitor states SC needs many capacitors and power transistors to achieve large number of conversion ratios. In [69] and [70], 3-states SC introduced to achieve more conversion ratios using the same number of fly capacitors.

This chapter presents the multi-state reconfigurable SC to realize the maximum conversion ratios without adding flying capacitors or power switches. Figure B.1 shows the expected efficiency of the three flying capacitors binary SC with 8 conversion ratios versus the proposed multi-state reconfigurable SC that yields 23 conversion ratios using

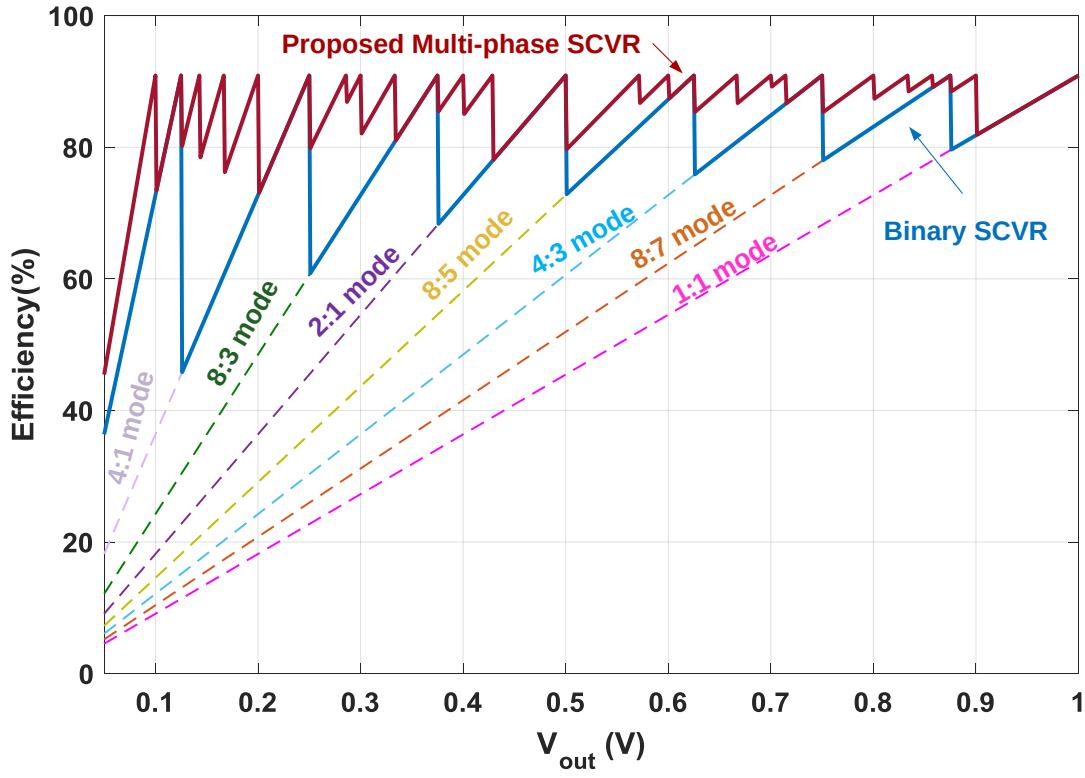

Figure B.1: The expected SC efficiency versus $Vout$ for the binary SC and the proposed multi-state SC with three flying capacitors.

the same number of fly capacitors assuming $R_{out} << R_L$. Simulations of three capacitors multi-state reconfigurable SC with 23 conversion ratios mode on 28nm technology show increase of up to 40% in the efficiency and reduction of up to 87% in the output voltage ripple.

B.1 Reconfigurable Multi-State SC Analysis for N Fly Capacitors

For N capacitors and $4N$ switches, there are $3^N - 1$ possible capacitor states; each capacitor is charging or discharging or not connected (NC). Different capacitor states can be represented by $M = 3^N - 1$ KVL equations in the following form:

$$a_{in,i}V_{in} + a_{o,i}V_{out} + \sum_{j=1}^{N} a_{o,i}a_{fj,i}V_{fj} = 0 \tag{B.1}$$

Where the input voltage coefficient $a_{in,i}$, the output voltage coefficient $a_{o,i}$ and the fly capacitor coefficient $a_{fj,i}$ for the steady state equation $i = 1..M$ are defined in (A.2), (**??**) and (A.4), respectively.

$$a_{in,i} = \begin{cases} 1 & V_{in} \text{ connected;} \\ 0 & V_{in} \text{ not connected.} \end{cases} \tag{B.2}$$

$$a_{o,i} = \begin{cases} -1 & V_{in} \text{ connected;} \\ 1 & V_{in} \text{ not connected.} \end{cases} \tag{B.3}$$

$$a_{fj,i} = \begin{cases} 1 & \uparrow C_{fj,i}\ ; \\ -1 & \downarrow C_{fj,i}\ ; \\ 0 & NC\ C_{fj,i} \end{cases} \tag{B.4}$$

The KVL steady state equations for the multi-state reconfigurable SC with N flying capacitor and $4N$ switches can be represented by the following matrix:

$$\begin{bmatrix} a_{in,1} & a_{o,1} & a_{o,1}a_{f_{1,1}} & . & a_{o,1}a_{f_{N,1}} \\ a_{in,2} & a_{o,2} & a_{o,2}a_{f_{1,2}} & . & a_{o,2}a_{f_{N,2}} \\ a_{in,3} & a_{o,3} & a_{o,3}a_{f_{1,3}} & . & a_{o,3}a_{f_{N,3}} \\ . & . & . & . & \ddots \\ a_{in,M} & a_{o,M} & a_{o,M}a_{f_{1,M}} & . & a_{o,M}a_{f_{N,M}} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \\ V_{f_1} \\ \ddots \\ V_{f_N} \end{bmatrix} = 0 \tag{B.5}$$

The possible conversion ratios for SC with N capacitors can be computed by solving different combinations of steady state equations in (B.5). Accordingly, for each conversion ratio (CR), there are k switching states. The duty cycle of each switching state D_i ($i = 1..k$) can be defined as following:

$$D_i = \frac{t_{\phi,i}}{\sum_{i=1}^{k} t_{\phi,i}} \tag{B.6}$$

where $t_{\phi,i}$ is the pulse width of capacitor state i.

In steady state, the charge conservation on each capacitor can be represented as following:

$$\sum_{i=1}^{k} a_{fj,i} t_{\phi,i} = 0 \tag{B.7}$$

The Energy Conservation law for SC converter $Q_{in}V_{in} = Q_o V_{out}$ yields (B.8) which is simplified in (B.9).

$$\begin{aligned} CR &= Q_{in}/Q_o \\ &= \frac{\sum_{i=1}^{k} a_{in,i} t_{\phi,i}}{\sum_{i=1}^{k} t_{\phi,i}} \end{aligned} \tag{B.8}$$

$$\sum_{i=1}^{k} (a_{in,i} - CR) t_{\phi,i} = 0 \tag{B.9}$$

For a computed CR, The pulse width of each switching state $t_{\phi,i}$ for $i = 1..k$ is computed by solving (B.7) and (B.9). Consequently, the duty cycle of each state D_i is computed from (B.6).

B.2 The Proposed Reconfigurable Multi-State SC

Figure B.2 shows the proposed reconfigurable multi-state power stage which consists of three capacitors and twelve switches. The proposed multi-state SC enables 23 conversion ratio modes. For three capacitors, there are $3^N - 1 = 26$ possible switch-

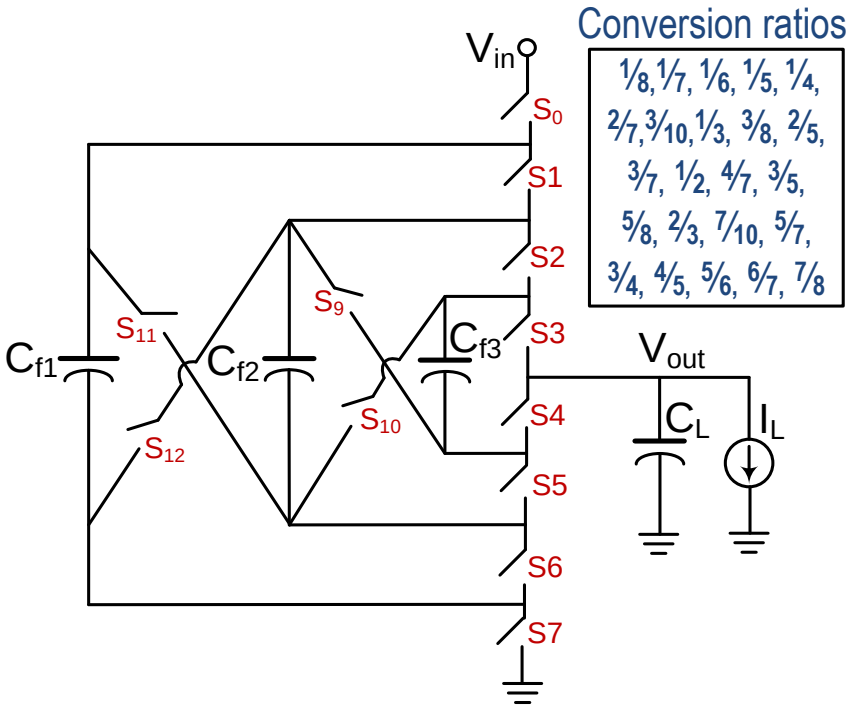

Figure B.2: The three capacitor multiphase Power stage

ing states which can be represented by 26 steady state equations by substituting in (B.5).

Figure B.3 shows the configurations of the 4 different switching states in 3/10 conversion mode as an example and the ON transistors S_i in each state. $CR = 3/10$ is computed by solving the following KVL equations:

$$V_{in} - V_{out} - V_{f1} - V_{f2} - V_{f3} = 0 \tag{B.10}$$

$$V_{out} - V_{f1} + V_{f3} = 0 \tag{B.11}$$

$$V_{out} - V_{f1} + V_{f2} - V_{f3} = 0 \tag{B.12}$$

$$V_{out} - V_{f2} - V_{f3} = 0 \tag{B.13}$$

The proposed multi-state SC switch between 4 different configurations to result in $CR = 3/10$. Solving (B.10), (B.11), (B.12) and (B.13) result in $V_{f_1} = 2/5$, $V_{f_2} = 1/5$, $V_{f_3} = 1/10$ and $CR = 3/10$. Substituting in (B.7) and (B.9):

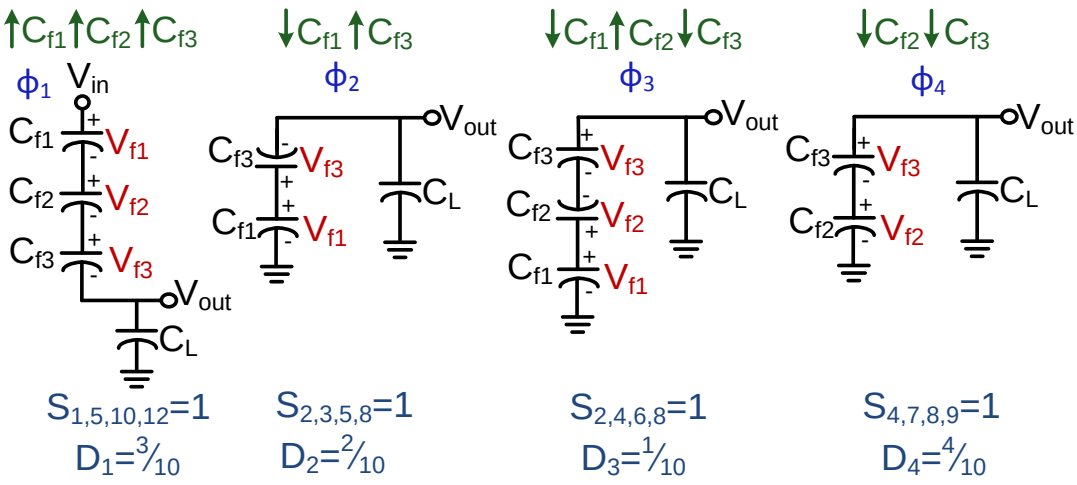

Figure B.3: Different switching states of the proposed SC in 3/10 conversion ratio mode.

$$t_{\phi,1} - t_{\phi,2} - t_{\phi,3} = 0 \tag{B.14}$$

$$t_{\phi,1} + t_{\phi,3} - t_{\phi,4} = 0 \tag{B.15}$$

$$t_{\phi,1} + t_{\phi,2} - t_{\phi,3} - t_{\phi,4} = 0 \tag{B.16}$$

$$0.7t_{\phi,1} - 0.3t_{\phi,2} - 0.3t_{\phi,3} - 0.3t_{\phi,4} = 0 \tag{B.17}$$

Solving (B.14), (B.15), (B.16) and (B.17) result in $t_{\phi,1} = 3$, $t_{\phi,2} = 2$, $t_{\phi,3} = 1$ and $t_{\phi,4} = 4$. The duty cycle of each state is computed by substituting in (B.6) which result in $D_1 = 0.4$, $D_2 = 0.3$, $D_2 = 0.2$ and $D_2 = 0.1$.

The output voltage is regulated around the reference voltage V_{ref} using pulse frequency modulation (PFM). A clocked comparator is used to trigger switching to the next capacitors state when V_{out} goes below V_{ref}. A finite state machine (FSM) is used to generate the appropriate capacitor configuration state based on the comparator output and the SC conversion ratio mode.

Figure B.4 shows the output voltage and the clocked comparator output of the multi-state SC in 3/10 conversion mode. The switching frequency of the output voltage is 4x the converter switching frequency, hence the output voltage ripple is lower than the

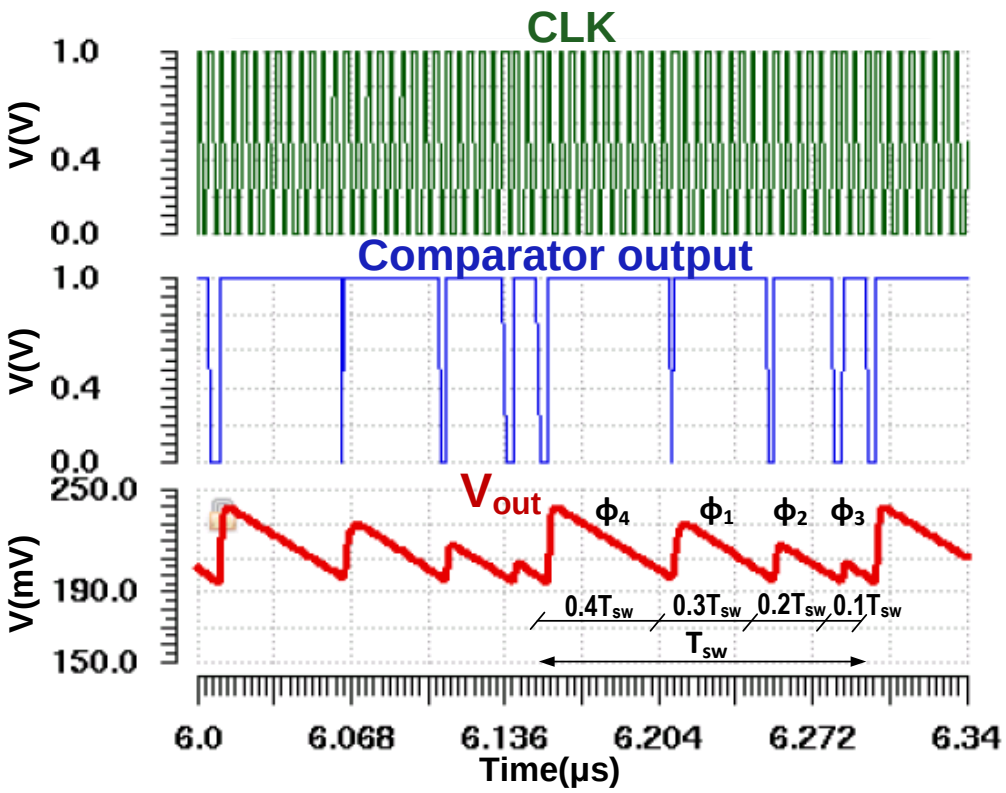

Figure B.4: Simulation results showing the output voltage and the clocked comparator output in 3/10 conversion ratio mode at V_{in}=1V and V_{ref}=200mV.

2-states converter. Figure B.5 shows the flying capacitors different states for $CR = 4/7$ along with their equivalent ON transistors and the duty cycle of each state. Figure B.6 shows the flying capacitors configuration for $CR = 3/4$ and CR=1/2 where the proposed multi-state SC is switching only between 2 states for these conversion ratios.

B.3 Simulation Results

The proposed reconfigurable multi-state SC with 23 different conversion ratio modes simulated on 28nm technology with $C_{f1} = C_{f2} = C_{f3} = 5nF$ and $C_L = 10nF$. Figure B.7 and Figure B.8 show the efficiency and the output voltage ripple, respectively of the binary SC and the proposed multiphase SC for $V_{in} = 2V$ and $I_{Ld} = 10mA$. The proposed SC result in an increase up to 40% in the efficiency and reduction

up to 87% in the output voltage ripple. The voltage ripple is a form of a series loss in the SC converters [50]. A typical binary SC would require more decoupling capacitors or interleaving [50] to meet the ripple specifications.

B.4 Conclusion

A multi-state reconfigurable switched capacitor (SC) that enables more conversion ratios without adding flying capacitors or power switches is presented. General expressions for the maximum number of the possible capacitor states for N capacitors derived along with their equivalent steady state equations. The proposed multi-state reconfigurable SC with three flying capacitors realize 23 conversion ratios and proved to achieve higher efficiency compared to the binary SC which can only realize 7 conversion ratios. Simulations on 28nm CMOS show increase of up to 40% in the efficiency and reduction of up to 87% in the output voltage ripple.

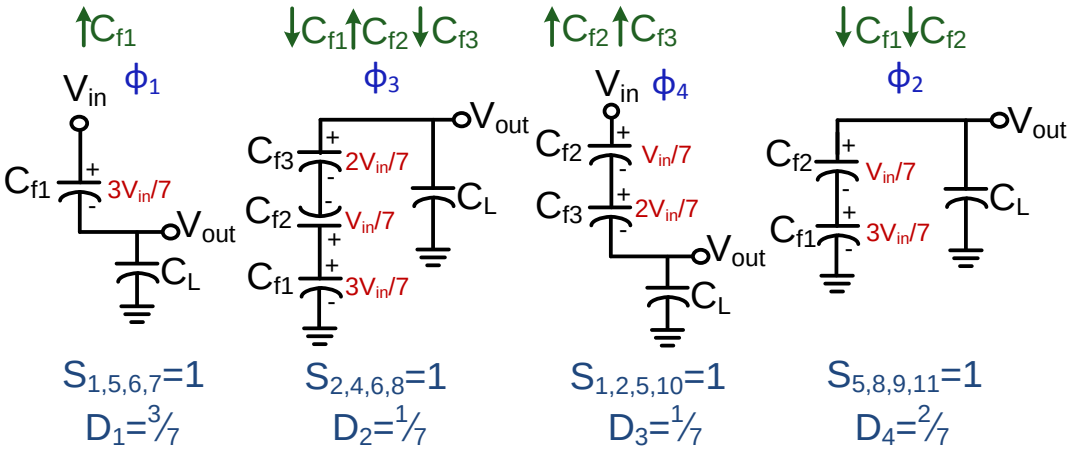

Figure B.5: Different switching states of the proposed SC in 4/7 conversion ratio mode.

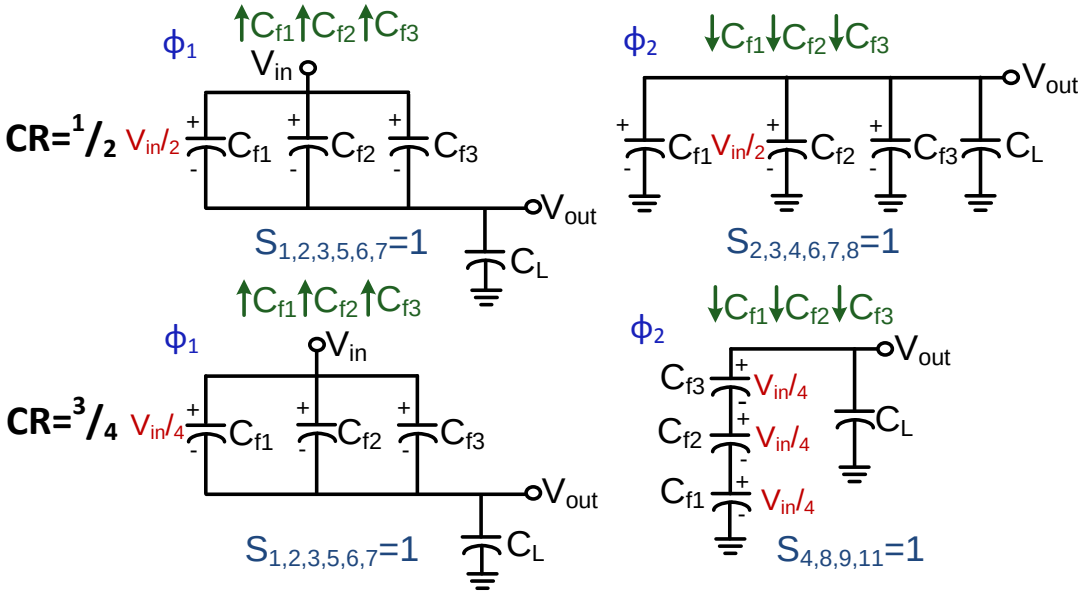

Figure B.6: Proposed multi-state SC in 3/4 and 1/2 conversion ratio modes switching between 2 states only with duty cycle 50%

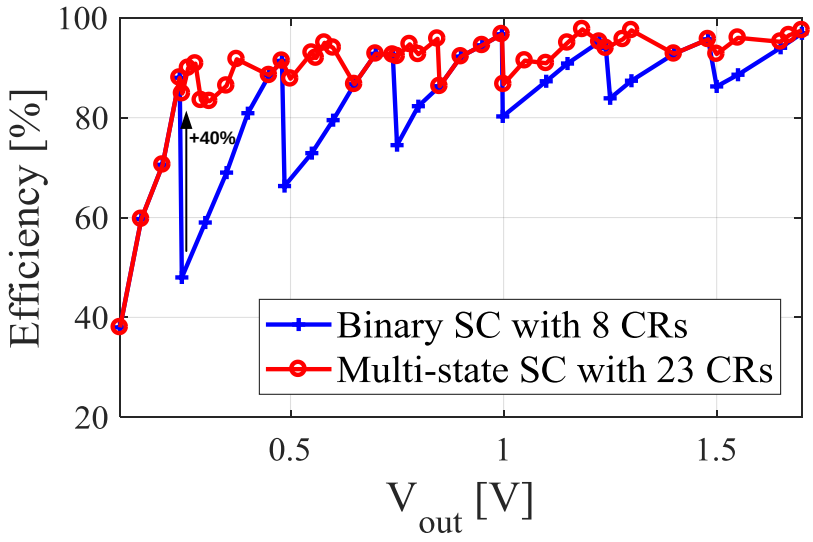

Figure B.7: Simulation results of the overall conversion efficiency of the conventional binary SC and the proposed multi-state SC

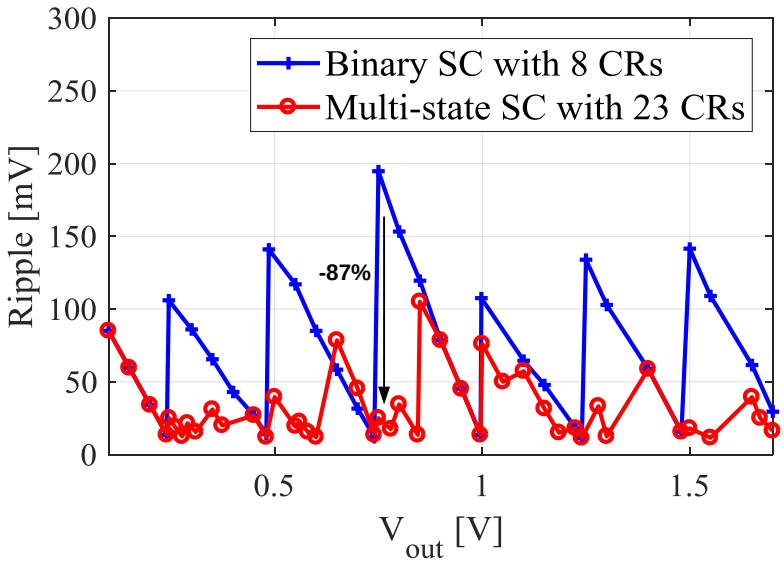

Figure B.8: Simulation results of the output ripple of the conventional binary SC and the proposed multi-state SC

References

[1] A. Bandodkar, W. Jia, and J. Wang, "Tattoo-based wearable electrochemical devices: A review," *Electroanalysis*, vol. 27, Jan 2015.

[2] A. Podsiadlo, "Anti-kidnap child protection provided by small wearable devices," *IoT News, Press Release*, April 2015.

[3] J. Kim, S. Imani, W. R. de Araujo, J. Warchall, G. Valds-Ramrez, T. R. Paixo, P. P. Mercier, and J. Wang, "Wearable salivary uric acid mouthguard biosensor with integrated wireless electronics," *Biosensors and Bioelectronics*, vol. 74, pp. 1061 – 1068, Dec 2015.

[4] G. Writer, "IoT applications in agriculture," Jan 2013.

[5] P. Harrop, J. Hayward, and G. Holland, "Wearable technology 2015-2025: Technologies, markets, forecasts," in *IDTechEx Report*, 2015.

[6] C. Alcaraz, P. Najera, J. Lopez, and R. Roman, "Wireless sensor networks and the internet of things: Do we need a complete integration?" in *1st International Workshop on the Security of the Internet of Things*, 2010.

[7] H. Jones, "Whitepaper: Semiconductor industry from 2015 to 2025," Aug 2015.

[8] M. N. Halgamuge, M. Zukerman, K. Ramamohanarao, and H. L. Vu, "An estimation of sensor energy consumption," *Progress In Electromagnetics Research B*, vol. 12, pp. 259–295, 2009.

[9] B. Martinez, M. Montn, I. Vilajosana, and J. D. Prades, "The power of models: Modeling power consumption for iot devices," *IEEE Sensors Journal*, vol. 15, no. 10, pp. 5777–5789, Oct 2015.

[10] D. Blaauw, D. Sylvester, P. Dutta, Y. Lee, I. Lee, S. Bang, Y. Kim, G. Kim, P. Pannuto, Y. . Kuo, D. Yoon, W. Jung, Z. Foo, Y. . Chen, S. Oh, S. Jeong, and M. Choi, "Iot design space challenges: Circuits and systems," in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, June 2014, pp. 1–2.

[11] S. Grady, "Energy harvesting for zero power devices architecture and technology overview," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb 2012.

[12] M. M. Tentzeris, A. Georgiadis, and L. Roselli, "Energy harvesting and scavenging [scanning the issue]," *Proceedings of the IEEE*, vol. 102, no. 11, pp. 1644–1648, Nov 2014.

[13] T. Skotnicki and S. Monfray, "UTBB FDSOI: Evolution and opportunities," in *2015 45th European Solid State Device Research Conference (ESSDERC)*, Sept 2015, pp. 76–79.

[14] E. Beigne, J. Christmann, A. Valentian, O. Billoint, E. Amat, and D. Morche, "UTBB FDSOI technology flexibility for ultra low power internet-of-things applications," in *2015 45th European Solid State Device Research Conference (ESSDERC)*, Sept 2015, pp. 164–167.

[15] G. Foundries, "Fd-soi technology innovations extend moores law," in *Global Foundries White Paper*, September 2015, pp. 1–4.

[16] M. Jurczak, N. Collaert, A. Veloso, T. Hoffmann, and S. Biesemans, "Review of finfet technology," in *2009 IEEE International SOI Conference*, Oct 2009, pp. 1–4.

[17] G. Jacquemod, A. Fonseca, E. de Foucauld, Y. Leduc, and P. Lorenzini, "2.45 GHz 0.8 mW voltage-controlled ring oscillator (VCRO) in 28 nm fully depleted silicon-on-insulator (fdsoi) technology," *Frontiers of Materials Science*, vol. 9, no. 2, pp. 156–162, Jun 2015.

[18] C. Shi, B. Miller, K. Mayaram, and T. Fiez, "A multiple-input boost converter for low-power energy harvesting," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 12, pp. 827–831, Dec 2011.

[19] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sept 2012.

[20] C. L. Chang and T. C. Lee, "A compact multi-input thermoelectric energy harvesting system with 58.5% power conversion efficiency and 32.4mW output power capability," in *International Symposium on Integrated Circuits (ISIC)*, Dec 2014, pp. 1–4.

[21] M. Dini, A. Romani, M. Filippi, V. Bottarel, G. Ricotti, and M. Tartagni, "A nanocurrent power management ic for multiple heterogeneous energy harvesting sources," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5665–5680, Oct 2015.

[22] S. Y. Jung, M. Park, M. Lee, J. Yang, and J. Kim, "Time slot optimization algorithm for multisource energy harvesting systems," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Sept 2016, pp. 499–502.

[23] G. Chowdary, A. Singh, and S. Chatterjee, "An 18nA, 87% efficient solar, vibration and rf energy-harvesting power management system with a single shared inductor," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2501–2513, Oct 2016.

[24] D. Goder and H. Santo, "Multiple output regulator with time sequencing," U.S. Patent 5 617 015, April 1, 1997.

[25] M. W. May, M. R. May, and J. E. Willis, "A synchronous dual-output switching dc-dc converter using multibit noise-shaped switch control," in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Feb 2001, pp. 358–359.

[26] D. Ma, W.-H. Ki, C.-Y. Tsui, and P. K. T. Mok, "Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 89–100, Jan 2003.

[27] C. S. Chae, H. P. Le, K. C. Lee, M. C. Lee, G. H. Cho, and G. H. Cho, "A single-inductor step-up dc-dc switching converter with bipolar outputs for active matrix oled mobile display panels," in *IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Feb 2007, pp. 136–592.

[28] M. H. Huang and K. H. Chen, "Single-inductor multi-output (SIMO) dc-dc converters with high light-load efficiency and minimized cross-regulation for portable devices," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1099–1111, April 2009.

[29] J. Kim, D. S. Kim, and C. Kim, "A single-inductor eight-channel output dc-dc converter with time-limited power distribution control and single shared hysteresis comparator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3354–3367, Dec 2013.

[30] N. J. Guilar, R. Amirtharajah, P. J. Hurst, and S. H. Lewis, "An energy-aware multiple-input power supply with charge recovery for energy harvesting applications," in *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb 2009, pp. 298–299,299a.

[31] Y. K. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35mV startup voltage," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 333–341, Jan 2011.

[32] K. Kadirvel, Y. Ramadass, U. Lyles, J. Carpenter, V. Ivanov, V. McNeil, A. Chandrakasan, and B. Lum-Shue-Chan, "A 330na energy-harvesting charger with battery management for solar and thermoelectric energy harvesting," in *2012 IEEE International Solid-State Circuits Conference*, Feb 2012, pp. 106–108.

[33] S. Uprety and H. Lee, "A 93%-power-efficiency photovoltaic energy harvester with irradiance-aware auto-reconfigurable MPPT scheme achieving >95% MPPT efficiency across 650μW to 1W and 2.9ms FOCV MPPT transient time," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 378–379.

[34] D. El-Damak and A. P. Chandrakasan, "Solar energy harvesting system with integrated battery management and startup using single inductor and 3.2nW quiescent power," in *Symposium on VLSI Circuits (VLSI Circuits)*, June 2015, pp. C280–C281.

[35] H. J. Chen, Y. H. Wang, P. C. Huang, and T. H. Kuo, "An energy-recycling three-switch single-inductor dual-input buck/boost dc-dc converter with 93% peak conversion efficiency and $0.5mm^2$ active area for light energy harvesting," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.

[36] A. Shrivastava, Y. K. Ramadass, S. Khanna, S. Bartling, and B. H. Calhoun, "A 1.2 μW simo energy harvesting and power management unit with constant peak inductor current control achieving 83-92% efficiency across wide input and output voltages," in *Symposium on VLSI Circuits Digest of Technical Papers*, June 2014, pp. 1–2.

[37] G. Yu, K. W. R. Chew, Z. C. Sun, H. Tang, and L. Siek, "A 400nW single-inductor dual-inputtri-output dcdc buckboost converter with maximum power point tracking for indoor photovoltaic energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 11, pp. 2758–2772, Nov 2015.

[38] W. Jia, X. Wang, S. Imani, A. J. Bandodkar, J. Ramirez, P. Mercier, and J. Wang, "Wearable textile biofuel cells for powering electronics," *Journal of Materials Chemistry A*, vol. 2, pp. 18 184–18 189, Sept 2014.

[39] A. Bandodkar, J.-M. You, N.-H. Kim, Y. Gu, R. Kumar, A. M. Mohan, J. Kurniawan, S. Imani, T. Nakagawa, B. Parish, M. Parthasarathy, P. Mercier, S. Xu, and J. Wang, "Soft, stretchable, high power density electronic skin-based biofuel cells for scavenging energy from human sweat," vol. 10, pp. 1581–1589, 2017.

[40] D. Kwon and G. A. Rincon-Mora, "Single-inductor multiple-output switching dc-dc converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 8, pp. 614–618, Aug 2009.

[41] A. A. Abdelmoaty and A. Fayed, "A single-step, single-inductor energy-harvesting based power supply platform with a regulated battery charger for mobile applications," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 666–669.

[42] M. Chen, M. Zhao, Q. Liu, and X. Wu, "Start-up module for low voltage energy harvesting systems," in *2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC)*, Dec 2012, pp. 1–3.

[43] P. Chen, K. Ishida, K. Ikeuchi, X. Zhang, K. Honda, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "Startup techniques for 95 mv step-up converter by capacitor pass-on scheme andv_{th}-tuned oscillator with fixed charge programming," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 5, pp. 1252–1260, May 2012.

[44] A. Das, Y. Gao, and T. T. Kim, "An output feedback-based start-up technique with automatic disabling for battery-less energy harvesters," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 233–236.

[45] T. D. Burd, T. A. Pering, A. J. Stratakos, and R. W. Brodersen, "A dynamic voltage scaled microprocessor system," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 11, pp. 1571–1580, Nov 2000.

[46] H. K. Krishnamurthy, V. A. Vaidya, P. Kumar, G. E. Matthew, S. Weng, B. Thiruvengadam, W. Proefrock, K. Ravichandran, and V. De, "A 500 MHz, 68% efficient, fully on-die digitally controlled buck voltage regulator on 22nm tri-gate CMOS," in *Symposium on VLSI Circuits Digest of Technical Papers*, June 2014, pp. 1–2.

[47] J. Wibben and R. Harjani, "A high-efficiency dc-dc converter using 2 nh integrated inductors," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 844–854, April 2008.

[48] M. Lee, Y. Choi, and J. Kim, "A 500-MHz, 0.76-W/mm power density and 76.2% power efficiency, fully integrated digital buck converter in 65-nm cmos," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3315–3323, July 2016.

[49] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A fully-integrated switched-capacitor step-down dc-dc converter with digital capacitance modulation in 45 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, Dec 2010.

[50] H. P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor dc-dc converters," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sept 2011.

[51] R. Jain, B. M. Geuskens, S. T. Kim, M. M. Khellah, J. Kulkarni, J. W. Tschanz, and V. De, "A 0.45-1V fully-integrated distributed switched capacitor dc-dc converter with high density MIM capacitor in 22nm tri-gate CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, April 2014.

[52] M. Turnquist, M. Hiienkari, J. Mkip, R. Jevtic, E. Pohjalainen, T. Kallio, and L. Koskinen, "Fully integrated dc-dc converter and a 0.4V 32-bit cpu with timing-error prevention supplied from a prototype 1.55V li-ion battery," in *2015 Symposium on VLSI Circuits (VLSI Circuits)*, June 2015, pp. C320–C321.

[53] T. Souvignet, B. Allard, and S. Trochut, "A fully integrated switched-capacitor regulator with frequency modulation control in 28-nm fdsoi," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4984–4994, July 2016.

[54] W. Kim, D. Brooks, and G. Y. Wei, "A fully-integrated 3-level dc-dc converter for nanosecond-scale DVFS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan 2012.

[55] P. Kumar, V. A. Vaidya, H. Krishnamurthy, S. Kim, G. E. Matthew, S. Weng, B. Thiruvengadam, W. Proefrock, K. Ravichandran, and V. De, "A 0.4V-1V 0.2A/mm^2 70% efficient 500MHz fully integrated digitally controlled 3-level buck voltage regulator with on-die high density MIM capacitor in 22nm tri-gate CMOS," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sept 2015, pp. 1–4.

[56] T. M. V. Breussegem and M. S. J. Steyaert, "Monolithic capacitive dc-dc converter with single boundary multiphase control and voltage domain stacking in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1715–1727, July 2011.

[57] H. P. Le, J. Crossley, S. R. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm^2 at 73% efficiency," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb 2013, pp. 372–373.

[58] S. Bang, D. Blaauw, and D. Sylvester, "A successive-approximation switched-capacitor dc-dc converter with resolution of $v_{IN}/2^N$ for a wide range of input and output voltages," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 543–556, Feb 2016.

[59] B. Nguyen, N. Tang, W. Hong, Z. Zhou, and D. Heo, "High-efficiency fully integrated switched-capacitor voltage regulator for battery-connected applications in low-breakdown process technologies," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6858–6868, Aug 2018.

[60] N. Butzen and M. Steyaert, "A 1.1W/mm^2-power-density 82%-efficiency fully integrated 3:1 switched-capacitor dc-dc converter in baseline 28nm cmos using stage outphasing and multiphase soft-charging," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 178–179.

[61] L. G. Salem and P. P. Mercier, "A recursive switched-capacitor dc-dc converter achieving $2^N - 1$ ratios with high efficiency over a wide output voltage range," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2773–2787, Dec 2014.

[62] S. Bandyopadhyay, Y. K. Ramadass, and A. P. Chandrakasan, "20μA to 100mA dc-dc converter with 2.8-4.2V battery supply for portable applications in 45nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2807–2820, Dec 2011.

[63] Y. Pu, C. Shi, G. Samson, D. Park, K. Easton, R. Beraha, A. Newham, M. Lin, V. Rangan, K. Chatha, D. Butterfield, and R. Attar, "A 9-mm^2 ultra-low-power highly integrated 28-nm CMOS soc for internet of things," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 936–948, March 2018.

[64] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, Oct 2015.

[65] G. Schrom, P. Hazucha, F. Paillet, D. S. Gardner, S. T. Moon, and T. Karnik, "Optimal design of monolithic integrated dc-dc converters," in *2006 IEEE International Conference on IC Design and Technology*, 2006, pp. 1–3.

[66] M. Ghoneima and Y. Ismail, "Accurate decoupling of capacitively coupled buses," in *IEEE International Symposium on Circuits and Systems*, May 2005, pp. 4146–4149 Vol. 4.

[67] Q. A. Khan, S. K. Wadhwa, and K. Misri, "A single supply level shifter for multi-voltage systems," in *19th International Conference on VLSI Design held jointly with 5th International Conference on Embedded Systems Design (VLSID'06)*, Jan 2006.

[68] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, March 2008.

[69] J. Jiang, Y. Lu, C. Huang, W. Ki, and P. K. T. Mok, "A 2-/3-phase fully integrated switched-capacitor dc-dc converter in bulk CMOS for energy-efficient digital circuits with 14% efficiency improvement," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.

[70] R. Karadi and G. V. Pique, "3-phase 6/1 switched-capacitor dc-dc boost converter providing 16V at 7mA and 70.3% efficiency in 1.1mm^3," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb 2014, pp. 92–93.