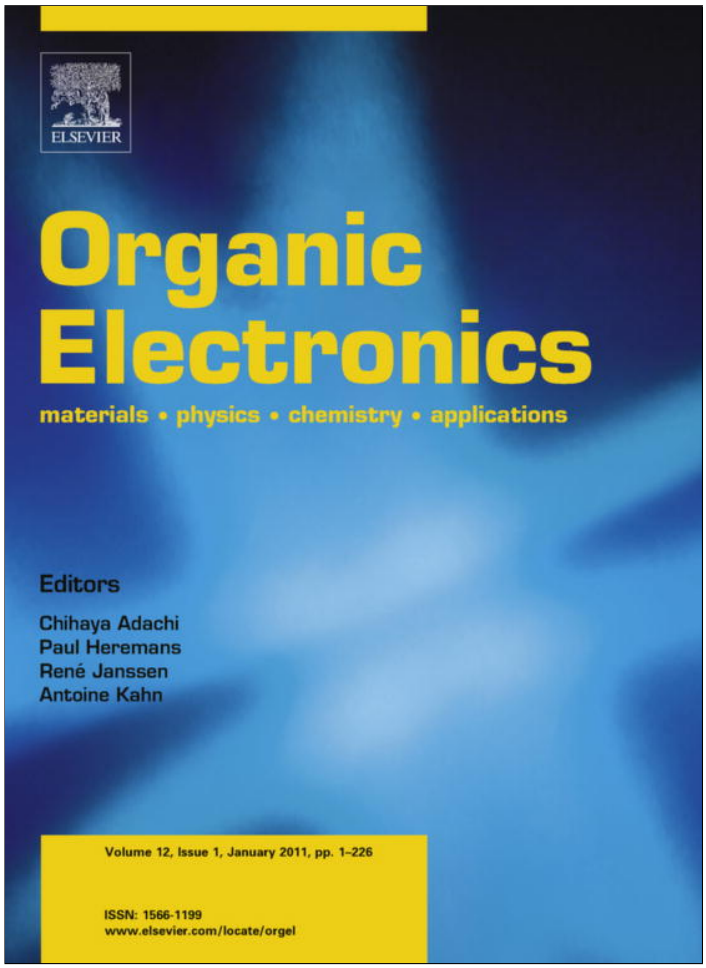

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Organic inkjet-patterned memory array based on ferroelectric field-effect transistors

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ABSTRACT

An inkjet-patterned, flexible organic memory array was demonstrated using non-volatile ferroelectric field-effect transistors which remained functional below 0.6% tensile strain. Each memory cell is comprised of an addressing transistor and a ferroelectric memory transistor. Less than 20% cross-talk was observed between neighboring cells, and binary memory states in a 7 × 8 array were retained for at least 8 h. Variations among the printed memory transistors were characterized and shown to be caused by different rates of charge trapping in the semiconductor–ferroelectric interface.

1. Introduction

Data storage is required in many electronic devices designed for mobile use, such as in sensors and actuators [1,2] and in wireless communication devices [3,4]. The use of non-volatile memory would reduce power consumption, and combining non-volatile memories with other circuit components would allow the realization of non-volatile random-access memory [5] and logic-in-memory architecture [6], which could reduce transistor count and eliminate existing bottlenecks between the logic and the data-storage components.

Non-volatile organic memory devices have been previously reported [7–10] as part of the efforts to develop plastic flexible electronics. Organic materials have shown superior mechanical robustness [11,12] in addition to being compatible with low-temperature processing techniques that may become vital to the realization of mechanically flexible integrated electronic systems. Organic materials are often processed from solution and can be deposited and patterned by inkjet printing [13]. Inkjet printing has been used to fabricate field-effect transistors in active matrix backplanes for reflective displays [14–16] with a typical patterning resolution of 40 μm. For large-area electronics [17–19] where high memory density is not required, the use of printing techniques in the fabrication process is desired due to the potential of low-cost processing steps.

There are several types of non-volatile organic memories reported in the literature such as floating-gate transistors [2], resistive memory [8], and ferroelectric devices [9]. In comparison to resistive memory, the switching mechanism of ferroelectrics is better understood. The floating-gate transistors require nanometer control of the tunneling distance between floating gates and control gates; in contrast, ferroelectric memory devices do not have such stringent thickness requirements and are more suitable for printing processes. Therefore in this paper we use ferroelectric field-effect transistors (feFETs) [20–22] as the memory components. The feFET gate dielectric used here was a ferroelectric co-polymer poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) that retained

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its polarization even after the external electric field was removed, and thus the feFETs were non-volatile. The ferroelectric transistors allowed reprogrammability and non-destructive read-out, and this offered an advantage over using ferroelectric capacitors, for which the read-out process would erase the polarization states.

The current performance of solution-processed organic memory has been sufficient to meet the requirement of short-term applications, including a pressure-sensor system [2] and a wireless communication sheet [4]. When incorporating memory devices into circuit systems, one of the main challenges involves device isolation and proper signal routing. In a memory array, there is potential cross-talk between neighboring devices. Addressing switches such as transistors or diodes are needed to isolate the neighboring cells. Previously in Ref. [4], memory cell isolation was achieved by combining one memory transistor with two addressing transistors, in which one addressing transistor controls the input voltage and the second one selects the readout signal. In this paper we describe a memory array design that uses only one addressing transistor in each memory cell, simplifying array design and reducing footprint requirements. This design can be applied as non-volatile random-access memory [5] to reduce power consumption. We have also examined device variations among the memory transistors, to determine how array performance could be improved.

Each memory cell is comprised of two transistors: one feFET (memory element) and one addressing transistor (signal switch). Both the feFET and the addressing transistors were in top-gate configuration and with p-type semiconductors. The typical transfer characteristics of an addressing transistor and of a memory feFET are plotted in Fig. 1(a) and (b), respectively. The transistors showed average saturation mobility of 0.2 $cm^2/V\,s$ for Flexink and 0.01 $cm^2/V\,s$ for PQT [23]. No significant hysteresis was observed in the addressing transistors during gate-voltage V_g sweeps, as shown by the measurement in Fig. 1(a). To use the feFETs as memory devices, the polarization of the ferroelectric dielectric was set by an input V_g. The remnant polarization affected the transistor source–drain current I_{sd}, and thus the I_{sd} hysteresis in Fig. 1(b) served as a record of the applied gate voltage. As the V_g pulse time was increased in Fig. 1(c), the output I_s became saturated. A V_g pulse length of 1 ms was the minimum switching time required for a feFET current to reach the plateau value. This timing requirement may be different depending on polarization direction (switching from positive to negative V_g versus negative to positive V_g) [21] and dielectric thickness [24]. The gate current in Fig. 1(d) shows peaks at ±25 V, indicating the coercive voltage where the ferroelectric dielectric switched polarization.

The effect of strain on feFET was examined for use in mechanically flexible applications. The transfer characteristics in Fig. 1(e) shows that current was reduced with tensile bending at 0.4% strain where radius of curvature = 1.5 cm. Nevertheless the characteristics recovered when the device was laid flat again and released from strain. The current reduction with bending has been previously observed in non-ferroelectric organic transistors [25], in which mechanical strain led to changes in dielectric capacitance and semiconductor mobility. The current in Fig. 1(f) was measured with source–drain voltage $V_{sd} = -10$ V and $V_g = 0$ V under tensile bending, after the feFET had been polarized at $V_g = +30$ V. Since PVDF-TrFE is a ferroelectric polymer, piezoelectric voltage was generated during bending and was observed as spikes at transitions. After the spikes, the I_{sd} was decreased by <5% under tensile strain of 0.4%, and the I_{sd} partially recovered when the substrate was relaxed to 0% strain. The reason for incomplete recovery was that, besides mechanical bending, the feFET current was also affected by electrical bias stress under constant V_{sd} bias. Without mechanical bending, electrical bias stress [26] alone would reduce I_{sd}, as indicated by the dashed line in Fig. 1(f). The measured feFET current change under constant V_{sd} is ~5% over 15 min, and this level of bias stress is comparable to the current change in previous studies [27,28] and is due to traps at the semiconductor–dielectric interface. The feFET remained functional up to tensile strain of 0.6% (radius of curvature of 1 cm) before it broke down with open circuit. The above results were promising for applying feFETs to mechanically flexible systems, but more detailed studies are needed to thoroughly characterize the influence of strain on feFET parameters and to elucidate the long-term effects of repetitive strain cycles on memory retention time.

To place the memory feFETs into an array, neighboring devices were isolated by addressing switches such as transistors or diodes preventing potential cross-talk. The schematics and the photograph of an active matrix array are shown in Fig. 2. The addressing transistor regulated the input voltage to a memory feFET within each cell. Although the cells in a column were connected to a common data-line, the input voltage was passed only to a specific feFET, by turning on its addressing switch through applying a voltage pulse to its select-line. The addressing transistors of neighboring rows were turned off by holding their select-lines at ground or positive voltage. The bus-lines B_N and the readout-lines R_N were maintained at ground during the memory input process. For the read-out process, the key to minimize cross-talk relied on that the readout-lines and bus-lines of feFETs were arranged perpendicular to each other and located on separate layers as shown in Fig. 2. To determine the memory state of cell C_{11}, a voltage pulse was applied to the bus-line B_1, and the feFET current or charge was measured from the read-out line R_1. The other bus-lines $B_2 \ldots B_N$ were maintained at ground potential. The measured current depended on the state of the feFET at cell C_{11} only and was not affected by other feFETs connected to the same readout line, because their bus-lines were grounded to not generate current.

The input signal to an addressed feFET and to its neighbor down the column is shown in Fig. 3(a) and (b), respectively, by monitoring the voltage at the feFET gate-electrode pad with a picoprobe [29]. The input voltage was transmitted to the intended feFET through its addressing transistor within 1 ms. The voltage at the neighboring feFET gate electrode has remained below 2.5 V (less than 20% of the input voltage at the data-line), indicating that neighboring cell was sufficiently isolated from cross-talk disturbance. Voltage overshoot due to capacitance feed-through [15] was observed during potential change in Fig. 3(a), but it was not deleterious to the signal routing

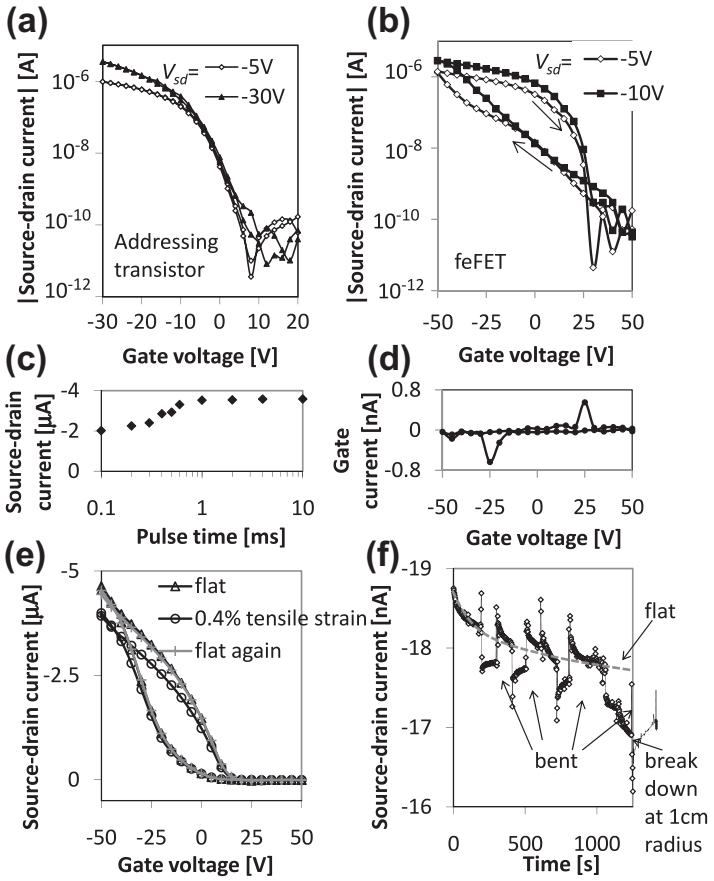

Fig. 1. Transfer characteristics of (a) an addressing transistor and (b) a memory ferroelectric transistor (feFET). (c) Current output of a feFET versus duration of the gate-voltage pulse, with $V_{sd} = -10$ V and $V_g = -30$ V. (d) Gate current of a feFET where $V_{sd} = 0$ V. (e) Transfer characteristics of a feFET with $V_{sd} = -10$ V in different strain conditions. (f) Source–drain current of a feFET under tensile strain cycles, measured at $V_{sd} = -10$ V and $V_g = 0$ V. The feFET had been previously polarized at $V_g = +30$ V. The sample was bent to radius of curvature = 1.5 cm, corresponding to 0.4% tensile strain. The voltage spikes were piezoelectric response of the ferroelectric dielectric. The dashed gray line indicates feFET current at 0% strain; the decrease in current is due to bias-stress effects.

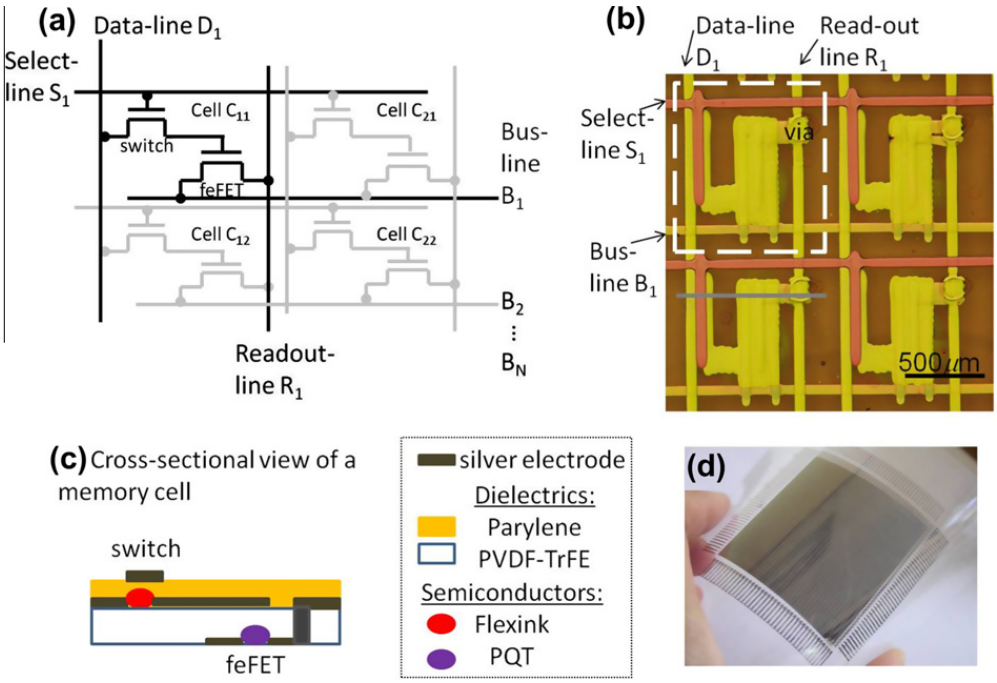

Fig. 2. (a) Schematics and (b) photograph of an active matrix memory array. The black lines in (a) and the white dash box in (b) indicate an individual cell. (c) Cross-sectional view at the location indicated by the gray line in (b). (d) A flexible memory array on plastic substrate.

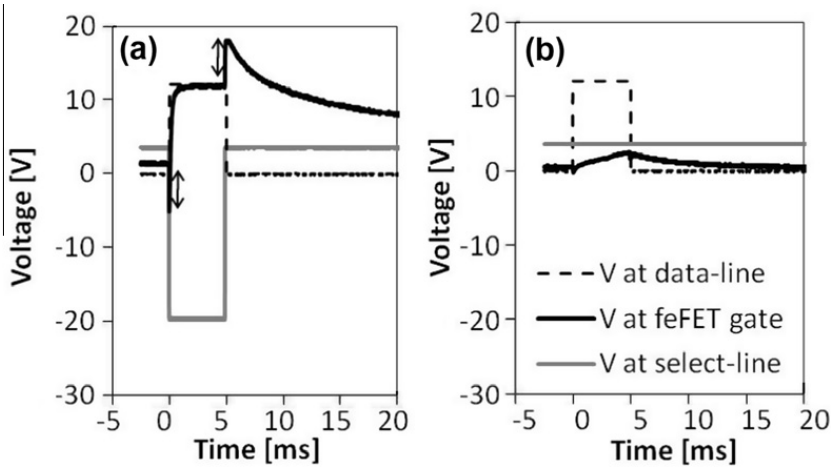

Fig. 3. Comparison between the oscilloscope traces of (a) an addressed feFET and (b) a neighboring feFET down the column. Voltage overshoot due to capacitance feed-through [15] was indicated by the arrows in (a).

process. It was observed that the rise and fall time of the feed-through voltage were not the same because of the difference in channel resistance at respective gate voltages ($V_g = -20$ V during rise, $V_g = 0$ V during fall). The feed-through voltage was due to the overlap between the gate and source electrodes and may be reduced by minimizing the overlapping area.

To write into a memory array as shown in Fig. 4, the select-line voltage was −15 V for turning an addressing transistor on and +10 V for off, and the input data-line voltage was a 5 ms pulse at −30 V for polarized state or at 0 V for unpolarized state, applied according to a checkerboard pattern. Eight hours after the pattern was recorded, the difference in dielectric polarization was obtained by charge amplifiers [30–32]. The read-out electronics applied a 130 μs pulse at −5 V to the bus-line of a selected cell and measured the feFET charge via the corresponding read-out line, while the remaining lines were held at ground. The results in Fig. 4(a) shows distinguishable memory states between neighboring feFETs in a 7 × 8 array. Signals of the two memory states differed by ~6000 readout units or 0.77 pC as seen in Fig. 4(b) (one readout unit corresponded to 800 electrons or 0.13 fC as explained in Ref. [30]). The histogram indicates signal variations of the two polarization states, with standard deviation of 580 units for unpolarized states and 1120 units for polarized states, indicating larger variation after polarization. In this proof-of-concept demonstration, the yield of working memory cells was low (~3.5%, since only the cells in Fig. 4(a) were detectable for a 40 × 40 array). The memory feFETs have been damaged during via processing step, in which solvent was printed to dissolve via holes in the dielectric [33]. Via holes were formed by printing solvent droplets, and eleven drops per site was required to dissolve the PVDF-TrFE film. In the photo in Fig. 2(b), the shape of via were oval instead of circular, due to misalignment of solvent drops. More severe misalignment caused shorts between the feFET gate and source–drain electrodes and was the main reason for low array yield. This misalignment issue can be mitigated by redesigning the cell layout and providing wider area for via process tolerance, or alternative via process such as laser ablation can be used. It should be feasible to improve the array yield in the future by improving layout design and equipment capability.

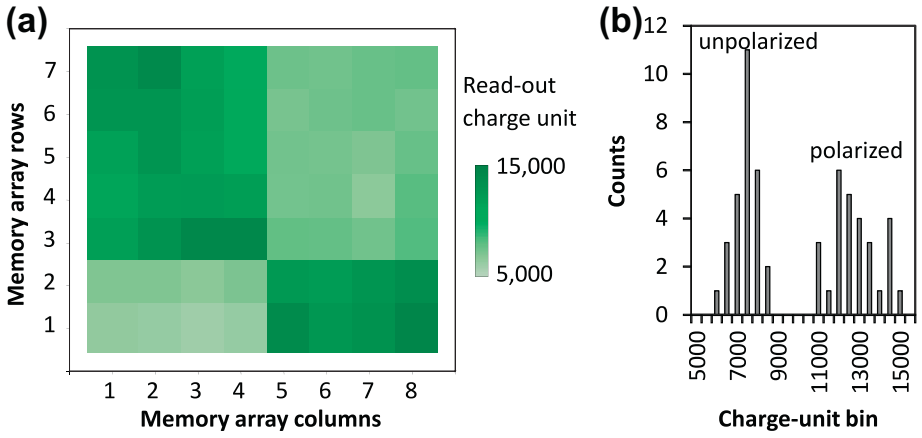

Fig. 4. (a) Memory states of a 7 × 8 array measured by charge sensors 8 h after the feFETs were polarized in a checkerboard pattern. The input voltages were 5 ms pulses at −30 V for the polarized state (dark green) or at 0 V for the unpolarized state (light green). One readout-charge unit corresponded to 800 electrons or 0.13 fC as explained in Ref. [30]. (b) Histogram of the memory cells in part (a). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Fig. 5 compared the output characteristics of twenty inkjet-printed feFETs that were fabricated in an array. The data were all obtained with $V_g = 0$ V and were taken by directly probing the electrodes of the feFETs. A polarization voltage of $V_g = -30$ V was used as it was the voltage limit for our array test setup. This voltage exceeded the coercive voltage of the ferroelectric dielectric Fig. 1(d) and enabled polarization switch, but it was still relatively low and the ferroelectric polarization was not saturated. The addressing transistors were not used for routing in these measurements, in order to only evaluate variations among the memory devices independent of other circuit components. Before polarization, the output current varied by a factor of 2 among the cells Fig. 5(a). After the polarization voltage was applied, the output characteristics varied by a factor of 3 and showed an increase in current variations among the cells Fig. 5(b). The polarized dielectric increased channel charge accumulation, and the feFETs reached saturation regime ($V_g - V_T < V_{sd}$) due to positive threshold voltage V_T. After two weeks since polarization, the output current was no longer saturated in Fig. 5(c), indicating shifts in threshold voltage due to charge trapping [27,28,34–36]. In Fig. 5(d), the values of output current at $V_{sd} = -20$ V showed the I_{sd} ratio between the polarized and unpolarized states was >25 (between 25 and 100). Although the feFET current has decreased to 50% of the initial values after a two-week interval, the memory states were still distinguishable. The decrease in current corresponded to the results from our previous study [36] of similarly inkjet-printed feFETs, in which the memory retention time was extrapolated to be roughly one month, with device variations taken into account.

Achieving consistent characteristics across an array is important for estimating the data-storage time of an array, because it will be limited by the cell with the worst retention time unless the low-performing cells are identified and excluded. Thus, in addition to improving the performance of individual feFETs, it is also desirable to understand and mitigate array variations in memory integration. Before polarization, the variations in output characteristics of Fig. 5(a) were mainly due to differences in mobility among the devices [15]. After the feFETs were polarized, the output characteristics became even less uniform with time. There were different rates of charge trapping among the polarized devices, leading to a widening range of output characteristics in Fig. 5(b) and (c) and larger variations for polarized states in Fig. 4(c). Therefore, besides semiconductor mobility, charge-trapping effects must be controlled to improve array uniformity. Techniques such as template annealing [37] or nano-embossing [38] might reduce charge-trapping effects in the dielectric to extend both the memory retention time and array uniformity.

In summary, inkjet-printed active-matrix memory arrays were demonstrated to show less than 20% cross-talk between neighboring cells. The readout signal from each feFET was isolated by using bus-lines and readout-lines on different layers to enable a memory design with two transistors per cell. The memory arrays were shown to retain data for at least 8 h and remained functional below 0.6% tensile strain. Array uniformity was reduced with time by different charge-trapping rates among the transistors. Thus, better control of charge trapping will improve the performance of individual feFETs as well as enhance array uniformity, to advance organic memory for flexible electronics.

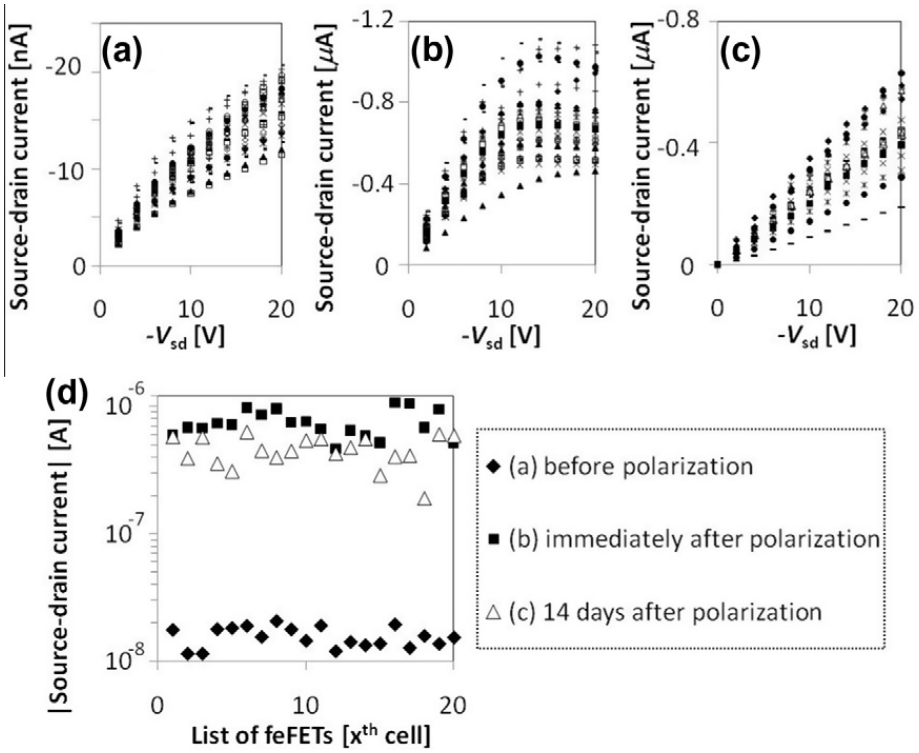

Fig. 5. Output characteristics of 20 feFETs (a) before polarization, (b) immediately after polarization at $V_g = -30$ V, and (c) after two weeks in the polarized state. These output characteristics were taken with $V_g = 0$ V. The graph (d) compares the values of output current at $V_{sd} = -20$ V.

2. Array fabrication

The memory devices were fabricated either on glass or on 125 μm poly(ethylenenapthalate) substrates. Both the addressing transistors and the memory feFETs were in top-gate configuration and were patterned with channel length L of 40 μm. The metal electrodes were inkjet-printed using a silver-nanoparticle solution from Cabot Corporation. The memory feFETs had channel width W of 1 mm and consisted of p-type semiconductor polythiophene (PQT). The memory gate dielectric was spin-coated from a solution of ferroelectric co-polymer poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE, 65:35 ratio) in methyl-ethyl-ketone to form a 600 nm film with capacitance $C_f = 16\ \mathrm{nF/cm^2}$ and was processed as described in Ref. [36]. Interconnects through the PVDF-TrFE dielectric were made by inkjet-printing the solvent methyl-ethyl -ketone to locally dissolve away the dielectric to form via openings, yielding vias with resistance of 150 Ω, similar to the procedure in Ref. [33]. Subsequent layers for the addressing transistors were fabricated with $W/L = 15$ using the polymer blend semiconductor FS12 from Flexink and vacuum-deposited parylene-N as the gate dielectric (film thickness = 400 nm and capacitance = 5 $\mathrm{nF/cm^2}$).

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