Title
Full-Duplex and Self-Interference Cancellation

Author
Gundu, Akshara

Publication Date
2017

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA,
IRVINE

Full Duplex and Self-Interference Cancellation

THESIS

submitted in partial satisfaction of the requirements
for the degree of

MASTER OF SCIENCE

in Electrical and Computer Engineering

by

Akshara Gundu

Thesis Committee:
Professor Ahmed M. Eltawil, Chair
Professor Fadi Kurdahi
Professor Ozdal Boyraz

2017

TABLE OF CONTENTS

Page

LIST OF FIGURES

Page

LIST OF TABLES

Page

ACKNOWLEDGMENTS

I would first like to thank my thesis advisor Professor Ahmed Eltawil. The door to Prof. Eltawil's office was always open whenever I had a question about my research or writing. He consistently allowed this thesis to be my own work, and steered me in the right the direction whenever he thought I needed it.

I am grateful to Dr. Ender Ayanoglu for his unwavering support throughout the course of my master's. A special thanks is in order to Dr. Ozdal Boyraz and Dr. Fadi Kurdahi for their encouragement and participating in my thesis committee.

I would also like to acknowledge Sergey Shaboyan, PhD student at Wireless Systems and Circuits Laboratory, UC Irvine. I am gratefully indebted to him for his very valuable guidance, input and comments on this thesis.

Finally, I must express my very profound gratitude to my parents, professors, mentors, family and to my friends for providing me with unfailing support and continuous encouragement throughout my years of study and through the process of researching and writing this thesis. This accomplishment would not have been possible without them. Thank you.

ABSTRACT OF THE THESIS

Full Duplex and Self-Interference Cancellation

By

Akshara Gundu

Master of Science in Electrical and Computer Engineering

University of California, Irvine, 2017

Professor Ahmed M. Eltawil, Chair

One of the main challenges of In-Band Full-Duplex (IBFD) communication systems is the mitigation of Self-Interference (SI). Most popular self-interference suppression techniques involve taking a copy of the transmitted signal and scaling the copy before subtracting it at the receiver to get the desired signal minus the interference. The scaling involves rotating the phase of the copy and modifying its amplitude. However, due to channel variations, the replica of the transmitted signal could be delayed.

Most systems work with the underlying assumption that the baseband signal remains constant over a delay time interval. It is commonly assumed that baseband information signal experiences an insignificant amount of delay. This does not hold true as the modulated bandwidth increases.

If this delay effect is taken into consideration when designing the canceller, the canceller's performance can be improved.

This thesis work analyzes the effects of the baseband signal delay in Single Channel Full Duplex SI Cancellation Systems. The analysis also attempts to investigate the relationship between signal bandwidth on the cancellation capabilities of the system. For this, an RF Cancellation (RFC) block was designed at the Wireless Systems and Circuits Laboratory to be added as a peripheral to the Single Channel RF System. This document details the results of controlled delay experiments conducted on the RF Cancellation Block.

CHAPTER 1 INTRODUCTION

In-band Full Duplex (IBFD) communication systems simultaneously transmit and receive on the same channel in typical SNR regimes, achieving close to the theoretical double of the throughput i.e. spectral efficiency (measured by the number of information bits reliably communicated per second per Hz), when compared to half-duplex systems. It was previously believed to not be possible because of the interference that results. Due to the advent of Self-Interference (SI) cancellation techniques, such systems are making fast progressions.

To achieve full duplex in a system, it is required that the significant SI resulting from its own transmissions to the received signal, be cancelled. If not completely cancelled the residual SI acts as noise to the received signal and reduces the SNR, thus consequently the throughput. Hence, it can be said that the amount of SI cancellation dictates the overall throughput and is a measure of performance for any full duplex design.

The transmitted signal that is used for cancellation is a complicated non-linear function of the ideal transmitted signal along with unknown noise. Subtracting it without accounting for analog distortions would not generate accurate results. The amount of cancellation achieved depends on the accuracy with which the SI channel between transmitter (TX) and receiver (RX) can be modelled.

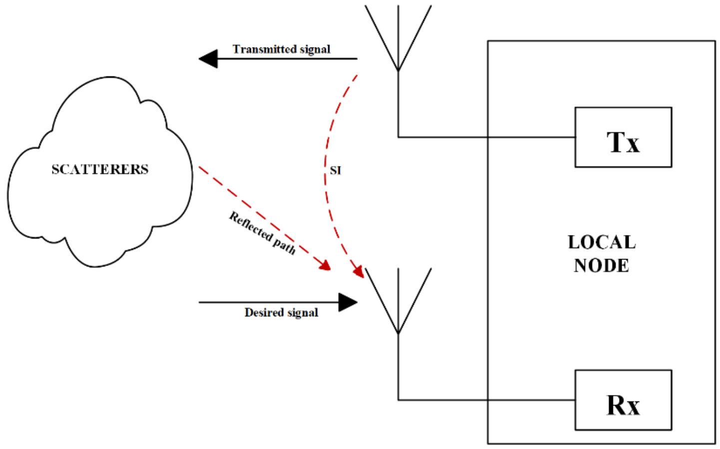


Figure 1.1: Self-Interference in a node

1.1 WHY SI CANCELLATION NOW?

Although IBFD self-interference mitigation techniques have been around for a while, it has gained more popularity in recent times. The reasons being twofold:

1. The traditional approaches to increasing spectral efficiency, such as advancements in modulation, coding and MIMO, have been exhausted
2. There also has been progression towards short-range systems such as small-cell systems and WiFi. Since their cell-edge path loss is less than in that in traditional systems, it makes the SI cancellation problem more manageable [1].

1.2 IMPACT OF SELF INTERFERENCE

To better understand the impact of self-interference, consider the following example: The noise floor is typically measured at -90dBm. To render the transmit self-interference negligible, it must be reduced to the same level as the noise floor. If a signal is transmitted at 20dBm average power, it must be canceled by 20dBm – (- 90dBm) = 110dB!

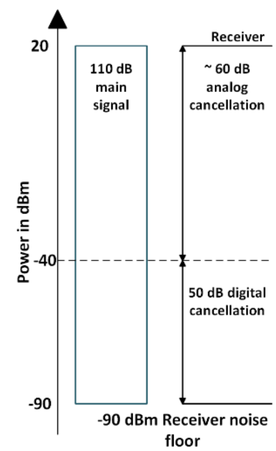


Figure 1.2: Understanding the impact of SI

1.3 SELF INTERFERENCE MITIGATION TECHNIQUES

The self-Interfering signal contains a number of reflections which can be classified as internal and far-field reflections. The internal reflections depend on the components and structure of the transceiver whereas the far-field or external reflections depend on the surrounding environment. Notably, the internal reflections are stronger than the far-field reflections. If the amount of self-interference cancellation does not reach the receiver noise floor, the residual power from the interfering signal will degrade the system's SNR reducing the throughput achievable. Typical full-duplex systems employ multiple types of cancellation to achieve as much cancellation as possible. Ongoing research focuses on eliminating self-interference at different locations within a transceiver system, such as the propagation, analog-circuit and digital domain systems.

A combination of propagation domain suppression and analog-circuit domain cancellation techniques are used to mitigate self-interference at the receiver input [1]. SI Cancellation can be categorized into passive cancellation and active suppression techniques.

PASSIVE CANCELLATION:

Also called propagation domain suppression, this technique is used to mitigate self-interference at the receiver input. Antenna isolation mechanisms and adaptive RF cancellation are examples of such techniques. They help reduce interference before the low-noise amplifier (LNA) in the receiver.

Cancellation in RF domain decreases the amount of non-linearity that would be generated after the signals were passed through down conversion hardware and analog-to-digital converter (ADC). Further employment of digital cancellation methods addresses the remaining interference.

There are two main propagation-domain suppression techniques implemented:

1. Isolation of the transmit and receive chains by the separate-antenna architecture with SI reduction methods
2. Sharing the antenna for transmission and receiving while using isolation devices such as circulators or directional couplers

Antenna separation, being the widely used method out of the two, works on the principle that increasing the path loss between transmit/receive antennas attenuates the SI power. Introducing a third transmit antenna such that the SI adds destructively is another explored method, but additional antennas for full duplex perform like MIMO systems in half duplex and the purpose of FD in such cases is lost.

Propagation domain cancellation techniques mitigate both the self-interference signal and the transmitter noise associated with it. Such techniques also decrease the effect of receiver noise [6].

ACTIVE CANCELLATION:

They are popularly divided into digital and analog cancellation techniques based on the signal domain where the SI signal is subtracted. The analog-circuit domain and the digital cancellation techniques reconstruct the self-interference signal and subtract it from the received signal based on the estimated Channel State Information (CSI) or self-adaptive algorithms [2]. The cancellation is performed at different stages in the transceiver as shown in figure 1.3.

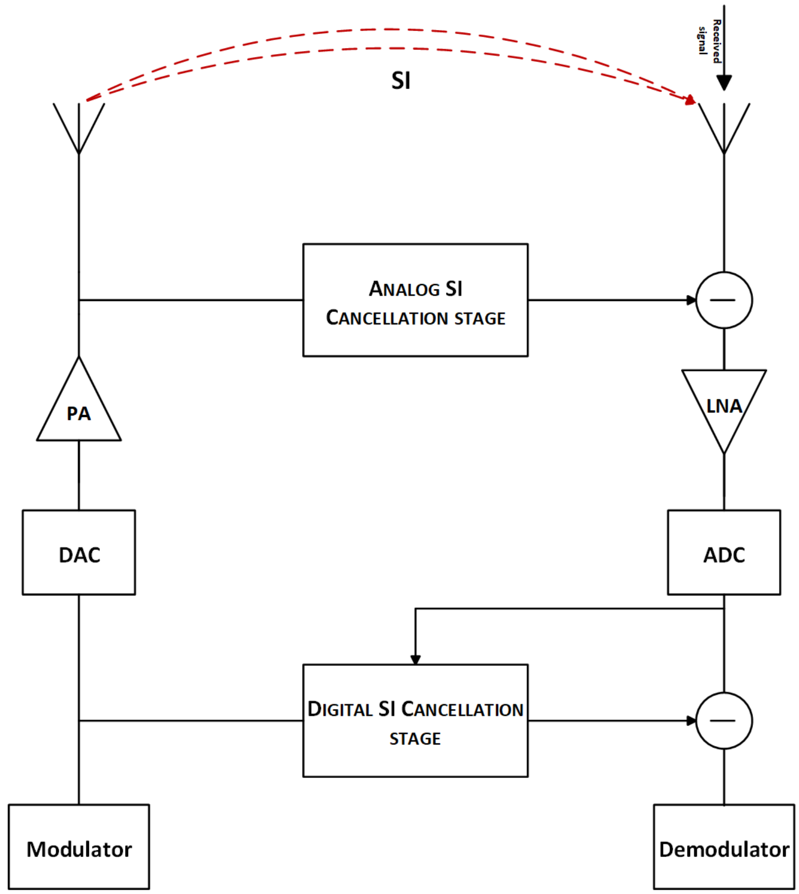


Figure 1.3: Block diagram of a FD transceiver with active cancellation

DIGITAL CANCELLATION:

The cancellation, as is obvious from the name, is performed in the digital-domain. Before trying to understand digital cancellation, it is essential to know what happens to the received signal at the receiver. The received signal, containing the desired signal along with other components such as the self-interference and noise, is amplified and downconverted to either a baseband frequency or some intermediate frequency. The signal is then filtered and sampled through an Analog-to-Digital converter (ADC) to create digital samples. The goal of digital cancellation is to cancel out any residual self-interference after analog and propagation domain cancellation have been performed. Digital cancellation by itself does not provide sufficient suppression and hence is always used in conjunction with analog and other passive cancellation techniques.

Most digital cancellation techniques involve subtracting the known signal from the filtered samples obtained from the ADC. One of the challenges in such systems is estimating the delay and phase shifts between the transmitted and received signals. There are also some non-linearities generated due to hardware and the analog cancellation stages which require to be eliminated. Two popular strategies for combating SI in the digital domain are:

1. Coherent detection method of detecting the self-interference for suppression
2. modelling the linear components as a non-causal function of the known transmitted signal and an approximation method for non-linear components

The coherent detection strategy is less complex and mostly independent of modulation schemes. It is also advantageous when the SI signal is weaker than the received signal, thus improving performance and allowing higher data rates for higher SNR links.

In conclusion, such techniques involve lesser complexity when compared to other techniques. However, the hardware imperfections limit the amount of cancellation achieved. The main limiting factors being the transceiver phase noise and non-linearities.

ANALOG CANCELLATION:

Due to difficulties in adapting analog circuitry to environmentally varying reflections, analog cancellation techniques mainly aim to suppress then dominant internal reflections. Analog-circuit-domain self-interference cancellation is usually deployed at the input of the receiver chain and suppresses the SI before the signal reaches Low Noise Amplifier (LNA) and the ADC. Like popular digital cancellation techniques, the estimated received SI is subtracted from the received signal.

It is imperative to obtain the right estimate of the SI that is received, naively subtracting the baseband information by converting it to analog and upconversion to carrier frequency does not generate favorable results. The various analog components such as the amplifier and Digital-to-Analog Converter (DAC) introduce noise and other non-linearities, thus distorting the signal.

Therefore, a copy of the transmitted signal, including distortions of the transmitter, needs be taken after the Power Amplifier (PA) in the transmit chain.

The analog cancellation stage employed in most systems suppresses the self-interference signal by modifying the phase and amplitude of the estimation of the transmitted SI signal. In addition, the SI channel is usually modelled using the tapped delay line structure, with each delay line consisting of variable delays, tunable attenuators and phase shifters. The lines are added back together, and the resulting estimate of the transmitted SI signal matching the received SI signal is subtracted from the received signal to obtain the desired signal. Matching the delays between the channel and control path containing the attenuators and phase shifters makes tuning very complex. Analog cancellation is also more challenging for MIMO systems since different TDLs would have to be adapted for each antenna pair.

Table 1 summarizes the advantages and disadvantages of the different types of suppression techniques that were described in this section.

The thesis focuses on the analysis of achievable suppression with an active analog cancellation technique. Before moving on to a system level description, it is crucial to comprehend the concept of analog cancellation using multi-tap RF cancellers described by Kolodziej et al [3].

Table 1: Advantages and Disadvantages of the different types of cancellation

TYPES OF CANCELLATION	ADVANTAGES	DISADVANTAGES
PASSIVE CANCELLATION	1. Mitigates SI and transmitter noise by path loss 2. Decreases effect of receiver noise 3. Reduces non-linearity introduced in received signal 4. Improves power efficiency	1. Antenna separation difficult to implement in small devices 2. Introducing additional TX antenna to add SI signals destructively is not efficient when compared to MIMO 3. Additional antenna may not necessarily cause destructive addition of the SI signal
ACTIVE CANCELLATION		
ANALOG CANCELLATION	1. Provides most cancellation when compared to other techniques 2. Cancels transmitter noise and other non-linearities introduced to baseband information since estimate of SI is generated after the PA stage	1. Requires additional hardware 2. Delay matching making tuning of attenuators and phase shifters complex 3. Difficult to implement in the case of MIMO
DIGITAL CANCELLATION	1. Less complex compared to other schemes 2. Does not always require additional hardware 3. Independent of modulation scheme	1. Hardware limitations on cancellation amount 2. Accuracy of SI estimation is hardware limited 3. Needs to be used in conjunction with other techniques

1.4 MULTI-TAP RF CANCELLATION

A popular analog cancellation technique is the channel-aware multi-tap canceller. The RF canceller design proposed mitigates SI by utilizing a passive tapped-delay-line (TDL) architecture, with non-uniform pre-weighted taps to match the natural response of the environment surrounding the antenna. It considers both the direct and reflected path components of self-interference cancellation. Designed in a Tapped-Delay-Line (TDL) architecture with a tap dependent transmission line for delaying the input signal, a variable attenuator and phase shifter are employed on each tap.

In a TDL architecture, as indicated in the figure 1.4, the input goes through several time delay stages as it travels through the transmission line. The delayed signals are extracted at each stage and combined to create a single output. These taps additionally also have the ability to individually adjust the amplitude and phase of their outputs. Over a specified frequency range, the variable attenuator and phase shifter modify the signal's amplitude and phase characteristics. When any filtering device is added in the transmission, an insertion loss occurs. It is a measure of how much the filter attenuates the signal at a given frequency.

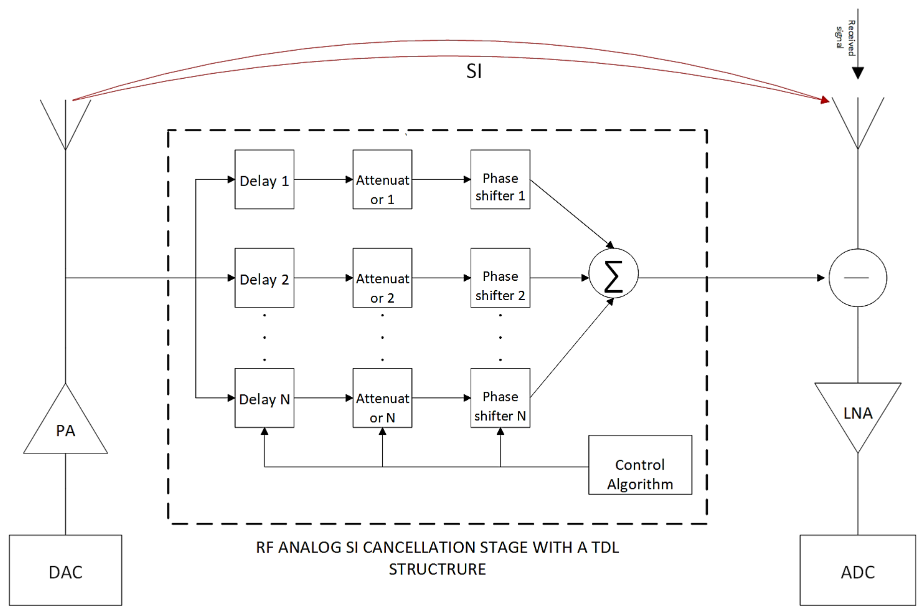


Figure 1.4: TDL Architecture

Numerically, it can be defined as the ratio of the signal level at the input of the filter to the signal of the output filter.

$$Insertion\ Loss\ (dB) = 20\ log_{10} \frac{Unfiltered\ Signal\ Amplitude}{Filtered\ Signal\ Amplitude} \qquad (1.1)$$

In the system described by the paper, each of the four taps require some degree of signal power. A completely passive architecture would create a physical limit on the number of taps, which is why they have only four taps. Even splitting of the canceller's finite input power among N taps is represented as

$$Insertion\ Loss = 10\ log_{10}(N) \qquad (1.2)$$

The insertion loss/divider loss is incurred twice since the canceller splits the input signal and then recombines the weighted tap outputs. The splitting and recombining losses are additional to the insertion loss incurred due to the attenuator, phase shifter and time delay components along with the physical implementation losses.

For the 4-tap canceller designed in this paper, the losses were optimized by analyzing the natural response of the environment surrounding the antenna. Thus, resulting in an extension of the dynamic range, when compared to other systems, by use of directional couplers [3].

In order to maximize the self-interference cancellation over a wide bandwidth, an adaptive algorithm is used to tune the attenuation and phase shift parameters. This algorithm called the Dithered Linear Search (DLS) optimizes over irregular performance surfaces with little internal state knowledge. The input to the algorithm is the Received Signal Strength Indicator (RSSI). The RSSI is dependent on the channel response, which contains both the direct and reflection paths, and the canceller response, which can be tuned.

Objective of the algorithm is to minimize the RSSI. Doing this matches the canceller response to that of the negative SI channel. An average of 30dB cancellation over a 30MHz bandwidth was obtained by the four-tap canceller. There also exists a secondary feedback parameter that consists of a power estimate at the canceller output. This information is unused in the paper presented by [3]. The system tested and analyzed for this thesis makes use of the power information to aid in tuning.

Another popular approach to self-interference cancellation is the full-duplex receiver with SI cancelling capability through LO phase shifting, presented by Agrawal et al [4]. Inter-modulation components generated by SI can degrade the sensitivity by raising the noise floor, since the SI is stronger than the desired signal.

The design exploits the high linearity of a passive mixer-first approach to maximize receiver linearity and allow toleration of larger SI at the input. The proposed receiver achieved >70.5 dB peak SINDR in 16.25 MHz RF BW across an operational frequency range of 800MHz to 1.7GHz.

1.5 MOTIVATION

The TDL architecture has multiple challenges. Since delays signals are extracted at each tap and combined to create a signal output, each tap produces a periodic signal in frequency as a function of the tap's delay parameter. Due to this the operational bandwidth is directly dependent on the time delay parameter of the taps as well as the delay spread. Delay spread is the amount of time in which reflections of the signal, having significant power, arrive. Hence choosing number of taps and their delays is cumbersome and crucial.

The frequency response of the canceller can be modelled as below:

$$H_{Canceller}(j\omega) = \begin{cases} \sum_{k=1}^{K} \alpha_k e^{-j\phi_k} e^{-j\omega\tau_k} & if\ \omega\ \geq 0 \\ \sum_{k=1}^{K} \alpha_k e^{j\phi_k} e^{-j\omega\tau_k} & if\ \omega < \ 0 \end{cases} \tag{1.3}$$

where the attenuation range is $0\ \leq \alpha_k \leq 1$ and the phase shift can vary from $0\ \leq \phi_k \leq 2\pi$ and τ_k is the time delay parameter.

Another challenge is mimicking the changes in SI channel over time by tunable operation of magnitude scaling and time delay. Time delay for narrowband signals was generally approximated as phase shift due to the inefficiency of having tunable delay. The narrowband transmitted signal can be modelled as shown below:

$$T_x(t) = \alpha(t)\cos[\omega_c t + \phi(t)] \qquad (1.4)$$

where ω_c is the carrier frequency, $\alpha(t)$ and $\phi(t)$ are the envelope and phase of the signal respectively.

For narrowband signals. It can be approximated that the envelope and phase are slowly varying with time and can be assumed constant for a time duration τ. According to this, the received signal that results is:

$$R_x(t) = \alpha(t - \tau)\cos[\omega_c t + \phi] \qquad (1.5)$$

Hence, if the cancelling signal is shifted by θ degrees ([0, 360]), the SI can be cancelled.

$$C(t) = [\,\alpha(t) - \alpha(t - \tau)]\cos[\omega_c t + \phi] \qquad (1.6)$$

Assuming the phase is properly aligned.

However, the amount of cancellation is restricted by the phase resolution of the cancelling path. If the error is given by ϕ_e , at band edge this is defined in terms of group delay as:

$$\phi_e = \delta \times \frac{2\pi BW}{2} \qquad (1.7)$$

where δ, is the tolerable group delay.

The amount of cancellation achieved is limited by the equation:

$$SIC_{general}(dB) = -20\log_{10}\left(2\sin\frac{\phi_e}{2}\right) \qquad (1.8)$$

If the phase resolution is given by $\delta\theta$, then the maximum error in phase between the two paths is $\delta\theta/2$, the equation can be rewritten as:

$$SIC(dB) = -20\log_{10}\left(2\sin\frac{\delta\theta}{4}\right) \qquad (1.9)$$

Since the baseband signal is usually a sinusoid with frequency ω_m, the equation finally becomes:

$$SIC(dB) = -20\log_{10}\left(2\sin\tfrac{\omega_m\tau}{4}\right)$$

$$\cong -20\log_{10}\left(\tfrac{\omega_m\tau}{2}\right) \qquad (1.10)$$

This approximation does not hold true when the signal contains a continuous band of frequencies.

$$SIC_{avg}(dB) = -20\,log_{10}\left(\tfrac{\omega_m\tau}{2\sqrt{3}}\right) \qquad (1.11)$$

These equations bound the maximum amount of cancellation and indicate that the group delay must be reduced as much as possible to attain best results. Thus, forming the basis of the study presented in this document.

CHAPTER 2 SYSTEM DESCRIPTION

During the academic year 2016-2017, A full-duplex system was designed and set up by Prof. Ahmed Eltawil and his PhD student Sergey Shaboyan. An overview of the initial system is as depicted in the figure 2.1. The base station is equipped with an omni-directional and a Multifunctional Reconfigurable Antenna (MRA). The MRA has beam-steering capabilities and nine modes of operation corresponding to nine steerable beam directions. It can achieve an average of 6 dB Signal to Noise Ratio (SNR) gain compared to legacy omni-directional antenna equipped systems with minimal training overhead [5].

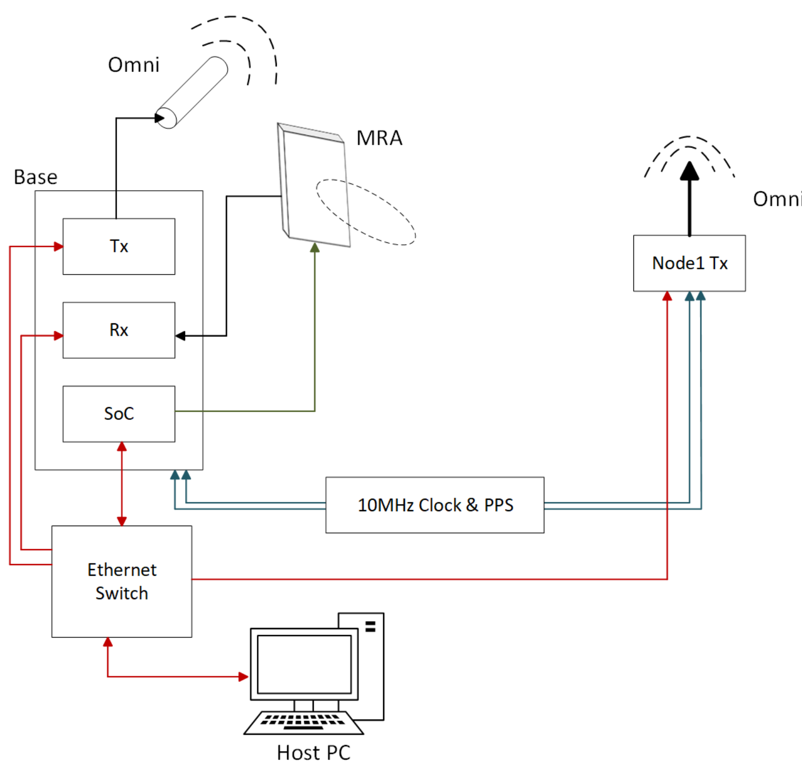


Figure 2.1: Full Duplex System

95 dB of self-interference suppression was obtained experimentally using an MRA based full duplex system [6]. The base station uses the omni-directional antenna to transmit and MRA to receive signals (full-duplex). The transmission data is generated in a host PC which also processes the received data.

As discussed previously, self-interference cancellation is a prevailing issue in such full duplex systems. To eliminate the SI, the MRA is trained and configured to provide its best suppression. For the remaining SI signal, an RF Cancellation block[1] was designed and added to the path as shown in the figure 2.2. It provides an element of extra suppression. Suppression is achieved by

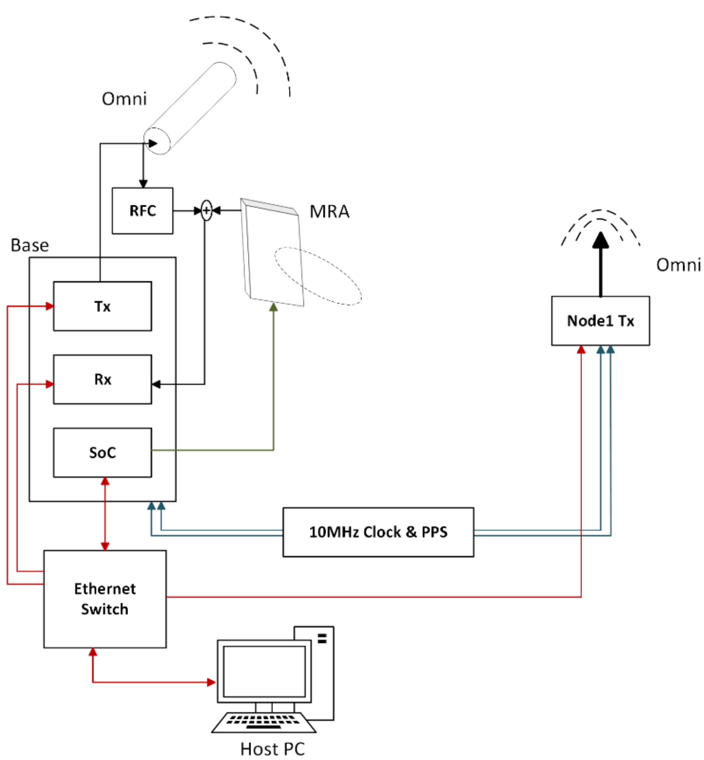


Figure 2.2: Modified system with RFC block

[1] Designed and developed by Sergey Shaboyan

taking a copy of the transmitted signal, estimating the interference present in received signal and deducting the estimate from it.

2.1 THE RF CANCELLATION BLOCK

The RF Cancellation (RFC) block modifies the amplitude and phase of the replica transmitted signal, which is then subtracted from the received signal. The RFC block contains an 8-bit attenuator and a phase shifter. In essence, it performs functionally similar to a Tapped Delay Line architecture system. The system blocks can be described as can be seen in figure 2.3.

For this particular system under test, the coupler is given the transmission data at the input. At the other end a copy of the transmitted signal is obtained, allowing its transmission through a control path. The coupler also allows for the signal to be transmitted through the channel. The coupling is achieved with minimal loss in power to the transmitted signal.

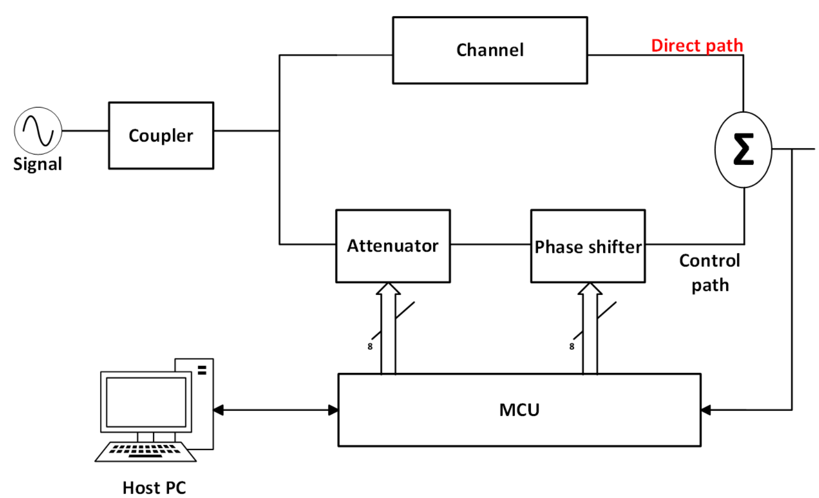


Figure 2.3: The RFC block

The replica traverses through the control path containing a 1-bit and 7-bit attenuator and a 9-bit phase shifter. A Microcontroller (MCU), in this case a National Instruments (NI) setup, is used as a secondary feedback parameter. It performs power estimation at the canceller output and aids in tuning of the attenuator and phase shifter. There also exists a provision to manually manipulate the attenuation and phase shift values of the replica. This can be done at the host PC, which receives information through the MCU block.

THE ATTENUATOR

A one-bit and 7-bit attenuators are integrated to be used in the system for attenuating the replica of the transmitted signal. The one-bit attenuator (HMC802ALP3E) by Analog Devices has an insertion loss of less than 3 dB and covers a wide range of frequencies. It is ideal for RF and cellular infrastructure applications. It provides two attenuation settings: either ‘0’ or no attenuation or 20 dB attenuation.

The 7-bit RF digital step attenuator (DSA) chip (PE43712), by peregrine semiconductors, provides flexible attenuation steps with glitch-less attenuation state transitions. It can provide up to 31.75 dB of cancellation. The attenuator chip can be used in a wide variety of 3G/4G wireless infrastructure, point-to-point communication systems and land mobile radio systems. The DSA supports a broad frequency range from 9 kHz to 6 GHz, making it ideal for use in the desired 802.11ac range. It has approximately a maximum of 2 dB insertion loss, in the desired frequency range of 2.3 – 2.5 GHz. The attenuation error can be calculated based on frequency range and the attenuation setting. A table providing different attenuation settings and attenuation error is available in the datasheet for the chip.

INTEGRATION OF THE TWO CHIPS

Since the two attenuator chips are integrated to provide a maximum of 52 dB of attenuation, it becomes crucial to ensure a smooth transition in attenuation states. The 7-bit attenuator is programmed in 0.25 dB attenuation step setting. Once it reaches 19.75 dB of attenuation, an additional increase in the steps activates the 1-bit attenuator, which then provides 20 dB of attenuation, ensuring a smooth transition. Once the single-bit attenuator is activated, the 7-bit attenuator is reset to zero attenuation setting. Attenuation after this is performed by incrementing the bits of the 7-bit attenuator in 0.25 dB steps.

While decrementing the amount of attenuation required a similar procedure is followed. When switching from 20 to 19.75 dB the, 1-bit attenuator is deactivated and 7-bit DSA takes over.

THE PHASE SHIFTER

An 8-bit digital phase shifter (DPS) by Peregrine semiconductor (PE44820), designed for use in a broad range of applications such as base station transceivers and active antenna arrays, is used in the RFC block. It covers a range of 358.6 degrees in 1.4 degree steps. It was chosen for its ability to maintain good phase and amplitude accuracy across a frequency band of 1.1 to 3.0 GHz. It has a maximum of 7.1 dB of insertion loss. Although, 9 bits are provided for the phase control, the 9th-bit is unused for the application in the RFC block and can be used for optimization in the future.

An integrated digital interface supports both serial and parallel programming of the phase setting. The serial control mode is the used setting and has a control register map with a phase setting word of 9 bits and unit address word of 4 bits. The unit address word is set to ‘1100’ and the desired positive phase shift can be obtained by incrementing the bits from values 0 to 255. Decrementing from 255 generates a negative phase shift if desired.

THE NI/ MCU SETUP

A National Instruments (NI) FPGA + RF module is used as feedback to control the amount of attenuation and phase shifting. The NI 5791R RF transceiver adapter module along with an NI FlexRIO FPGA module are inserted into the PXI chassis slot.

The transceiver module has an analog-to-digital converter (ADC) and digital-to-analog converter (DAC) along with programmable attenuators, selectable receive and transmit filters. It can upconvert and downconvert RF signals ranging from 200 MHz to 4.4 GHz. The canceller output is also sent to the RF module, which then downconverts the input signal through a series of filters and attenuators, after which it is converted to digital data. The FPGA module then is used to analyze the data and view on the host PC. This also provides a UI through LABVIEW.

2.2 RFC BLOCK SYSTEM DESCRIPTION

This system performs RF interference cancellation using the knowledge of transmission to cancel self-interference in the analog domain, before the signal is digitized. The ideal scenario for such a cancellation is when the amplitudes from the direct path & the controlled path are perfectly matched, and the phase of the signals differs by π. The inverse of the transmitted signal is obtained by using a phase shifter with an attenuator, dynamically controlling and adjusting the phase and attenuation values to match the SI signal.

Assuming some unit signal $s(t)$ with amplitude A_1 and phase ϕ_1 , the transmitted signal, at the input of the coupler, $T_x(t)$ can be given by

$$T_x(t) = A_1 s(t) e^{-j(\omega t + \phi_1)} \qquad (2.1)$$

The direct path and control path signals before the summing component can be expressed respectively as follows:

$$x_D = (1 - \alpha_1) A_1 s(t) e^{-j(\omega t + \phi_1)} \quad (2.2)$$

$$x_C = \alpha_c A_1 s(t) e^{-j(\omega t + \phi_c)} \qquad (2.3)$$

Where α_1 is the attenuation coefficient introduced due to the coupler. When summed, we require the signal to cancel out.

Hence, the values of the phase and attenuation values are to be:

$$\phi_c = \phi_1 + \pi \qquad (2.4)$$

$$\alpha_c = 1 - \alpha_1 \qquad (2.5)$$

$\alpha_c$and ϕ_c are functions of the attenuation and phase of the signal when at the beginning of the control path which was

$$x_{CP} = \alpha_1 A_1 s(t) e^{-j(\omega t + \phi_2)} \qquad (2.6)$$

This can be pictorially represented as shown in the block diagram below in figure 2.4.

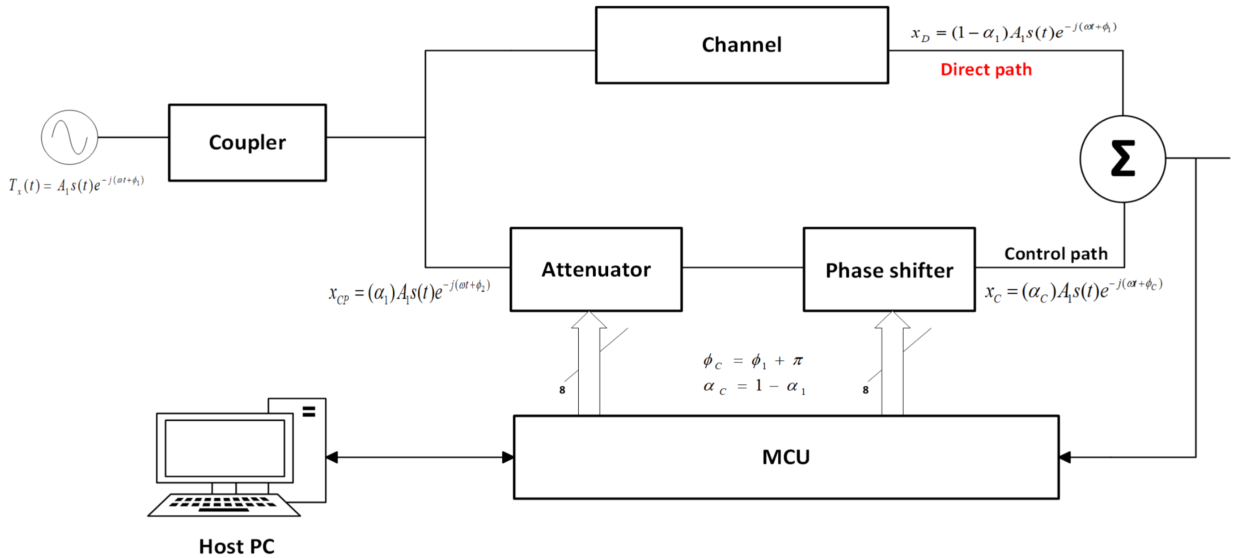


Figure 2.4: System equations in each path

CHAPTER 3 EXPERIMENTAL TESTS AND RESULTS

Once the concepts of full duplex and self-interference were established, an experiment was performed on the system described in the previous section to analyze the effect of delay in channel on cancellation. The experimental setup is as shown below in figure 3.1.

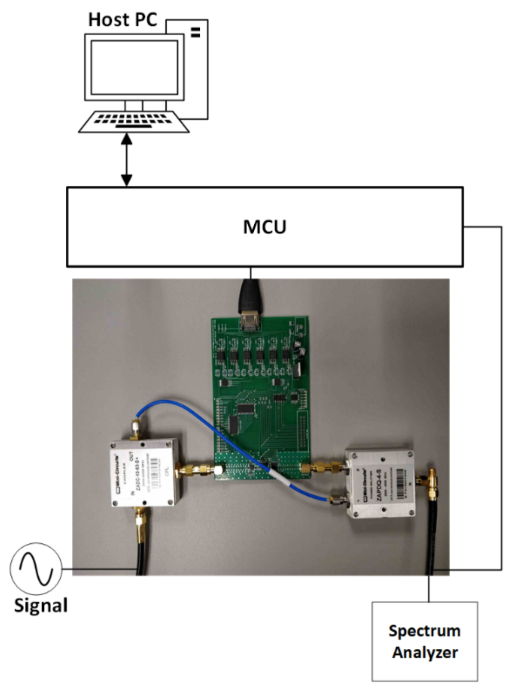


Figure 3.1: Experimental Setup

The setup consists of a signal generator, spectrum analyzer, power source, NI FPGA module, a coupler, the PCB containing the RFC block, coaxial cables acting as transmitter, receiver and channel. The PCB also has LEDs to indicate the values of attenuation and phase shifter in binary. An OFDM QPSK pulse is generated, with center frequency of 2.5 GHz, at the signal generator. A voltage of 5 V is required to power up the board. The experiment is performed over a bandwidth of 20MHz. The NI FPGA module interfaced with the board and acts as a controller and provides a LABVIEW GUI to control the values of attenuation and phase.

The LABVIEW GUI allows for a manual and automatic adjustments in attenuation and phase. For the manual adjustment, either the phase or attenuation are first chosen to be modified. Adjustments are made in steps while observing the signal to see if there is any reduction in signal power. Once a change is noticed in signal power and maximum cancellation possible by the parameter is obtained, the values of the other parameter are modified. Complete cancellation is achieved once the appropriate attenuation and phase shift values are found.

For the initial setup, the signal is cancelled without introducing any delay to observe the amount of cancellation that can be obtained. The waveform is as shown in figure 3.2.

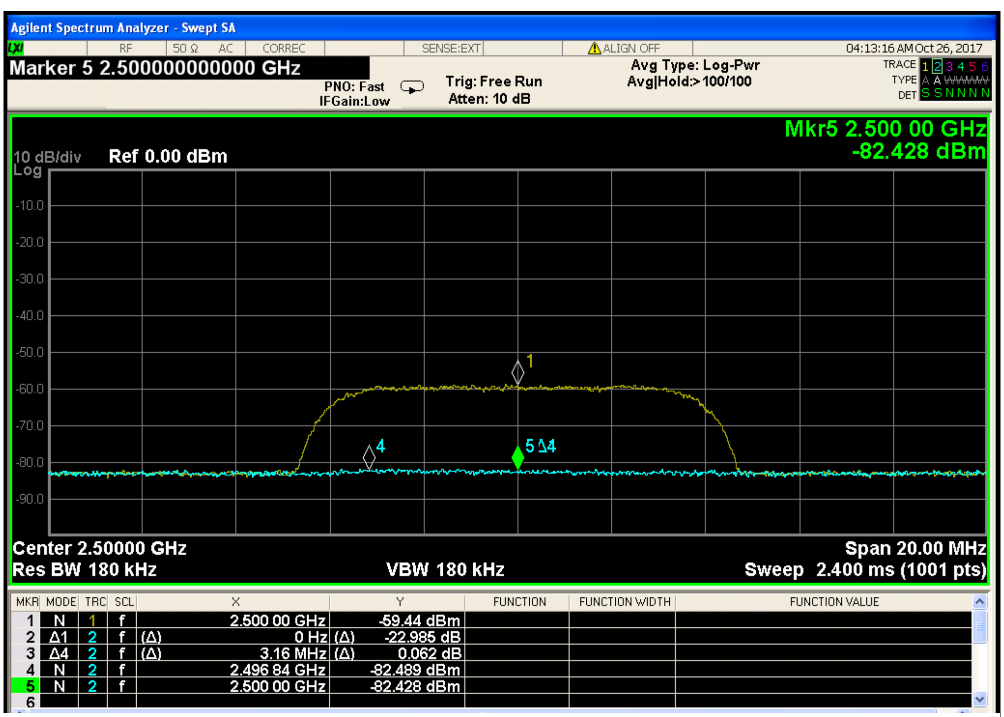


Figure 3.2: Suppression with no delay

As it can be seen in the figure, the noise floor is around -83 dBm, the transmitted self-interference signal is recorded at approximately -60 dBm. A total and near complete cancellation was observed. Nearly 23 dB of suppression was required to cancel the self-interference and bring it down to the noise floor.

3.1 INTRODUCING CHANNEL DELAY

The goal of the experiment is to introduce delay in the channel and see its effect on cancellation at the output. For the sake of the experiment, we want to cancel the input signal (in this case the self-interference) completely. Delay is introduced by using coaxial cables of various lengths in the channel path. The system with delay introduced in the direct path can be described as seen in figure 3.3.

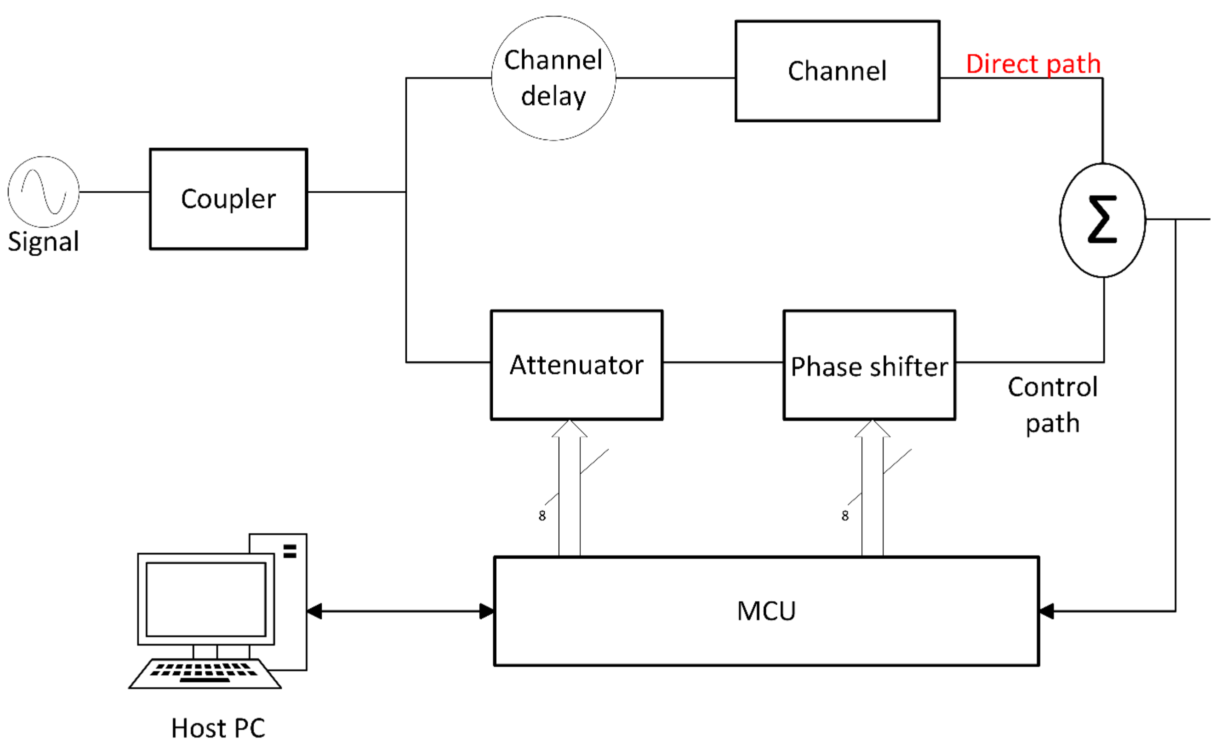


Figure 3.3: System with channel delay

The length of the coaxial cable is used to determine the amount of delay introduced by it. Ideally, the delay increases linearly with the cable length. To calculate the delay in free space, we would use the speed of light to determine the wavelength. A similar concept is used to mathematically model the relationship between length of the coaxial cable and delay introduced by it.

$$v = \frac{Length\ of\ the\ cable}{Delay} \qquad (3.1)$$

Where $v \cong 1.966 \times 10^{8}\ m/s$, as calculated based on the impedance of the cable [7]

Rearranging the equation to calculate delay gives the expression:

$$Delay = \frac{Length\ of\ the\ cable}{1.966 \times 10^{8}} \qquad (3.2)$$

The expression (3.2) was used to obtain the delays corresponding to various cable lengths, the values are tabulated in table 2.

Table 2: Delays for various coaxial cable lengths

COAXIAL CABLE LENGTH (cm)	**DELAY (ns)**
50	2.54
61	3
82	4.17
100	5
143	7.27
161	8
173	8.8
200	10

When a delay is introduced in one path, at the summing point a misalignment of the two signals occurs and can be visually thought of as two misaligned sine waves as seen in figure 3.4.

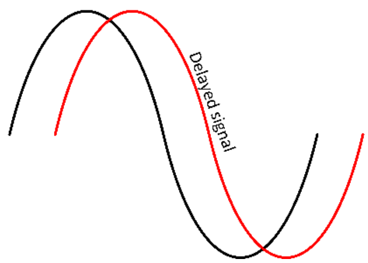


Figure 3.4: Misalignment in direct path and control path signals

When traversing through the bandwidth, the misalignment is more at the band edges and cancelling such signals does not cancel the side lobes completely. This was observed for various delays, the suppression for a channel delay of 3ns is shown in figure 3.5.

Figure 3.5: Suppression with 3ns channel delay

It is observed that there exists a peak (side lobe), at almost 2dB above the minimum, at the output.

3.2 INTRODUCING MATCHED DELAY

If the delay was matched in the control path, then the side lobes could be cancelled and better suppression obtained. For this purpose, a matched delay was introduced in the control path. The delay is provided by coaxial cables of varying lengths. The control path delay required to match the channel delay is lesser than the delay introduced in the channel. This is because the control path components introduce delays in cancellation and the delay varies with the amount of attenuation and phase shift applied to the signal.

The system with matched delay is as shown in the figure:

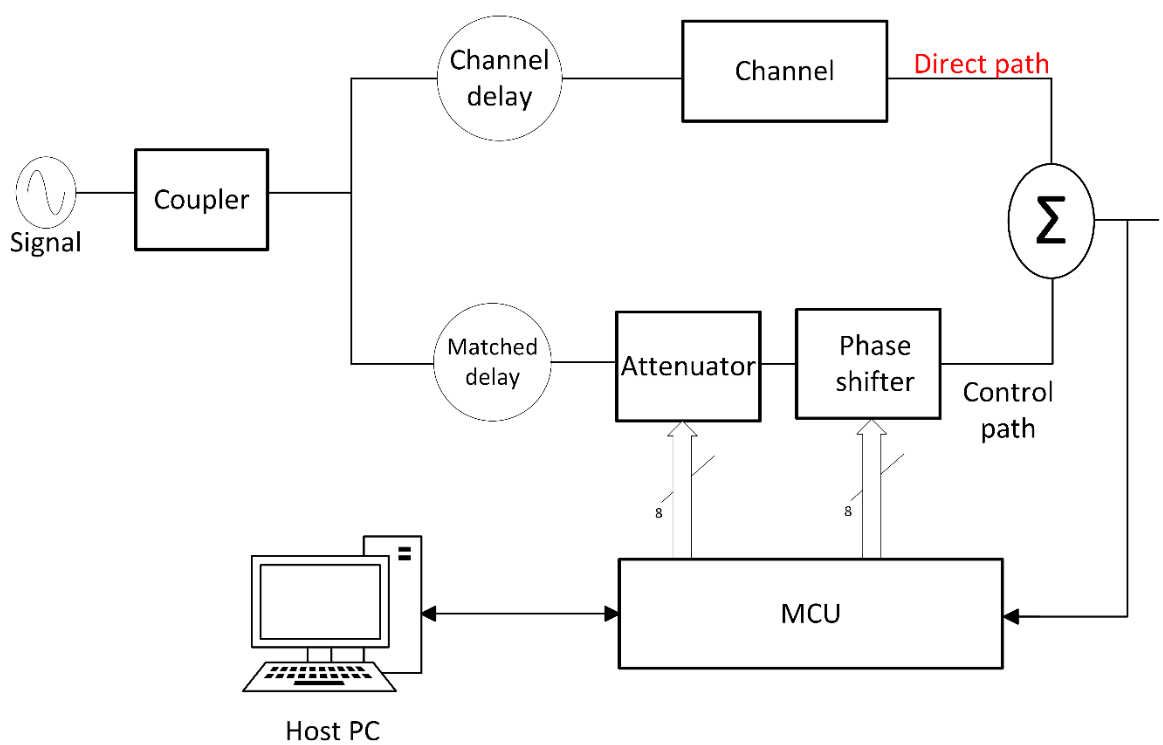


Figure 3.6: System with matched delay

For a 3ns delay in the channel, a matched delay of 2.54 ns was required to obtain complete suppression to noise floor, as seen in figure 3.7.

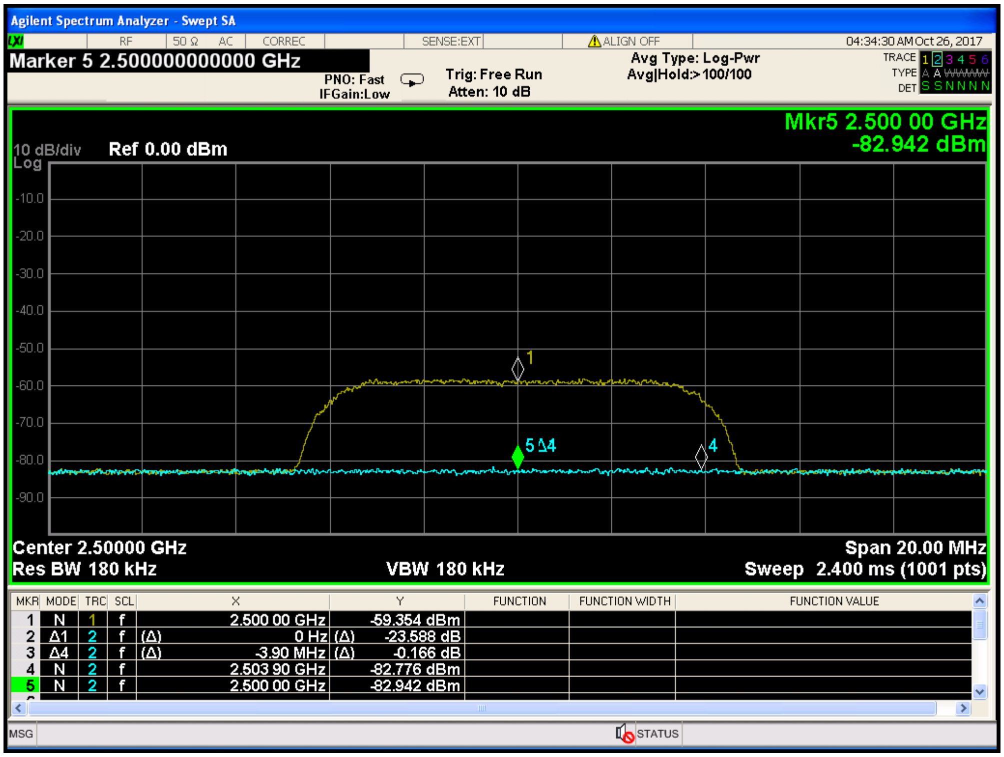
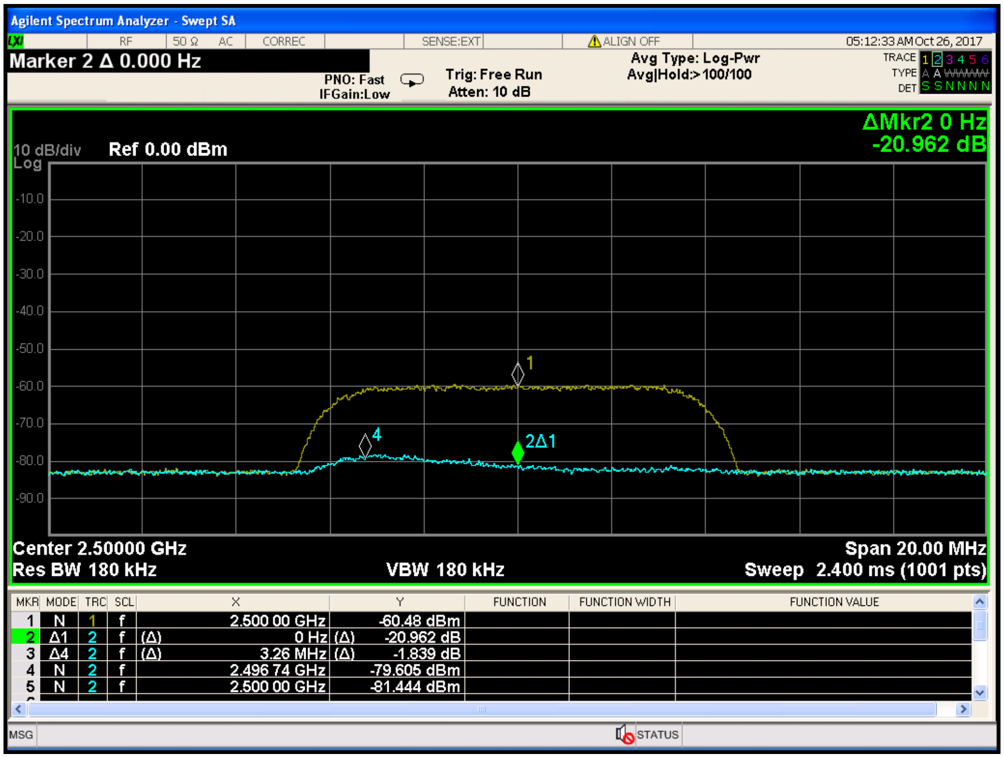


Figure 3.7: Suppression with matched delay when channel delay is 3ns

As it can be seen, the side lobe was cancelled and residual power of the suppressed signal is in a negligible range. The experiment was repeated for channel delays of 5ns, 8ns and 10ns. It was observed that larger the delay, larger the residual side lobe power without matching delays. The results of the experiment are as seen in the following figures.



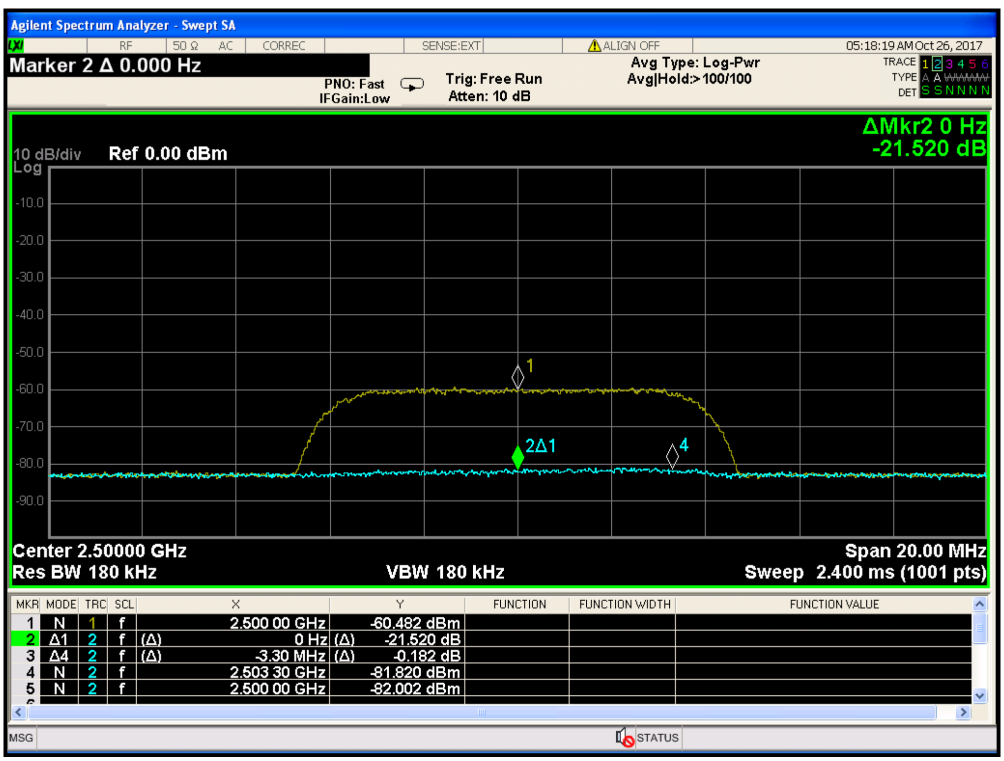


Figure 3.8: Suppression with 5ns delay

Figure 3.9: Suppression with 8ns delay

Figure 3.10: Suppression with 10ns delay

The results of the experiment were tabulated, and the amount of suppression obtained with matched delay and without is compared in figure 3.11.

Table 3: Delays vs Suppression obtained

CH cable length (cm)	**Delay introduced in the channel (ns)**	**suppression obtained(dB)**	**Side lobe unmatched (dB)**	**Side lobe matched(dB)**	**Matched cable length (cm)**	**matched delay(ns)**
ref	no delay	23	0.08	-	-	-
61	3	22.8	1.84	0.18	50	2.54
100	5	21.50	1.84	0.18	82	4.17
161	8	22	5.32	0.83	143	7.27
200	10	20.12	8.58	1.27	173	8.8

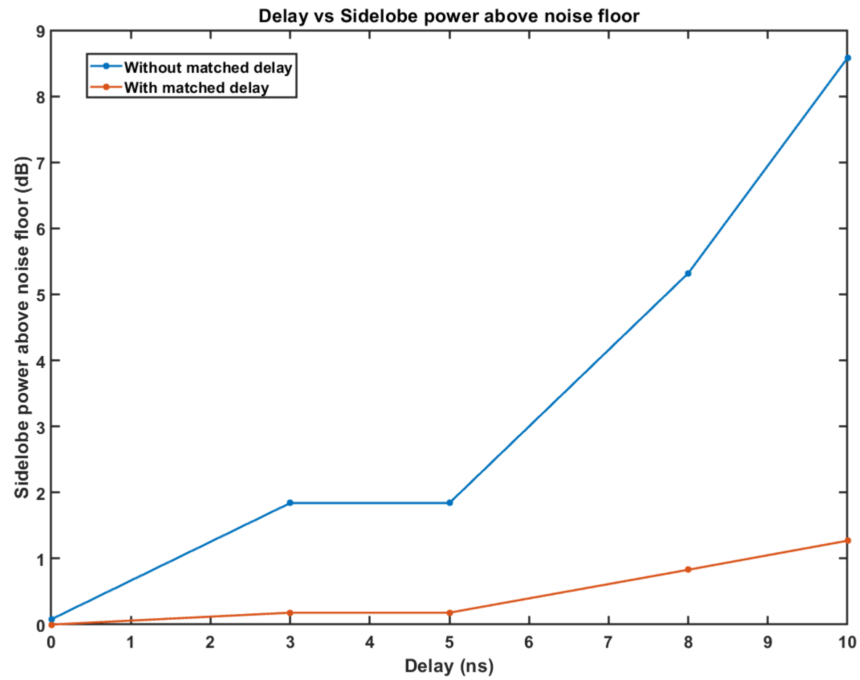


Figure 3.11: Delay vs Side lobe power above noise floor

There are also two other effects occurring during cancellation:

1. Sometimes, when a delay is introduced in the channel and attenuation and phase shift parameters, even without adjustment indicate that cancellation is occurring. Although the values of phase and attenuation are zero, some cancellation is occurring because the control path signal's phase and attenuation are adding destructively to the direct path signal that has some delay. This effectively reduces signal power.
2. Another effect observed was that introducing delay caused the signal to be at a higher power than the reference signal. This is because the signals from paths are adding up in a way that increases the SI signal power.

3.3 CONCLUSION

Analyzing the SI is one of the most important aspects of study for development of full duplex systems. The thesis described a FD system with a tunable RF cancellation block that suppresses the self-interference in the analog domain. An experiment was conducted by introducing channel delays of 3,5,8 and 10ns for a 20Mhz bandwidth system centered at 2.5Ghz. The observation that, when there is a channel delay, a misalignment occurs at the summing point, causing the side lobes to have significant power, was discussed. The misalignment tends to be maximum at band edges. One method to combat this issue would be to introduce a delay in the control path as well to match the channel delay. Matched delay was introduced in the control path and output was observed. The matched delay must be a little less than the channel delay since the control path introduces a small amount of delay based on the attenuation and phase values chosen. Introducing matched delay reduced the side lobe power to an acceptable range toward the noise floor.

In conclusion, there are three different, most popularly used, stages for SI Cancellation. The maximum amount of cancellation is obtained when multiple cancellation methods are used in conjunction.

BIBLIOGRAPHY

[1] Sabharwal, P. Schniter, D. Guo, D. Bliss, S. Rangarajan, and R. Wichman, “In-band full-duplex wireless: Challenges and opportunities,” IEEE J. Sel. Areas Commun., vol. 32, no. 9, pp. 1637–1652, Sep. 2014

[2] Liu, Donglin, Ying Shen, Shihai Shao, Youxi Tang, and Yi Gong. "On the Analog Self-Interference Cancellation for Full-Duplex Communications with Imperfect Channel State Information." *IEEE Access* (2017).

[3] K.E.Kolodziej, J.G.McMichael and B.T.Perry, ‘‘Multitap RF canceller for in-band full-duplex wireless communications,’’ IEEE Trans. Wireless Commun., vol. 15, no. 6, pp. 4321–4334, Jun. 2016

[4] Gaurav Agrawal, S. Aniruddhan and R. K. Ganti, “A Self-Interference Reliever for Full-Duplex Radios”, unpublished

[5] Le-Ngoc, Tho, and Ahmed Masmoudi. *Full-Duplex Wireless Communications Systems: Self-Interference Cancellation*. Springer, 2017.

[6] Li, Zhouyuan, Elsayed Ahmed, Ahmed M. Eltawil, and Bedri A. Cetiner. "A beam-steering reconfigurable antenna for WLAN applications." *IEEE Transactions on Antennas and Propagation* 63, no. 1 (2015): 24-32.

[7] Ahmed, Elsayed, et al. "Full-duplex systems using multireconfigurable antennas." *IEEE Transactions on Wireless Communications* 14.11 (2015): 5971-5983.

[8] Jacques Audet. Coaxial cable delay. [Online] Available: https://pdfs.semanticscholar.org/c692/b83e28ca902022af720cd23e10d71697d1b0.pdf

[9] Liu, Donglin, et al. "Analysis of Analog Self-Interference Cancellation with Imperfect Channel State Information for Full-Duplex Radios." *Globecom Workshops (GC Wkshps), 2016 IEEE*. IEEE, 2016.

[10] Choi, Jung Il, Mayank Jain, Kannan Srinivasan, Phil Levis, and Sachin Katti. "Achieving single channel, full duplex wireless communication." In Proceedings of the sixteenth annual international conference on Mobile computing and networking, pp. 1-12. ACM, 2010.

[11] El_Mashade, Mohamed B., Ashraf Aboshosha, and Ehab A. Hegazy. "Active and Passive Self-Interference Cancellation Techniques for Full-Duplex Systems in the Next Generation (5G) of Mobile Communication Networks."

[12] Phungamngern, N., P. Uthansakul, and M. Uthansakul. "Digital and RF interference cancellation for single-channel full-duplex transceiver using a single antenna." *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2013 10th International Conference on*. IEEE, 2013.

[13] Ahmed, Elsayed, and Ahmed M. Eltawil. "All-digital self-interference cancellation technique for full-duplex systems." *IEEE Transactions on Wireless Communications* 14.7 (2015): 3519-3532.

[14] van den Broek, Dirk-Jan, Eric AM Klumperink, and Bram Nauta. "An in-band full-duplex radio receiver with a passive vector modulator downmixer for self-interference cancellation." *IEEE journal of solid-state circuits* 50.12 (2015): 3003-3014.

[15] Jain, Mayank, et al. "Practical, real-time, full duplex wireless." *Proceedings of the 17th annual international conference on Mobile computing and networking*. ACM, 2011.
[16] Zhang, Zhongshan, et al. "Full duplex techniques for 5G networks: self-interference cancellation, protocol design, and relay selection." *IEEE Communications Magazine* 53.5 (2015): 128-137.
[17] Duarte, Melissa, Chris Dick, and Ashutosh Sabharwal. "Experiment-driven characterization of full-duplex wireless systems." *IEEE Transactions on Wireless Communications* 11, no. 12 (2012): 4296-4307.
[18] Bharadia, Dinesh, Emily McMilin, and Sachin Katti. "Full duplex radios." *ACM SIGCOMM Computer Communication Review* 43, no. 4 (2013): 375-386.