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Cryogenic Calorimetric Signal Readout with 180nm CMOS at 20 mK

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***Abstract*—We present a demonstration of readout of physical cryogenic calorimetric signals from 20 mK with a two-stage amplifier using 180 nm CMOS technology placed at 20 mK and 700 mK. We observe a number of cryogenic effects in 180 nm CMOS that deviate from typical warm behavior, which are not prohibitive to their cryogenic operation but whose potential impacts we discuss. This represents a new step towards the viability of cryogenic electronics using 180 nm CMOS in cryogenic calorimetric experiments.**

***Index Terms*—Cryogenic, CMOS, NTD, Interface, Calorimeter**

I. Introduction

Cryogenic CMOS are now widely considered an appealing method of interfacing with sensors and quantum information systems that operate in sub-Kelvin cryogenic environments, offering a number of advantages over conventional room temperature electronics chains [1]. In particular, cryogenic electronics offer the opportunity for more precise readout and control of devices in the cryogenic environment by virtue of proximity, improving latency and reducing the impact of noise pickup in the cabling. They also allow for cold multiplexing, significantly reducing the required amount of cryogenic cabling, which could otherwise impose prohibitive thermal loads on a cryogenic setup as channel numbers are scaled up.

These advantages could similarly be useful in large scale deep-cryogenic particle detectors such as CUORE (Cryogenic Underground Observatory for Rare Events) [2], which utilizes the largest dilution fridge in the world [3]. CUORE operates 988 TeO_2 crystals weighing 750 grams each as cryogenic calorimeters with temperatures near 10 mK. Each individual crystal acts as an independent detector that requires its own readout, currently done entirely with room temperature electronics [4]. There are now plans for an upgrade to what will be called CUPID (CUORE Upgrade with Particle ID), which will use the same cryostat as CUORE but further enhance its background rejection capabilities with the addition of light detectors [5]. These future upgrades to CUORE offer the opportunity to introduce cryogenic CMOS into the electronics chain.

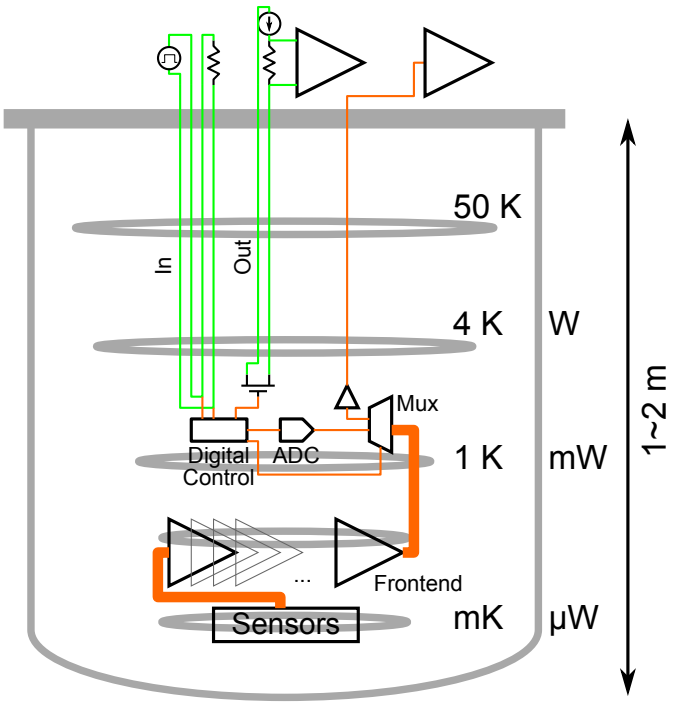

Fig. 1. A possible scheme for cryogenic circuit placement to read signals coming from sensors at the milliKelvin stage of a dilution fridge. Front-end amplifiers are placed as close as possible to the sensors, while supporting electronics can be placed at slightly warmer stages where cooling power is more abundant.

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A schematic of how this could be done in a CUPID-like experiment is shown in Fig. 1. While existing applications of cryogenic CMOS have typically left them at the 4 K stage, we envision additional benefit from pushing the front-end amplifiers down to the mK stage as close to the detector sensors as possible. This presents additional challenges in the form of even tighter power constraints. Other supporting electronics can be placed around 1 K, where cooling power is more plentiful. Given the available cooling power at these stages and the number of ASICs that will be needed, this scheme would limit the ASIC design to O(nW) power per channel and O(mW) for the sum of all supporting electronics at the 1 K stage.

While 180 nm CMOS have shown some unusual behaviors in the deep cryogenic regime, they nonetheless are an appealing option for large-scale applications due to their accessibility and affordability. We present a summary of cryogenic effects that should be accounted for in circuit design, as well as first results demonstrating stable readout of physical light signals with amplifiers using 180 nm CMOS placed at the 700 mK and 20 mK stages of a dilution fridge.

II. Cryogenic Effects in 180 nm CMOS

We leave the details of the typical changes in transconductance, threshold voltages, conductivity, and other basic properties of CMOS that have been previously observed as they are cooled to cryogenic temperatures to the references [6]. We summarize here the hysteretic behaviors seen in a number of MOSFETs, which we expect to impact the behavior of cryogenic amplifiers designed with this technology due to their deviation from the "ideal" behavior of CMOS that one would expect from warm measurements. In large-channel NMOS and PMOS, we observe a difference in drain-source current response depending on whether the drain-source voltage is scanned with increasing or decreasing magnitude, an example of which is shown in Fig. 2.

We also observe a memory effect in several NMOS and PMOS where the channel conductivity at low V_{ds} is initially high when the device is first turned on by its gate voltage. After V_{ds} is increased so that the device enters its saturation regime, it then sees lower channel conductivity after V_{ds} is dropped back to low values. The devices remain in this lower-conductivity state until they are turned off by their gate voltage and then turned back on again. An example of this effect is shown in Fig. 3. A similar bistability was recently seen in 180 nm CMOS at 4 K [7], which provides a model to further study this behavior.

III. Cryogenic Amplifier Setup and Results

We operate a two-stage cryogenic amplifier to read out signals from a light detector operated around 20 mK. The light detector is a thin silicon wafer, which detects light signals by the temperature rise they induce on the wafer when it absorbs the photon energy. The wafer is instrumented with a neutron-transmutation doped (NTD) germanium thermistor that experiences a sharp drop in resistance when its temperature rises,

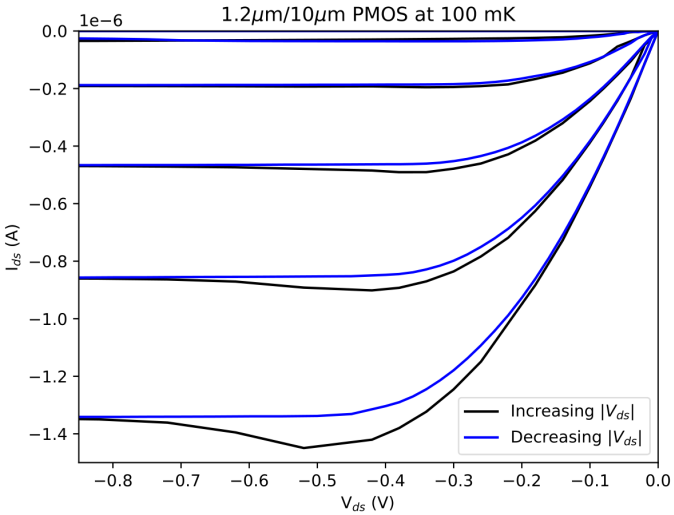

Fig. 2. Hysteresis seen in large-channel MOSFETs at temperatures where charge carrier freeze-out is significant. The I_{ds} response is different depending on whether V_{ds} is scanned with increasing or decreasing magnitude.

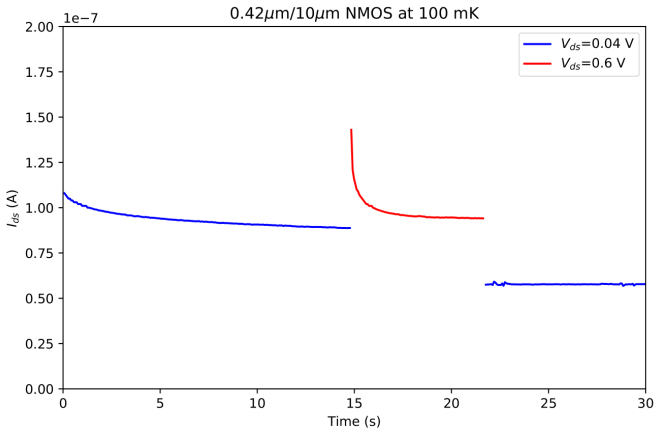

Fig. 3. Two-state behavior of a NMOS seen at 100 mK. The I_{ds} response is higher when the NMOS is first turned on by its gate voltage, but drops to a lower I_{ds} after V_{ds} is increased to the saturation regime and then dropped back down. These states remain stable on long timescales of at least several minutes. This effect is observed in PMOS as well.

corresponding to a voltage signal when an external bias current is applied. We observe typical resistances of O(10 MΩ) in the NTD with bias currents of O(1 nA). An optical fiber is pointed at the silicon wafer to allow the injection of LED pulses from outside the cryostat.

One end of the NTD is directly connected to a front-end pre-amplifier also placed at 20 mK, near the light detector. This pre-amplifier is designed for a gain of around 100 while maintaining low enough power consumption to not disturb cryogenic operations at the mixing chamber where it is located. The output of the pre-amplifier is cabled to the input of a line driver located at the still of the dilution fridge, around 700 mK. This line driver is designed for unity gain with a bandwidth of greater than 1 MHz, which fully captures the calorimetric signals we are considering. The line driver

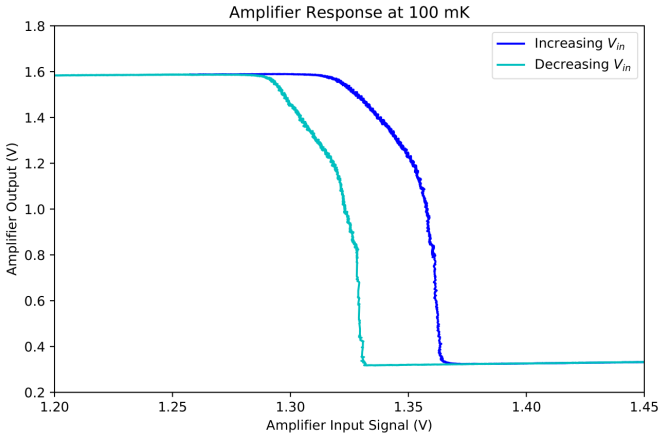

Fig. 4. Pre-amplifier response at 100 mK, showing a shift in the appropriate input voltage bias depending on whether it is approached from high or low V_{in} values. In addition, the region of maximal gain is decreased in size due to the tapering off of the amplifier's output voltage swing, which does not appear at warm.

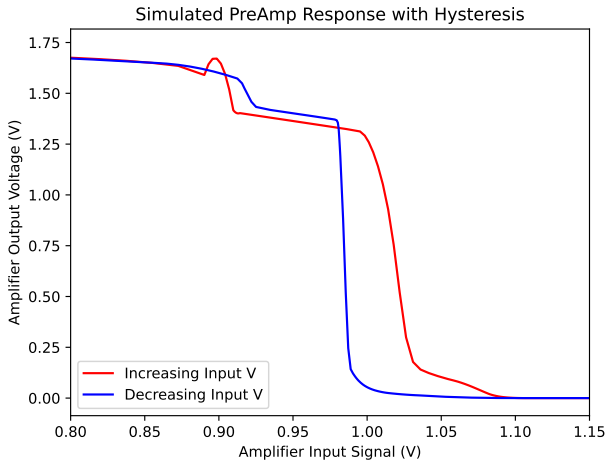

Fig. 5. Simulation of the response of the pre-amplifier measured in Fig. 4, when hysteresis of the MOSFETs is incorporated. The simulation replicates the change in the response depending on whether the input voltage is scanned going up or down, as well as a "shelf" in the output voltage swing. The exact numbers and characteristics are not expected to match, as this model was not precisely tuned to the cryogenic IV characteristics of the MOSFETs.

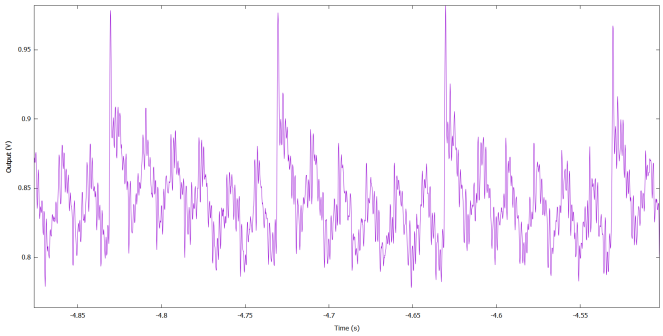

Fig. 6. Output of the two-stage cryogenic amplifier connected to the light detector, while LED pulses are being injected at a rate of 10 Hz. Despite the notable 60 Hz pickup noise, the LED pulses are clearly visible, with an estimated gain of ~ 100 provided by the cryo-amplifier.

then drives the signal up the remaining length of cables to warm readout electronics outside of the fridge.

In characterization measurements of the two-stage amplifier setup, we find that the pre-amplifier exhibits a hysteretic effect depending on whether the input voltage is scanned upwards or downwards, in addition to a decrease in the size of its region of maximal gain, shown in Fig. 4. This separation into two curves is unstable in time, with the amplifier response eventually collapsing if biased along the "wrong" curve, as we would expect if it is related to the cryogenic hysteresis we have observed in the component MOSFETs. We perform a rudimentary incorporation of the hysteresis observed during our MOSFET characterization measurements into a LTspice simulation of the pre-amplifier response, using a memory element to create two response curves for the MOSFETs depending on the direction of the voltage scan. These simulations roughly replicate the observed amplifier behavior at a qualitative level, as seen in Fig. 5. The detailed behavior and the numbers given by the simulation are not expected to be correct since the model is both simple and not tuned, but this suggests that the cryogenic hysteretic behavior of the amplifier is likely attributable to known cryogenic MOSFET behaviors.

With this single-channel two-stage setup, we measure a power draw of 1-5 mA in the line driver at 700 mK with an operating voltage of 1.8 V and bias current of 20 μA. We measure at the same time a power draw of ~ 50 nW in the pre-amplifier at 20 mK with an operating voltage of 1.8 V and bias current of 25 nA. These values are within the cooling power limits of the dilution fridge, and we observe that the general cryogenic environment is stable even with these electronics powered on continuously.

We bias the NTD and amplifier carefully and limit the amplitude of our signal to avoid the effects of the observed hysteresis in this test. Upon injecting LED pulses to the light detector, we observe corresponding physical pulses with a cryogenic gain of about 100 in our readout, shown in Fig. 6. There is significant 60 Hz noise in the results, but study of our setup strongly suggests this is the result of environmental pickup due to a sub-optimal setup for biasing the NTD, and not due to intrinsic characteristics of the cryogenic amplifiers. The noise power spectrum of the two-stage cryogenic amplifier setup's readout is shown in Fig. 7, where the pre-amplifier input is connected to a biased NTD and kept in the sensitive region. We observe that the 60 Hz peak in particular is roughly consistent with the noise we see in the NTD bias setup simply magnified by our expected gain of ~ 100.

IV. Conclusion

We have demonstrated readout of physical light signals on a cryogenic light detector with a two-stage amplifier using 180 nm CMOS at 20 mK and 700 mK. The amplifiers exhibited sufficiently low power dissipation to not disturb the stability

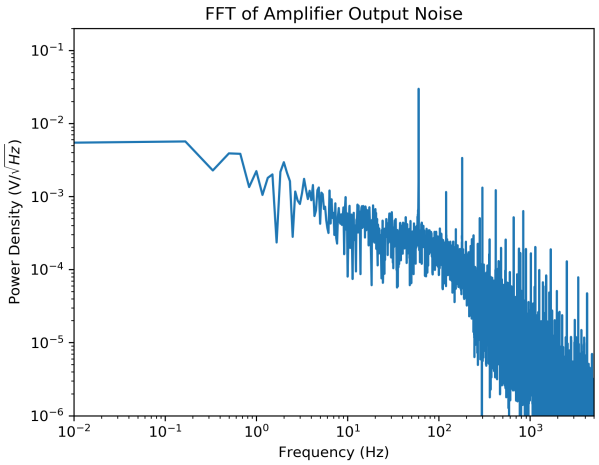

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Fig. 7. Noise power spectral density of the two-stage cryo-amplifier output when its input is connected to a biased NTD, without light signals being injected. There is a significant peak at 60 Hz, as expected from the data observed in Fig. 6, but it does not spoil the rest of the spectrum and its magnitude is consistent with what we expect from the amplified input noise.

of the cryogenic environment, while yielding an overall gain of ~ 100. We observe some non-idealities in the cryogenic behavior of the amplifiers, which are understood to be related to previously seen cryogenic behaviors of the component MOSFETs. These require further study, but do not seem to be prohibitive to the operation of these amplifiers in deep cryogenic conditions.

Future work will focus on improving the general noise conditions in the testing environment, to allow for more precise study of the amplifier characteristics. Future iterations of the amplifier designs will look at furthering decreasing their power consumption, as well as working with the different cryogenic behaviors.

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